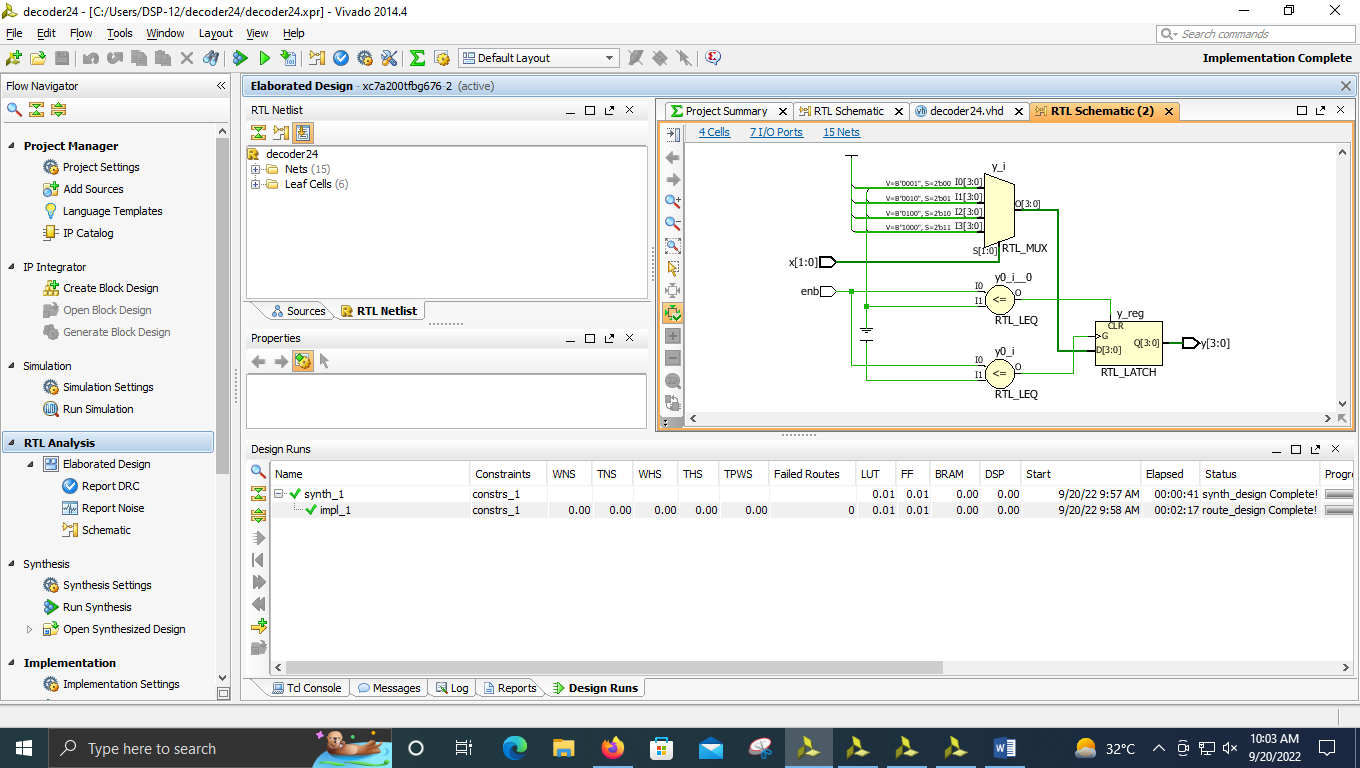
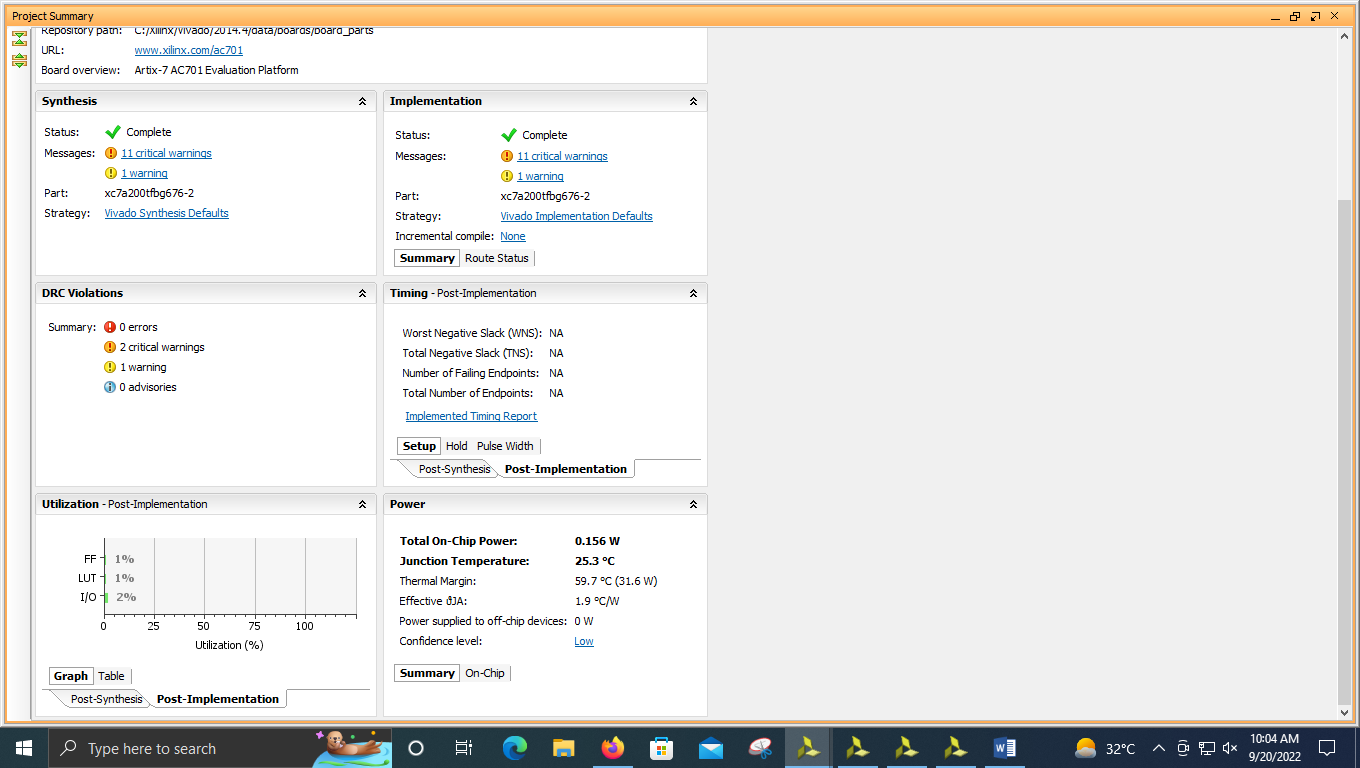
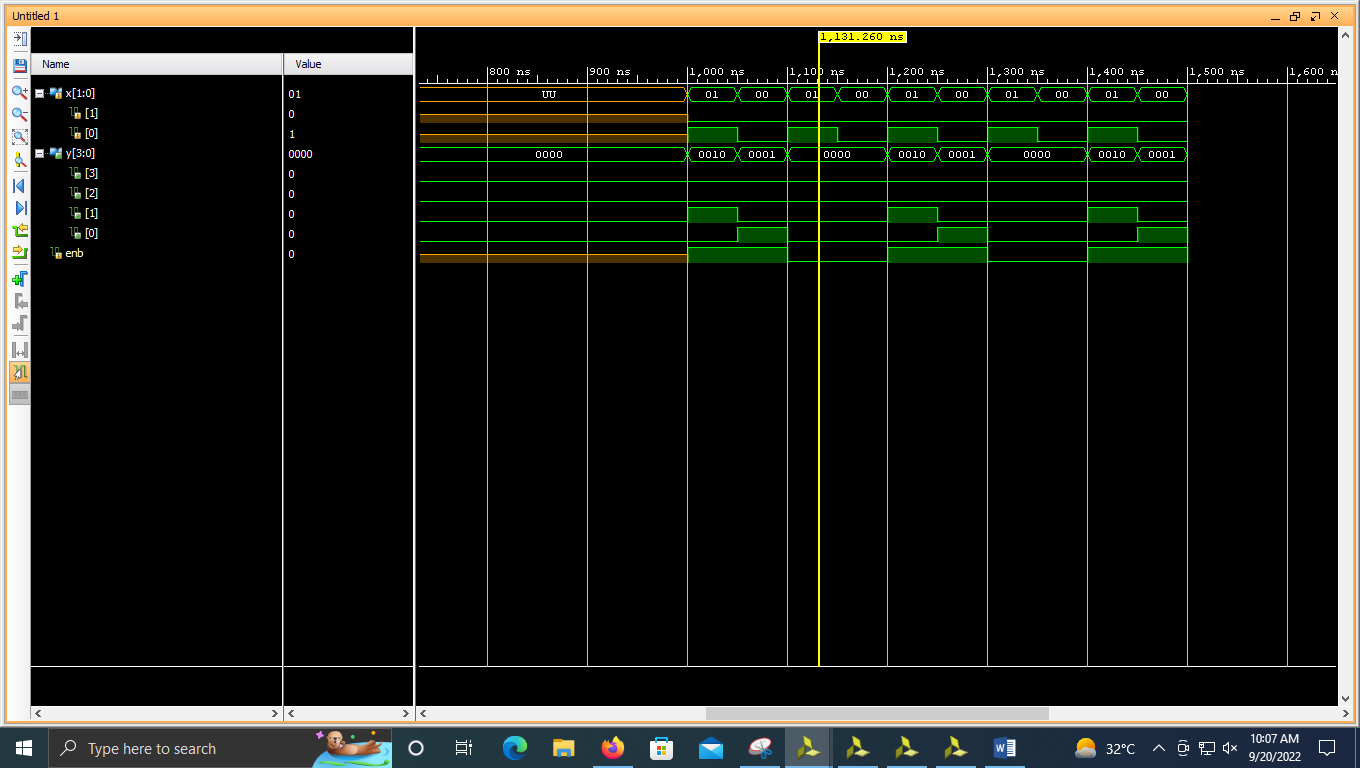
1)







**----------------------------------------------------------------------------------**

**-- Company:**

**-- Engineer:**

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**-- Create Date: 09/20/2022 09:34:58 AM**

**-- Design Name:**

**-- Module Name: decoder24 - Behavioral**

**-- Project Name:**

**-- Target Devices:**

**-- Tool Versions:**

**-- Description:**

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**-- Dependencies:**

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**-- Revision:**

**-- Revision 0.01 - File Created**

**-- Additional Comments:**

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**----------------------------------------------------------------------------------**

**library IEEE;**

**use IEEE.STD\_LOGIC\_1164.ALL;**

**-- Uncomment the following library declaration if using**

**-- arithmetic functions with Signed or Unsigned values**

**--use IEEE.NUMERIC\_STD.ALL;**

**-- Uncomment the following library declaration if instantiating**

**-- any Xilinx leaf cells in this code.**

**--library UNISIM;**

**--use UNISIM.VComponents.all;**

**entity decoder24 is**

**Port ( x : in STD\_LOGIC\_VECTOR (1 downto 0);**

**y : out STD\_LOGIC\_VECTOR (3 downto 0);**

**enb : in STD\_LOGIC);**

**end decoder24;**

**architecture Behavioral of decoder24 is**

**begin**

**process(x,enb)**

**begin**

**if enb <= '0' then y<="0000";**

**elsif enb <= '1' then**

**case x is**

**when "00" => y<= "0001";**

**when "01" => y<= "0010";**

**when "10" => y<= "0100";**

**when "11" => y<= "1000";**

**when others => y<="----";**

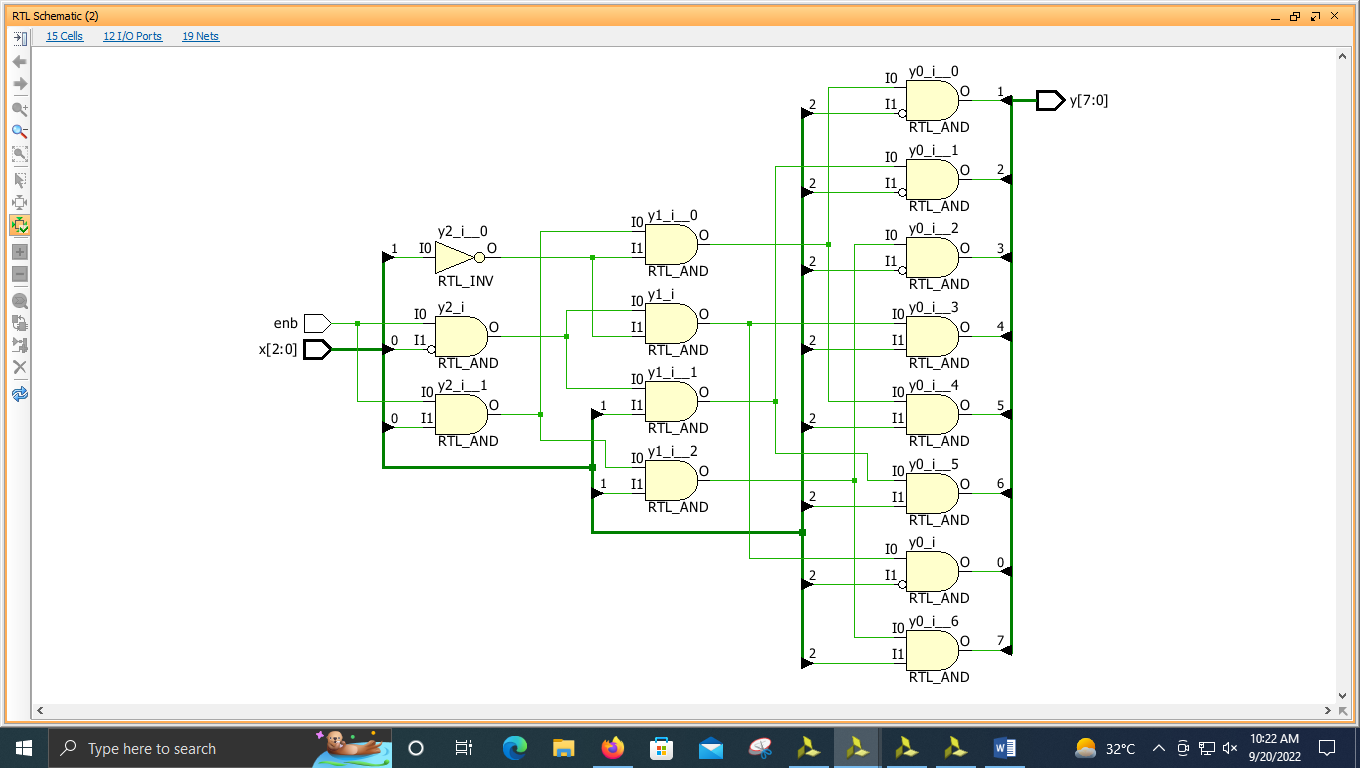
**end case;**

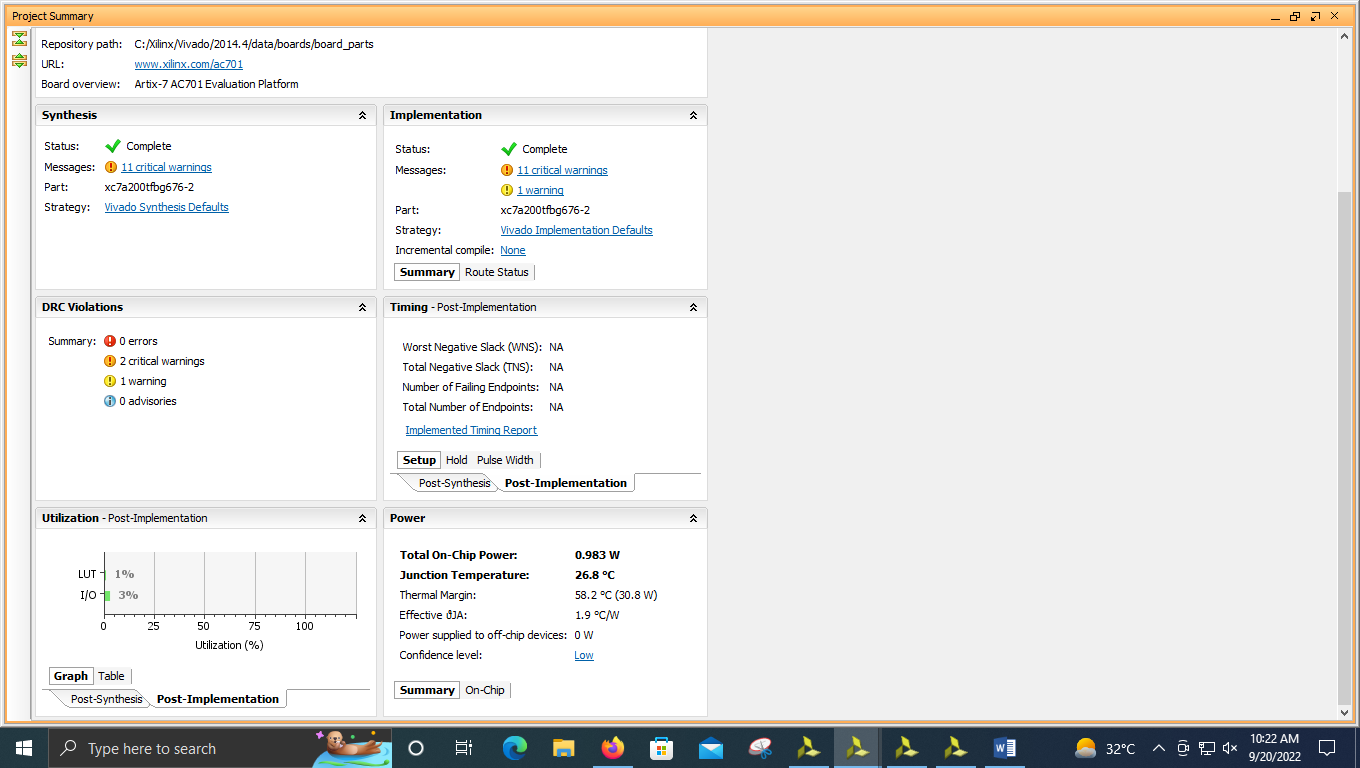
**end if;**

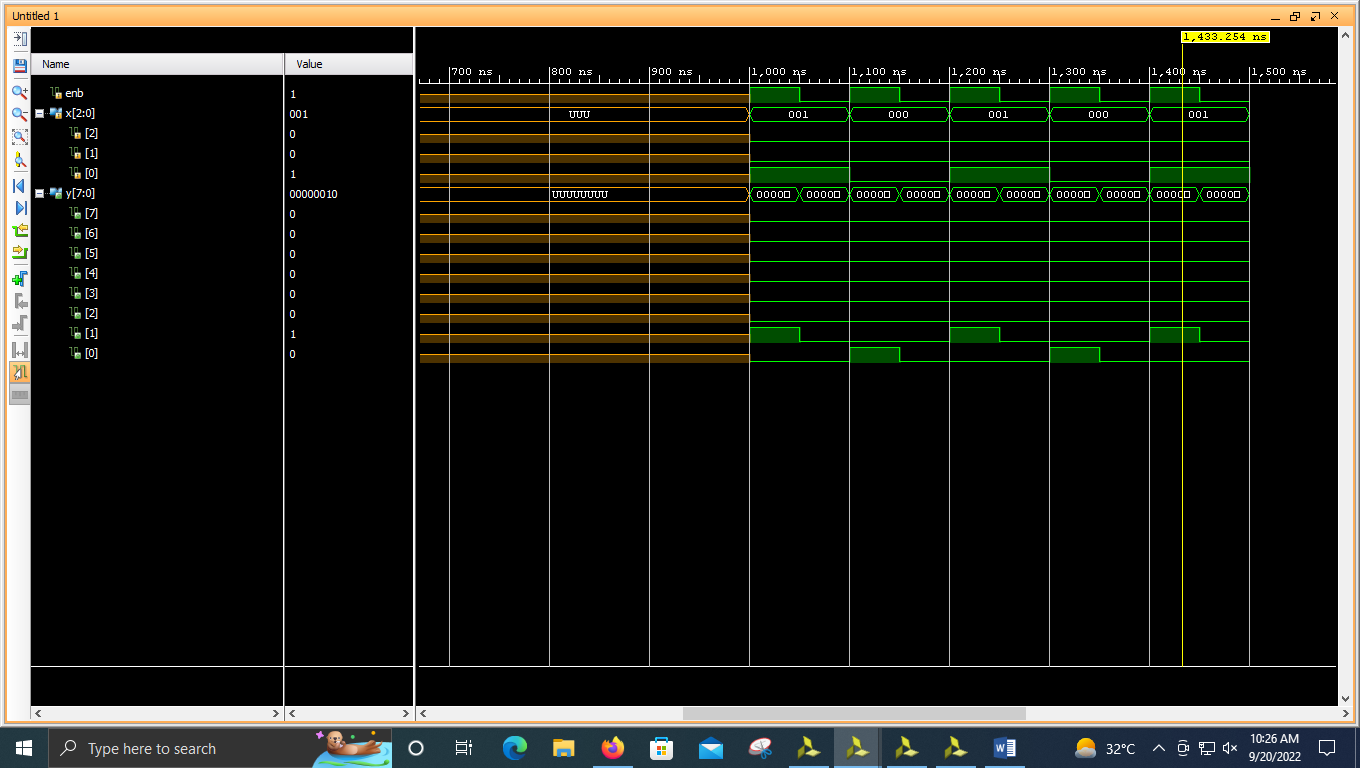
**end process;**

**end Behavioral;**

**2)**







**----------------------------------------------------------------------------------**

**-- Company:**

**-- Engineer:**

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**-- Create Date: 09/20/2022 10:00:07 AM**

**-- Design Name:**

**-- Module Name: decoder38 - Behavioral**

**-- Project Name:**

**-- Target Devices:**

**-- Tool Versions:**

**-- Description:**

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**-- Dependencies:**

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**-- Revision:**

**-- Revision 0.01 - File Created**

**-- Additional Comments:**

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**----------------------------------------------------------------------------------**

**library IEEE;**

**use IEEE.STD\_LOGIC\_1164.ALL;**

**-- Uncomment the following library declaration if using**

**-- arithmetic functions with Signed or Unsigned values**

**--use IEEE.NUMERIC\_STD.ALL;**

**-- Uncomment the following library declaration if instantiating**

**-- any Xilinx leaf cells in this code.**

**--library UNISIM;**

**--use UNISIM.VComponents.all;**

**entity decoder38 is**

**Port ( enb : in STD\_LOGIC;**

**x : in STD\_LOGIC\_VECTOR (2 downto 0);**

**y : out STD\_LOGIC\_VECTOR (7 downto 0));**

**end decoder38;**

**architecture Behavioral of decoder38 is**

**begin**

**y(0)<=(enb and not(x(0)) and not(x(1)) and not(x(2)));**

**y(1)<=(enb and (x(0)) and not(x(1)) and not(x(2)));**

**y(2)<=(enb and not(x(0)) and (x(1)) and not(x(2)));**

**y(3)<=(enb and (x(0)) and (x(1)) and not(x(2)));**

**y(4)<=(enb and not(x(0)) and not(x(1)) and (x(2)));**

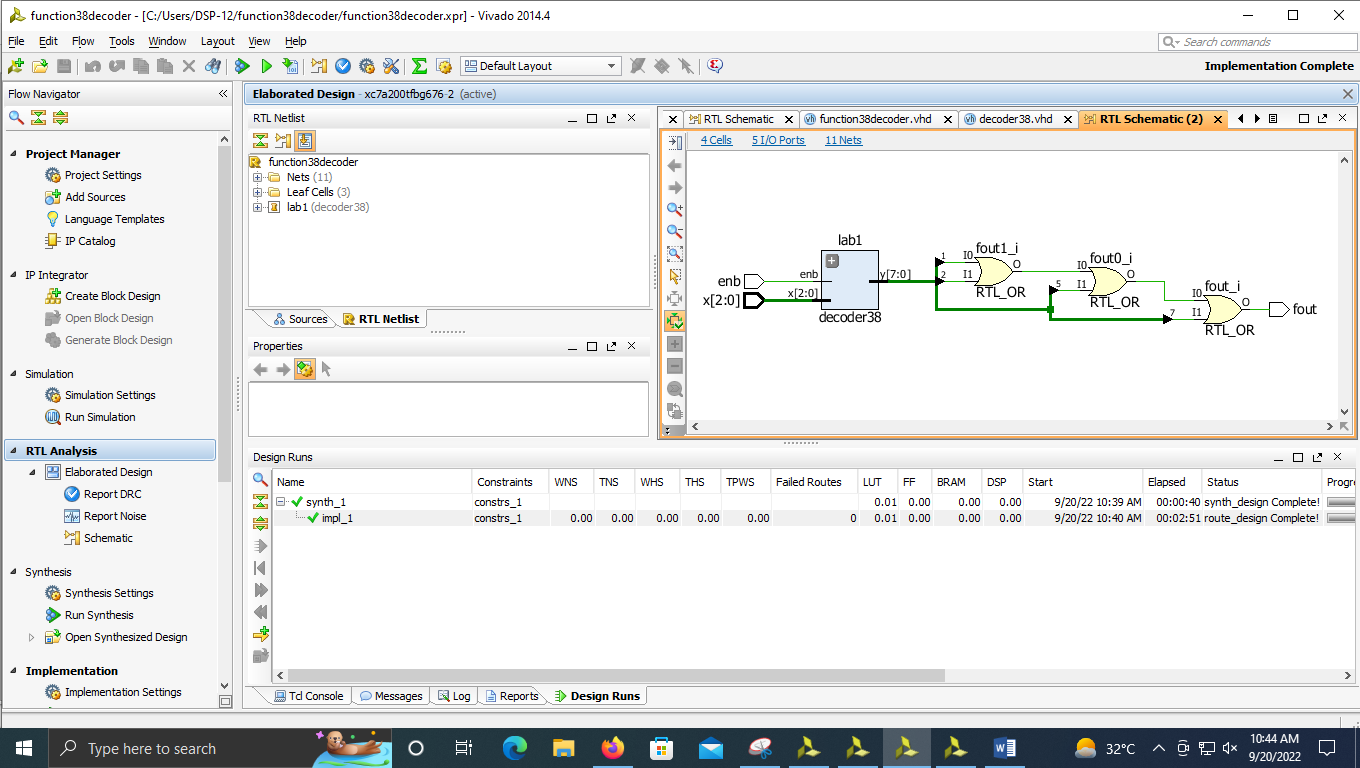
**y(5)<=(enb and (x(0)) and not(x(1)) and (x(2)));**

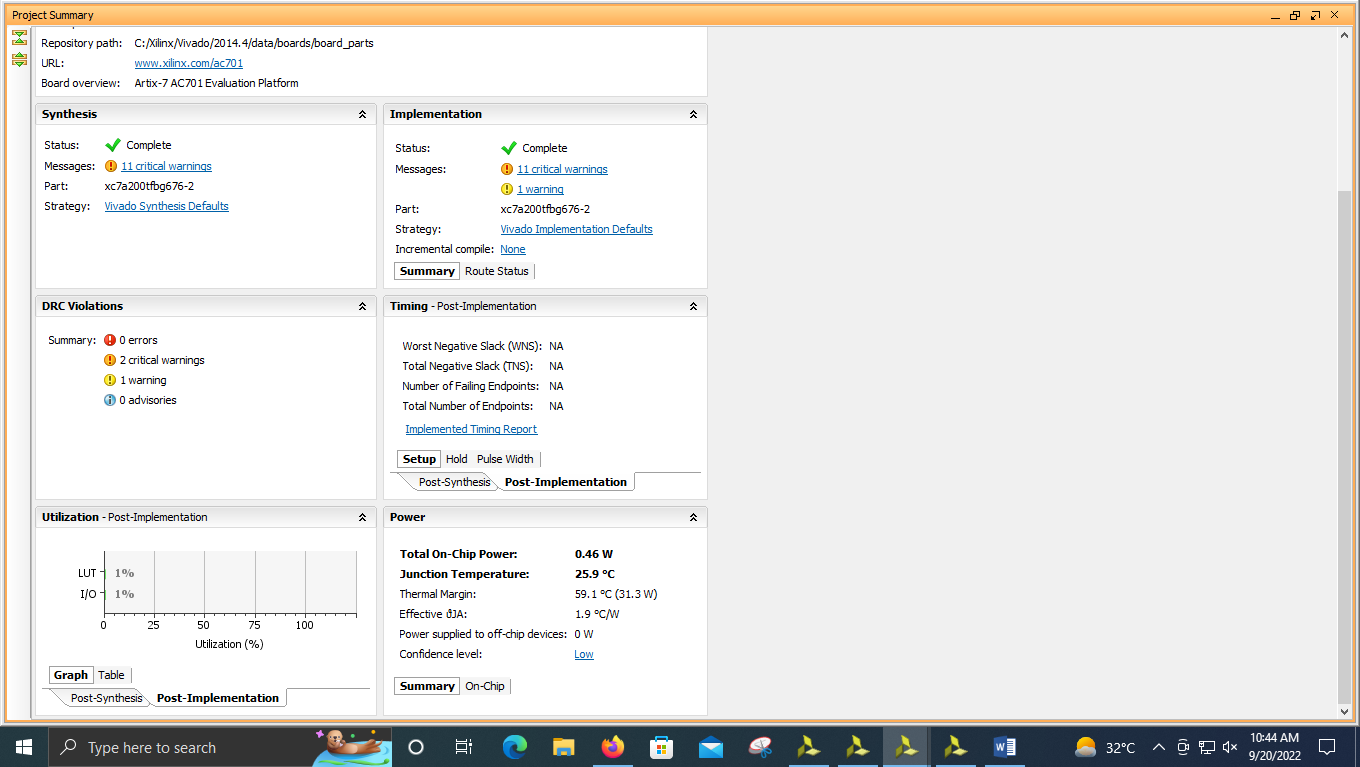
**y(6)<=(enb and not(x(0)) and (x(1)) and (x(2)));**

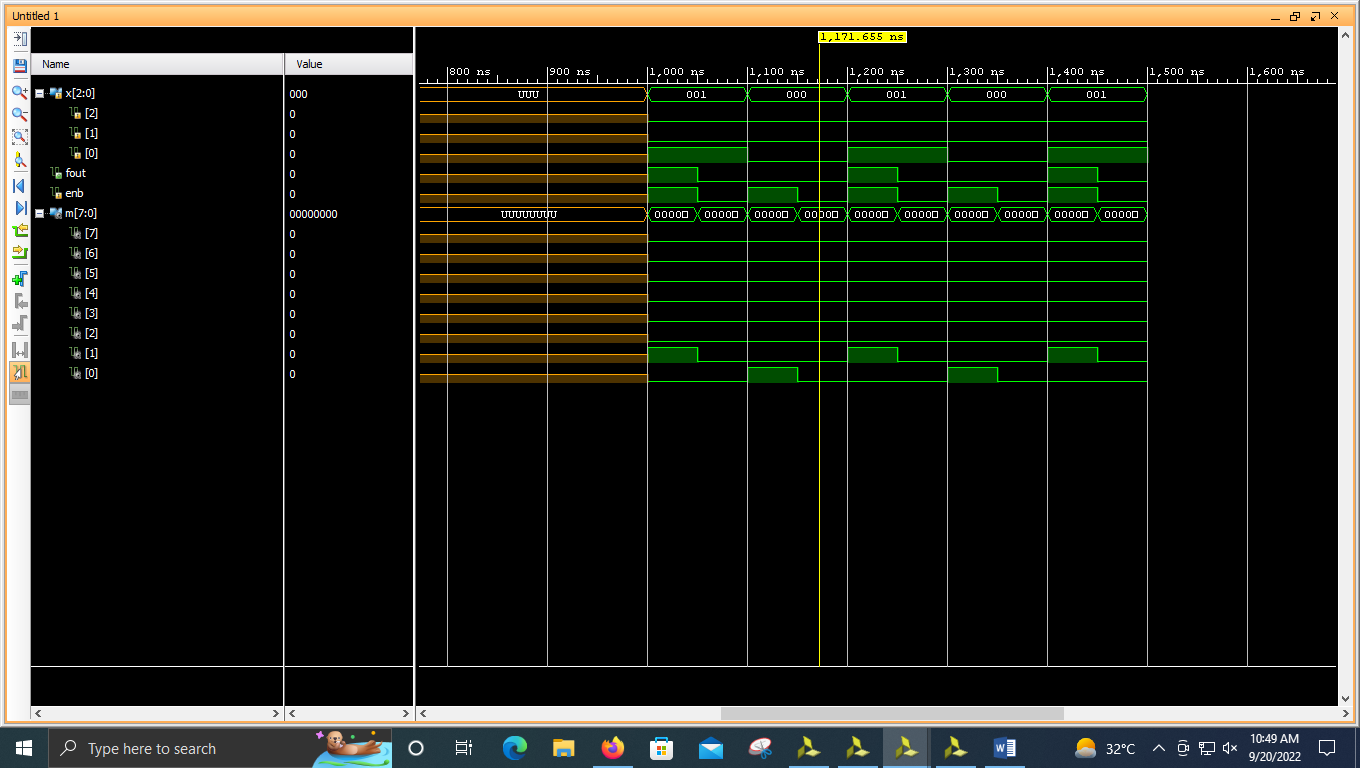
**y(7)<=(enb and (x(0)) and (x(1)) and (x(2)));**

**end Behavioral;**

**3)**







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**-- Company:**

**-- Engineer:**

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**-- Create Date: 09/20/2022 10:21:47 AM**

**-- Design Name:**

**-- Module Name: function38decoder - Behavioral**

**-- Project Name:**

**-- Target Devices:**

**-- Tool Versions:**

**-- Description:**

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**-- Dependencies:**

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**-- Revision:**

**-- Revision 0.01 - File Created**

**-- Additional Comments:**

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**----------------------------------------------------------------------------------**

**library IEEE;**

**use IEEE.STD\_LOGIC\_1164.ALL;**

**-- Uncomment the following library declaration if using**

**-- arithmetic functions with Signed or Unsigned values**

**--use IEEE.NUMERIC\_STD.ALL;**

**-- Uncomment the following library declaration if instantiating**

**-- any Xilinx leaf cells in this code.**

**--library UNISIM;**

**--use UNISIM.VComponents.all;**

**entity function38decoder is**

**Port ( x : in STD\_LOGIC\_VECTOR (2 downto 0);**

**fout : out STD\_LOGIC;**

**enb : in STD\_LOGIC);**

**end function38decoder;**

**architecture Behavioral of function38decoder is**

**component decoder38 is**

**Port ( enb : in STD\_LOGIC;**

**x : in STD\_LOGIC\_VECTOR (2 downto 0);**

**y : out STD\_LOGIC\_VECTOR (7 downto 0));**

**end component;**

**signal m:STD\_LOGIC\_VECTOR(7 downto 0);**

**begin**

**lab1 : decoder38 port map(enb,x(2 downto 0),m(7 downto 0));**

**fout <= m(1) or m(2) or m(5) OR m(7);**

**end Behavioral;**

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**-- Company:**

**-- Engineer:**

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**-- Create Date: 09/20/2022 10:28:06 AM**

**-- Design Name:**

**-- Module Name: decoder38 - Behavioral**

**-- Project Name:**

**-- Target Devices:**

**-- Tool Versions:**

**-- Description:**

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**-- Dependencies:**

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**-- Revision:**

**-- Revision 0.01 - File Created**

**-- Additional Comments:**

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**----------------------------------------------------------------------------------**

**library IEEE;**

**use IEEE.STD\_LOGIC\_1164.ALL;**

**-- Uncomment the following library declaration if using**

**-- arithmetic functions with Signed or Unsigned values**

**--use IEEE.NUMERIC\_STD.ALL;**

**-- Uncomment the following library declaration if instantiating**

**-- any Xilinx leaf cells in this code.**

**--library UNISIM;**

**--use UNISIM.VComponents.all;**

**entity decoder38 is**

**Port ( enb : in STD\_LOGIC;**

**x : in STD\_LOGIC\_VECTOR (2 downto 0);**

**y : out STD\_LOGIC\_VECTOR (7 downto 0));**

**end decoder38;**

**architecture Behavioral of decoder38 is**

**begin**

**y(0)<=(enb and not(x(0)) and not(x(1)) and not(x(2)));**

**y(1)<=(enb and (x(0)) and not(x(1)) and not(x(2)));**

**y(2)<=(enb and not(x(0)) and (x(1)) and not(x(2)));**

**y(3)<=(enb and (x(0)) and (x(1)) and not(x(2)));**

**y(4)<=(enb and not(x(0)) and not(x(1)) and (x(2)));**

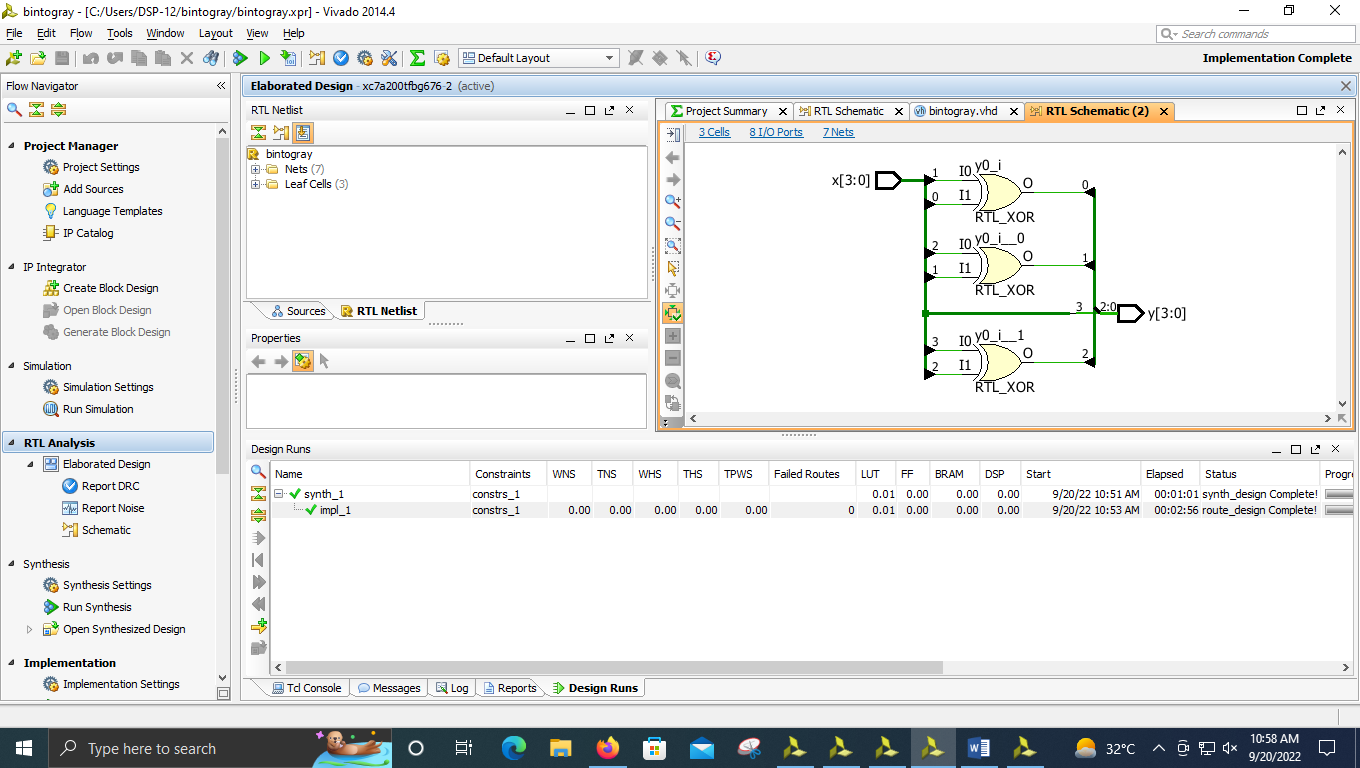
**y(5)<=(enb and (x(0)) and not(x(1)) and (x(2)));**

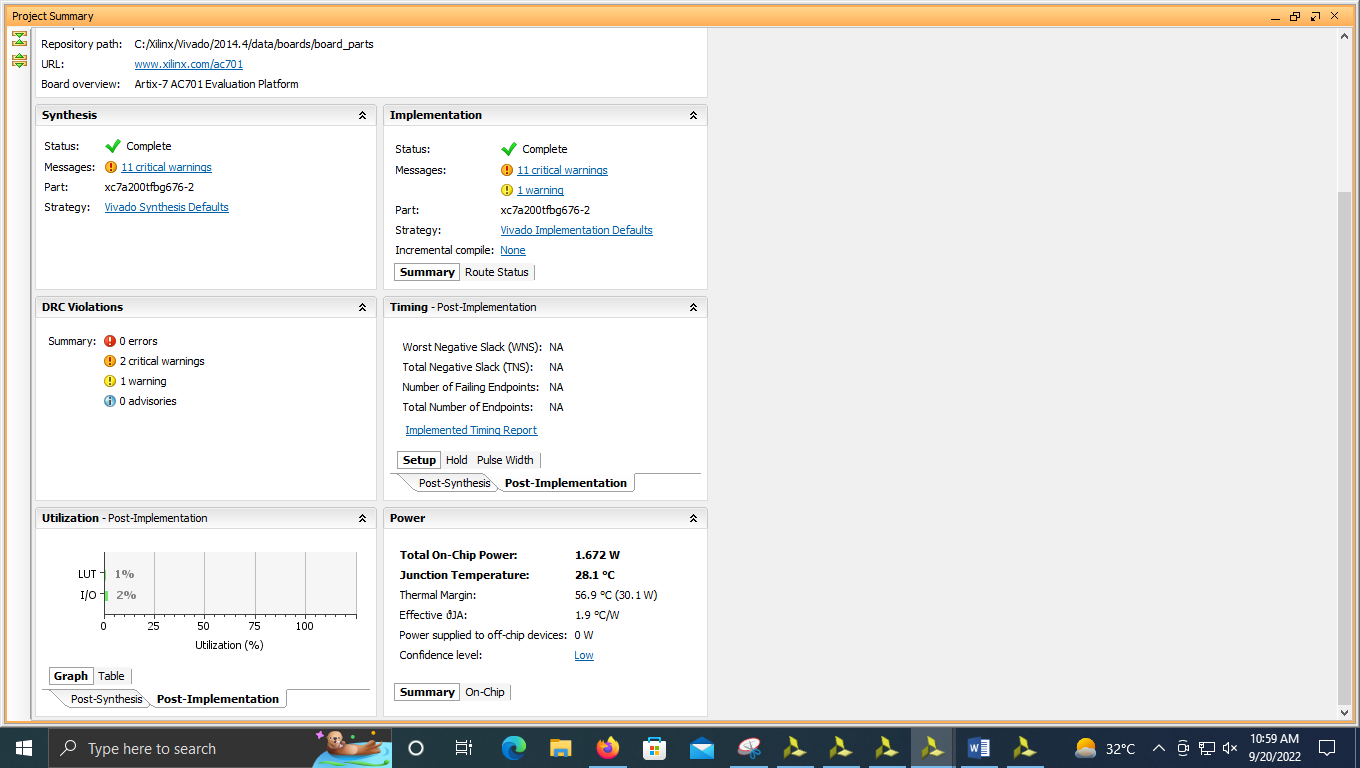
**y(6)<=(enb and not(x(0)) and (x(1)) and (x(2)));**

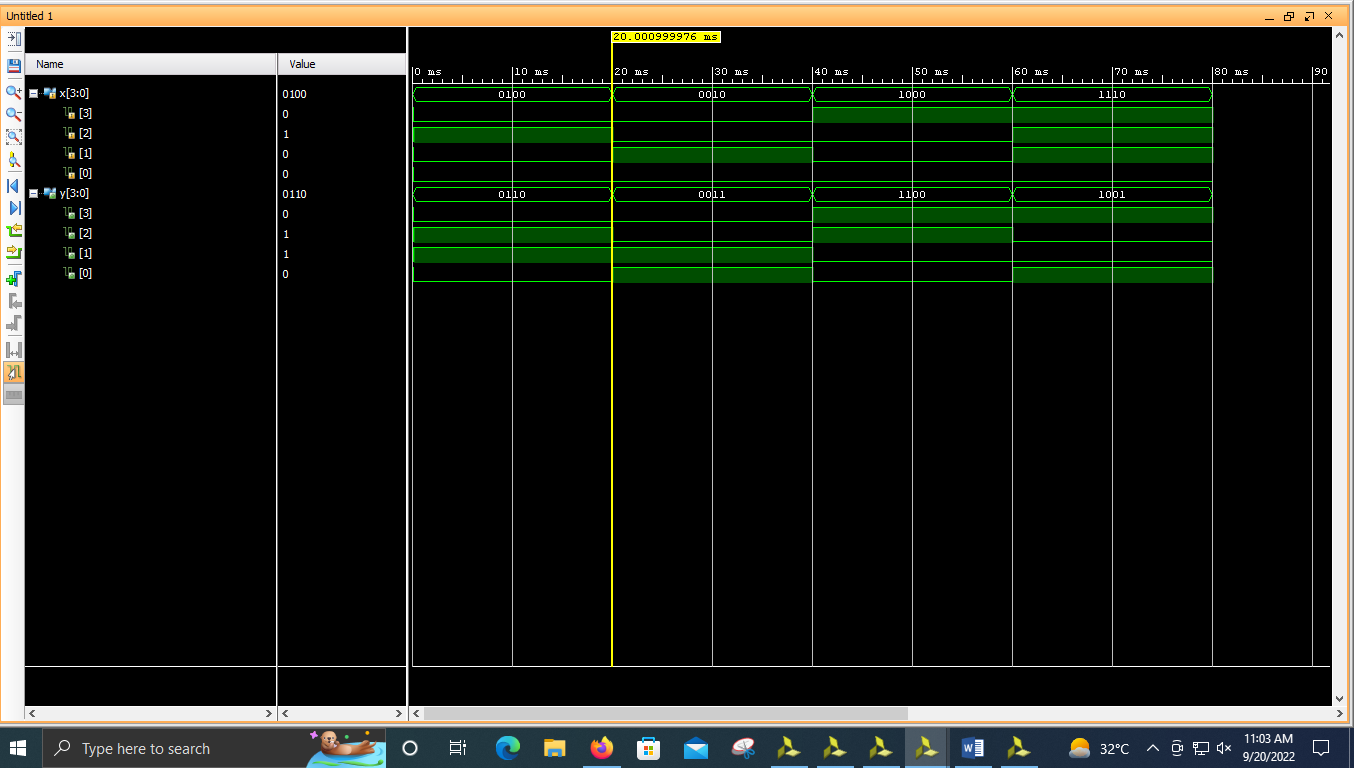
**y(7)<=(enb and (x(0)) and (x(1)) and (x(2)));**

**end Behavioral;**

**4)**







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**-- Company:**

**-- Engineer:**

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**-- Create Date: 09/20/2022 10:43:26 AM**

**-- Design Name:**

**-- Module Name: bintogray - Behavioral**

**-- Project Name:**

**-- Target Devices:**

**-- Tool Versions:**

**-- Description:**

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**-- Dependencies:**

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**-- Revision:**

**-- Revision 0.01 - File Created**

**-- Additional Comments:**

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**----------------------------------------------------------------------------------**

**library IEEE;**

**use IEEE.STD\_LOGIC\_1164.ALL;**

**-- Uncomment the following library declaration if using**

**-- arithmetic functions with Signed or Unsigned values**

**--use IEEE.NUMERIC\_STD.ALL;**

**-- Uncomment the following library declaration if instantiating**

**-- any Xilinx leaf cells in this code.**

**--library UNISIM;**

**--use UNISIM.VComponents.all;**

**entity bintogray is**

**Port ( x : in STD\_LOGIC\_VECTOR (3 downto 0);**

**y : out STD\_LOGIC\_VECTOR (3 downto 0));**

**end bintogray;**

**architecture Behavioral of bintogray is**

**begin**

**y(3)<=x(3);**

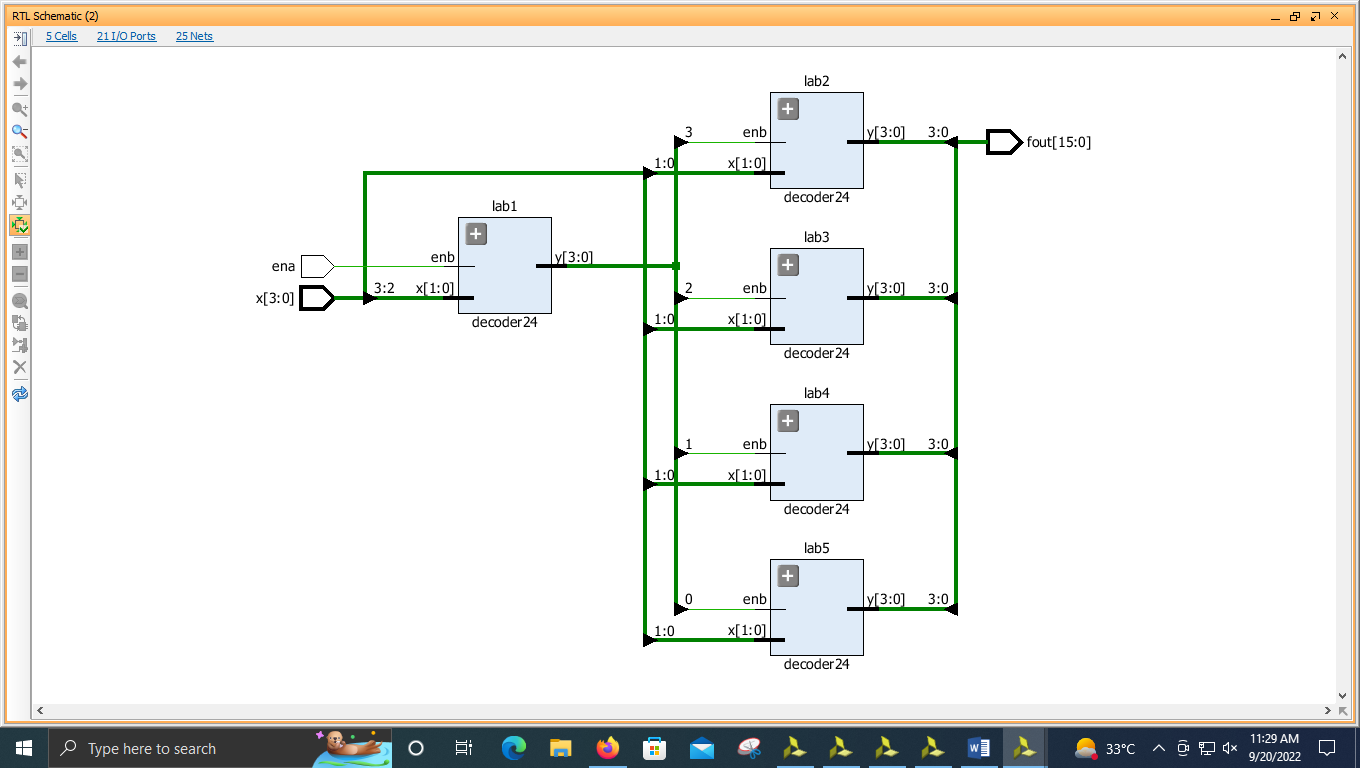
**y(2)<=x(3) xor x(2);**

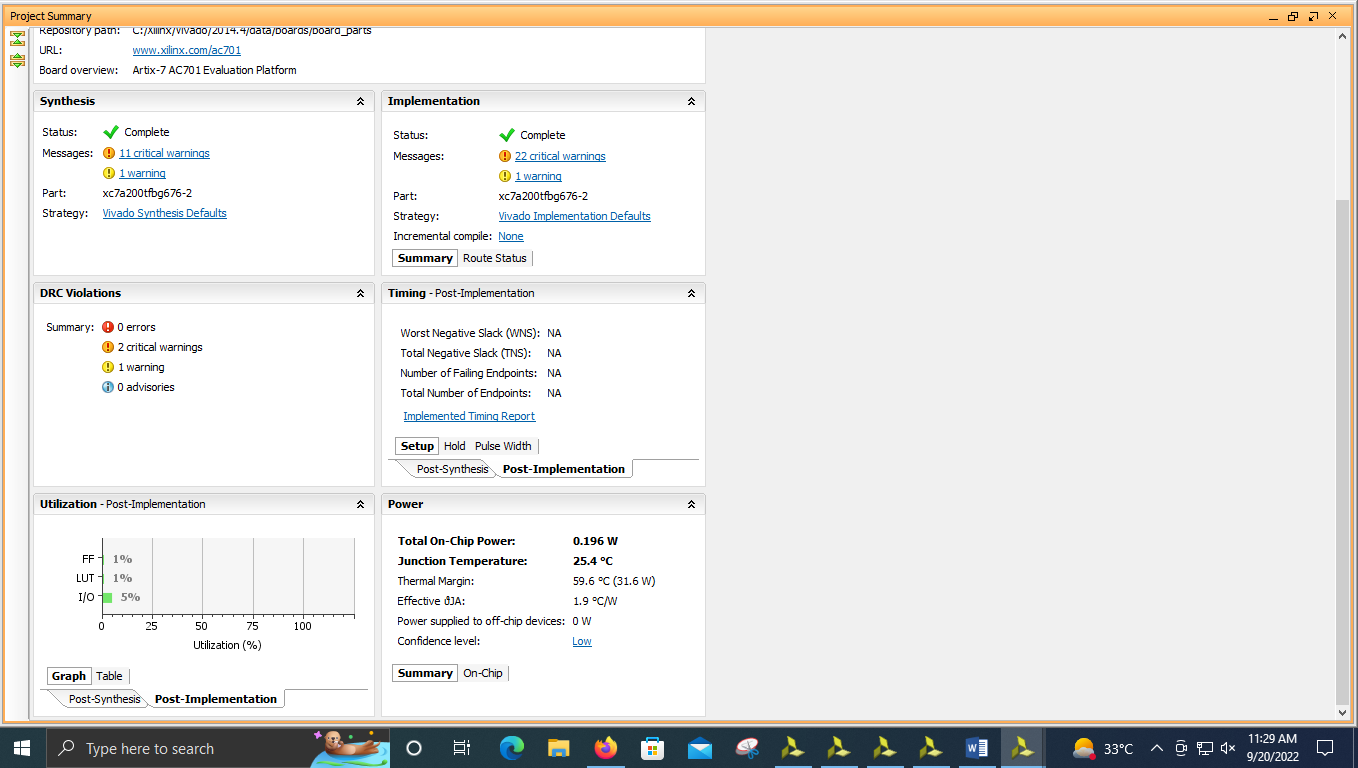
**y(1)<=x(2) xor x(1);**

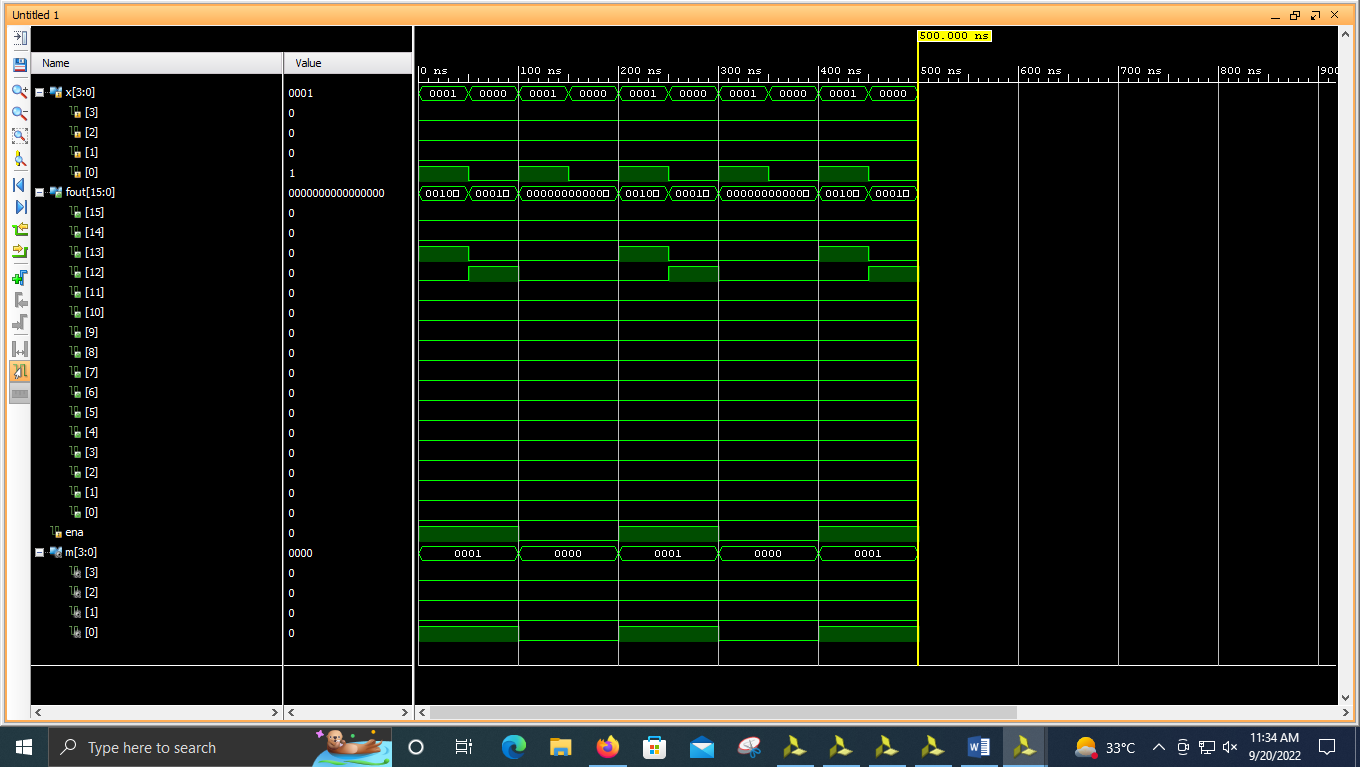
**y(0)<=x(1) xor x(0);**

**end Behavioral;**

**5)**







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**-- Company:**

**-- Engineer:**

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**-- Create Date: 09/20/2022 11:05:12 AM**

**-- Design Name:**

**-- Module Name: decoder416 - Behavioral**

**-- Project Name:**

**-- Target Devices:**

**-- Tool Versions:**

**-- Description:**

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**-- Dependencies:**

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**-- Revision:**

**-- Revision 0.01 - File Created**

**-- Additional Comments:**

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**----------------------------------------------------------------------------------**

**library IEEE;**

**use IEEE.STD\_LOGIC\_1164.ALL;**

**-- Uncomment the following library declaration if using**

**-- arithmetic functions with Signed or Unsigned values**

**--use IEEE.NUMERIC\_STD.ALL;**

**-- Uncomment the following library declaration if instantiating**

**-- any Xilinx leaf cells in this code.**

**--library UNISIM;**

**--use UNISIM.VComponents.all;**

**entity decoder416 is**

**Port ( x : in STD\_LOGIC\_VECTOR (3 downto 0);**

**fout : out STD\_LOGIC\_VECTOR (15 downto 0);**

**ena : in STD\_LOGIC);**

**end decoder416;**

**architecture Behavioral of decoder416 is**

**component decoder24 is**

**Port ( x : in STD\_LOGIC\_VECTOR (1 downto 0);**

**y : out STD\_LOGIC\_VECTOR (3 downto 0);**

**enb : in STD\_LOGIC);**

**end component;**

**signal m: STD\_LOGIC\_VECTOR(3 downto 0);**

**begin**

**lab1 : decoder24 port map(x(3 downto 2),m(3 downto 0),ena);**

**lab2 : decoder24 port map(x(1 downto 0),fout(3 downto 0),m(3));**

**lab3 : decoder24 port map(x(1 downto 0),fout(7 downto 4),m(2));**

**lab4 : decoder24 port map(x(1 downto 0),fout(11 downto 8),m(1));**

**lab5 : decoder24 port map(x(1 downto 0),fout(15 downto 12),m(0));**

**end Behavioral;**

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**-- Company:**

**-- Engineer:**

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**-- Create Date: 09/20/2022 11:06:15 AM**

**-- Design Name:**

**-- Module Name: decoder24 - Behavioral**

**-- Project Name:**

**-- Target Devices:**

**-- Tool Versions:**

**-- Description:**

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**-- Dependencies:**

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**-- Revision:**

**-- Revision 0.01 - File Created**

**-- Additional Comments:**

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**----------------------------------------------------------------------------------**

**library IEEE;**

**use IEEE.STD\_LOGIC\_1164.ALL;**

**-- Uncomment the following library declaration if using**

**-- arithmetic functions with Signed or Unsigned values**

**--use IEEE.NUMERIC\_STD.ALL;**

**-- Uncomment the following library declaration if instantiating**

**-- any Xilinx leaf cells in this code.**

**--library UNISIM;**

**--use UNISIM.VComponents.all;**

**entity decoder24 is**

**Port ( x : in STD\_LOGIC\_VECTOR (1 downto 0);**

**y : out STD\_LOGIC\_VECTOR (3 downto 0);**

**enb : in STD\_LOGIC);**

**end decoder24;**

**architecture Behavioral of decoder24 is**

**begin**

**process(x,enb)**

**begin**

**if enb <= '0' then y<="0000";**

**elsif enb <= '1' then**

**case x is**

**when "00" => y<= "0001";**

**when "01" => y<= "0010";**

**when "10" => y<= "0100";**

**when "11" => y<= "1000";**

**when others => y<="----";**

**end case;**

**end if;**

**end process;**

**end Behavioral;**