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**Winter Semester 2022-2023**

**ASIC Theory Digital Assignment - I**

**M. Tech VLSI Design**

**School of Electronics Engineering**

**Vellore Institute of Technology**

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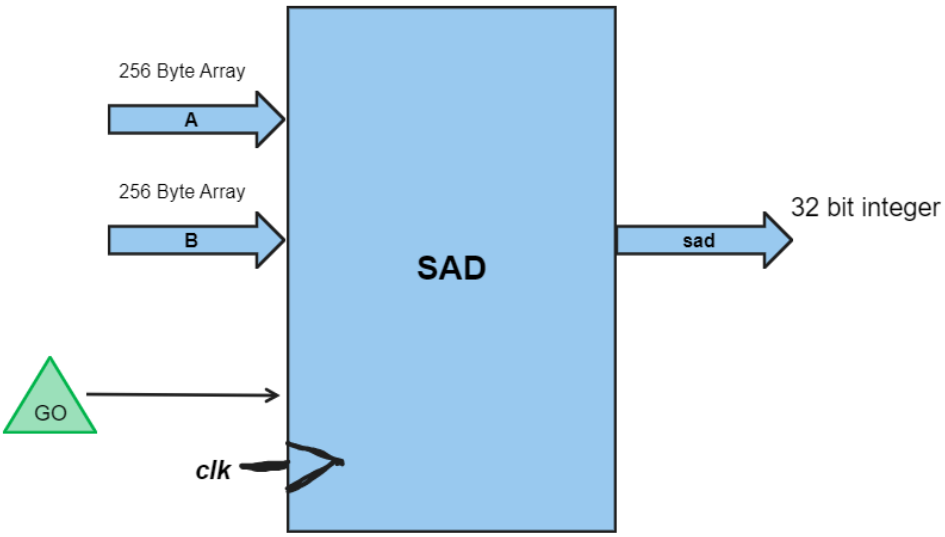
## Objective:

To design an Architectural block, State diagram and control signals of a SAD module (Sum of Absolute Differences) containing a Data path and Control path logic.

**Theory:-** In digital image processing, the sum of absolute differences (SAD) is a measure of the similarity between image blocks. It is calculated by taking the absolute difference between each pixel in the original block and the corresponding pixel in the block being used for comparison. These differences are summed to create a simple metric of block similarity.

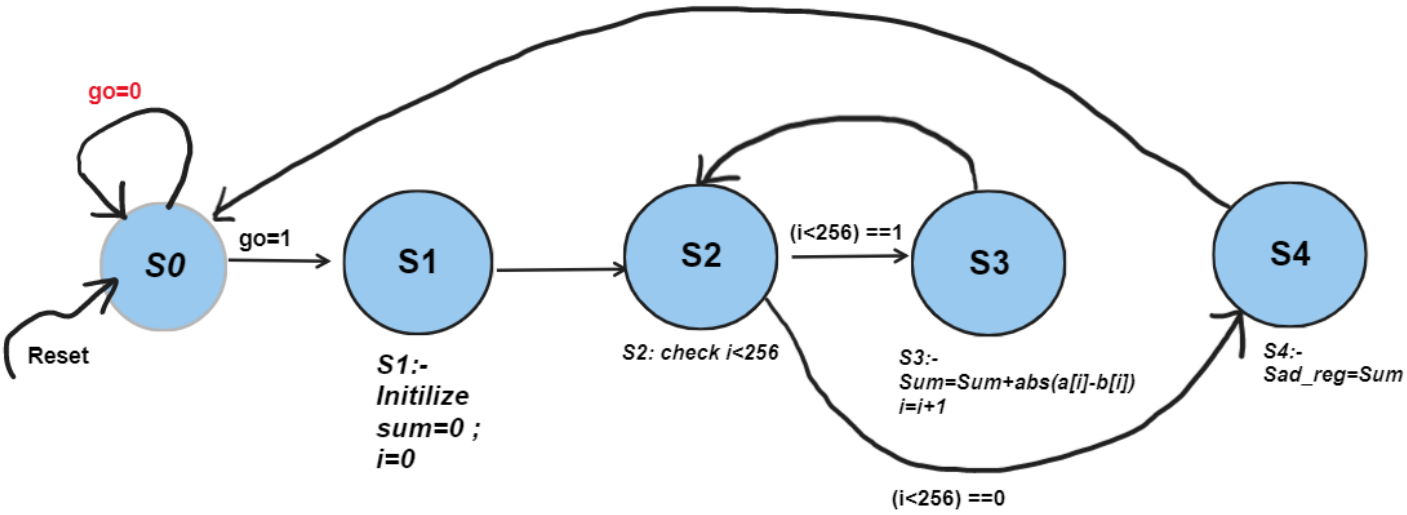
The sum of absolute differences can be used for a variety of purposes, such as object recognition, the generation of disparity maps for stereo images, and motion estimation for video compression.

## Architecture Block:



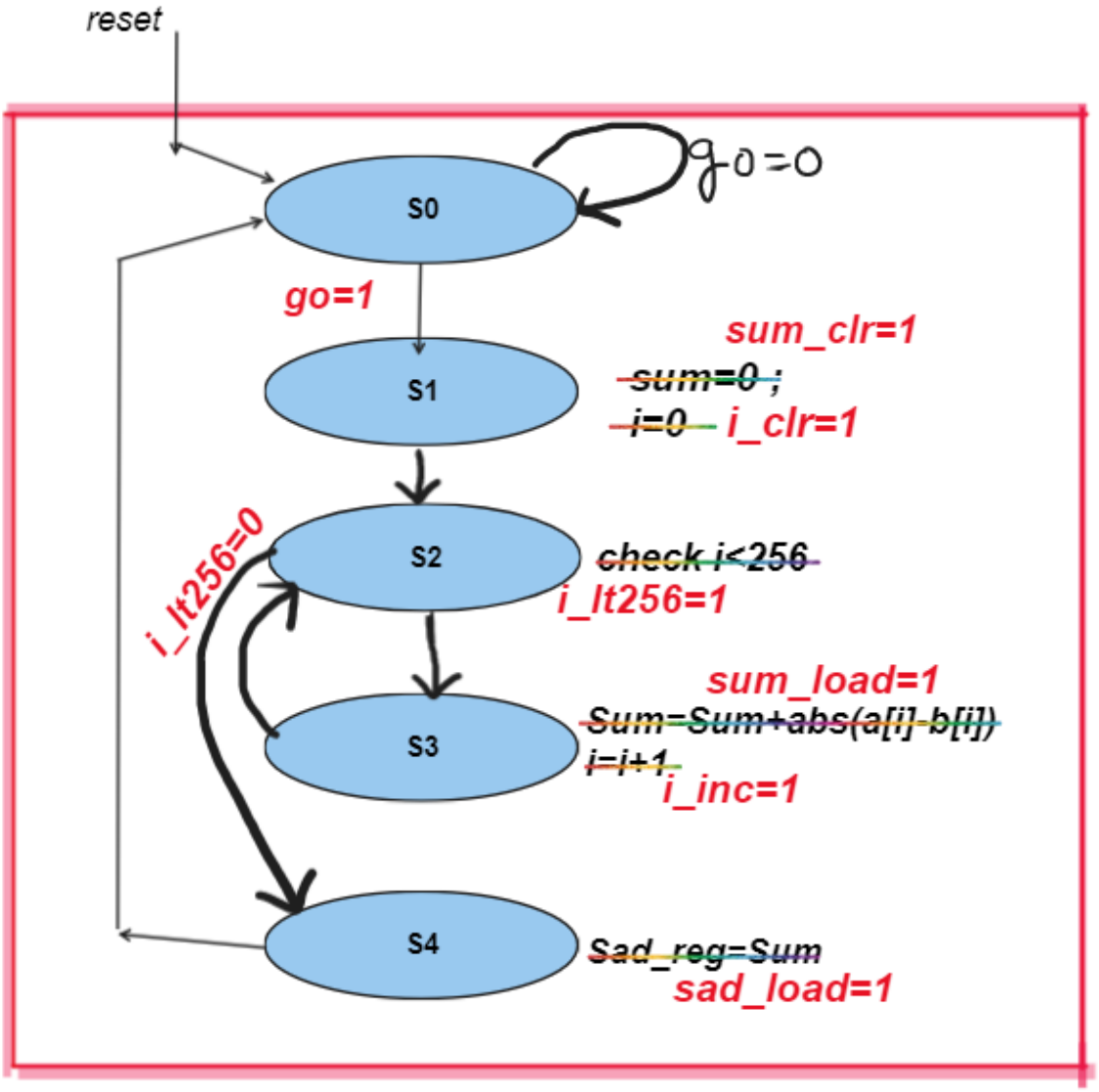

- Inputs: A, B (256-byte memory array)
  go signal (1'bit),clk
- Outputs: Sad (32-bit integer)

**State Diagram:**




- **S0**:- Wait for ***"go"***
- **S1**:- Initialize for ***"Sum=0 & i=0"***
- **S2**:- Check for ***"(i<=256)"***
- **S3**:- 1. Perform abs(a[i]-b[i])
  2. ***sum=sum+ abs(a[i]-b[i])***
  3. ***i=i+1***
- **S4**:- Write output "***sum to Sad_reg***"

## CONTROLLER FSM:-

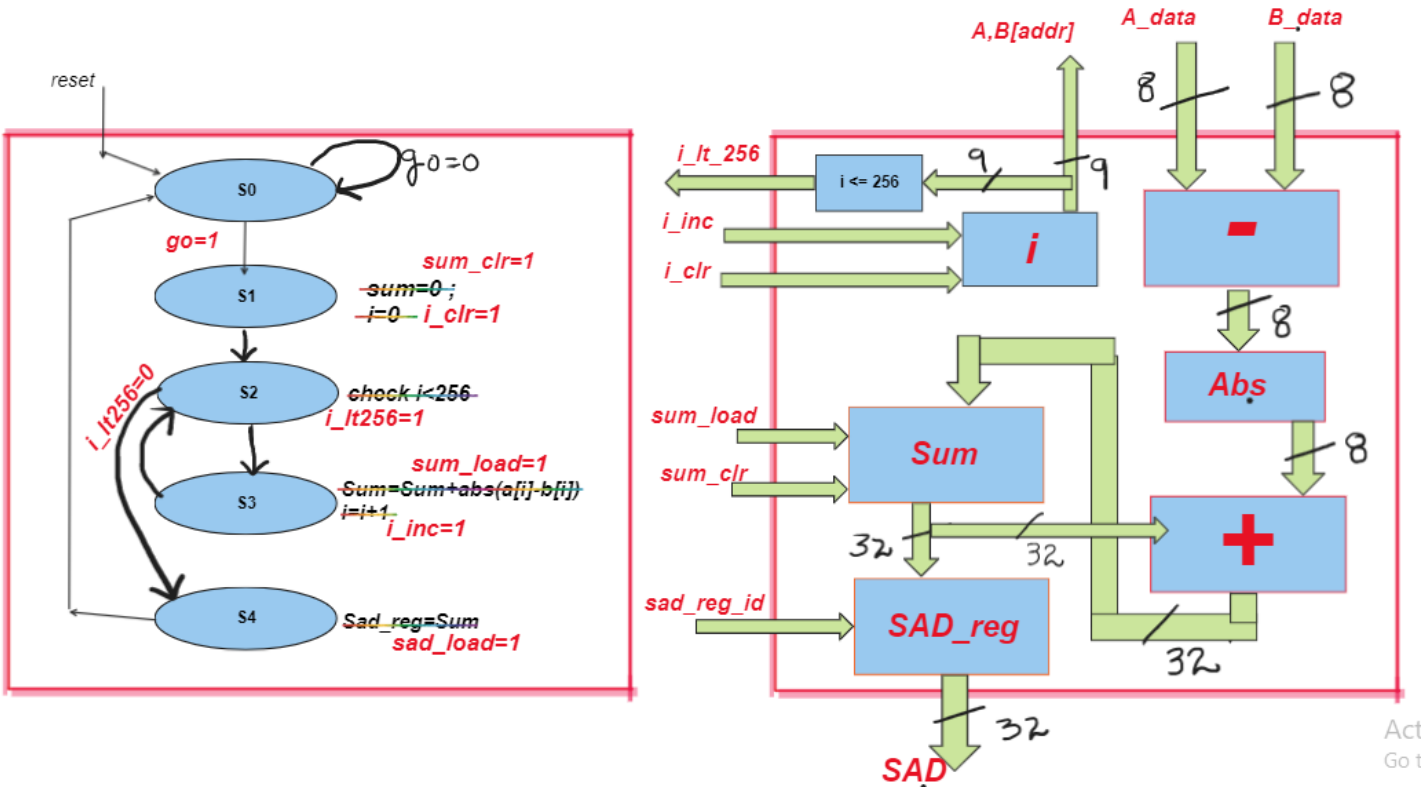



**No of states in FSM:- 5**

**No of control signals:- 8**

**Type of Encoding:- Binary**

# Data path and Control path logic:

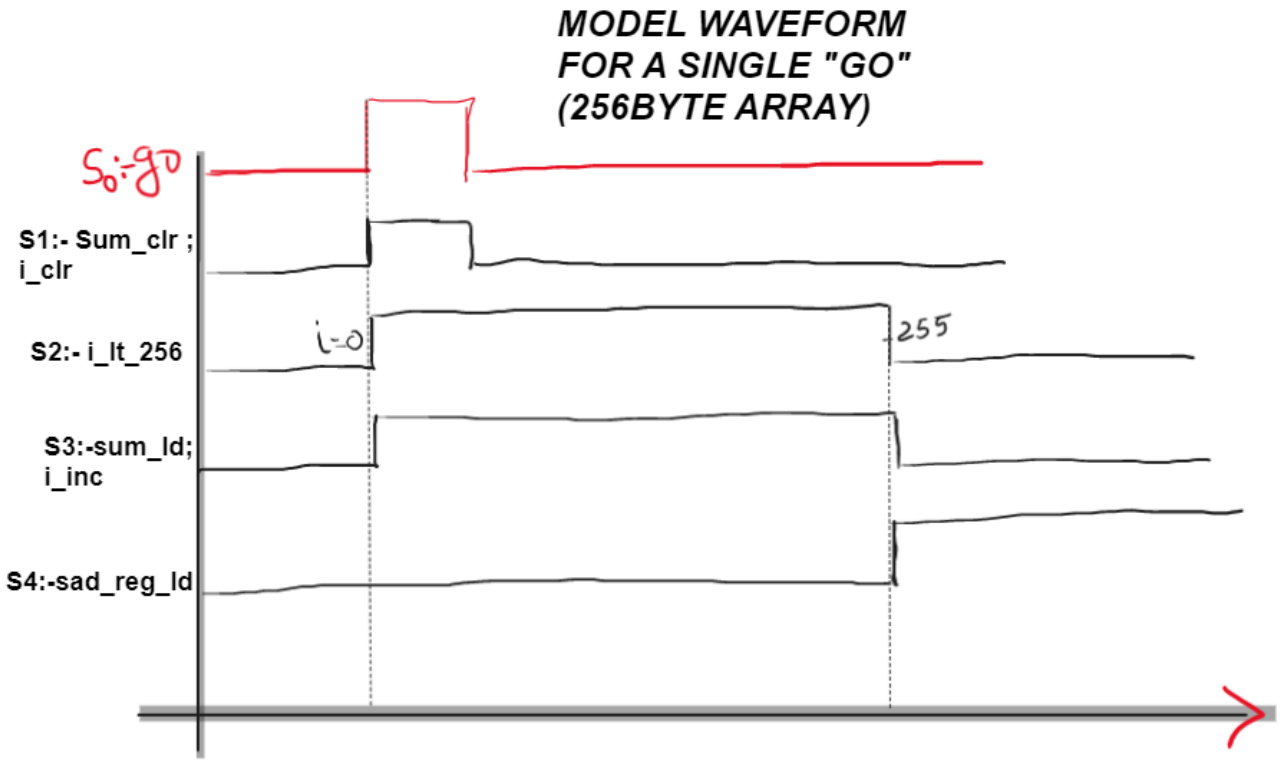



## Data logic signals:

- Inputs: A, B (256-byte memory array)
  go signal (1'bit)
- Outputs: Sad (32 bit integer)
- Local registers: sum, sad_reg (32 bits)
- Integer i counts from 0 to 255 (9 bits)

## Control logic signals:

- I_lt_256, i_inc, i_clr ,go,reset
- Sum_load, sum_clr , sad_reg_id




Refrences:-

[1]. Vanne, Jarno & Aho, Eero & Hämäläinen, Timo & Kuusilinna, Kimmo. (2006). A High-Performance Sum of Absolute Difference Implementation for Motion Estimation. IEEE Trans. Circuits Syst. Video Techn.. 16. 876-883. 10.1109/TCSVT.2006.877150.

[2] Vayalil, Niras & Safari, Azadeh & Kong, Yinan. (2015). ASIC design in Residue Number System for calculating minimum sum of Absolute Differences. 129-132. 10.1109/ICCES.2015.7393032.

[3] https://www.ics.uci.edu/~harris/cs151/slides/dd_vahid_ch5.pdf