Preparation of measurement systems for the PASTTREC ASIC testing

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Preface

This report describes a set-up (hardware) and procedures developed for measurements of the PASSTREC chip performance important for its quality tests during mass production. Some obtained results characterizing chip performance are given to illustrate its successful operation. Recommendation concerning criteria for quality test of chips for mass production are presented in conclusion.

1 Key characteristics of PASTREC

PASTTREC is a configurable ASIC with 64k possible settings which include: charge pre-amplifier gain, peaking times, tail cancellation, shaper circuits and DAC's for baseline settings and a common threshold. Table 1 below presents list of parameters, ranges and regulations steps. The key parameters for the straw tube operation are: a linear and uniform gain among the channels, a fast shaping for high-rate capabilities (signal duration $<$ 500 ns) , a time resolution better than 2 ns, alignment of base line positions such that a common threshold value reject same amount of pulses in each channel and small noise level allowing for a low threshold setting ($\leq 10mV$), important for high efficiency at lowest possible detector gain. The latter reduces aging effects in straws exposed to a high count rate environment of the PANDA experiment.

To determine optimal configuration of PASTTREC a two step procedure was applied. In the first step measurements with signal generataros, radioactive sources were performed to find out optimal configurations for the chip. In the second step the configurations were verified in-beam tests using various multi-detector systems by measuring spatial and time over threshold (TOT) resolutions, which are the key parameters for the detector performance. Finally, the configuration fulfilling PANDA requirements were identified and accepted and also chosen for benchmarking chips for the upcoming mass production.

The two section below describes test system and summarize most important results.

Table 1: PASTTREC settings.

Parameter	**Values**
Gain (K)	0.67,1,2,4 mV/fC
Peaking time (Tp)	10,15,20,35 ns
1^st stage tail cancelation capacitance	1-16.5 pF (step 1.5 pF)
1^st stage tail cancelation resistance	3-31 kΩ (step 4 kΩ
2^st stage tail cancelation capacitance	0.6-1.65 pF (step 0.15 pF)
2^st stage tail cancelation resistance	5-26 kΩ (step 3 kΩ)
Common discrimination threshold	0-254 mV (step 2 mV)
Baseline fine tunning	-32 to +32 mV (setp 2 mV)

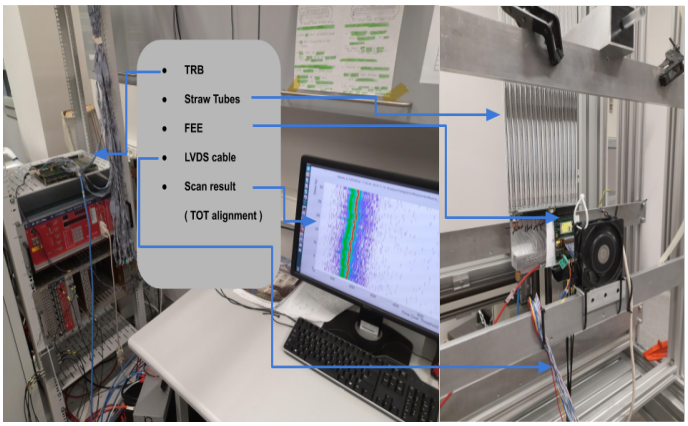

Figure 1: Experimental set-up used for test measurements with PASSTREC chips

2 Description of the test system

In order to perform measurement described above a dedicated test set-up was developed. The set-up consist of following components :

- Front-End Boards (FEB) with 2 PASSTREC chips (version v1), 8 channels each
- read-out board : Trigger Read-out Board v3 (TRBv3) with 4 TDC's for time measurements (48 channel each, 0.1ns resolution) and digital link for data transmission and slow control
- PC for communication with TRBv3 and PASSTRECv1.

PASTTRECv1 chips (2 on every FEB) were bonded to the especially designed printed circuit boards (PCB) of the size $5.3 \times 8,6$ cm. Four layer PCB has 16 input and 16 differential (LVDS) output lines carrying leading edge discriminator outputs for timing measurements. For inspection and measurements

Figure 2: The snapshot of GUI for the FEB setup with two ASIC's selected

of analogue signals another PCB board with additional analogue buffers, driving signal from 16 channels via MMCX connectors, were build. This board was used for measurements of signal shapes, gain functions, noise distributions etc. which were basis for the definition of the optimal chip settings. Two test inputs, connected to dedicated ASIC pads, allowed for charge injection to even and odd channels (separately) of the chip via internal capacitors to measure response to δ-current source.

16 LVDS signals are transmitted via KEL 8930E 40-pin connector which provides 4 additional LVDS lines for the parameters setting. The LVDS cable is connected to an add-on card placed on top of TRBv3 with 3 connectors. In such way, 3 FEB can be connected to one TDC (see below). FEBs with analogue buffers are powered with the symmetrical voltage of 6V (480mA) and -6V (250mA). Power consumption for FEBs without analogue buffers is smaller and amount to 200mA and requires only 4V (similar boards will be used for measurements in PANDA). The FEBs are connected to the straw tubes via an additional passive resistor-capacitor (RC) board equipped with resistors for limiting the wire current and capacitors for voltage decoupling.

The TRB version 3 (TRVv3) is an electronic board designed and developed at GSI Darmstadt in collaboration with HADES group from the Jagiellonian University Krakow. The board contains 5 Lattice EPC3 FPGA's; four edge

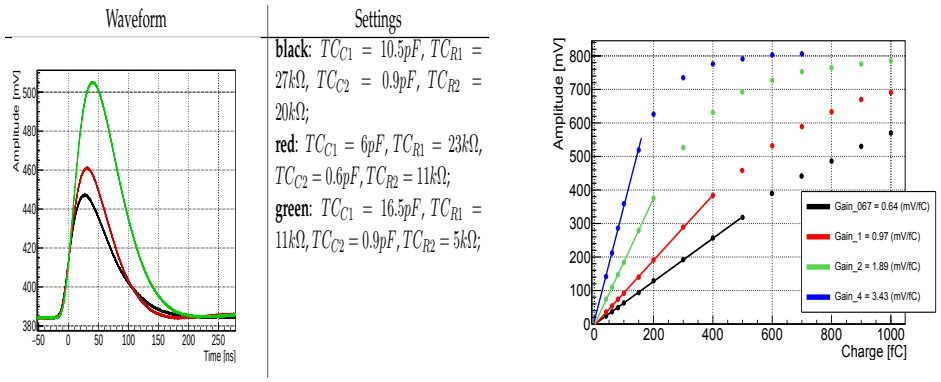

Figure 3: Left: analogue output for three optimal TC settings found for the preamplifier gain K=1 mV/fC and the peaking time PT=20ns, Right: gain functions for δ pulses for the four settings of preamplifier gain parameter (K) and the optimal (TC) settings (see text for details)

FPGA's are configured as 48 channels TDCs and the 5'th (central one) is responsible for data collection from the edge TDCs and communication with an external PC using Gigabit Ethernet network. With this set-up, up to three FEB could be connected to a single TDC (and up to 12 for one TRB) and were controlled via a dedicated slow control system. The system is composed of a Graphical User Interface (GUI) that allows to send chosen configurations with the chip settings to the FEB. GUI is created with use of HTML5 and JS with JQuery library. ASIC's on the given FEB are accessible via the TDC address and the unique address of FEB. Selecting one of the addresses results in showing in the GUI the ASIC configuration panel and allows to change ASIC settings. The configuration module is implemented in the VHDL and it is integrated with the TDC configware. The communication protocol between the FPGA and the PASTTRECv1 chip uses four lines and it is similar to the SPI.

The example of the GUI screen is displayed in Fig. 2. More details of the set-up can be found in [2]

Results of measurements-demonstration of successful operation

Measurements of the chip characteristics were performed injecting the "δ-like" current pulse via test inputs to the chip. A step-like voltage pulse was generated in pulse generator and injected to the chip through a capacitor of known capacitance. Signal from straw tubes irradiated with ^{55}Fe source were also measured for comparison. Note that in the latter case only about 20% of total deposited charge in straw is integrated in the ASIC (long ion tail contribution is suppressed). Analogue outputs from the chip were measured on an oscillo-

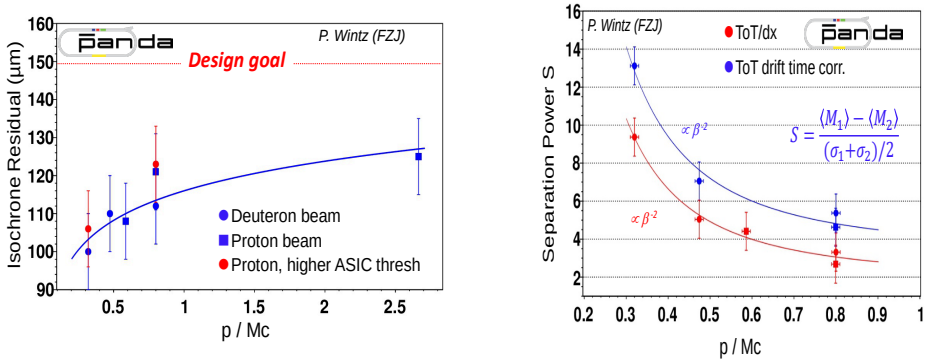

Figure 4: Left: Spatial resolution as a function of $\beta\gamma$, Right: separation power measured as the difference between truncated means TOT/dx for the given $\beta\gamma$ and the corresponding one for MIP protons (red points) obtained in in-beam experiments

scope and respective waveforms were transmitted to the PC where they were analysed. Typical signal parameters like amplitude, baseline position, rise time were extracted for evaluation of the chip characteristics. The results of these measurements are published and can be found in [1].

The preamplifier gain (K) and the peaking time (PT) have four possible settings (see Tab. 1). Furthermore, four parameters (capacitance and resistivity of both stages) that configure the tail cancellation (TC) circuit are also configurable. For each of 4095 possible TC combinations for the given (K,PT) one hundred waveforms of signals coming from the straw tube detector irradiated with the iron source were collected and then averaged. The analysis algorithm was prepared and used to search for the optimal settings defined according to following requirements on analogue signals: (a) no significant undershoot nor overshoot, (b) a high amplitude for the given peaking time. Fig. 3 (left) shows examples of analogue outputs for the three optimal TC settings found for K=1 mV/fC, Tp=20 ns. They differ slightly in amplitude and a small overshoot (1-2 mV only, not visible on the scale of Fig. 3). In similar way optimal settings for the other gain and peaking times combinations were found. Fig. 3 (right) shows the respective gain characteristics of a one chip channel measured for the four preamplifier gain factors (K) using such optimal settings. The characteristic is linear and spread of gain coefficients between channels is small. Th standard deviation of a distribution of gain factors extracted from linear fits to the gain characteristics of about 200 channels equals to 1.3%, only.

The optimal configurations found for each of the selected K (1,2,4 mV/fc) and PT (15,20,35 ns) combinations were tested in several in-beam experiments using STT and FT detector prototypes. For typical HV settings of straws the PASTTREC configurations with gain K=1 mV and peaking times (Tp=15,20,35) are found to best suited for the detector performance. From various analysis of

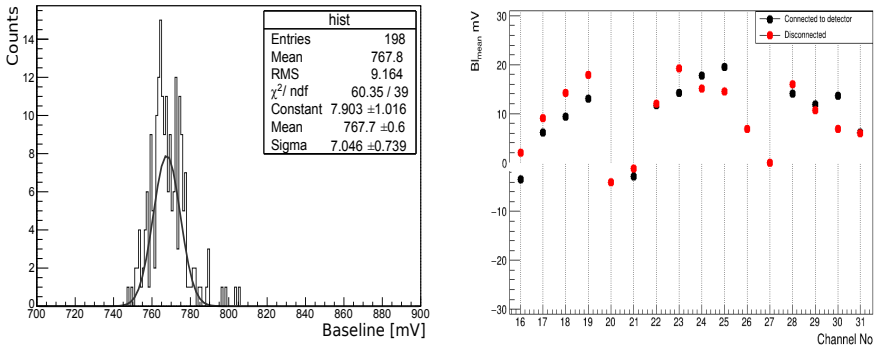

Figure 5: Left: Distribution of baseline positions measured for 198 channels, Right: baseline positions found in the baseline-scan procedure (see text for details) for (K=1 mV, Tp=15) for the two case: FEB is connected to detector (black) and disconnected (red)

data from in-beam experiments results on spatial and TOT resolutions were obtained. Fig.4 displays the achieved spatial resolution and the separation power in TOT as a function of the $\beta\gamma = p/Mc$ (courtesy of P. Wintz). The result clearly demonstrate that PANDA requirements are matched in the anticipated region of operation of the PANDA straw trackers. These results are important since they validate the chip design and the configurations found in the first step. In this way also chip configurations for the quality assurance test for the ASIC mass production has been fixed.

One of the most important parameters requested for PASTTRECv1 are: gain, baseline uniformity and low noise. As already mentioned, measured spread of the gain coefficient of 1.3% is very good and is considered to be sufficient for treating all straw channels as having equal gain without further TOT calibration, provided that baseline levels for all channels are the same. The latter also justifies a common threshold approach and guarantees that timing information obtained from the leading edge discriminator, measuring time of the signal crossing the threshold, is not biased by different baseline positions of various channels. Indeed, as measurements of chip performance show [1], time jitter of singe channel amounts only to 0.14 ns but time walk related to change of threshold value by 40 mV corresponds to almost 2ns and could influence measurement precision. Hence, the baseline alignment between channels must be very good, on the level of DAC precision.

Measurements show that baseline dispersion among chip channels are not negligible, as expected from PASSTREC simulations. Fig. 5 (left) shows distribution of baseline positions measured for 198 channels by means of digitised analogue outputs. It shows a gaussian distribution with $\sigma = 7$ mV, in agreement with results of simulations of PASTTRECv1 chip. Baseline positions can, however, be further aligned with a precision of 2 mV using internal DAC circuit,

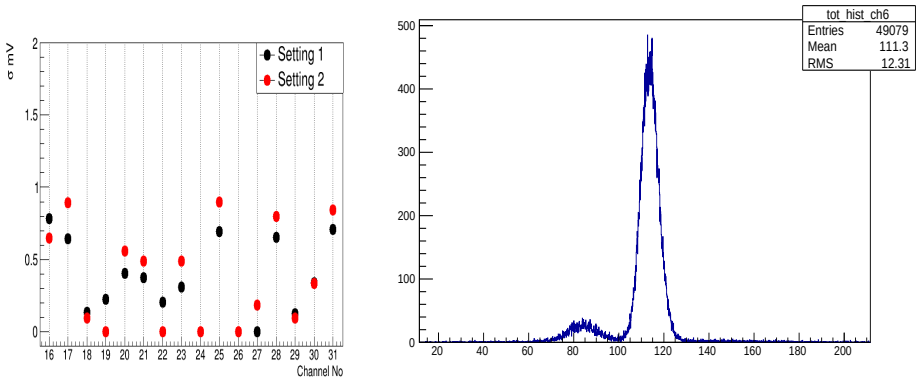

Figure 6: Left: RMS of the noise distribution for 16 channels from one FEB with 2 PASSTREC chips with K=4 mV/fC (high gain) and Tp=15 (red) and 20 (black) ns peaking time. Right: TOT spectrum obtained with ^{55}Fe irradiating straw tube at high voltage set to 1700 V. The more intense right peak corresponds to the full absorption of the 5.9 keV X-rays and it is well separated from the 2.9 keV argon escape peak

designed especially for this purpose. It allows to move baseline position within $\pm$ 32 mV range.

In order to measure baseline position for each chip channel without usage of analogue outputs (which will not be available in the final FEB) a dedicated fast procedure, called base line scan was developed. In this procedure a comment threshold value of 0 mV is set and baseline positions for each channel in a chip are varied within allowed range of $-32; +32$ mV with 2 mV steps. During the scan number of counts is measured for each baseline position and every channel. The baseline position is determined from the measured profile of the number counts as its mean value. The calculated mean value is then subtracted for each channel by the respective DAC setting. Fig. 5 shows results of the baseline position determination for two cases where FEB is connected (black) or disconnected (red) from a straw detector.

The measured distribution is also used to characterise noise of individual channels by means of RMS. This is another important characteristics of the chip performance. As already mentioned above, the low threshold position w.r.t baseline is important for detector operation. Fig. 6 shows distributions of RMS for the two ASIC configurations with K=4 mV and Tp=15 and Tp=20 ns peaking time. The RMS distributions are below 1 mV.

The described method of baseline alignment was verified by in independent measurements with ^{55}Fe radioactive source irradiating straw tube. Fig. 6 (right) shows distribution of TOT measured before and after baseline alignment as a function of channel number. The two X-ray lines from ^{55}Fe source become nicely aligned after application of the procedure.

3 Conclusions

Full characterisation of ASIC performance has been established in various measurements using radioactive sources and in-beam measurements. In particular, chip characteristics (gain functions, baseline distributions, time resolution, signal shaping etc.) have been measured and relevant optimal configurations for the successful straw tube operation have been identified and verified to fulfil PANDA spec. Production of ASIC in AMS showed about 90% success rate and is considered to be very efficient. Therefore, we conclude that quality assurance test of chips should be performed on PASTTREC mounted FEB and focus on following key parameters: (a) power consumption per board (approx. 50 mW/channel) (b) number of fully operational channels (16) (c) baseline position alignment better than 4 mV (d) noise level RMS ¡?? mV (e) TOT uniformity test with iron source.

References

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[2] G. Korcyl *et al.*, IEEE Trans. Nucl. Sci. **65**, no. 2, 821 (2017). doi:10.1109/TNS.2017.2786464