Akshay Malige, Ph.D.

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SUMMARY

FPGA and ML Hardware Engineer with expertise in real-time data acquisition, low-latency ML inference, and heterogeneous computing. 10+ FPGA-based projects across high-energy physics, industrial automation, and AI-on-FPGA applications. Specialist in hls4ml, Xilinx Alveo, and Versal ACAP platforms with end-to-end experience deploying AI models using Vitis, HLS, and embedded software integration. Strong contributor to cross-functional, globally distributed teams. 40+ technical publications. Full list at Google Scholar.

SKILLS

HDL/Hardware: VHDL, Verilog, AXI, PCIe, Vivado IP Integrator, Timing Closure, HBM

HLS/ML: Vivado HLS, Vitis HLS, hls4ml, AI Engine (AIE, AIE-ML), DPU.

Platforms: Xilinx Alveo U55c/U250/U280, Versal VEK280, PYNQ-Z2, ZCU104, Zynq UltraScale+ MPSoC ZCU102, Kintex Kintex Ultrascale KU15P, Lattice ECP3, Lattice ECP5.

Software: Python, C/C++, Bash, Git, Linux, MATLAB, ROOT, Docker

Frameworks: PyTorch, TensorFlow, PYNQ, OpenCAPI, XRT, Vitis AI

Tools: Vivado, Vitis, ModelSim, HLS Profiler, Vitis Analyzer, Lattice Diamond, Quartus

EXPERIENCE

Postdoctoral Research Associate, Brookhaven National Lab *Dec 2024 – Present*
Upton, NY, USA

- Designed real-time tracking system for ATLAS trigger using hls4ml-deployed ML models on Alveo U250, boosting inference throughput.
- Architected detector alignment algorithm on Versal ACAP VEK280 using AI Engine tiles, DMA interfaces, and PS-to-PL dataflows.

Postdoctoral Research Scientist, Columbia University *Jul 2023 – Dec 2024*
New York, NY, USA

- Built FPGA firmware for low-latency DAQ and anomaly detection (DUNE, ICEBERG, MicroBooNE) with real-time ML.
- Coordinated multi-institution FPGA integration for NASA-funded GRAMS project; supervised design, testing, and deployment phases.

R&D Product Engineer, Hitachi Energy *Feb 2023 – Jun 2023*
Kraków, Poland

- Developed and validated VHDL-based protection/control blocks for HVDC systems using rigorous bench-testing and timing closure.
- Delivered integration of FPGA logic into grid-scale industrial converters, adhering to IEC standards.

Research Assistant (Ph.D.), AGH University *Jan 2022 – Feb 2023*
Kraków, Poland

- Designed custom FPGA DAQ pipeline with hit clustering and trigger logic for PANDA/HADES using Xilinx FPGAs.
- Created slow-control and monitoring framework improving uptime and remote diagnostics; awarded PANDA@HADES group prize.

Training Specialist, ThinkLabs Technosolutions *Nov 2016 – Sep 2017*
Bengaluru, India

- Delivered 100+ hardware-oriented STEM workshops across India, engaging 500+ students and educators in applied electronics.

SELECTED PROJECTS

- **Real-Time Alignment on Versal ACAP:** Designed ML-based alignment algorithm across AI Engine + PL + ARM cores on VEK280.
- **ATLAS ML Trigger:** HLS-optimized hls4ml model for event filter tracking in ATLAS; implemented on Alveo U250.
- **Anomaly Detection FPGA Pipeline:** Autoencoder-based anomaly detection for streaming data on U280 using HLS.
- **GRAMS Readout:** DAQ firmware and integration lead for TPC-based gamma-ray balloon experiment.

EDUCATION

Ph.D. in Physics, Jagiellonian University, Poland *2017 – 2023*
M.Sc. in Physics, Christ University, Bangalore, India *2014 – 2016*
B.Sc. in Physics, Electronics & Mathematics, Mangalore University, India *2011 – 2014*