PASTTREC ASIC documentation

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Last change: 17 February, 2021

Contents

Documentation Conventions

To aid the readers understanding, a consistent formatting style has been used throughout this manual.

- Internal signals are written using *italic* font.
- External connections names (pads) like supplies use CAPITAL LETTERS only.
- External signals names, however, are in capital letters but using *ITALIC* font also.
- Configuration elements like register names are written in sans serif font.
- Signals controlled by configuration bits use *slanted sans serif* font.

For numbers the Verilog prefix style is used:

- **'b** for binary numbers e.g 'b1010,
- **'h** for hexadecimal numbers e.g 'hA7,
- **'d** for decimal numbers e.g 'd72,
- no prefix means that the number is in decimal notation.

1 Overview of the PASTTREC ASIC

The PASTTREC is an 8-channel straw tube readout Application Specific Integrated Circuit (ASIC) for $\overline{\text{P}}$ANDA experiment which name stands for $\overline{\textbf{P}}$**A**NDA **S**traw **T**ube **T**racker **RE**adout **C**hip. A block diagram of the ASIC is shown in figure 1.

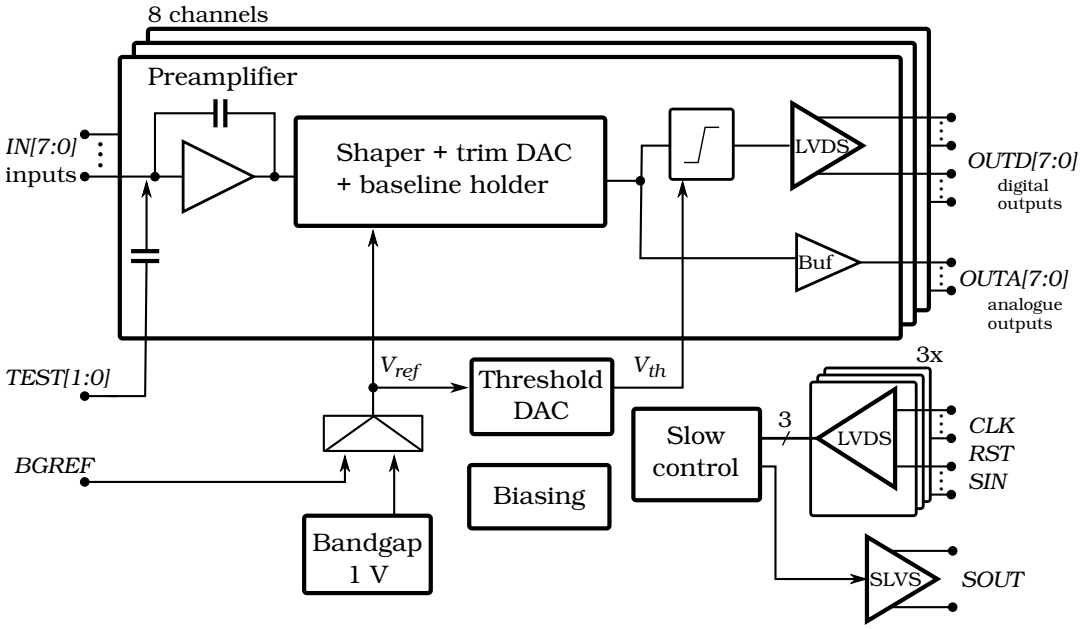

Figure 1: Block diagram of the PASTTREC ASIC.

2 Requirements for the front-end electronics

For the front-end electronics the most important detector parameters are: a sensor capacitance, a signal amplitude, shape and length, an expected count rate, a front-end electronics noise. These parameters are very similar for both $\overline{\text{P}}$ANDA straw tube trackers.

The expected straw capacitance depends on the length of straws (varying from 40 to 150 cm) and is in the order of $\approx$15 pF/m which gives a maximum capacitance of 22 pF for 150 cm straw length.

The current signal generated in straw detector has fast (ns range) electron component and slow (μs range) ion movement. For a cylindrical geometry and a point ionization, the signal induced in the detector is described by the following relationship:

$$i(t) = \frac{Q_t}{2\tau \ln\left(\frac{b}{a}\right)} \cdot \frac{1}{a^2 + b^2 \frac{t}{\tau}}, \tag{1}$$

where Q_t is the total charge produced in avalanche, a and b are anode and cathode radii

respectively, and τ is the ion collection time given by:

$$\tau = \frac{b^2 p \ln\left(\frac{b}{a}\right)}{2\mu_{ion} V}, \tag{2}$$

where p is the filling gas pressure, μ_{ion} is the ion mobility and V is the anode to cathode voltage. The total charge produced in the straw depends on the particle specific ionization power and the gas gain. The latter depends on the high voltage applied to the anode wire and is typically in the order of 10^4.

The front-end should provide both the amplitude and time measurements and it should be able to operate at the expected rate of 800 kHz/straw. The required position resolution of $\approx 150\mu m$ translates to the time resolution of the order of 1 ns. The energy loss measurement in a single straw should cover a dynamical range spanned by minimum ionizing pions up to slow protons and kaons resulting in factor 4 – 5 larger energy deposition. The energy is measured using a Time-over-Threshold (ToT) technique. To operate with the maximum requested rate a Tail Cancellation (TC) of the slow ion signal component is implemented.

The detailed specifications to be met by the front-end are summarized in table 1.

Table 1: The requirements for front-end electronics.

Peaking time	$\leq 10 - 40$ ns
Double pulse resolution	~ 100 ns
Variable gain	2 – 16 mV/fC
Intrinsic electronic noise	< 1 fC
Straw tube capacitance	6 – 25 pF
Discriminator threshold	≈ 5 fC
Max. drift time in STT	200 ns
Time resolution	~ 1 ns

3 Front-end architecture

The block diagram of the PASTTREC i^{th} channel is shown in figure 2. The PASTTREC channel comprises a Charge Sensitive Preamplifier (CSP) with a variable gain and a discharge time constant, a Pole Zero Cancellation (PZC) unit, a second order shaper with a variable peaking time, an ion tail cancellation circuit with trimming, a BaseLine Holder (BLH) to stabilize the baseline, a Leading Edge Discriminator (LED) with Low Voltage Differential Signaling (LVDS) output, and a buffered analog output.

The baseline reference voltage of the front-end is set by V_{ref} obtained either locally from internal 1 V bandgap circuit or externally from pad *BGREF* (see also figure 1). This setting is controlled by field *baseline_sel* of register preamp_cfg described in table 2. Each channel has internal 5-bit DAC for baseline tuning, controlled by fields *baseline_trim*

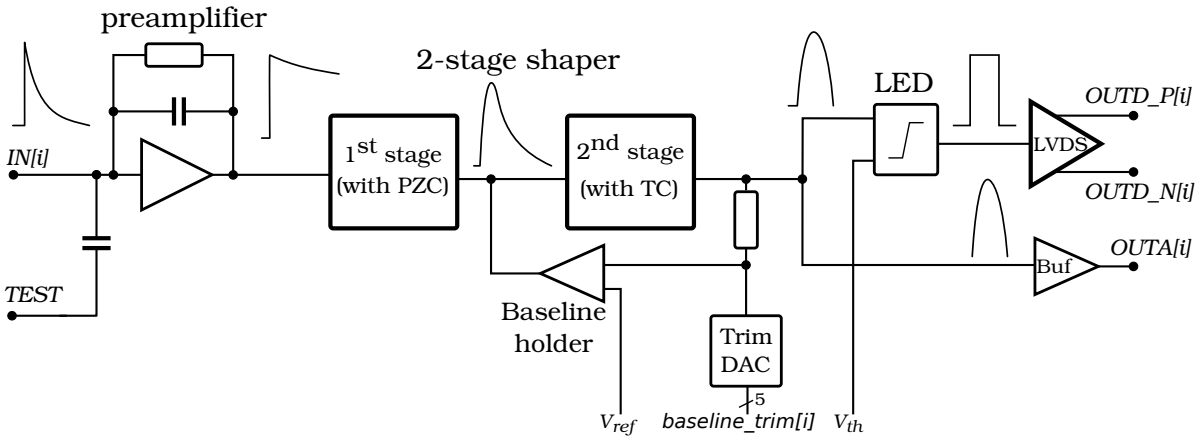

Figure 2: Block diagram of the front-end electronics channel.

of registers channel_0_cfg – channel_7_cfg (see table 2). The descrimination threshold V_{th} is set with respect to V_{ref} voltage (see also figure 1), and it is obtained from 7-bit DAC, controlled by field *global_threshold* of register threshold_cfg described in table 2.

3.1 Preamplifier and 1st shaper stage

A schematic diagram of the CSP, PZC, and the first shaper stage is shown in figure 3. The variable gain of CSP is achieved by the switching feedback capacitance C_{fed} between

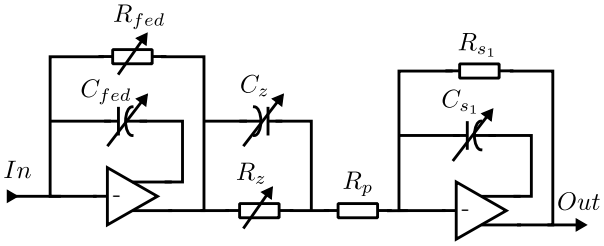

Figure 3: Schematic diagram of CSP, PZC, and first shaper stage.

0.25, 0.5, 1, and 2 pF respectively (controlled by field *gain* of register preamp_cfg – table 2). The feedback resistance R_{fed} can be also changed in the range between 100 and 400 kΩ providing various CSP time constants in the range of 25 to 800 ns. The CSP is followed by the PZC circuit matched to the CSP time constant. The PZC capacitor C_z can be varied in the range of 5 to 20 pF while resistor R_z in the range of 5 to 40 kΩ respectively. The PZC together with the first shaper stage provides a classic CR-RC shaping with a peaking time defined by proper settings of the PZC and the shaper

feedback elements. The shaper output is expressed by the following formula:

$$V_{out}^{1st}(s) \approx \frac{I_{in}(s)}{C_{fed}C_{s_1}R_p} \cdot \frac{s+\frac{1}{C_zR_z}}{s+\frac{1}{C_{fed}R_{fed}}} \cdot \frac{1}{\left(s+\frac{1}{C_{s_1}R_{s_1}}\right)\left(s+\frac{1}{C_z(R_p\|R_z)}\right)} \approx \frac{I_{in}(s)}{C_{fed}C_{s_1}R_p} \cdot \frac{1}{\left(s+\frac{1}{\tau_{sh}}\right)^2}. \tag{3}$$

The time constant τ_{sh} can be set to 5, 7.5, 10, or 20 ns (which is controlled by field *peaking_time* of register preamp_cfg from table 2) by changing values of the PZC and the shaper capacitances C_z and C_{s_1}. The above formula is obtained by assuming high enough open loop gain and negligible output impedance of the amplifiers and also neglecting resistances and capacitances of the switches. In practice the peaking time is about 10, 15, 20, or 35 ns for the corresponding settings.

3.2 Tail cancellation and 2nd shaper stage

The main idea of the tail cancellation circuit was proposed by by Boie. The shape of current signal induced in the straw detector, proportional to $1/(1+t/\tau)$, is approximated by a linear combination of a few exponential functions with different amplitudes and time constants, as follows:

$$i(t) \propto -Q_t \cdot \frac{1}{1+\frac{t}{\tau}} \approx -Q_t \sum_{k=1}^{N} A_k \cdot e^{-\alpha_k t}, \tag{4}$$

where A_k are amplitudes and α_k are time constant reciprocals. In the PASTTREC the detector signal is approximated by a sum of two exponents and so two ion tail components are eliminated by the tail cancellation circuit.

Figure 4 presents the implemented TC circuit, together with the second shaper stage, BLH, LED, and the analogue buffer.

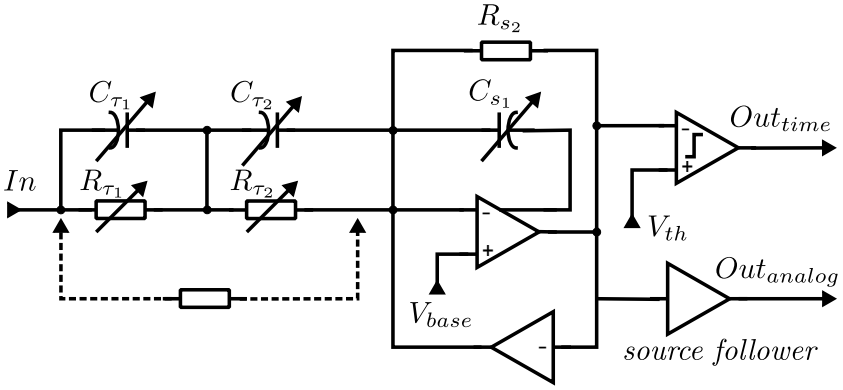

Figure 4: Schematic diagram of TC circuit, second shaper stage, BLH, LED, and output analogue buffer.

The TC works in four different modes. In the first one, for operation with straw tubes,

both time constants ($R_{\tau_1}C_{\tau_1}$ and $R_{\tau_2}C_{\tau_2}$) are switched on. The second and third ones are active when only one time constant is enabled ($R_{\tau_1}C_{\tau_1}$ or $R_{\tau_2}C_{\tau_2}$ respectively), and the last one when the TC is switched off (and replaced by single resistor) providing classic CR-RC^2 shaping.

In order to demonstrate how the tail cancellation circuit works one can apply the output voltage from the first stage of the shaper (eq. 3) to the input of the TC circuit followed by the second stage of shaper, to obtain following formula:

$$V_{out}^{2nd}(s) = -\frac{I_{in}(s)}{C_{fed}C_{s_1}R_p} \cdot \left(s + \frac{1}{\tau_{sh}}\right)^{-3} \cdot \left(\frac{C_{s_2}}{C_{\tau_1}} \frac{1}{s + \frac{1}{R_{\tau_1}C_{\tau_1}}} + \frac{C_{s_2}}{C_{\tau_2}} \frac{1}{s + \frac{1}{R_{\tau_2}C_{\tau_2}}}\right)^{-1}. \quad (5)$$

Now, inserting the exact form of the detector current with the first two exponents only (N=2 in eq. 4) results in the following form in Laplace domain:

$$I_{in}(s) = -Q_t \left(\frac{A_1}{s + \alpha_1} + \frac{A_2}{s + \alpha_2}\right). \quad (6)$$

Finally the following formula for the output voltage can be obtained:

$$V_{out}^{2nd}(s) = \frac{Q_t}{C_{fed}C_{s_1}R_p} \cdot \left(s + \frac{1}{\tau_{sh}}\right)^{-3} \cdot \left(\frac{C_{s_2}}{C_{\tau_1}} \frac{1}{s + \frac{1}{R_{\tau_1}C_{\tau_1}}} + \frac{C_{s_2}}{C_{\tau_2}} \frac{1}{s + \frac{1}{R_{\tau_2}C_{\tau_2}}}\right)^{-1} \cdot \left(\frac{A_1}{s + \alpha_1} + \frac{A_2}{s + \alpha_2}\right). \quad (7)$$

The above equation shows that with a proper choice of the ratio of C_{τ_1} and C_{τ_2}, proportional to the ratio of the amplitudes A_2 and A_1, and setting the time constants of the TC circuit to the corresponding parameters α_k, a complete ion tail elimination can be achieved. Especially when:

$$A_k = \frac{C_{s_2}}{C_{\tau_k}}, \alpha_k = \frac{1}{R_{\tau_k}C_{\tau_k}}, \quad (8)$$

the formula for the output voltage simplifies to a classical second order pseudo-gaussian shaping as follows:

$$V_{out}^{2nd}(s) = \frac{Q_t}{C_{fed}C_{s_1}R_p} \cdot \left(s + \frac{1}{\tau_{sh}}\right)^{-3} \quad (9)$$

However, the ion tail approximated with equation 4 depends on the parameters A_k and α_k which differ for various gas mixtures or pressure. For this reason, each tail cancellation circuit element (two resistors and two capacitors) can be trimmed by 3-bit DACs providing in total 4096 various settings of the TC time constants (register tail_cancel_1_cfg in table 2) in the ranges of 18 – 511 ns ($R_{\tau_1}C_{\tau_1}$ controlled by fields *tc1_c*, *tc1_r*) and 3 – 43 ns ($R_{\tau_2}C_{\tau_2}$ controlled by fields *tc2_c*, *tc2_r*) respectively. This feature allows the proposed front-end ASIC to work for a wide range of gaseous detectors. Moreover, enabling only one time constant makes this design useful for applications using avalanche photodiodes and also for standard semiconductor detector applications if the TC circuit is switched off.

4 Slow control and registers list

At the very beginning, before any slow control command chip should be reseted because there is no power-on reset in the ASIC. Reset sets all internal registers to their default values shown in register description in table 2. Reset signal is active low and synchronous, therefore clock signal have to be active during the whole reset sequence. It may last any number (at least one) of clock cycles but when removed during next 5 clock cycles chip is still internally in reset, so the user should wait at least 6 clock cycles before sending any command.

When reset is done chip can be programmed by slow control commands which has the form:

$$Header[3:0] \,|\, Address[1:0] \,|\, R/\overline{W} \,|\, RegNo[3:0] \,|\, RegData[7:0] \tag{10}$$

where header is constant and equal 'b1010. Timing diagram of the command is shown in figure 5. Mode detailed one, with all data blocks expanded to individual bits, is presented in top part of the figure 6 (page 9). The ASIC samples its inputs and send data out on rising clock edge, so at this clock edge value on the *SIN* pad should be stable. On the other hand data should be read by the receiver at the falling clock edge.

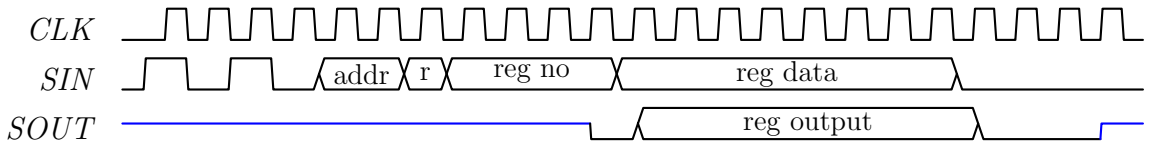

Figure 5: Slow control command; for more detailed diagram see figure 6 on page 9

The command is executed only if value in field *Address* is equal the chip ID defined via input pads *ID*. However, the commands with different addresses are still tracked to avoid collisions during communication with several chips. The ASIC waits for a header only when the previous command was ended regardless of received *Address*.

The ASIC receiving correct *Address* sends the value of register *RegNo* through the output *SOUT*. If the bit $R/\overline{W}$ is zero the register *RegNo* is also written with the new value *RegData*. In the opposite case (bit $R/\overline{W}$ is one) the chip only sends out the current register value.

Output pad *SOUT* is in the high impedance state all the time except the chip is transmitting data. Data buffer at *SOUT* pad is turn on when the last bit of *RegNo* is sampled. The first bit send by the buffer is zero and should be ignored. This clock cycle gives the output LVDS time to start avoiding data distortion. Then, register contents is send (8 bits) and after that the buffer is still active during next 3 clock cycles. As a result, to be sure that the buffer is off, at least 5 zeros should follow the register data (*RegData*).

Taking into account all clock cycles necessary to inactivate output buffers a single command is 23 bits long. However if many commands have to be sent sequentially they may be partially pipelined (see bottom part of the figure 6). The following command

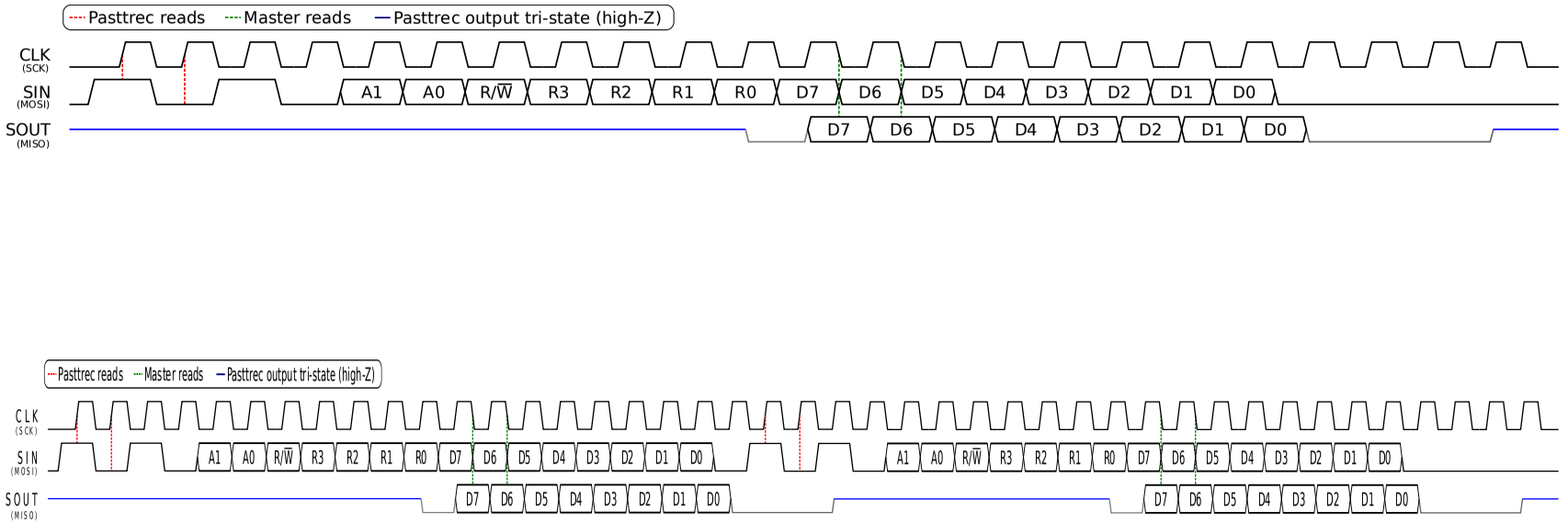

Figure 6: Detailed diagrams of slow control command; top – single command; bottom – two pipelined commands. Legend: Ax – chip ID, R/$\overline{\text{W}}$ – read/write bit, Rx – register number, Dx – register data.

may start almost just after register data of the previous one. Only a single separation bit of value zero is needed. This scheme will work even when several different chips are programmed in a single command train. At the end of the train at least 5 zeros should send to turn off the output buffer.

Table 2: Chip registers.

Addr	Name	Bit	Bit Name	Description
'h0	preamp_cfg		reset value	'h10
		7:5	—	Reserved
		4	*baseline_sel*	Baseline control selection • 0 – $V_{ref} = BGREF$ (external pad) • 1 – $V_{ref} = 1\,\mathrm{V}$ (internal bandgap)
		3:2	*gain*	Front-end gain selection • 'b00 – 4 mV/fC • 'b01 – 2 mV/fC • 'b10 – 1 mV/fC • 'b11 – 0.67 mV/fC
		1:0	*peaking_time*	Front-end peaking time selection • 'b00 – 10 ns • 'b01 – 15 ns • 'b10 – 20 ns • 'b11 – 35 ns
'h1	tail_cancel_1_cfg		reset value	'h00
		7:6	—	Reserved
		5:3	*tc1_c*	First tail cancelation filter capacitance • 'b000 – 6.0 pF • 'b001 – 7.5 pF • 'b010 – 9.0 pF • 'b011 – 10.5 pF • 'b100 – 12.0 pF • 'b101 – 13.5 pF • 'b110 – 15.0 pF • 'b111 – 16.5 pF

Continued on next page

Table 2 – continued from previous page

Addr	Name	Bit	Bit Name	Description
		2:0	*tc1_r*	First tail cancelation filter resistance • 'b000 – 3 kΩ • 'b001 – 7 kΩ • 'b010 – 11 kΩ • 'b011 – 15 kΩ • 'b100 – 19 kΩ • 'b101 – 23 kΩ • 'b110 – 27 kΩ • 'b111 – 31 kΩ
'h2	tail_cancel_2_cfg		reset value	'h00
		7:6	—	Reserved
		5:3	*tc2_c*	Second tail cancelation filter capacitance • 'b000 – 0.60 pF • 'b001 – 0.75 pF • 'b010 – 0.90 pF • 'b011 – 1.05 pF • 'b100 – 1.20 pF • 'b101 – 1.35 pF • 'b110 – 1.50 pF • 'b111 – 1.65 pF
		2:0	*tc2_r*	Second tail cancelation filter resistance • 'b000 – 5 kΩ • 'b001 – 8 kΩ • 'b010 – 11 kΩ • 'b011 – 14 kΩ • 'b100 – 17 kΩ • 'b101 – 20 kΩ • 'b110 – 23 kΩ • 'b111 – 26 kΩ
'h3	threshold_cfg		reset value	'h08
		7	—	Reserved

Continued on next page

Table 2 – continued from previous page

Addr	Name	Bit	Bit Name	Description
		6:0	*global_threshold*	Global setting which defines threshold for all channels with respect to V_{ref}; its value changes from V_{ref} to V_{ref} + 254 mV with step 2 mV
'h4	channel_0_cfg	reset value		'h0F
		7:5	—	Reserved
		4:0	*baseline_trim[0]*	Channel 0 baseline trimming DAC; range ±30 mV with step 2 mV, where MSb is the sign
'h5	channel_1_cfg	reset value		'h0F
		7:5	—	Reserved
		4:0	*baseline_trim[1]*	Channel 1 baseline trimming DAC; range ±30 mV with step 2 mV, where MSb is the sign
'h6	channel_2_cfg	reset value		'h0F
		7:5	—	Reserved
		4:0	*baseline_trim[2]*	Channel 2 baseline trimming DAC; range ±30 mV with step 2 mV, where MSb is the sign
'h7	channel_3_cfg	reset value		'h0F
		7:5	—	Reserved
		4:0	*baseline_trim[3]*	Channel 3 baseline trimming DAC; range ±30 mV with step 2 mV, where MSb is the sign
'h8	channel_4_cfg	reset value		'h0F
		7:5	—	Reserved
		4:0	*baseline_trim[4]*	Channel 4 baseline trimming DAC; range ±30 mV with step 2 mV, where MSb is the sign
'h9	channel_5_cfg	reset value		'h0F
		7:5	—	Reserved
		4:0	*baseline_trim[5]*	Channel 5 baseline trimming DAC; range ±30 mV with step 2 mV, where MSb is the sign
'hA	channel_6_cfg	reset value		'h0F
		7:5	—	Reserved
		4:0	*baseline_trim[6]*	Channel 6 baseline trimming DAC; range ±30 mV with step 2 mV, where MSb is the sign

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Table 2 – continued from previous page

Addr	Name	Bit	Bit Name	Description
'hB	channel_7_cfg		reset value	'h0F
		7:5	—	Reserved
		4:0	*baseline_trim[7]*	Channel 7 baseline trimming DAC; range ±30 mV with step 2 mV, where MSb is the sign
'hC	reserved_cfg		reset value	'h00
		7:0	—	A register without any function
'hD	lvds_cfg		reset value	'h05
		7:3	—	Reserved
		2:0	*lvds_dac*	Nonlinear biasing DAC for LVDS drivers; range 35 μA – 4 mA; default value corresponds to 3.4 mA

5 Padring

The pad ring of the ASIC is shown in figure 7. A reference number has been assigned to each pad.The numbering starts in the upper left corner of the die and runs counter-clockwise. The tables 3, 4, 5, and 6 describe all the pads. The pad coordinates refer to the centre of the pad opening. The origin of the coordinate system is defined by the lower left chip corner (0,0). The die size is 1940 μm × 2590 μm.

Table 3: **Front Pads**.

No	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
From TOP					
1	*TEST*[0]	53.25	2150.425	input	Analogue; input of test signal for even channels
2	*IN*[0]	53.25	1950.425	input	Analogue; input of channel [0]
3	*IN*[1]	53.25	1750.425	input	Analogue; input of channel [1]
4	*IN*[2]	53.25	1550.425	input	Analogue; input of channel [2]
5	*IN*[3]	53.25	1350.425	input	Analogue; input of channel [3]
6	*IN*[4]	53.25	1150.425	input	Analogue; input of channel [4]
7	*IN*[5]	53.25	950.425	input	Analogue; input of channel [5]
8	*IN*[6]	53.25	750.425	input	Analogue; input of channel [6]
9	*IN*[7]	53.25	550.425	input	Analogue; input of channel [7]
10	*TEST*[1]	53.25	350.425	input	Analogue; input of test signal for odd channels

Table 4: **Bottom Pads**.

No	Pin name	Coordinates		Type	Description
		x [μm]	**y** [μm]		
From LEFT					
11	*VDDR*	289.5	47.5	ESD	Analogue; ESD power supply
12	*VDDA*	390	47.5	power	Analogue; power supply
13	*GND*	490	47.5	power	Analogue; ground
14	*VDDA*	620	47.5	power	Analogue; power supply
15	*GND*	720	47.5	power	Analogue; ground
16	*VDDA*	850	47.5	power	Analogue; power supply
17	*GND*	950	47.5	power	Analogue; ground
18	*VDD*	1185.775	47.5	power	Digital; power supply
19	*GND*	1285.775	47.5	power	Digital; ground
20	*ID*[0]	1385.775	47.5	CMOS in	Digital; chip address [0]
21	*ID*[1]	1485.775	47.5	CMOS in	Digital; chip address [1]
22	*SIN_P*	1585.775	47.5	LVDS in	Digital; slow control input positive
23	*SIN_N*	1685.775	47.5	LVDS in	Digital; slow control input negative
24	*VDDR*	1785.775	47.5	ESD	Digital; ESD power supply

Table 5: **Backside Pads**.

No	Pin name	Coordinates		Type	Description
		x [μm]	**y** [μm]		
From BOTTOM					
25	*GND*	1886.775	142.85	power	Digital; ground
26	*SOUT_N*	1886.775	342.85	LVDS out	Digital; slow control output negative
27	*SOUT_P*	1886.775	442.85	LVDS out	Digital; slow control output positive
28	*OUTD_N*[7]	1886.775	542.85	LVDS out	Digital; discriminator output negative [7]
29	*OUTA*[7]	1649.75	583.7	analogue out	Analogue; front-end output [7]
30	*OUTD_P*[7]	1886.775	642.85	LVDS out	Digital; discriminator output positive [7]
31	*OUTD_N*[6]	1886.775	742.85	LVDS out	Digital; discriminator output negative [6]
Continued on next page					

Table 5 – continued from previous page

No	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
32	$OUTA$[6]	1649.75	783.7	analogue out	Analogue; front-end output [6]
33	$OUTD\_P$[6]	1886.775	842.85	LVDS out	Digital; discriminator output positive [6]
34	$OUTD\_N$[5]	1886.775	942.85	LVDS out	Digital; discriminator output negative [5]
35	$OUTA$[5]	1649.75	983.7	analogue out	Analogue; front-end output [5]
36	$OUTD\_P$[5]	1886.775	1042.85	LVDS out	Digital; discriminator output positive [5]
37	$OUTD\_N$[4]	1886.775	1142.85	LVDS out	Digital; discriminator output negative [4]
38	$OUTA$[4]	1649.75	1183.7	analogue out	Analogue; front-end output [4]
39	$OUTD\_P$[4]	1886.775	1242.85	LVDS out	Digital; discriminator output positive [4]
40	$OUTD\_N$[3]	1886.775	1342.85	LVDS out	Digital; discriminator output negative [3]
41	$OUTA$[3]	1649.75	1383.7	analogue out	Analogue; front-end output [3]
42	$OUTD\_P$[3]	1886.775	1442.85	LVDS out	Digital; discriminator output positive [3]
43	$OUTD\_N$[2]	1886.775	1542.85	LVDS out	Digital; discriminator output negative [2]
44	$OUTA$[2]	1649.75	1583.7	analogue out	Analogue; front-end output [2]
45	$OUTD\_P$[2]	1886.775	1642.85	LVDS out	Digital; discriminator output positive [2]
46	$OUTD\_N$[1]	1886.775	1742.85	LVDS out	Digital; discriminator output negative [1]
47	$OUTA$[1]	1649.75	1783.7	analogue out	Analogue; front-end output [1]
48	$OUTD\_P$[1]	1886.775	1842.85	LVDS out	Digital; discriminator output positive [1]
49	$OUTD\_N$[0]	1886.775	1942.85	LVDS out	Digital; discriminator output negative [0]
50	$OUTA$[0]	1649.75	1983.7	analogue out	Analogue; front-end output [0]
51	$OUTD\_P$[0]	1886.775	2042.85	LVDS out	Digital; discriminator output positive [0]
52	GND	1886.775	2441.85	power	Digital; ground
TOP of the ASIC					

Table 6: **Top Pads**.

No	Pin name	Coordinates		Type	Description
		x [μm]	**y** [μm]		
From RIGHT					
53	*VDDR*	1785.775	2537.5	ESD	Digital; ESD power supply
54	*RSTN_N*	1685.775	2537.5	LVDS in	Digital; reset input negative
55	*RSTN_P*	1585.775	2537.5	LVDS in	Digital; reset input positive
56	*CLK_N*	1485.775	2537.5	LVDS in	Digital; clock input negative
57	*CLK_P*	1385.775	2537.5	LVDS in	Digital; clock input positive
58	*GND*	1285.775	2537.5	power	Digital; ground
59	*VDD*	1185.775	2537.5	power	Digital; power supply
60	*BGREF*	1055	2537.5	analogue in	Analogue; external baseline input
61	*GND*	950	2537.5	power	Analogue; ground
62	*VDDA*	850	2537.5	power	Analogue; power supply
63	*GND*	720	2537.5	power	Analogue; ground
64	*VDDA*	620	2537.5	power	Analogue; power supply
65	*GND*	490	2537.5	power	Analogue; ground
66	*VDDA*	390	2537.5	power	Analogue; power supply
67	*VDDR*	289.5	2537.5	ESD	Analogue; ESD power supply

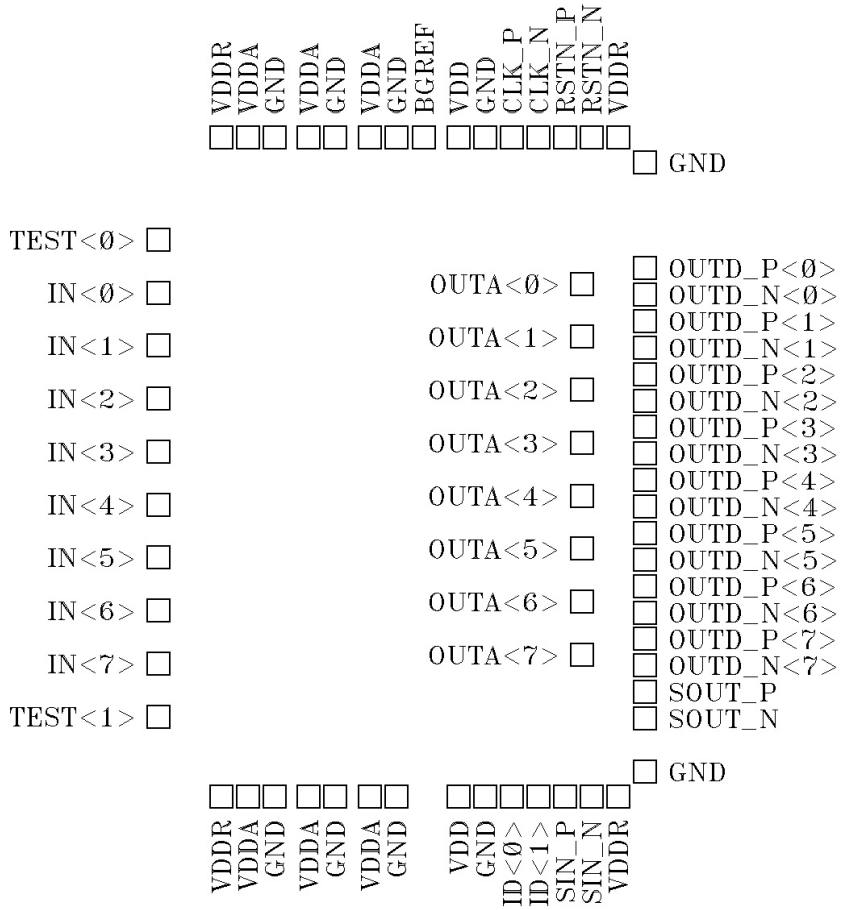

Figure 7: Pad layout of the PASTTREC ASIC.