

Unit - 1

BASICS OF OPERATIONAL AMPLIFIERS

* Basics:

IC μ A741 - operational Amplifiers

- There are two types of IC's

- monolithic : In monolithic IC's devices are mounted on a single piece semiconductor material.
- hybrid : In hybrid IC's devices are interconnected with the use of bonding wires deposited on insulating substrate.

- Examples of Op-amps IC's

<u>Manufacturers</u>	<u>IC number</u>
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Fairchild	μ A741
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National Semiconductors	LH741
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Motorola	MC1741
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RCA	CA3741
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Texas Instruments	SN52741
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Signetics	N5741
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- Types of Integrated Circuit Packages

- Flat top

- Metal can (BJT's and FET's)

- Dual in line package (Op-amps)

- History

1940 - First Op-amp : used in analog computers

1948 - using vacuum tubes

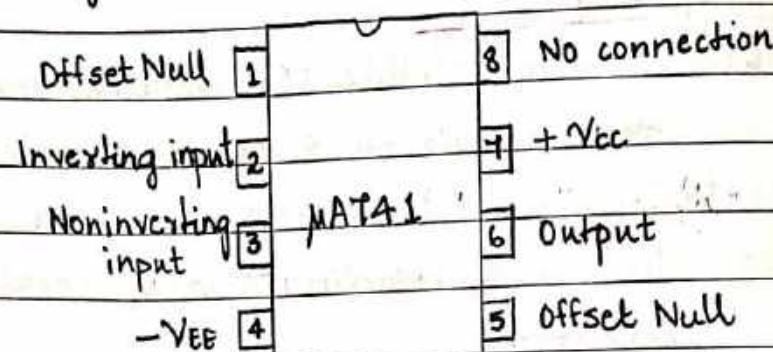
Since vacuum tubes are large in size, expensive and consume more power it was converted into single integrated circuit.

1964-1968 - Robert J Widlar (IC's)

Features of Op-amps

- * direct coupled multistage voltage amplifier with extremely high gain.
- * it has very high input impedance and very low output impedance.

Pin Diagram



Op amps require dual power supply for operation, they can be $\pm 9V$, $\pm 12V$, $\pm 15V$ or $\pm 22V$.

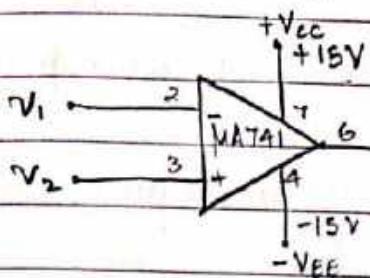
Purpose of offset null

On short circuiting the two input pins (2 and 3) the output should be zero but in some cases the output is not zero. In such cases both the offset null pins are connected to each other through potentiometer. On varying the value of the potentiometer the output can be obtained as zero.

Various Parameters of Op-Amps:

	Parameters	Ideal	Practical
1.	Open loop voltage gain : A	∞	2×10^6
2.	Input resistance : R_i	∞	$2M\Omega$
3.	Output resistance : R_o	0	45.5Ω
4.	Input offset current : I_{io}	0	$20nA$
5.	Input bias current : I_B	0	$80nA$
6.	Input offset voltage : V_{io}	0	$2mV$
7.	CMRR : CMRR, S	∞	$90dB$
8.	Bandwidth : BW	∞	$1MHz$
9.	Slew-rate : SR	∞	$0.5V/\mu s$
10.	Power supply Rejection Ratio: PSRP	0	$30\mu V/V$

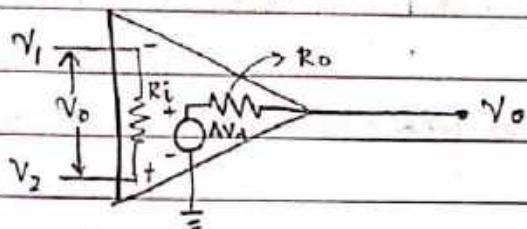
Differential voltage



$$V_d = A(V_2 - V_1) = AV_d$$

V_d - differential voltage.

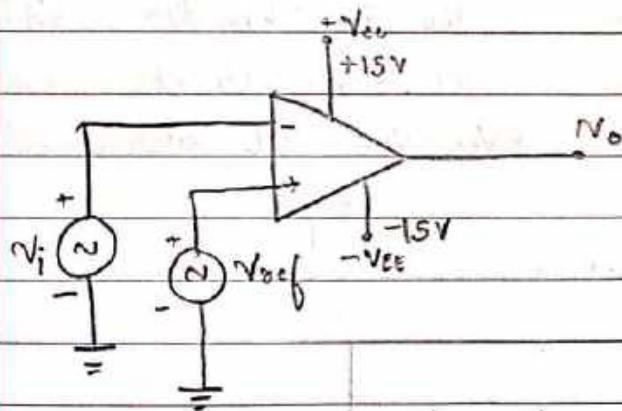
Equivalent circuit for μA741



Saturable property of Op-Amp:

$$V_d = AV_d = 2 \times 10^5 (V_2 - V_1)$$

$$V_d = \pm 15 - 1.5V \Rightarrow +13.5V; -13.5V.$$



$V_i > V_{ref}$: positive saturation

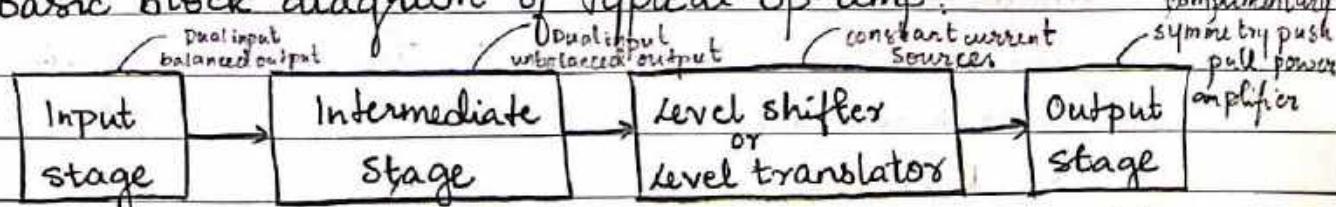
Output voltage = +13.5V

$V_i < V_{ref}$: negative saturation

Output voltage = -13.5V

* Differential Amplifier:

Basic block diagram of typical Op-amp.



Input: Dual input balanced output differential amplifier
(high gain and high input resistance)

Intermediate: Dual input unbalanced output differential amplifier.

Level Shifter: Such as emitter follower using constant current source.

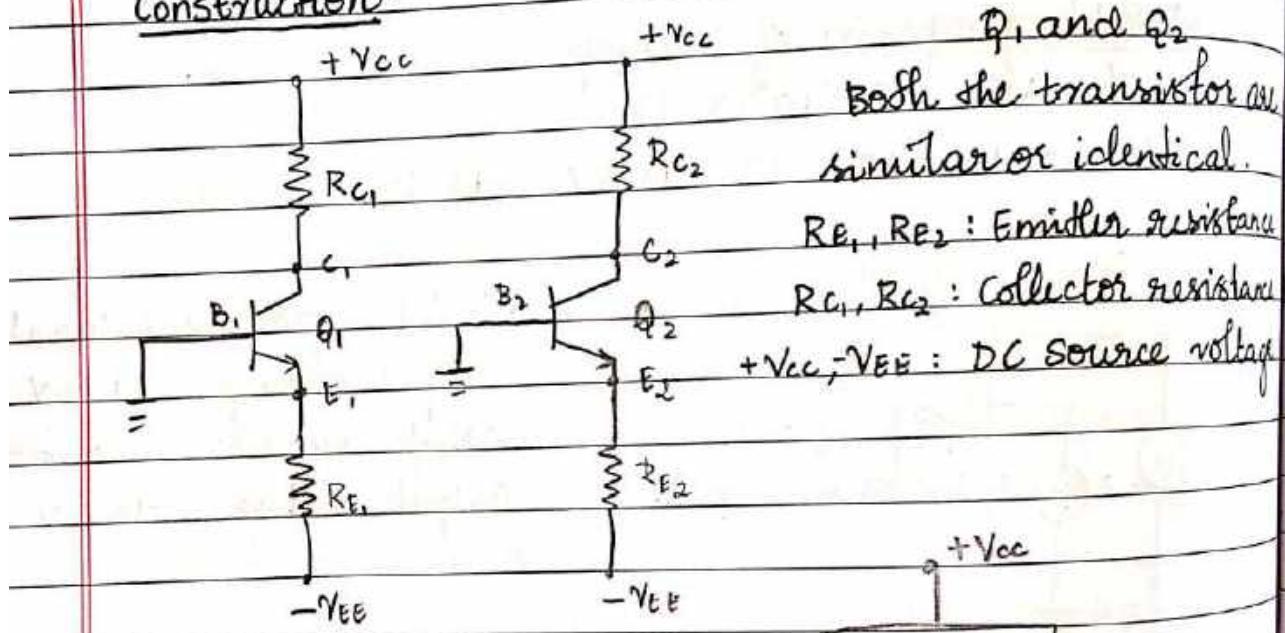
Output: Complementary symmetry push pull amplifier (low output resistance)

- Common Mode Rejection Ratio: CMRR

$$\text{CMRR} : 8 = \frac{A_d}{A_c} \geq 20 \log \left| \frac{A_d}{A_c} \right| \text{dB} \quad (\text{in dB})$$

- Differential amplifier amplifies the differential voltage of the two inputs.

Construction:



collector resistance

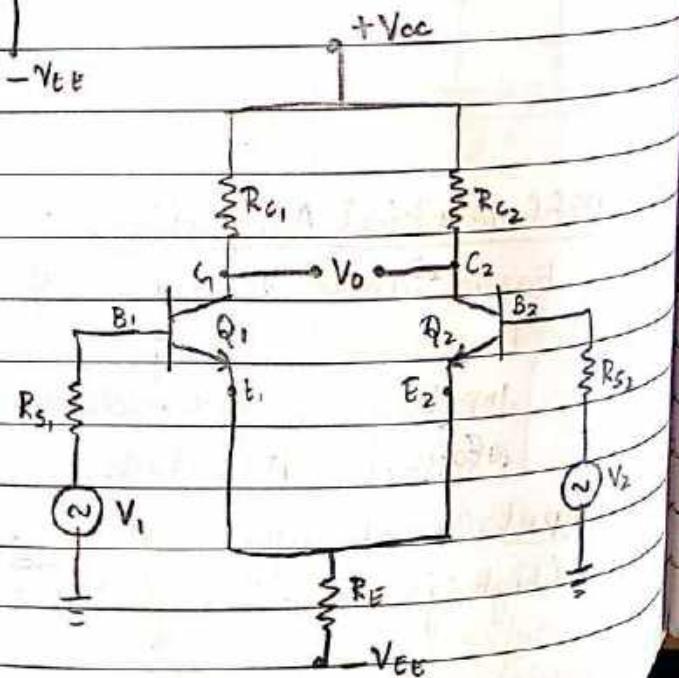
$$R_c = R_{c1} = R_{c2}$$

Emitter resistance

$$R_E = R_{E1} \parallel R_{E2}$$

source resistance

$$R_S = R_{S1} = R_{S2}$$



Balanced output : when the output is analysed, between both the collectors are at same potential C_1 and C_2 .

Unbalanced output : when the output is analysed, between one of the collector (C_1 or C_2) and ground.

Applications

- used as phase-splitter amplifier.

- noise can be reduced. (by given common input).

Phase Splitter Amplifier:

→ V_o with respect to $V_1 \Rightarrow V_2 = 0$

$$\text{wkt } V_o = A(V_1 - V_2)$$

$$\therefore V_o = AV_1$$

Here the output is positive, hence the output is in phase.

→ V_o with respect to $V_2 \Rightarrow V_1 = 0$

$$\text{wkt } V_o = A(V_1 - V_2)$$

$$\therefore V_o = -AV_2$$

Here the output is negative, hence the output is out of phase with a phase difference of 180° .

Different modes of Operation:

common Mode Rejection Ratio

$$\text{CMRR} = \frac{A_d}{A_c}$$

$$A_d = A(V_1 - V_2)$$

$$A_d = AV_d \quad (\because V_d = V_1 - V_2)$$

$$A_c = AV_c \quad (V_c = \frac{V_1 + V_2}{2})$$

$$\therefore V_o = A_d V_d + A_c V_c$$

$$V_o = A_d V_d \left[1 + \frac{A_c V_c}{A_d V_d} \right]$$

$$V_o = A_d V_d \left[1 + \frac{1}{\text{CMRR}} \left(\frac{V_c}{V_d} \right) \right]$$

Q: calculate the CMRR, and CMRR in dB for the values
 $A_d = 6000$ and $A_u = 15$.

Sol:
$$\text{CMRR} = \frac{A_d}{A_u} = \frac{6000}{15} = 400$$

$$\text{CMRR}_{\text{dB}} = 20 \log \left| \frac{A_d}{A_u} \right| = 20 \log |400| = 52.04$$

- Analysis of Differential Amplifiers:
 (Balanced input balanced output)
 Dual

1. Gain

$$A_d = \frac{V_o}{V_i - V_2} \quad A_u = \frac{V_o}{V_i}$$

2. Input resistance

$$R_{i1} = \left| \frac{V_{i1}}{I_{b1}} \right| \quad R_{i2} = \left| \frac{V_{i2}}{I_{b2}} \right|$$

3. Output resistance.

D.C. Analysis (same for all

To find I_{CQ} (the configurations)

Applying KVL to the

left hand side loop

$$R_s I_b + V_{BE} + 2 I_E R_E = V_{EE}$$

$$V_{EE} - R_s I_b + V_{BE} - 2 I_E R_E = 0$$

$$\text{wkt } h_{fe} = \frac{I_c}{I_b} = \beta_{dc}$$

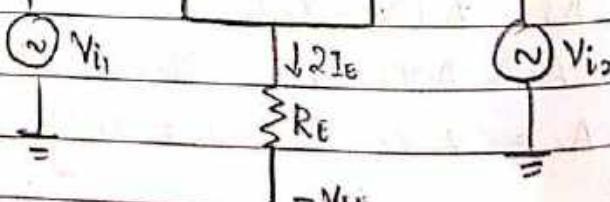
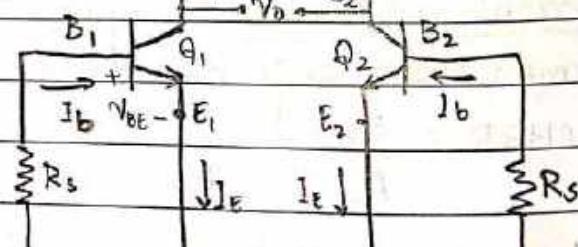
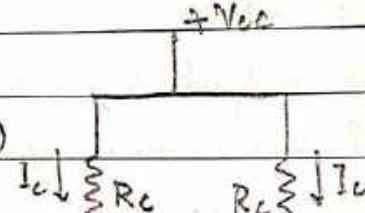
$$V_{EE} - \frac{I_c R_s}{\beta_{dc}} - V_{BE} - 2 I_E R_E = 0$$

$$V_{EE} - V_{BE} = \frac{I_c R_s + 2 I_E R_E}{\beta_{dc}}$$

$$\text{wkt } I_E \approx I_c$$

$$V_{EE} - V_{BE} = \frac{I_E R_s + 2 I_E R_E}{\beta_{dc}}$$

$$V_{EE} - V_{BE} = I_E \left[\frac{R_s}{\beta_{dc}} + 2 R_E \right]$$



D.C. analysis

$$\therefore V_{i1} = V_{i2} = 0$$

$$\therefore I_E = \frac{V_{EE} - V_{BE}}{\frac{R_s}{\beta_{dc}} + 2R_E}$$

For faithful amplification

$$\frac{R_s}{\beta_{dc}} \ll 2R_E, \text{ therefore } R_s \text{ is neglected.}$$

$$\therefore I_E = \frac{V_{EE} - V_{BE}}{2R_E}$$

$$\Rightarrow I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E}$$

$$V_{CE} = V_C - V_E$$

$$\text{but } V_C = V_{CC} - I_C R_C$$

$$V_E \approx -V_{BE}$$

$$\therefore V_{CEQ} = V_{CC} - I_C R_C - (-V_{BE})$$

$$\boxed{V_{CEQ} = V_{CC} + V_{BE} - I_C R_C}$$

Q: For a differential amplifier shown determine I_{CQ} and V_{CEQ} , assume silicon transistor.

sol:

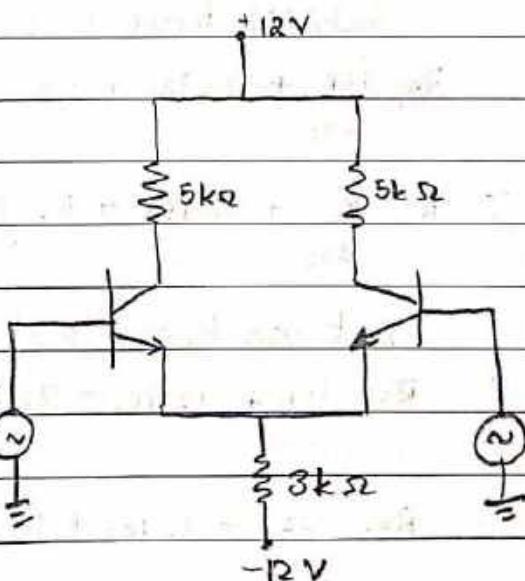
$$I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E}$$

$$I_{CQ} = \frac{12 - 0.7}{2(3k)} = 1.883 \text{ mA}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$$

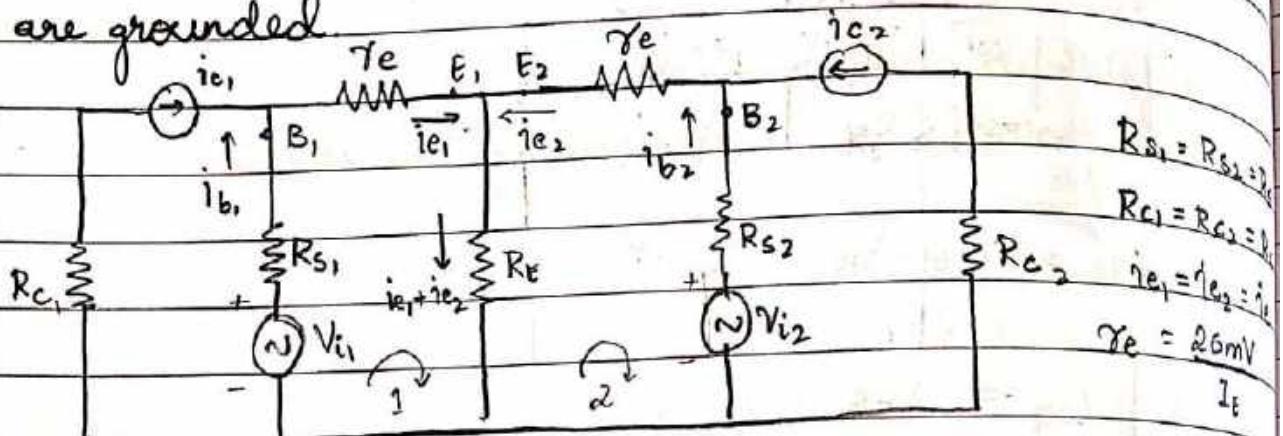
$$V_{CEQ} = 12 + 0.7 - (1.883 \text{ mA})(5k)$$

$$\underline{\underline{V_{CEQ} = 3.85 \text{ V}}}$$



AC analysis

All dc sources
are grounded.

Equivalent ac model

Applying KVL to loop 1

$$R_S i_{b1} + \gamma_e i_{e1} + R_E (i_{e1} + i_{e2}) = V_{i1} \quad \text{--- (1)}$$

Applying KVL to loop 2

$$R_S i_{b2} + \gamma_e i_{e2} + R_E (i_{e1} + i_{e2}) = V_{i2} \quad \text{--- (2)}$$

$$\text{wkt } h_{FE} = \beta_{AC} = \frac{i_C}{I_B} \Rightarrow I_B = \frac{i_C}{\beta_{AC}}$$

$$\therefore i_{b1} = \frac{i_{C1}}{\beta_{AC}} \text{ and } i_{b2} = \frac{i_{C2}}{\beta_{AC}}$$

Substituting in eq. (1) and eq. (2)

$$R_S \frac{i_{C1}}{\beta_{AC}} + \gamma_e i_{e1} + R_E (i_{e1} + i_{e2}) = V_{i1}$$

$$R_S \frac{i_{C2}}{\beta_{AC}} + \gamma_e i_{e2} + R_E (i_{e1} + i_{e2}) = V_{i2}$$

but we know that $i_{C1} \approx i_{e1}$ and $i_{C2} \approx i_{e2}$

$$\therefore R_S \frac{i_{e1}}{\beta_{AC}} + \gamma_e i_{e1} + R_E (i_{e1} + i_{e2}) = V_{i1}$$

$$R_S \frac{i_{e2}}{\beta_{AC}} + \gamma_e i_{e2} + R_E (i_{e1} + i_{e2}) = V_{i2}$$

since $\frac{R_{S1}}{\beta_{AC}}$ and $\frac{R_{S2}}{\beta_{AC}}$ is very small, it can be neglected

$$\gamma_e i_{e1} + R_E (i_{e1} + i_{e2}) = V_{i1} \quad \text{--- (3)}$$

$$\gamma_e i_{e2} + R_E (i_{e1} + i_{e2}) = V_{i2} \quad \text{--- (4)}$$

$$\text{eq. ③: } i_{e_1}(\gamma_e + R_E) + i_{e_2}R_E = V_{i_1} \quad \text{--- (5)}$$

$$\text{eq. ④: } i_{e_2}(\gamma_e + R_E) + i_{e_1}R_E = V_{i_2} \quad \text{--- (6)}$$

Applying Cramer's rule to eq. ⑤ and eq. ⑥

$$\Delta = \begin{vmatrix} \gamma_e + R_E & R_E \\ R_E & \gamma_e + R_E \end{vmatrix} = (\gamma_e + R_E)^2 - R_E^2$$

$$i_{e_1} = \begin{vmatrix} V_{i_1} & R_E \\ V_{i_2} & \gamma_e + R_E \end{vmatrix}$$

 Δ_1

$$i_{e_1} = \frac{V_{i_1}(\gamma_e + R_E) - V_{i_2}R_E}{(\gamma_e + R_E)^2 - R_E^2} \quad \text{--- (7)}$$

$$i_{e_2} = \begin{vmatrix} \gamma_e + R_E & V_{i_1} \\ R_E & V_{i_2} \end{vmatrix}$$

 Δ_2

$$i_{e_2} = \frac{V_{i_2}(\gamma_e + R_E) - V_{i_1}R_E}{(\gamma_e + R_E)^2 - R_E^2} \quad \text{--- (8)}$$

For balanced output

$$V_o = V_{C_2} - V_{C_1}$$

$$V_o = -i_{C_2}R_{C_2} - (-i_{C_1}R_{C_1})$$

$$V_o = R_C(i_{C_1} - i_{C_2}) \quad \text{because } R_{C_1} = R_{C_2} = R_C$$

considering $i_{C_1} \approx i_{e_1}$ and $i_{C_2} \approx i_{e_2}$

$$V_o = R_C(i_{e_1} - i_{e_2})$$

Substituting eq. ⑦ and eq. ⑧

$$V_o = R_C \left[\frac{V_{i_1}(\gamma_e + R_E) - V_{i_2}R_E - V_{i_2}(\gamma_e + R_E) + V_{i_1}R_E}{(\gamma_e + R_E)^2 - R_E^2} \right]$$

$$V_o = R_C \left[\frac{V_{i_1}\gamma_e + V_{i_1}R_E - V_{i_2}R_E - V_{i_2}\gamma_e - V_{i_2}R_E + V_{i_1}R_E}{(\gamma_e + R_E)^2 - R_E^2} \right]$$

$$V_o = R_C \left[\frac{\gamma_e(V_{i_1} - V_{i_2}) + 2R_E(V_{i_1} - V_{i_2})}{(\gamma_e + R_E)^2 - R_E^2} \right]$$

$$V_o = R_C(V_{i_1} - V_{i_2}) \left[\frac{\gamma_e + 2R_E}{(\gamma_e + 2R_E)(\gamma_e)} \right]$$

$$V_o = R_C(V_{i_1} - V_{i_2}) \frac{\gamma_e}{\gamma_e + 2R_E}$$

$$\text{wkt } V_d = V_{i1} - V_{i2}$$

$$\therefore V_o = \frac{R_c V_d}{g_e}$$

$A_d = \frac{V_o}{V_d} = \frac{R_c}{g_e}$

Gain of differential amplifier

Input resistance

$$R_{i1} = \left| \frac{V_{i1}}{i_{b1}} \right|_{V_{i2}=0}$$

$$R_{i2} = \left| \frac{V_{i2}}{i_{b2}} \right|_{V_{i1}=0}$$

$$\text{wkt } i_{b1} = \frac{i_{e1}}{\beta_{ac}} \text{ and } i_{b2} = \frac{i_{e2}}{\beta_{ac}}$$

$$\therefore R_{i1} = \frac{V_{i1} \beta_{ac}}{i_{e1}} \quad R_{i2} = \frac{V_{i2} \beta_{ac}}{i_{e2}}$$

Substituting i_{e1} and i_{e2} (eq. ④ and ⑤)

$$R_{i1} = \frac{V_{i1} \beta_{ac}}{\frac{V_{i1}(\gamma_e + R_E) - V_{i2} R_E^2}{(R_E + R_E)^2 - R_E^2}}$$

$$R_{i1} = \frac{V_{i1} \beta_{ac} [(R_E + R_E)^2 - R_E^2]}{V_{i1} (\gamma_e + R_E)}$$

$$R_{i1} = \frac{\beta_{ac}}{\gamma_e + R_E} [(\gamma_e + 2R_E) \gamma_e]$$

Since $R_E \gg r_e$

$$R_{i1} = \frac{\beta_{ac} (2R_E r_e)}{r_e + R_E}$$

$R_{i1} = \frac{2r_e \beta_{ac}}{R_E}$	similarly	$R_{i2} = \frac{2r_e \beta_{ac}}{R_E}$
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Output resistance

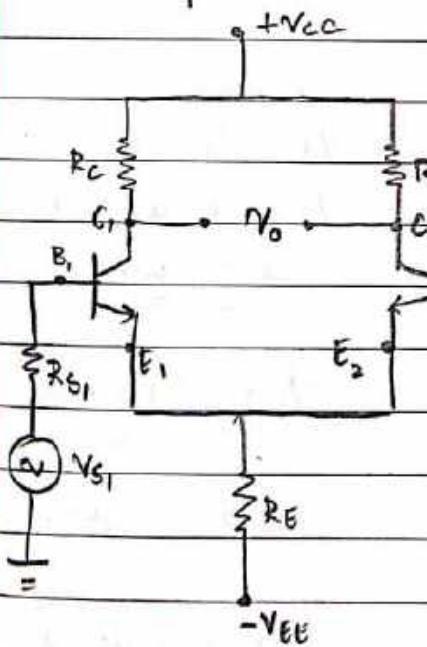
The output is taken across the two collector terminals

$$\therefore R_{o1} = R_{c1} = R_C$$

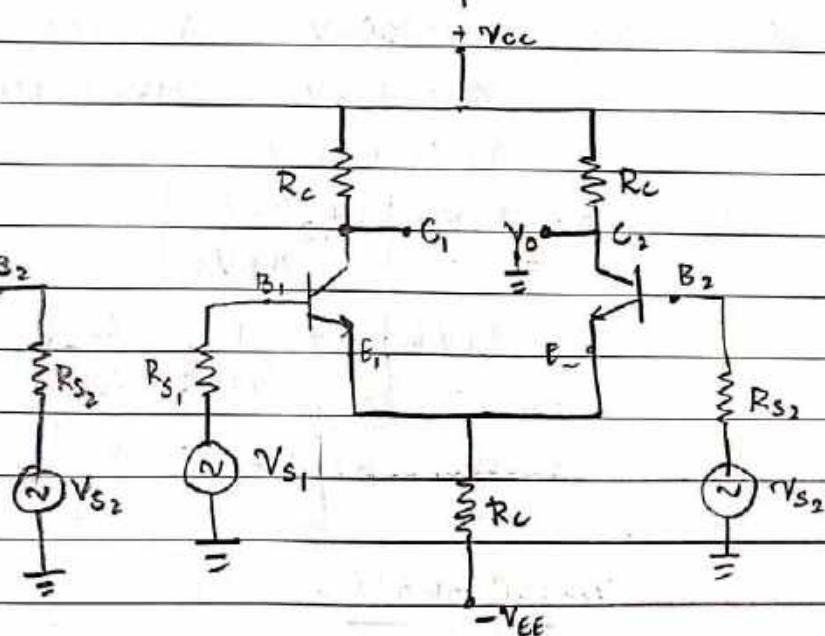
$$R_{o2} = R_{c2} = R_C$$

Configuration	Gain (A_d)	Input resistance	Output resistance
1. Dual input balanced output.	$A_d = \frac{R_c}{2r_e}$	$R_i = 2r_e \beta_{ac}$ $r_e \gg r_e$	$R_{o1} = R_{o2} = R_c$
2. Dual input unbalanced output.	$A_d = \frac{R_c}{2r_e}$	$R_i = 2r_e \beta_{ac}$	$R_o = R_c$
3. Single input balanced output.	$A_d = \frac{R_c}{2r_e}$	$R_i = 2r_e \beta_{ac}$	$R_o = R_c$
4. Single input unbalanced output	$A_d = \frac{R_c}{2r_e}$	$R_i = 2r_e \beta_{ac}$	$R_o = R_c$

1. Dual input balanced output.



2. Dual input unbalanced output.

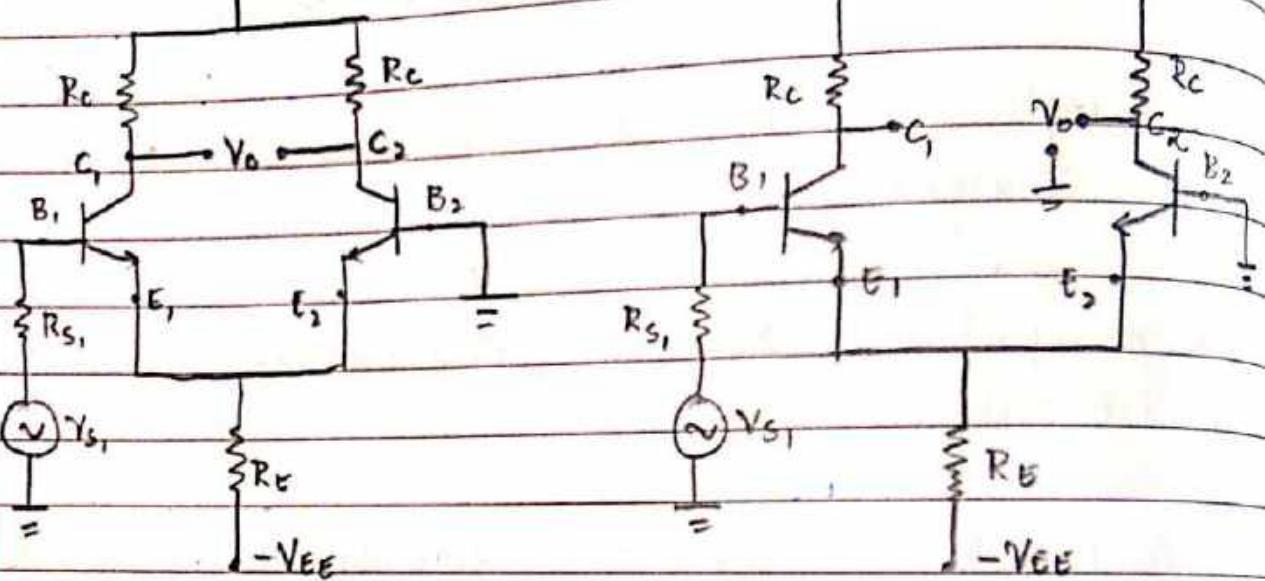


3. Single Input balanced output

+V_{cc}

4. Single Input unbalance output.

+V_{cc}



Q: Determine the output voltage of an op-amp given input voltage with $V_{i_1} = 200\mu V$ and $V_{i_2} = 140\mu V$. The amp has differential gain of 6000 and CMRR = 200

Sol:

$$\text{Given: } V_{i_1} = 200\mu V \quad A_d = 6000$$

$$V_{i_2} = 140\mu V \quad \text{CMRR} = 200$$

$$V_o = A_d V_d + A_c V_c$$

$$V_o = A_d V_d \left[1 + \frac{A_c V_c}{A_d V_d} \right]$$

$$V_o = A_d V_d \left[1 + \frac{1}{\text{CMRR}} \frac{V_c}{V_d} \right]$$

$$V_o = 6000(60\mu) \left[1 + \frac{140\mu}{200 \times 60\mu} \right]$$

$$V_o = 0.365V$$

$$V_d = V_{i_1} - V_{i_2}$$

$$V_d = 200\mu V - 140\mu V$$

$$V_d = 60\mu V$$

$$V_c = \frac{V_{i_1} + V_{i_2}}{2}$$

$$V_c = \frac{200\mu + 140\mu}{2}$$

$$V_c = 170\mu V$$

- Q: Calculate the output voltage of a differential amplifier in
 i. differential mode.
 ii. common mode.

Given differential gain of an amplifier is 45 dB and CMRR is 70 dB. The input voltage are $V_1 = 1.5 \mu V$ and $V_2 = 1.2 \mu V$.

Sol: Given: $CMRR = 70 \text{ dB}$ $V_1 = 1.5 \mu V$
 $A_d = 45 \text{ dB}$ $V_2 = 1.2 \mu V$

i. differential mode

$$\begin{aligned} V_d &= (V_1 - V_2) A_d & A_d \text{ dB} &= 20 \log_{10} A_d \\ V_d &= (1.5 \mu V - 1.2 \mu V) A_d & 45 &= 20 \log_{10} A_d \\ V_d &= (0.3 \mu V)(5623.41) & \log_{10} A_d &= 3.45 \\ \underline{V_d} &= \underline{1.687 \mu V} & \underline{A_d} &= \underline{5623.41} \end{aligned}$$

ii. common mode

$$\begin{aligned} V_o &= A_c V_c & V_c &= \frac{V_1 + V_2}{2} = \frac{1.5 \mu V + 1.2 \mu V}{2} \\ V_o &= 1.478 (1.35 \mu V) & \underline{V_c} &= \underline{1.35 \mu V} \\ \underline{V_o} &= \underline{2.4 \mu V} & & \end{aligned}$$

$$CMRR_{dB} = 20 \log_{10} \left| \frac{A_d}{A_c} \right|$$

$$\begin{aligned} 70 &= 20 \log_{10} CMRR \\ \underline{CMRR} &= \underline{3162.27} \end{aligned}$$

$$CMRR = \frac{A_d}{A_c}$$

$$A_c = \frac{A_d}{CMRR} = \frac{5623.41}{3162.27}$$

$$\underline{A_c} = \underline{1.478}$$

Analysing the configurations using hybrid model

$$I_C = \left[\frac{h_{FE}}{1+h_{FE}} \right] I_E$$

$$A_d = \frac{h_{FE} R_C}{R_S + h_{IE}} \quad (\text{differential mode})$$

$$R_i = 2 [R_S + h_{IE}]$$

$$R_o = R_C$$

$$A_c = \frac{h_{FE} R_C}{2 R_E (1+h_{FE}) + R_S + h_{IE}} \quad (\text{common mode})$$

Q: For a dual input balanced output differential amplifier with $h_{FE} = 100$ for silicon transistor, find Q point values, differential and common mode gain, differential input and output impedance and CMRR.

Given: $R_C = 4.4 k\Omega$, $R_E = 3.3 k\Omega$, $R_{S1} = R_{S2} = 100 \Omega$.

Take $V_{CC} = 12V$ and $V_{EE} = 12V$. Also $h_{IE} = 1.4 k\Omega$.

Sol:

$$\text{Given: } h_{FE} = 100$$

$$R_E = 4.4 k\Omega$$

$$V_{CC} = 12V$$

$$h_{IE} = 1.4 k\Omega$$

$$R_E = 3.3 k\Omega$$

$$V_{EE} = 12V$$

$$R_S = 100 \Omega$$

i. Q point values

$$I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E} = \frac{12 - 0.7}{2(3.3)k} = 1.712 \text{ mA}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_{CQ} R_C$$

$$= 12 + 0.7 - (1.712 \text{ mA})(4.4 k)$$

$$V_{CEQ} = 7.6536 V$$

ii. Differential mode gain

$$A_d = \frac{h_{fe} R_c}{R_s + h_{ie}}$$

$$A_d = \frac{100(4.7k)}{100 + 1.4k}$$

$$\underline{A_d = 313.33}$$

Common mode gain

$$A_c = \frac{h_{fe} R_E}{2 R_E (1 + h_{fe}) + R_s + h_{ie}}$$

$$A_c = \frac{100(4.7k)}{2(3.3k)(1+100) + 100 + 1.4k}$$

$$\underline{A_c = 0.4034}$$

iii. differential input impedance

$$R_i = 2[R_s + h_{ie}]$$

$$R_i = 2[100 + 1.4k]$$

$$\underline{R_i = 3k\Omega}$$

differential output impedance

$$Z_o = R_c = 4.7k\Omega$$

iv. CMRR = $\frac{A_d}{A_c} = \frac{313.33}{0.4034} = 445.45$

Q: For a dual input unbalanced output differential amplifier

$V_{cc} = 13V$ and $-V_{EE} = -13V$ and $R_c = 4.7k\Omega$ and $R_E = 6.8k\Omega$ and $R_s = 15\Omega$. Determine Q point values, voltage gain, differential input resistance, output resistance. Take $h_{fe} = 300$, $h_{ie} = 20k\Omega$ and $V_{BE} = 0.4V$.

Sol: Given: $V_{cc} = 13V$ $R_c = 4.7k\Omega$ $h_{ie} = 20k\Omega$
 $-V_{EE} = -13V$ $R_E = 6.8k\Omega$ $h_{fe} = 300$
 $R_s = 15\Omega$

i. Q point values

$$I_{cq} = \frac{V_{EE} - V_{BE}}{2 R_E} = \frac{13 - 0.4}{2(6.8)k} = 0.904mA$$

$$V_{ceq} = V_{cc} + V_{BE} - I_{cq} R_c \\ = 13 + 0.4 - (0.904mA) 4.7k$$

$$\underline{\underline{V_{ceq} = 9.45V}}$$

ii. voltage gain

$$A_d = \frac{h_{FE} R_c}{2(R_s + h_{ie})}$$

$$A_d = \frac{300(4.4k)}{2(15+20k)}$$

$$= \frac{35.22}{2}$$

$$\underline{\underline{A_d = 35.22}}$$

since

For unbalanced configuration

$$A_d = \frac{h_{FE} R_c}{2(R_s + h_{ie})}$$

$$= \frac{35.22}{2}$$

iii. Differential input resistance

$$R_i = 2 [R_s + h_{ie}]$$

$$= 2 [15 + 20k]$$

$$\underline{\underline{R_i = 40.03k\Omega}}$$

iv. Differential output resistance

$$R_o = R_c = 4.4k\Omega$$

* Swamping Resistors

A_d is dependent on R_c and r_e . we need to make sure that it is less dependent on r_e this can be done by using swamping resistors R'_E .

This is done because change in r_e causes alteration of gain A_d and input resistance R_i .

DE Analysis:

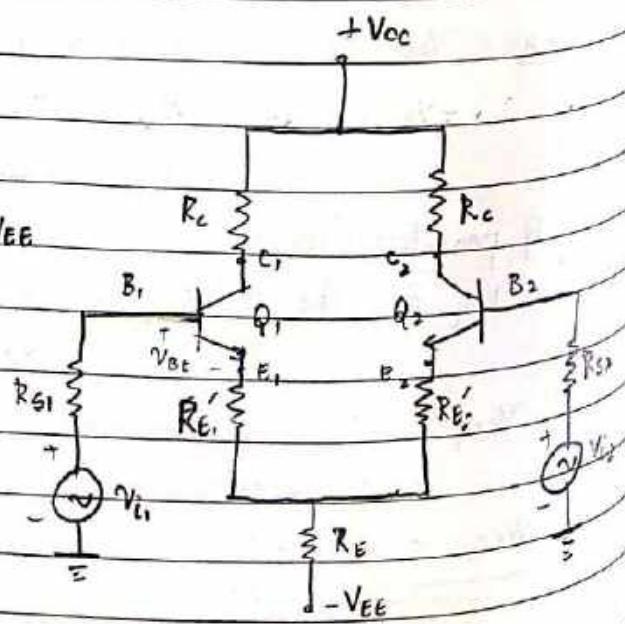
$$V_{i_1} = 0 \text{ and } V_{i_2} = 0$$

Applying KVL to input loop 1.

$$R_s I_B + V_{BE} + R_E' I_E + 2I_E R_E = V_{EE}$$

$$\text{volt } I_B = \frac{I_E}{\beta_{dc}}$$

$$\frac{R_s I_E}{\beta_{dc}} + R_E' I_E + 2I_E R_E = V_{EE} - V_{BE}$$



$$I_E = \frac{V_{EE} - V_{BE}}{R_E' + 2R_E + \frac{R_s}{\beta_{dc}}}$$

Since R_s/β_{dc} is very small

$$I_E = \frac{V_{EE} - V_{BE}}{R_E' + 2R_E}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$$

AC analysis

$$A_d = \frac{R_C}{r_e}$$

Here r_e is replaced by $r_e + R_E'$

$$A_d = \frac{R_C}{r_e + R_E'} \quad \text{Gain}$$

$$R_{i1} = R_{i2} = R_i$$

$$R_i = 2r_e \beta_{dc}$$

Here r_e is replaced by $r_e + R_E'$

$$R_i = 2\beta_{dc} (r_e + R_E') \quad \text{Input resistance}$$

$$R_{o1} = R_{o2} = R_o = R_C \quad \text{Output resistance}$$

q: The following specifications are given for dual input balanced output differential amplifier.

$$R_C = 2.2k\Omega, R_E = 4.4k\Omega \text{ when } R_{in1} = R_{in2} = 50\Omega$$

$$+V_{CC} = 10V, -V_{EE} = -10V \text{ with } \beta_{dc} = \beta_{ac} = 100 \text{ and}$$

$$V_{BE} = 0.715V, R_E' = 100\Omega$$

a. Determine I_{CQ} and V_{CEQ}

b. Voltage gain

c. Input and output resistance.

Sol: For dual input balanced output without swamping resistors

$$a. I_{CQ} = \frac{V_{CE} - V_{BE}}{2R_E + R_{in}/\beta_{dc}}$$

$$I_{CQ} = \frac{10 - 0.715}{2(4.7k) + \frac{50}{100}}$$

$$\underline{\underline{I_{CQ} = 0.984mA}}$$

$$V_{CEQ} = V_{CC} + V_{BE} - R_C I_{CQ}$$

$$V_{CEQ} = 10 + 0.715 - (2.2k)(0.984)m$$

$$\underline{\underline{V_{CEQ} = 8.54V}}$$

$$b. A_d = \frac{R_C}{r_e}$$

$$r_e = \frac{26mV}{I_E} = \frac{26m}{0.984m} =$$

$$A_d = \frac{2.2k}{26.3}$$

$$\underline{\underline{A_d = 83.65}}$$

$$c. R_i = 2r_e\beta_{dc}$$

$$R_o = R_C = 2.2k\Omega$$

$$R_i = 2(26.3)(100)$$

$$\underline{\underline{R_i = 5.26k\Omega}}$$

For dual input balanced output with swamping resistors

$$a. I_{CQ} = \frac{V_{CC} - V_{BE}}{2R_E + R_E' + R_{in}/\beta_{dc}}$$

$$I_{CQ} = \frac{10 - 0.715}{2(4.7k) + 100 + \frac{50}{100}}$$

$$\underline{\underline{I_{CQ} = 0.974mA}}$$

$$V_{AEQ} = V_{AC} + V_{BE} - R_C I_{CA}$$

$$\underline{V_{CEQ} = 8.51 \text{ V}}$$

b. $A_d = \frac{R_C}{r_e + R_E'}$

$$A_d = \frac{2.2k}{26.3 + 100}$$

$$\underline{\underline{A_d = 17.42}}$$

c. $R_i = 2(r_e + R_E')\beta_{DC}$

$$R_i = 2(26.3 + 100)(100)$$

$$\underline{\underline{R_i = 25.26 k\Omega}}$$

$$R_o = R_C = 2.2k\Omega$$

Disadvantage and Advantage

the gain decreases whereas the input resistance will be high with swamping resistors.

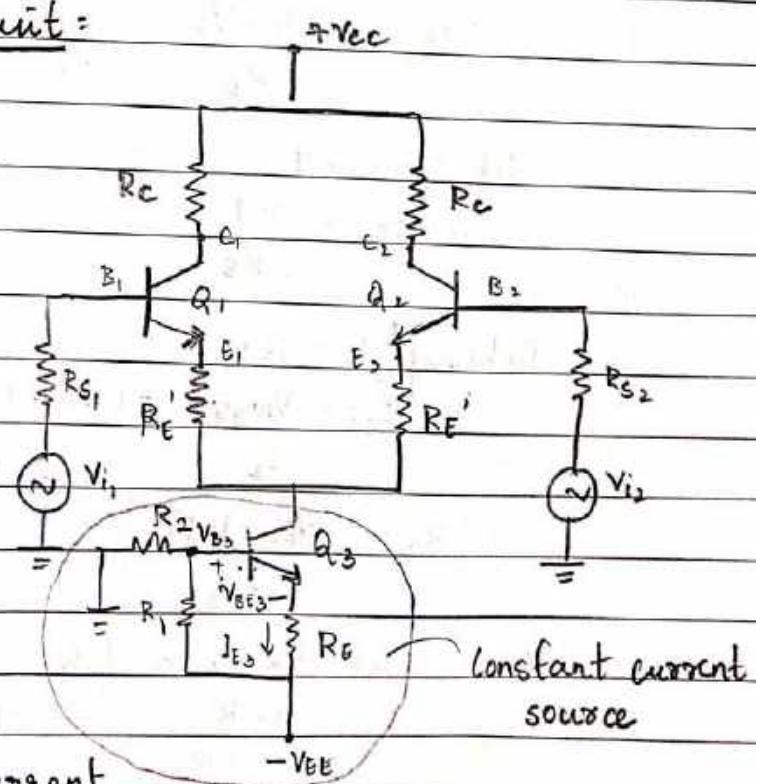
* constant current Bias Circuit:

A constant current source

is a power generator whose internal resistance is very high compared to the load it is giving power to.

Due to this it can supply a constant current to a load whose resistance value varies even over a wide range.

This comes in use when a circuit needs a steady current supply without fluctuations.



Constant current source

constant current bias with compensating diodes

$$I_A = I_D + I_{B3}$$

$$V_{D3} = 2V_D - V_{EE} \quad \text{--- (1)}$$

$$V_{E3} = V_{B3} - V_{BE3} \quad \text{--- (2)}$$

Substituting eq (1) in eq (2)

$$V_{E3} = 2V_D - V_{EE} - V_{BE3} \quad \text{--- (3)}$$

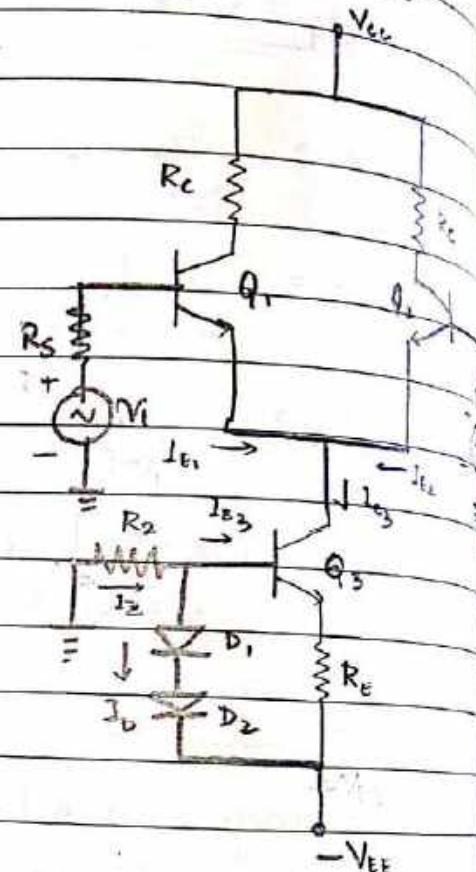
$$I_{E3} = \frac{V_{E3} - (-V_{EE})}{R_E}$$

$$I_{E3} = \frac{V_{E3} + V_{EE}}{R_E} \quad \text{--- (4)}$$

Substituting eq (3) in eq (4)

$$I_{E3} = \frac{2V_D - V_{EE} - V_{BE3} + V_{EE}}{R_E}$$

$I_{E3} = \frac{2V_D - V_{BE3}}{R_E}$



Let the diodes D_1 and D_2 of transistor Q_3 be chosen such that $V_{BE3} = V_D$.

$$\therefore I_{E3} = \frac{2V_D - V_D}{R_E} = \frac{V_D}{R_E}$$

$$\text{Let } V_D = 0.7$$

$$\therefore I_{E3} = \frac{0.7}{R_E}$$

Taking $I_2 = I_{E3}$

$$R_2 = \frac{-V_{B3}}{I_2} = \frac{-(2V_D - V_{EE})}{I_2} = \frac{V_{EE} - 2V_D}{I_2}$$

$\therefore R_2 = \frac{V_{EE} - 1.4}{I_{E3}}$
--

Voltage at the base of Q_3

$$V_{B3} = \frac{-V_{EE} R_2}{R_1 + R_2} \quad \text{--- (1)}$$

Emitter voltage of Q_3 .

$$\gamma_{E_3} = \gamma_{B_3} - \gamma_{BE_3} \quad \text{--- (2)}$$

substituting eq ① in eq ②

$$V_{E_3} = -\frac{V_{EE} R_2}{R_1 + R_2} - V_{BE_3} \quad \text{--- (3)}$$

$$I_{E_3} = \frac{V_{E_3} - (-V_{EE})}{R_E} = \frac{V_{E_3} + V_{EE}}{R_E} \quad \text{--- (4)}$$

Substituting eq. ③ in eq. ④

$$I_{E_3} = \frac{-V_{EE}R_2 - V_{BE} + V_{EE}}{R_1 + R_2}$$

$$wkt \quad l_{E_3} \approx l_{C_3}$$

$$I_{E_1} = I_{E_2} = \frac{I_{E_3}}{2}$$

$$\therefore I_{E_1} = I_{E_2} = \frac{V_{EE} - V_{EG} R_2}{R_1 + R_2} - \frac{V_{BE_3}}{2R_E}$$

Constant current bias with Zener diode:

$$\gamma_{B_3} = -\gamma_E e + \gamma_z \quad \text{--- (1)}$$

$$V_{t_3} = V_{B3} - V_{BE3} \quad \text{--- (2)}$$

Substituting eq. ① in eq. ②

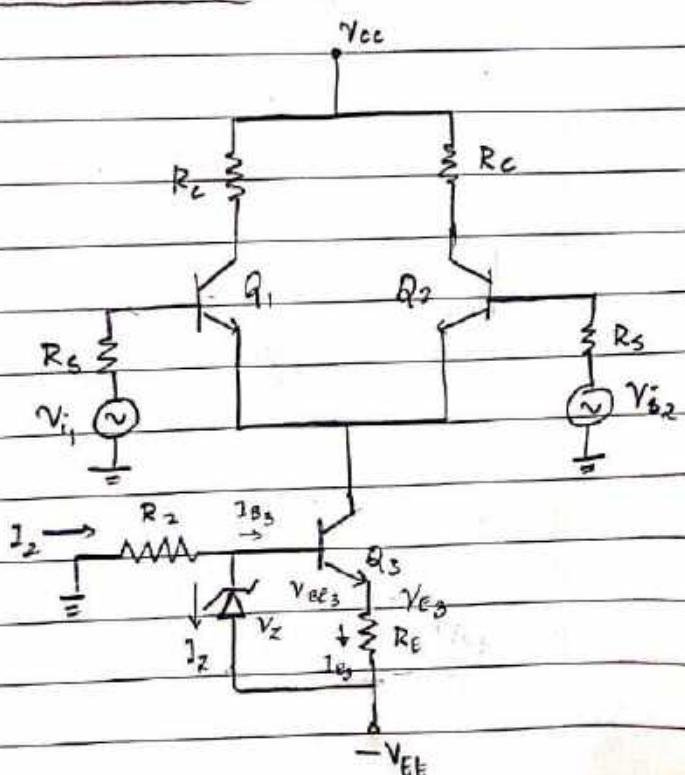
$$V_{E_3} = -V_{EE} + V_Z - V_{BE_3} \quad \text{--- (3)}$$

$$I_{E_3} = \frac{V_{E_3} - (-V_{EE})}{R_F}$$

$$I_{E_3} = \frac{V_{E_3} + V_{CE}}{R_C} \quad \text{--- (4)}$$

Substituting eq.③ in eq.④

$$I_{E_3} = -V_{EE} + V_Z - V_{BE} + V_{EE}$$



$$I_{E_3} = \frac{V_Z - V_{BE3}}{R_E}$$

$$\text{Let } V_{BE_3} = 0.4V$$

$$I_{E_3} = \frac{V_L - 0.7}{R_E}$$

$$\therefore R_E = \frac{\gamma_x - 0.4}{1_{E_3}}$$

considering $I_2 = 1.2 I_1$ — ①

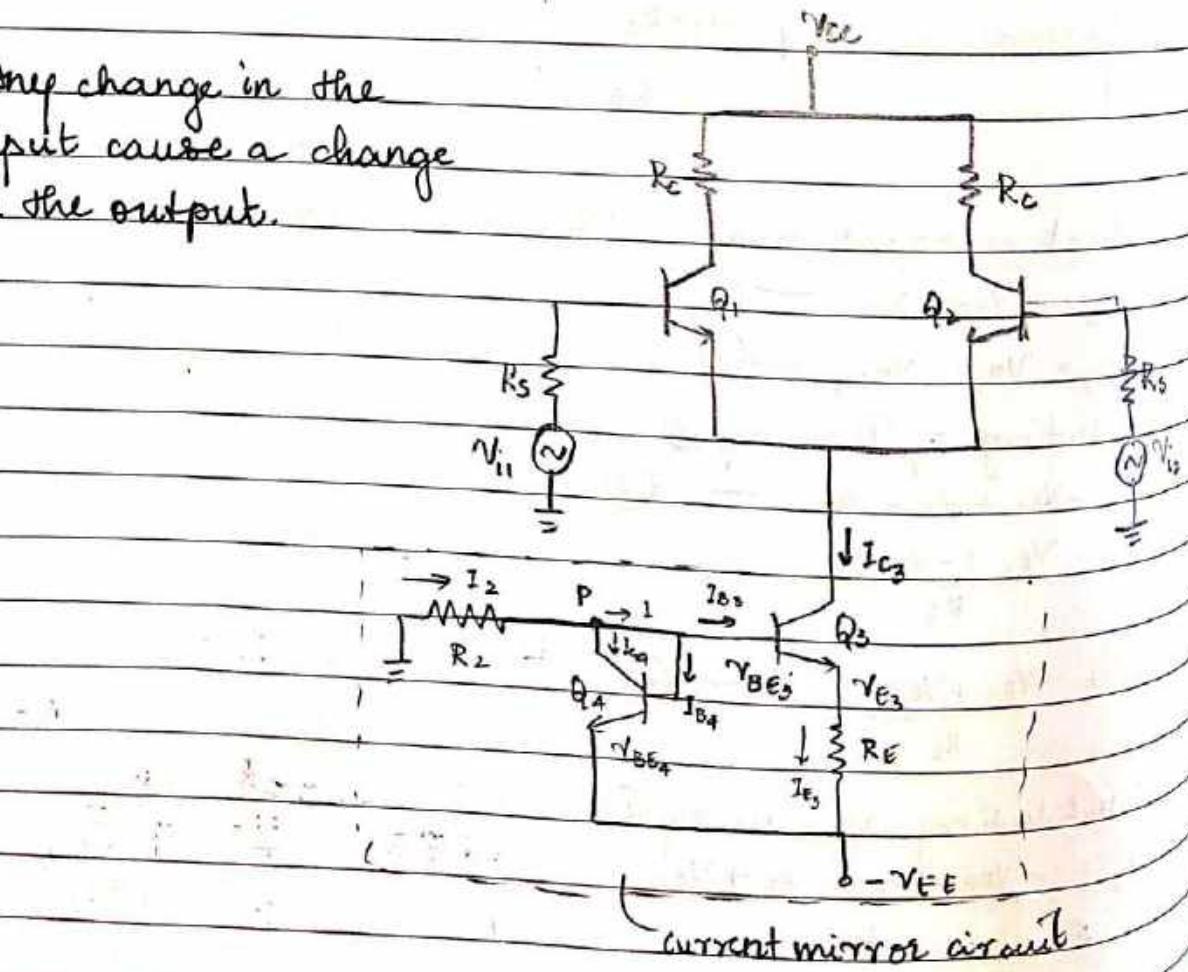
$$R_2 = \frac{V_{EE} - V_x}{I_d} \quad \text{--- (2)}$$

Substituting eq. ① in eq. ②

$$R_2 = \frac{V_{EE} - V_Z}{1.2]_Z}$$

* Current Mirror Circuit:

Any change in the input cause a change in the output.



→ To achieve thermal stability

Transistors Q₃ and Q₄ are identical

$$\therefore V_{BE3} = V_{BE4}$$

$$\Rightarrow I_{B3} = I_{B4}$$

since input is equal, output is equal

$$\therefore I_{C3} = I_{C4}$$

Applying KCL at point P.

$$I_2 = I + I_{C4}$$

$$I_2 = I_{B3} + I_{B4} + I_{C4} \quad (\because I = I_{B3} + I_{B4})$$

$$I_2 = I_{C3} + 2I_{B3} \quad (\because I_{C3} = I_{C4} \text{ and } I_{B3} = I_{B4})$$

$$I_2 = I_{C3} + 2\frac{I_{C3}}{\beta_{dc}} \quad (\because I_{B3} = I_{C3}/\beta_{dc})$$

$$I_2 = I_{C3} \left[1 + \frac{2}{\beta_{dc}} \right]$$

since $2/\beta_{dc}$ is very small

$$I_2 \approx I_{C3} \Rightarrow I_2 \approx I_{C3} = I_C$$

Applying KVL to the base-emitter loop of Q₄.

$$I_2 R_2 + V_{BE4} = V_{EE}$$

$$I_2 = \frac{V_{EE} - V_{BE4}}{R_2}$$

$$R_2 = \frac{V_{EE} - 0.7}{I_2}$$

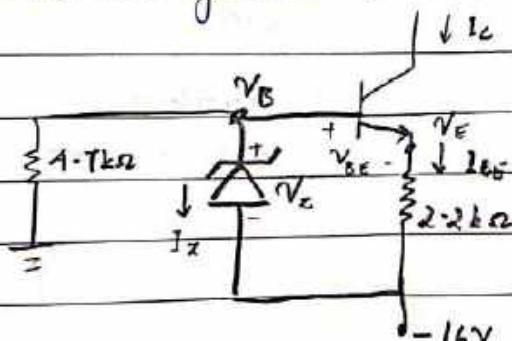
- Q: For the constant current source circuit shown in the figure find the current I_C if the zener voltage is 5V.

Sol: $V_Z = 5V$ (Given)

To find: I_C

$$-V_{EE} = 16V; R_E = 2.2k\Omega$$

$$R_L = 4.7k\Omega$$



$$V_B = -V_{EE} + V_Z$$

$$V_B = -16 + 5 = \underline{\underline{-11V}}$$

$$V_E = V_B - V_{BE}$$

$$V_E = -11 - 0.7 = \underline{\underline{-11.7V}}$$

$$I_E = \frac{V_Z - V_{BE}}{R_E}$$

$$I_E = \frac{5 - 0.7}{2.2k} = \underline{\underline{1.95mA}}$$

$$\underline{\underline{I_E = I_c = 1.95mA}}$$

Q: For the current mirror circuit shown in the figure, find the suitable values of R_2 so that the circuit delivers a constant biasing current of $2mA$ to the transistor of the differential amplifier.

Sol:

Given:

$$-V_{EE} = -20V$$

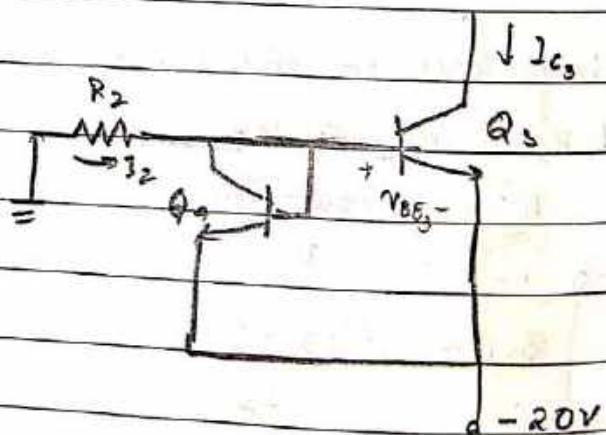
$$I_{C3} = 2mA$$

$$I_2 = \frac{V_{EE} - V_{BE3}}{R_2}$$

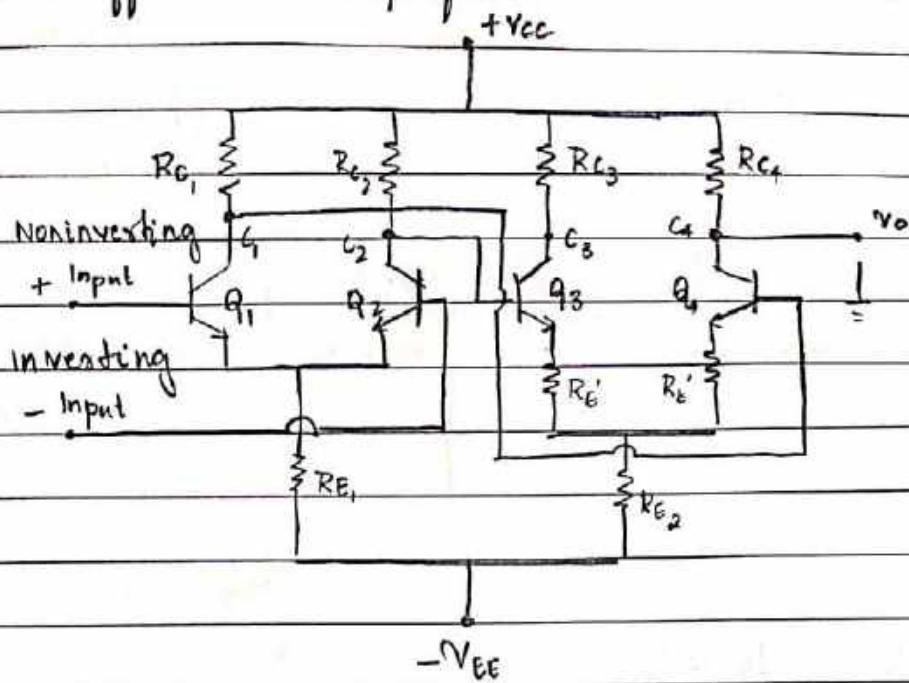
$$\Rightarrow R_2 = \frac{V_{EE} - 0.7}{I_2}$$

$$R_2 = \frac{20 - 0.7}{2m}$$

$$\underline{\underline{R_2 = 9.65k\Omega}}$$



* cascaded differential amplifier:



Output of first stage is given as the input of second stage.

R_E , and R_E' : to improve biasing

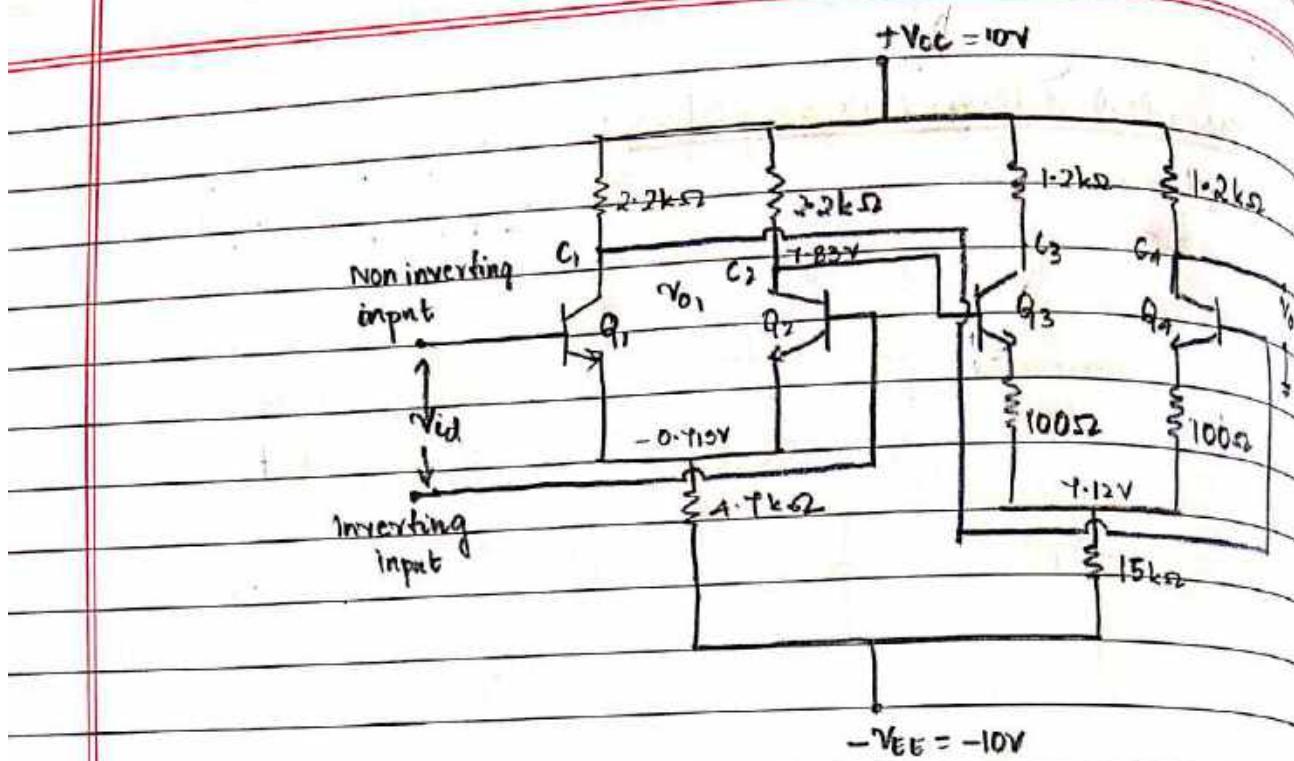
R_E' : swamping resistors to increase the input resistance and also to avoid the dependence of r_e .

Q: The circuit shown consists of multistage differential amplifier.

Determine:

- the collector current and collector to emitter voltage for each transistor
- the overall voltage gain
- the input resistance
- the output resistance.

Assume that $\beta_{dc} = 100$ and $\beta_{ac} = 100$, $V_{BE} = 0.415V$



$$\text{Sol: i. } I_C \approx I_E \quad I_E \approx I_{E2}$$

$$I_E = I_{EQ} = \frac{V_{FE} - V_{BE}}{2R_E} = \frac{10 - 0.915}{2(4.7k)} = 0.988 \text{ mA}$$

$$\underline{\underline{I_{E1} = 0.988 \text{ mA}}}$$

$$\therefore \underline{\underline{I_{C1} = I_{C2} = 0.988 \text{ mA}}}$$

$$\text{ii. } V_{CE} = V_{CE2}$$

$$V_C = V_{CC} - I_C R_C$$

$$V_C = 10 - (0.988 \text{ mA})(2.2k) = 7.83 \text{ V}$$

$$V_{CE1} = V_{C1} - V_{E1}$$

$$V_{CE1} = 7.83 - (-0.915) = 8.745 \text{ V}$$

$$\underline{\underline{V_{CE1} = 8.545 \text{ V}}}$$

$$\therefore \underline{\underline{V_{CE1} = V_{CE2} = 8.545}}$$

iii. Base to emitter loop of transistor Q_3 .

$$-V_{CC} + I_{C2} R_{C2} + V_{BE3} + R_E' I_{E3} + R_E (2 I_{E3}) - (V_{EE}) = 0$$

$$-10 + (0.988 \text{ mA})(2.2k) + 0.915 + (100) I_{E3} + 2(15k) I_{E3} + 10 = 0$$

$$-20 + 2.1436 + 0.915 + (100 + 30k) I_{E3} = 0$$

$$30100 I_{E3} = -22.088226 \quad 17.114$$

$$\underline{\underline{I_{E3} = -0.56 \text{ mA}}}$$

$$I_{E_3} = I_{E_4} = -0.09 \text{ mA}$$

$$I_{C_3} \approx I_{E_3}$$

$$V_{C_3} = V_{CC} - I_{C_3} R_3 =$$

$$I_{C_3} = I_{C_4} = 0.56 \text{ mA}$$

$$V_{C_3} = 10 - (0.56 \text{ mA})(1.2 \text{ k})$$

$$\underline{V_{C_3} = 7.328 \text{ V}}$$

$$V_{CE_3} = V_{C_3} - V_{E_3}$$

$$V_{CE_3} = V_{CE_4} = 2.908$$

$$V_{CE_3} = 7.328 - 4.12$$

$$\underline{V_{CE_3} = 2.908 \text{ V}}$$

$$\text{ii. } r_{e_1} = \frac{26 \text{ mV}}{I_{E_1}} = \frac{26 \text{ m}}{0.988 \text{ mA}} = \underline{26.316 \Omega} = r_{e_2}$$

$$r_{e_3} = \frac{26 \text{ mV}}{I_{E_2}} = \frac{26 \text{ m}}{0.56 \text{ mA}} = \underline{46.43 \Omega} = r_{e_4}$$

$$A_d = A_{d1} \times A_{d2}$$

$$A_{d1} = \frac{V_o}{V_{id}} = \frac{R_{C_2} || R_{i_2}}{r_{e_1}} =$$

$$R_{i_2} = 2\beta_{ac}(r_{e_3} + R_E') \\ R_{i_2} = 2(100)(46.43) \\ R_{i_2} = 2000.66 \Omega$$

$$A_{d1} = \frac{2.2 \text{ k} || 29.285 \text{ k}}{26.316}$$

$$\underline{R_{i_2} = 29.285 \text{ k} \Omega}$$

$$\underline{A_{d1} = 80.4}$$

$$A_{d2} = \frac{V_o}{V_{o_1}} = \frac{R_{C_4}}{2(R_E' + r_{e_4})} = \frac{1.2 \text{ k}}{2(100 + 46.43)}$$

$$\underline{A_{d2} = 4.16}$$

$$A_d = A_{d1} \times A_{d2} = 336.85$$

$$\text{iii. } R_{i_1} = 2\beta_{ac} r_{e_1} = 2(100)(26.316)$$

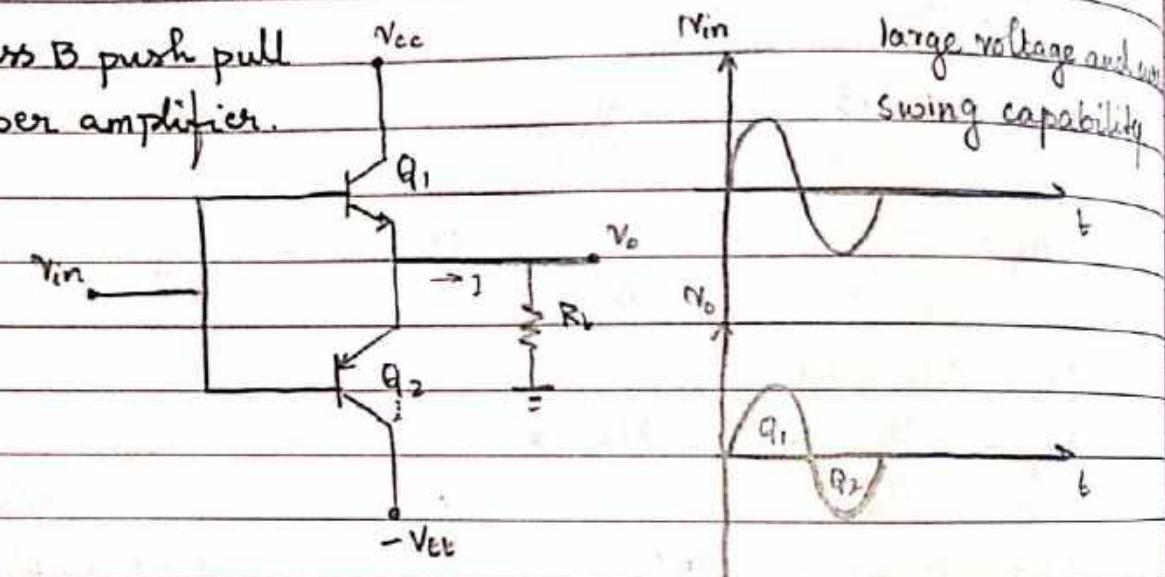
$$\underline{R_{i_1} = 5.06 \text{ k} \Omega}$$

* Complementary Symmetry Push Pull Amplifier

At output stage the following has to be achieved

- low output impedance
- large voltage swing capability
- large current swing capability
- short circuit protection.
- low power dissipation

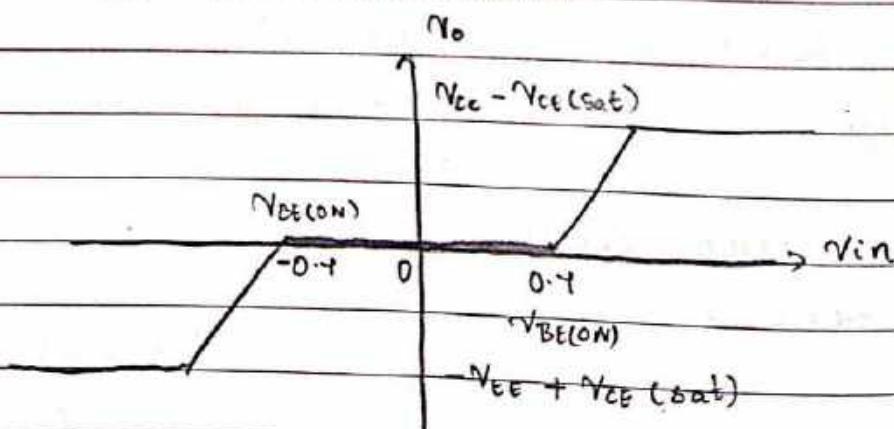
Class B push pull power amplifier.



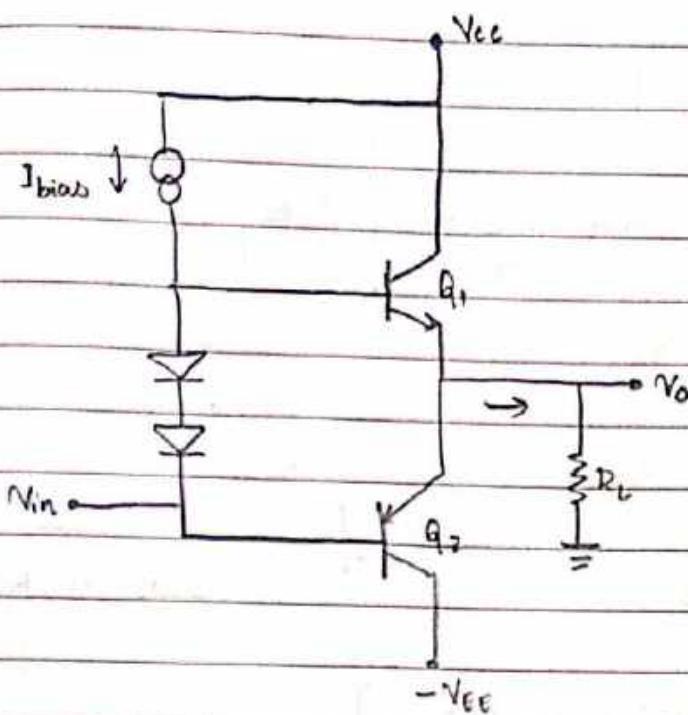
V_{in} : positive : Q_1 is on and Q_2 is off

V_{in} : negative : Q_1 is off and Q_2 is on

But since it is class B push pull power amplifier
there is cross-over distortion.

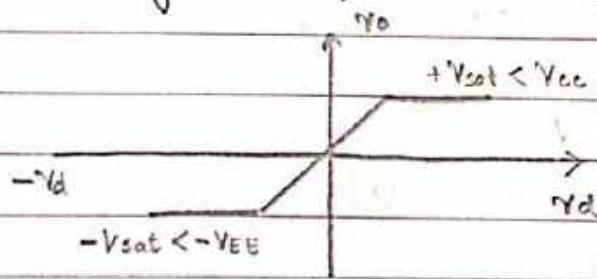


The cross over distortion can be overcome by using current bias circuit in the push pull power amplifier that reduces the power dissipation.



The two compensating diodes helps in short circuit protection. With the current bias and the diodes all the required parameters are achieved.

* Ideal Voltage Transfer characteristics:



$$V_o = A(V_i_1 - V_i_2)$$

$$V_o = A V_d$$

Let us assume ideally gain A is constant
then $V_o \propto V_d$

* Practical transfer characteristics of differential characteristics: It is a graphical representation of I_c with respect to V_d .

$$V_d = V_{B1} - V_{B2}$$

Ebers Moll Equation

$$I_c = I_s e^{(V_{BE}/V_T)}$$

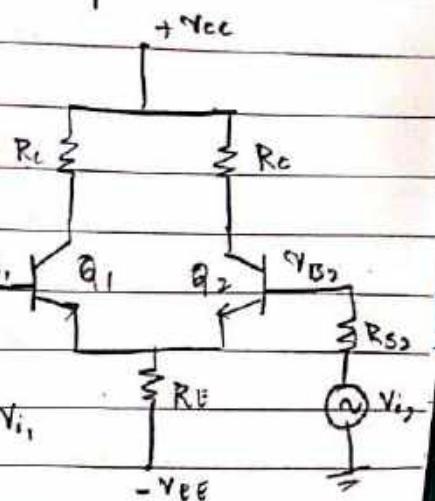
I_s - reverse saturation current

$$\text{For } Q_1 \Rightarrow I_{c1} = I_s e^{(V_{BE1}/V_T)} \quad \text{--- (1)}$$

$$\text{For } Q_2 \Rightarrow I_{c2} = I_s e^{(V_{BE2}/V_T)} \quad \text{--- (2)}$$

From eq, (1)

$$V_{BE1} = V_T \log \left[\frac{I_{c1}}{I_{s1}} \right]$$



similarly from eq. ②

$$V_{BE2} = V_T \log \left[\frac{I_{C2}}{I_{S2}} \right]$$

$$\therefore V_{BE1} - V_{BE2} = V_T \left[\log \frac{I_{C1}}{I_{S1}} - \log \frac{I_{C2}}{I_{S2}} \right]$$

Neglect R_E , R_{S1} and R_{S2}

Applying KVL

$$V_{i1} - V_{BE1} + V_{BE2} - V_{i2} = 0$$

$$V_{i1} - V_{i2} = V_{BE1} - V_{BE2}$$

$$\therefore V_d = V_{BE1} - V_{BE2}$$

$$\therefore V_d = V_T \left[\log_e \left(\frac{I_{C1}}{I_{S1}} \right) - \log_e \left(\frac{I_{C2}}{I_{S2}} \right) \right]$$

$$V_d = V_T \left[\log_e \left(\frac{I_{C1}}{I_{S1}} \cdot \frac{I_{S2}}{I_{C2}} \right) \right]$$

$$V_d = V_T \log_e \left(\frac{I_{C1}}{I_{C2}} \right)$$

$\frac{I_{C1}}{I_{C2}} = e^{\frac{(V_d/V_T)}{}}$	— ①
--	-----

$$I_E = I_{E1} + I_{E2}$$

$$\text{but } \alpha = \frac{I_{C1}}{I_{E1}} \Rightarrow I_{E1} = \frac{I_{C1}}{\alpha} \text{ and } I_{E2} = \frac{I_{C2}}{\alpha}$$

$$\therefore I_E = \frac{1}{\alpha} \left[I_{C1} + I_{C2} \right]$$

$$\alpha I_E = I_{C1} + I_{C2} — ②$$

$$\alpha I_E = I_{C2} \left[\frac{I_{C1}}{I_{C2}} + 1 \right]$$

$$\alpha I_E = I_{C2} \left[e^{\frac{V_d}{V_T}} + 1 \right]$$

$\therefore I_{C2} = \frac{\alpha I_E}{1 + e^{\frac{V_d}{V_T}}}$
--

considering eq. ①

$$I_{C_1} = e^{\frac{V_d}{V_T}} I_{C_2}$$

$$I_{C_1} e^{-\frac{V_d}{V_T}} = I_{C_2} \quad \text{--- } ③$$

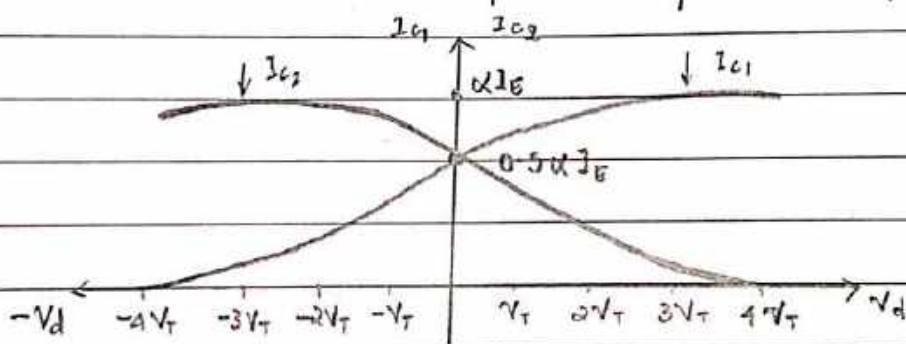
substituting eq. ③ in eq. ②

$$\alpha I_E = I_{C_1} + I_{C_1} e^{-\frac{V_d}{V_T}}$$

$$\alpha I_E = I_{C_1} [1 + e^{-\frac{V_d}{V_T}}]$$

$$I_{C_1} = \frac{\alpha I_E}{1 + e^{-\frac{V_d}{V_T}}}$$

The currents I_{C_1} and I_{C_2} vary linearly but in opposite direction.



Transfer
Characteristics.

$$V_d < -100 \text{ mV}$$

$$V_d > 100 \text{ mV at room temp}$$

$$V_d < -V_T \quad I_{C_1} = 0 \quad I_{C_2} = \alpha I_E$$

$$V_d > V_T \quad I_{C_1} = \alpha I_E \quad I_{C_2} = 0$$

Q_1 is off Q_2 is on

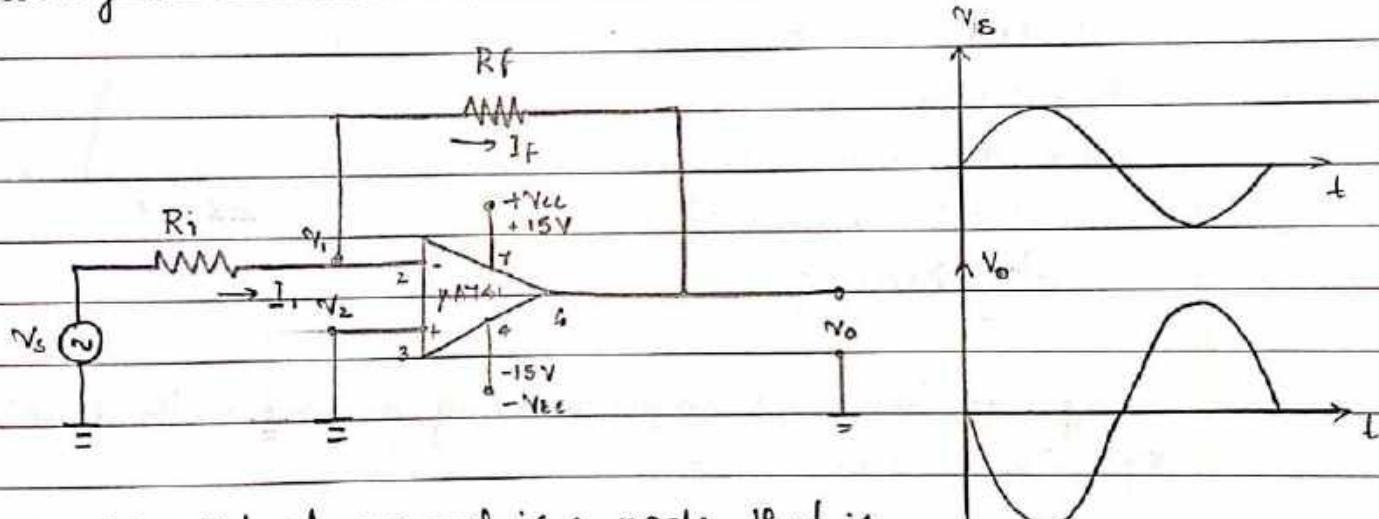
Q_1 is on Q_2 is off

Unit - 2

LINEAR APPLICATIONS OF AN OPAMP

* Inverting Amplifier:

Inverting amplifier is an amplifier whose amplified output is negatively proportional to the input. Its gain is also negative. That is because the amplified output will be 180° out of phase with input. Hence when the input voltage increases the output voltage will decrease and vice versa.



NOTE: A virtual ground is a node that is maintained at a steady reference potential without actually being connected directly to the reference potential. In some cases the reference potential is ground, hence the reference node is called ~~virtual~~ ground.

In the circuit

Due to virtual ground $V_1 = V_2 = 0$

Applying KCL to node V_1 ,

$$I_1 = I_F$$

$$V_s - V_1^0 = \frac{V_1^0 - V_o}{R_f}$$

$$R_i \quad R_f$$

$$\frac{V_o}{R_i} = -\frac{V_o}{R_f} \Rightarrow A_F = \frac{V_o}{V_s} = -\frac{R_f}{R_i}$$

$$\therefore V_o = -\frac{R_f}{R_i} V_s$$

Q1: A 200mV(p-p) sine wave form voltage is applied to an inverting amplifier. Given $R_F/R_1 = 10$. Sketch the output.

Sol: For an inverting amplifier

$$V_o = -\frac{R_F}{R_1} V_i$$

$$V_o = -10V_i \quad \text{--- (1)}$$

but given $2V_m = 200 \text{ mV}$
 $\Rightarrow V_m = 100 \text{ mV}$

$$V_i = V_m \sin \omega t$$

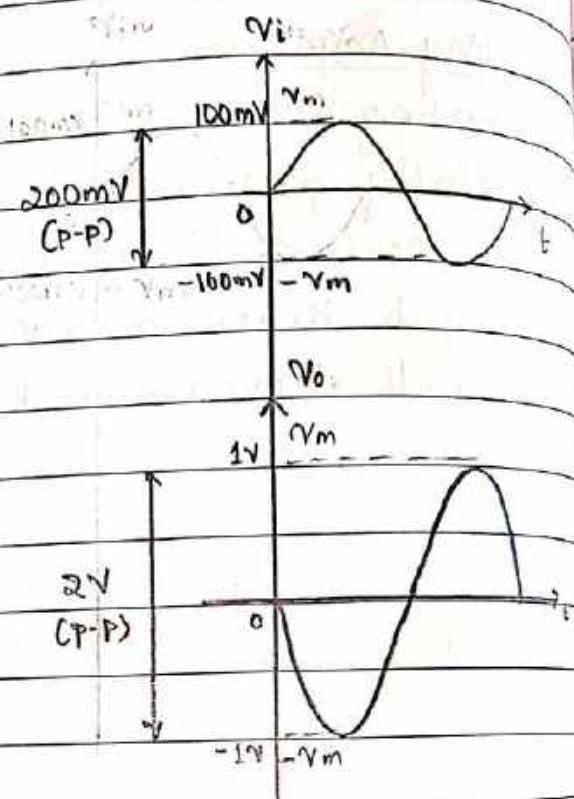
$$V_i = (100 \text{ m}) \sin \omega t$$

$$V_i = 0.1 \sin \omega t$$

Substituting in eq (1)

$$V_o = -10(0.1 \sin \omega t)$$

$$\underline{V_o = -1 \sin \omega t}$$



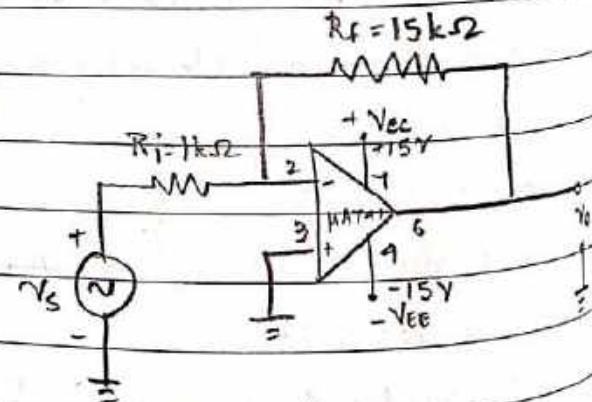
Q2: Design an inverting amplifier using op amp with a closed loop voltage gain of -15.

Sol: For inverting amplifier

$$\text{Gain} : A_g = -\frac{R_F}{R_1} = -15$$

$$\Rightarrow R_F = 15R_1$$

$$\text{If } R_1 = 1k\Omega \text{ then } R_F = 15k\Omega$$



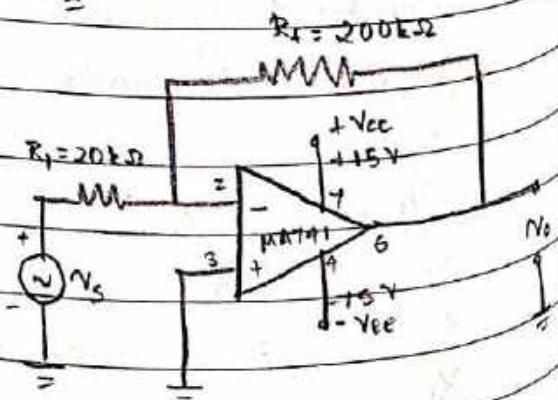
Q3: For the circuit shown

calculate the output voltage for the following input voltage.

i. $V_i = 0.2 \text{ V}$

ii. $V_i = 0.5 \sin 314t$

iii. $V_i = -0.4 \text{ V}$



Page _____

Sol: For an inverting amplifier

$$V_o = -\frac{R_F}{R_I} V_i$$

i. $V_i = 0.2V$

$$\therefore V_o = -\frac{200k}{20k} (0.2) \Rightarrow \underline{\underline{V_o = -2V}}$$

ii. $V_i = 0.5 \sin 314t$

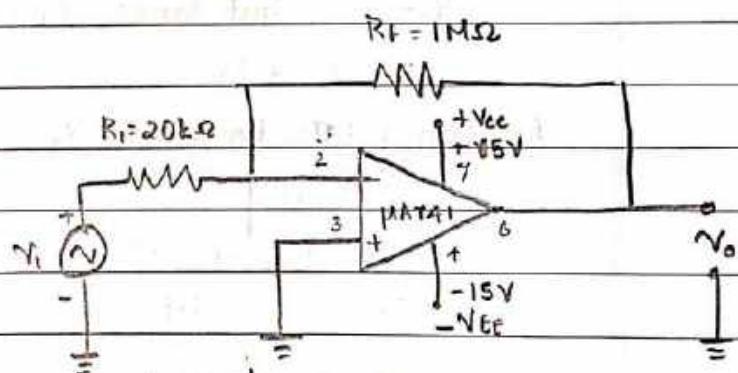
$$\therefore V_o = -\frac{200k}{20k} (0.5 \sin 314t)$$

$$\underline{\underline{V_o = -5 \sin 314t}}$$

iii. $V_i = -0.4V$

$$\therefore V_o = -\frac{200k}{20k} (-0.4) \Rightarrow \underline{\underline{V_o = 4V}}$$

Q4: For the circuit shown calculate the closed loop voltage gain, required input voltage to get an output voltage of 2V.



Sol: For inverting amplifier

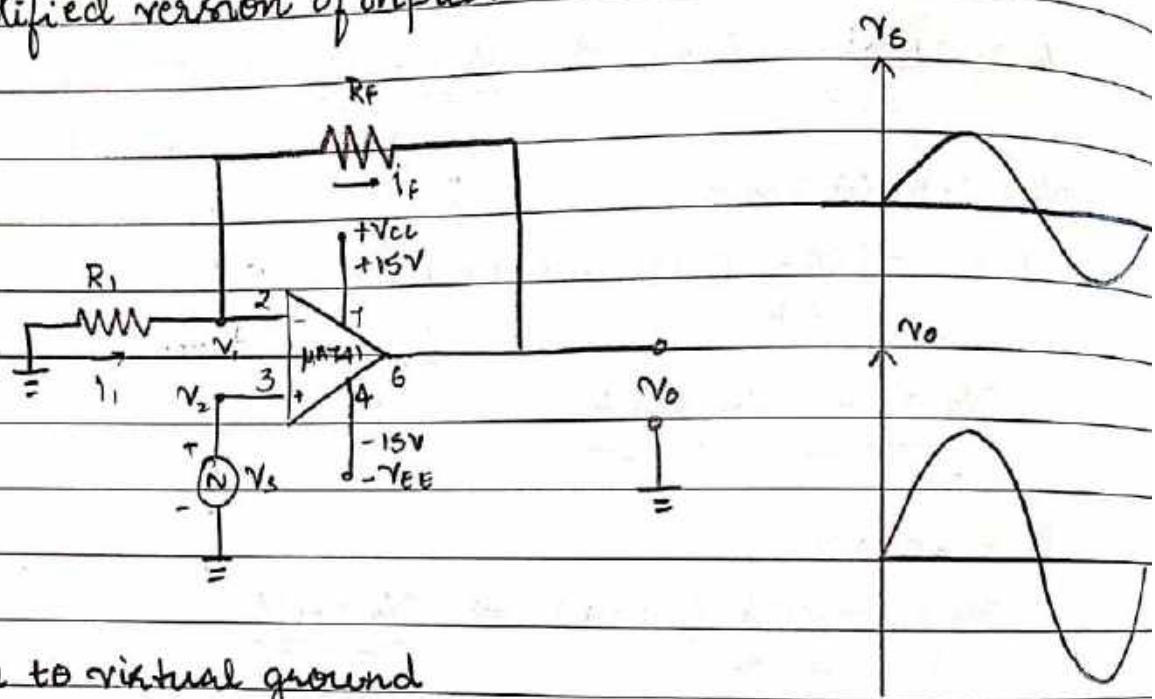
$$A = -\frac{R_F}{R_I} = -\frac{1 \times 10^6}{20 \times 10^3} = -50$$

Input voltage to get output voltage of 2V

$$V_i = \frac{V_o}{A} \approx \frac{2}{-50} = \underline{\underline{-0.04V}}$$

* Non-inverting Amplifier:

Non inverting amplifier is one in which the output is in phase with respect to the input. The output is a non-inverted amplified version of input.



Due to virtual ground

$$V_1 = V_2 \quad \text{but since } V_2 = V_s$$

$$\therefore V_1 = V_2 = V_s$$

Applying KCL to node V_1 ,

$$i_1 = i_f$$

$$\frac{0 - V_1}{R_1} = \frac{V_1 - V_o}{R_f}$$

$$\frac{-V_s}{R_1} = \frac{V_s - V_o}{R_f}$$

$$\frac{V_o}{R_f} = \frac{V_s}{R_1} \left[\frac{1}{R_f} + \frac{1}{R_1} \right]$$

$$\frac{V_o}{V_s} = R_f \left[\frac{1}{R_f} + \frac{1}{R_1} \right]$$

$$\therefore A = \frac{V_o}{V_s} = \left[1 + \frac{R_f}{R_1} \right]$$

$$\Rightarrow V_o = \left[1 + \frac{R_f}{R_1} \right] V_s$$

Q1: Design a non inverting amplifier using op-amp with a closed loop gain as 10.

Sol: For non inverting amplifier

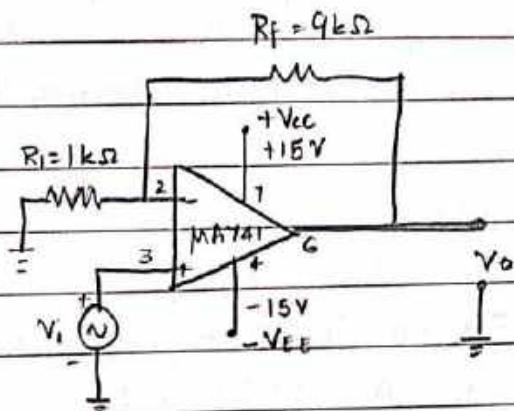
$$A = 1 + \frac{R_f}{R_1}$$

$$10 = 1 + \frac{R_f}{R_1}$$

$$\therefore \frac{R_f}{R_1} = 9$$

$$\Rightarrow \underline{\underline{R_f = 9R_1}}$$

If $R_1 = 1k\Omega$ then $R_f = 9k\Omega$



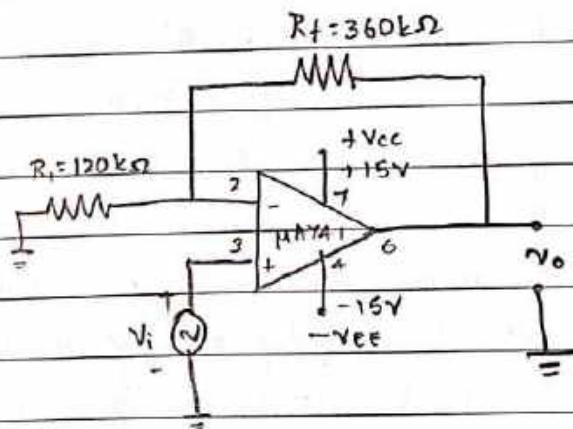
Q2: For the circuit shown,

calculate the output voltage
for the following input voltage

$$\text{i. } V_i = 0.5V$$

$$\text{ii. } V_i = 0.6 \cos 314t V$$

$$\text{iii. } V_i = -0.3V$$



Sol: For non inverting Amplifier

$$A = 1 + \frac{R_f}{R_1} = 1 + \frac{360k}{120k} = 1+3 = 4$$

$$\text{i. } V_i = 0.5V$$

$$V_o = AV_i$$

$$V_o = (4)(0.5) = 2V //$$

$$\text{iii. } V_i = -0.3V$$

$$\therefore V_o = AV_i$$

$$V_o = (4)(-0.3)$$

$$V_o = \underline{\underline{-1.2V}}$$

$$\text{ii. } V_i = 0.6 \cos 314t V$$

$$\therefore V_o = AV_i$$

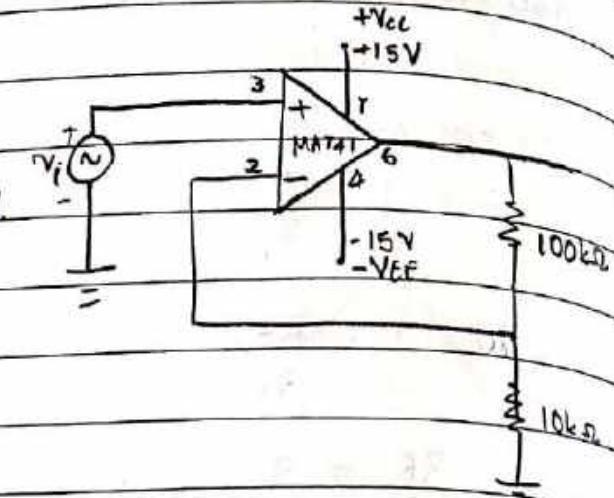
$$V_o = (4)0.6 \cos 314t$$

$$V_o = \underline{\underline{2.4 \cos 314t}}$$

Q3: For the circuit shown

calculate:

- closed loop voltage gain
- required input voltage to get an output voltage of 4V.



Sol: Given: $R_f = 100\text{k}\Omega$

$$R_i = 10\text{k}\Omega$$

For non inverting amplifier

$$\text{i. } A = 1 + \frac{R_f}{R_i} = 1 + \frac{100\text{k}}{10\text{k}}$$

$$\underline{\underline{A = 11}}$$

$$\text{ii. } V_o = A V_i$$

~~non-inverting~~

$$\Rightarrow V_i = V_o / A = 4 / 11$$

$$\underline{\underline{V_i = 0.364\text{V}}}$$

Q4: In an op-amp inverting amplifier $R_i = 1\text{k}\Omega$, $R_f = 100\text{k}\Omega$, the DC supply voltage to the op-amp is $\pm 15\text{V}$. calculate the output voltage if the input voltage is 1V.

Sol: Given: $R_i = 1\text{k}\Omega$ $+ V_{cc} = 15\text{V}$

$$R_f = 100\text{k}\Omega \quad - V_{ee} = -15\text{V}$$

For noninverting amplifier

$$V_o = A V_i$$

$$V_o = \left[1 + \frac{R_f}{R_i} \right] V_i$$

$$V_o = \left[1 + \frac{100\text{k}}{1\text{k}} \right] V_i$$

For inverting amplifier

$$V_o = A V_i$$

$$V_o = - \frac{R_f}{R_i} V_i$$

$$V_o = - \frac{100\text{k}}{1\text{k}} (1)$$

Output voltage does not exceed -13.5V due to saturable property.

$$V_o = \underline{-100\text{V}}$$

Q5: In an op-amp non inverting amplifier $R_1 = 2k\Omega$, $R_f = 200k\Omega$. The dc supply voltage to the op-amp is $\pm 12V$. calculate the output voltage if the input voltage is $1.5V$.

Sol: Given : $R_f = 200k\Omega$ $+V_{CC} = 12V$

$R_1 = 2k\Omega$ $-V_{EE} = -12V$

For non inverting amplifier

$$V_o = A V_i$$

$$V_o = \left[1 + \frac{R_f}{R_1} \right] V_i$$

$$V_o = \left[1 + \frac{200k}{2k} \right] (1.5)$$

$$\underline{V_o = 151.5V}$$

output voltage does not exceed

$10.5V$ due to saturable property.

Q6: Design an op-amp inverting amplifier with a gain of -50 and input resistance of $2k\Omega$.

Sol: For inverting amplifier

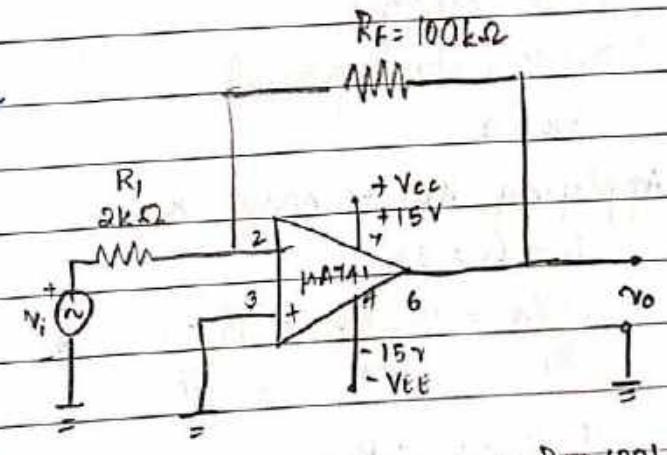
$$A = -R_f = -50$$

$$R_1$$

$$\Rightarrow R_f = 50 R_1$$

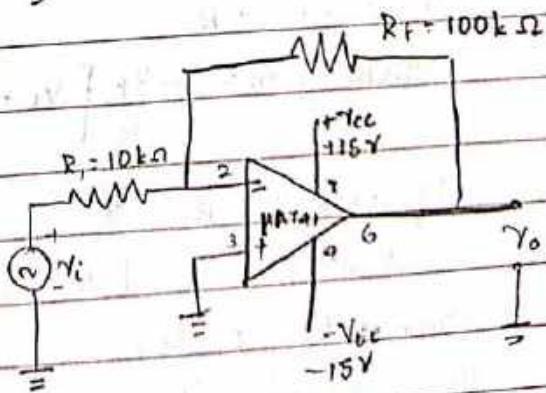
$$R_f = 50(2k)$$

$$\underline{R_f = 100k\Omega}$$



Q7: For the circuit shown, find
i. the closed loop voltage gain A_f .

ii. input resistance R_i if current
flowing through R_1 if $V_i = 0.5V$



sol:

Inverting Amplifier

$$\text{i. } A_f = \frac{-R_f}{R_1} = \frac{-100k}{10k}$$

$$\underline{A_f = -10}$$

$$\text{ii. } R_{if} = R_1 = 10k\Omega //$$

$$\text{iii. } V_i = 0.5$$

$$i_1 = \frac{V_i}{R_1} = \frac{0.5}{10k} \Rightarrow i_1 = 0.05mA$$

* Summing Amplifier:

The summing amplifier is an op-amp circuit that combines two or more input voltages into a single output voltage.

- Inverting Adder

The adder will produce the negative sum of any number of input voltages.

Due to virtual ground

$$V_{x2} = 0.$$

Applying KCL to node V_x

$$I_1 + I_2 = I_f$$

$$\frac{V_1 - V_x^o}{R_1} + \frac{V_2 - V_x^o}{R_2} = \frac{V_x^o - V_o}{R_f} \Rightarrow \frac{V_1}{R_1} + \frac{V_2}{R_2} = -\frac{V_o}{R_f}$$

$$\text{If } R_1 = R_2 = R$$

then

$$V_o = -\frac{R_f}{R} [V_1 + V_2] \quad \text{With gain}$$

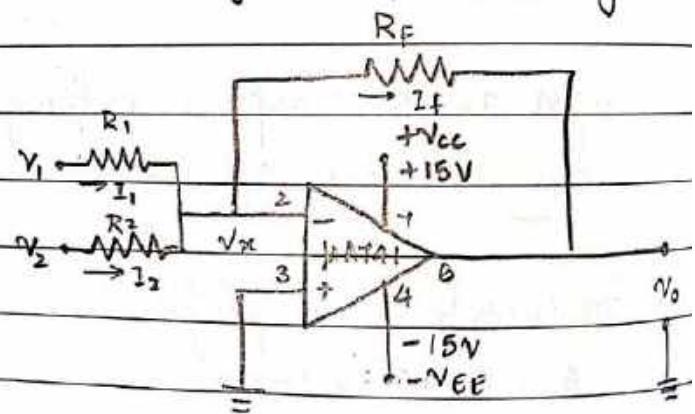
$$\text{If } R_f = R_1 = R_2 = R$$

then

$$V_o = -[V_1 + V_2] \quad \text{Without gain}$$

- Noninverting Adder

The adder will produce the positive sum of any number of input voltages on giving inputs to the noninverting terminal



For non-inverting amplifier

$$V_o = \left[1 + \frac{R_f}{R_{11}} \right] V_x$$

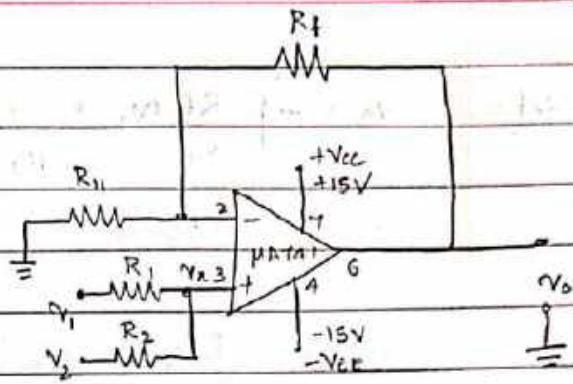
Using superposition at V_x

$$\text{When } V_2 = 0 \Rightarrow V_{x1} = \frac{V_1 R_2}{R_1 + R_2}$$

$$\text{When } V_1 = 0 \Rightarrow V_{x2} = \frac{V_2 R_1}{R_1 + R_2}$$

$$\therefore V_x = V_{x1} + V_{x2} = \frac{V_1 R_2 + V_2 R_1}{R_1 + R_2}$$

$$\therefore V_o = \left[1 + \frac{R_f}{R_{11}} \right] \left[\frac{V_1 R_2 + V_2 R_1}{R_1 + R_2} \right]$$



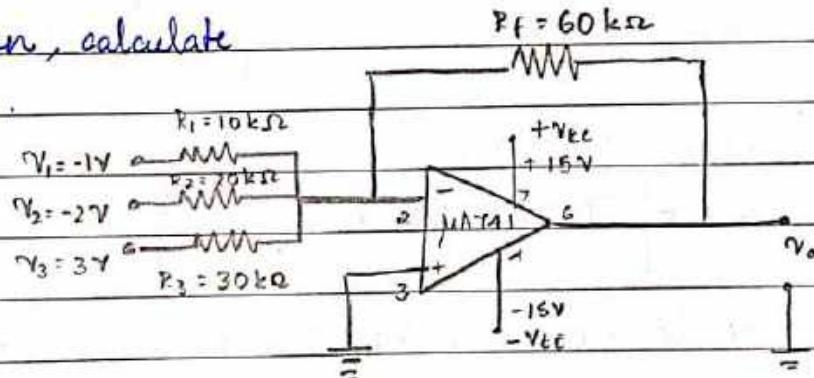
If $R_1 = R_2 = R$ (with gain)

$$V_o = \left[1 + \frac{R_f}{R_{11}} \right] \left[\frac{V_1 + V_2}{2} \right]$$

If $R_{11} = R_f = R$

$$V_o = [V_1 + V_2] \text{ without gain}$$

Q1: For the circuit given, calculate the output voltage.



Sol: Inverting summer

$$V_o = - \left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]$$

$$V_o = - \left[\frac{60k}{10k} (-1) + \frac{60k}{20k} (-2) + \frac{60k}{30k} (3) \right]$$

$$V_o = - [-6 - 6 + 6]$$

$$\underline{\underline{V_o = 6V}}$$

Q2: calculate the output voltage of 3 input summing amplifier given that $R_1 = 200k\Omega$, $R_2 = 250k\Omega$, $R_3 = 500k\Omega$, $R_f = 1M\Omega$.
 $V_1 = -2V$, $V_2 = 2V$, $V_3 = 1V$.

$$\underline{\text{Sol:}} \quad V_o = - \left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]$$

$$V_o = - \left[\frac{1500k}{200k} (-2) + \frac{1M}{250k} (2) + \frac{1M}{500k} (1) \right]$$

$$V_o = - [-10 + 8 + 2]$$

$$\underline{\underline{V_o = 0V}}$$

~~Temp~~

~~Q3:~~ Design an adder circuit using op-amp. to obtain the output voltage given by ~~as~~

$$V_o = - [0.5 V_1 + 0.8 V_2 + 2 V_3]$$

where V_1, V_2, V_3 are inputs.

Sol: Adder (Inverting)

$$V_o = - \left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]$$

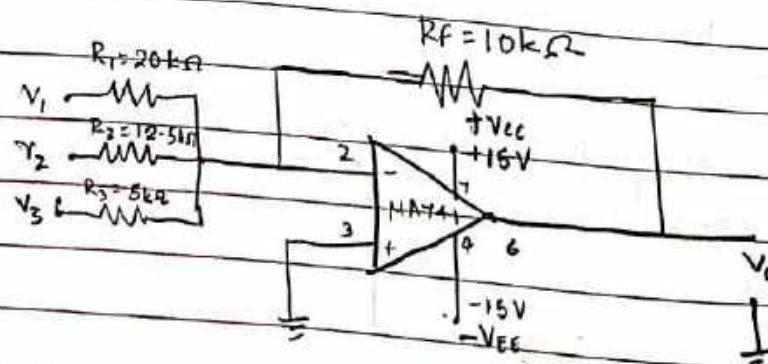
$$\Rightarrow \frac{R_f}{R_1} = 0.5 \quad \therefore R_f = 0.5 R_1 \quad \therefore R_1 = 2 R_f$$

$$\therefore \frac{R_f}{R_2} = 0.8 \quad \therefore R_f = 0.8 R_2 \quad \therefore R_2 = 1.25 R_f$$

$$\therefore \frac{R_f}{R_3} = 2 \quad \therefore R_f = 2 R_3 \quad \therefore R_3 = 0.5 R_f$$

Assuming $R_f = 10k\Omega$

then $R_1 = 20k\Omega, R_2 = 12.5k\Omega, R_3 = 5k\Omega$



Q4: Design an adder circuit using op amp to obtain an output voltage given by $V_o = 2[0.1V_1 + 0.5V_2 + 2.0V_3]$

Sol: For inverting adder

$$V_o = - \left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]$$

$$\Rightarrow -R_f = 2(0.1) \Rightarrow R_1 = 5R_f$$

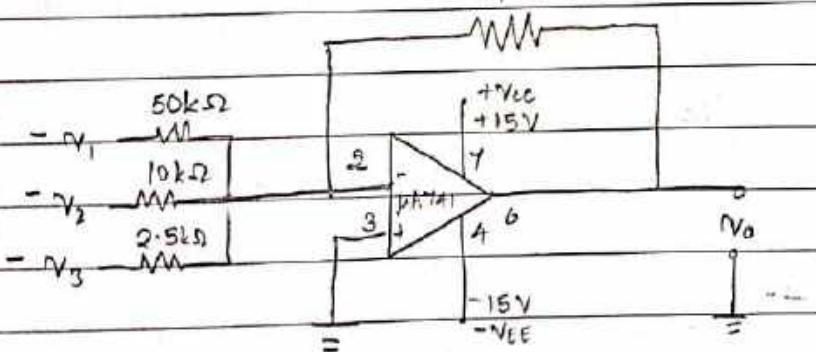
$$\Rightarrow -\frac{R_f}{R_2} = 2(0.5) \Rightarrow R_2 = -R_f$$

$$\Rightarrow -\frac{R_f}{R_3} = 2(2.0) \Rightarrow R_3 = 0.25R_f$$

Let us assume $R_f = 10k\Omega$

then $R_1 = 50k\Omega$, $R_2 = 10k\Omega$ and $R_3 = 2.5k\Omega$

$$R_f = 10k\Omega$$



Q5: Design an opamp circuit so that the output

$$V_o = V_1 + V_2 - 3V_3$$

Sol: Given: $V_o = V_1 + V_2 - 3V_3$

$$V_o = -[V_1 - V_2 + 3V_3]$$

For inverting adder

$$V_o = - \left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]$$

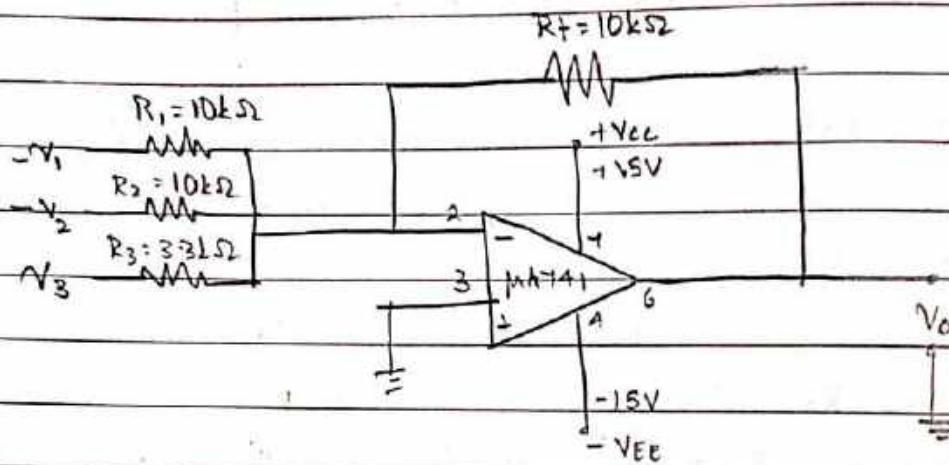
$$\Rightarrow \frac{R_f}{R_1} = -1 \therefore R_1 = R_f$$

$$\Rightarrow \frac{R_f}{R_2} = -1 \quad \therefore R_2 = R_f$$

$$\Rightarrow \frac{R_f}{R_3} = 3 \quad \therefore R_3 = 0.33 R_f$$

Let us assume $R_f = 10k\Omega$

then $R_1 = 10k\Omega$, $R_2 = 10k\Omega$ and $R_3 = 3.3k\Omega$



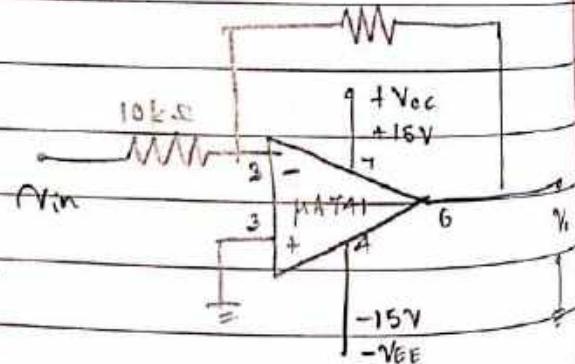
Q6: Determine the voltage gain of the op-amp circuit

$A = 1.7k\Omega$

sol: For inverting amplifier

$$A = -\frac{R_f}{R_1}$$

$$A = -\frac{10k\Omega}{10k} = -0.4$$



Q7: A sine wave of 0.5 peak-to-peak voltage is applied to inverting input using $R_1 = 10k\Omega$ and $R_f = 50k\Omega$. It uses the supply voltages. Determine the output and sketch the waveform. If now the amplitude of input sine wave is increased to 5V what will be the output? Is it practically possible? Sketch the waveform.

sol: $R_1 = 10k\Omega$ (given) $V_m = 0.5V$
 $R_f = 50k\Omega$

Q7: For inverting amplifier

$$\text{Gain } A = \frac{-R_f}{R_1} = \frac{-50k}{10k} = -5$$

$$V_o = -AV_i$$

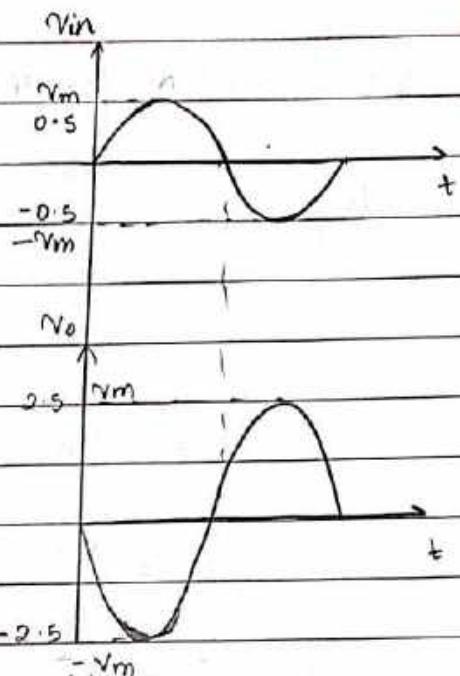
$$\therefore V_o = AV_m$$

$$V_o = (-5)0.5 \Rightarrow V_o = -2.5V$$

$$\text{Now } V_{in} = 5V$$

$$\Rightarrow V_o = AV_{in} = (-5)(5)$$

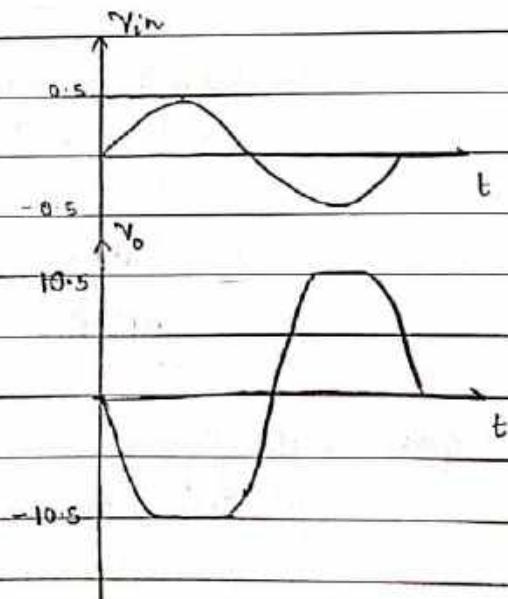
$$\underline{\underline{V_o = -25V}}$$



But the supply voltage is $\pm 12V$.

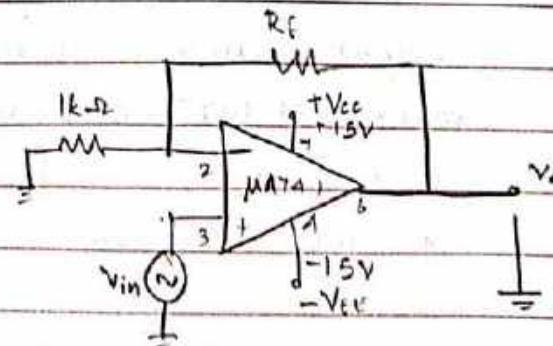
Hence the output is saturated to $10.5V$.

Practically we get a clipped off output to $10.5V$ due to the saturable property of the op-amp.



Q8: For the op-amp shown, the

gain required is 61. Determine the appropriate value of feedback resistance.

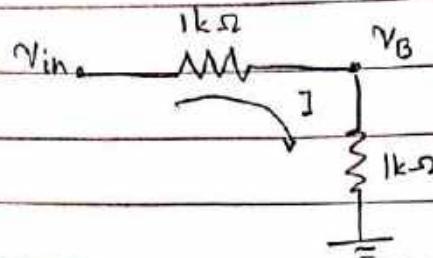


Sol: For inverting amplifier

$$A = \frac{R_f}{R_1} + 1 \Rightarrow 61 = \frac{R_f}{1k} + 1 \quad \therefore \underline{\underline{R_f = 60k\Omega}}$$

Q9: Find V_B for the circuit shown

Sol:



$$I = \frac{V_{in}}{1k + 1k}$$

$$I = \frac{V_{in}}{2k\Omega}$$

$$V_B = \frac{V_{in} \times 1 \times 10^3}{2 \times 10^3} = \frac{10}{2}$$

$$\therefore \underline{\underline{V_B = 5V}}$$

For non-inverting amplifier

$$V_o = \left[\frac{R_f + 1}{R_i} \right] V_B$$

$$V_o = \left[\frac{50k}{10k} + 1 \right] 5 = \underline{\underline{V_o = 30V}}$$

Q10: In the figure, an inverting

amplifier with $R_i = 20k\Omega$

and $R_f = 100k\Omega$, A load

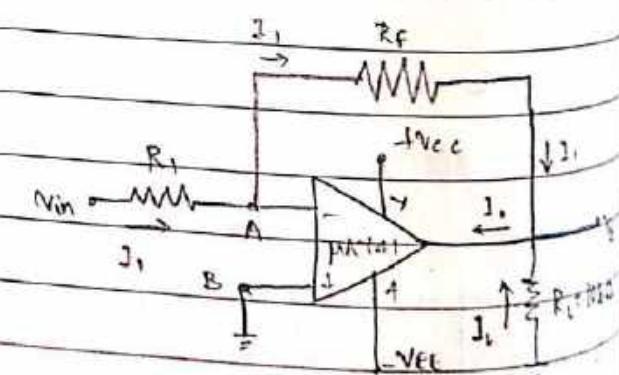
of $10k\Omega$ is connected to the

output with an input

voltage of $0.4V$. calculate

i. I_1 ii. V_o iii. I_L

iv. Total current I_o



Sol: i. $I_1 = \frac{V_{in} - V_A}{R_i}$ but due to virtual ground $V_A = 0$

$$I_1 = \frac{0.4}{20k} = 35\mu A$$

$$\text{ii. } V_o = \frac{-R_f}{R_1} V_{in}$$

$$V_o = \frac{-100k}{20k} (0.4) \therefore V_o = -3.5V$$

$$\text{iii. } I_L = \frac{0 - V_o}{10k} = \frac{-(-3.5)}{10k}$$

$$I_L = 0.35mA$$

iv. Total current

$$I_o = I_i + I_L = 35\mu A + 0.35mA$$

$$I_o = 0.385mA$$

Q11: For the figure of non inverting amplifier, find:

i. I_i, ii. V_o, iii. I_L

iv. ~~for feedback~~ Gain

$$\text{Sol: i. } I_i = \frac{V_A - 0}{R_1}$$

By virtual ground V_A = V_{in} = 0.8V

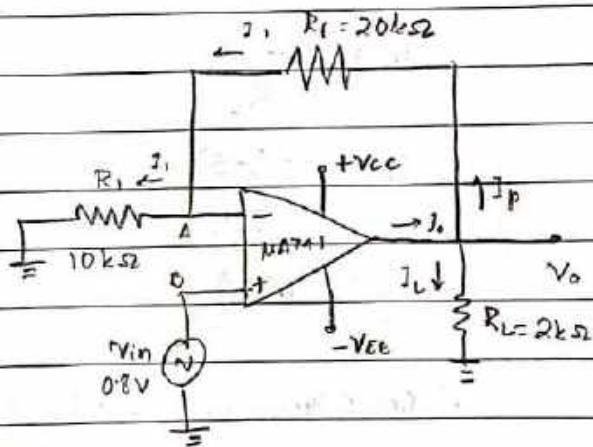
$$\therefore I_i = \frac{0.8}{10k} \approx 80\mu A$$

$$\text{ii. } V_o = \left[\frac{R_f + 1}{R_1} \right] V_{in} = \left[\frac{20k + 1}{10k} \right] 0.8$$

$$\underline{\underline{V_o = 2.4}}$$

$$\text{iii. } I_L = \frac{V_o - 0}{R_L} = \frac{2.4}{2k} = \underline{\underline{1.2mA}}$$

$$\text{iv. Gain} = \frac{R_f + 1}{R_1} = \frac{20k + 1}{10k} = 3$$



Q12: If a load resistance of $50k\Omega$ is connected to the output terminal of inverting amplifier of 3:1. Find the load current, output voltage and input current if $V_i = 0.5V$.

Sol: Input current

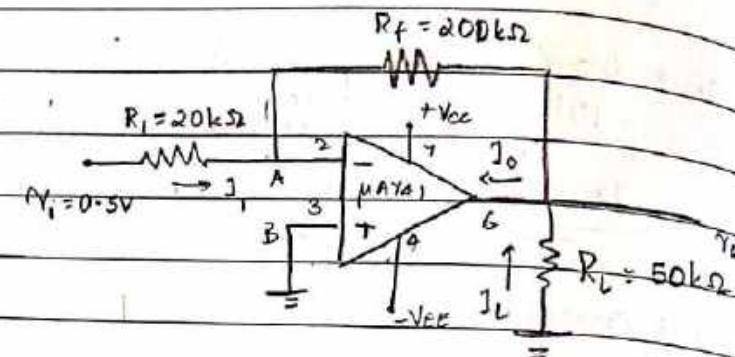
$$I_i = V_i - V_A$$

$$R_i$$

$$I_i = \frac{0.5 - 0}{20k} = 0.5 - 0$$

$$20k$$

$$\underline{I_i = 0.025mA}$$



Load current

$$I_L = \frac{0 - V_o}{R_L}$$

$$I_L = \frac{-(-5)}{50k} = 0.1mA$$

$$\underline{I_L = 0.1mA}$$

$$I_{FE} = I_i = I_F$$

$$0.025mA = \frac{V_A - V_o}{R_F}$$

$$0.025mA = \frac{-V_o}{200k}$$

$$\underline{V_o = -5V}$$

~~$$I_o = I_L + I_i = 0.1mA + 0.025mA$$~~

~~$$\underline{I_o = 0.125mA}$$~~

Q13: Find V_o in the circuit shown,

$$\begin{cases} R_f = 10k\Omega \text{ and } R_1 = 2k\Omega \text{ and} \\ R_2 = 5k\Omega \end{cases}$$

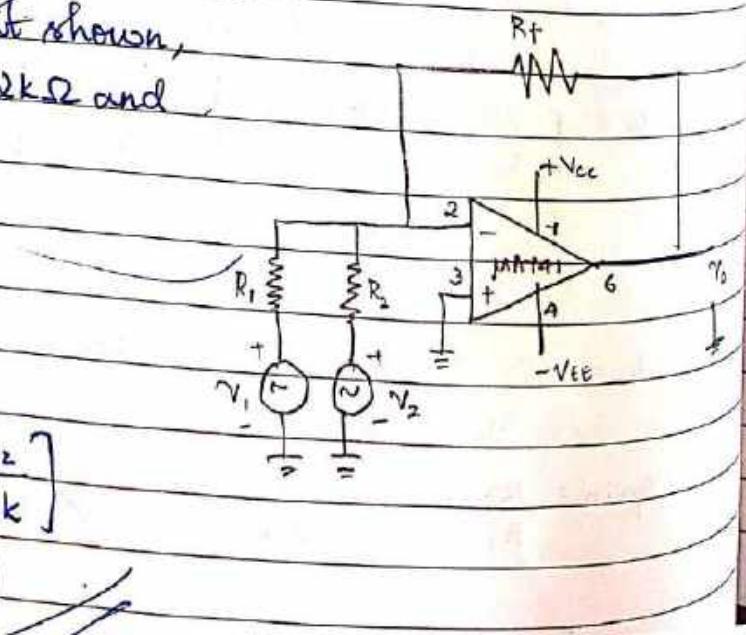
Sol:

Inverting amplifier

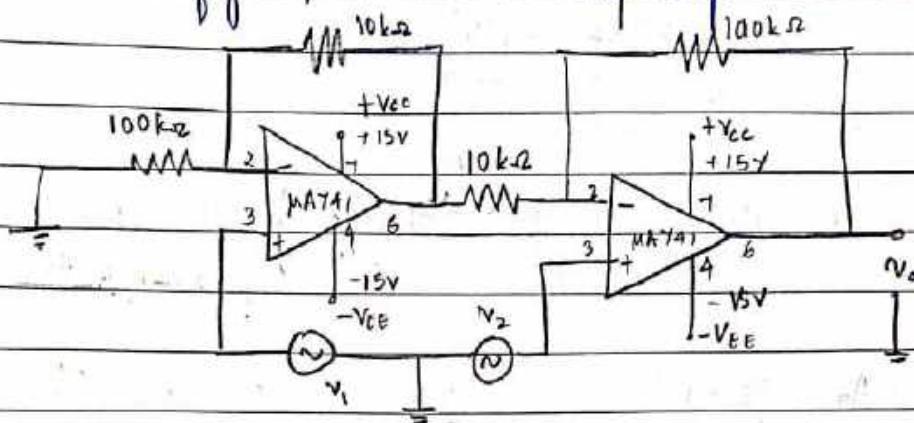
$$V_o = -R_f \left[\frac{V_1 + V_2}{R_1 + R_2} \right]$$

$$V_o = -10k \left[\frac{V_1 + V_2}{2k + 5k} \right]$$

$$V_o = -[5V_1 + 2V_2]$$



Q19. Find output voltage V_o in terms of V_1 and V_2 for the op-amp circuit shown in the figure, assume ideal op-amp.



Sol: — First Stage:

$$V_{o1} = \left[\frac{R_f + 1}{R_1} \right] V_1$$

$$V_{o1} = \left[\frac{10k + 1}{100k} \right] V_1$$

$$\underline{\underline{V_{o1} = 1.1 V_1}}$$

— Second Stage

We use superposition

CASE 1: Assume V_o is active and $V_2 = 0$

then the circuit acts as inverting amplifier

$$V'_o = \frac{-R_f}{R_1} V_{o1}$$

$$V'_o = \frac{-100k}{10k} V_{o1}$$

$$\therefore \underline{\underline{V'_o = -10 V_{o1} = -11 V_1}}$$

CASE 2: Assume V_2 is active and V_{o1} is zero

then the circuit acts as non-inverting amplifier.

$$V''_o = \left[\frac{R_f + 1}{R_1} \right] V_2$$

$$V''_o = \left[\frac{100k + 1}{10k} \right] V_2 = \underline{\underline{11 V_2}}$$

Therefore output voltage is

$$V_o = V_o' + V_o''$$

$$V_o = -11V_1 + 11V_2$$

$$\therefore \underline{V_o = 11[V_2 - V_1]}$$

Q15:

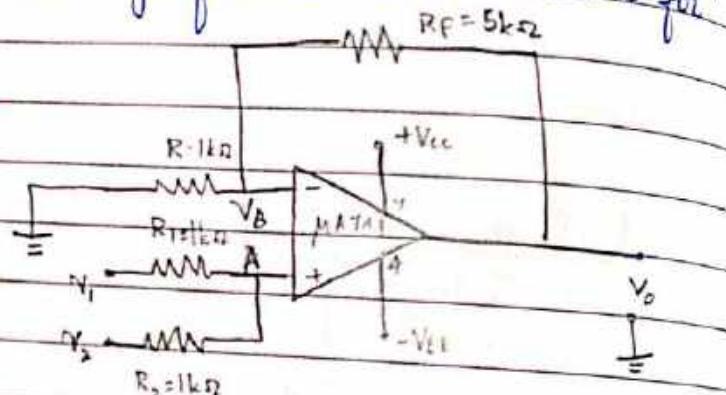
Determine the output voltage for the circuit shown for
 $V_1 = 1V$ and $V_2 = 3V$

Sol:

$$A_{in} = \left[\frac{R_F + 1}{R} \right]$$

$$A = \left[\frac{5k + 1}{1k} \right]$$

$$\underline{\underline{A = 6}}$$



$$V_{A1} = \frac{V_1 R_2}{R_1 + R_2} = \frac{(1)(1k)}{2k} = \underline{\underline{0.5V}}$$

$$V_{A2} = \frac{V_2 R_1}{R_1 + R_2} = \frac{3(1k)}{2k} = \underline{\underline{1.5V}}$$

$$V_A = V_{A1} + V_{A2} = \underline{\underline{2V}}$$

Due to virtual ground

$$V_A = V_B = 2V$$

For non-inverting amplifier

$$V_o = \frac{R_F}{R} V_B$$

$$V_o = \left[1 + \frac{R_F}{R} \right] V_A$$

$$V_o = \left[1 + \frac{5k}{1k} \right] 2$$

$$\underline{\underline{V_o = 12V}}$$

Q16: Calculate the value of R_f from the circuit such that $V_o = 0$.

Sol: Using superposition

CASE1: 6V is ground

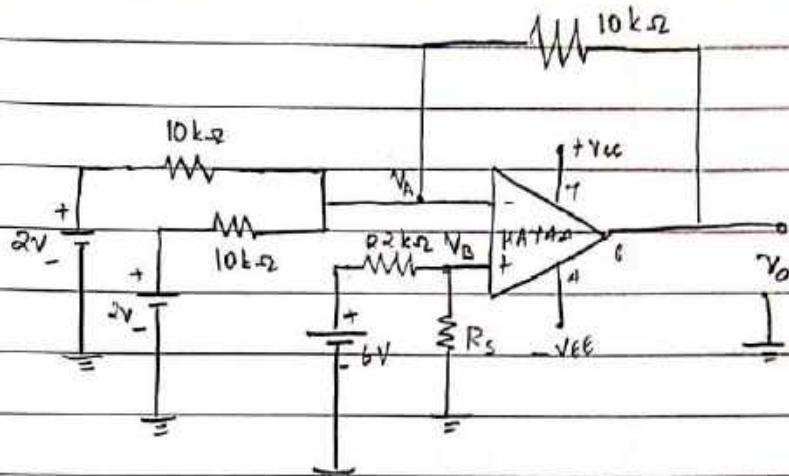
hence the circuit acts as inverting summer.

$$V_o' = \left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 \right]$$

$$V_o' = - \left[\frac{10k\Omega}{10k\Omega} + \frac{10k\Omega}{10k\Omega} \right] V_2$$

$$V_o' = - [2+2]$$

$$\underline{\underline{V_o' = -4V}}$$



CASE2: 2V batteries are grounded, hence the circuit acts as non-inverting

$$V_o'' = \left[1 + \frac{R_f}{R_1} \right] V_B$$

$$V_o'' = \left[1 + \frac{10k\Omega}{5k\Omega} \right] V_B$$

$$V_o'' = 3V_B$$

by voltage divider

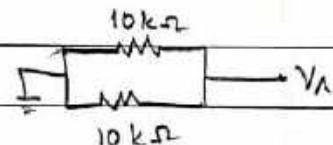
$$V_B = \frac{6Rs}{22k\Omega + Rs}$$

$$\therefore V_o'' = 3 \left[\frac{6Rs}{22k\Omega + Rs} \right]$$

Total output voltage

$$V_o = V_o' + V_o''$$

$$V_o = -4 + \frac{18Rs}{22k\Omega + Rs}$$



Given that $V_o = 0$

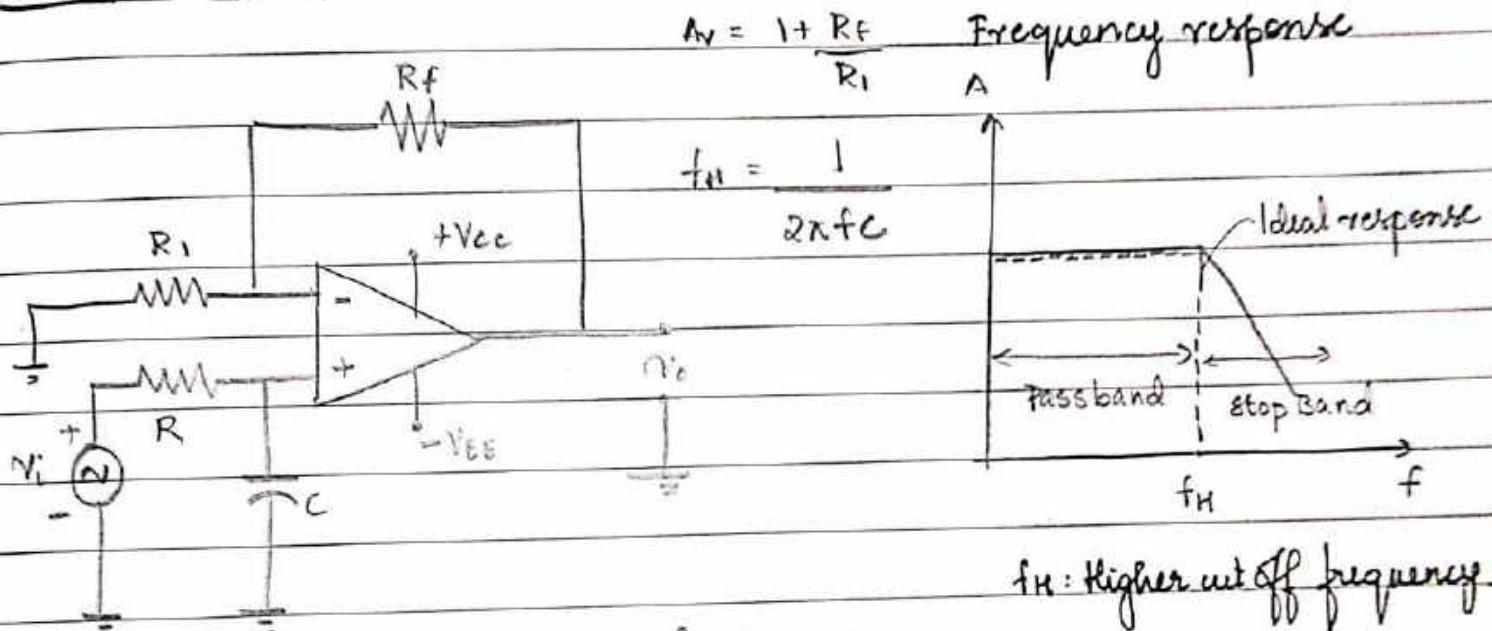
$$0 = -4 + \frac{18Rs}{22k\Omega + Rs}$$

$$4 = \frac{18Rs}{22k\Omega + Rs}$$

$$4Rs + 88k\Omega = 18Rs$$

$$14Rs = 88k\Omega$$

$$\underline{\underline{Rs = 6.286k\Omega}}$$

Low Pass Filter:

A low pass filter has a constant gain from 0Hz to a high cut off frequency f_H . A low pass filter allows frequency upto f_H and then attenuates the higher frequency. After f_H the gain is decreasing with the increase in input frequency. Bandwidth is equal to f_H .

Frequencies between 0Hz to f_H : pass band frequencies
 Frequencies which are above f_H are attenuated : stop band frequencies.

Q1: Design a low pass filter at a cut off frequency $f_H = 10 \text{ kHz}$ and pass band gain of 2.

Sol: Given: $A_p = 2 \quad f_H = 10 \text{ kHz}$

$$f_H = \frac{1}{2\pi RC}$$

$$A_p = 1 + \frac{R_f}{R_i}$$

$$RC = \frac{1}{2\pi(10k)}$$

$$A_p = 1 + \frac{R_f}{R_i}$$

Assuming $C = 0.01 \mu\text{F}$

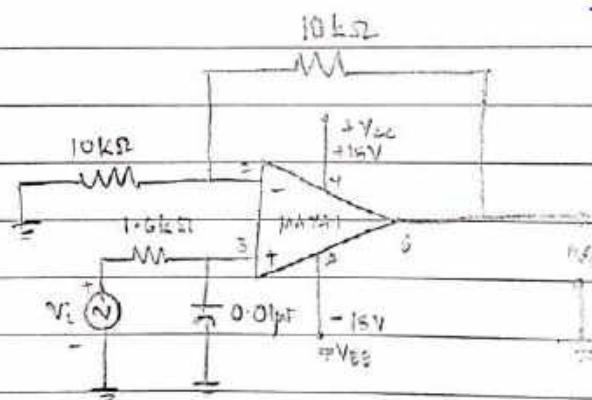
$$R = \frac{1}{2\pi(10k)(0.01\mu)}$$

$$\frac{R_f}{R_i} = 1$$

$$R = 1.6 \text{ k}\Omega$$

Assuming $R_f = 10 \text{ k}\Omega$

$$\therefore R_i = 10 \text{ k}\Omega$$



Q2: Design a low pass filter at a cut off frequency of 15.9 kHz with a pass band gain of 1.5.

Sol:

$$f_H = \frac{1}{2\pi RC}$$

$$A = 1.5 = 1 + \frac{R_f}{R_i}$$

Assuming $C = 0.01 \mu\text{F}$

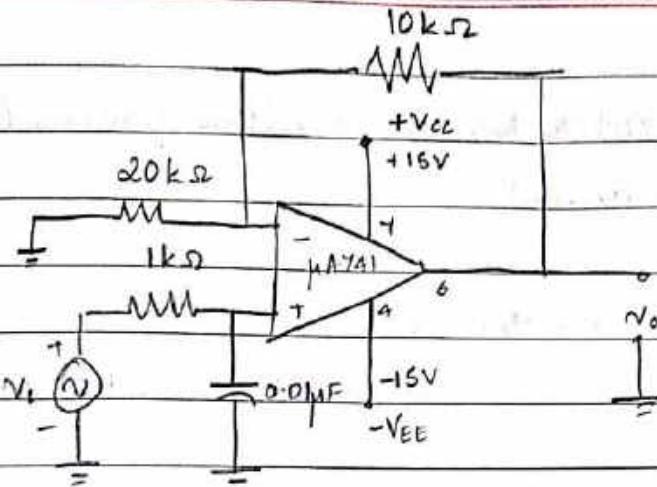
$$\Rightarrow R_f = 0.5 R_i$$

$$R = \frac{1}{2\pi(15.9k)(0.01\mu)}$$

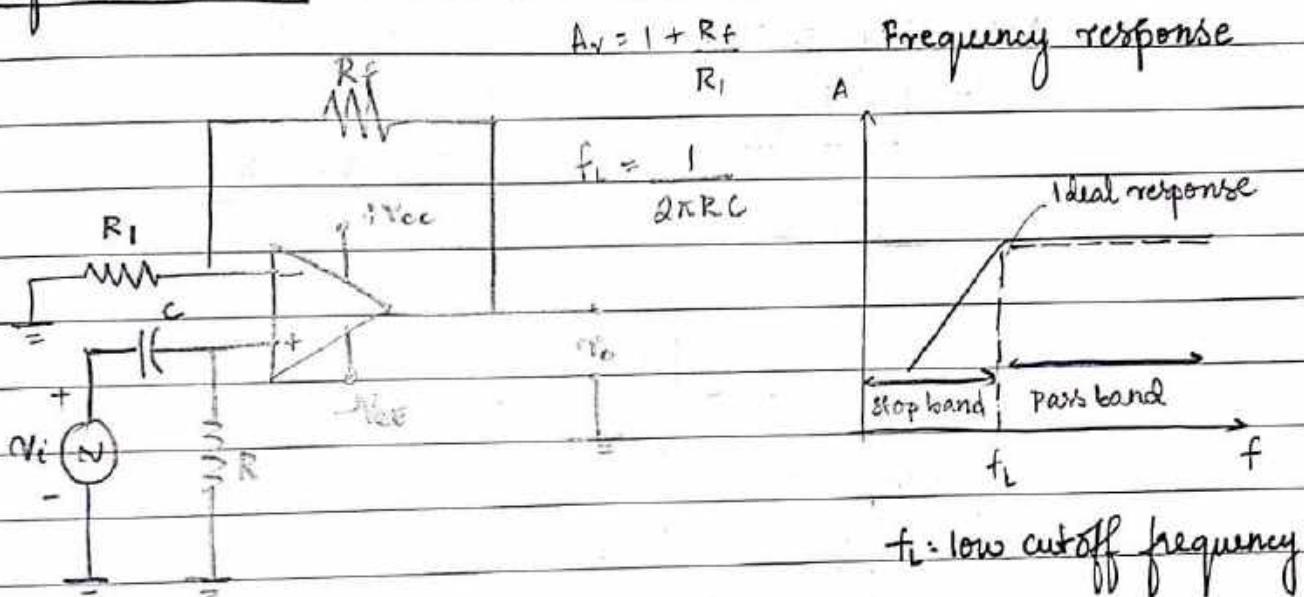
Assuming $R_f = 10 \text{ k}\Omega$

$$R = 1 \text{ k}\Omega$$

$$R_i = 20 \text{ k}\Omega$$



* High Pass Filter:



A high pass filter has a constant gain from low cut-off frequency and above. A high pass filter attenuates frequencies upto f_L and then allows frequency above f_L .

From 0Hz to f_L the gain increases with increase in input frequency.

Frequencies between 0Hz to f_L : stop band frequencies as they are attenuated and frequencies above f_L : pass band frequencies.

Q1: Design a first order high pass filter to have lower cut off frequency of 1.5 kHz and a pass band gain of 1.5.

Sol: Given: $f_L = 1.5 \text{ kHz}$ $A = 1.5$

$$f_L = \frac{1}{2\pi RC}$$

$$A = 1 + \frac{R_f}{R_1}$$

$$RC = \frac{1}{2\pi(1.5k)}$$

$$1.5 = 1 + \frac{R_f}{R_1}$$

Assuming $C = 0.01 \mu\text{F}$

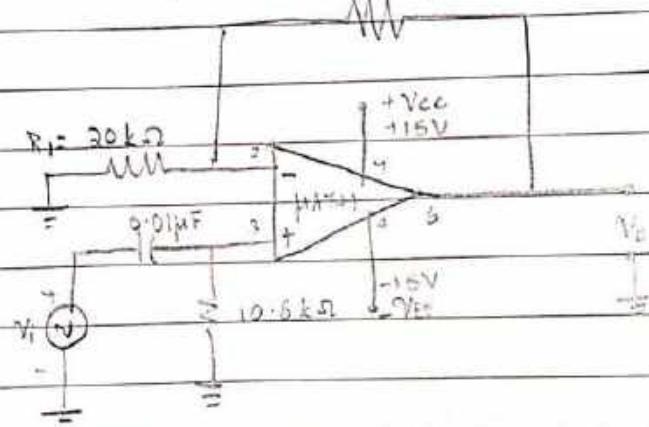
$$R = 10.6 \text{ k}\Omega$$

$$R_f = 0.5 R_1$$

Assuming $R_f = 10 \text{ k}\Omega$

$$R_1 = 20 \text{ k}\Omega$$

$$R_f = 10 \text{ k}\Omega$$



* Differentiator and Integrator:

→ Design steps for differentiator and integrator:

Select f_a equal to highest frequency of the input signal to be differentiated. Then assuming the value of $C_1 < 1 \mu\text{F}$.

Calculate the value of R_f

$$f_a = \frac{1}{2\pi R_f C_f}$$

$$f_b = \frac{1}{2\pi R_1 C_1}$$

$$R_1 C_1 = R_f C_f$$

Choose $f_b = 10 f_a$ or $f_b = 20 f_a$ and calculate R and C . (In most of the wave shaping circuits and FM modulator we use integrator and differentiator.)

Differentiator:

The circuit performs the mathematical operation of differentiation i.e., the output waveform is the derivative of the input waveform. The differentiator is constructed by replacing the input resistance R_i of inverting amplifier by a capacitor C_i .

Due to virtual ground

$$V_x = 0$$

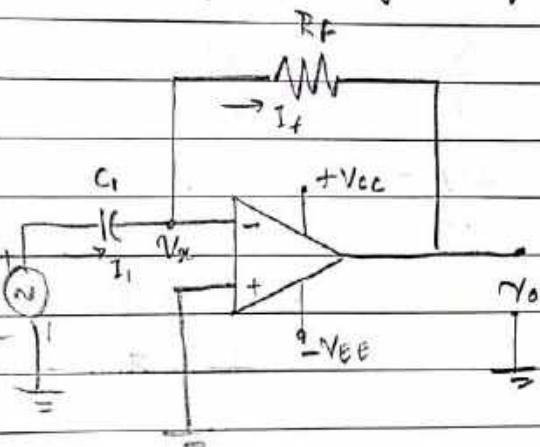
Applying KCL

$$I_i = I_f$$

$$C_i \frac{d[V_i - V_x]}{dt} = \frac{V_x - V_o}{R_f}$$

$$C_i \frac{dV_i}{dt} = -\frac{V_o}{R_f}$$

$$V_o = -R_f C_i \frac{dV_i}{dt}$$

Differentiator

Input:

sine

triangular

Output:

sine

square wave

Integrator:

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator or the integration amplifier. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_f is replaced by a feedback capacitor C_f .

Due to virtual ground

$$V_x = 0$$

Applying KVL

$$I_1 = I_f$$

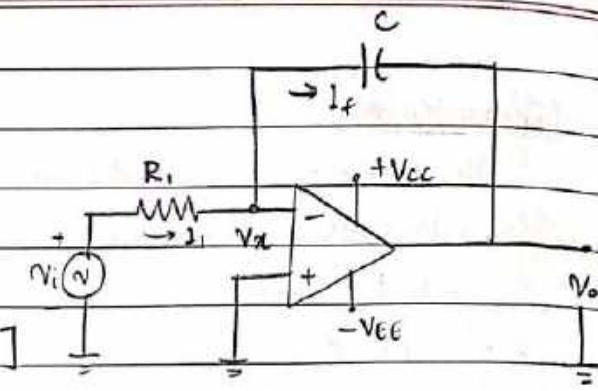
$$\frac{V_i - V_o}{R_1} = C \frac{d(V_o)}{dt}$$

$$R_1$$

$$\frac{V_i}{R_1} = -C \frac{dV_o}{dt}$$

$$\frac{dV_o}{dt} = -\frac{1}{RC} V_i$$

$$V_o = -\frac{1}{RC} \int_{0}^{t} V_i dt$$



Integrator:

Input	Output
sine	cosine
square	triangular

- Q1: a. Design a differentiator to differentiate an input signal that varies in frequency from 10Hz to about 1kHz.
 b. If a sine wave of 1V peak at 1000Hz is applied to the differentiator of part a, then draw the output waveform.

Sol: Given: $f_a = 1\text{kHz}$ $f_b = 10\text{Hz}$

$$f_a = \frac{1}{2\pi R_f C_f}$$

$$\Rightarrow R_f = \frac{1}{2\pi(1\text{k})(0.01\mu)}$$

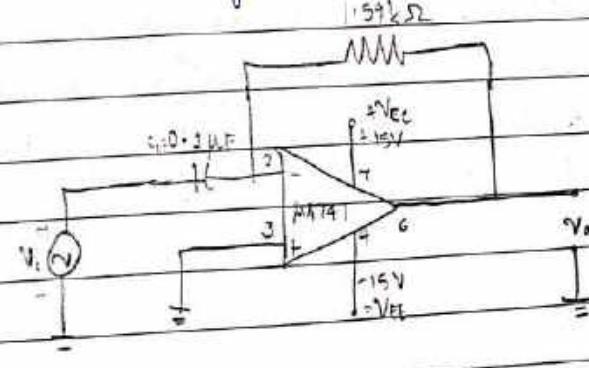
$$R_f = 1.59\text{k}\Omega$$

$$f_b = 20f_a$$

$$f_b = 20(1\text{k})$$

$$f_b = 20\text{kHz}$$

Assuming $C_f < 1\mu\text{F}$



$$f_b = \frac{1}{2\pi R_1 C_1}$$

$$20k = \frac{1}{2\pi R_1 (0.1\mu F)} \quad \text{assuming } C_1 < 1\mu F$$

$$R_1 = 79.57\Omega$$

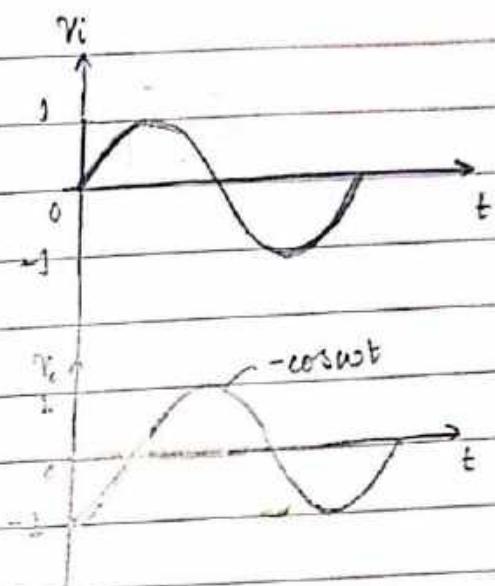
b. $V_o = -R_f C_1 \frac{dV_i}{dt}$

$$V_o = -(1.59k)(0.1\mu) \frac{d(\sin \omega t)}{dt}$$

$$V_o = -159 \times 10^{-6} \omega \cos \omega t$$

$$V_o = -159 \times 10^{-6} (2\pi(1000)) \cos \omega t$$

$$V_o = -0.199 \cos \omega t$$



Q2: Design a differentiator using op-amp to differentiate an input signal with $f_{max} = 200\text{Hz}$. Also draw the output waveform for a sine wave input of $1V_p$ at 200Hz .

sol: $f_a = 200\text{Hz}$

assume: $C_f = 0.1\mu F$

$$f_a = \frac{1}{2\pi R_f C_f} \Rightarrow R_f = \frac{1}{2\pi(0.1\mu F)(200)}$$

$$\therefore R_f = 7.95k\Omega$$

$$f_b = 10f_a = 2000\text{Hz}$$

$$f_b = \frac{1}{2\pi R_1 C_1} \Rightarrow R_1 = \frac{1}{2\pi(2000)(0.1\mu)}$$

$$\therefore R_1 = 0.795k\Omega$$

$$V_i = 1 \sin(2\pi \times 200)t$$

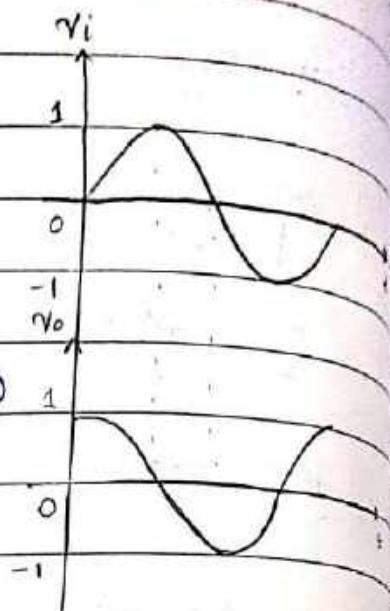
$$V_o = -R_f C_1 \frac{dV_i}{dt}$$

$$V_o = -(7.95k)(0.1\mu F) \frac{d}{dt} \sin(\pi \times 200t)$$

$$V_o = -7.95 \times 10^{-4} \cos(2\pi 200t) \times 2\pi (200)$$

$$V_o = -0.999 \cos(2\pi 200t)$$

$$V_o \approx -i \cos(2\pi 200t)$$



Q3: Assuming $R_f = 100k\Omega$ and $R_i = 10k\Omega$ and $C_f = 10nF$ in a practical integrator circuit, determine the lower frequency limit of integrator and output response for the sine wave input.

$$\text{Sol: } R_i = 10k\Omega \quad R_f = 100k\Omega \quad C_f = 10nF$$

$$f_a = \frac{1}{2\pi R_f C_f}$$

$$\Rightarrow f_a = \frac{1}{2\pi(100k)(10n)} = 159 \text{ Hz}$$

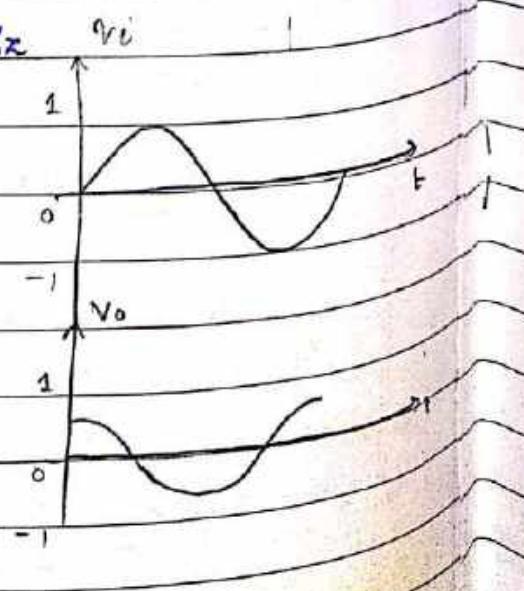
For an input voltage of 1Vp and 2.5kHz

$$V_o = -\frac{1}{R_i C_f} \int V_i(t) dt$$

$$V_o = -\frac{1}{(10k)(10n)} \int \sin 2\pi(2.5k)t dt$$

$$V_o = -10000 \frac{[-\cos 2\pi(2.5k)t]}{2\pi(2.5k)}$$

$$V_o = 0.636 \cos 2\pi(2.5k)t$$



* Summing, scaling and averaging amplifiers using op-amp:
 Different configurations.

- Inverting configuration
- Non inverting configuration
- Differential configuration.

* Inverting configuration:

Due to virtual ground

$$V_1 = V_2 = 0$$

$$\Rightarrow I_{B1} = I_{B2} = 0$$

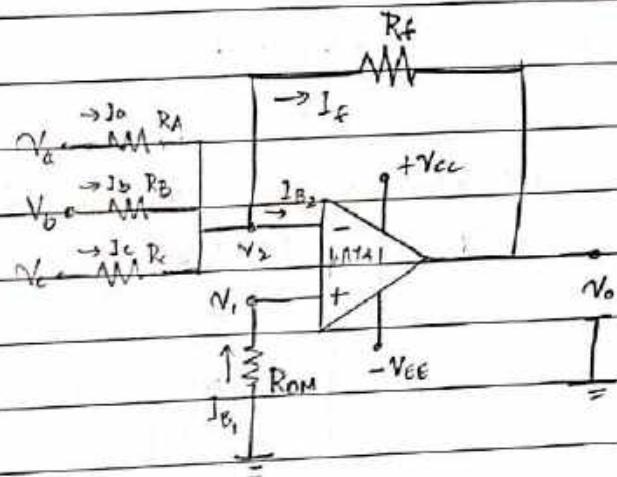
$$I_{B1} = I_{B2} = I_B$$

Applying KCL at V_2

$$I_a + I_b + I_c = I_f + I_B$$

$$\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c} = -\frac{V_o}{R_f}$$

$$\Rightarrow V_o = - \left[\frac{R_f}{R_a} V_a + \frac{R_f}{R_b} V_b + \frac{R_f}{R_c} V_c \right]$$



a. Summing amplifier:

If $R_a = R_b = R_c = R$, then

$$V_o = -\frac{R_f}{R} [V_a + V_b + V_c]$$

If gain is 1 then $V_o = -[V_a + V_b + V_c]$

b. Scaling or Weighted Amplifier:

$$\frac{R_f}{R_a} \neq \frac{R_f}{R_b} \neq \frac{R_f}{R_c}$$

$$V_o = - \left[\frac{R_f}{R_a} V_a + \frac{R_f}{R_b} V_b + \frac{R_f}{R_c} V_c \right]$$

c. Averaging amplifier:

If $R_a = R_b = R_c = R$ and gain $\frac{R_f}{R} = \frac{1}{n}$ where n is number of inputs.

$$V_o = -\frac{1}{n} [V_a + V_b + V_c]$$

* NON INVERTING CONFIGURATION:

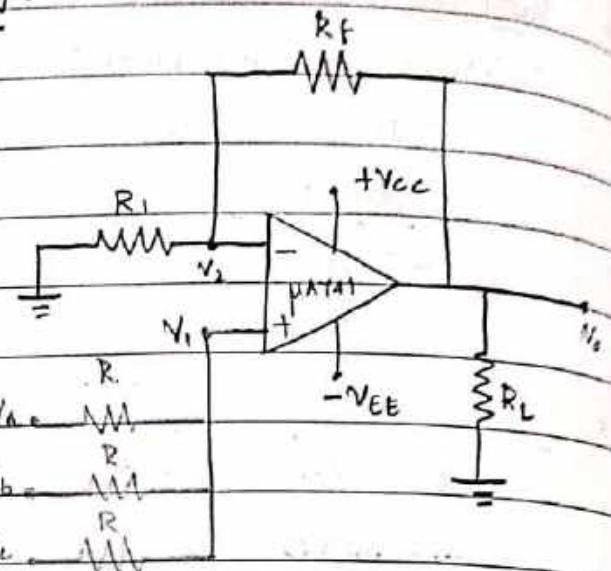
Here $R_a = R_b = R_c = R$

By superposition principle

$$V_i = \frac{R/2}{R+R/2} V_a + \frac{R/2}{R+R/2} V_b + \frac{R/2}{R+R/2} V_c$$

$$V_i = \frac{V_a}{3} + \frac{V_b}{3} + \frac{V_c}{3}$$

$$V_i = \frac{V_a + V_b + V_c}{3}$$



For noninverting configuration

$$V_o = \left[1 + \frac{R_f}{R_1} \right] V_i$$

$$\therefore V_o = \left[1 + \frac{R_f}{R_1} \right] \left[\frac{V_a + V_b + V_c}{3} \right]$$

a. Summing Amplifier

If $\left[1 + \frac{R_f}{R_1} \right]$ is number of inputs.

$$V_o = [V_a + V_b + V_c]$$

b. Averaging Amplifier

- No sign change or phase reversal occurs between the average of input and output.

- In non-inverting configuration V_i is the average of all the three inputs whereas in inverting configuration V_o is the average of all the three inputs.

$$V_o = - \left[\frac{V_a + V_b + V_c}{3} \right]$$

* DIFFERENTIAL CONFIGURATION:

By using differential configuration we can construct summing amplifier and subtractor.

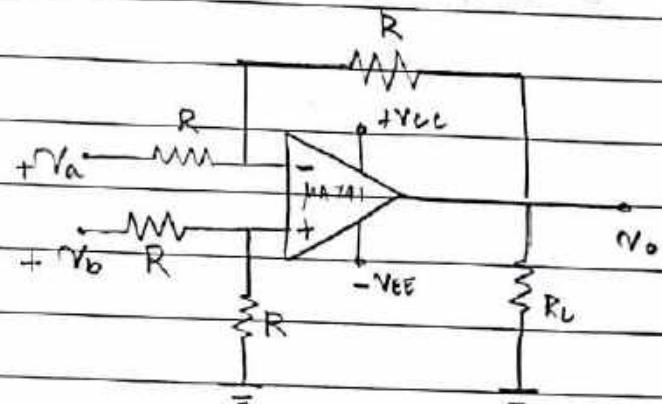
a. Subtractor:

For inverting

$$V_o = -\frac{R_f}{R_i} V_i$$

$$\therefore V_o = -\frac{R}{R} [V_a - V_b]$$

$$\boxed{V_o = V_b - V_a}$$



b. Summing amplifier:

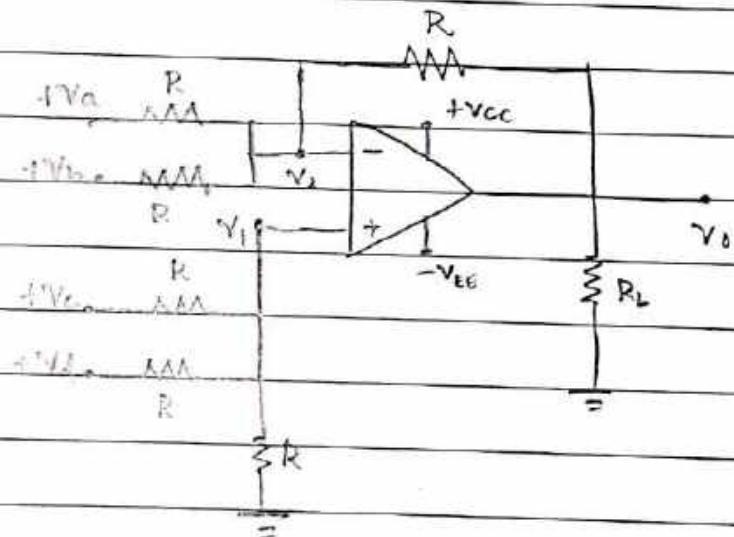
By superposition principle

$$V_{oa} = -\frac{R}{R} V_a = -V_a$$

$$V_{ob} = -\frac{R}{R} V_b = -V_b$$

$$V_{oc} = \left[1 + \frac{R}{R/2} \right] V_i = V_c$$

$$V_{od} = \left[1 + \frac{R}{R/2} \right] V_d = V_d$$



Output voltage

$$V_o = V_{oa} + V_{ob} + V_{oc} + V_{od}$$

$$\boxed{V_o = -V_a - V_b + V_c + V_d}$$

$$V_i = \frac{R/2}{R+R/2} V_c = \frac{V_c}{3}$$

$$V_i = \frac{R/2}{R+R/2} V_d = \frac{V_d}{3}$$

Q1: In the circuit shown in the figure (above)

$$R = 1k\Omega$$

$$V_a = 2V, V_b = 3V \text{ and } V_c = 4V, V_d = 5V$$

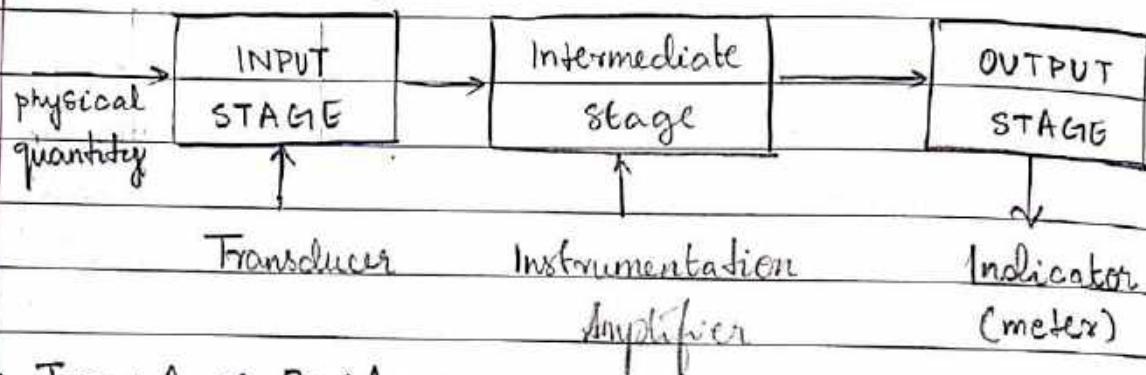
and the supply voltage is $\pm 15V$. Determine the output voltage V_o .

$$\boxed{\text{sol: } V_o = -2 - 3 + 4 + 5 = 4V}$$

* Instrumentation Amplifier:

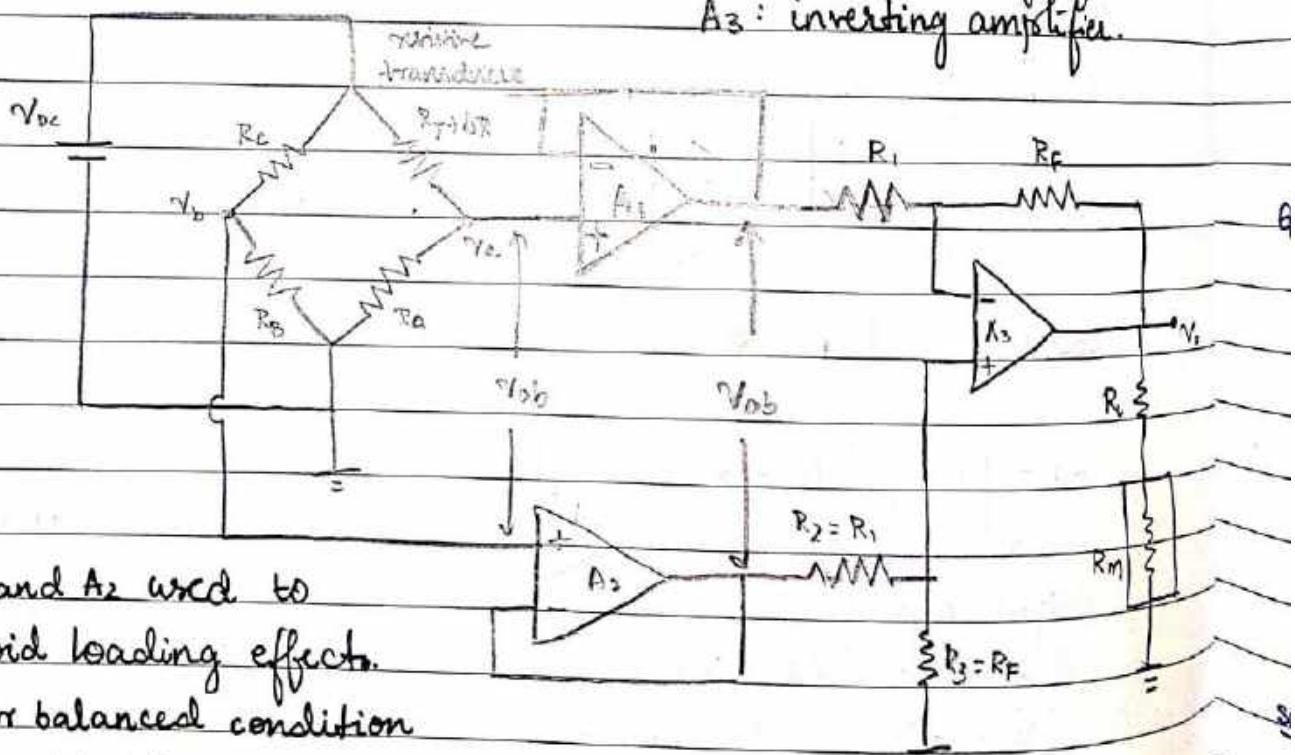
Application: used to measure physical quantities such as temperature, flow rate, pressure.

- Basic Block Diagram of Instrumentation Amplifier



- Transducer Bridge:

A_1 and A_2 : voltage follower
 A_3 : inverting amplifier.



A_1 and A_2 used to avoid loading effects.

For balanced condition

$$V_a = V_b$$

$$R_A = R_B = R_c = R_T$$

$$\frac{R_c}{R_B} = \frac{R_T}{R_A}$$

$$V_{ab} = V_a - V_b$$

$$V_a = V_{DC} \left[\frac{R_A}{R_A + (R_T + \Delta R)} \right]$$

$$V_b = V_{DC} \left[\frac{R_B}{R_B + R_c} \right]$$

$$V_{ab} = V_a - V_b = V_{DC} \left[\frac{R_A}{R_A + (R_T + \Delta R)} - \frac{R_B}{R_B + R_c} \right]$$

Let $R_A = R_B = R_C = R_T = R$

$$V_{ab} = V_{DC} \left[\frac{R}{2R + \Delta R} - \frac{R}{2R} \right]$$

$$V_{ab} = V_{DC} \left[\frac{2R - 2R - \Delta R}{2(2R + \Delta R)} \right]$$

$$V_{ab} = -V_{DC} \left[\frac{\Delta R}{2(2R + \Delta R)} \right]$$

For A₃ amplifier

$$V_o = \frac{-R_f}{R_1} V_{ab}$$

$$V_o = -\frac{R_f}{R_1} \left[-V_{DC} \left(\frac{\Delta R}{2(2R + \Delta R)} \right) \right] \quad 2R + \Delta R \approx 2R$$

$$\boxed{V_o = \frac{R_f}{R_1} V_{DC} \frac{\Delta R}{4R}} \Rightarrow V_o \propto \Delta R.$$

Q1: In an instrumentation amplifier $R_1 = 1k\Omega$, $R_f = 4.4k\Omega$, then $R_a = R_b = R_c = 100k\Omega$, then $V_{DC} = 5V$. The opamp supply voltage is $\pm 15V$. The transducer is a thermistor with the following specifications: $R_T = 100k\Omega$. At the reference temperature of $25^\circ C$, the temperature coefficient of resistance is equal to $1k\Omega / {}^\circ C$ or $1\% / {}^\circ C$. Determine the output voltage at $0^\circ C$ and at $100^\circ C$.

Sol: Given: $R_1 = 1k\Omega$ $R_f = 4.4k\Omega$ $V_{DC} = 5V$

$$R_a = R_b = R_c = 100k\Omega \quad +V_{CC} \text{ & } -V_{EE} = +15V$$

Reference Temp: $25^\circ C$. $R_T = 100k\Omega$

$$\text{TCR} = 1k\Omega / {}^\circ C$$

as $R_a = R_b = R_c = R_T = 100k\Omega$ at $25^\circ C$

It is balanced

$$\text{Hence } V_a = V_b \text{ and } V_o = 0$$

Temp (0°C)

CASE 1: $\Delta R = -1k \text{ (0-25)}$

$$\underline{\Delta R = 25k\Omega}$$

$$V_o = \frac{R_f}{R_i} V_{DC} \left[\frac{\Delta R}{4R} \right]$$

$$V_o = \frac{4.7k}{1k} (5) \frac{25k}{4(100k)}$$

$$\underline{V_o = 1.468 \text{ V}}$$

CASE 2: $\Delta R = -1k (100-25)$

$$\underline{\Delta R = -75k\Omega}$$

$$V_o = \frac{R_f}{R_i} V_{DC} \left[\frac{\Delta R}{4R} \right]$$

$$V_o = -\frac{4.7k}{1k} (5) \frac{75k}{4(100k)}$$

$$\underline{V_o = -4.4 \text{ V}}$$

* Voltage to current converter (Transconductance Amplifier)

Applications:

- low voltage ac or dc voltmeter
- zener diode tester
- LED

The conversion can be done by two methods

- a. V - I converter using floating load.
- b. V - I converter using grounded load.

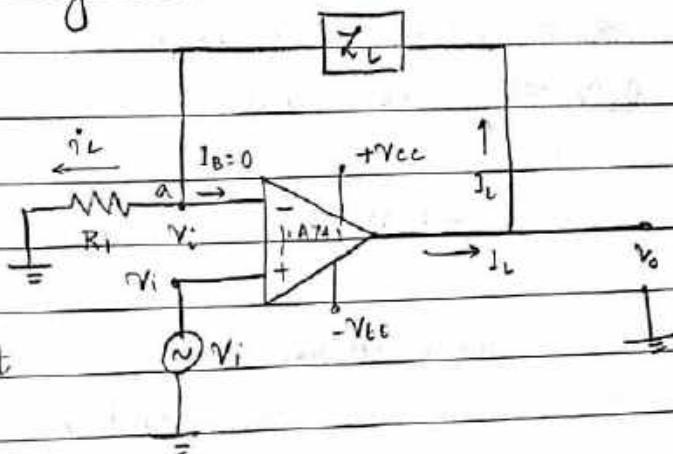
2. γ -1 converter using floating load at 'a' due to virtual ground potential is V_i

since $I_B = 0$

I_L is current across R_1 ,

$$\therefore V_i = I_L R_1 \text{ input}$$

$$\therefore I_L = \frac{V_i}{R_1} \text{ output}$$



2. γ -1 converter using grounded load

Due to virtual ground

at inverting terminal

potential is V_i .

At node 'a'

$$I_L = i_1 + i_2$$

$$I_L = \frac{V_i - V_1}{R} + \frac{V_o - V_1}{R}$$

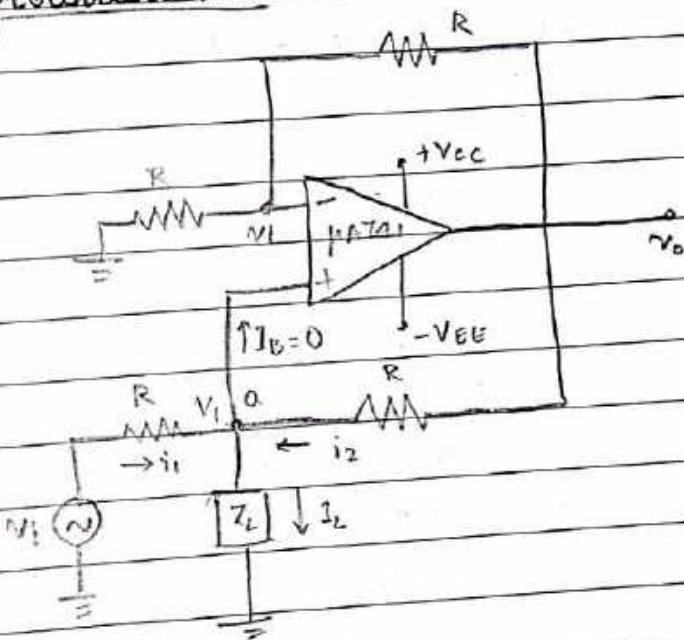
$$I_L = \frac{V_i - 2V_1 + V_o}{R}$$

$$I_L R = V_i - 2V_1 + V_o$$

$$V_1 = \frac{V_i + V_o - I_L R}{2} \text{ input}$$

$$\text{but } V_i = I_L R$$

$$I_L = \frac{V_i}{R}$$



* Current to Voltage converter (Transresistance Amplifier)
Applications

- Photo diode

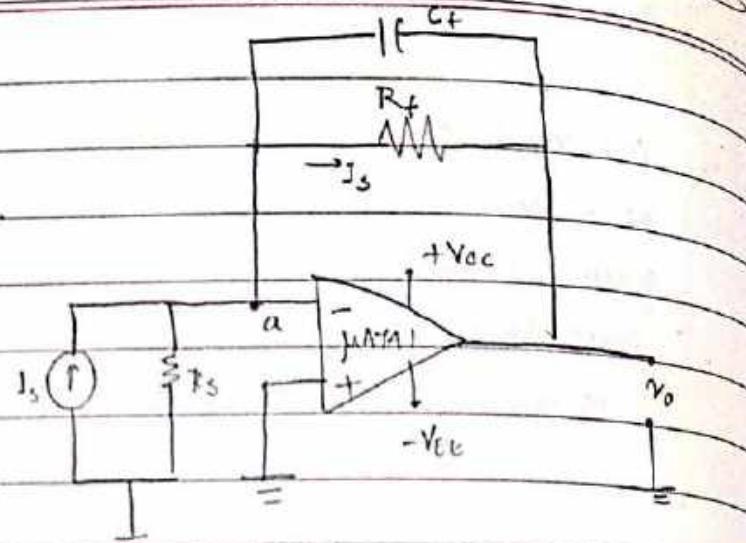
- Photo multiplier

- Photo FET Detector

Due to virtual ground
the potential at 'a' is 0.

$$\frac{V_o - V_a}{R_f} = I_s \text{ Input}$$

$$V_o = -I_s R_f \text{ output}$$

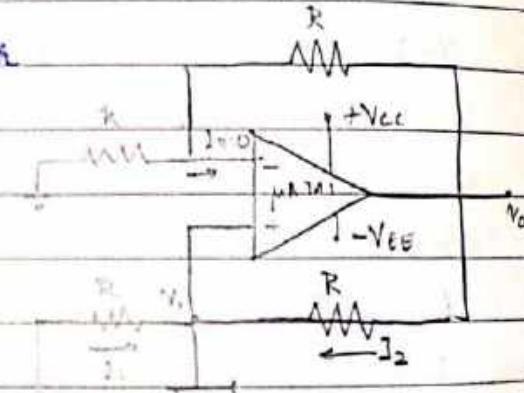


CF is used to reduce
the high frequency noise and oscillations.

Q: For a voltage to current converter

shown, $V_i = 5V$, $R = 10k\Omega$,

$V_1 = 1V$. Find the load current
and output voltage.



Sol: Initially assume $I_3 = 0$

$$I_L = I_1 + I_2$$

$$I_L = \frac{V_i - V_1}{R} + \frac{V_o - V_1}{R}$$

$$I_L = \frac{V_i + V_o - 2V_1}{R}$$

$$I_L = \frac{5 + 2 - 2(1)}{10k}$$

$$\underline{\underline{I_L = 0.5mA}}$$

For non inverting amplifier

$$V_o = \left[1 + \frac{R_f}{R_1} \right] V_i$$

Here $R_f = R_1 = R$

$$\underline{\underline{V_o = 2V_1}}$$

$$\underline{\underline{V_o = 2V}}$$

classmate

Date _____

Page _____

current Amplifier:

At output applying KVL

$$I_o = I_s + I_L$$

$$I_o = \frac{V_o}{R_1} + \frac{V_o}{R_L}$$

$$I_o = V_o \left[\frac{1}{R_1} + \frac{1}{R_L} \right]$$

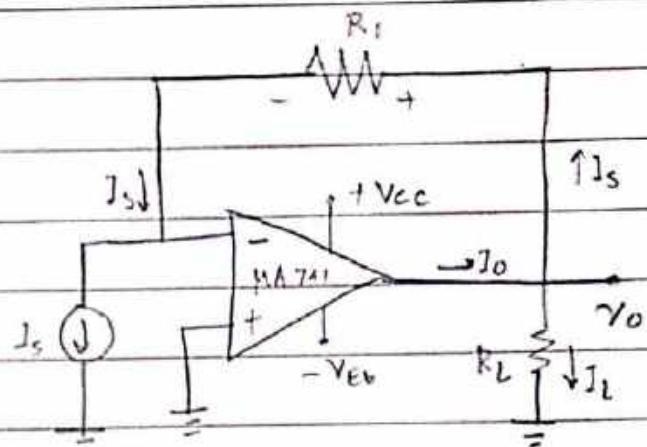
$$\therefore \boxed{V_o = \frac{R_1 R_2}{R_1 + R_2} I_o}$$

$$\text{but } V_o = I_L R_L$$

$$\frac{R_1 R_2}{R_1 + R_2} I_o = I_L R_L$$

$$\frac{R_1 R_2}{R_1 + R_2} [I_s + I_L] = I_L R_L$$

$$\boxed{I_L = I_s \frac{R_1}{R_L}}$$



Unit - 3

LINEAR APPLICATIONS OF AN OP AMP - 11

Precision Rectifier:

The precision rectifier is obtained with an operational amplifier in order to have a circuit behave like an ideal diode and rectifier. It is useful for high precision signal processing.

Precision Half Wave Rectifier:

Due to virtual ground

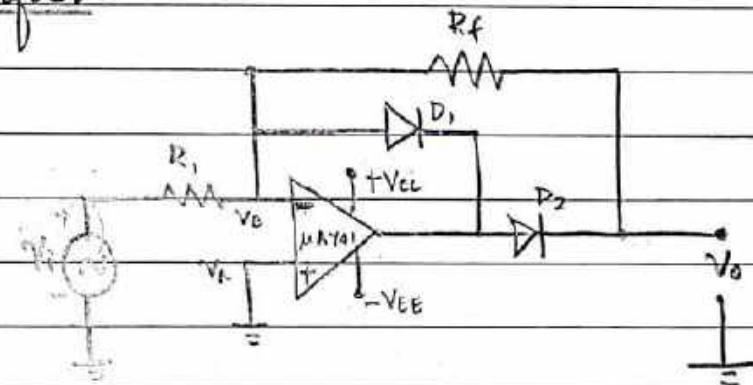
$$V_A = V_B = 0$$

During positive half cycle

D_1 - forward biased

D_2 - reverse biased

$$\therefore V_o = 0$$



During negative half cycle

D_1 - reverse biased

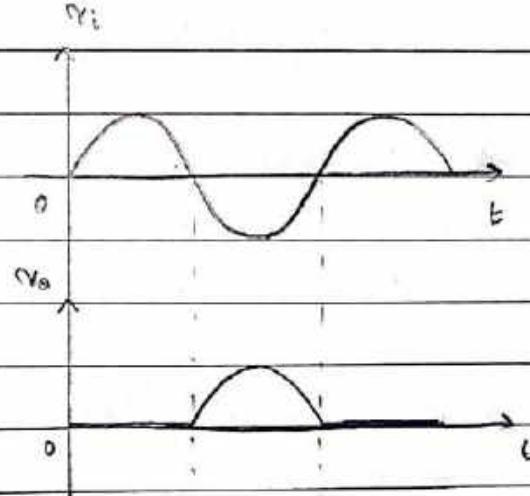
D_2 - forward biased

Then it is like an inverting amplifier

$$\therefore V_o = -\frac{R_f}{R_i} V_i$$

$$\cdot \text{ if } R_f = R_i, \text{ then } V_o = -V_i$$

(Positive)

Precision Full Wave Rectifier:

During positive half cycle

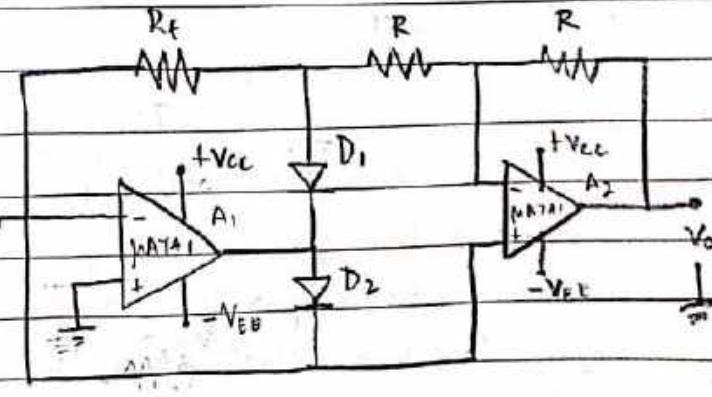
A_1 is negative

$\therefore D_1$ is forward biased

D_2 is reverse biased

Here op-amp 1 acts as inverting amplifier

$$\therefore V_{o1} = -\frac{R_f}{R_i} V_{in} \Rightarrow V_{o1} = -V_{in}$$



If $R_1 = R_f$ then $V_o = -V_{in}$

Now op amp 2 acts as an inverting adder

$$\therefore V_o = - \left[\frac{R}{R/2} V_{o1} + \frac{R}{R} V_{in} \right]$$

but $V_{o1} = -V_{in}$

$$\therefore V_o = - \left[-2V_{in} + V_{in} \right]$$

$$\boxed{V_o = V_{in}}$$

During negative half cycle
A1 is positive

$\therefore D_1$ is reverse biased and D_2 is forward biased

But due to virtual ground output of op amp 1, $V_{o1} = 0$.

Now op amp 2 has an output

$$V_o = - \left[\frac{R}{R} V_{in} + \frac{R}{R/2} V_{o1} \right]$$

$$\therefore \boxed{V_o = -V_{in}}$$

* Filters:

- Based on the nature of signal processing, filters are classified as:

a. Analog filter

b. Digital filter.

- Based on the components used, filters are classified as:

a. Active filters

b. Passive filters.

- Based on the frequency, filters are classified as:

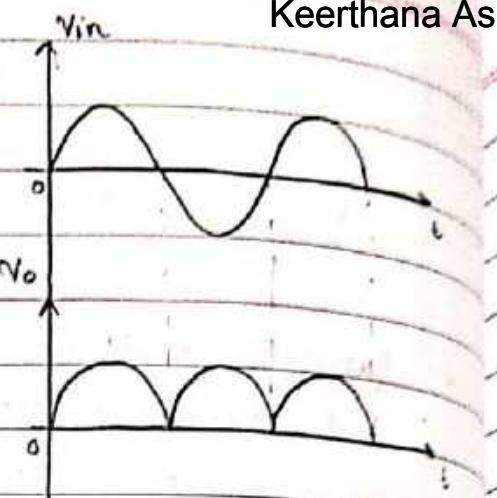
a. lowpass filter.

b. high pass filter.

3. bandpass filter.

4. band stop / band elimination / band reject filter.

5. All pass filter.



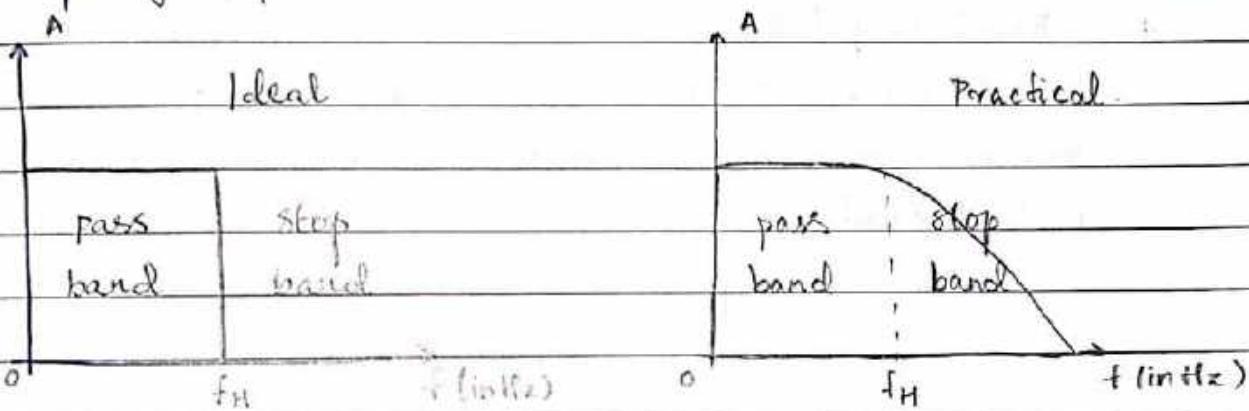
* Active filters:

Passive filters (R,L,C) along with op-amp /transistor forms an active filter.

1. Low pass filter:

It allows the frequency range upto the cut off frequency f_H , beyond which it attenuates.

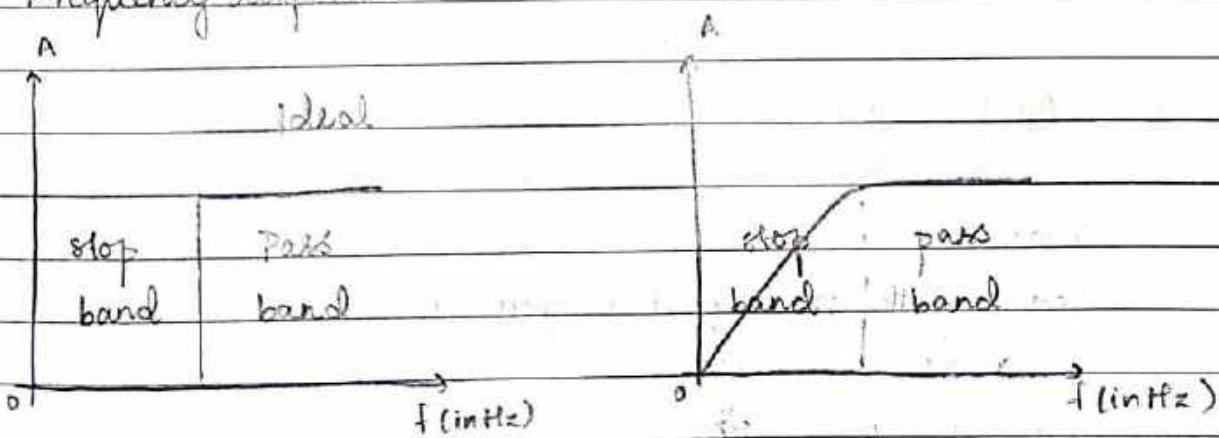
Frequency response



2. High pass filter:

It allows the frequency range beyond the cut off frequency, f_L , until f_H it is attenuated.

Frequency response

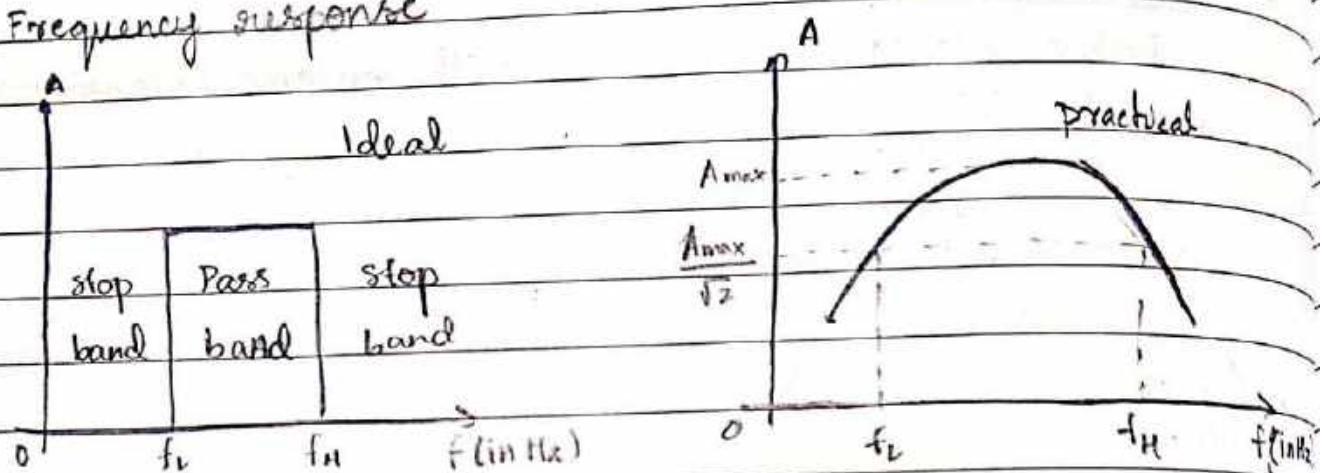


3. Band Pass filter:

It allows the band of frequency of the range f_L to f_H . Other frequencies are attenuated.

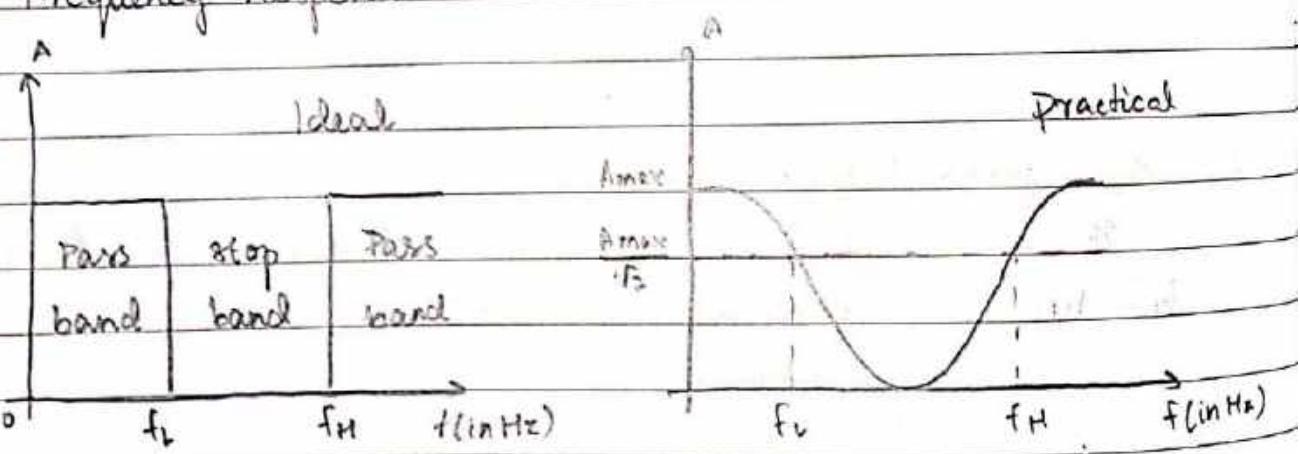
(combination of high pass and low pass filter)

Frequency response



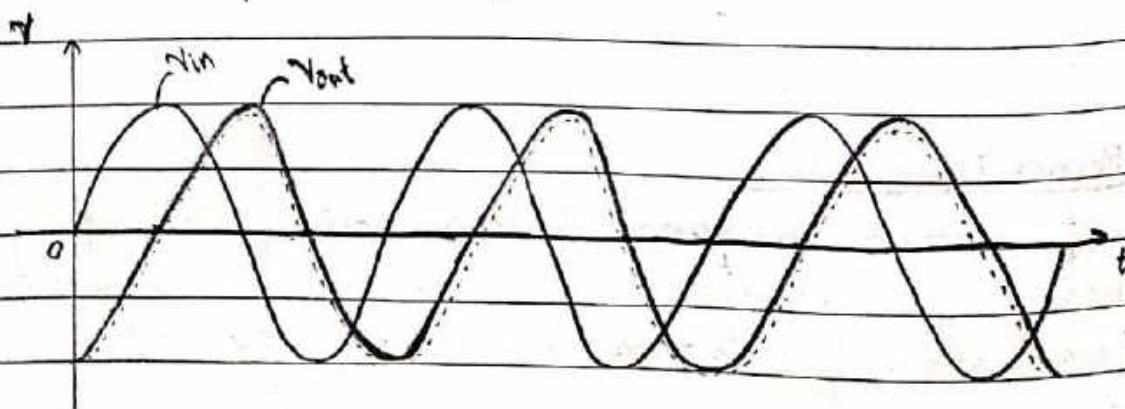
4. Band stop filter (notch filters: based on shape of frequency response)
 It blocks/attenuates the frequencies from f_L to f_H frequency range and all other frequencies are allowed to pass through.

Frequency response



5. All pass filter

It allows all frequency to pass through, that is from zero to maximum. But there is around 90° phase shift between the input and output.



* Order of filter:

Depending upon the gain roll off the filters may be classified as first order, second order, third order, etc.

order of filter	Rate of roll off of the gain
I order	-20 dB/decade
II order	-40 dB/decade
III order	-60 dB/decade
IV order	-80 dB/decade

Note: Number of RC network is equal to the order of the filter

* Filters are also classified as:

1. Butterworth filter
2. Chebyshev filter
3. Elliptic filter
4. Bessel filter

* 1 order Low Pass Butterworth filter:

For a non-inverting amplifier

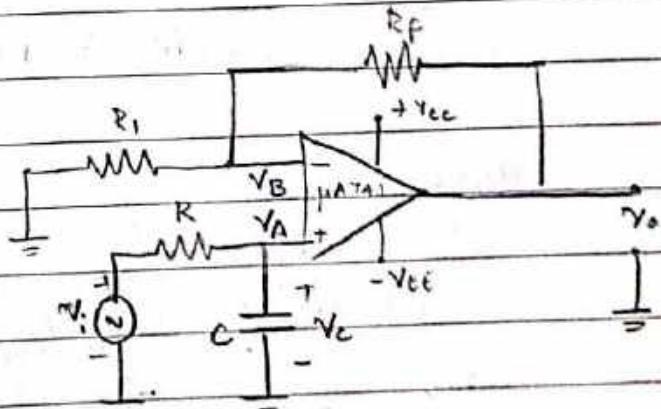
$$A = 1 + \frac{R_f}{R_1}$$

$$\therefore V_o = \left[1 + \frac{R_f}{R_1} \right] V_A \quad \textcircled{1}$$

By superposition.

$$V_A = V_c = -jX_C V_i$$

$$V_A = V_c = \frac{-j}{2\pi f C} V_i = \frac{-j V_i}{2\pi f C}$$



$$V_A = V_C = \frac{-jV_i}{2\pi f R C - j}$$

$$V_A = V_C = \frac{V_i / j}{2\pi f R C + j}$$

$$V_A = V_C = \frac{V_i / j}{j \frac{2\pi f R C + j}{j}}$$

$$\therefore V_A = V_C = \frac{V_i}{j^2 2\pi f R C + 1}$$

Substituting in eq ①

$$V_o = \left[1 + \frac{R_f}{R_1} \right] \left[\frac{V_i}{1 + j^2 2\pi f R C} \right]$$

Here $A_f = 1 + \frac{R_f}{R_1}$ and $\frac{1}{j^2 2\pi f R C} = f_H$

$$\therefore V_o = A_f \left[\frac{V_i}{1 + j f / f_H} \right]$$

$$\boxed{\frac{V_o}{V_i} = \frac{A_f}{1 + j \left(\frac{f}{f_H} \right)}}$$

Magnitude

$$\boxed{\left| \frac{V_o}{V_i} \right| = \frac{A_f}{\sqrt{1 + \left(\frac{f}{f_H} \right)^2}}}$$

Phase angle

$$\boxed{\phi = \tan^{-1} \left(\frac{f}{f_H} \right)}$$

Frequency response of Low pass Butterworth filter:

$$\frac{V_o}{V_i} = \frac{A_f}{1 + j(f/f_H)}$$

CASE 1: For frequency $f = 0$.

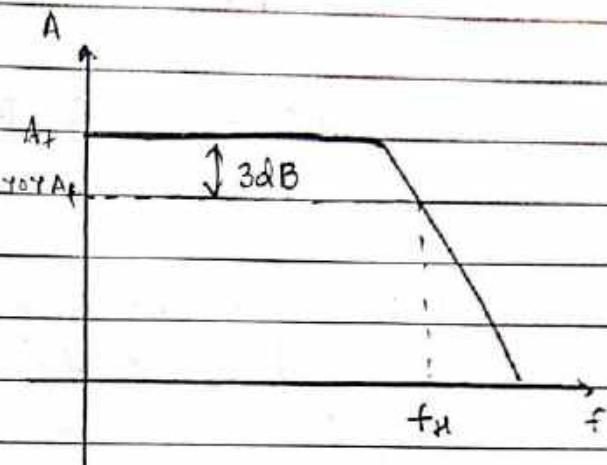
$$A = A_f$$

CASE 2: For frequencies $f < f_H$

$$A = A_f$$

CASE 3: For frequency $f = f_H$

$$A = \frac{A_f}{\sqrt{2}} = 0.707 A_f$$



CASE 4: For frequencies $f > f_H$

$$A < A_f$$

Design rule for low pass Butterworth filter:

Assume $C \leq 1\mu F$.

$$f_H = \frac{1}{2\pi RC}$$

$$\text{Gain: } A_f = 1 + \frac{R_f}{R_1}$$

Frequency scaling technique to find new resistance

$$\text{Ex: } f_H = 10 \text{ kHz} \quad f_H' = 12 \text{ kHz}$$

$$R_{\text{new}} = R \left(\frac{f_H}{f_H'} \right)$$

Q: Design a low pass filter at a cut off frequency of 10 kHz with a pass band gain of 2.

Sol:

$$\text{Given: } f_H = 10 \text{ kHz} \quad A_f = 2$$

$$\text{Assuming } C = 0.01 \mu F$$

$$f_H = \frac{1}{2\pi RC} \Rightarrow R = \frac{1}{2\pi(10k)(0.01\mu)} = \underline{\underline{1.59 \text{ k}\Omega}}$$

$$A_f = 1 + \frac{R_f}{R_1}$$

$$2 = 1 + \frac{R_f}{R_1}$$

$$\frac{R_f}{R_1} = 1 \Rightarrow R_f = R_1 \quad \text{For } R_f = 10k\Omega$$

$$R_1 = 10k\Omega$$

Q2: If in the previous problem the cut off frequency is changed from 10kHz to 12kHz , find the new value of R using frequency scaling technique.

Sol: Given: $f_H = 10\text{kHz}$ $f_{H'} = 12\text{kHz}$

$$R_{\text{New}} = R \left(\frac{f_H}{f_{H'}} \right)$$

$$R_{\text{New}} = 1.59k \left(\frac{10k}{12k} \right)$$

$$R_{\text{New}} = 1.326k\Omega$$

* II Order Low Pass Butterworth Filter:

Let $R_2 = R_3 = R$

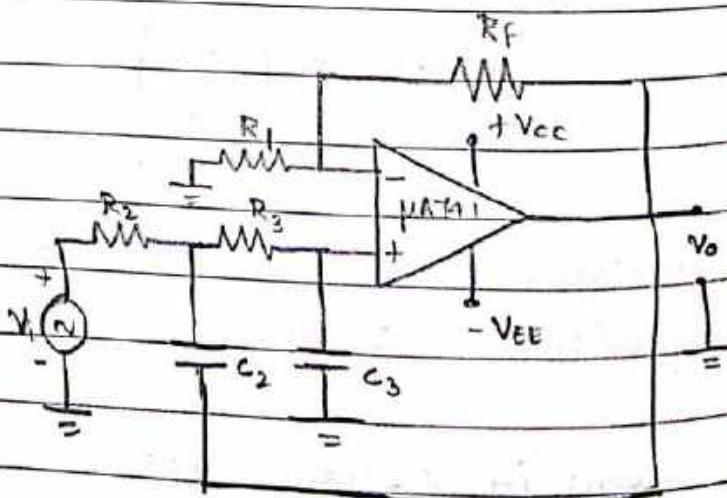
and $C_2 = C_3 = C$

$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

$$\therefore f_H = \frac{1}{2\pi R C}$$

Magnitude

$\left \frac{V_o}{V_i} \right $	$=$	A_f
	$=$	$\sqrt{1 + \left(\frac{f}{f_H} \right)^4}$



Designing of 11 order Butterworth low pass filter:

Assume $C < 1\mu F$

$$A_f = 1 + \frac{R_f}{R_1}$$

$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}} \quad \text{if } R_2 = R_3 \text{ & } C_2 = C_3 \text{ - then } f_H = \frac{1}{2\pi R C}$$

$$R_1 \leq 100 k\Omega$$

If the gain value is not given then assume that

$$A_f = 1 + \frac{R_f}{R_1} = 1.586$$

$$\text{where } \frac{R_f}{R_1} = 0.586 \Rightarrow R_f = 0.586 R_1$$

Q1: Design a 11 order low pass Butterworth filter to have a higher cut-off frequency of 1.5 kHz.

Sol: Given: $f_H = 1.5 \text{ kHz}$

Assuming $C = 0.05 \mu F$

$$f_H = \frac{1}{2\pi R C}$$

$$\Rightarrow R = \frac{1}{2\pi f_H C} = \frac{1}{2\pi (1.5 \text{ k})(0.05 \mu)} = 2.12 k\Omega$$

since A_f is not given, assuming $A_f = 1.586$

$$\therefore 1 + \frac{R_f}{R_1} = 1.586$$

$$\frac{R_f}{R_1} = 0.586$$

$$R_f = 0.586 R_1$$

Assuming $R_1 = 29 k\Omega$

$$R_f = 15.822 k\Omega$$

* 1 Order high pass Butterworth Filter:

For non inverting amplifier

$$A = 1 + \frac{R_f}{R_1}$$

$$R_1$$

$$\therefore V_o = \left[1 + \frac{R_f}{R_1} \right] V_A \quad \text{--- (1)}$$

By superposition

$$V_A = \frac{RV_i}{R - jX_C}$$

$$V_A = \frac{RV_i}{jX_C \left(\frac{R}{jX_C} - 1 \right)} \quad \text{where } X_C = \frac{1}{2\pi f C}$$

$$V_A = \frac{RV_i}{\frac{j}{2\pi f C} \left[\frac{2\pi f RC}{j} - 1 \right]} = \frac{RV_i}{\frac{j}{2\pi f C} \left[\frac{2\pi f RC}{j} - j \right]}$$

$$V_A = \frac{\frac{2\pi f RC}{j} V_i}{2\pi f RC - j} = \frac{2\pi f RC V_i}{2\pi f RC + j}$$

$$V_A = \frac{j 2\pi f R C V_i}{j 2\pi f R C + 1}$$

Substituting in eq (1)

$$V_o = \left[1 + \frac{R_f}{R_1} \right] \left[\frac{j 2\pi f R C V_i}{j 2\pi f R C + 1} \right]$$

$$V_o = \left[1 + \frac{R_f}{R_1} \right] \left[\frac{j f / f_L}{j f / f_L + 1} \right] V_i$$

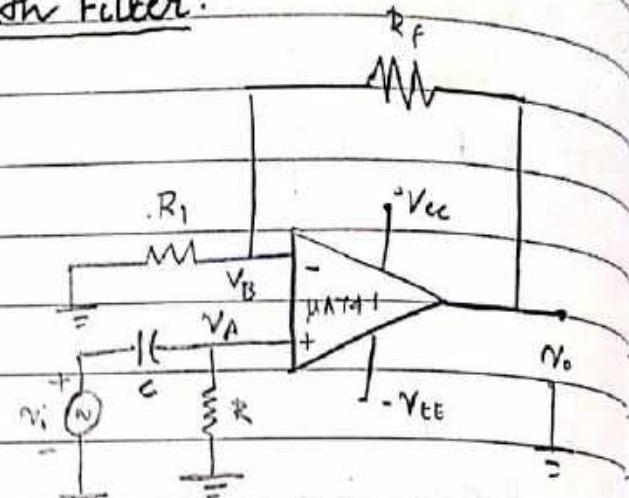
$$\frac{1}{2\pi R C} = f_L$$

$$\text{Here } \left[1 + \frac{R_f}{R_1} \right] = A_f$$

$$\frac{V_o}{V_i} = \frac{A_f j (f / f_L)}{j (f / f_L) + 1}$$

Magnitude

$$\left| \frac{V_o}{V_i} \right| = \sqrt{1 + \left(\frac{f}{f_L} \right)^2}$$



Frequency response of High Pass Butterworth filter:

$$V_o = A_f \cdot (f/f_L)$$

$$V_i = 1 + j(f/f_L)$$

CASE 1: $f = 0$

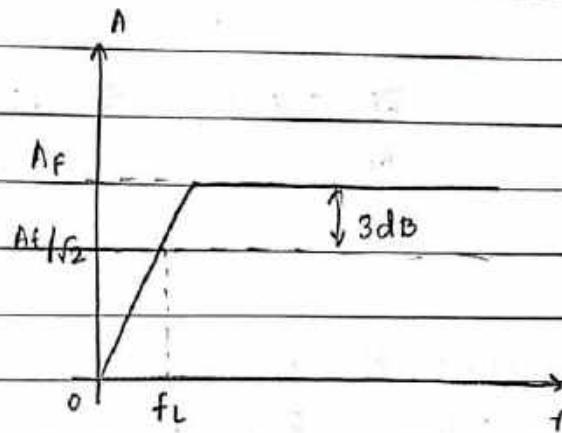
$$A = \infty$$

CASE 2: $f < f_L$

$$A < A_f$$

CASE 3: $f = f_L$

$$A = \frac{A_f}{\sqrt{2}} = 0.707 A_f$$



CASE 4: $f > f_L$

$$A = A_f$$

* 11 Order High Pass Butterworth Filter:

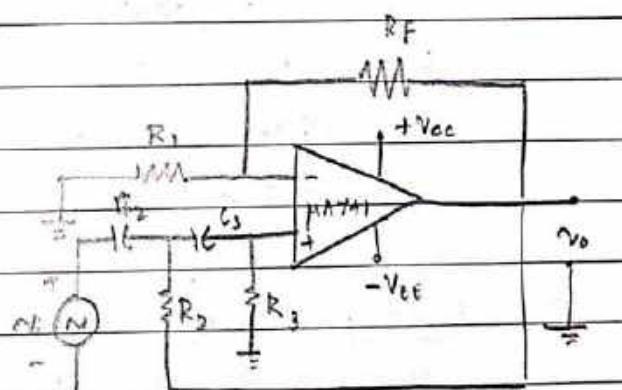
$$\text{Let } R_2 = R_3 = R \text{ and } C_2 = C_3 = C$$

$$f_L = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

$$\therefore f_L = \frac{1}{2\pi R C}$$

Magnitude

$$\left| \frac{V_o}{V_i} \right| = \frac{A_f (f/f_L)}{\sqrt{1 + \left(\frac{f}{f_L}\right)^4}}$$



Q1: Design a first order high pass filter to have a lower cut-off frequency of 1.5 kHz and the pass band gain of 1.5.

Sol: Given: $f_L = 1.5 \text{ kHz}$ $A = 1.5$

Assuming $C = 0.01 \mu\text{F}$

$$f_L = \frac{1}{2\pi R C} \Rightarrow R = \frac{1}{2\pi f L} = \frac{1}{2\pi (1.5k)(0.01\mu)} = 10.61 \text{ k}\Omega$$

$$A_f = 1 + \frac{R_f}{R_1}$$

$$1.5 = 1 + \frac{R_f}{R_1}$$

$$\frac{R_f}{R_1} = 0.5 \Rightarrow R_f = 0.5 R_1$$

Assuming $R_1 = 10\text{k}\Omega$

$$\therefore \underline{R_f = 5\text{k}\Omega}$$

Q2: Obtain the value of lower cut off frequency of 11 order high pass Butterworth filter. Given: $R_1 = 4.7\text{k}\Omega$ and $R_2 = R_3 = 10\text{k}\Omega$, $C_2 = C_3 = 0.01\mu\text{F}$.

Sol: Given: $R_1 = 4.7\text{k}\Omega$

$$R_2 = R_3 = 10\text{k}\Omega$$

$$C_2 = C_3 = 0.01\mu\text{F}$$

$$f = \frac{1}{2\pi R C} = \frac{1}{2\pi(10\text{k})(0.01\mu)}$$

$$\underline{f = 1.59\text{ kHz}}$$

* Band Pass Filter:

Based on the Q factor it is classified as

1. Wide band pass filter
2. Narrow band pass filter

$$Q\text{-factor} = \frac{f_c}{BW} \Rightarrow Q \propto \frac{1}{BW} \quad Q = \frac{f_c}{f_H - f_L}$$

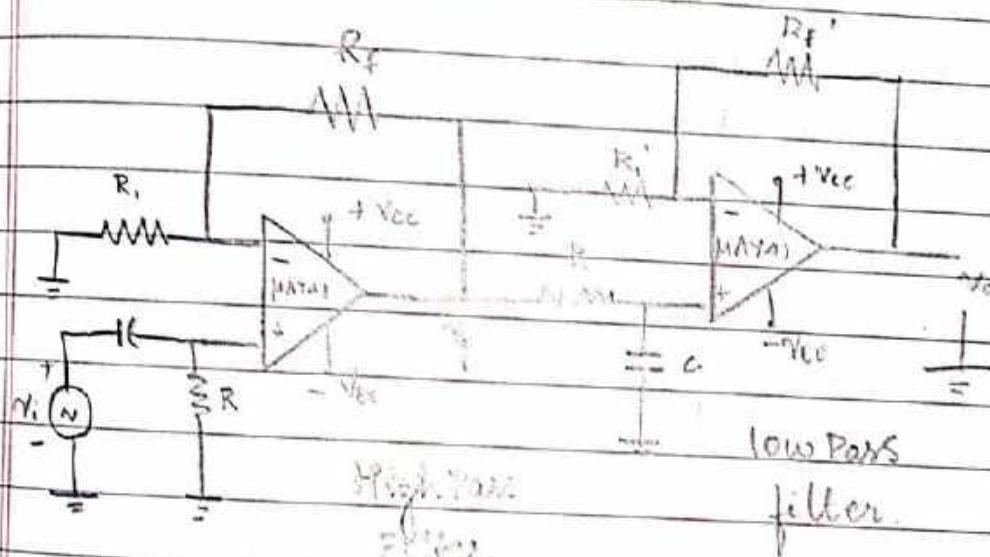
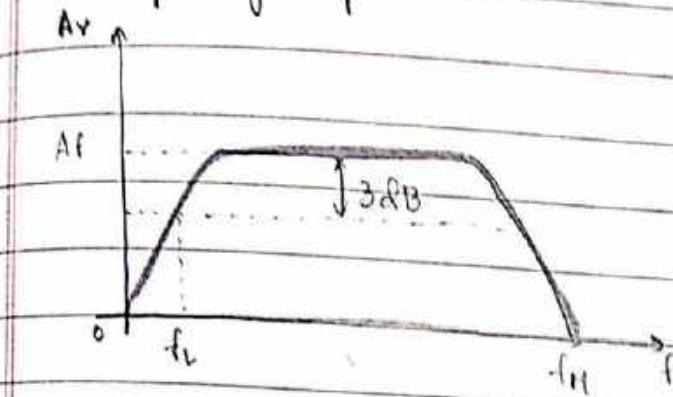
If $Q < 10$: wide band pass filter

If $Q > 10$: narrow band pass filter.

Band pass filter allows all the frequencies in the range from lower cut off frequency f_L to higher cut off frequency f_H . All other frequencies are attenuated.

- Wide Bandpass Filter: (highpass filter + low pass filter)

Frequency response



Gain is given by

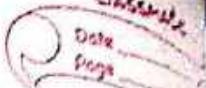
$$A_f = A_1 \cdot A_2$$

$$\text{High pass filter: } A_1 = \frac{A_{f_1}(f/f_c)}{\sqrt{1 + (f/f_c)^2}}$$

$$\text{Low pass filter: } A_2 = \frac{A_{f_2}}{\sqrt{1 + (f/f_H)^2}}$$

$$\therefore A_f = \frac{A_{f_1}(f/f_c)}{\sqrt{1 + (f/f_c)^2}} \cdot \frac{A_{f_2}}{\sqrt{1 + (f/f_H)^2}}$$

Q1: Design a wide band pass filter to have lower and higher cut off frequency of 500Hz and 1.5 kHz respectively and a pass band gain of 4. Also calculate Q-factor of the filter.



sd: Given: $f_L = 500\text{Hz}$ $f_H = 1.5\text{kHz}$

$$A_f = 4$$

To design high pass filter
assuming $C_1 = 0.01\mu\text{F}$.

$$f_L = \frac{1}{2\pi R C}$$

$$\Rightarrow R = \frac{1}{2\pi f_L C_1} = \frac{1}{2\pi (500)(0.01\mu)} = 31.8\text{k}\Omega$$

To design low pass filter

assuming $C_2 = 0.01\mu\text{F}$.

$$f_H = \frac{1}{2\pi R_2 C_2}$$

$$\Rightarrow R = \frac{1}{2\pi f_H C_2} = \frac{1}{2\pi (1.5\text{k})(0.01\mu)} = 10.61\text{k}\Omega$$

$$A_f = 4$$

$$A_1 = A_2 = \sqrt{4} = 2$$

$(\because A_1 A_2 = 4)$

$$Q\text{-factor} = \frac{f_c}{f_H - f_L}$$

$$\alpha = 1 + \frac{RF}{R_1}$$

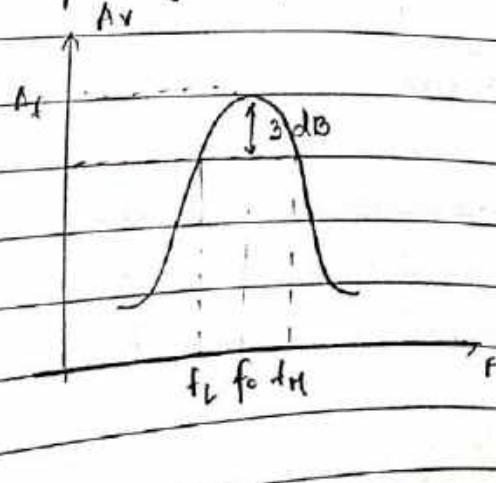
$$Q = \frac{\sqrt{f_L f_H}}{f_H - f_L}$$

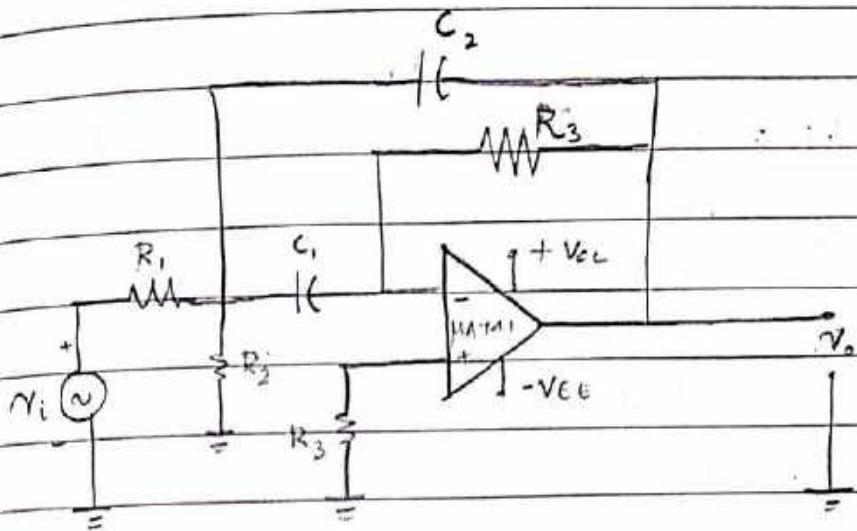
$$\therefore RF = R_1 = 10\text{k}\Omega$$

$$Q = \frac{\sqrt{500(1.5\text{k})}}{1500 - 500} = 0.866$$

* Narrow Band Pass Filter:

Frequency response





Design rule:

Take $C_1 = C_2 = C$ and $C < 1 \mu\text{F}$

calculate all resistors based on the relationship given below:

$$R_1 = \frac{Q}{2\pi f_c C A_f}$$

$$A_f = \frac{R_3}{2R_1}$$

$$R_2 = \frac{Q}{2\pi f_c C (2Q^2 - A_f)}$$

$$A_f < 2Q^2$$

$$R_3 = \frac{Q}{\pi f_c C}$$

If the center frequency changes from f_c to f_c'

$$R_2' = R_2 \left(\frac{f_c}{f_c'} \right)^2$$

- Q1: Design a narrow pass band filter for which $f_c = 1\text{kHz}$, $Q = 3$ and $A_f = 10$. How do you change the centre frequency to 1.2kHz keeping A_f and BW constant.

Given: $f_c = 1\text{kHz}$; $Q = 3$; $A_f = 10$.

$$f_c' = 1.2\text{kHz}$$

$$C_1 = C_2 = C = 0.01\mu\text{F}$$

$$R_1 = \frac{Q}{2\pi f_c C A_f} = \frac{3}{2\pi (1\text{k})(0.01\mu\text{F})(10)}$$

$$R_1 = 4.47\text{k}\Omega$$

$$R_2 = \frac{Q}{2\pi f_c C (2Q^2 - A_f)} = \frac{3}{2\pi (1k) (0.01\mu) (2(9)-10)}$$

$$\underline{R_2 = 5.9k\Omega}$$

$$R_3 = \frac{Q}{\pi f_c C} = \frac{3}{\pi (1k) (0.01\mu)}$$

$$\underline{R_3 = 95.49k\Omega}$$

$$R'_2 = R_2 \left(\frac{f}{f'} \right)^2 = 5.9k \left[\frac{1k}{1.2k} \right]^2$$

$$\underline{R'_2 = 4.14k\Omega}$$

* Band Stop Filter:

It is classified as:

1. Wide band stop filter
2. Narrow band stop filter.

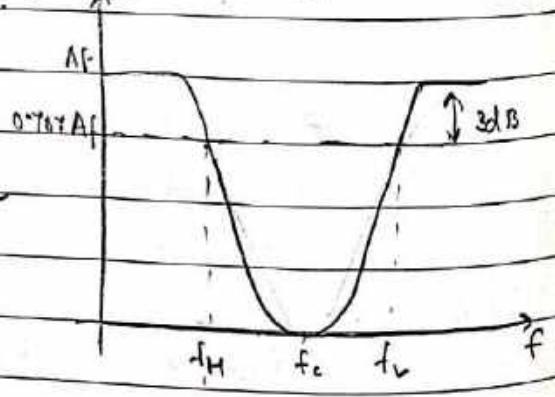
- Wide band stop filter:

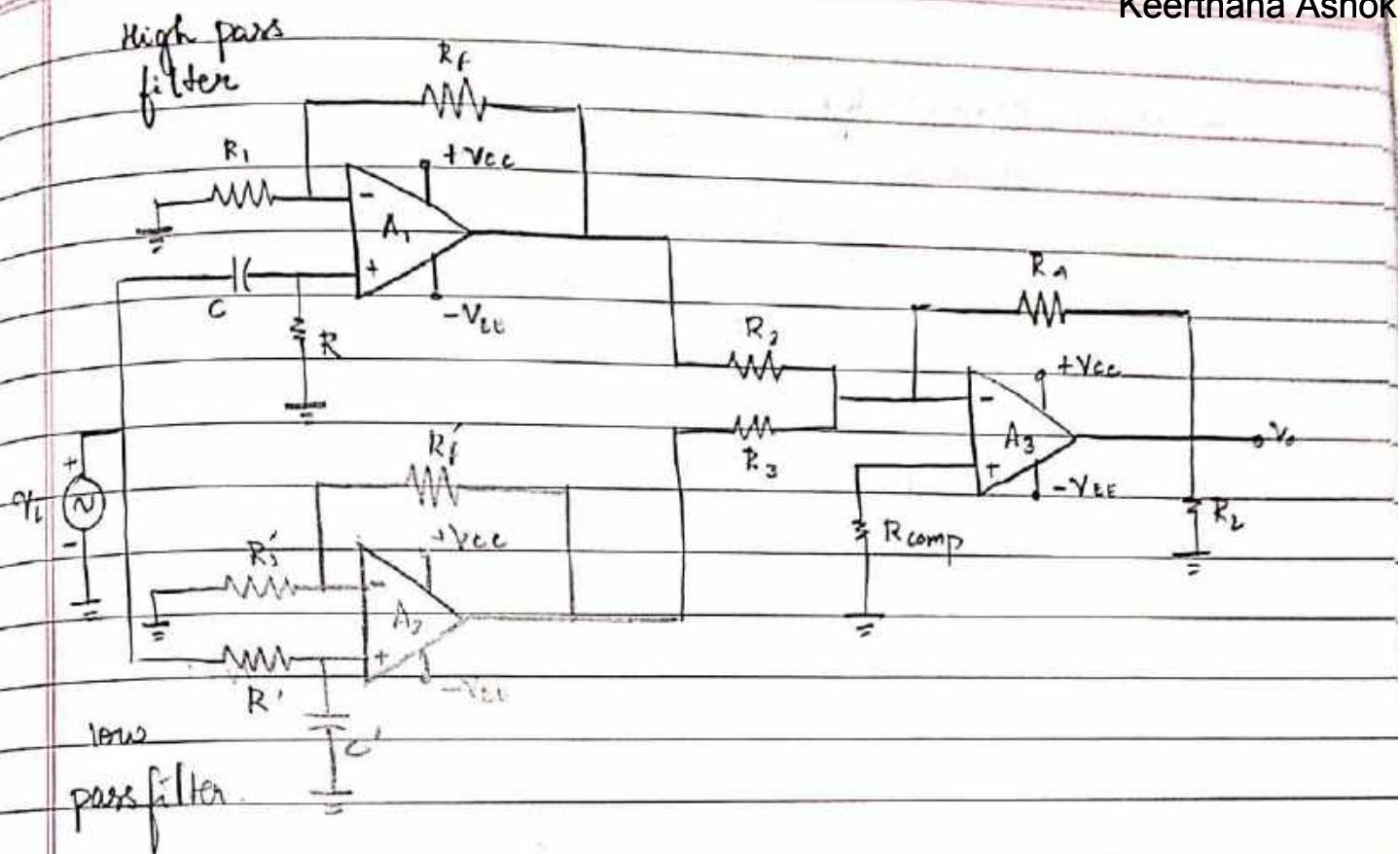
~~(Characteristics: - high pass filter + inverting amplifier)~~

- The lowpass and the high pass filter has equal pass band gain.

This condition has to be satisfied for a wide band stop filter.

- The lower cut off frequency f_L of high pass filter should be greater than higher cut off frequency f_H of lowpass filter.





Q: Design a wide band stop filter to have $f_L = 500\text{Hz}$ and $f_H = 1.5\text{kHz}$.

Given: $f_L = 1.5\text{kHz}$; $f_H = 500\text{Hz}$

Assuming $C = 0.05\mu\text{F}$ and $C' = 0.01\mu\text{F}$

$$f_H = \frac{1}{2\pi f_H C}$$

$$\Rightarrow R = \frac{1}{2\pi f_H C} = \frac{1}{2\pi(500)(0.05\mu)} = 6.36\text{k}\Omega$$

$$f_L = \frac{1}{2\pi R'C'}$$

$$\Rightarrow R' = \frac{1}{2\pi f_L C'} = \frac{1}{2\pi(1.5k)(0.01\mu)} = 10.61\text{k}\Omega$$

$$R'_1 = R_f' = 10\text{k}\Omega$$

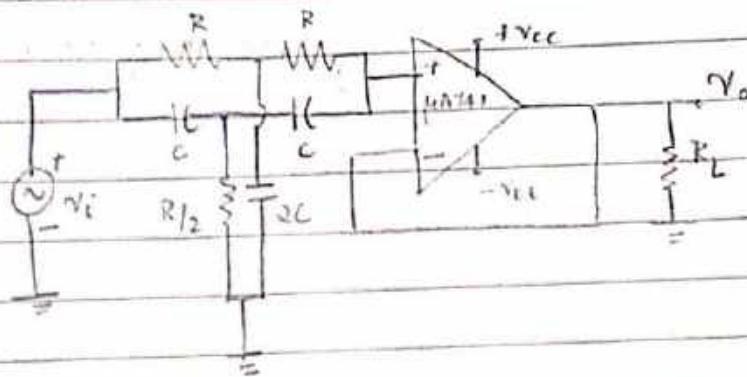
$$R_1 = R_F = 10\text{k}\Omega$$

If the gain of the summing amplifier is assumed as 1
 $R_2 = R_3 = R_4 = 10\text{k}\Omega \Rightarrow R_{comp} = \frac{10k}{3} = 3.33\text{k}\Omega$

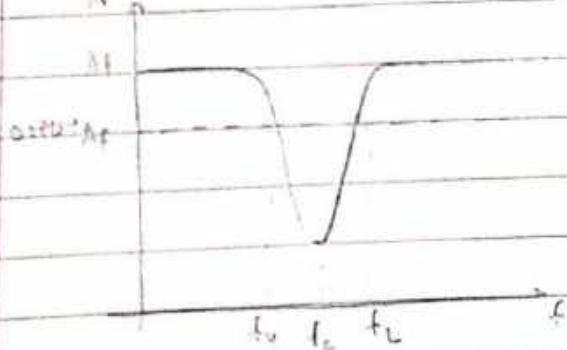
- Narrow Band stop Filter: (Notch filter)

To reject a signal at a particular frequency we used narrow band stop filter.

It is used in a twin-T network



Frequency response



Notch filter frequency

$$f_N = \frac{1}{2\pi RC}$$

Q: Design an active notch filter to eliminate 100 Hz frequency

Sol: $f_N = 100 \text{ Hz}$

Assuming $C = 0.01 \mu\text{F}$

$$f_N = \frac{1}{2\pi RC}$$

$$\rightarrow R = \frac{1}{2\pi f_N C} = \frac{1}{2\pi(100)(0.01\mu\text{F})} = 159.1 \text{ k}\Omega$$

$$R/2 = 79.5 \text{ k}\Omega$$

$$2C = 0.02 \mu\text{F}$$

All Pass Filter:

It alters all the frequencies with certain phase shift.

Let us consider $R_1 = R_f$

Using superposition

R_1 is grounded hence acts as non inverting amplifier.

$$\therefore V_{o1} = \left[1 + \frac{R_f}{R_1} \right] V_A$$

$$V_{o1} = 2 V_A \quad (\because R_f = R_1)$$

R_f is grounded hence acts as inverting amplifier.

$$V_{o2} = -\frac{R_f}{R_1} V_A$$

$$V_{o2} = -V_A \quad (\because R_f = R_1)$$

By Voltage divider rule

$$V_A = \frac{-jX_C}{R - jX_C} V_i$$

$$\text{but } X_C = \frac{1}{2\pi f C}$$

$$V_A = \frac{V_i}{1 + j2\pi f RC}$$

Therefore

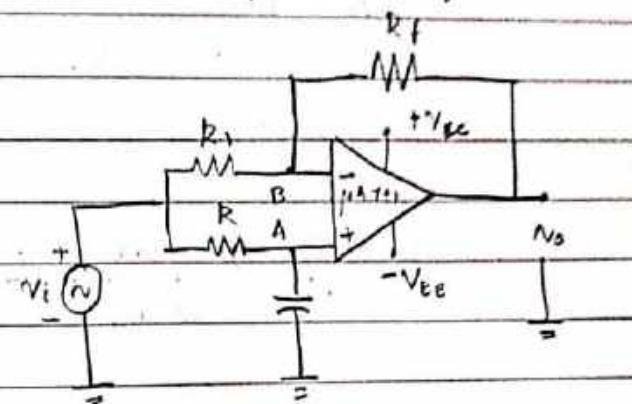
$$V_o = V_{o1} + V_{o2}$$

$$V_o = 2V_A - V_i$$

~~Therefore~~

$$V_o = \frac{2V_i}{1 + j2\pi f RC} - V_i$$

$$V_o = V_i \left[\frac{2}{1 + j2\pi f RC} - 1 \right]$$



$$V_o = V_i \left[\frac{1 - j2\pi f R C}{1 + j2\pi f R C} \right]$$

$$\left| \frac{V_o}{V_i} \right| = \sqrt{\frac{1 + (2\pi f R C)^2}{1 + (2\pi f R C)^2}}$$

$\left \frac{V_o}{V_i} \right $	= 1
----------------------------------	-----

In order to analyse phase shift ϕ , we have :

$$\phi = -2 \tan^{-1}(2\pi f R C)$$

If the phase shift is negative, then the output lags behind the input by an angle ϕ .

If the phase shift is positive, then the output leads the input by an angle ϕ .

Q: Find the phase shift in an all pass filter given a signal frequency $2k$ Hz and $R = 20k\Omega$ and $C = 0.01\mu F$.

Sol: Given: $f = 2k$ Hz

$$R = 20k\Omega$$

$$C = 0.01\mu F$$

$$\phi = -2 \tan^{-1}(2\pi f R C)$$

$$\phi = -2 \tan^{-1}(2\pi(2k)(20k)(0.01\mu))$$

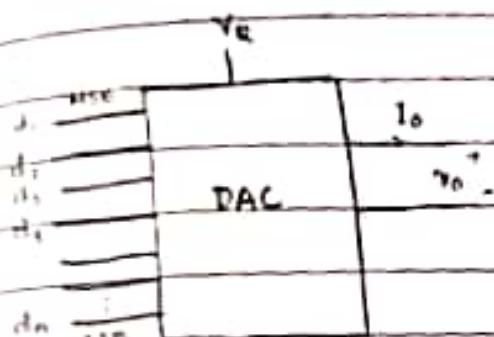
$$\phi = -2 \tan^{-1}(2.5132)$$

$$\phi = -136.6^\circ$$

Data Converters:Digital to Analog Data Converters:

It can be done by:

1. Binary Weighted Resistor
2. R-R Ladder Network.

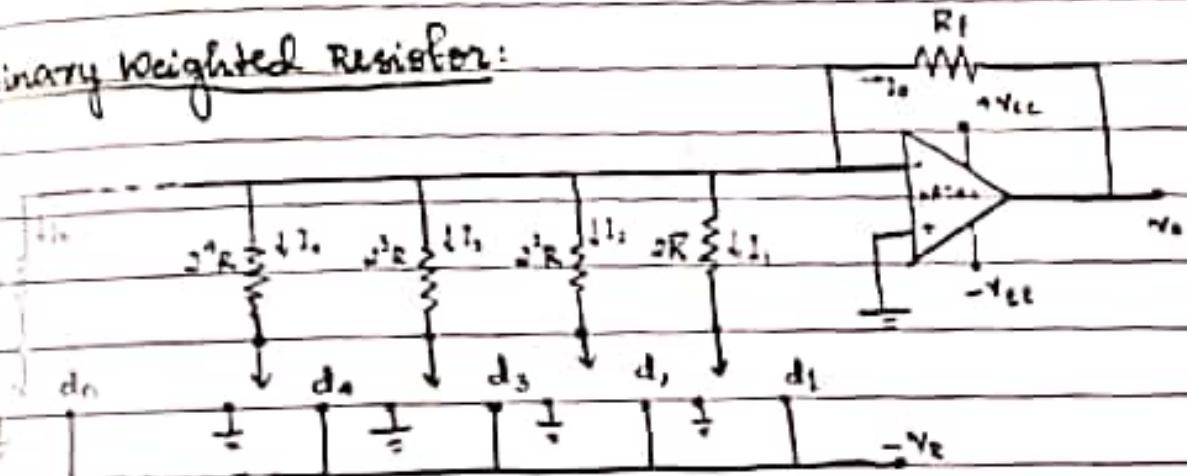


Output voltage

$$V_0 = k V_{FS} (d_3 \cdot 2^3 + d_2 \cdot 2^2 + \dots + d_0 \cdot 2^0)$$

where k : scaling factor = 3

V_{FS} : Full scale output voltage V_{FS} .

Binary Weighted Resistor:

$$I_0 = I_1 + I_2 + I_3 + \dots + I_n$$

$$I_0 = \frac{V_R d_1}{2R} + \frac{V_R d_2}{2^2 R} + \frac{V_R d_3}{2^3 R} + \frac{V_R d_4}{2^4 R} + \dots + \frac{V_R d_n}{2^n R}$$

$$I_0 = \frac{V_R}{R} [2^{-1} d_1 + 2^{-2} d_2 + 2^{-3} d_3 + 2^{-4} d_4 + \dots + 2^{-n} d_n]$$

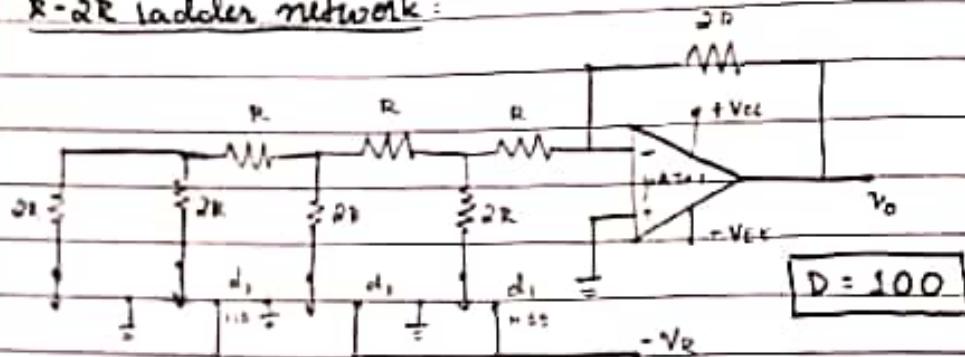
$$\text{but, } V_0 = 2k R_f$$

$$\therefore V_0 = \frac{V_R}{R} [2^{-1} d_1 + 2^{-2} d_2 + 2^{-3} d_3 + \dots + 2^{-n} d_n] R_f$$

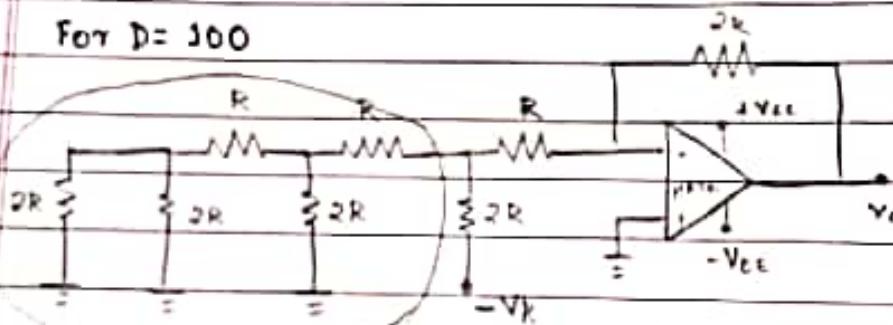
$$\therefore V_0 = V_R [2^{-1} d_1 + 2^{-2} d_2 + 2^{-3} d_3 + \dots + 2^{-n} d_n]$$

But there will be a voltage drop across each resistor
hence to overcome this drawback by R-2R ladder network

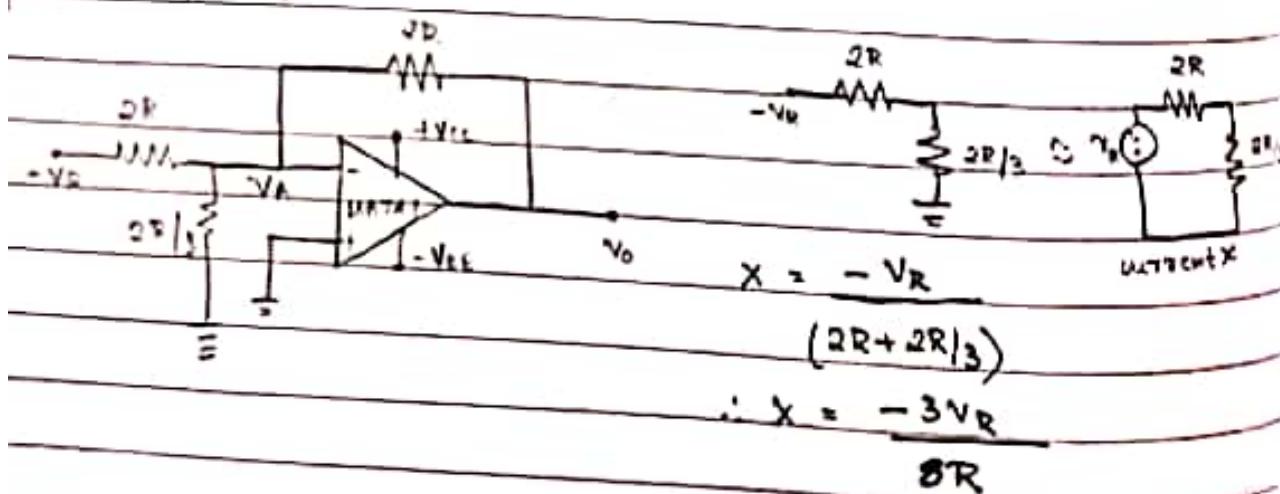
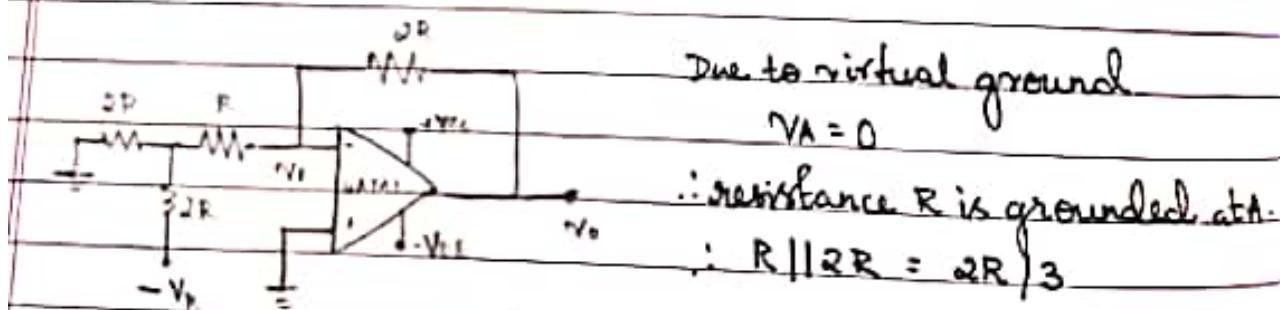
2. R-2R ladder network:



For $D = 100$



Equivalent resistance = $2R$



~~check~~

classmate

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Voltage at node A

$$V_A = IR$$

$$V_A = \frac{X \cdot 2R}{3}$$

$$V_A = -\frac{3V_R}{8R} \left(\frac{2R}{3} \right)$$

$$V_A = -\frac{V_R}{4}$$

For inverting amplifier

$$V_o = -\frac{R_f}{R_i} V_i$$

$$V_o = -\frac{2R}{R} \left[-\frac{V_R}{4} \right]$$

$$\gamma_o = \frac{V_R}{2} //$$

- Performance Parameters:

1. Resolution: least value that can be converted.

$$\text{Resolution} = \frac{V_{\text{FS}}}{2^n - 1}$$

V_{FS} : Full scale output voltage
 n - number of bits.

2. Accuracy: closeness of the value.

within $\pm 0.5\%$ the system is said to accurate.

3. Stability: The stability can be determined by the following parameters

- change in temperature.

- change in power supply.

- long usage.

4. Conversion time: Time taken to convert from digital to analog.

lower the conversion time greater the performance.

5. Settling time: Time taken to set to analog.

6. Monotonicity:

Q1: An 8-bit DAC has an output voltage range of 0 to 10.2V. Find its resolution as per both defnition.

Sol: method 1

$$2^n = 2^8 = 256 \quad n=8 : 8\text{-bit DAC.}$$

method 2

$$\text{resolution} = \frac{V_{\text{FS}}}{2^n - 1} = \frac{10.2}{2^8 - 1} = \frac{10.2}{255} = 40\text{mV/LSB}$$

Q2: A 4-bit DAC has a resolution of 10mV/LSB, find V_{FS} and V_o for an input $(1011)_2$.

Sol: $n = 4$

$$\text{resolution} = 10\text{mV/LSB}$$

$$\text{input} = (1011)_2$$

$$\text{resolution} = \frac{V_{\text{FS}}}{2^n - 1}$$

$$10\text{m} = \frac{V_{\text{FS}}}{2^4 - 1}$$

$$\underline{\underline{V_{\text{FS}} = 150\text{mV}}}$$

$$V_o = V_{\text{FS}}(d_12^{-1} + d_22^{-2} + d_32^{-3} + d_42^{-4})$$

$$V_o = 150\text{m} \left[1\left(\frac{1}{2}\right) + 0\left(\frac{1}{2}\right)^2 + 1\left(\frac{1}{2}\right)^3 + 1\left(\frac{1}{2}\right)^4 \right]$$

$$\underline{\underline{V_o = 150\text{m} [0.687]}}$$

$$\underline{\underline{V_o = 0.103\text{V}}}$$

$$\text{or: } V_o = \text{Resolution} \times (\text{input})$$

Q3: Suggest a suitable value of resistor and reference for a 4-bit R-2R ladder type DAC. If the resolution required is 0.5V.

sol: $n = 4$ resolution = $0.5V$

let us assume

$$V_R = 10V$$

$$\text{resolution} = \left[\frac{1}{2^n} \times \frac{V_R}{R} \right] R_f \quad (R-2R \text{ ladder network})$$

$$0.5 = \left[\frac{1}{2^4} \times \frac{10}{R} \right] R_f \quad \text{let us assume } R_f = 10k\Omega.$$

then $R = 12.5k\Omega$

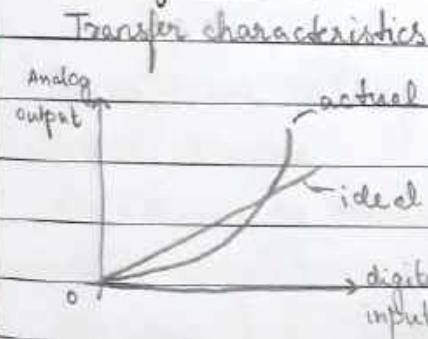
$$\frac{R}{R_f} = 1.25$$

let us assume $R_f = 20k\Omega$

then $R = 25k\Omega$

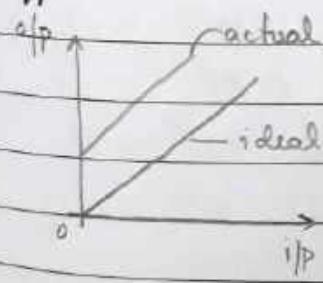
- Types of Errors:

1. Linearity Error:



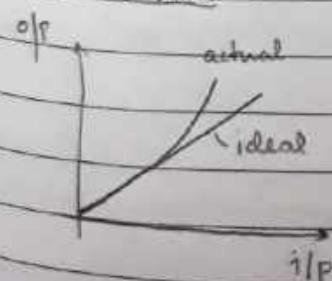
In the transfer characteristics a linear graph is expected but practically it is not perfectly linear. This is called linearity error as output is not linear to input.

2. Offset Error:



Ideally the output is zero when the input is zero. But practically even at zero input, there will be a small output.

3. Gain Error:



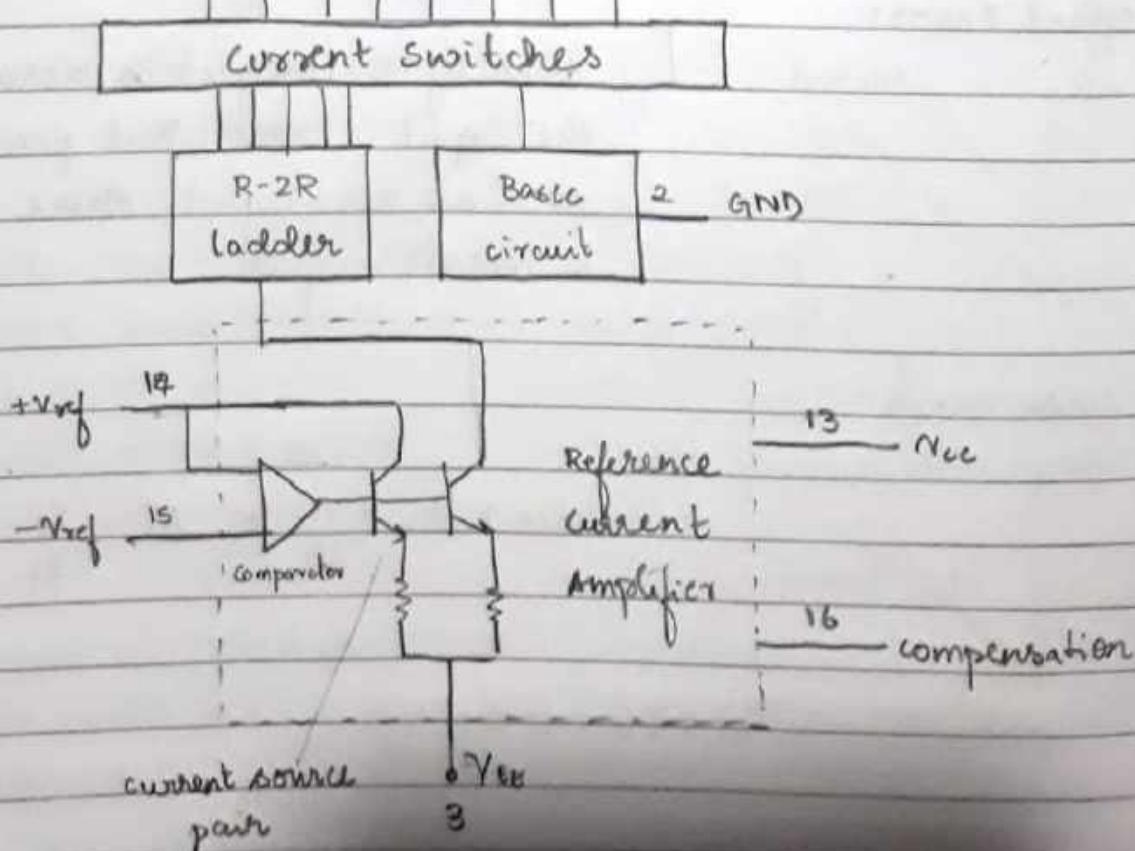
$$\text{Gain} = A_v = \frac{V_o}{V_i} \text{ or } A_i = \frac{I_o}{I_i}$$

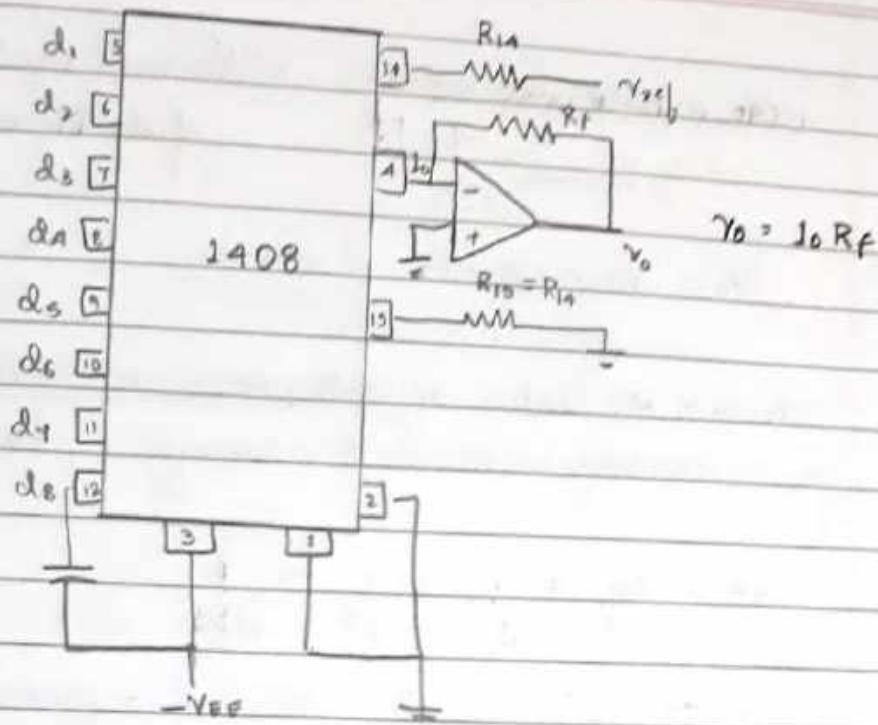
* Monolithic DAC:

1408 : 8 bit monolithic DAC: Inbuilt R-2R ladder, switches and resistors within a single IC.
 settling time : 300nsec .
 reference current of 2mA .
 $V_{cc} = +5\text{V}$ and $-V_{ee} = -5\text{V}$

output range control	1	comparator
GND	2	$-V_{ref}$
V_{dd}	3	$+V_{ref}$
current output	4	1408
d_1	5	I_C
d_2	6	d_2
d_3	7	d_4
d_4	8	d_5

(MSB) $d_1 d_2 d_3 d_4 d_5 d_6 d_7 d_8$ (LSB)





The reference voltage and R_{14} determines the total reference current source.

$R_{15} = R_{14}$, to match the input impedance of a reference current amplifier.

The circuit at pin 4 is used to convert current to voltage current output:

$$I_0 = \frac{V_{ref}}{R_{14}} \left[\frac{d_1}{2^1} + \frac{d_2}{2^2} + \frac{d_3}{2^3} + \frac{d_4}{2^4} + \frac{d_5}{2^5} + \frac{d_6}{2^6} + \frac{d_7}{2^7} + \frac{d_8}{2^8} \right]$$

$$I_0 = \frac{V_{ref}}{R_{14}} \sum_{i=1}^8 d_i 2^{-i} \quad \text{where } d_i \text{ is 0 or 1.}$$

The basic step of 8 bit DAC is 10.2mV, if 00000000 represents zero volts (0V), find the output when the input is 10101011

$$\text{input} = 10101011$$

$$= 1 \times 2^7 + 0 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$$

$$= (171)_{10}$$

$$n = 8$$

output voltage = 10.2mV for least significant bit (LSB).

$V_o = \text{basic step voltage} \times \text{decimal equivalent of the binary input}$

$$V_o = 10.2m \times 171 = \underline{\underline{174V}}$$

Q2: calculate the value of LSB, MSB and full scale output for 8 bit DAC with 0-5V range.

sol: $\text{LSB} = \frac{d_n}{2^n} = \frac{1}{2^n} = \frac{1}{2^8} = \frac{1}{256}$

For 5V range: $\text{LSB} = \frac{1}{256} \times 5 = 19.53mV$

$$\text{MSB} = \frac{d_1}{2^1} = \frac{1}{2}$$

For 5V range: $\text{MSB} = \frac{1}{2} \times 5 = 2.5V$

Full scale output = Full scale voltage - LSB for given range

$$V_{oFS} = 5 - 19.53mV$$

$$V_{oFS} = \underline{\underline{4.9805V}}$$

Q3: If $V_{cc} = 5V$, $V_{EE} = -5V$, $V_{ref} = 5V$, $R_{14} = 2.5k\Omega$
Find I_o and V_o .

sol: $I_o = \frac{V_{ref}}{R_{14}} \left[\sum_{i=1}^8 d_i 2^{-i} \right]$

$$I_o = \frac{5}{2.5k} \left[\sum_{i=1}^8 1 \times 2^{-i} \right]$$

$$I_o = 2m \left[\frac{\frac{1}{2} - \frac{1}{2^9}}{1 - \frac{1}{2}} \right] = 2m [0.996]$$

$$I_o = \underline{\underline{1.992mA}}$$

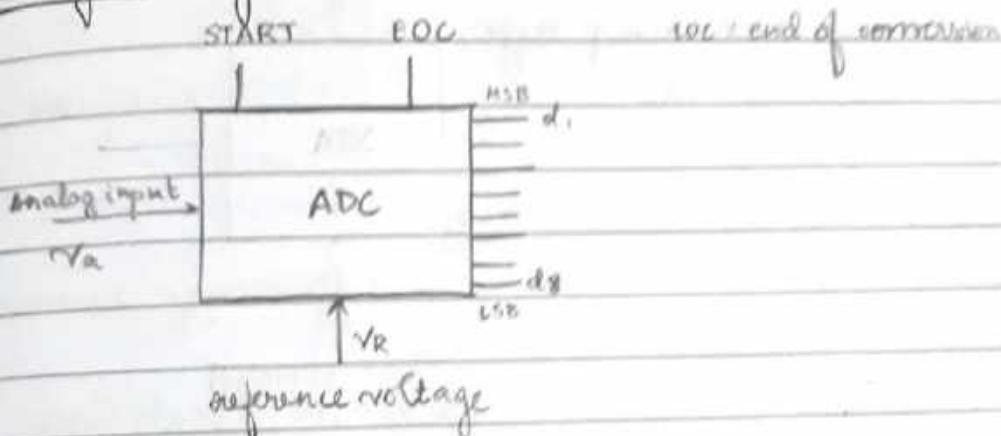
$$V_o = I_o R_f$$

Assuming $R_f = 5k\Omega$

$$V_o = 1.992mV (5k)$$

$$\underline{\underline{V_o = 9.96V}}$$

Analog to Digital Data Converters:



Performance Parameters:

1. Resolution: 2^n

$$\text{resolution} = \frac{V_{REF}}{2^n - 1}$$

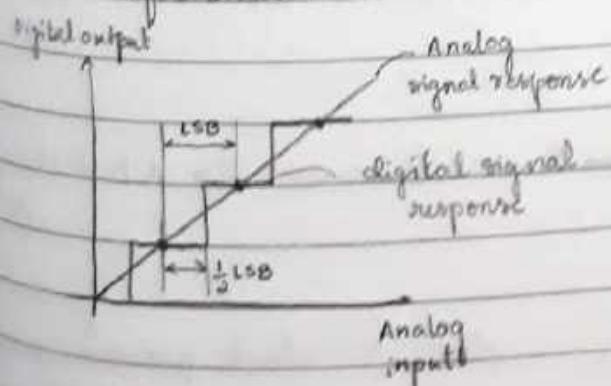
2. Stability: It can be determined by

- change in temperature
- change in power supply
- long usage.

Conversion time: Time taken to convert from analog to digital.

Quantisation Error:

Transfer characteristics



The error must be less than
 $\pm \frac{1}{2} LSB$ to be neglected.

* Classification of ADC:

Direct type: Direct conversion: comparison with basic signal.

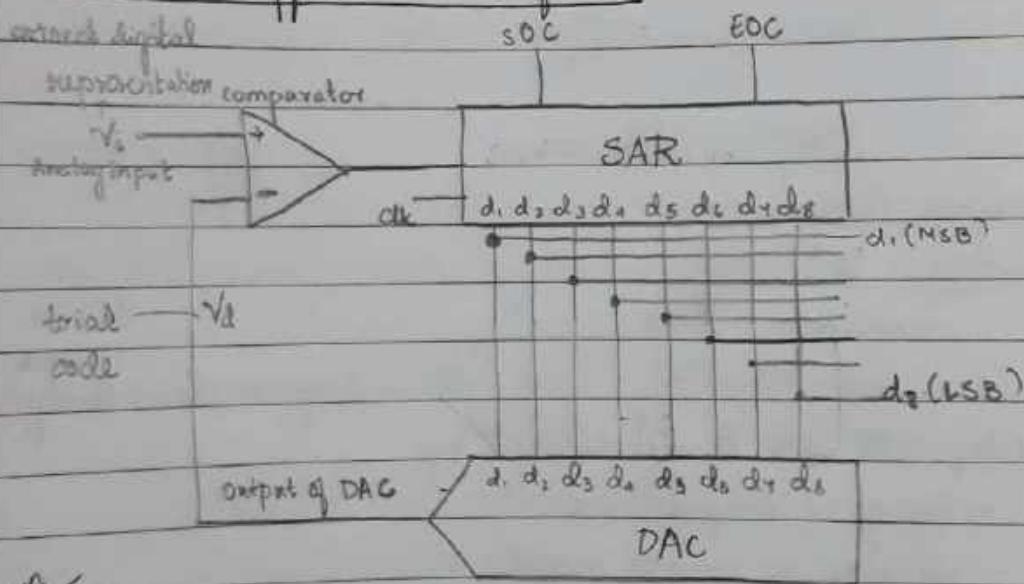
- Flash converter
- Sigma converter

- Successive Approximation of ADC

Indirect type: Indirect conversion: Analog \rightarrow frequency/time \rightarrow digital

- Charge balancing type.
- Dual slope DAC.

* Successive Approximation of ADC:



~~Operation:~~ Trial code: $V_d : 1000000$ (initially)

CASE 1: If $V_i > V_d$

Let $V_i = 10110010$

then MSB bit is retained as 1 and the next bit is set to 1.

CASE 2: If $V_i < V_d$

Let $V_i = 00110010$

then MSB bit is 0 and the next msb is set to 1 and checked further

conversion time

$$T_c = T(n+1)$$

where T : clock period

n : number of bits

Date _____
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An 8-bit successive approximation ADC is driven by 1 MHz clock, then what is the conversion time.

$$\underline{\text{Sol:}} \quad T = \frac{1}{f} = \frac{1}{1 \times 10^6} = 10^{-6} = \underline{1 \mu\text{sec}}$$

conversion time

$$T_c = T(n+1)$$

$$T_c = 1 \mu(8+1)$$

$$\underline{T_c = 9 \mu\text{sec}}$$

successive approximation of DAC

Ex:

Initial state : $\gamma_d = 10000000$

comparator output

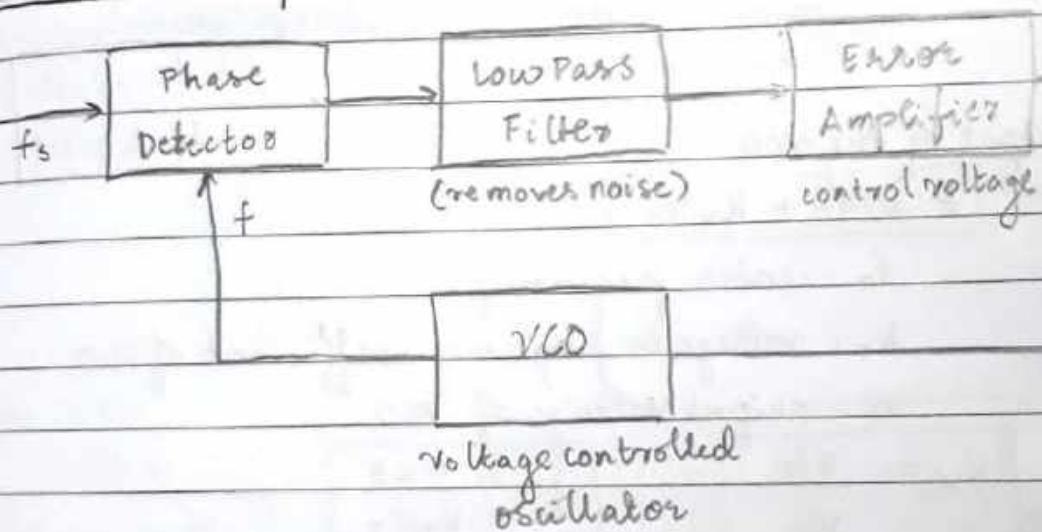
1100 0000	0
1010 0000	1
1011 0000	1
1011 1000	0
1011 0100	0
1011 0010	1
1011 0010	0

UNIT - 05

Additional Linear IC Circuits

Phase Locked Loop:

IC 563 PLL



When we consider control voltage then the output is f for an input f_s and when control voltage is zero then the output is f_0 .

f_0 : center frequency

f_c : capture frequency

f_L : lock frequency.

Capture range: There is variation in the output similar to the variation occurring in input. in this frequency range.

lock range: Here $f_s \approx f$.

lock range is greater than capture range.

Application

- frequency multiplier

- frequency synthesizer

- AM detector

- FM detector.

Widely used in communication application.

Pin configuration of VCO.

GND	3	NE/SE 566	8 + V _{cc}
NC	2	VCO	7 C _T : Timing capacitor
square wave output	3		6 R _T : External resistance
Triangular wave output	4		5 Modulation

Output of the VCO

$$f = f_0 + k_v V_c$$

f_0 : center frequency

k_v : voltage to frequency coefficient of VCO

V_c : output voltage of VCO.

$$k_v = \frac{8f_0}{V_{cc}}$$

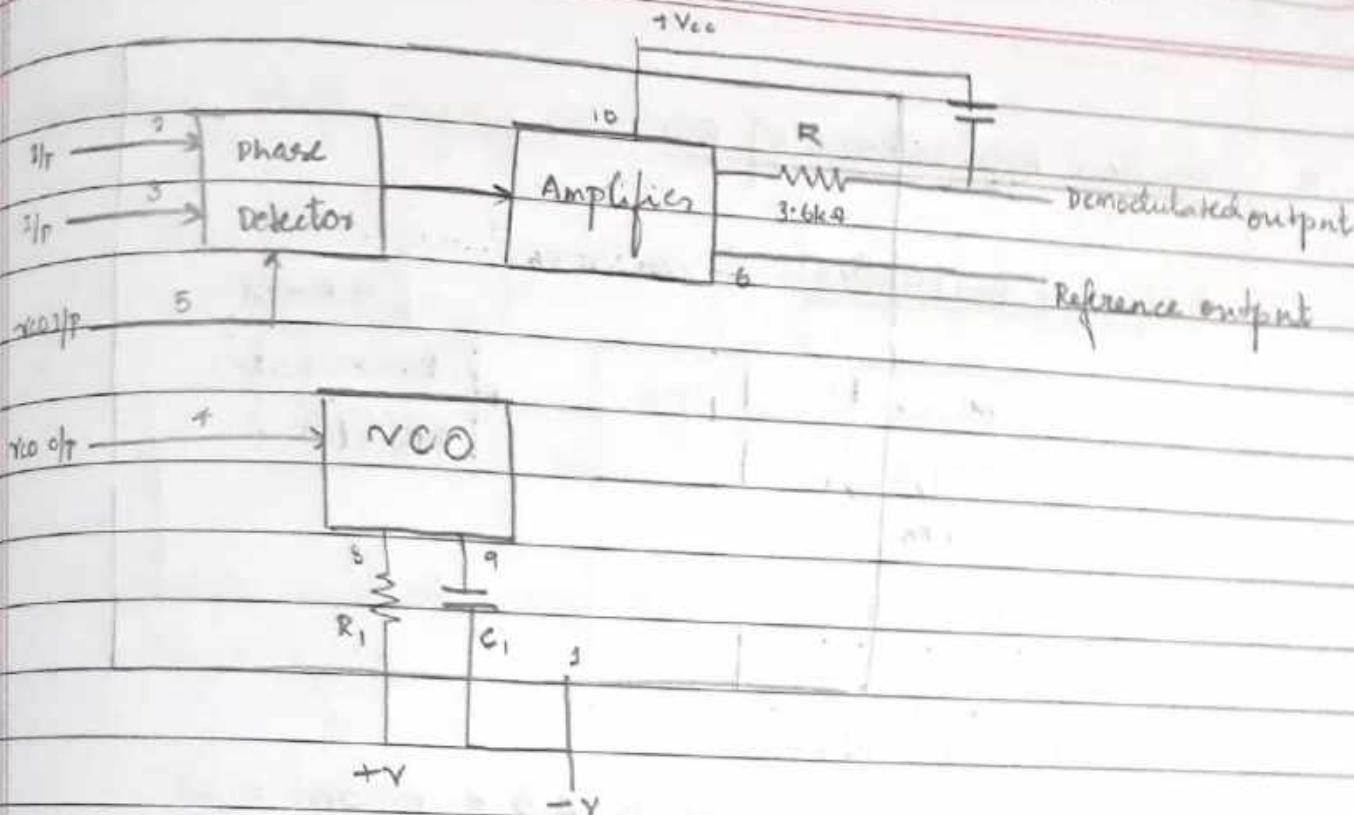
$$f_0 = \frac{0.25}{R_T C_T}$$

Pin configuration of PLL

-V _{cc}	1		Pin 8 and 9
S/P	2	J6365PLL	should be connected to phase detector.
S/P	3	NE/SE	
VCO O/P	4	565	
VCO IIP	5		
reference output	6		Timing capacitor
VCO control voltage	7		Timing resistor

$$k_v = \frac{\Delta f_0}{\Delta V_c}$$

$$f_0 = \frac{1.2}{4 R_1 C_1}$$



$$f_0 = \frac{1.2}{4R_1C_1}$$

$$f_L = \pm \frac{8f_0}{v'}$$

$$v' = +V - (-V)$$

$$f_L = \pm \sqrt{\frac{f_L}{2\pi RC_2}}$$

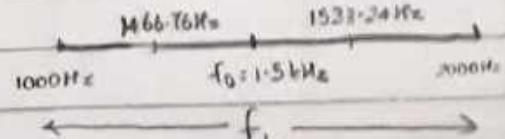
If $R_1 = 20\text{k}\Omega$ and $C_1 = 0.01\mu\text{F}$, $+V = 12\text{V}$, $-V = -12\text{V}$ and $C_2 = 20\mu\text{F}$. Find f_0 , f_L and f_C .

$$f_0 = \frac{1.2}{4R_1C_1} = \frac{1.2}{4(20k)(0.01\mu)} = 1.5\text{kHz}$$

$$f_L = \pm \frac{8f_0}{v'} \quad v' = +V - (-V)$$

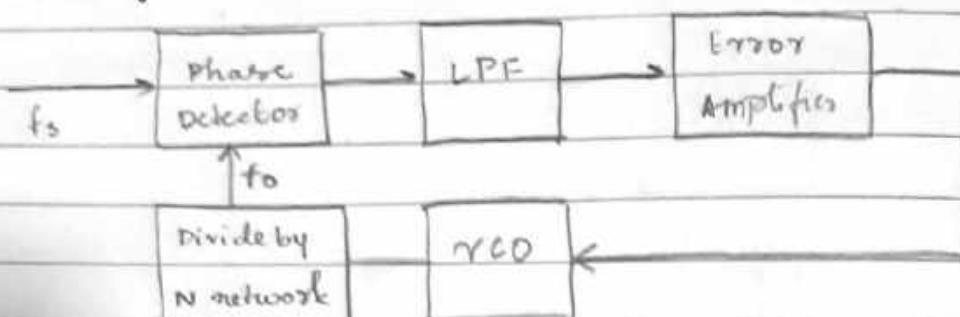
$$f_L = \pm \frac{8(1.5k)}{24} = \pm 0.5\text{kHz}$$

$$f_C = \pm \sqrt{\frac{f_L}{2\pi RC_2}} = \pm \sqrt{\frac{500}{2\pi(3.6k)(20\mu)}} = \pm 33.24\text{Hz}$$



* Practical applications of PLL:

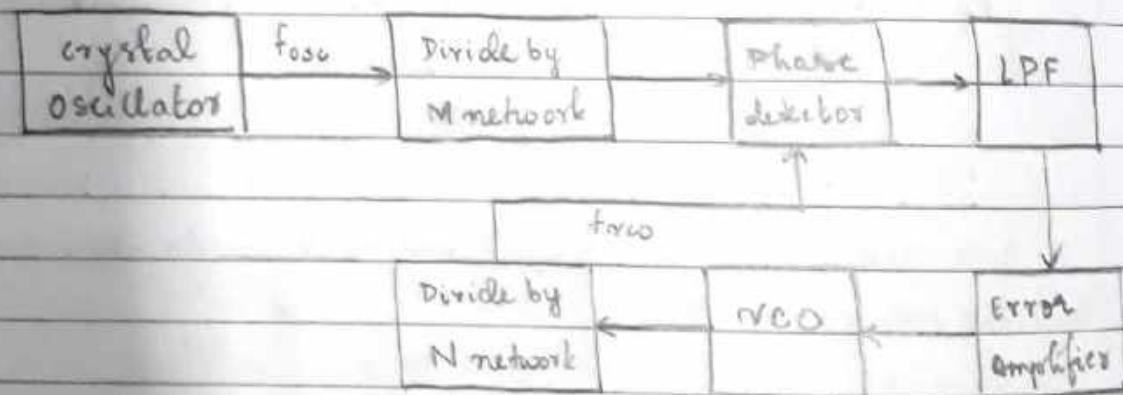
1. Frequency multiplier:



$$\text{Output: } f = Nf_s$$

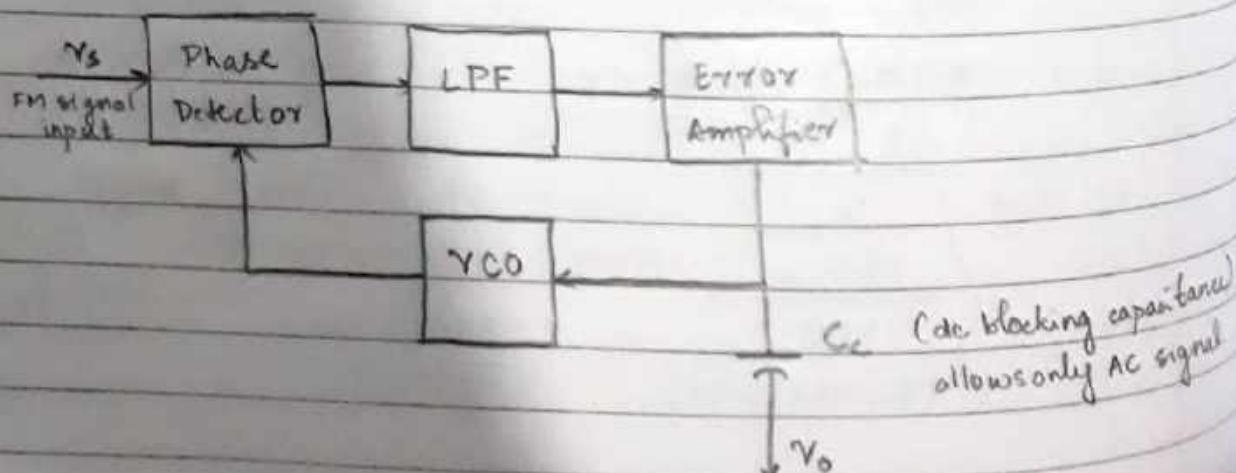
where $N = 4, 6, 8, 10, 20, \dots$

2. Frequency Synthesizer:



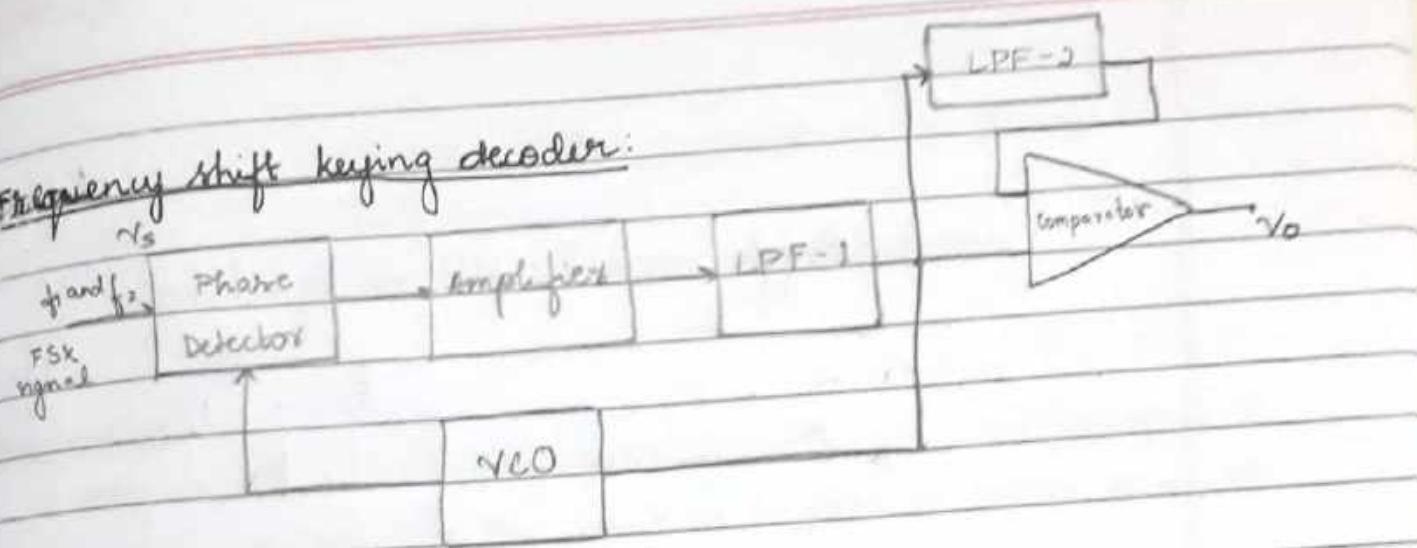
$$f_{vco} = \left(\frac{N}{M} \right) f_{osc}$$

3. FM detector: (demodulation)



C_c (ac blocking capacitor)
allows only AC signal

4. Frequency shift keying decoder:



$$V_{c_1} = V_{CO_1} \text{ and } V_{c_2} = V_{CO_2}$$

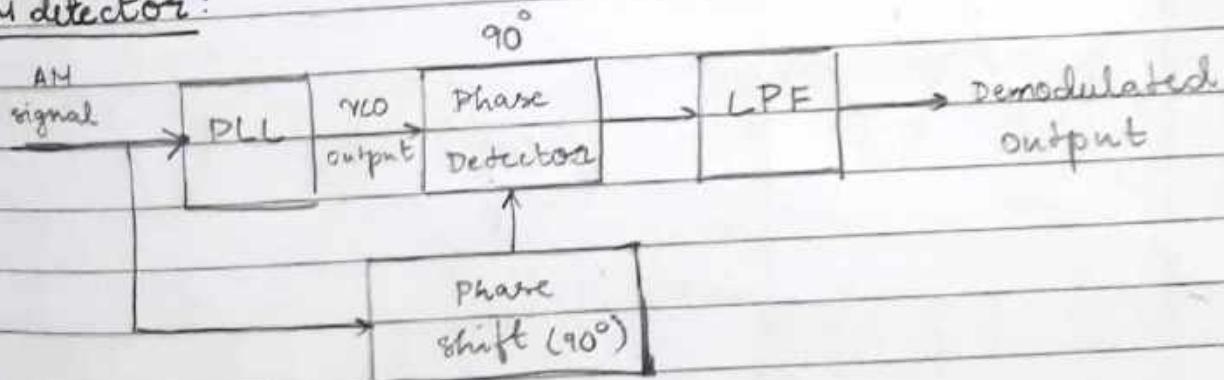
$$V_{c_1} = \frac{f_1 - f_0}{k_v}$$

k_v - voltage to frequency coefficient

$$V_{c_2} = \frac{f_2 - f_0}{k_v}$$

$$\Delta V_{CO} = \frac{f_2 - f_0}{k_v} - \frac{f_1 - f_0}{k_v} = \frac{f_2 - f_1}{k_v}$$

5. AM detector:



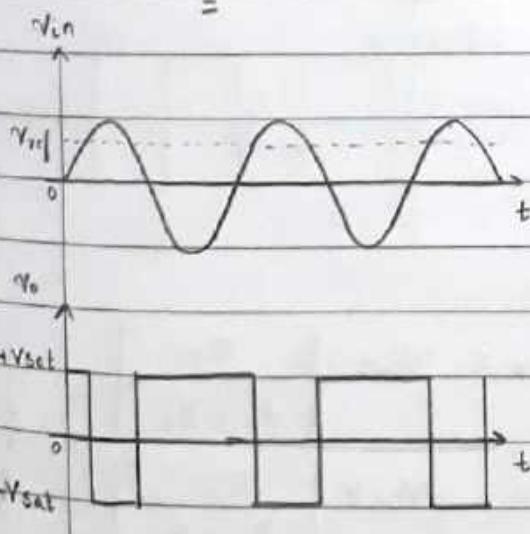
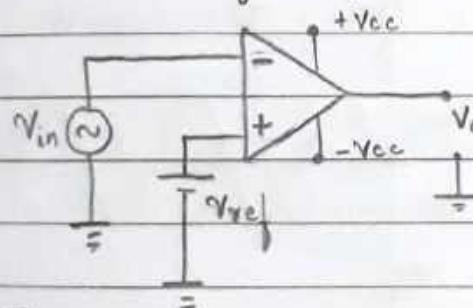
UNIT - 04

Op-Amp in Non-linear Applications

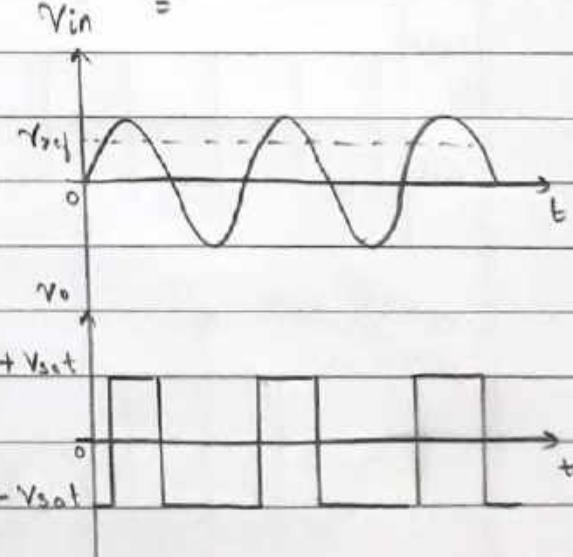
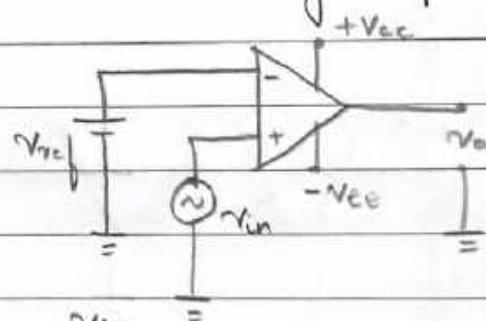
* comparator:

A comparator circuit compares two voltages and output is either 1 or 0 to indicate the input is higher or lower than the reference voltage respectively.

1. Inverting comparator



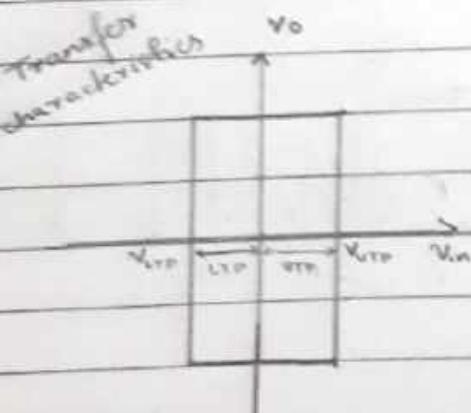
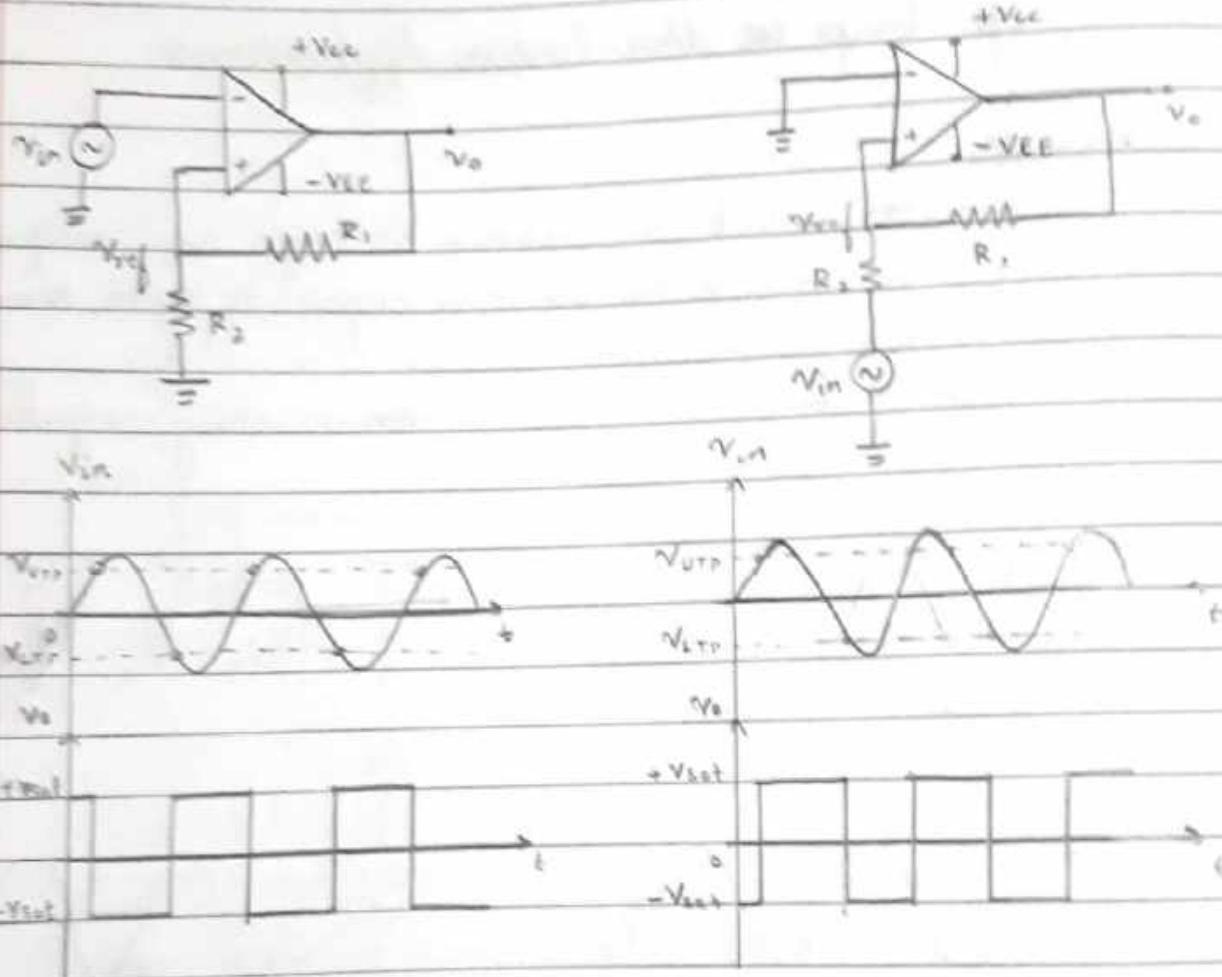
2. Non inverting comparator.

* Schmidt trigger:

It is an active circuit which converts an analog input signal to a digital output signal. The output retains its value until the input changes sufficiently to trigger a change.

1. Inverting Schmitt trigger

2. Non-inverting Schmitt trigger



$$\text{Inverting} \quad V_{UTP} = V_{sat} \left[\frac{R_2}{R_1 + R_2} \right]$$

$$V_{LTP} = -V_{sat} \left[\frac{R_2}{R_1 + R_2} \right]$$

$$H = V_{UTP} - V_{LTD}$$

$$H = \frac{V_{sat} R_2}{R_1 + R_2} - \left(-\frac{V_{sat} R_2}{R_1 + R_2} \right)$$

For inverting schmitt trigger

$$V_i < V_{LTP} : V_o = +V_{sat} \quad \therefore H = \frac{2V_{sat} R_2}{R_1 + R_2}$$

$$V_i > V_{UTP} : V_o = -V_{sat}$$

$$\text{For non-inverting schmitt trigger} \quad V_{UTP} = I_{in} R_2 = \frac{V_{sat} R_2}{R_1}; \quad V_{LTP} = I_{in} R_2 = \frac{-V_{sat} R_2}{R_1}$$

$$V_i < V_{LTP} : V_o = -V_{sat}$$

$$V_i > V_{UTP} : V_o = +V_{sat} \quad \therefore H = V_{UTP} - V_{LTP} = \frac{V_{sat} R_2 - (-V_{sat} R_2)}{R_1} = \frac{2V_{sat} R_2}{R_1}$$

i. Design an inverting Schmidt trigger to have trigger voltage of $\pm 4V$. Use an op-amp μA741 with supply voltage of $\pm 15V$.

Designing:

To calculate R_1 and R_2

$$R_2 = \frac{\text{trigger voltage}}{I_2}$$

$$R_1 = \frac{V_o - \text{trigger voltage}}{I_2}$$

Assuming I_2 value should be in μA if not given.

Given:

$$V_{UTP} = 4V \quad V_{LTP} = -4V$$

$$\text{Supply} = \pm 15V$$

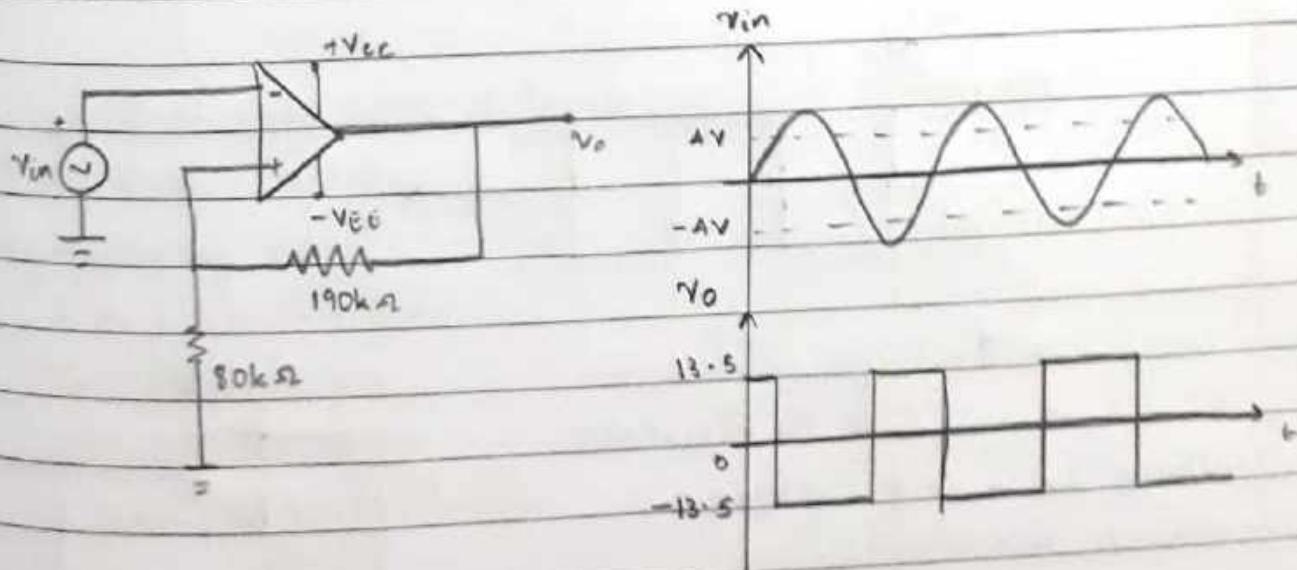
$$V_{sat} = \text{Supply voltage} - 1.5$$

$$\therefore V_{sat} = \pm 13.5V$$

Assuming $I_2 = 50\mu A$

$$R_2 = \frac{4}{50\mu} = \underline{\underline{80k\Omega}}$$

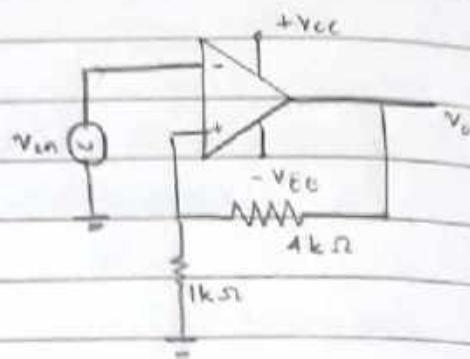
$$R_1 = \frac{13.5 - 4}{50\mu} = \frac{9.5}{50\mu} = \underline{\underline{190k\Omega}}$$



Q2: The opamp comparator circuit is shown in the figure.

Assume $\pm V_{cc} = 12V$ and $V_{sat} = 0.9V_{cc}$.

If a sine wave of 10V is applied calculate the threshold levels of and plot the input and output waveforms.



$$\underline{\text{sol:}} \quad R_1 = 4k\Omega \quad R_2 = 1k\Omega$$

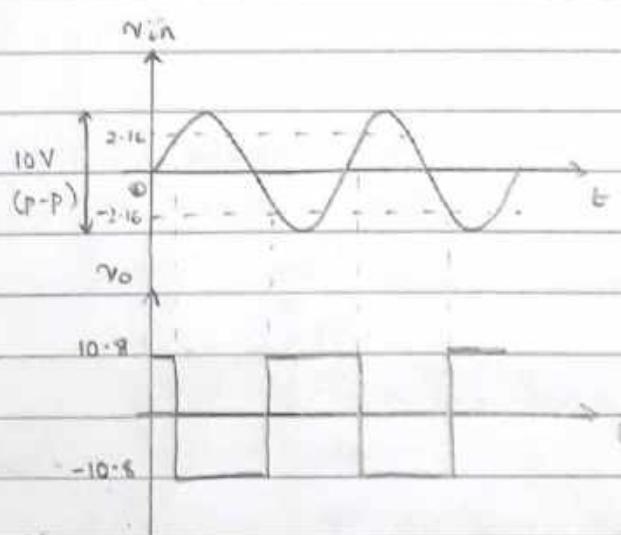
$$\pm V_{cc} = 12V$$

$$V_{sat} = 0.9V_{cc} = 0.9(12)$$

$$\pm V_{sat} = \pm 10.8V$$

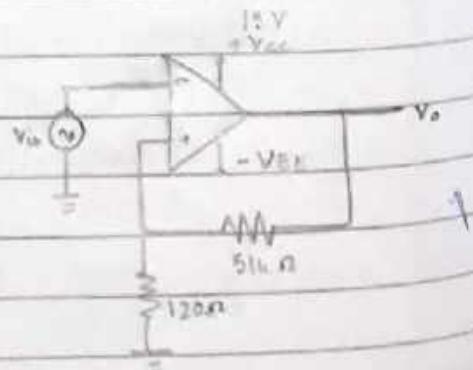
$$V_{UTP} = \frac{V_{sat} R_2}{R_1 + R_2} = 10.8 \left(\frac{2k}{4k+1k} \right) = \underline{2.16V}$$

$$V_{LTP} = -V_{sat} \frac{R_2}{R_1 + R_2} = -10.8 \left(\frac{1k}{4k+1k} \right) = \underline{-2.16V}$$



Q3: For schmitt trigger shown in the figure calculate the threshold voltage levels and hysteresis.

Assume $V_{sat} = 0.9V_{cc}$.

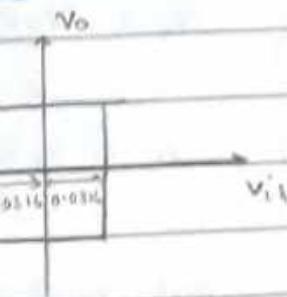


$$\begin{aligned} V_{sat} &= 0.9V_{cc} \\ V_{sat} &= 0.9(15) \\ \underline{V_{sat}} &= 13.5V \end{aligned}$$

$$\begin{aligned} V_{UTP} &= \frac{V_{sat}R_2}{R_1 + R_2} = \frac{13.5(120)}{51k + 120} = 0.0316V \\ V_{LTP} &= -V_{UTP} = -0.0316V \end{aligned}$$

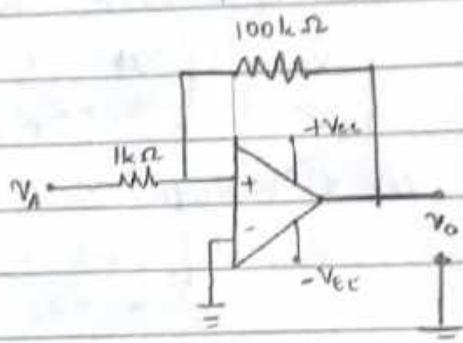
$$H = V_{UTP} - V_{LTP}$$

$$H = 0.0632 = \underline{63.2mV}$$



Q: For a non inverting regenerative comparator shown in the figure calculate tripping voltage.

$$\text{Assume } \pm V_{sat} = \pm 13.5V$$



$$\underline{R_1 = 100k\Omega \quad R_2 = 1k\Omega}$$

$$V_{UTP} = \frac{V_{sat}R_2}{R_1} = \frac{13.5(1k)}{(100k)} = 0.135V$$

$$V_{LTP} = \frac{-V_{sat}R_2}{R_1} = -0.135V$$

$$\therefore H = V_{UTP} - V_{LTP} = 2(0.135) = \underline{0.27V}$$

Q: Schmitt trigger with different UTP and LTP levels:

$$\text{Here } R_{comp} = R_1 // R_2$$

By applying KVL

$$I_1 R_1 + I_2 R_2 + X = V_o$$

$$V_o = I_1 R_1 + I_2 R_2 + X$$

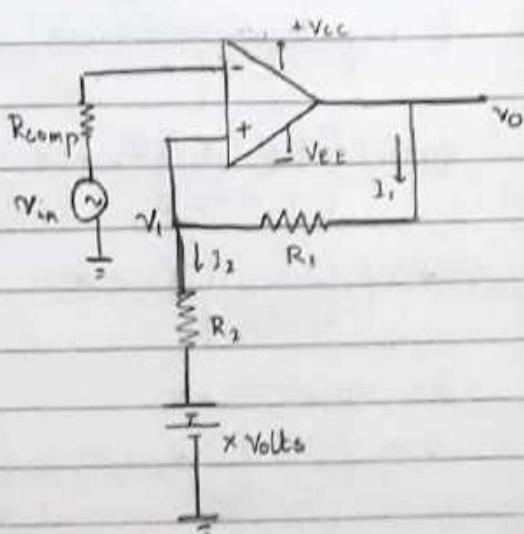
$$I_1(R_1 + R_2) = V_o - X$$

$$I_1 = \frac{V_o - X}{R_1 + R_2} \quad \textcircled{1}$$

By applying KVL

$$V_i - I_2 R_2 - X = 0$$

$$V_i = I_2 R_2 + X \quad \textcircled{2}$$



Substituting eq ① in eq ②

$$V_1 = \left(\frac{V_o - x}{R_1 + R_2} \right) R_2 + x$$

$$V_1 = \frac{V_o R_2 - x R_2 + x R_1 + x R_2}{R_1 + R_2}$$

$$V_1 = \frac{V_o R_2 + x R_1}{R_1 + R_2}$$

Let $V_1 = V_{UTP}$ and $V_o = V_{sat}$

$$V_{UTP} = \left(\frac{V_{sat} - x}{R_1 + R_2} \right) R_2 + x$$

Let $V_1 = V_{LTP}$ and $V_o = -V_{sat}$

$$V_{LTP} = \left(\frac{-V_{sat} - x}{R_1 + R_2} \right) R_2 + x$$

$$\therefore H = V_{UTP} - V_{LTP}$$

$$H = \frac{(V_{sat} - x) R_2 + x - (-V_{sat} - x) R_2 - x}{R_1 + R_2}$$

$H = \frac{2V_{sat} R_2}{R_1 + R_2}$

Q1: Design an opamp schmitt trigger for the following specifications

$\rightarrow UTP = 2V$ and $LTP = -4V$

\rightarrow the output swings between $\pm 10V$.

If input is 5sinwt, plot the waveforms of input and output.

sol:

$$V_{UTP} = \left(\frac{V_{sat} - x}{R_1 + R_2} \right) R_2 + x \quad V_{LTP} = \left(\frac{-V_{sat} - x}{R_1 + R_2} \right) R_2 + x$$

$$2 = \left(\frac{10 - x}{R_1 + R_2} \right) R_2 + x$$

$$-4 = \left(\frac{-10 - x}{R_1 + R_2} \right) R_2 + x$$

$$H = V_{UTP} - V_{LTP} =$$

$$6 = \left(\frac{10 - x}{R_1 + R_2} \right) R_2 + x - \left(\frac{-10 - x}{R_1 + R_2} \right) R_2 - x$$

$$\frac{6(R_1 + R_2)}{R_2} = 10 - x + 10 + x$$

$$6R_1 + 6R_2 = 20R_2$$

$$6R_1 = 14R_2$$

$$R_1 = \frac{14R_2}{6}$$

Hypothetical condition

$$2 = \left(\frac{10 - x}{2.33k + 1k} \right) 1k + x$$

$$2(3.33) = 10 - x + 3.33x$$

$$2.33x = 6.66 - 10$$

$$x = -1.433V$$

Assuming $R_2 = 1k\Omega$

$$R_1 = \frac{14(1k)}{6} =$$

$$R_1 = 2.33k\Omega$$

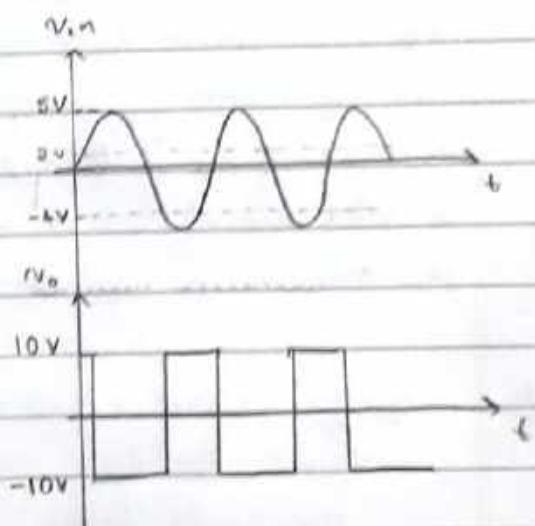
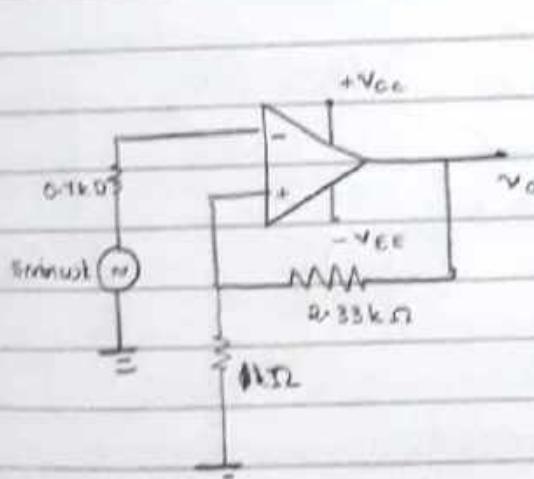
$$R_{comp} = R_1 // R_2$$

$$= \frac{14R_2 // R_2}{6}$$

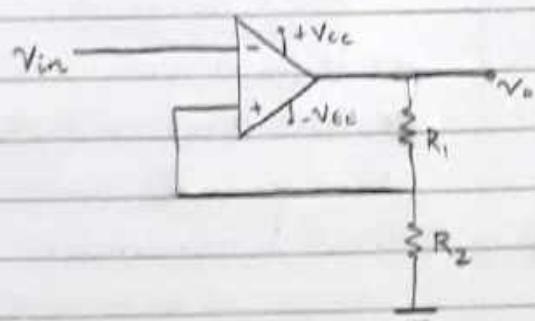
$$= \frac{14R_2 R_2 / 6}{10 \cdot 20R_2 / 6} = 0.7R_2$$

$$10 \cdot 20R_2 / 6$$

$$R_{comp} = 0.7k\Omega$$



- Q1: For the circuit shown in the figure calculate the values of R_1 and R_2 , if saturation voltage are $\pm 12V$. Assume hysterisis width as $6V$.



Given: $\pm V_{sat} = \pm 12V$

$$H = 6V$$

$$V_{UTP} = \frac{V_{sat} R_2}{R_1 + R_2} = \frac{12 R_2}{R_1 + R_2}$$

$$V_{LTP} = -\frac{V_{sat} R_2}{R_1 + R_2} = -\frac{12 R_2}{R_1 + R_2}$$

$$H = V_{UTP} - V_{LTP}$$

$$H = 2 \left[\frac{12 R_2}{R_1 + R_2} \right]$$

$$3R_1 + 3R_2 = 12R_2$$

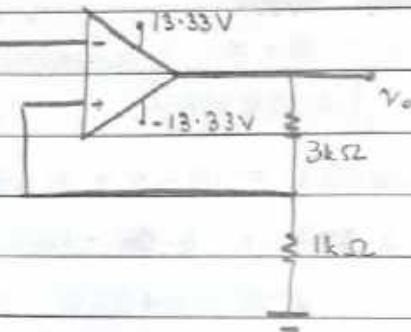
$$3R_1 = 9R_2$$

$$\underline{R_1 = 3R_2}$$

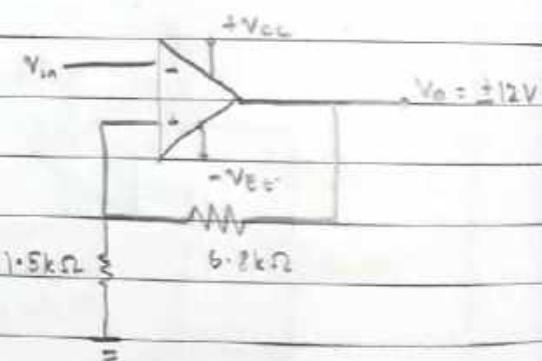
Assuming $R_2 = 1k\Omega$

then $R_1 = 3(1k)$

$\therefore R_1 = 3k\Omega$



Q3: For a Schmitt trigger shown in the figure calculate the trip point and hysteresis if saturation is $\pm 13.5V$. If the resistance have a tolerance of $\pm 5\%$. What is the minimum hysteresis.



Sol: Given: $\pm V_{sat} = \pm 13.5V$

$$V_{UTP} = \frac{V_{sat} R_2}{R_1 + R_2} = \frac{13.5 (1.5k)}{1.5k + 6.8k} = \frac{13.5 (1.5k)}{(8.3k)}$$

$$V_{UTP} = 0.2913V \Rightarrow V_{LTP} = -0.2913V$$

$$H = V_{UTP} - V_{LTP}$$

$$H = 2(0.2913) = 0.5826V$$

For minimum hysteresis R_2 must be minimum and R_1 must be maximum.

$$R_{2min} = R_2 - 5\% \cdot R_2 = 1.5k - 5(1.5k) = \underline{\underline{1.4925k\Omega}}$$

$$R_{1max} = R_1 + 5\% \cdot R_1 = 6.8k + 6.8k \left(\frac{5}{100} \right) = \underline{\underline{7.14k\Omega}}$$

$$H = \frac{2V_{sat}R_2}{R_1 + R_2} = \frac{2(13.5)(1.5k)}{(6.8k + 1.5k)} = \frac{13.5(3k)}{8.3k} = 0.5356V$$

* Logarithmic Amplifier:

logarithmic amplifier can be constructed by using diode and transistor.

- Logarithmic Amplifier using diode

By virtual ground

$$V_A = V_B = 0$$

$$\therefore I = I_f$$

$$I = \frac{V_i - V_A}{R} = \frac{V_i}{R} = I_f$$

By diode equations

$$I_f = I_0 [e^{\frac{V_A - V_D}{V_T}} - 1]$$

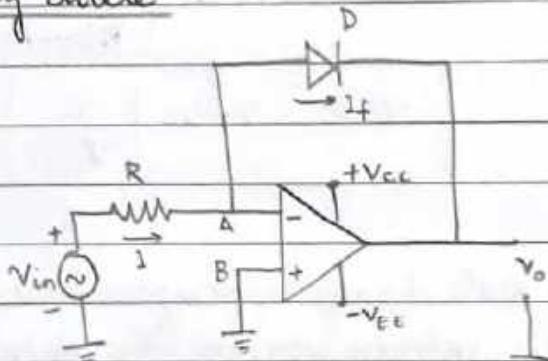
and

$$V = \eta V_T \ln \left[\frac{I_f}{I_0} \right]$$

$$\therefore -V_D = \eta V_T \ln \left[\frac{I_f}{I_0} \right]$$

$$\Rightarrow V_o = -\eta V_T \ln \left[\frac{V_i}{R I_0} \right]$$

$$\therefore V_o = -\eta V_T \ln \left[\frac{V_i}{V_{ref}} \right] \quad \text{where } V_{ref} = 20R$$



Voltage across the diode

$$V_A - V_D = -V_o$$

- Logarithmic Amplifier using Transistor:

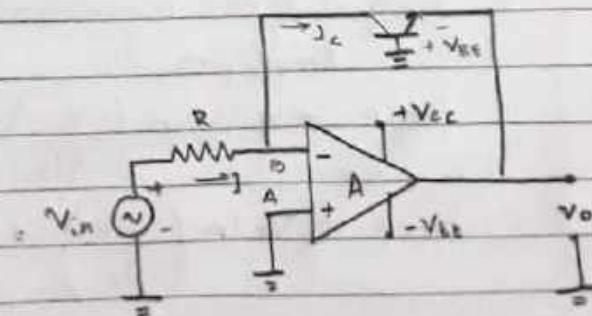
By virtual ground

$$V_A = V_B = 0$$

$$I = I_c$$

$$I = \frac{V_i - V_B}{R} = \frac{V_i}{R} = I_c$$

$$V_{CB} = 0$$



$$V_{BE} = V_T \ln \left(\frac{I_c}{I_s} \right)$$

$$\text{By KVL: } V_o + V_{BE} = 0$$

$$\Rightarrow V_o = -V_{BE}$$

$$\therefore V_o = -V_T \ln \left(\frac{I_c}{I_s} \right)$$

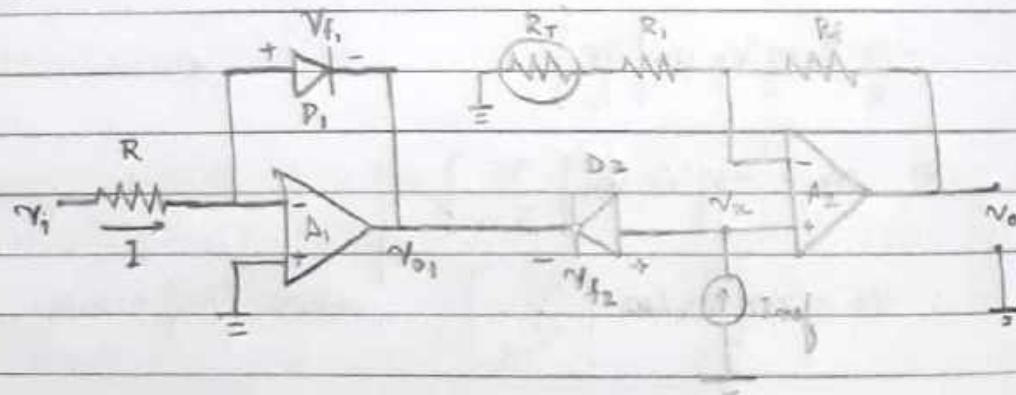
$$V_o = -V_T \ln \left(\frac{V_i}{R I_s} \right)$$

$$V_o = -V_T \ln \left[\frac{V_i}{V_{ref}} \right]$$

where $V_{ref} = I_s R$

With change in temperature the current I_o and I_s varies this in turn varies the output voltage. Hence to overcome this a temperature compensating diode is used.

- Logarithmic Amplifier Using Temperature compensating Diode



D_2 : compensating diode.

$$\text{Here } V_{o1} + V_{f2} = V_x \quad \text{--- (1)}$$

V_{o1} : Output of the logarithmic
Amplifier

$$V_{o1} = -\eta V_T \ln \left(\frac{V_i}{R I_o} \right) \quad \text{--- (2)}$$

$$V_{f2} = \eta V_T \ln \left(\frac{I_{f2}}{I_o} \right) \quad \bullet$$

V_x : drop across the compensating
diode.

V_{o1} : Input of second amplifier

$$\therefore V_{T_2} = \eta V_T \ln \left(\frac{I_{ref}}{I_0} \right) \quad \text{--- (3)} \quad (\because I_{T_2} = I_{ref})$$

Substituting eq (2) and eq (3) in eq (1)

$$V_x = -\eta V_T \ln \left(\frac{V_i}{R I_0} \right) + \eta V_T \ln \left(\frac{I_{ref}}{I_0} \right)$$

$$V_x = -\eta V_T \left[\ln \left(\frac{V_i}{R I_0} \right) - \ln \left(\frac{I_{ref}}{I_0} \right) \right]$$

$$V_x = -\eta V_T \left[\frac{V_i}{R} - \ln I_0 - \ln I_{ref} + \ln I_0 \right]$$

$$V_x = -\eta V_T \left[\ln \left(\frac{V_i}{R I_{ref}} \right) \right] \quad \text{--- (4)}$$

Second amplifier is a non inverting amplifier.

The output of non inverting amplifier is given by

$$V_o = V_x \left[1 + \frac{R_f}{R_i} \right]$$

$$\therefore V_o = V_x \left[1 + \frac{R_f}{R_i + R_T} \right]$$

Substituting eq (4)

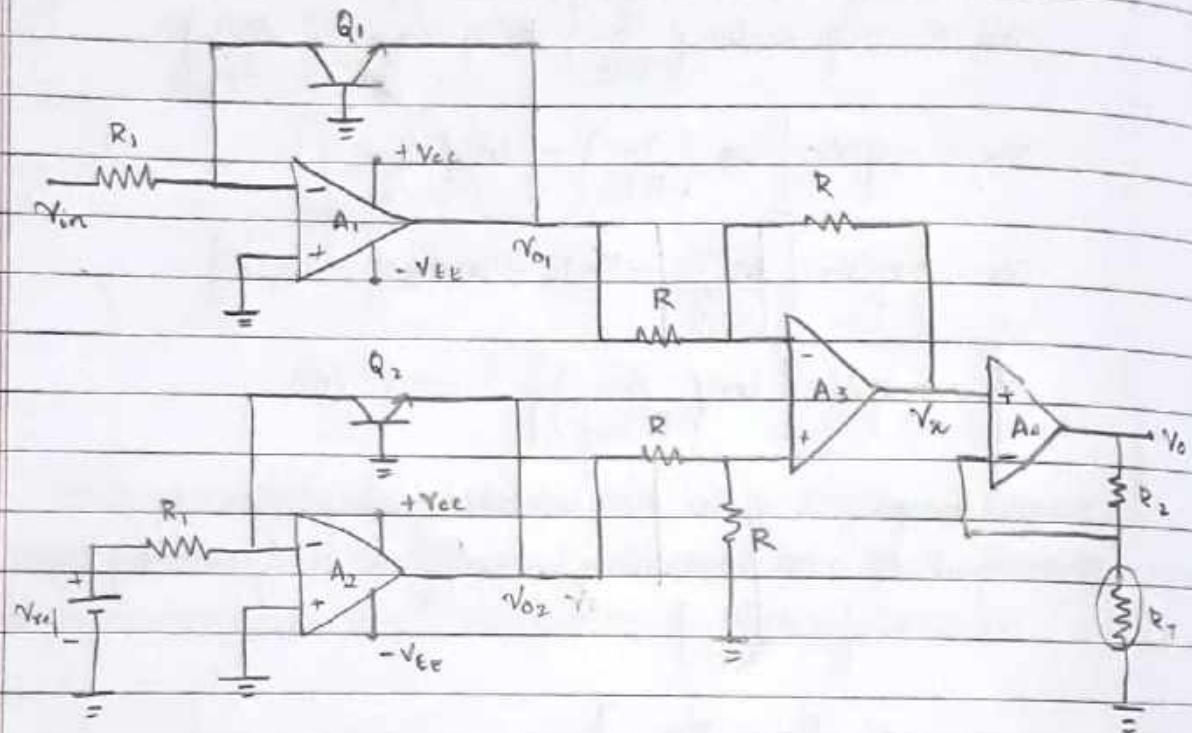
$$V_o = -\eta V_T \ln \left(\frac{V_i}{R I_{ref}} \right) \left[\frac{R_i + R_T + R_f}{R_i + R_T} \right]$$

R_T : Positive temperature coefficient of a thermistor ($R_T \propto T$)

$$V_o = -k \ln \left(\frac{V_i}{R I_{ref}} \right)$$

$$\text{where } k = \eta V_T \left[\frac{R_i + R_T + R_f}{R_i + R_T} \right]$$

- Temperature compensating Technique for logarithmic Amplifier using Transistor:



$$\text{Here } V_x = V_02 - V_01 \quad \text{--- (1)}$$

Output of 1st amplifier

$$V_{01} = -V_T \ln \left(\frac{V_{in}}{R_1 I_s} \right)$$

Output of 2nd amplifier

$$V_{02} = -V_T \ln \left(\frac{V_{ref}}{R_1 I_s} \right)$$

Substituting in eq (1)

$$V_x = -V_T \ln \left(\frac{V_{ref}}{R_1 I_s} \right) + V_T \ln \left(\frac{V_{in}}{R_1 I_s} \right)$$

$$V_x = -V_T \left[\ln \left(\frac{V_{ref}/R_1 I_s}{V_{in}/R_1 I_s} \right) \right]$$

$$V_x = -V_T \ln \left(\frac{V_{ref}}{V_{in}} \right) \quad \text{--- (2)}$$

V_x : Input to the 4th amplifier which is non-inverting amplifier.

The output of non inverting amplifier is given by

$$V_o = V_i \left(1 + \frac{R_f}{R_1} \right)$$

$$V_o = V_{in} \left(1 + \frac{R_2}{R_T} \right)$$

Substituting eq ②

$$V_o = -V_T \ln \left(\frac{V_{ref}}{V_{in}} \right) \left(\frac{R_T + R_2}{R_T} \right)$$

$$V_o = -k \ln \left(\frac{V_{ref}}{V_{in}} \right)$$

$$\text{where } k = V_T \left(\frac{R_T + R_2}{R_T} \right)$$

* Antilogarithmic Amplifier:

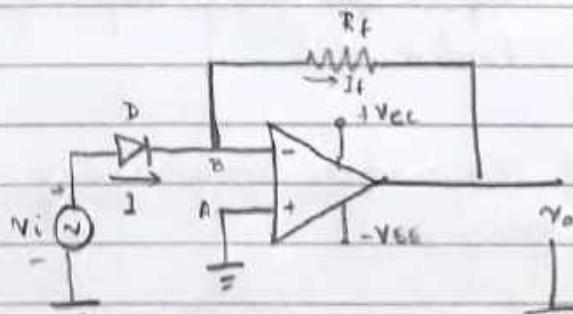
- Antilog Amplifier using diode:

By virtual ground

$$V_A = V_B = 0$$

$$I = I_f$$

$$I_f = \frac{V_B - V_o}{R_f} = -\frac{V_o}{R_f} = I$$



By diode equation

$$I_f = I_0 [e^{V_B / \eta V_T}]$$

$$\therefore -\frac{V_o}{R_f} = I_0 e^{V_B / \eta V_T}$$

$$V_o = -I_0 R_f e^{V_B / \eta V_T}$$

$$\therefore V_o = -V_{ref} e^{V_B / \eta V_T}$$

$$\text{where } V_{ref} = I_0 R_f$$

Here the output is dependent on I_0 and V_{ref} hence we adopt compensating technique using temperature compensating diode.

— Antilog amplifier using transistor

By virtual ground

$$V_A = V_B = 0$$

Hence $V_{CB} = 0$

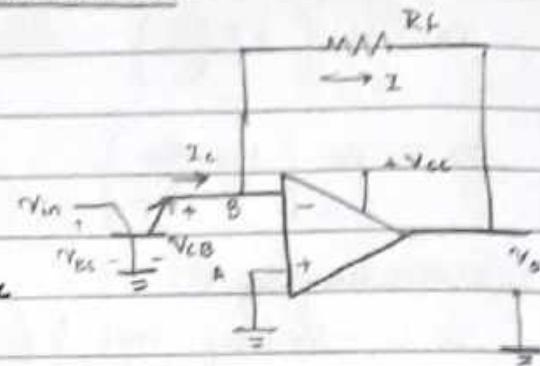
$$I = I_C$$

$$I = \frac{V_B - V_0}{R_f} = \frac{-V_0}{R_f} = I_C$$

$$I_C = I_s e^{\frac{V_{BE}}{kT}}$$

$$\therefore -\frac{V_0}{R_f} = I_s e^{\frac{V_{BE}}{kT}}$$

$$V_0 = -I_s R_f e^{\frac{V_{BE}}{kT}}$$

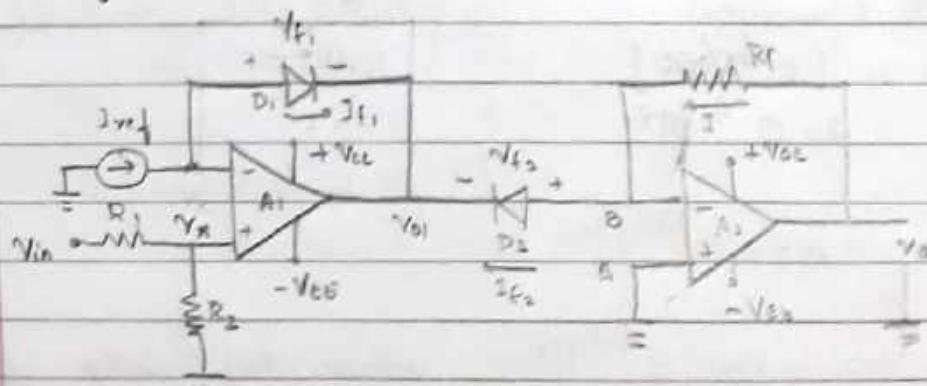


$$V_0 = -V_{ref} e^{\frac{V_{BE}}{kT}}$$

where $V_{ref} = I_s R_f$

Here V_0 is dependent on I_s and V_T which varies with temperature hence temperature compensating technique is adopted.

— Temperature compensating Technique for Antilog amplifier using diode :



D_2 : compensating diode

$$V_{o1} = V_x - V_{f1} \quad \text{--- (1)}$$

By voltage divider rule

$$V_x = \frac{V_{in} R_2}{R_1 + R_2} \quad \text{--- (2)}$$

V_{f2} : drop across the compensating diode

V_x : Input to first amplifier
 V_{o1} : Output of 1st amplifier (antilog)

Basic voltage equation for a diode

$$V_F = \eta V_T \ln \left(\frac{I_{F1}}{I_0} \right) \quad \textcircled{3}$$

Substituting eq. ② and eq. ③ in eq. ①

$$V_{O1} = \frac{V_{in} R_2}{R_1 + R_2} - \eta V_T \ln \left[\frac{I_{F1}}{I_0} \right] \quad \textcircled{4}$$

By virtual ground $V_B = 0$

$$\therefore V_{O1} = -V_{F2}$$

$$\text{but } V_{F2} = \eta V_T \ln \left(\frac{I_{F2}}{I_0} \right)$$

$$I_{F2} = I = \frac{V_O - V_B}{R_f} = \frac{V_O}{R_f}$$

$$\therefore V_{F2} = \eta V_T \ln \left(\frac{V_O}{R_f I_0} \right)$$

$$\therefore V_{O1} = -\eta V_T \ln \left(\frac{V_O}{I_0 R_f} \right) \quad \textcircled{5}$$

Equating eq. ④ and eq. ⑤

$$\frac{V_{in} R_2}{R_1 + R_2} - \eta V_T \ln \left[\frac{I_{F1}}{I_0} \right] = -\eta V_T \ln \left[\frac{V_O}{I_0 R_f} \right]$$

$$\frac{V_{in} R_2}{R_1 + R_2} = \eta V_T \left[\ln \left(\frac{I_{F1}}{I_0} \right) - \ln \left(\frac{V_O}{I_0 R_f} \right) \right]$$

$$\frac{V_{in} R_2}{R_1 + R_2} = \eta V_T \ln \left(\frac{I_{F1} / I_0}{V_O / I_0 R_f} \right)$$

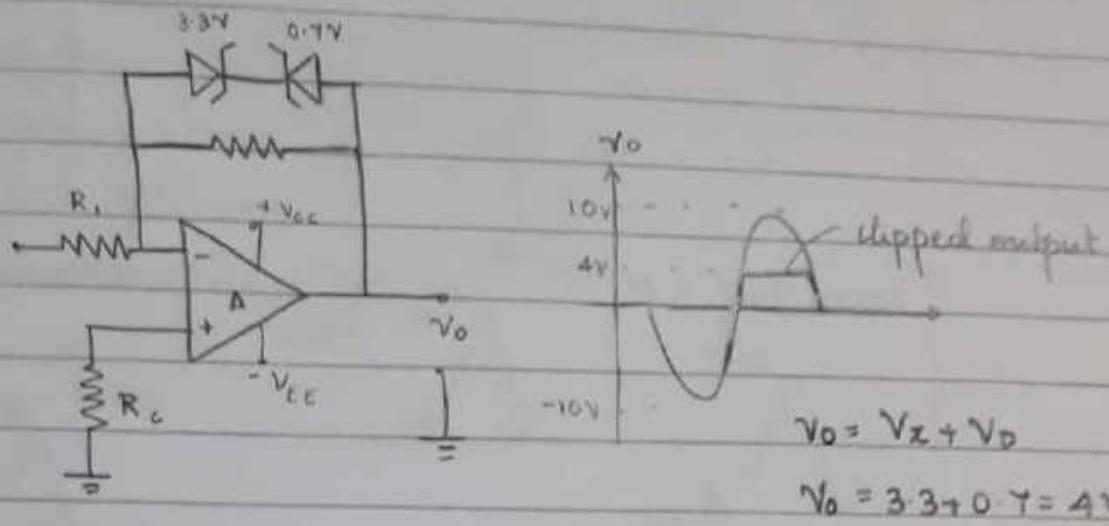
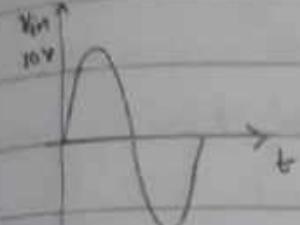
$$\frac{V_{in} R_2}{R_1 + R_2} = -\eta V_T \ln \left[\frac{V_O}{I_{F1} R_f} \right]$$

$$V_O = I_{F1} R_f e^{\left[\frac{-V_{in} R_2}{\eta V_T (R_1 + R_2)} \right]}$$

By taking appropriate value for R_1 and R_2 we can overcome the effect of V_T over V_O .

- Temperature compensating technique for Antilog amplifier using transistor: (ma'am notes)

clippers:



When only 1 zener diode is connected in reverse biased and the other is forward biased (acts as normal diode). It acts as positive clipper.

When both the zener diodes are reverse biased i.e., they are connected back to back then it acts a double ended clipper circuit.

i Design a clipping circuit for a clipping levels of $+0.35V$ given an input sine wave signal of $0.5V_p$. Assume the gain of the amplifier is 10 and it has an input resistance of $1k\Omega$ connected.

When unclipped

$$V_o = V_i \times A$$

$$V_o = 0.5 \times 10 = 5V //$$

When clipped

$$V_o = 0.35 \times 10 = 3.5V //$$

For positive clipper

$$V_o = V_x + V_d$$

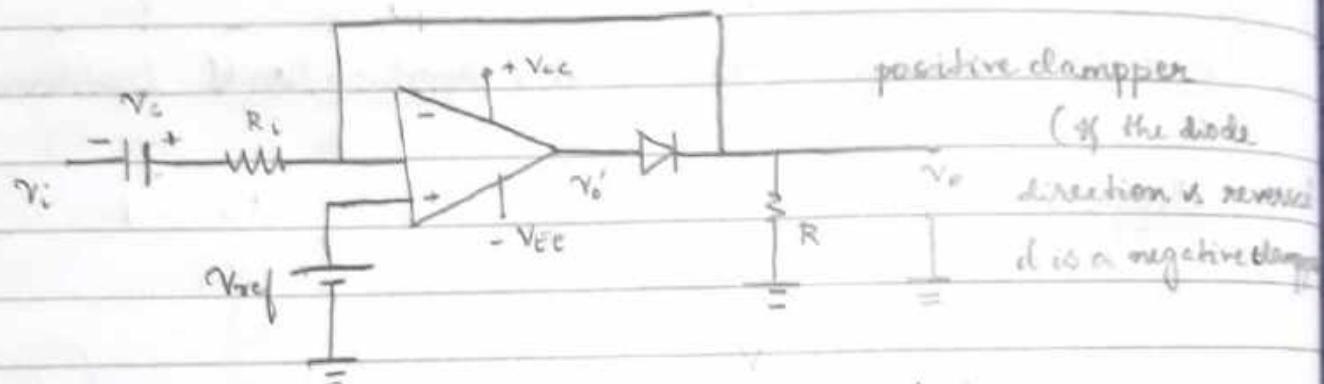
$$V_x = 3.5 - 0.7$$

$$\underline{\underline{V_x = 2.8V}}$$

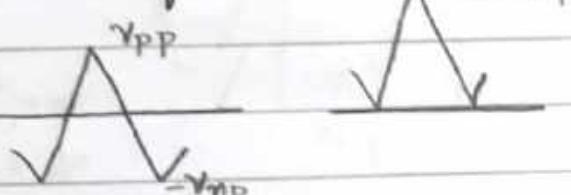
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* clampers



when $V_{ref} = 0$

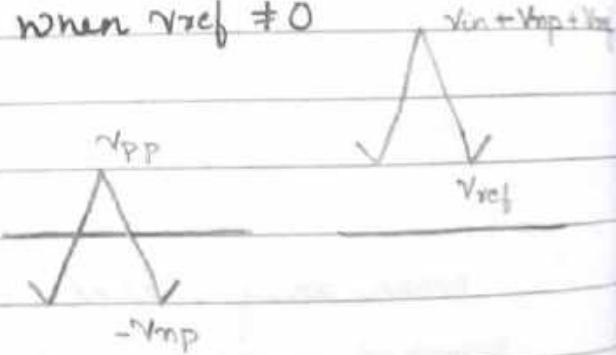


$$V_c = V_{np}$$

$$V_o = V_i + V_c$$

$$V_o = V_i + V_{np}$$

when $V_{ref} \neq 0$



$$V_c = V_{np} + V_{ref}$$

$$V_o = V_i + V_c$$

$$V_o = V_{in} + V_{np} + V_{ref}$$