INSTITUTE OF ENGINEERING AND TECHNOLOGY

DEVI AHILYA VISHWAVIDYALAYA, INDORE

Session: 2024-25

System On Chip Project using Verilog

Submitted by:
21T6004 Akshay Pandey

Submitted to:
Dr. Ravi Sindal Sir

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Assignment-1

Q.1 Write Verilog code for gates using all modelling.

a. Basic Gates(NOT/OR/AND)

b. Universal Gates

c. EX-OR and EX-NOR gates

Sol a.> NOT GATE

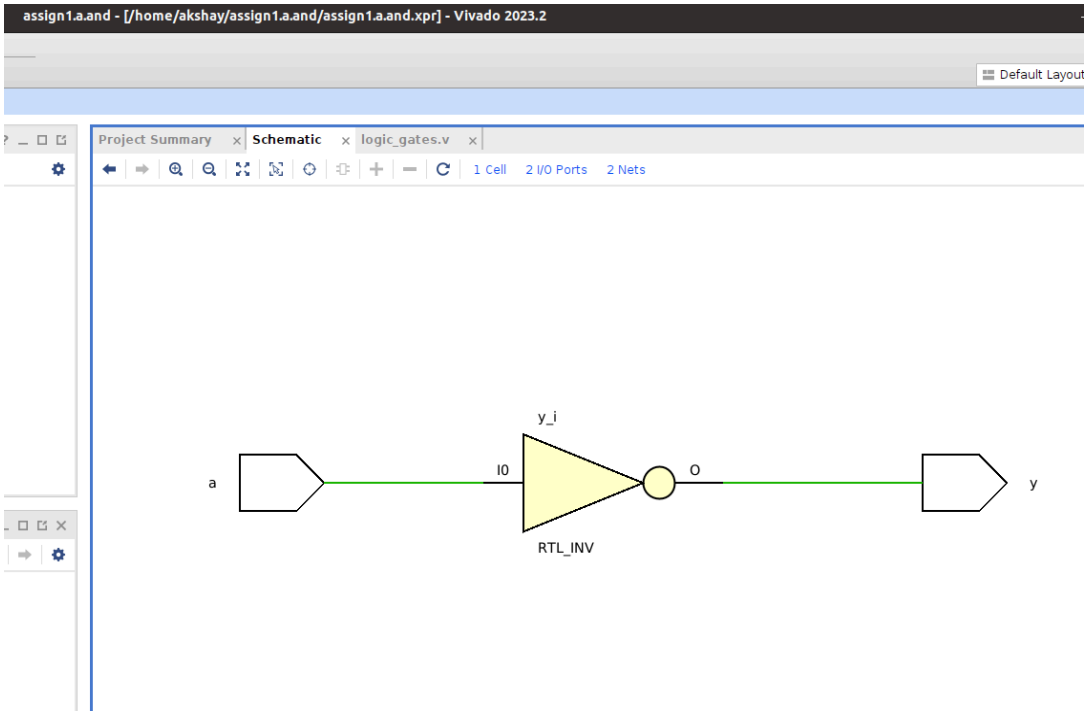
```
//NOT gate using Structural modeling
module not_gate_s(a,y);
input a;
output y;
not(y,a);
endmodule
//NOT gate using data flow modeling
module not_gate_d(a,y);
input a;
output y;
assign y = ~a;
endmodule
//NOT gate using behavioural modeling
module not_gate_b(a,y);
input a;
output reg y;
always @ (a)
```

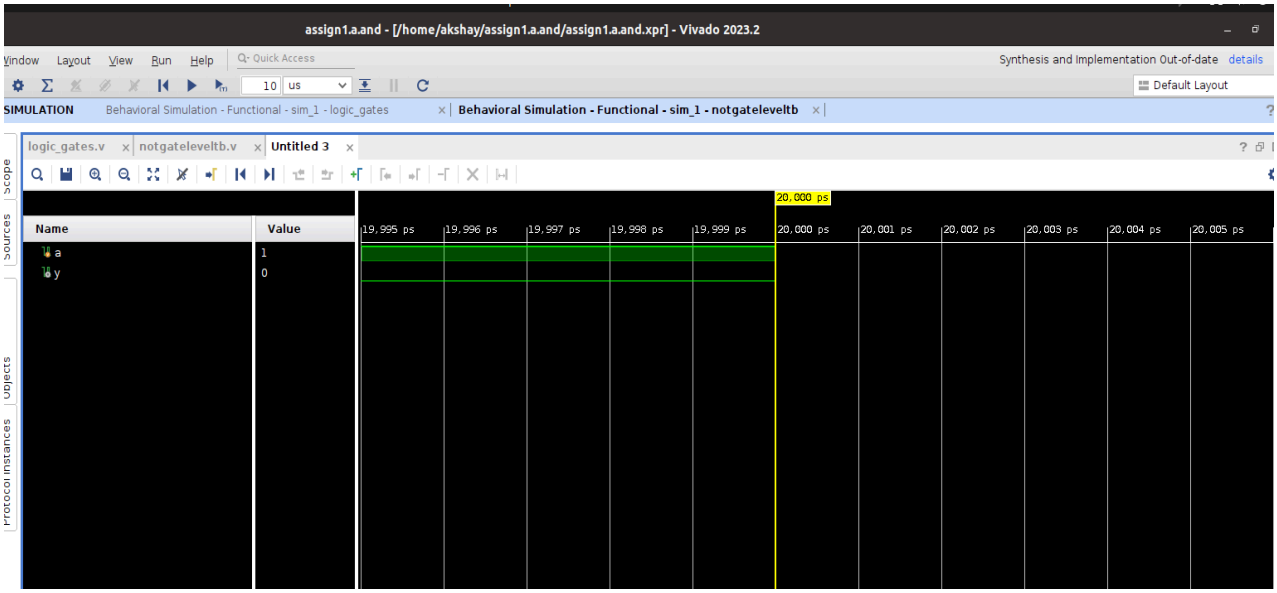
y=~a;

endmodule

TESTBENCH CODE:

```
module not_gate_tb;

reg a;

wire y;

not_gate_s uut(a,y);

initial begin

a = 0;

#10

b = 1;

#10

$finish();

end

Endmodule
```




assign1.a.and - [/home/akshay/assign1.a.and/assign1.a.and.xpr] - Vivado 2023.2
Window
Layout
View
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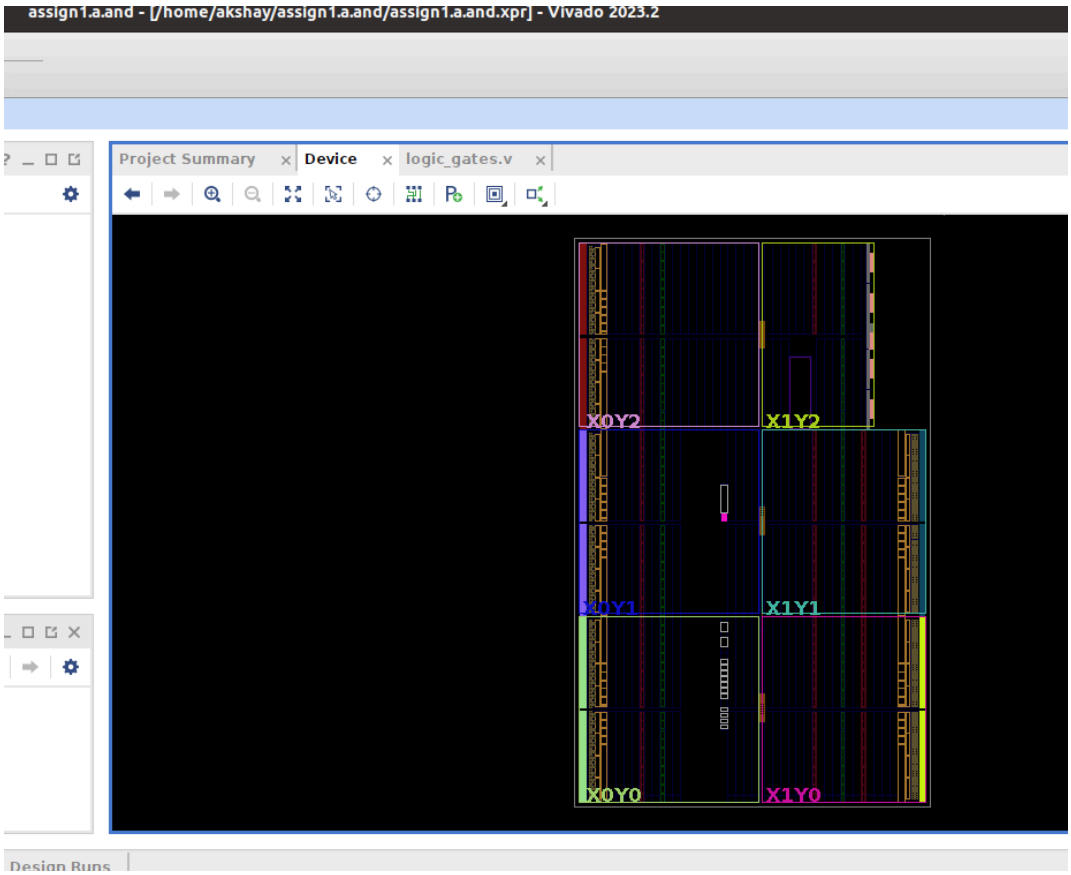
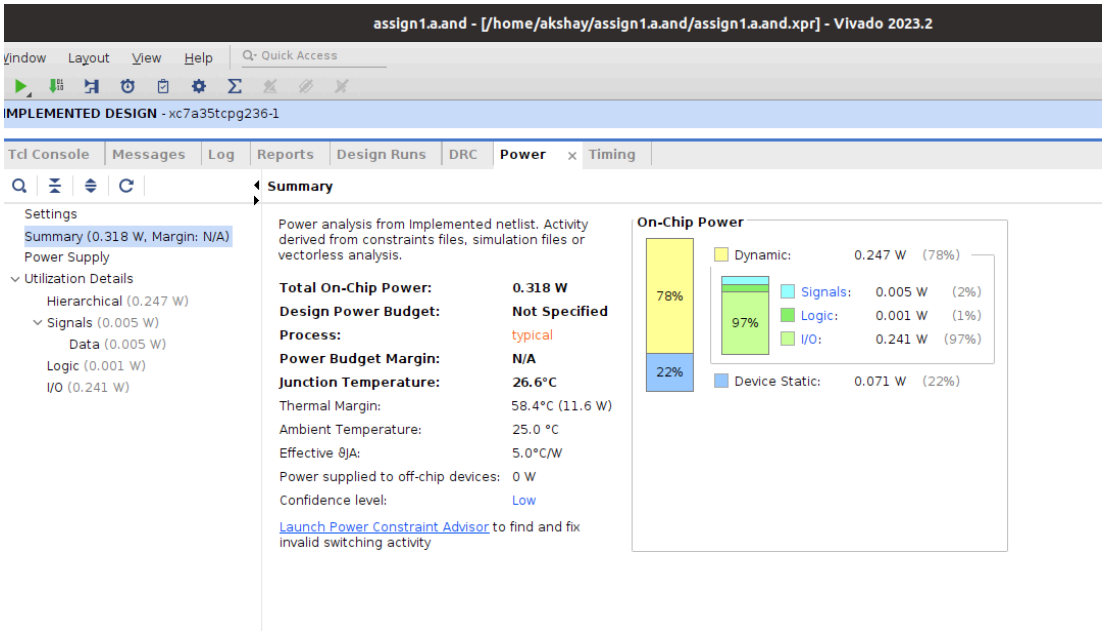
Help
Quick Access
Synthesis and Implementation Out-of-date
details
Default Layout
SIMULATION
Behavioral Simulation - Functional - sim_1 - logic_gates
Behavioral Simulation - Functional - sim_1 - notgateleveltb
logic_gates.v
notgateleveltb.v
Untitled 3
Name
Value
a
y
1
0
20,000 ps
19,995 ps
19,996 ps
19,997 ps
19,998 ps
19,999 ps
20,000 ps
20,001 ps
20,002 ps
20,003 ps
20,004 ps
20,005 ps


assign1.a.and - [/home/akshay/assign1.a.and/assign1.a.and.xpr] - Vivado 2023.2
Project Summary
Device
logic_gates.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Design Runs



OR GATE

//OR gate using Structural modeling

```
module or_gate_s(a,b,y);

input a,b;

output y;

or(y,a,b);

endmodule
```

//OR gate using data flow modeling

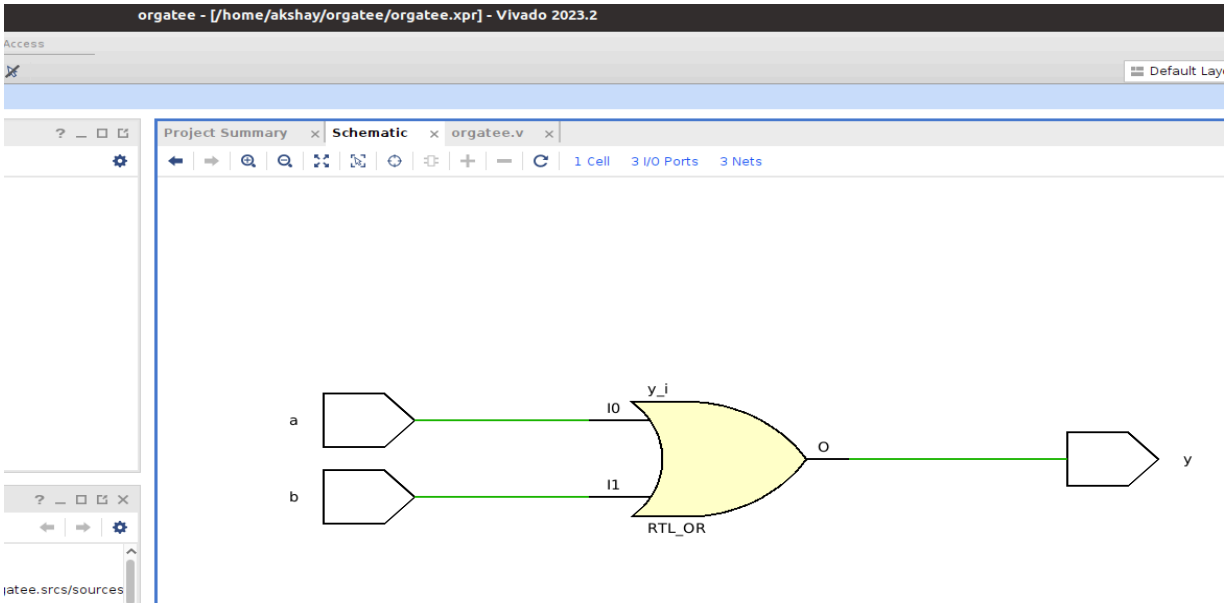
```
module or_gate_d(a,b,y);

input a,b;

output y;

assign y = a | b;

endmodule
```

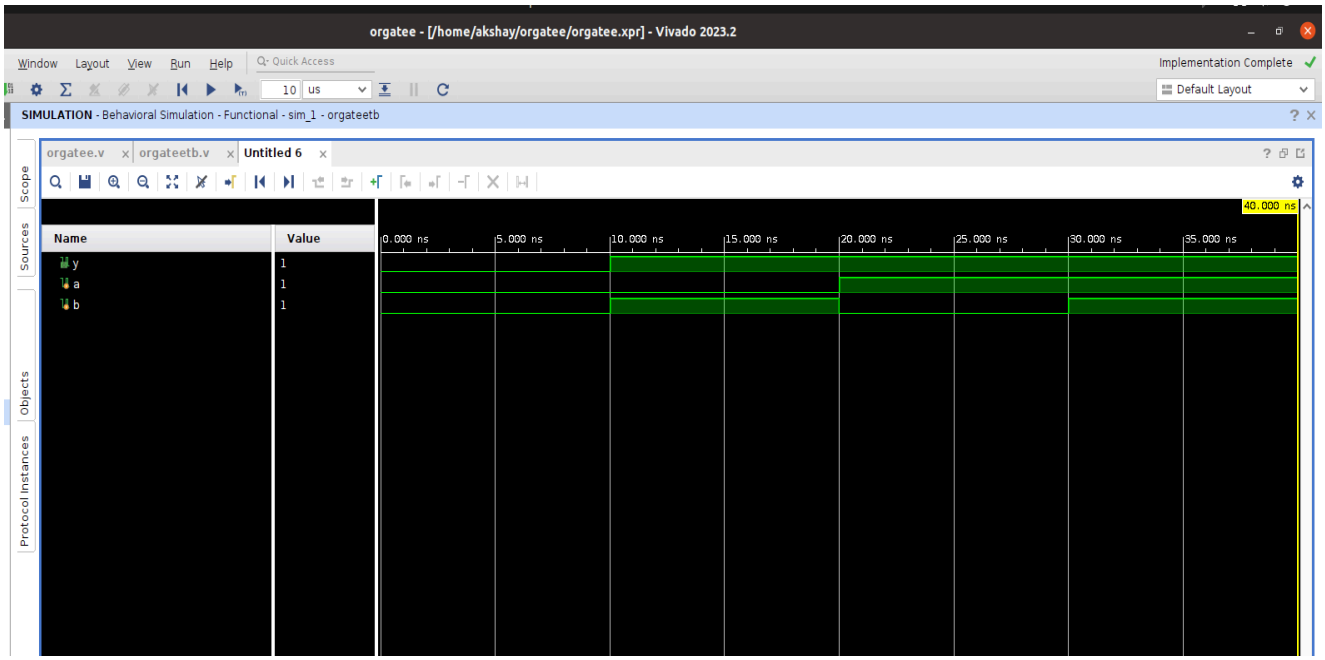
//OR gate using behavioural modeling

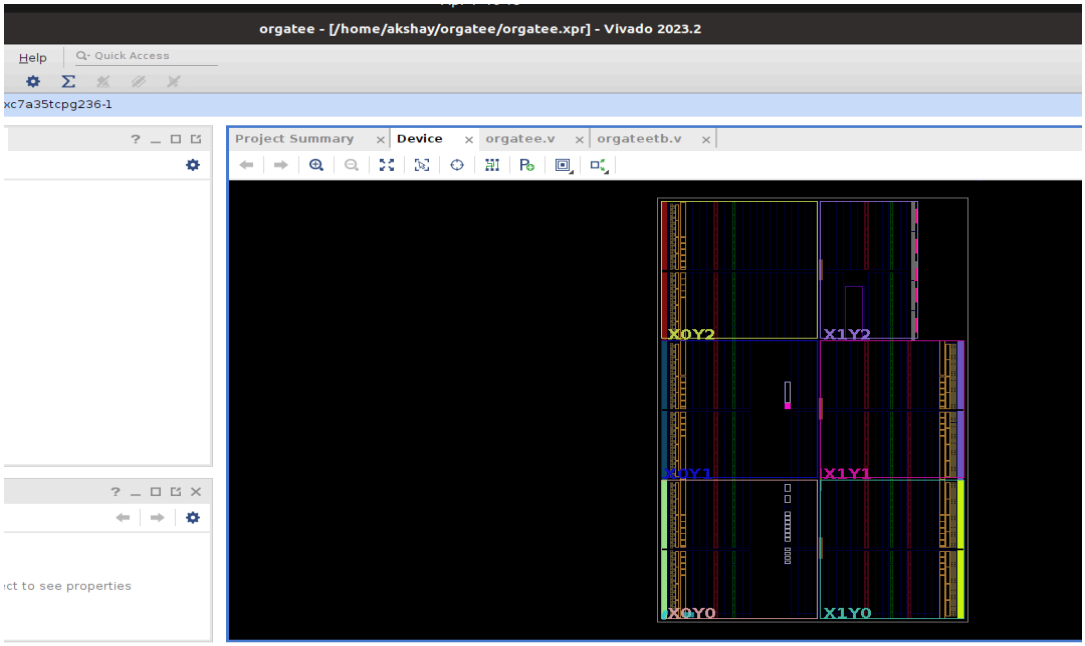
```
module or_gate_b(a,b,y);
input a;
output y;
always @ (a,b)
y = a | b;
endmodule
```

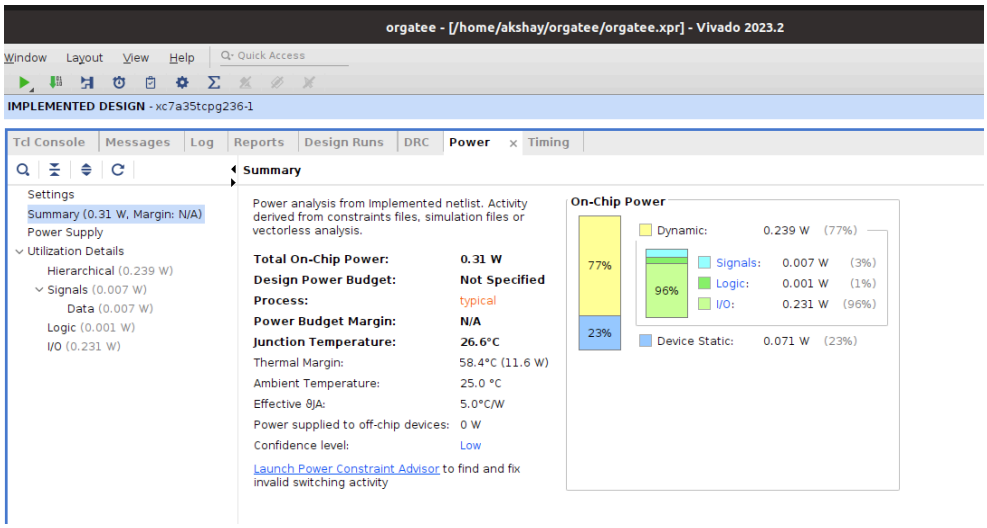
TESTBENCH CODE:

```
module or_gate_tb;
reg a,b;
wire y;
or_gate_s uut(a,b,y);
initial begin
a = 0; b = 0;
#10
b = 0; b = 1;
#10
a = 1; b = 0;
#10
b = 1; b = 1;
#10
$finish();
end
endmodule
```


orgatee - [/home/akshay/orgatee/orgatee.xpr] - Vivado 2023.2
Access
Default Lay
Project Summary
Schematic
orgatee.v
1 Cell
3 I/O Ports
3 Nets
a
b
I0
I1
y_i
O
y
RTL_OR
atee.srcs/sources


orgatee - [/home/akshay/orgatee/orgatee.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Implementation Complete
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - orgateetb
orgatee.v
orgateetb.v
Untitled 6
Scope
Sources
Objects
Protocol Instances
Name
Value
y
a
b
1
1
1
40.000 ns
0.000 ns
5.000 ns
10.000 ns
15.000 ns
20.000 ns
25.000 ns
30.000 ns
35.000 ns





AND GATE

```
//AND gate using Structural modeling

module and_gate_s(a,b,y);

input a,b;

output y;

and(y,a,b);
```

```
endmodule
```

//AND gate using data flow modeling

```
module and_gate_d(a,b,y);
input a,b;
output y;
assign y = a & b;
endmodule
```

//AND gate using behavioural modeling

```
module nAND_gate_b(a,b,y);
input a;
output y;
always @ (a,b)
y = a & b;
Endmodule
```

TESTBENCH CODE:

```
module and_gate_tb;
reg a,b;
wire y;
and_gate_s uut(a,b,y);
initial begin
a = 0; b = 0;
#10
b = 0; b = 1;
#10
```

a = 1; b = 0;

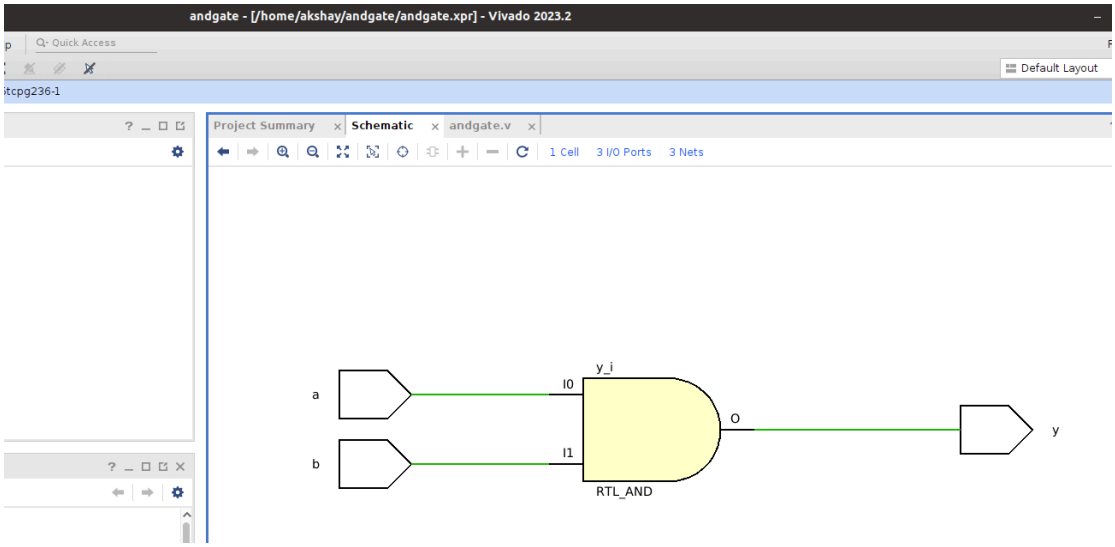
#10

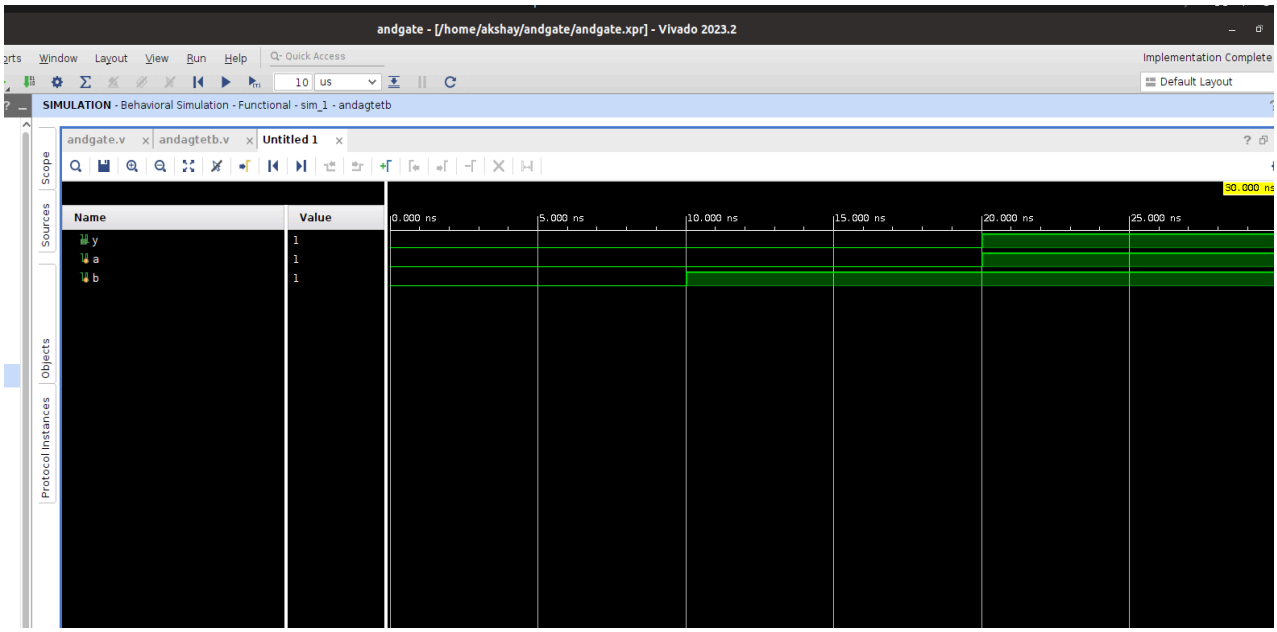
b = 1; b = 1;

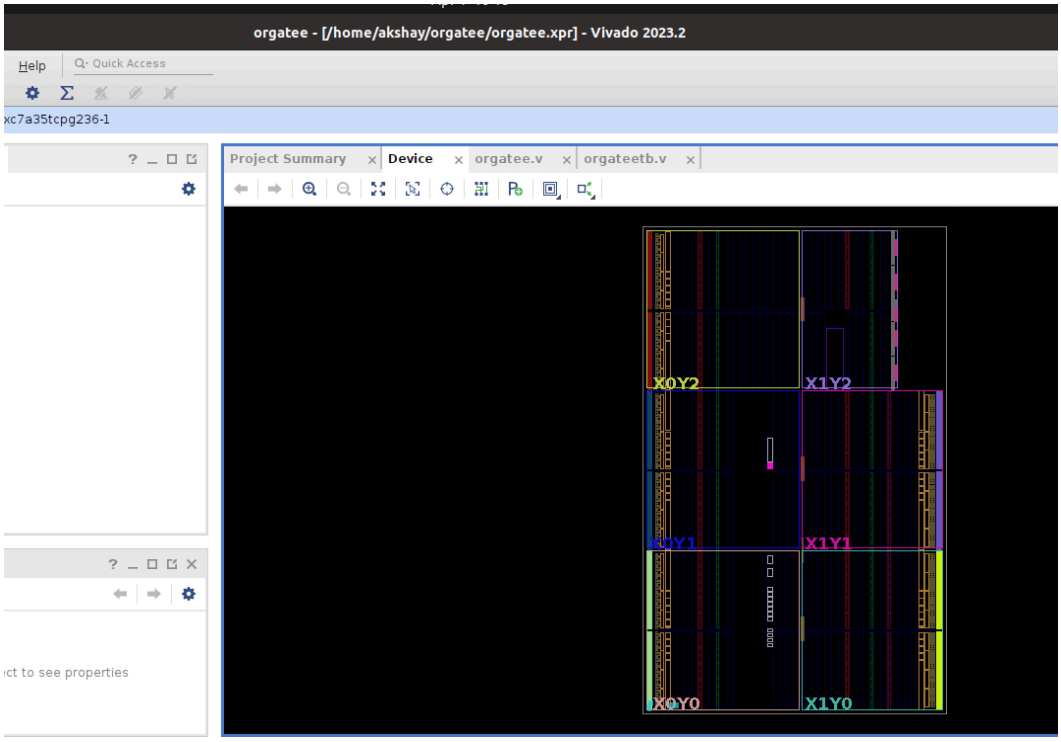
#10

$finish();

End



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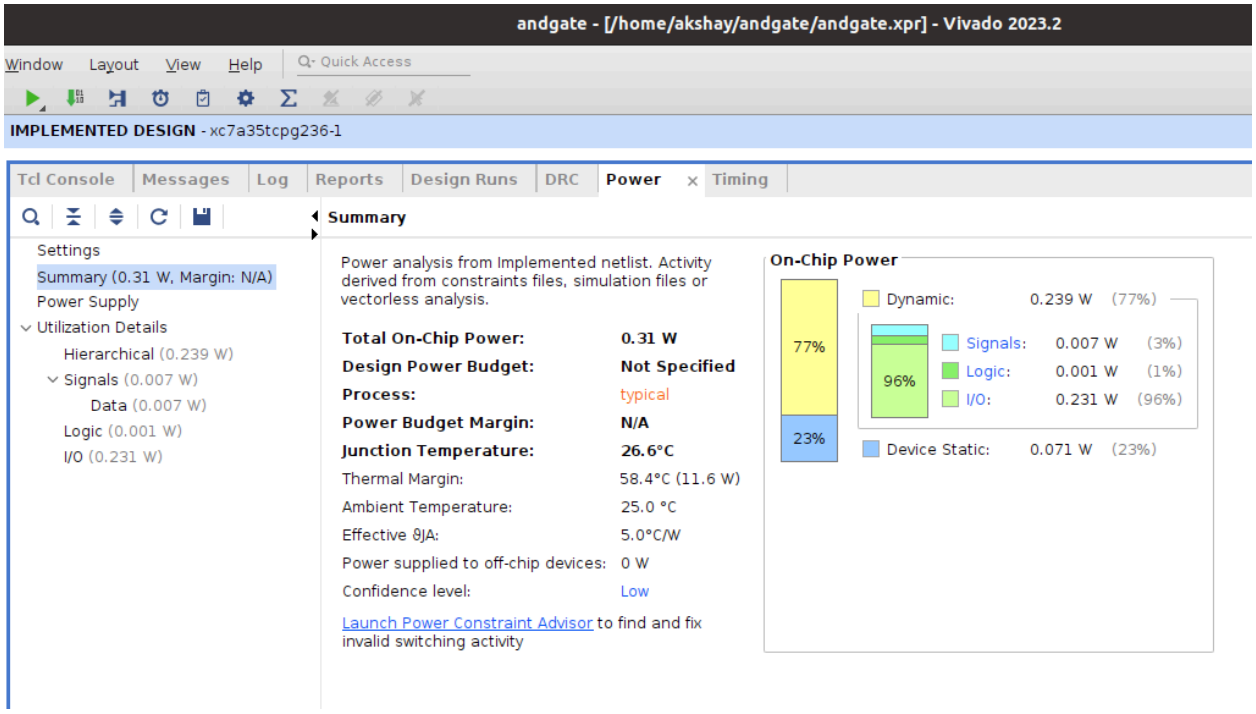
Help
Quick Access
xc7a35tcpg236-1
Project Summary
Device
orgatee.v
orgateetb.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0


andgate - [/home/akshay/andgate/andgate.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Settings
Summary (0.31 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.239 W)
Signals (0.007 W)
Data (0.007 W)
Logic (0.001 W)
I/O (0.231 W)
Summary
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.31 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 26.6°C
Thermal Margin: 58.4°C (11.6 W)
Ambient Temperature: 25.0 °C
Effective ϑJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
77%
23%
96%
Dynamic: 0.239 W (77%)
Signals: 0.007 W (3%)
Logic: 0.001 W (1%)
I/O: 0.231 W (96%)
Device Static: 0.071 W (23%)

Sol b.> NAND GATE

//NAND gate using Structural modeling

```
module nand_gate_s(a,b,y);
input a,b;
output y;
nand(y,a,b);
endmodule
```

//NAND gate using data flow modeling

```
module nand_gate_d(a,b,y);
input a,b;
output y;
assign y = ~(a & b);
endmodule
```

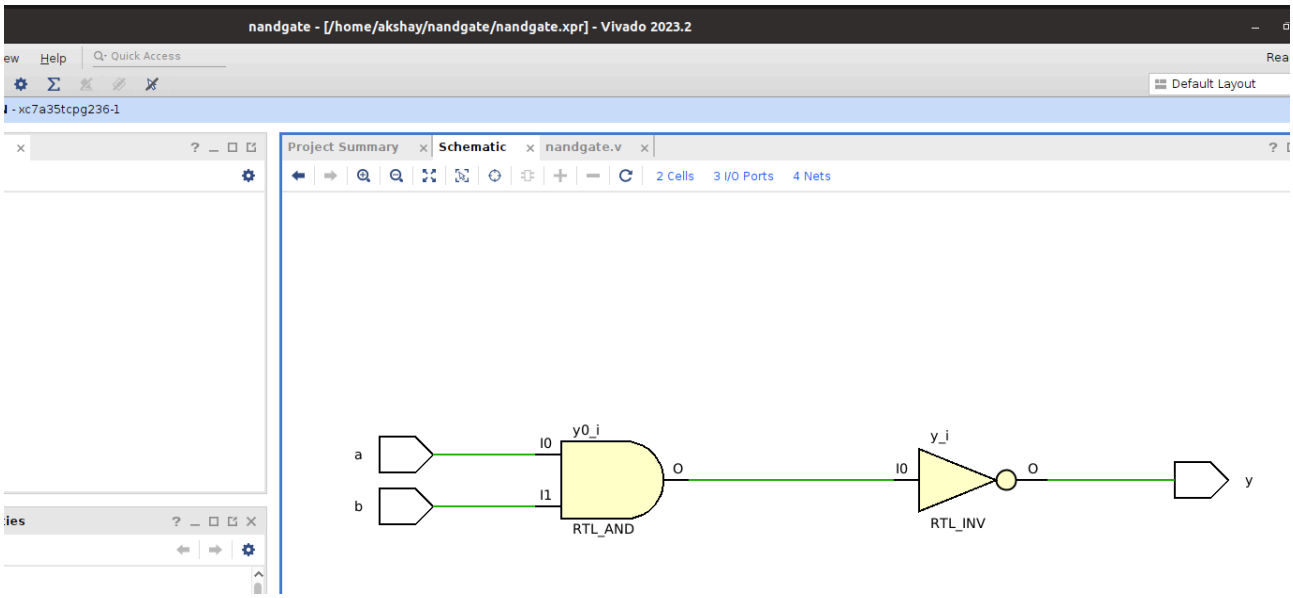
//NAND gate using behavioural modeling

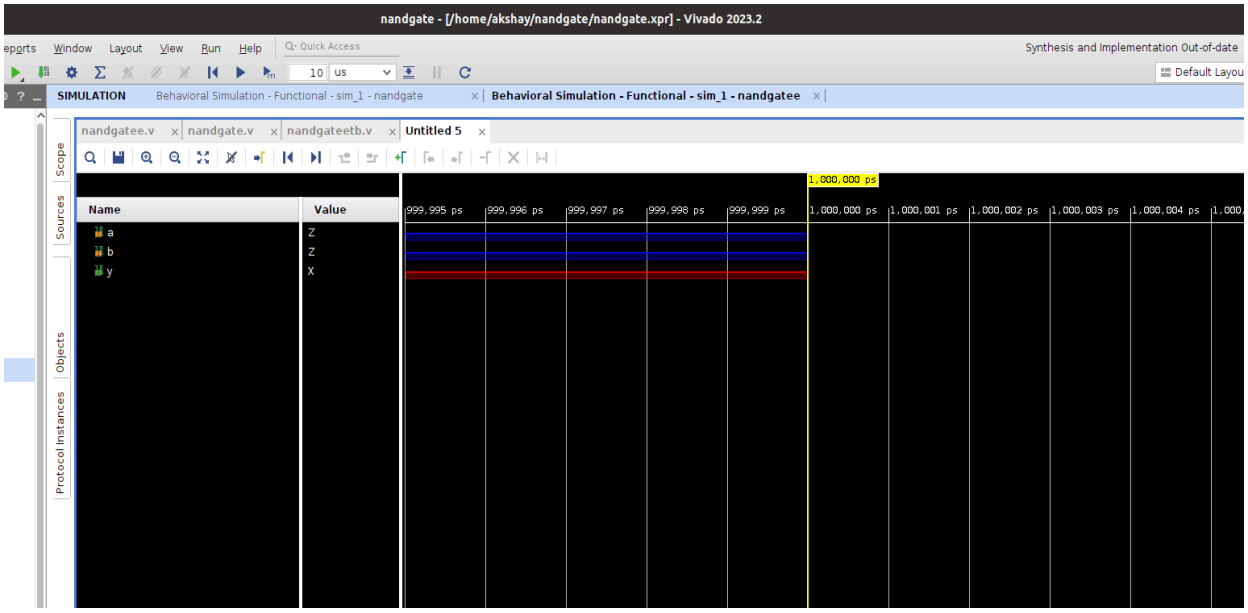
```
module nand_gate_b(a,b,y);
input a;
output reg y;
always @ (a,b)
y = ~(a & b);
Endmodule
```

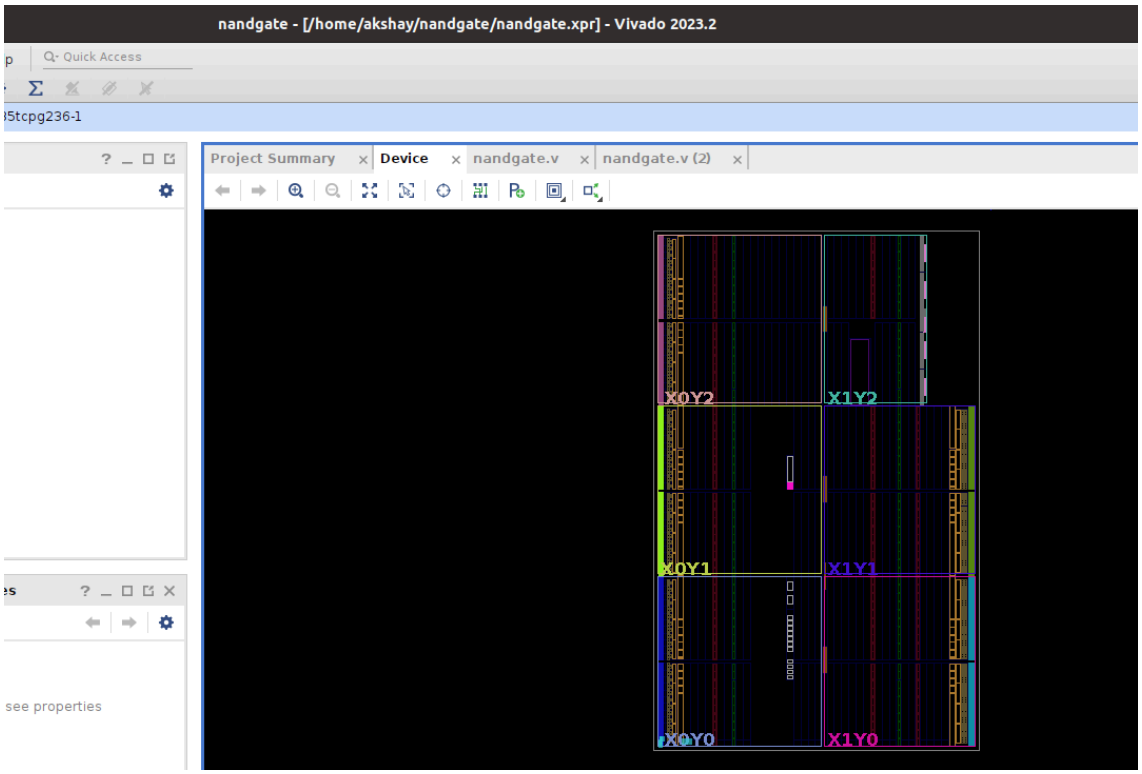
TESTBENCH CODE:

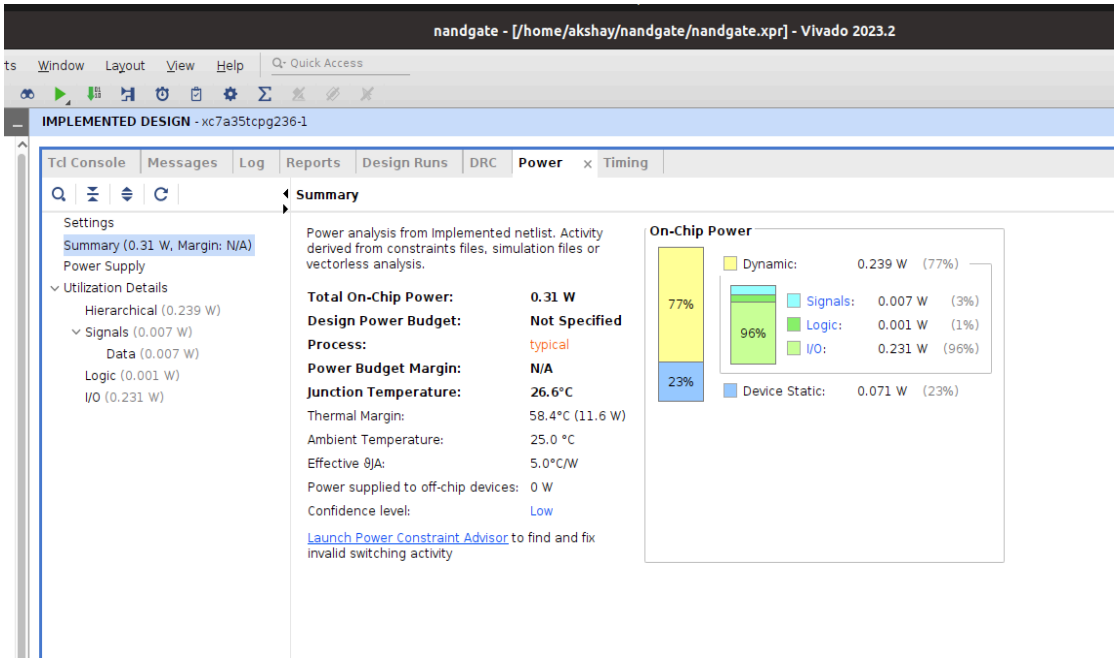
```
module nand_gate_tb;
reg a,b;
```

```
wire y;

nand_gate_s uut(a,b,y);

initial begin

a = 0; b = 0;

#10

b = 0; b = 1;

#10

a = 1; b = 0;

#10

b = 1; b = 1;

#10

$finish();

end

Endmodule
```




nandgate - [/home/akshay/nandgate/nandgate.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Synthesis and Implementation Out-of-date
SIMULATION
Behavioral Simulation - Functional - sim_1 - nandgate
Behavioral Simulation - Functional - sim_1 - nandgatee
nandgatee.v
nandgate.v
nandgateetb.v
Untitled 5
Scope
Sources
Objects
Protocol Instances
Name
Value
a
b
y
Z
Z
X
1,000,000 ps
999,995 ps
999,996 ps
999,997 ps
999,998 ps
999,999 ps
1,000,000 ps
1,000,001 ps
1,000,002 ps
1,000,003 ps
1,000,004 ps


nandgate - [/home/akshay/nandgate/nandgate.xpr] - Vivado 2023.2
Quick Access
Project Summary
Device
nandgate.v
nandgate.v (2)
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
see properties



NOR GATE

//NOR gate using Structural modeling

```
module nor_gate_s(a,b,y);

input a,b;

output y;

nor(y,a,b);

endmodule
```

//NOR gate using data flow modeling

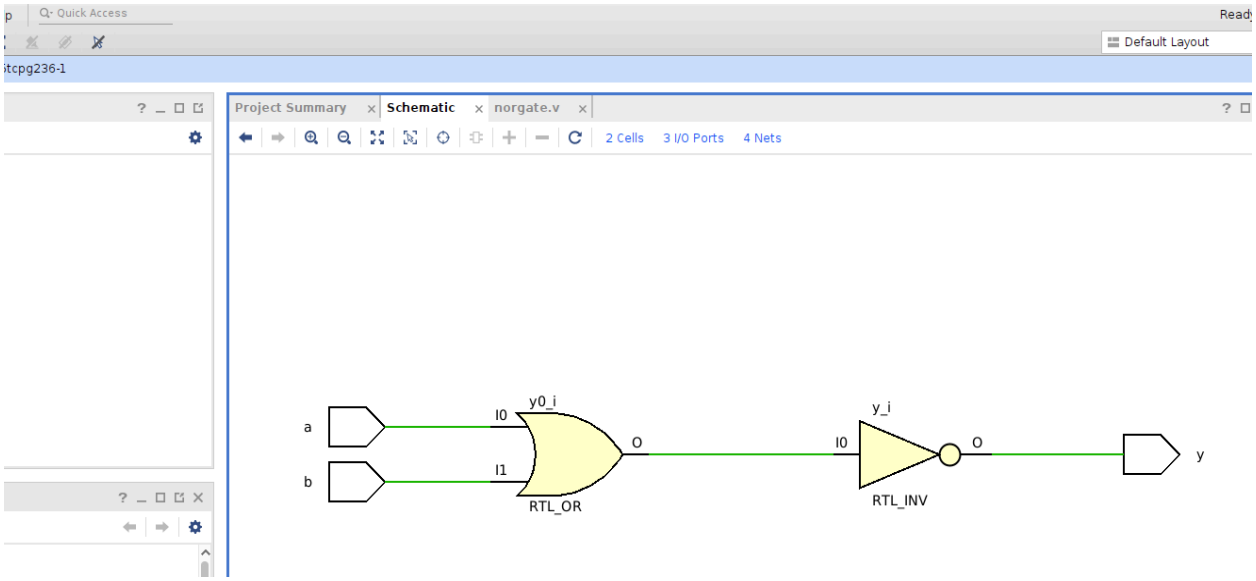
```
module nor_gate_d(a,b,y);

input a,b;

output y;

assign y = ~(a | b); endmodule
```

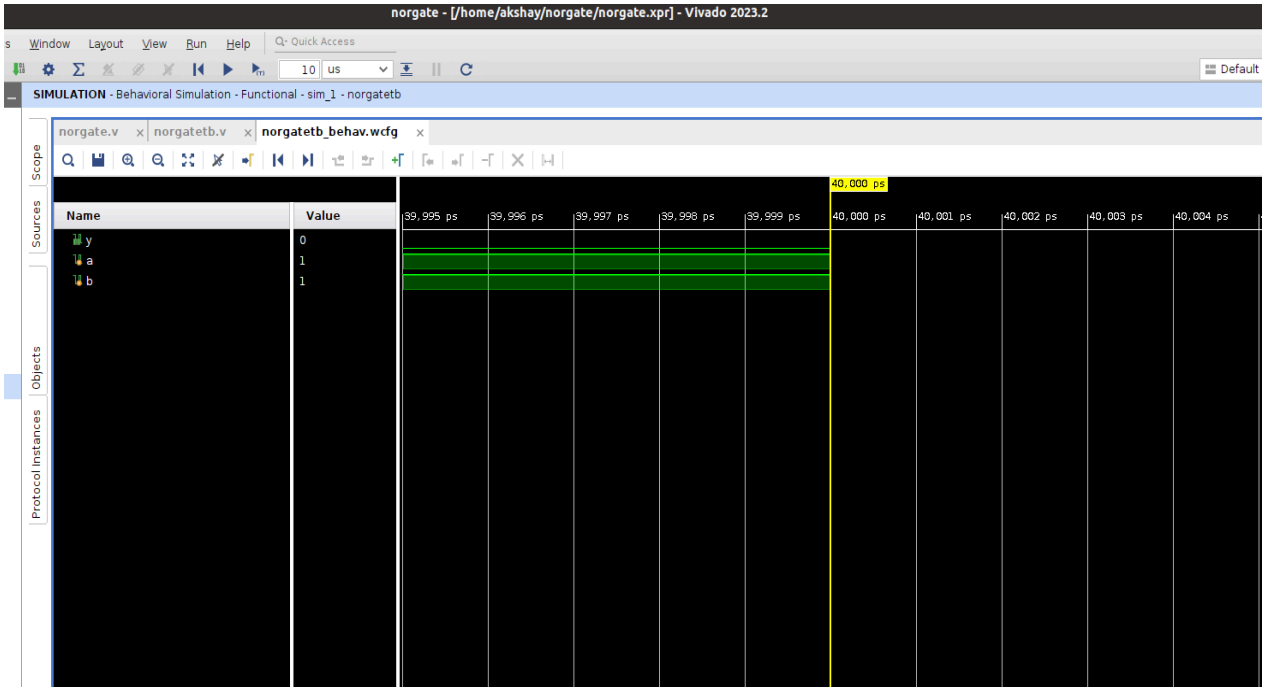
//NOR gate using behavioural modeling

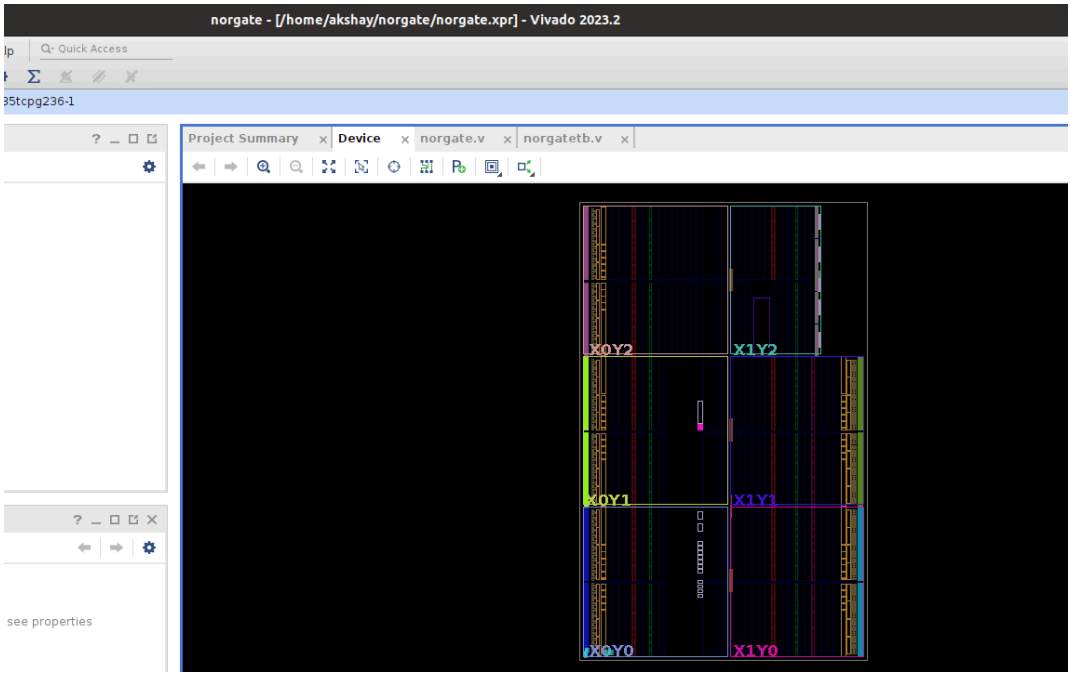
```
module nor_gate_b(a,b,y);
input a;
output reg y;
always @ (a,b)
y = ~(a | b);
endmodule
```

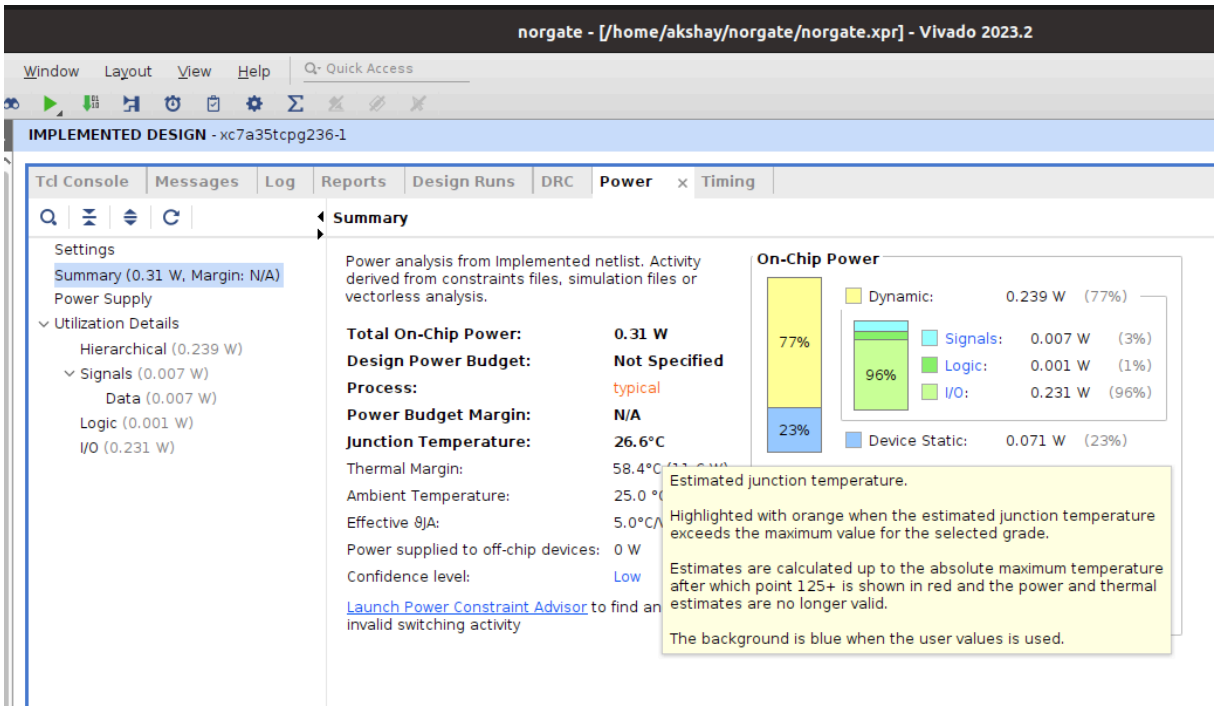
-TESTBENCH CODE:

```
module nor_gate_tb;
reg a,b;
wire y;
nor_gate_s uut(a,b,y);
initial begin
a = 0; b = 0;
#10
b = 0; b = 1;
#10
a = 1; b = 0;
#10
b = 1; b = 1;
#10
$finish();
end
endmodule
```


Quick Access
Ready
Default Layout
itcpg236-1
Project Summary
Schematic
norgate.v
2 Cells
3 I/O Ports
4 Nets
a
b
I0
I1
y0_i
O
RTL_OR
y_i
I0
O
RTL_INV
y


norgate - [/home/akshay/norgate/norgate.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
10
us
Default
SIMULATION - Behavioral Simulation - Functional - sim_1 - norgatetb
norgate.v
norgatetb.v
norgatetb_behav.wcfg
Scope
Sources
Objects
Protocol Instances
Name
Value
y
a
b
0
1
1
40,000 ps
39,995 ps
39,996 ps
39,997 ps
39,998 ps
39,999 ps
40,000 ps
40,001 ps
40,002 ps
40,003 ps
40,004 ps


norgate - [/home/akshay/norgate/norgate.xpr] - Vivado 2023.2
Quick Access
Project Summary
Device
norgate.v
norgatetb.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
see properties


norgate - [/home/akshay/norgate/norgate.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Summary
Settings
Summary (0.31 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.239 W)
Signals (0.007 W)
Data (0.007 W)
Logic (0.001 W)
I/O (0.231 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.31 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 26.6°C
Thermal Margin: 58.4°C
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find an invalid switching activity
On-Chip Power
77%
23%
Dynamic: 0.239 W (77%)
96%
Signals: 0.007 W (3%)
Logic: 0.001 W (1%)
I/O: 0.231 W (96%)
Device Static: 0.071 W (23%)
Estimated junction temperature.
Highlighted with orange when the estimated junction temperature exceeds the maximum value for the selected grade.
Estimates are calculated up to the absolute maximum temperature after which point 125+ is shown in red and the power and thermal estimates are no longer valid.
The background is blue when the user values is used.

Sol c.> EX-OR GATE

//EX-OR gate using Structural modeling

```
module xor_gate_s(a,b,y);
input a,b;
output y;
xor(y,a,b);
endmodule
```

//EX-OR gate using data flow modeling

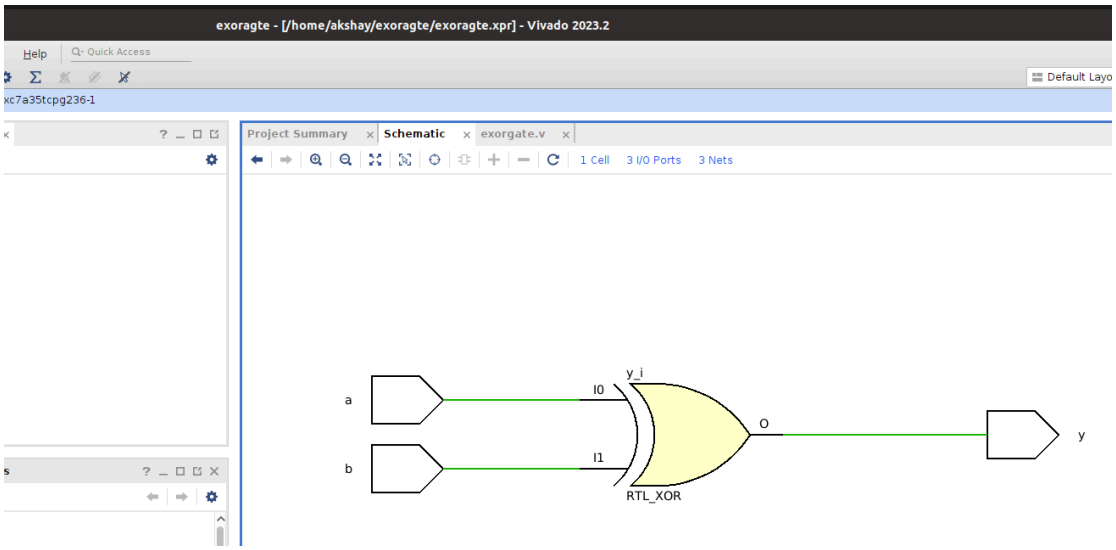
```
module xor_gate_d(a,b,y);
input a,b;
output y;
assign y = a ^ b;
endmodule
```

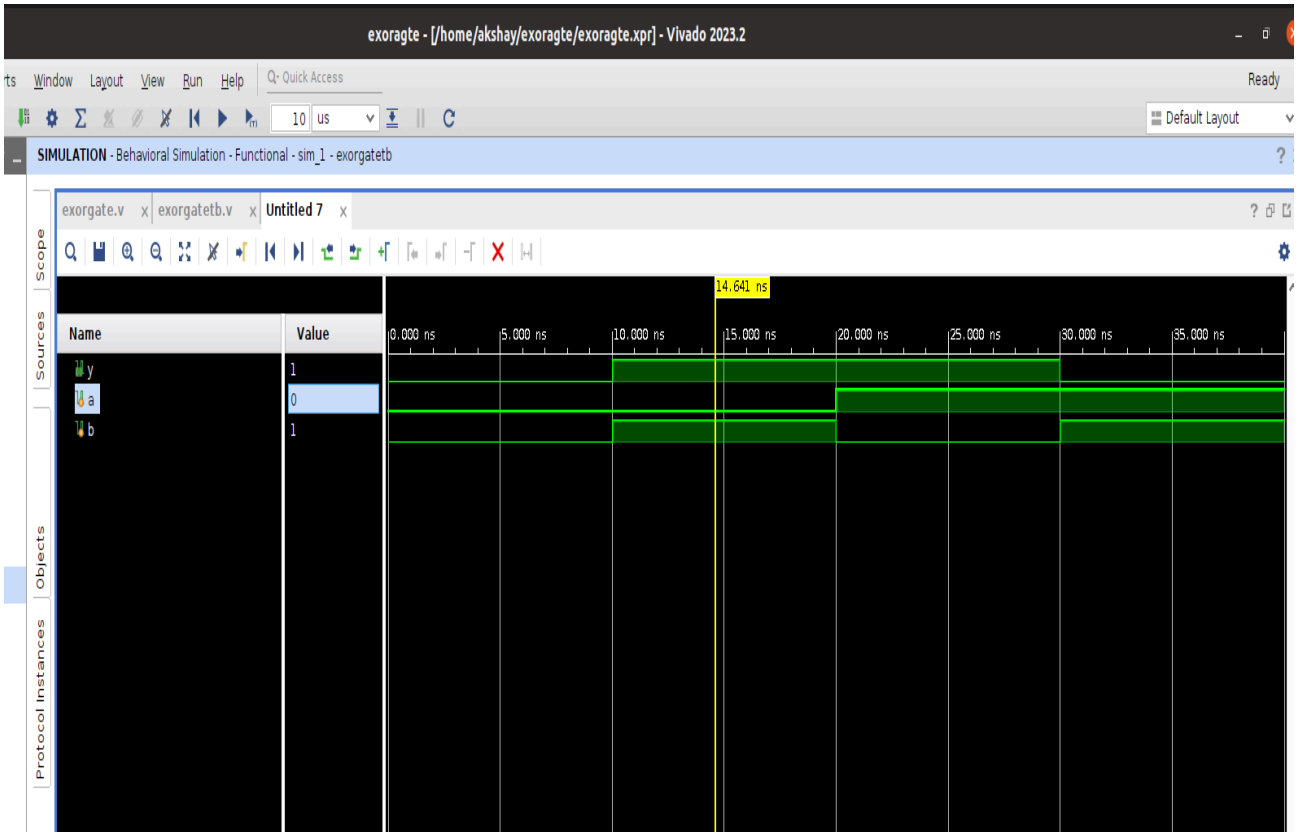
//EX-OR gate using behavioural modeling

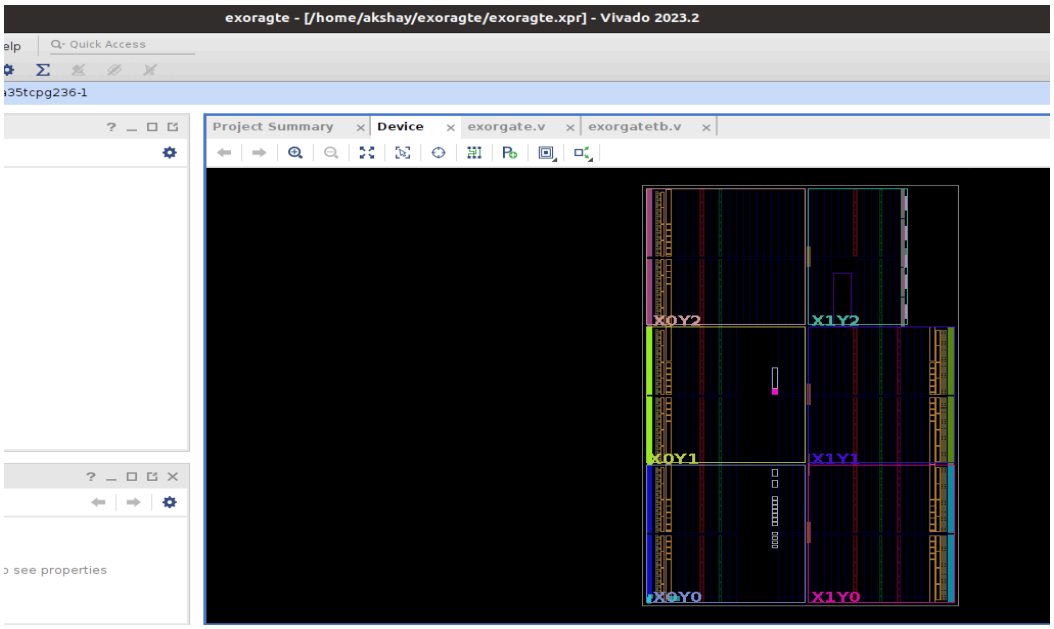
```
module xor_gate_b(a,b,y);
input a;
output reg y;
always @ (a,b)
y = a ^ b;
endmodule
```

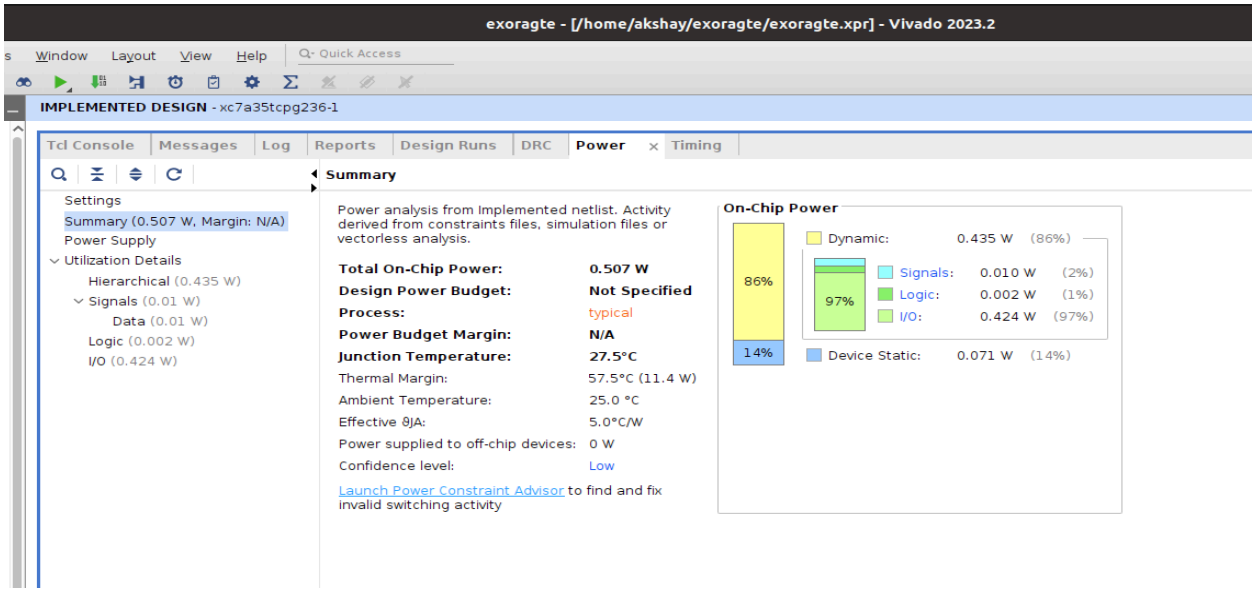
TESTBENCH CODE:

```
module xor_gate_tb;

reg a,b;

wire y;

xor_gate_s uut(a,b,y);

initial begin

a = 0; b = 0;

#10

b = 0; b = 1;

#10

a = 1; b = 0;

#10

b = 1; b = 1;

#10

$finish();

end

Endmodule
```




exoragte - [/home/akshay/exoragte/exoragte.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Ready
10
us
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - exorgatetb
exorgate.v
exorgatetb.v
Untitled 7
Scope
Sources
Objects
Protocol Instances
14.641 ns
Name
Value
y
a
b
1
0
1
0.000 ns
5.000 ns
10.000 ns
15.000 ns
20.000 ns
25.000 ns
30.000 ns
35.000 ns


exoragte - [/home/akshay/exoragte/exoragte.xpr] - Vivado 2023.2
Quick Access
Project Summary
Device
exorgate.v
exorgatetb.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
see properties



EX- NOR GATE:

//EX-NOR gate using Structural modeling

```
module xnor_gate_s(a,b,y);

input a,b;

output y;

xnor(y,a,b);

endmodule
```

//EX-NOR gate using data flow modeling

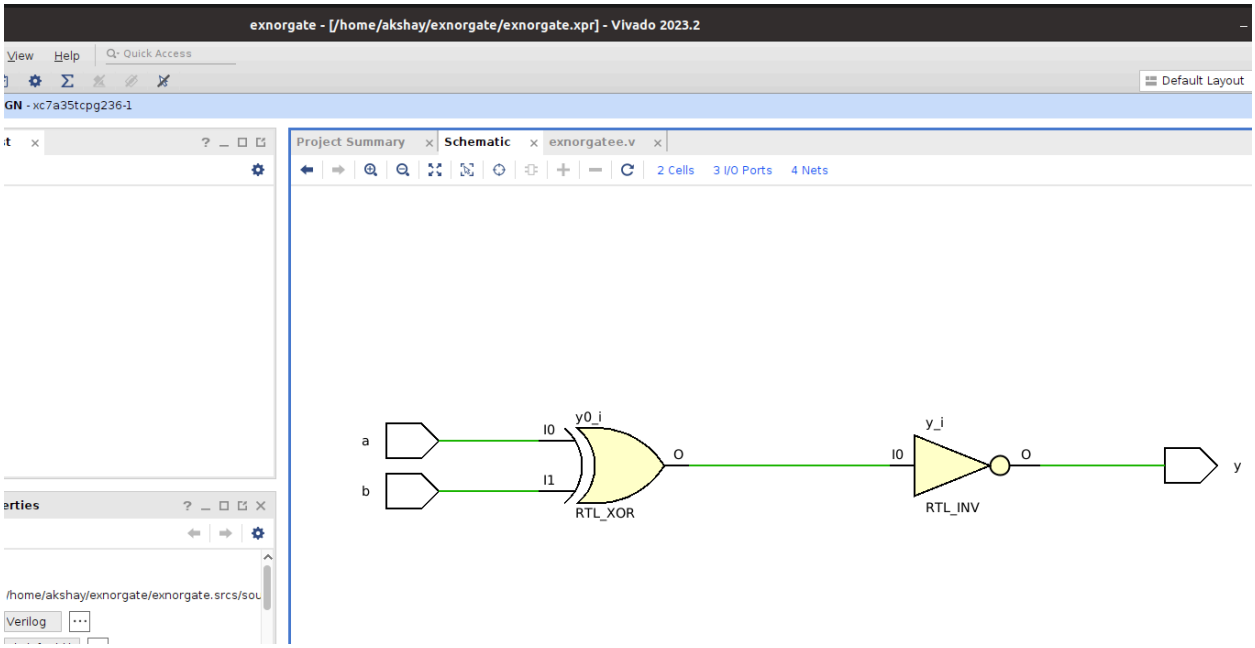
```
module xnor_gate_d(a,b,y);

input a,b;

output y;

assign y = ~(a ^ b);

Endmodule
```

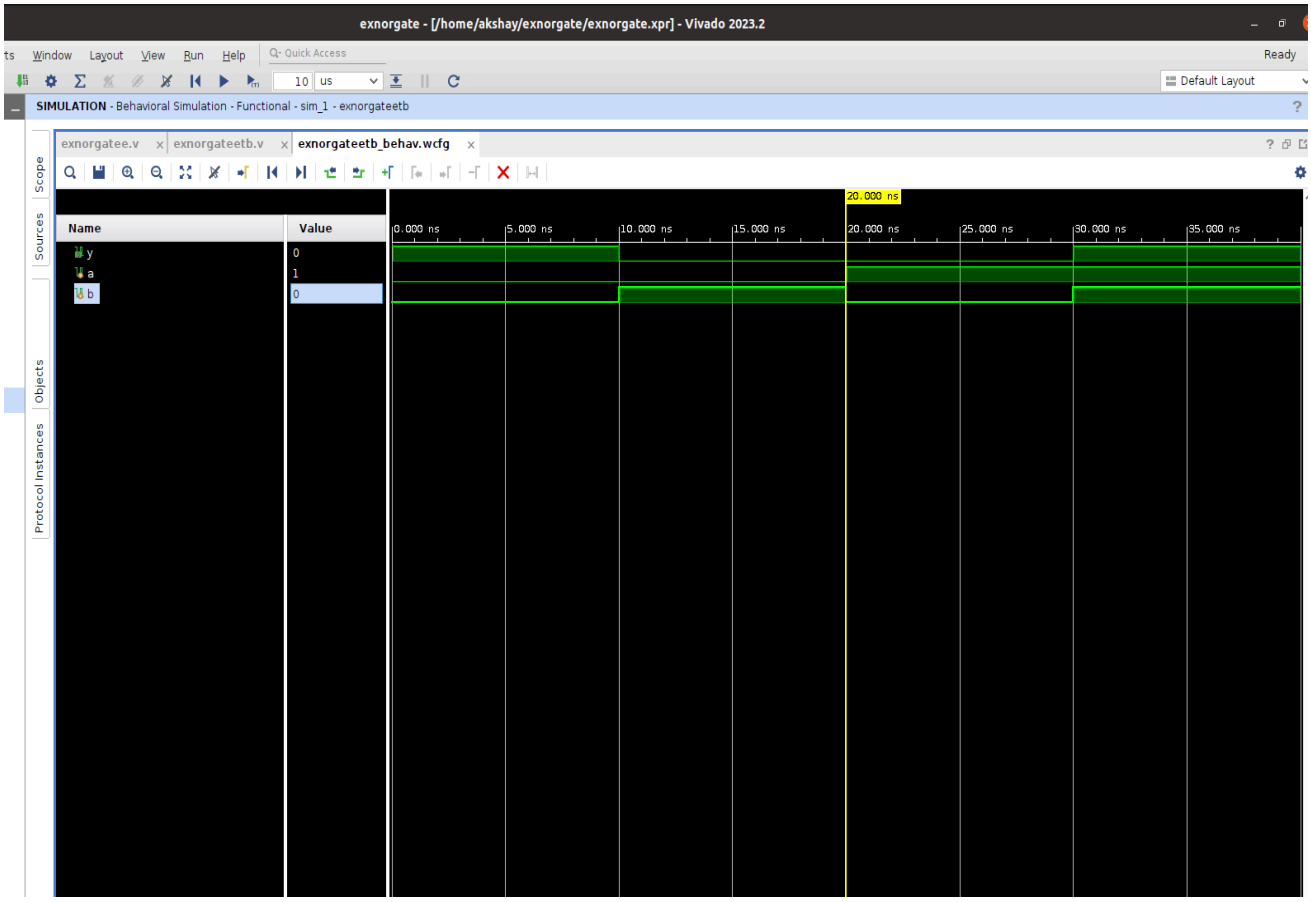
//EX-NOR gate using behavioural modeling

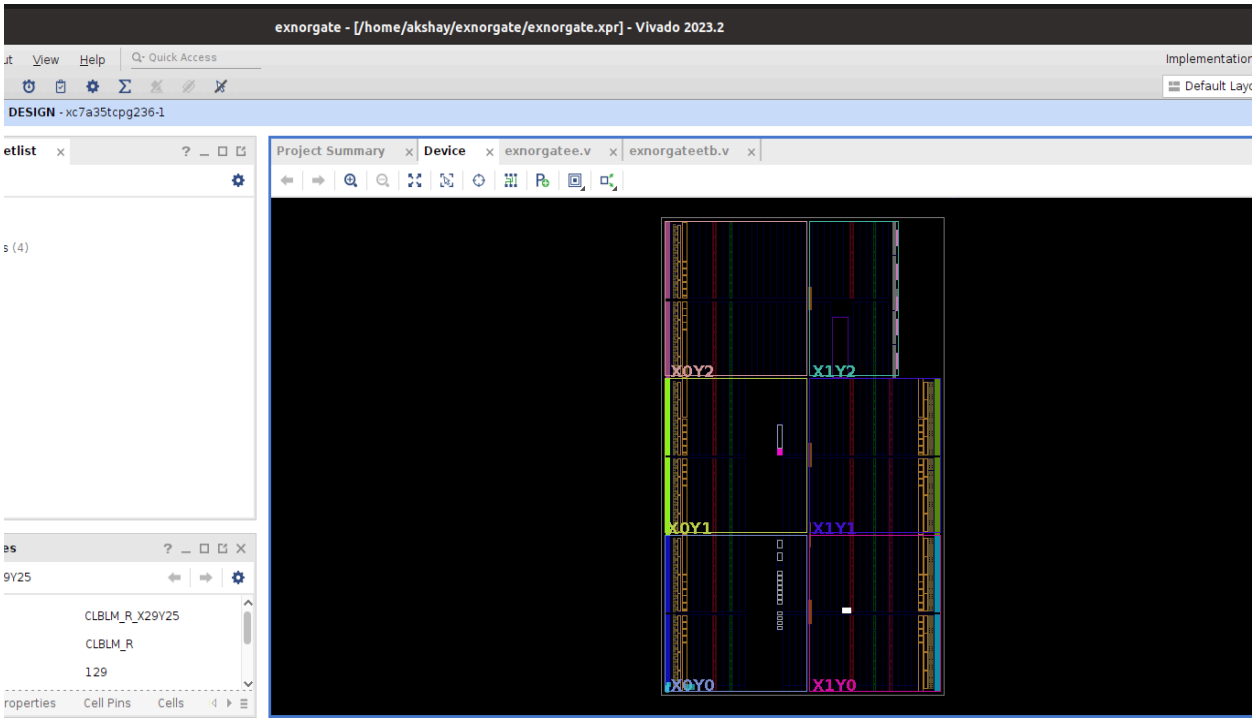
```
module xor_gate_b(a,b,y);
input a;
output reg y;
always @ (a,b)
y = ~(a ^ b);
endmodule
```

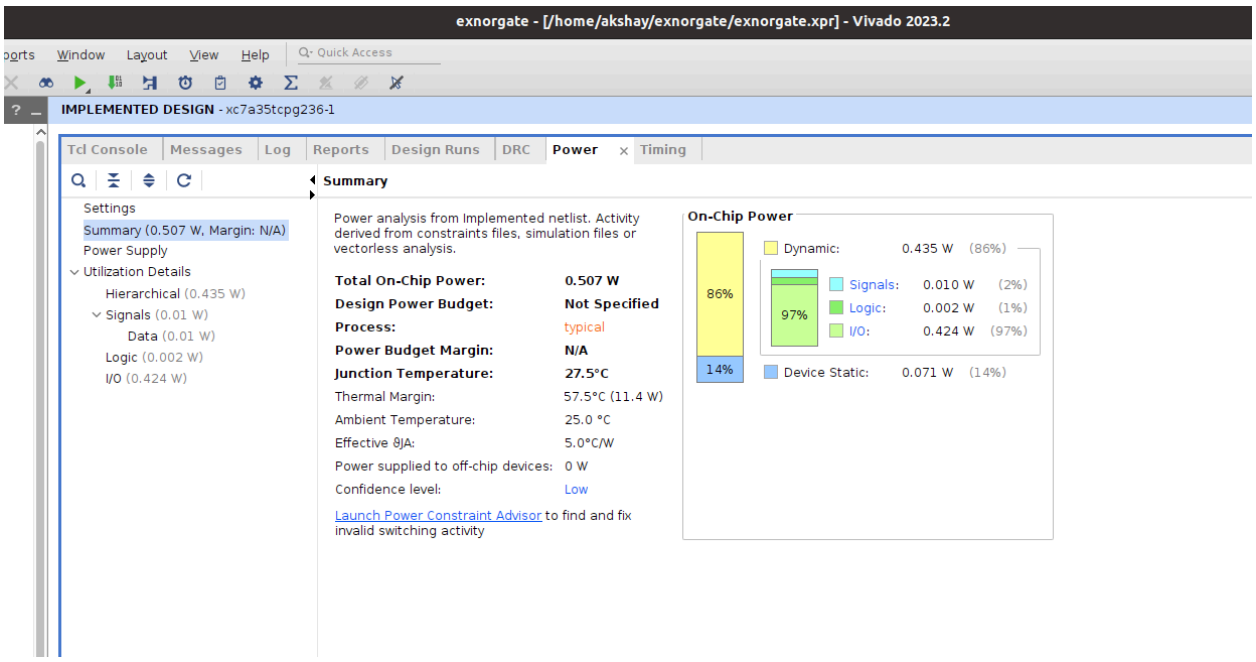
TESTBENCH CODE:

```
module xnor_gate_tb;
reg a,b;
wire y;
xnor_gate_s uut(a,b,y);
initial begin
a = 0; b = 0;
#10
b = 0; b = 1;
#10
a = 1; b = 0;
#10
b = 1; b = 1;
#10
$finish();
end
Endmodule
```


exnorgate - [/home/akshay/exnorgate/exnorgate.xpr] - Vivado 2023.2
View
Help
Quick Access
Default Layout
GN - xc7a35tcpg236-1
Project Summary
Schematic
exnorgatee.v
2 Cells
3 I/O Ports
4 Nets
a
b
I0
I1
y0_i
O
RTL_XOR
y_i
I0
O
RTL_INV
y
erties
/home/akshay/exnorgate/exnorgate.srcs/sou
Verilog


exnorgate - [/home/akshay/exnorgate/exnorgate.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Ready
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - exnorgateetb
exnorgatee.v
exnorgateetb.v
exnorgateetb_behav.wcfg
Scope
Sources
Objects
Protocol Instances
Name
Value
y
a
b
0
1
0
0.000 ns
5.000 ns
10.000 ns
15.000 ns
20.000 ns
25.000 ns
30.000 ns
35.000 ns
20.000 ns


exnorgate - [/home/akshay/exnorgate/exnorgate.xpr] - Vivado 2023.2
View
Help
Quick Access
DESIGN - xc7a35tcpg236-1
Project Summary
Device
exnorgatee.v
exnorgateetb.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
CLBLM_R_X29Y25
CLBLM_R
129
Cell Pins
Cells


exnorgate - [/home/akshay/exnorgate/exnorgate.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Settings
Summary (0.507 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.435 W)
Signals (0.01 W)
Data (0.01 W)
Logic (0.002 W)
I/O (0.424 W)
Summary
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.507 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 27.5°C
Thermal Margin: 57.5°C (11.4 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
86%
14%
97%
Dynamic: 0.435 W (86%)
Signals: 0.010 W (2%)
Logic: 0.002 W (1%)
I/O: 0.424 W (97%)
Device Static: 0.071 W (14%)

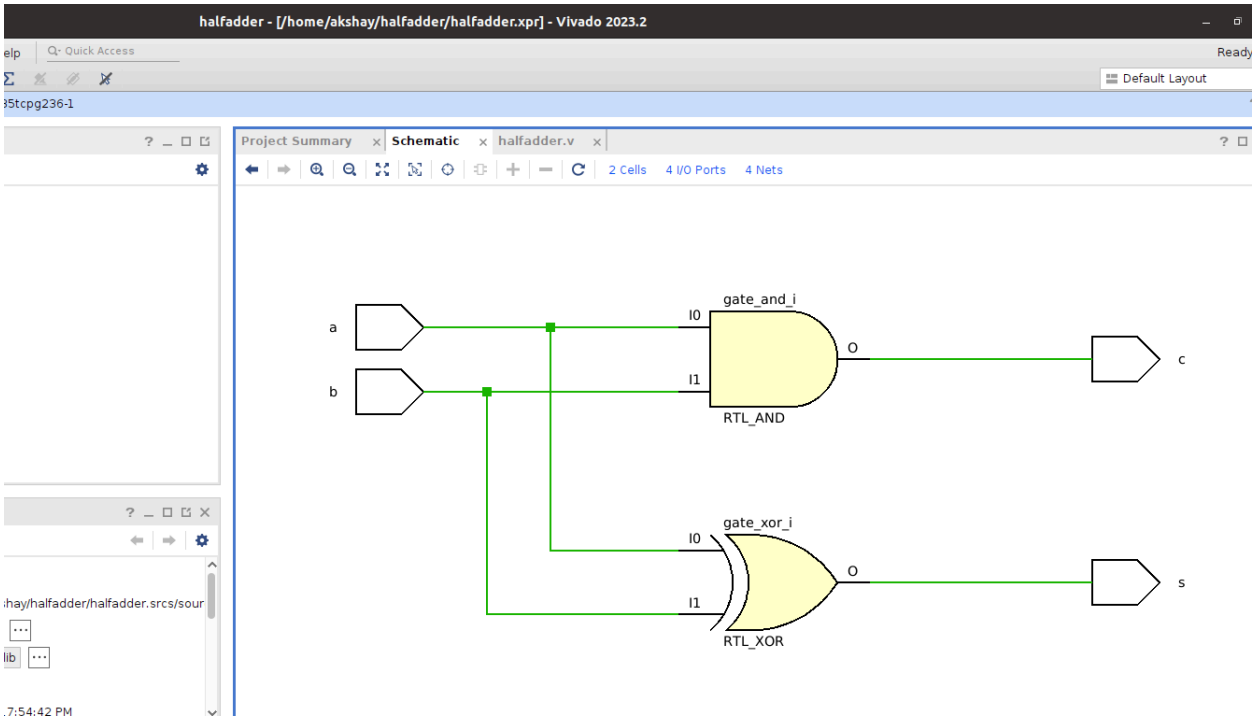
Assignment-2 (Combinational Circuits)

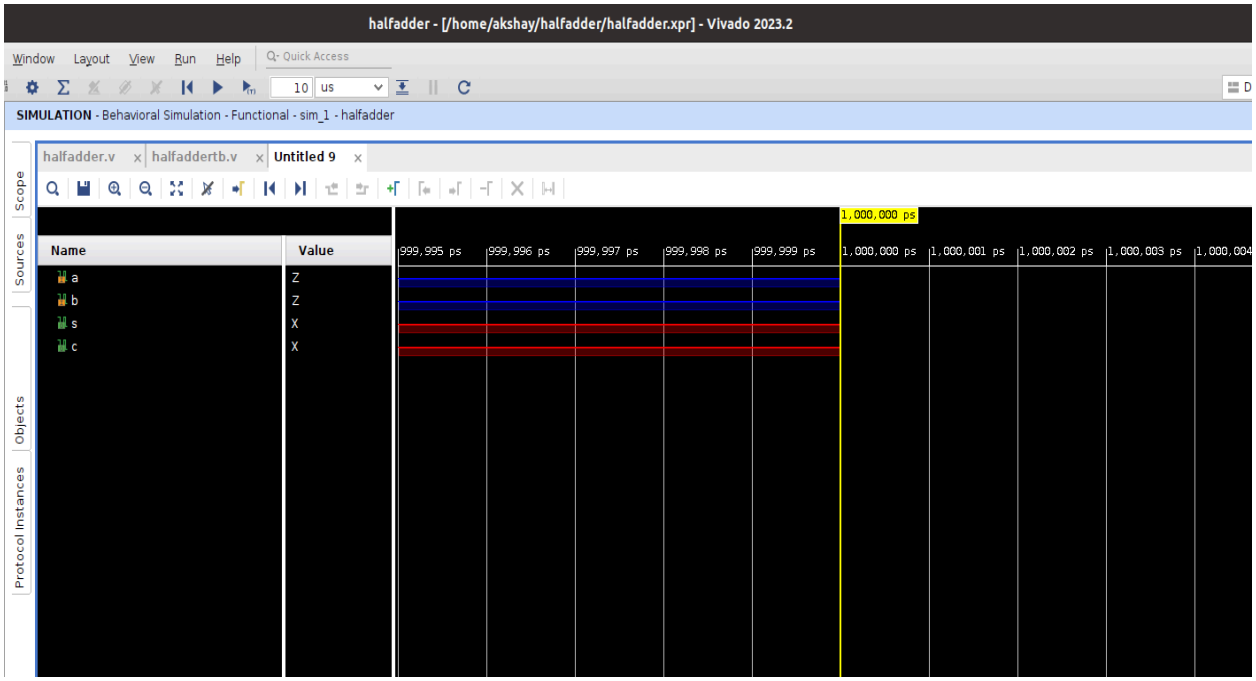
Q.2 Write a Verilog Code for Half-Adder.

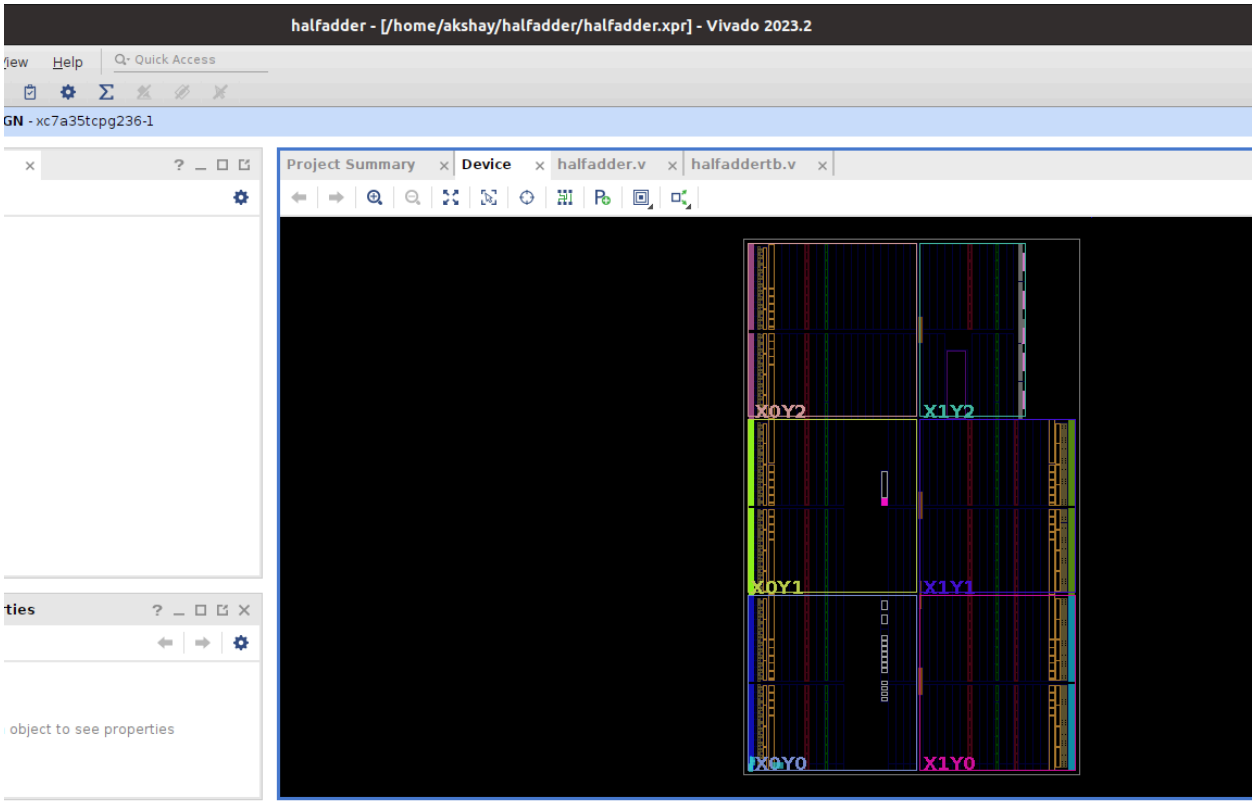
```
module half_adder_structural (
input a, // Input 'a'
input b, // Input 'b'
output s, // Output 's' (Sum)
output c // Output 'c' (Carry)
);
xor gate_xor (s, a, b); // XOR gate for sum
and gate_and (c, a, b); // AND gate for carry
endmodule
```

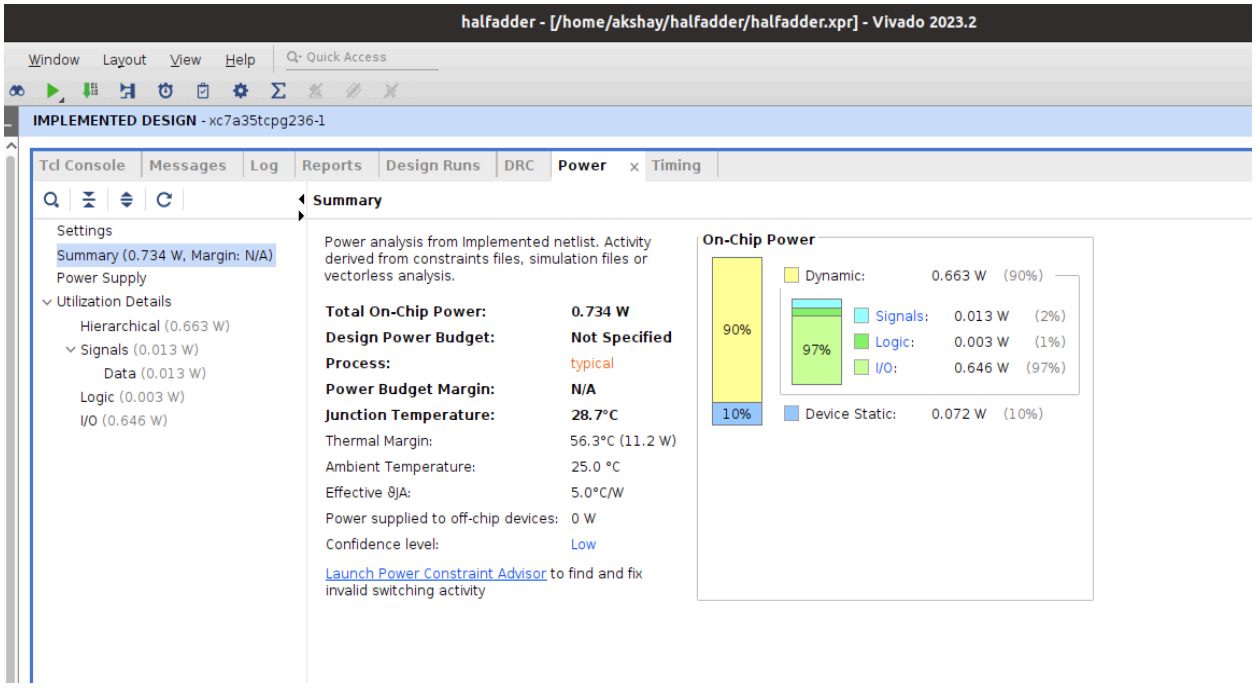
Testbench Code

```
module tb_top;
  reg a, b;
  wire s, c;
   half_adder ha(a, b, s, c);
  initial begin
    $monitor("At time %0t: a=%b b=%b, sum=%b, carry=%b",$time, a,b,s,c);
    a = 0; b = 0; #1;
    a = 0; b = 1; #1;
    a = 1; b = 0; #1;
    a = 1; b = 1;
  end
Endmodule
```


halfadder - [/home/akshay/halfadder/halfadder.xpr] - Vivado 2023.2
Quick Access
Ready
Default Layout
Project Summary
Schematic
halfadder.v
2 Cells
4 I/O Ports
4 Nets
a
b
gate_and_i
I0
I1
O
RTL_AND
c
gate_xor_i
I0
I1
O
RTL_XOR
s


halfadder - [/home/akshay/halfadder/halfadder.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
SIMULATION - Behavioral Simulation - Functional - sim_1 - halfadder
halfadder.v
halfaddertb.v
Untitled 9
Scope
Sources
Objects
Protocol Instances
Name
Value
a
b
s
c
Z
Z
X
X
1,000,000 ps
999,995 ps
999,996 ps
999,997 ps
999,998 ps
999,999 ps
1,000,000 ps
1,000,001 ps
1,000,002 ps
1,000,003 ps


halfadder - [/home/akshay/halfadder/halfadder.xpr] - Vivado 2023.2
Help
Quick Access
GN - xc7a35tcpg236-1
Project Summary
Device
halfadder.v
halfaddertb.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
ties
object to see properties


halfadder - [/home/akshay/halfadder/halfadder.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Summary
Settings
Summary (0.734 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.663 W)
Signals (0.013 W)
Data (0.013 W)
Logic (0.003 W)
I/O (0.646 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.734 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 28.7°C
Thermal Margin: 56.3°C (11.2 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
90%
10%
97%
Dynamic: 0.663 W (90%)
Signals: 0.013 W (2%)
Logic: 0.003 W (1%)
I/O: 0.646 W (97%)
Device Static: 0.072 W (10%)

Q.3 Write a Verilog Code For Full adder.

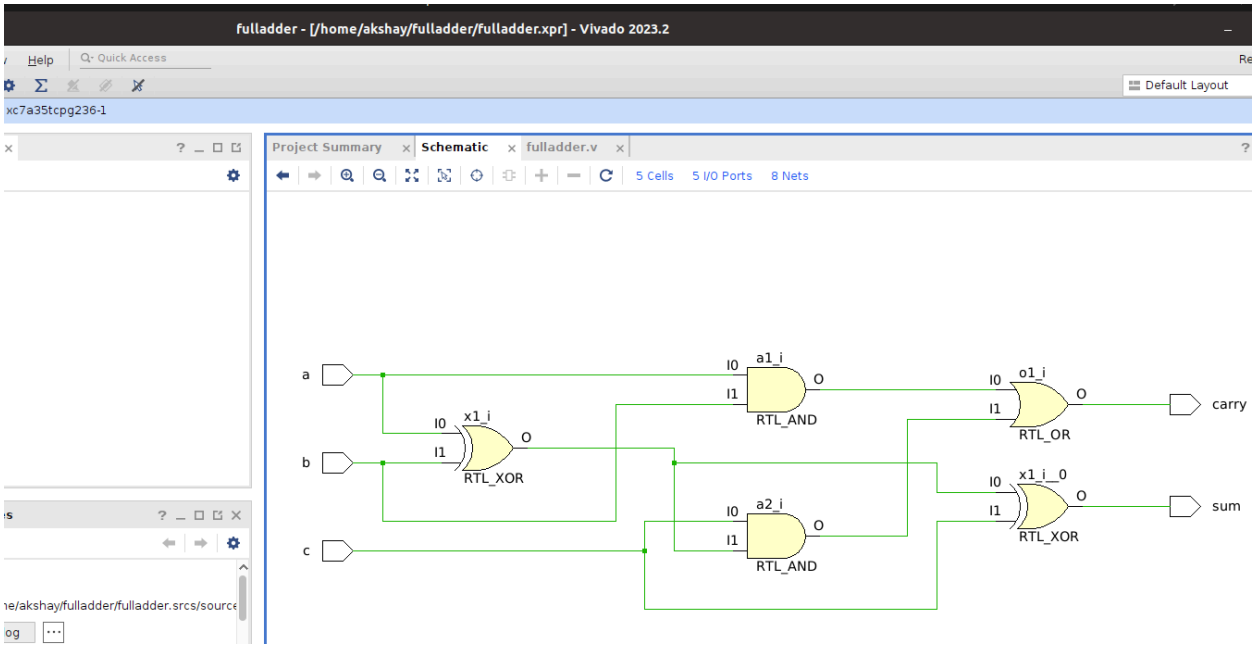
```
//module fulladder(
//    input a,b,c,
//    output sum , carry
//    );
//    assign sum= (a^b^c);
//  assign carry= ((a&b)|(b&c)|(c&a));
//endmodule


//module fulladder(
//    input a,b,c,
//    output reg sum , carry
//    );
//     always @(*) begin
//    case ({a,b,c})
//      3'b000: begin sum = 0;carry =0 ;end
//      3'b001: begin sum = 1;carry =0 ;end
//      3'b010: begin sum = 1;carry =0 ;end
//      3'b011: begin sum = 0;carry =1 ;end
//      3'b100: begin sum = 1;carry =0 ;end
//      3'b101: begin sum = 0;carry =1 ;end
//      3'b110: begin sum = 0;carry =1 ;end
//      3'b111: begin sum = 1;carry =1 ;end
//      default begin sum = 0;carry =0 ;end
```

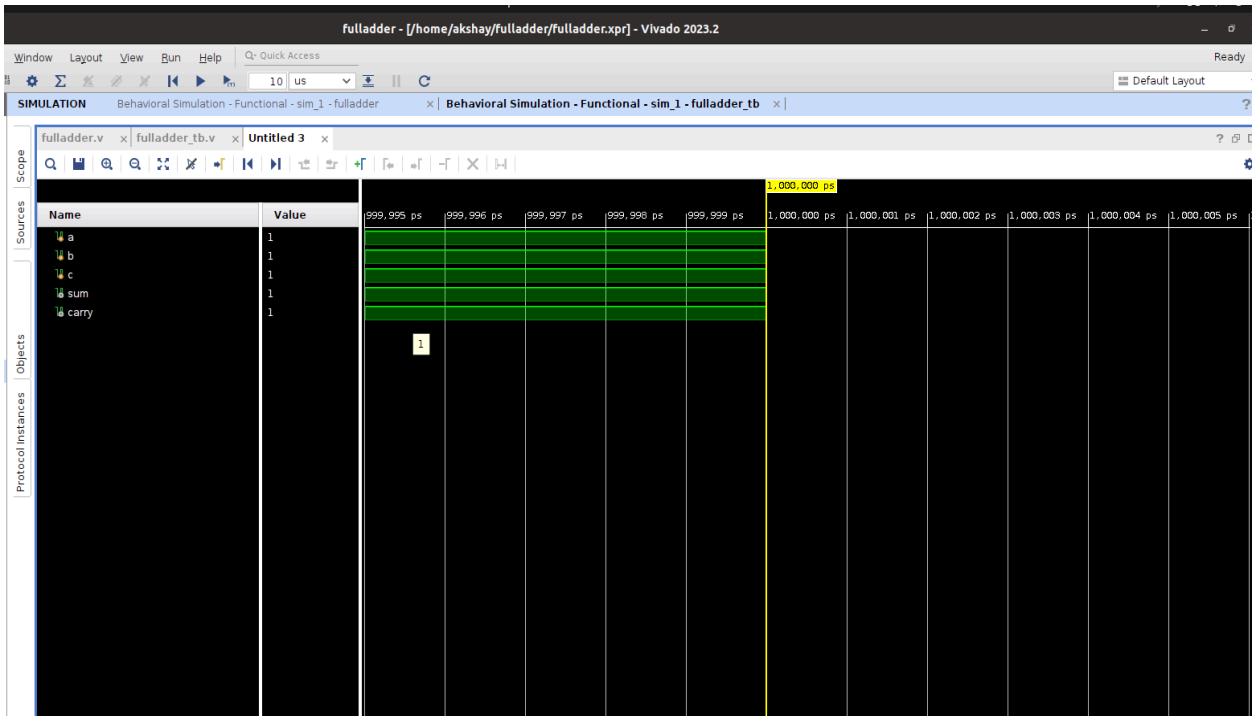
```
//    endcase
//    end
//endmodule


module fulladder(
    input a,b,c,
    output  sum , carry
    );
  wire w1,w2,w3;
  xor x1(sum, a,b,c);
   and a1(w1,a,b);
  xor x2(w2,a,b);
  and a2(w3,c,w2);
  or o1(carry,w1,w3);
 endmodule
```

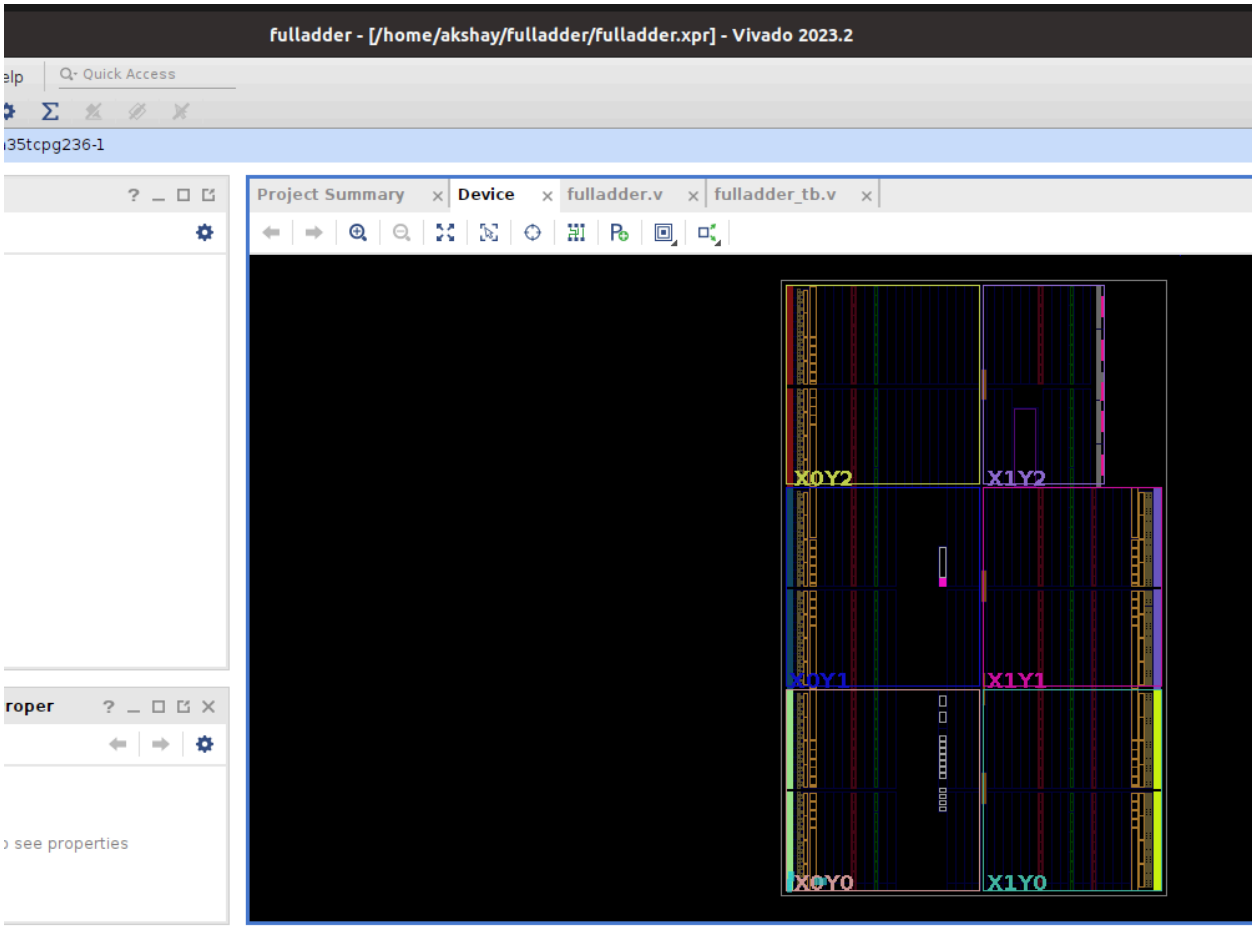
Testbench Code:

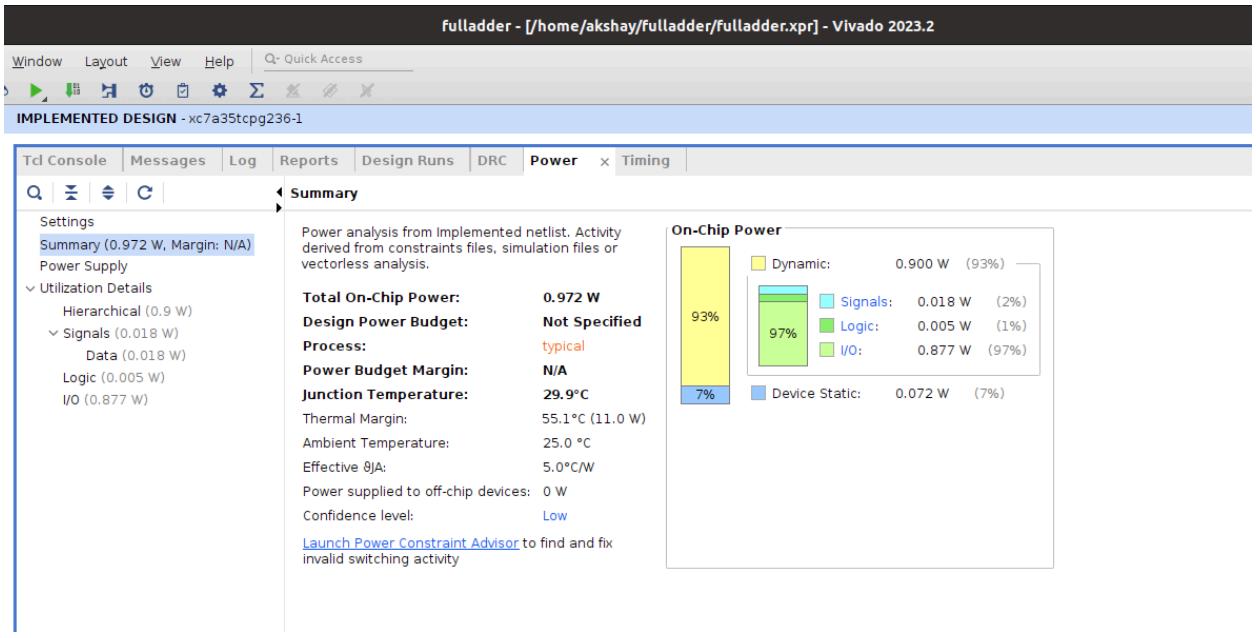
```
module fulladder_tb(


    );
    reg a,b,c;
  wire sum,carry;
  fulladder dut(a,b,c,sum,carry);
  initial begin;
    a=0; b=0 ; c=0;
```

```
   #10;
    a=0; b=0; c=1;
    #10;
    a=0; b=1; c=0;
    #10;
    a=0; b=1; c=1;
    #10;
    a=1; b=0 ;c=0;
    #10;
    a=1; b=0; c=1;
    #10;
    a=1; b=1; c=0;
    #10;
    a=1; b=1; c=1;
    #10;
  end
  initial $monitor("a=%d, b=%d, c=%d, sum=%d, carry=%d ", a,b,c,sum,carry);
endmodule
```


fulladder - [/home/akshay/fulladder/fulladder.xpr] - Vivado 2023.2
Help
Quick Access
Default Layout
xc7a35tcpg236-1
Project Summary
Schematic
fulladder.v
5 Cells
5 I/O Ports
8 Nets
a
b
c
x1_i
RTL_XOR
a1_i
RTL_AND
a2_i
RTL_AND
o1_i
RTL_OR
x1_i_0
RTL_XOR
carry
sum


fulladder - [/home/akshay/fulladder/fulladder.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Ready
Default Layout
SIMULATION
Behavioral Simulation - Functional - sim_1 - fulladder
Behavioral Simulation - Functional - sim_1 - fulladder_tb
fulladder.v
fulladder_tb.v
Untitled 3
Scope
Sources
Objects
Protocol Instances
Name
Value
a
b
c
sum
carry
1
999,995 ps
999,996 ps
999,997 ps
999,998 ps
999,999 ps
1,000,000 ps
1,000,001 ps
1,000,002 ps
1,000,003 ps
1,000,004 ps
1,000,005 ps


fulladder - [/home/akshay/fulladder/fulladder.xpr] - Vivado 2023.2
Quick Access
35tcpg236-1
Project Summary
Device
fulladder.v
fulladder_tb.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
roper
see properties


fulladder - [/home/akshay/fulladder/fulladder.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Summary
Settings
Summary (0.972 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.9 W)
Signals (0.018 W)
Data (0.018 W)
Logic (0.005 W)
I/O (0.877 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.972 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 29.9°C
Thermal Margin: 55.1°C (11.0 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
93%
7%
97%
Dynamic: 0.900 W (93%)
Signals: 0.018 W (2%)
Logic: 0.005 W (1%)
I/O: 0.877 W (97%)
Device Static: 0.072 W (7%)

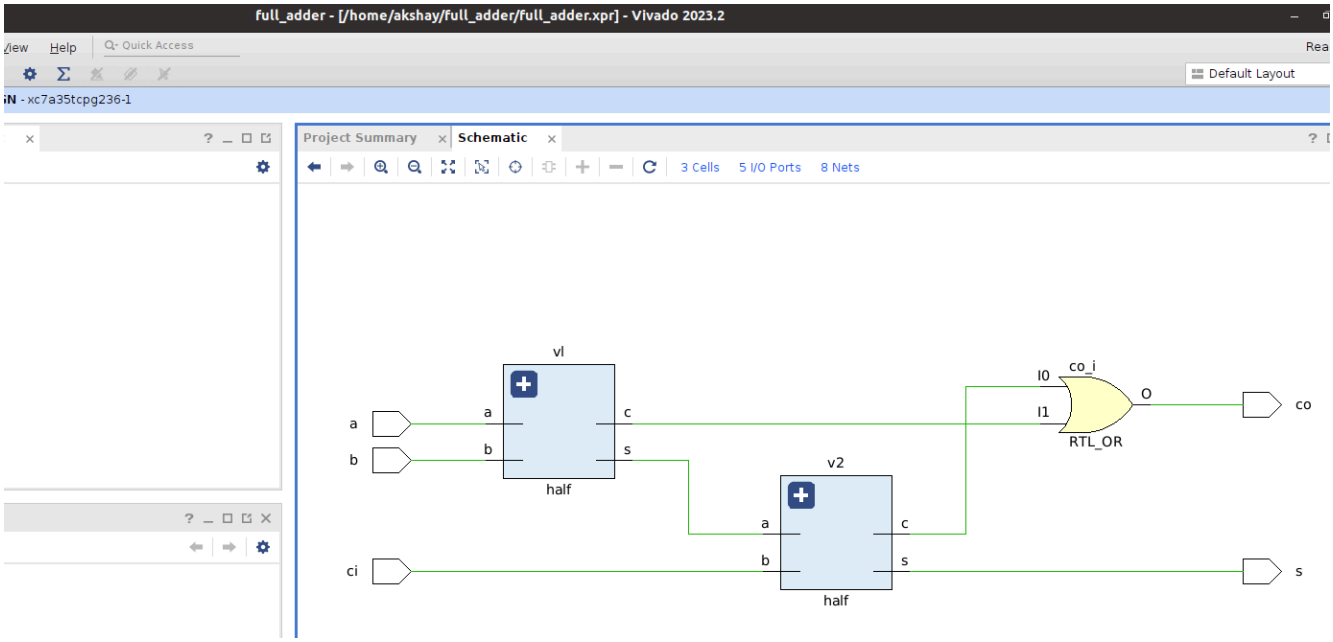
Q.4 Write a Verilog Code for full adder using Half-adder.

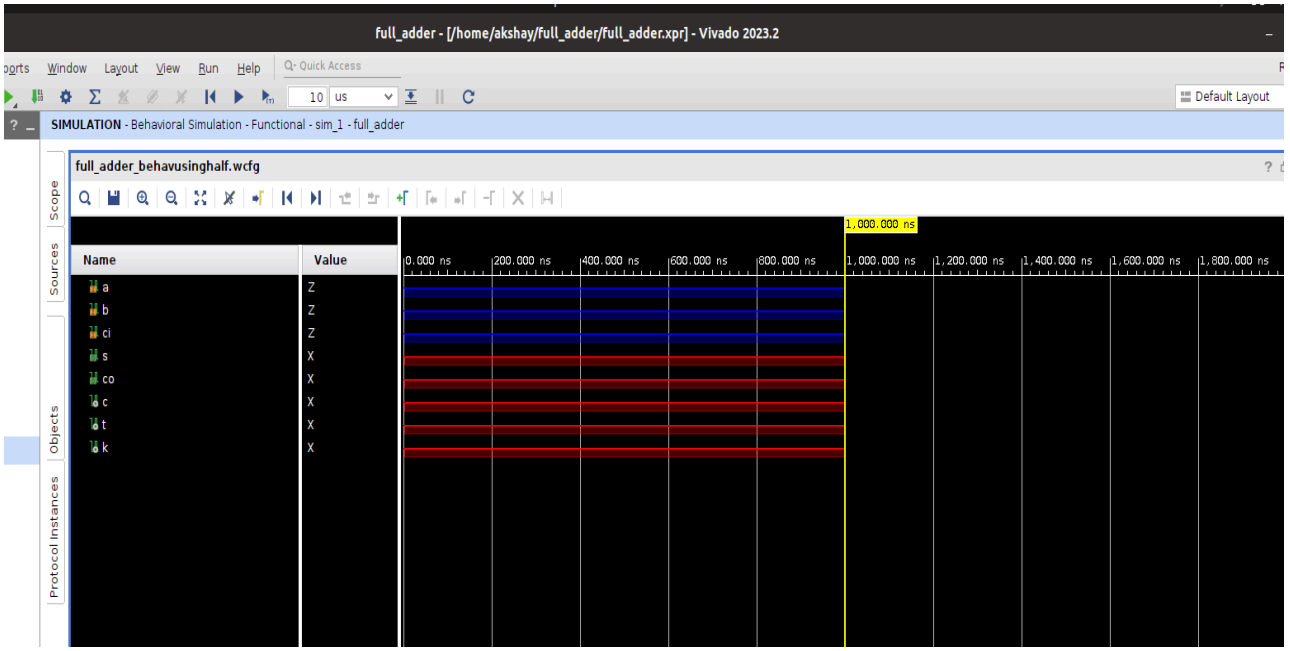
```
// Code your design here

module full_adder(s,co,a,b,ci);

input a,b,ci;

output s,co;

wire c,t,k;

half vl(t,c,a,b);

half v2 (s,k,t,ci);

or (co,k, c);

endmodule

module half(s,c,a,b);

input a,b;

output s,c;

assign s=a^b;

assign c=a&b;

endmodule
```

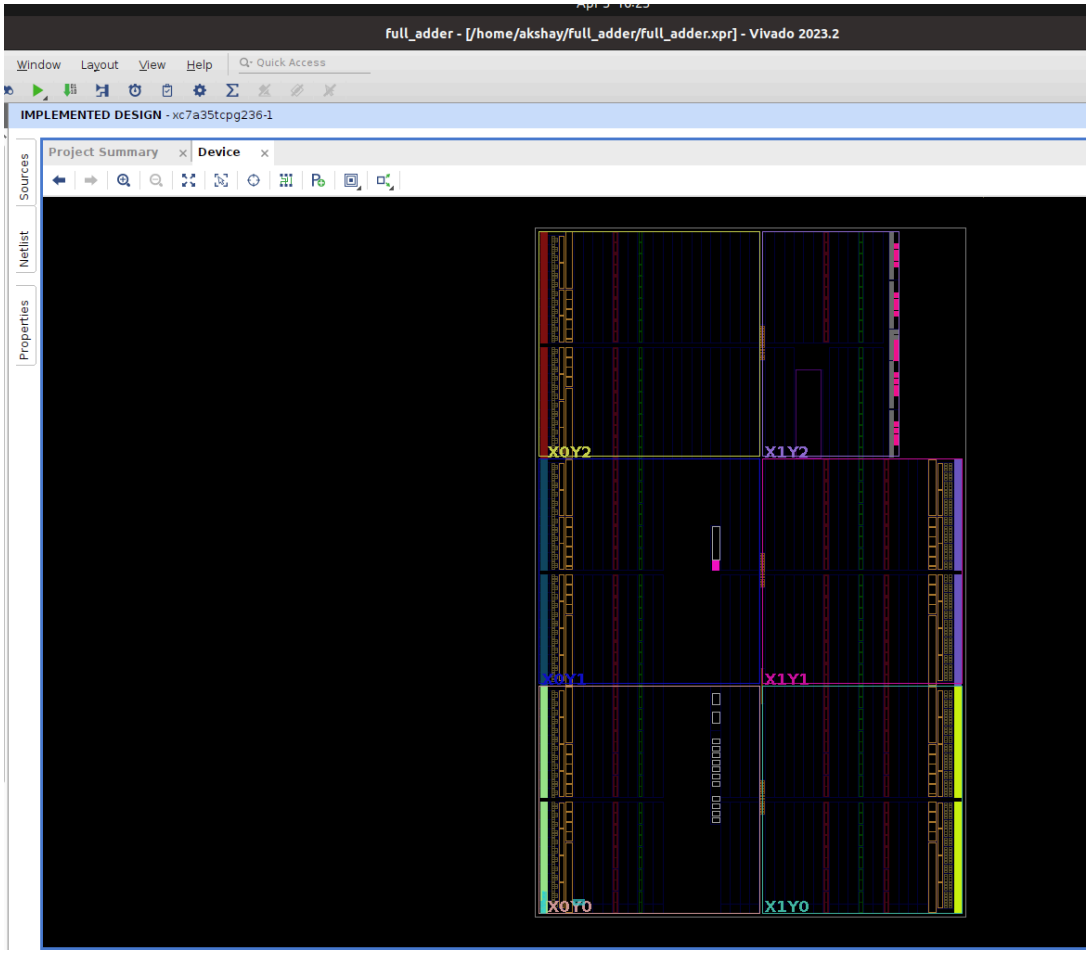
Testbench:

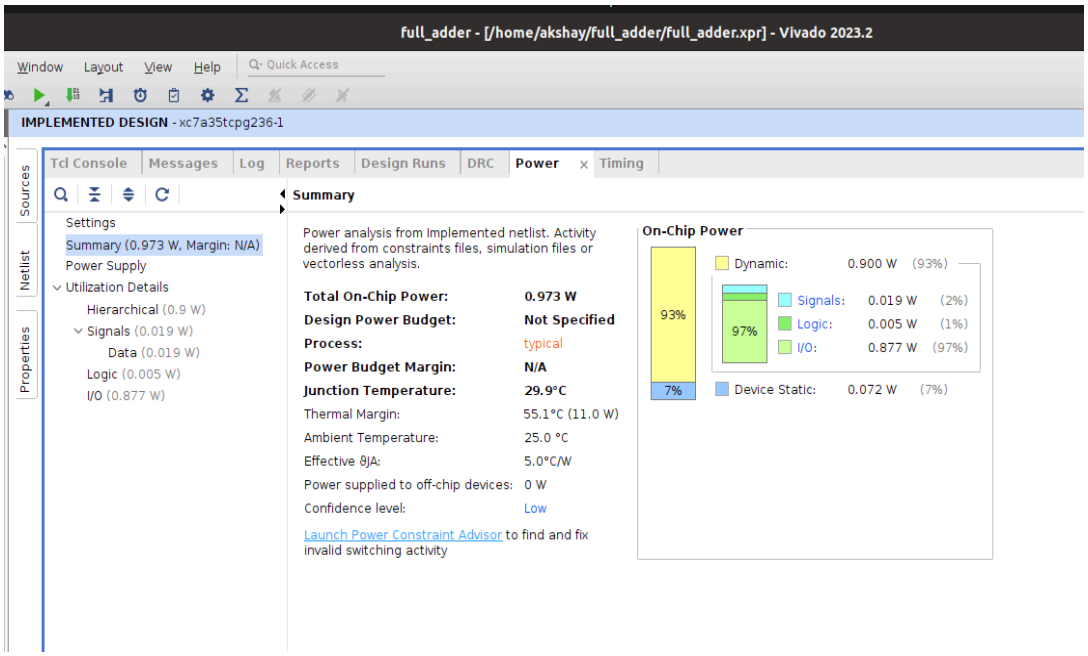
```
module full_adder_tb;

reg a,b,ci;

wire s,co;


full_adder uut(a,b,ci,s,co);


initial begin
```

```
a = 0; b = 0; ci = 0;

#10

a = 0; b = 0; ci = 1;

#10

a = 0; b = 1; ci = 0;

#10

a = 0; b = 1; ci = 1;

#10

a = 1; b = 0; ci = 0;

#10

a = 1; b = 0; ci = 1;

#10

a = 1; b = 1; ci = 0;

#10

a = 1; b = 1; ci = 1;

#10

$finish();

end

            endmodule
```


full_adder - [/home/akshay/full_adder/full_adder.xpr] - Vivado 2023.2
Default Layout
Project Summary
Schematic
3 Cells
5 I/O Ports
8 Nets
v1
a
b
c
s
half
v2
a
b
c
s
half
ci
co_i
I0
I1
O
RTL_OR
co
s


full_adder - [/home/akshay/full_adder/full_adder.xpr] - Vivado 2023.2
SIMULATION - Behavioral Simulation - Functional - sim_1 - full_adder
full_adder_behavusinghalf.wcfg
Name
Value
a
b
ci
s
co
c
t
k
Z
Z
Z
X
X
X
X
X
1,000.000 ns
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns
1,200.000 ns
1,400.000 ns
1,600.000 ns
1,800.000 ns
Scope
Sources
Objects
Protocol Instances


full_adder - [/home/akshay/full_adder/full_adder.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Project Summary
Device
Sources
Netlist
Properties
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0

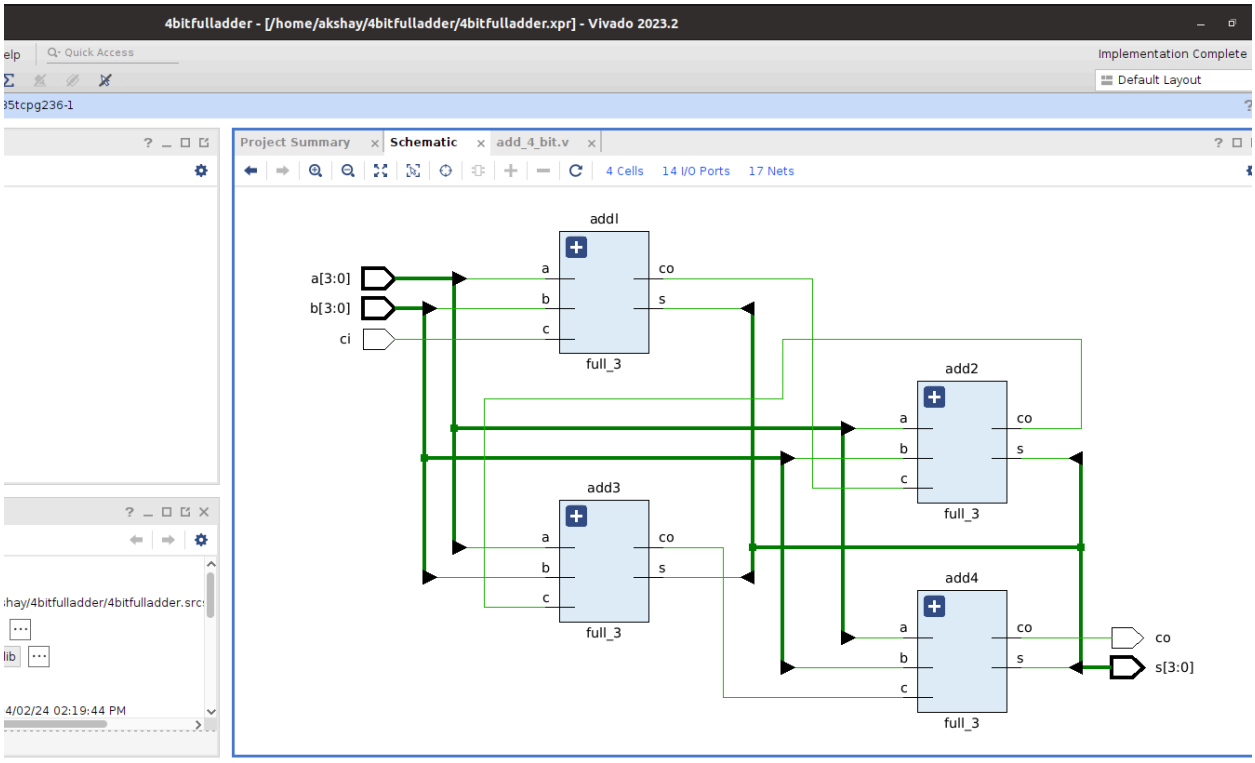

full_adder - [/home/akshay/full_adder/full_adder.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Sources
Netlist
Properties
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Settings
Summary (0.973 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.9 W)
Signals (0.019 W)
Data (0.019 W)
Logic (0.005 W)
I/O (0.877 W)
Summary
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.973 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 29.9°C
Thermal Margin: 55.1°C (11.0 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
93%
7%
97%
Dynamic: 0.900 W (93%)
Signals: 0.019 W (2%)
Logic: 0.005 W (1%)
I/O: 0.877 W (97%)
Device Static: 0.072 W (7%)

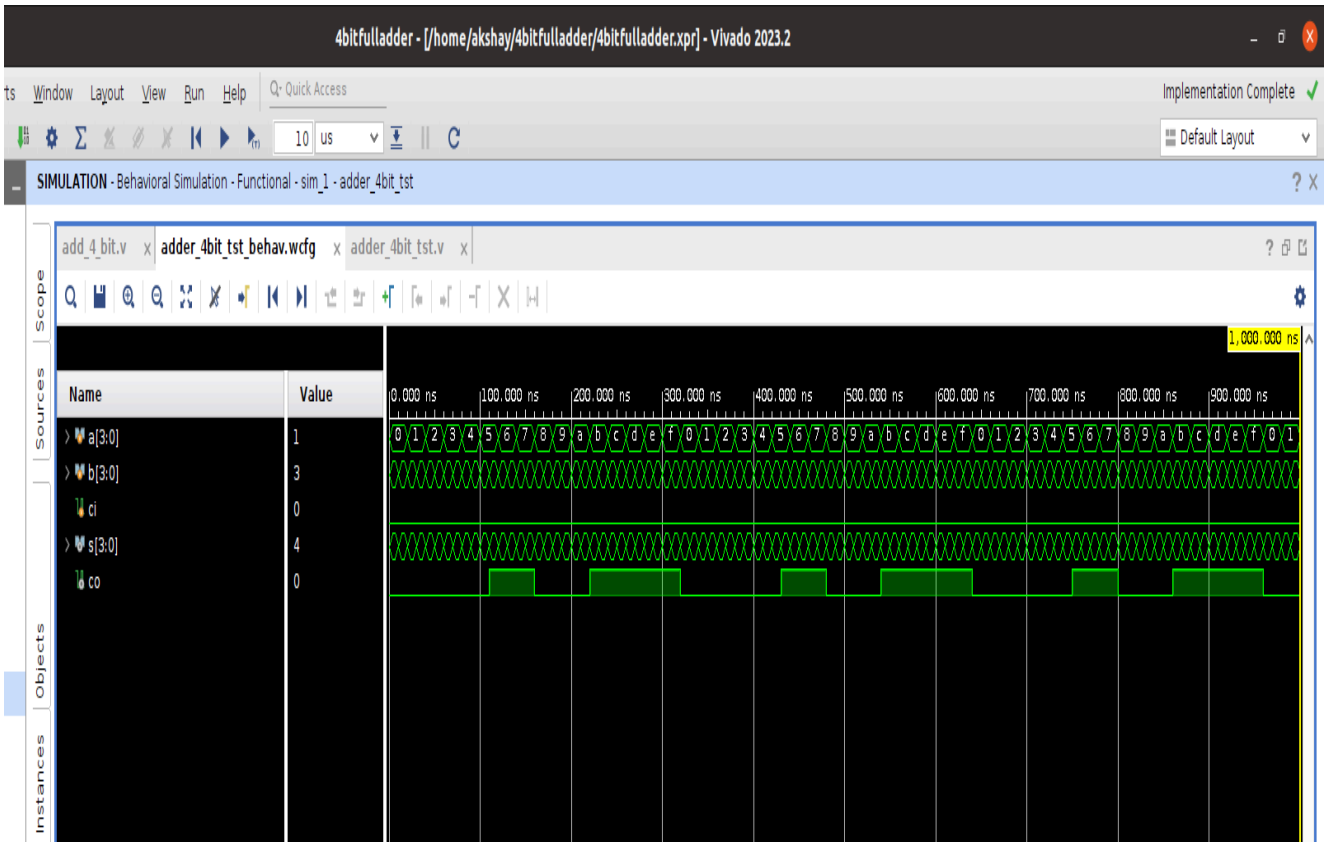
Q.5 Write a Verilog Code for 4-bit full adder.

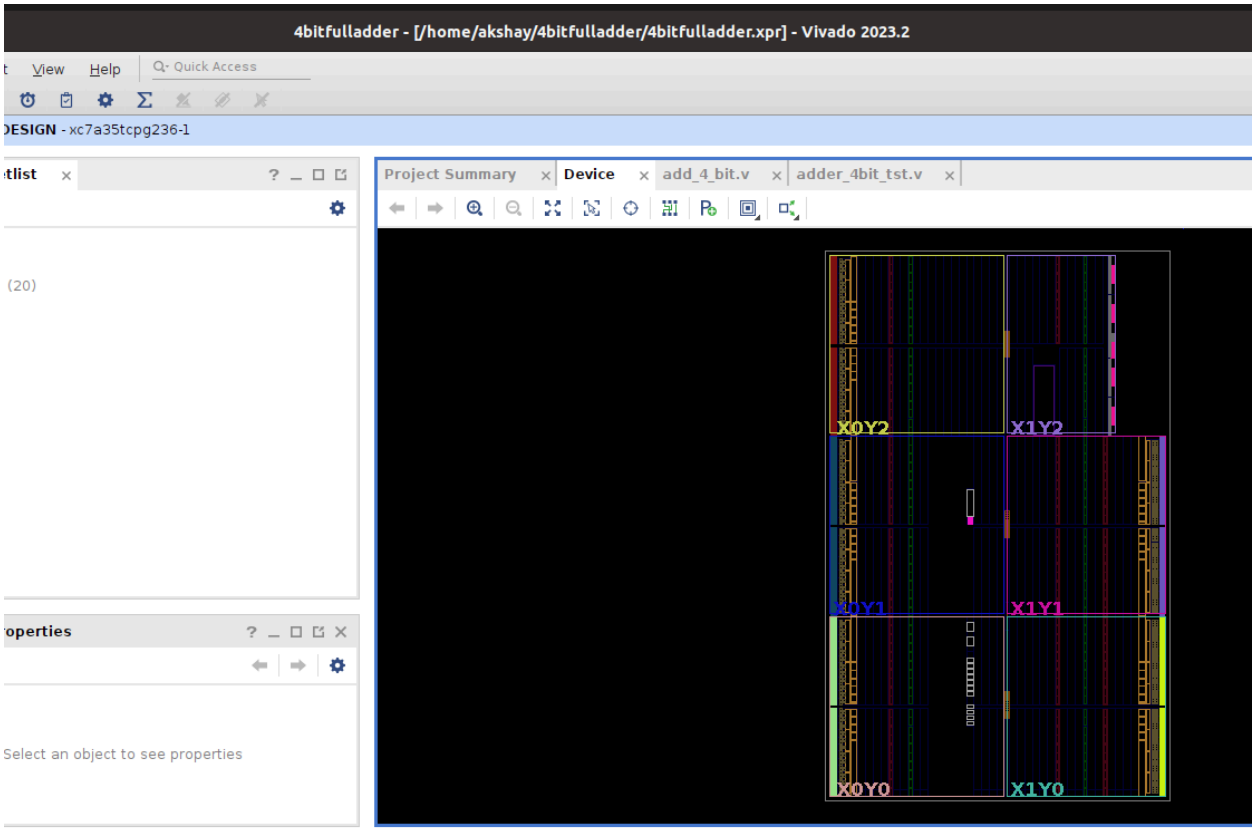
```
module add_4_bit(s,co, a,b,ci);
output [3:0]s;
output co;
wire [2:0]c;
input [3:0]a,b;
input ci;
full_3 addl(s[0],c[0],a[0],b[0],ci);
full_3 add2(s[1],c[1],a[1],b[1],c[0]);
full_3 add3(s[2],c[2],a[2],b[2],c[1]);
full_3 add4(s[3], co,a[3],b[3],c[2]);
endmodule
module full_3(s,co,a,b,c);
input a,b,c;
output reg s,co; always @ (*)
begin
s=a^b^c;
co=(a&b)|(b&c)|(a&c);
end
Endmodule
```

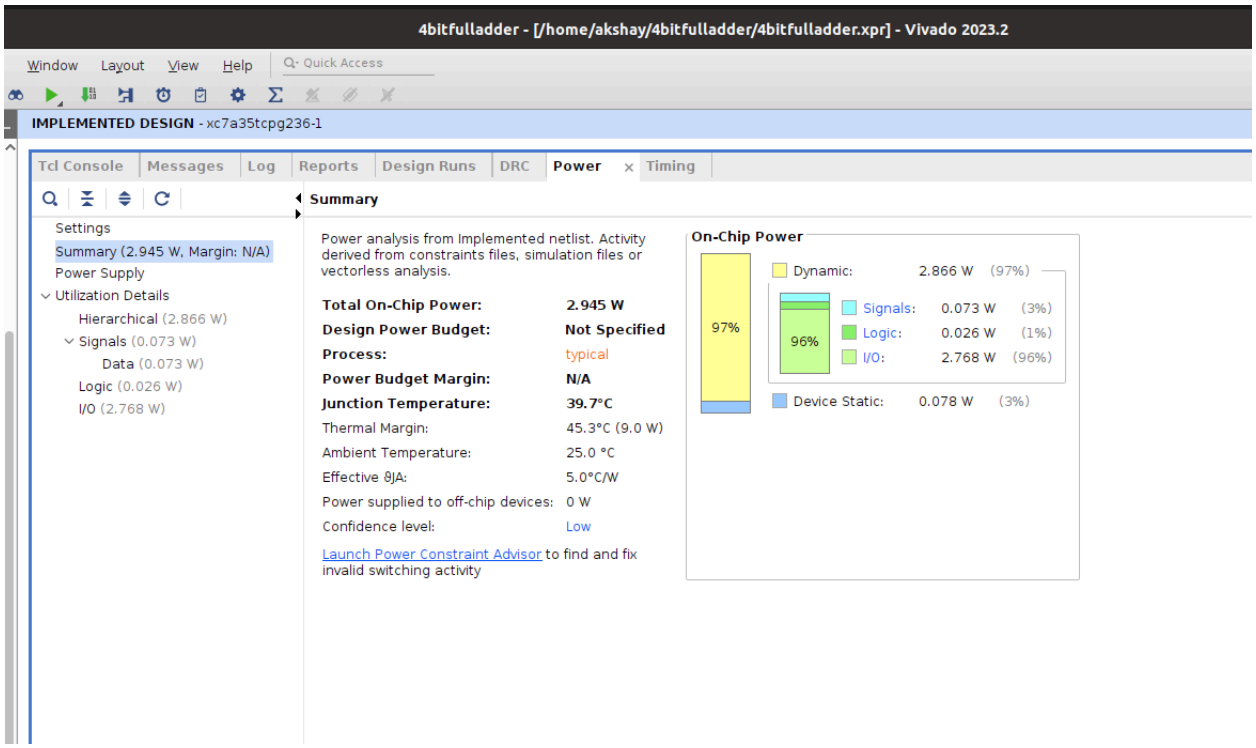
Testbench Code:

```
module adder_4bit_tst;
  reg [3:0] a;
 reg [3:0] b;
  reg ci;
  wire [3:0] s;
  wire co;
add_4_bit dut (s,co,a,b,ci);
initial begin
      a = 4'b0000;
    b = 4'b0000;
    ci = 0;
  end
  always #10 b = b + 1'b1;
  always #20 a = a + 1'b1;
    initial $monitor ("a=%b, b=%b, ci=%b, s=%b, co=%b", a, b, ci, s,
co);
  initial #1000 $finish;
endmodule
```


4bitfulladder - [/home/akshay/4bitfulladder/4bitfulladder.xpr] - Vivado 2023.2
Implementation Complete
Default Layout
Project Summary
Schematic
add_4_bit.v
4 Cells
14 I/O Ports
17 Nets
add1
add2
add3
add4
full_3
a[3:0]
b[3:0]
ci
a
b
c
co
s
co
s[3:0]


4bitfulladder - [/home/akshay/4bitfulladder/4bitfulladder.xpr] - Vivado 2023.2
Implementation Complete
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - adder_4bit_tst
add_4_bit.v
adder_4bit_tst_behav.wcfg
adder_4bit_tst.v
Name
Value
a[3:0]
b[3:0]
ci
s[3:0]
co
1,000.000 ns
Scope
Sources
Objects
Instances





Q.6.> Write a Verilog Code for half substractor.

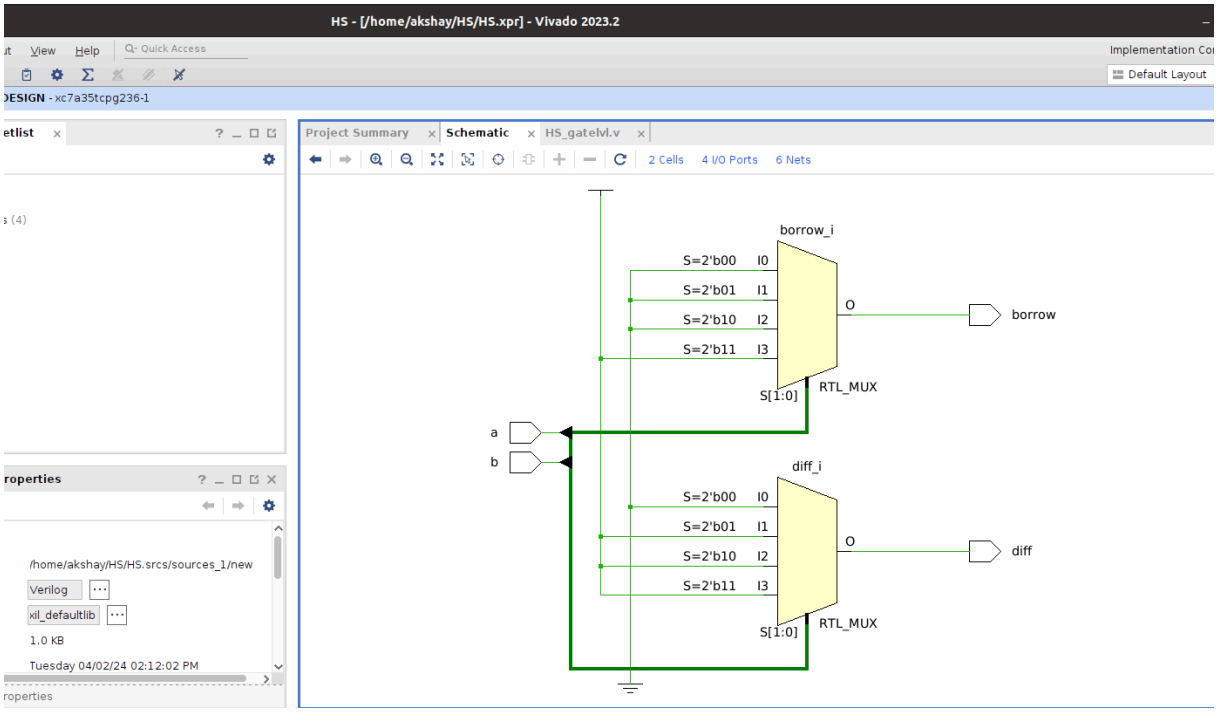
Q.6.> Write a Verilog Code for half substractor.

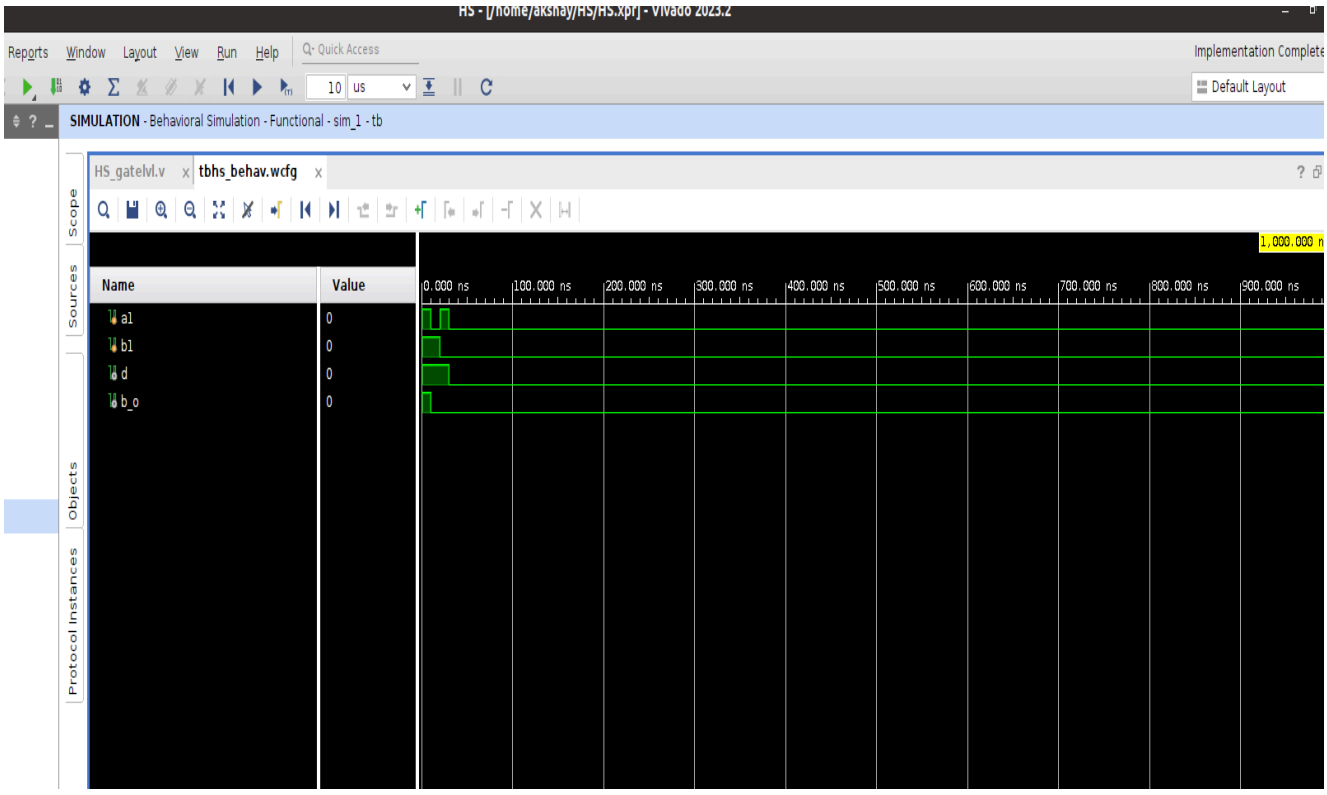
```
//module HS_gatelvl(
//input a,b,
//  output diff, borrow   );
//  wire a_o;
//  xor (diff,a,b);
//  not (a_o,a);
//  and (borrow,b,a_o);
//endmodule

//module HS_gatelvl(
//input a,b,
//  output diff, borrow   );
//   assign d = a^b;
// assign b_o = ~a&b;
//  endmodule

module HS_gatelvl(
   input a, b,
   output reg diff, borrow
);
always @* begin
   case({a, b})
      2'b00: begin diff = 0; borrow = 0; end
      2'b01: begin diff = 1; borrow = 0; end
```

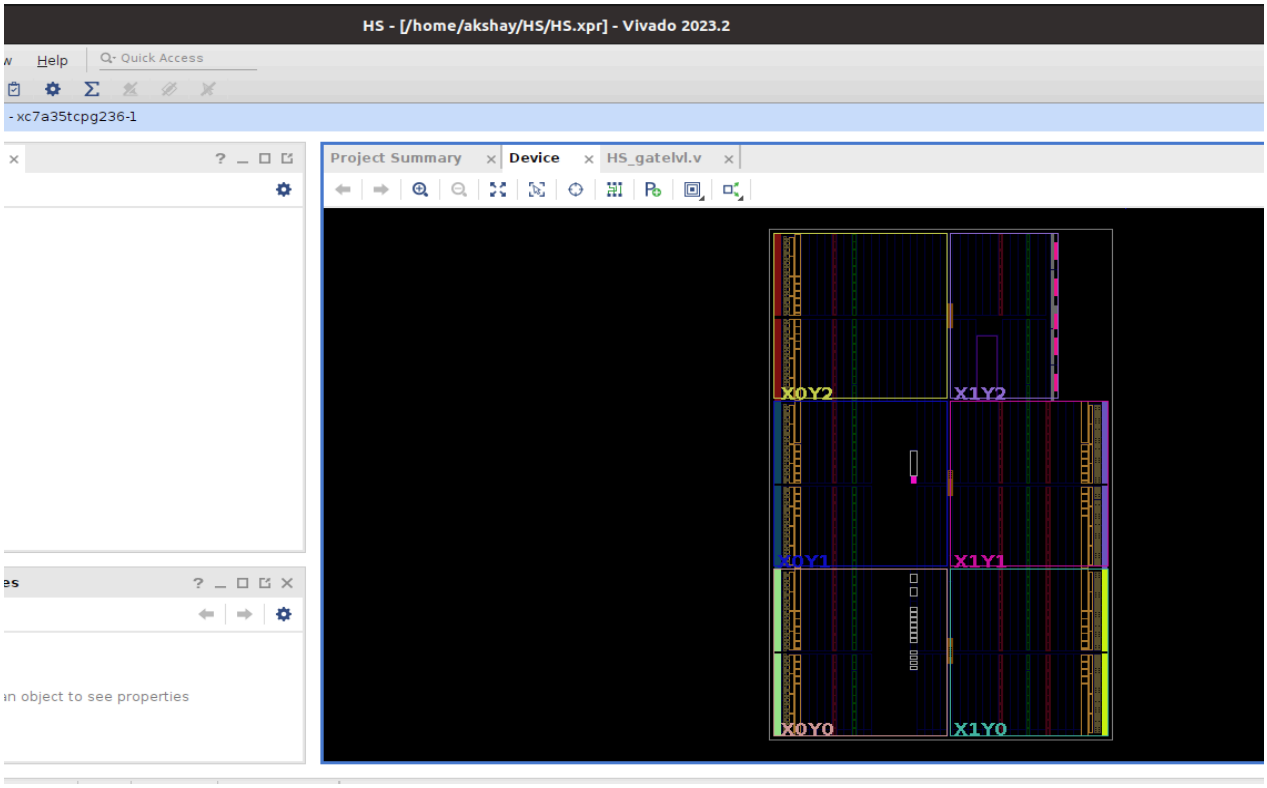
```
            2'b10: begin diff = 1; borrow = 0; end
            2'b11: begin diff = 1; borrow = 1; end
          endcase
        end
endmodule
```

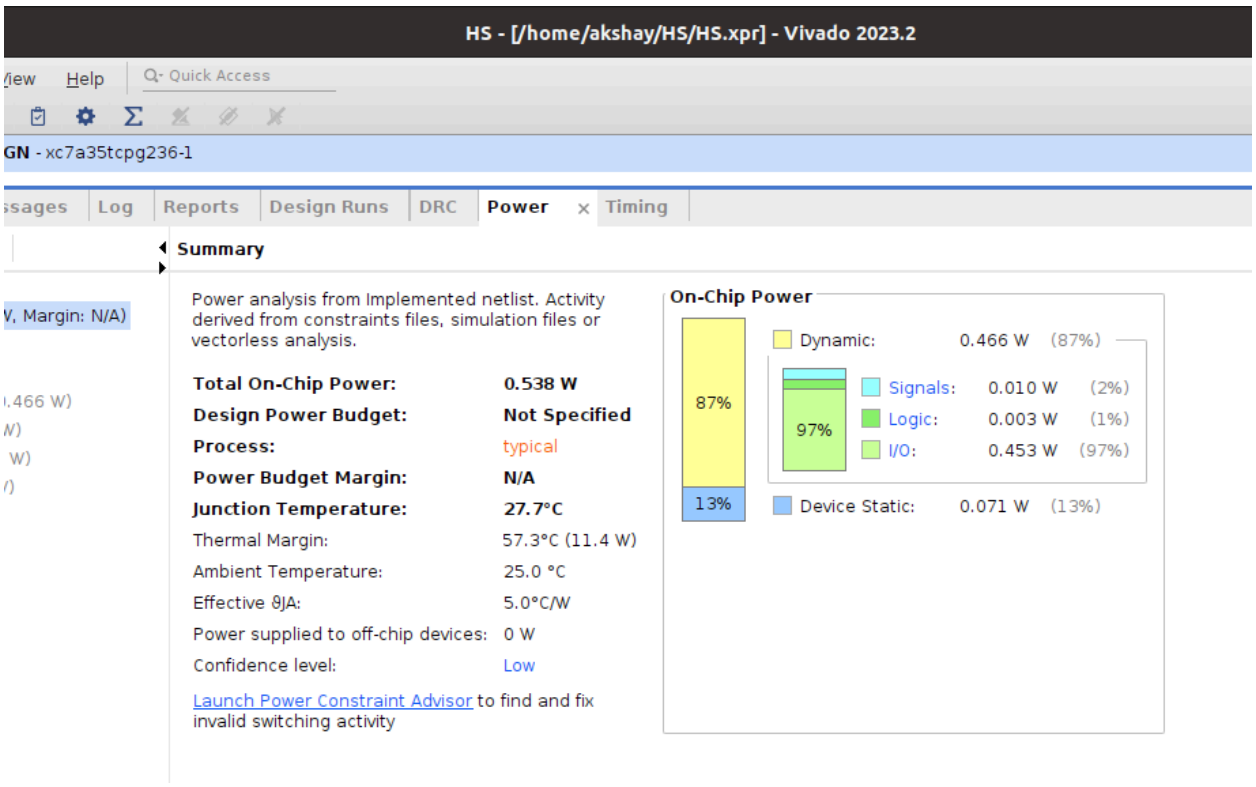
Testbench Code:

```
module tb(
 );
 reg a1;   reg b1;
 wire d;
 wire b_o;
   HS_gatelvl dut(a1,b1,d,b_o);
 initial begin
   $monitor("a = %d, b = %d, Diff = %d, B_O = %d ", a1,b1,d,b_o);
   a1 = 1; b1=1;    #10;
   a1 = 0; b1=1;    #10;
  a1 = 1; b1=0;     #10;
   a1 = 0; b1=0;     #10;
   End
Endmodule
```


HS - [/home/akshay/HS/HS.xpr] - Vivado 2023.2
Project Summary
Schematic
HS_gatelvl.v
2 Cells
4 I/O Ports
6 Nets
borrow_i
S=2'b00 I0
S=2'b01 I1
S=2'b10 I2
S=2'b11 I3
O
borrow
S[1:0]
RTL_MUX
a
b
diff_i
diff
/home/akshay/HS/HS.srcs/sources_1/new
Verilog
1.0 KB
Tuesday 04/02/24 02:12:02 PM


Reports
Window
Layout
View
Run
Help
Implementation Complete
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb
HS_gatelvl.v
tbhs_behav.wcfg
Scope
Sources
Objects
Protocol Instances
Name
Value
a1
b1
d
b_o
0
0
0
0
0.000 ns
100.000 ns
200.000 ns
300.000 ns
400.000 ns
500.000 ns
600.000 ns
700.000 ns
800.000 ns
900.000 ns


HS - [/home/akshay/HS/HS.xpr] - Vivado 2023.2
Help
Quick Access
- xc7a35tcpg236-1
Project Summary
Device
HS_gatelvl.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
n object to see properties


HS - [/home/akshay/HS/HS.xpr] - Vivado 2023.2
Help
Quick Access
- xc7a35tcpg236-1
Log
Reports
Design Runs
DRC
Power
Timing
Summary
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.538 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 27.7°C
Thermal Margin: 57.3°C (11.4 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
87%
13%
97%
Dynamic: 0.466 W (87%)
Signals: 0.010 W (2%)
Logic: 0.003 W (1%)
I/O: 0.453 W (97%)
Device Static: 0.071 W (13%)

Assignment-3

Q.7.> Write a Verilog Code for full substractor.

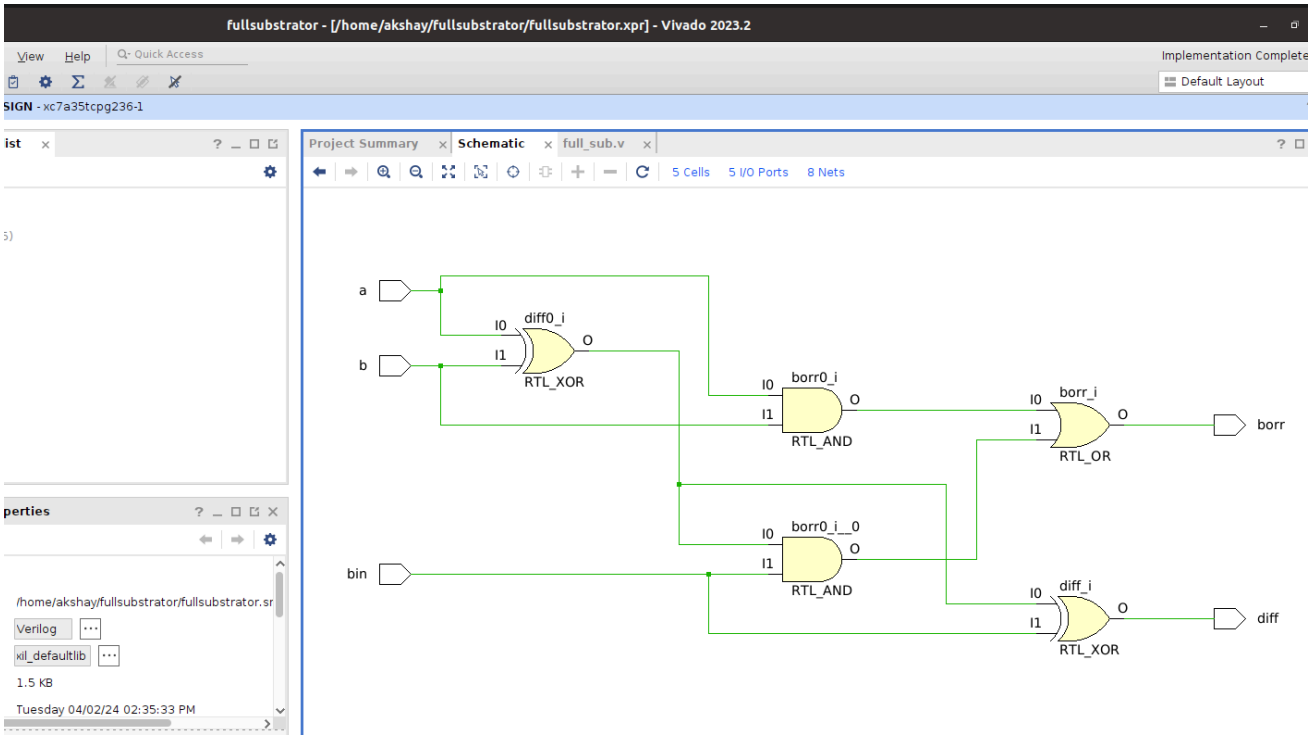
```
//module full_sub(
//    input a,b,bin,
//    output diff, borr
//    );
//    wire a_o,w1,w2,w3;
  //  xor x1(diff,a,b,bin);
//  not(a_o,a);
//  and a1(w1,a_o,bin);
//  and a2(w2,a_o,b);
//  and a3(w3,b,bin);
//  or o1(borr,w1,w2,w3);
  //endmodule


// Code your design here
//module full_sub (a,b,bin,diff,borr);
//  input a,b,bin;
//  output reg diff, borr;
//  always @(a,b,bin) begin
//    case ({a,b,bin})
//      3'b000: begin diff = 0;borr =0 ;end
//      3'b001: begin diff = 1;borr =1 ;end
//      3'b010: begin diff = 1;borr =1 ;end
//      3'b011: begin diff = 0;borr =1 ;end
```

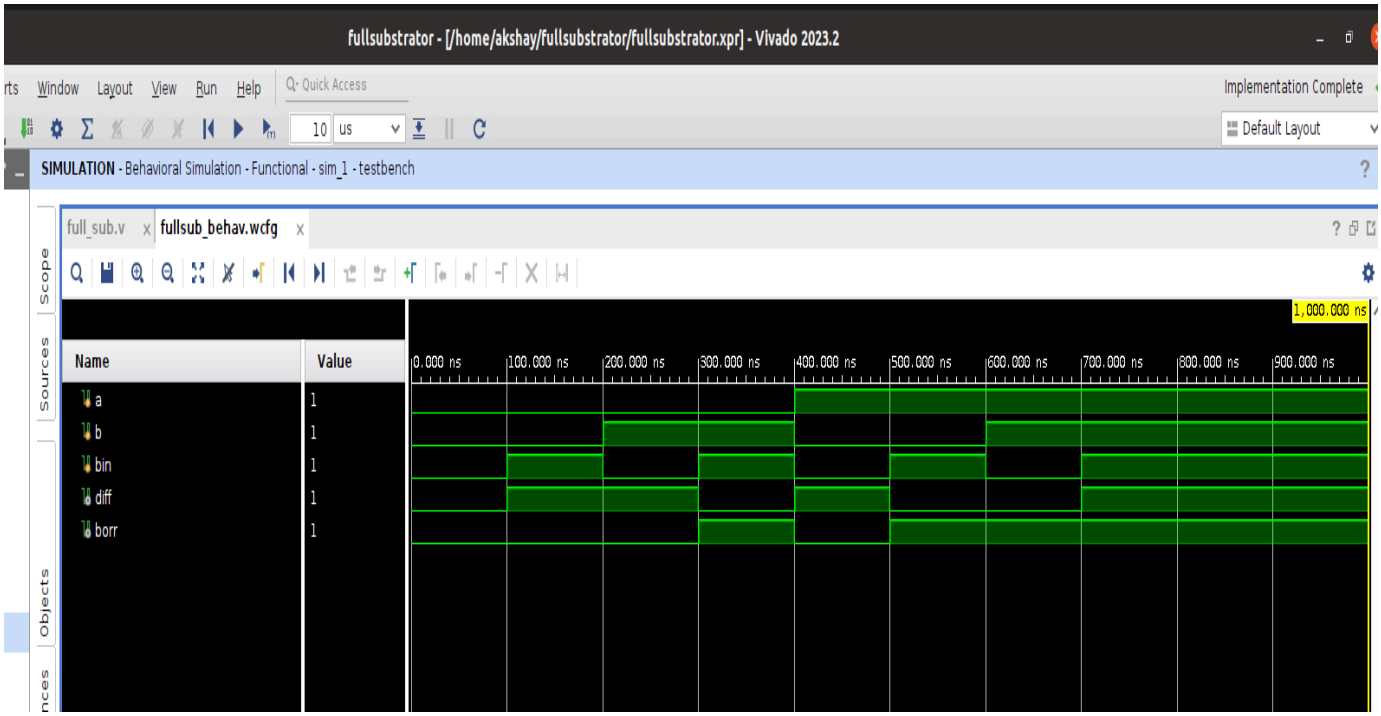
```
//      3'b100: begin diff = 1;borr =0 ;end
//      3'b101: begin diff = 0;borr =0 ;end
//      3'b110: begin diff = 0;borr =0 ;end
//      3'b111: begin diff = 1;borr =1 ;end
//      default begin diff = 0;borr =0 ;end
//    endcase
//    end
//endmodule


// Code your design here
module full_sub (a,b,bin,diff,borr);
  input a,b,bin;
  output diff , borr;
  assign diff = a^b^bin;
  assign borr = (a&b) | ((a^b)&bin) ;
Endmodule
```

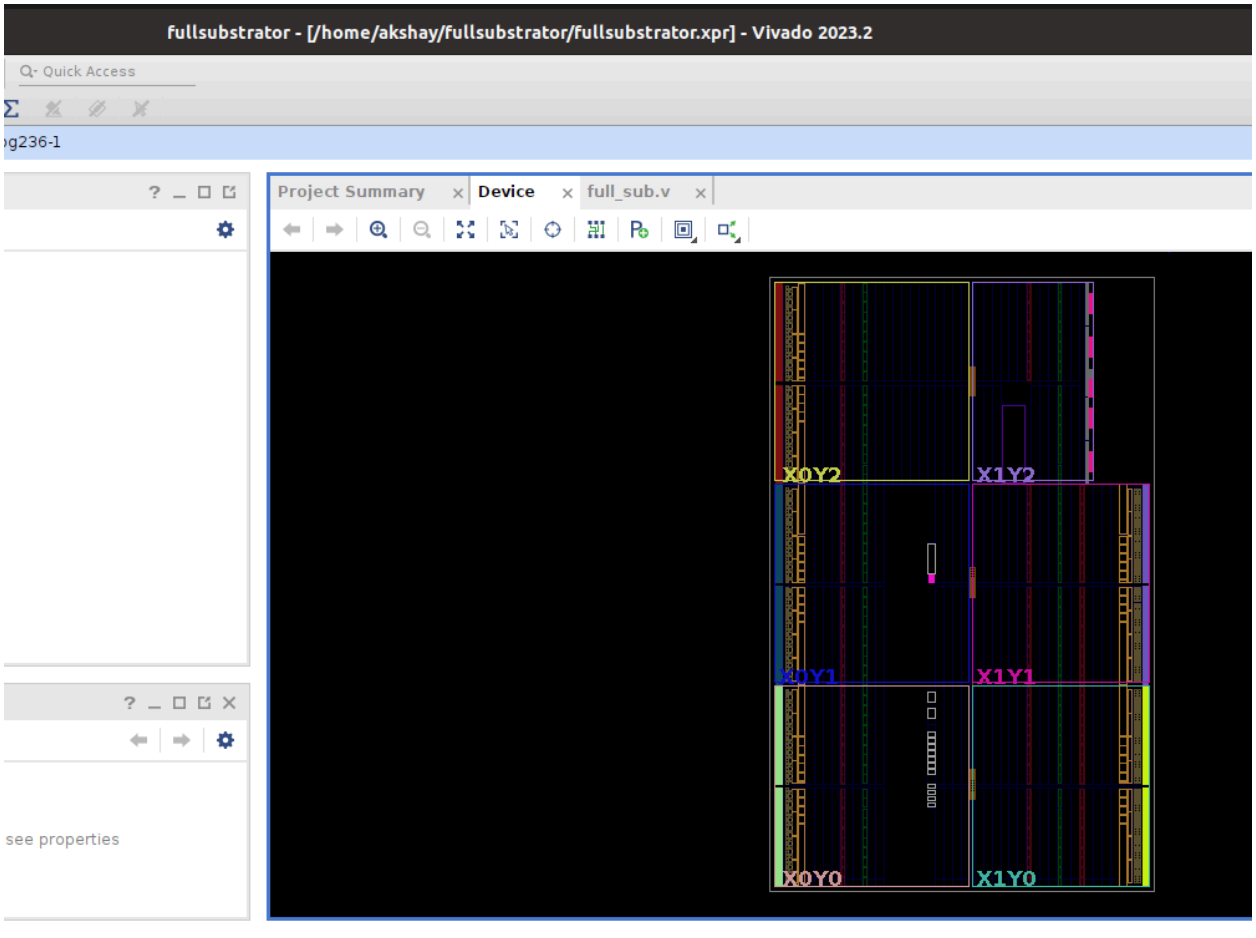
Testbench Code:

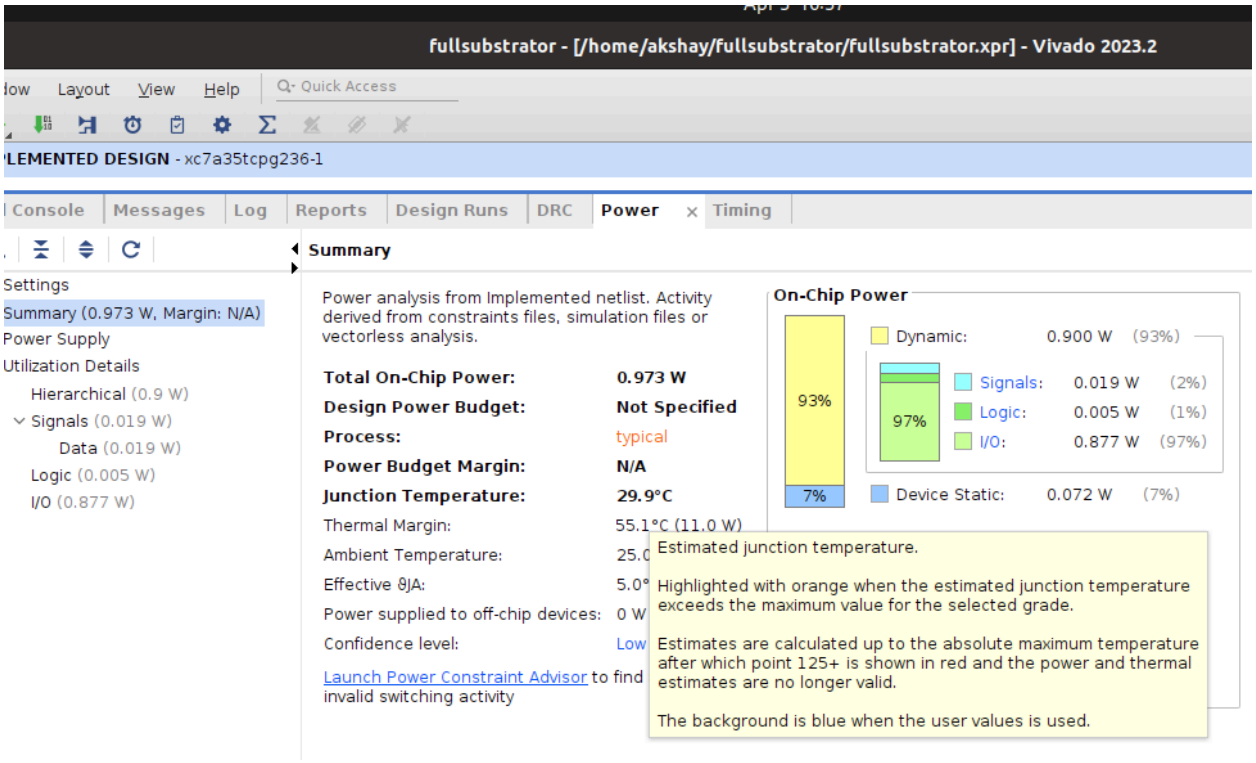
```
module testbench(
 );
      reg a, b, bin;
  wire diff, borr;
  full_sub dut(a, b, bin,diff,borr);
  initial begin
```

```
$monitor("a=%b b=%b, bin=%b, diff =%b, borr=%b", a,b,bin,diff,borr);
  a = 0; b = 0; bin = 0; #100;
  a = 0; b = 0; bin = 1; #100;
  a = 0; b = 0; bin = 1; #100;
  a = 0; b = 1; bin = 1; #100;
  a = 1; b = 0; bin = 0; #100;
  a = 1; b = 0; bin = 1; #100;
  a = 1; b = 1; bin = 0; #100;
  a = 1; b = 1; bin = 1; #100;
 End
endmodule
```




fullsubstrator - [/home/akshay/fullsubstrator/fullsubstrator.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Implementation Complete
10
us
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - testbench
full_sub.v
fullsub_behav.wcfg
Scope
Sources
Objects
Name
Value
a
b
bin
diff
borr
1
0.000 ns
100.000 ns
200.000 ns
300.000 ns
400.000 ns
500.000 ns
600.000 ns
700.000 ns
800.000 ns
900.000 ns
1,000.000 ns


fullsubstrator - [/home/akshay/fullsubstrator/fullsubstrator.xpr] - Vivado 2023.2
Quick Access
Project Summary
Device
full_sub.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
see properties


fullsubstrator - [/home/akshay/fullsubstrator/fullsubstrator.xpr] - Vivado 2023.2
Layout
View
Help
Quick Access
LEMENTED DESIGN - xc7a35tcpg236-1
Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Settings
Summary (0.973 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.9 W)
Signals (0.019 W)
Data (0.019 W)
Logic (0.005 W)
I/O (0.877 W)
Summary
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.973 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 29.9°C
Thermal Margin: 55.1°C (11.0 W)
Ambient Temperature: 25.0
Effective θJA: 5.0°
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find invalid switching activity
On-Chip Power
93%
7%
97%
Dynamic: 0.900 W (93%)
Signals: 0.019 W (2%)
Logic: 0.005 W (1%)
I/O: 0.877 W (97%)
Device Static: 0.072 W (7%)
Estimated junction temperature.
Highlighted with orange when the estimated junction temperature exceeds the maximum value for the selected grade.
Estimates are calculated up to the absolute maximum temperature after which point 125+ is shown in red and the power and thermal estimates are no longer valid.
The background is blue when the user values is used.

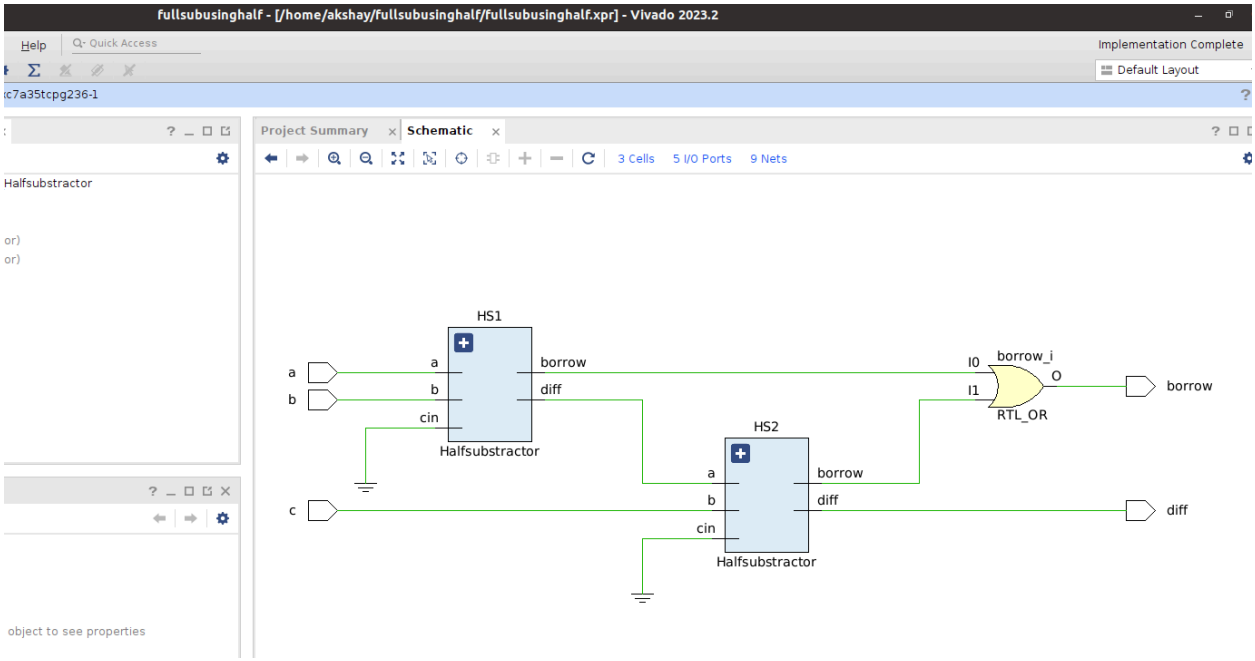
Q.8.> Write a Verilog Code for full substractor using half substractor.

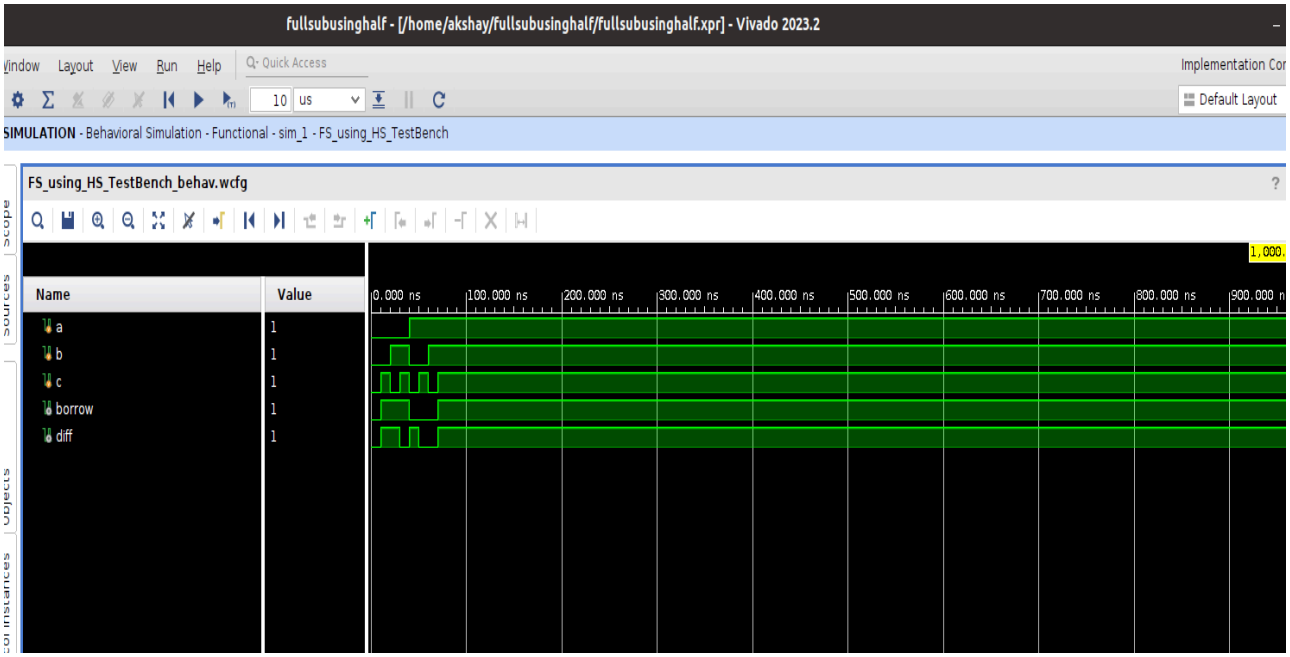
```
module Fullsubstractor_using_Halfsubstractor (
    input a, b, c,
    output diff, borrow
);
    wire dl, bl,b2;
    Halfsubstractor HS1(a, b, 1'b0, bl, dl);
   Halfsubstractor HS2(dl, c, 1'b0, b2, diff);
  assign borrow = bl | b2;
endmodule
module Halfsubstractor (
    input a, b, cin,
    output borrow, diff
);
    wire na;
   assign diff = a ^ b ^ cin;
    assign na = ~a;
    assign borrow = (na & b) | (cin & (a ^ b));
endmodule
```

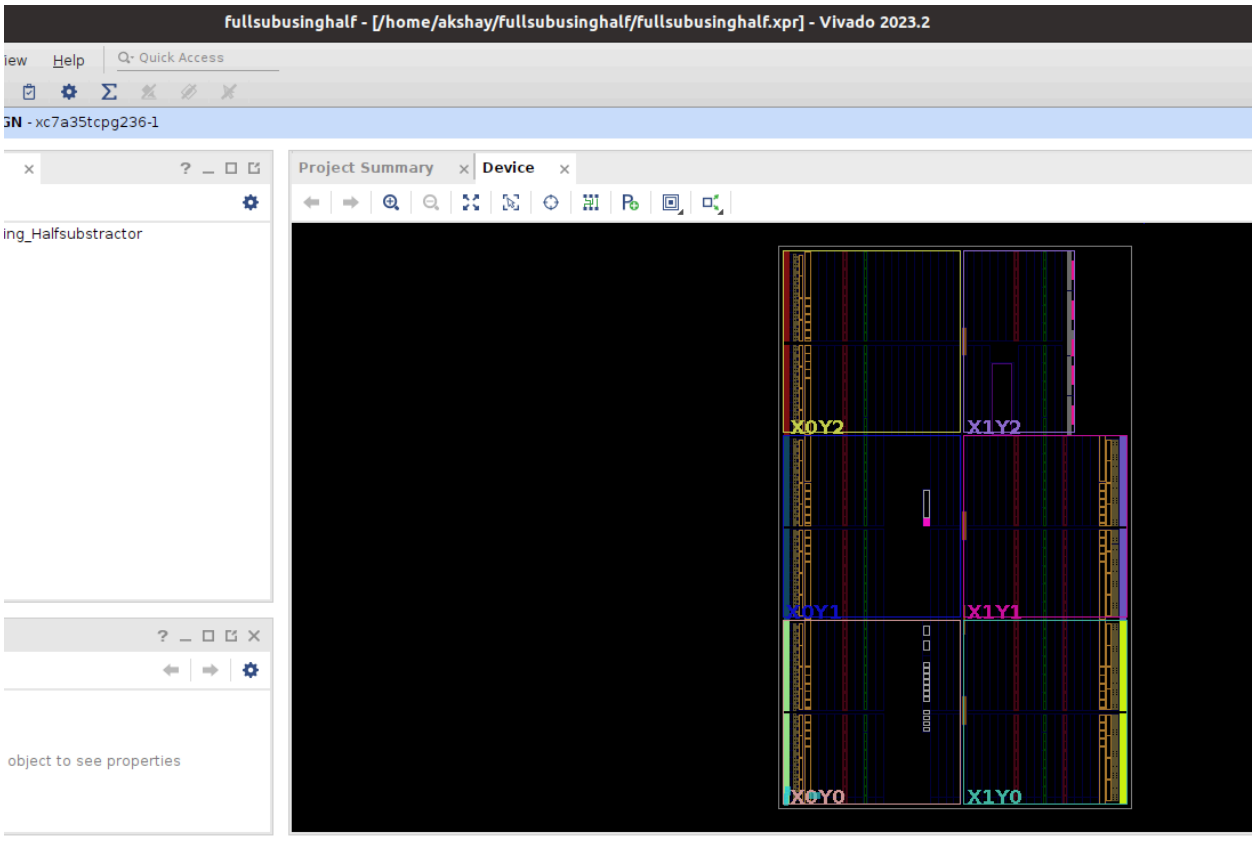
Testbench Code:

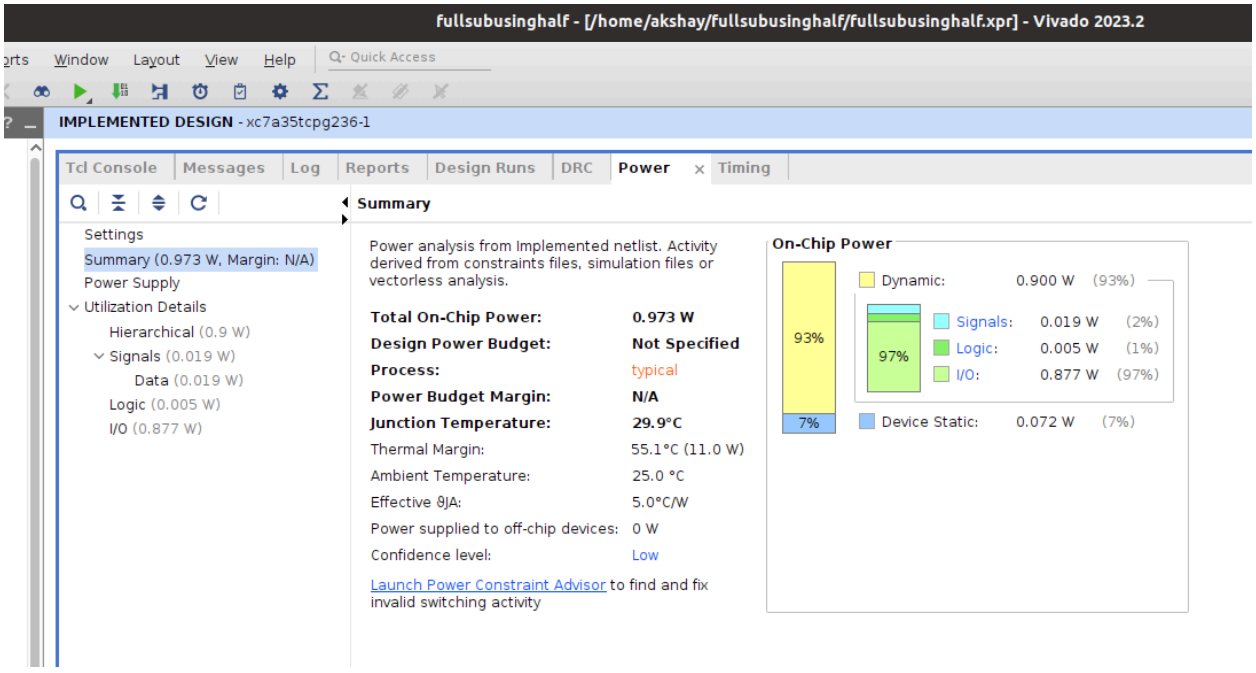
```
module FS_using_HS_TestBench();
//inputs
    reg a, b, c;
```

```
//outputs
        wire borrow, diff;
 //instantiate the unit under test (UUT)
        Fullsubstractor_using_Halfsubstractor dut (
            .a(a),
            .b(b),
            .c(c),
            .borrow(borrow),
            .diff(diff)
        );
    initial
        begin
        a=0; b=0 ; c=0;#10;
        a=0; b=0; c=1;#10;
        a=0; b=1; c=0;#10;
        a=0; b=1; c=1;#10;
        a=1; b=0 ;c=0;#10;
        a=1; b=0; c=1;#10;
        a=1; b=1; c=0;#10;
        a=1; b=1; c=1; #10;
       end
Initial
  $monitor("a=%b, b=%b, c=%b, borrow=%b, diff=%b",a, b, c, borrow, diff);
         endmodule
```


fullsubusinghalf - [/home/akshay/fullsubusinghalf/fullsubusinghalf.xpr] - Vivado 2023.2
Help
Quick Access
Implementation Complete
Default Layout
Project Summary
Schematic
3 Cells
5 I/O Ports
9 Nets
Halfsubstractor
HS1
a
b
cin
borrow
diff
Halfsubstractor
HS2
a
b
cin
borrow
diff
Halfsubstractor
c
I0
I1
borrow_i
O
RTL_OR
borrow
diff
object to see properties


fullsubusinghalf - [/home/akshay/fullsubusinghalf/fullsubusinghalf.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - FS_using_HS_TestBench
FS_using_HS_TestBench_behav.wcfg
Name
Value
a
b
c
borrow
diff
1
0.000 ns
100.000 ns
200.000 ns
300.000 ns
400.000 ns
500.000 ns
600.000 ns
700.000 ns
800.000 ns


fullsubusinghalf - [/home/akshay/fullsubusinghalf/fullsubusinghalf.xpr] - Vivado 2023.2
Help
Quick Access
GN - xc7a35tcpg236-1
ing_Halfsubstractor
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
object to see properties


fullsubusinghalf - [/home/akshay/fullsubusinghalf/fullsubusinghalf.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Summary
Settings
Summary (0.973 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.9 W)
Signals (0.019 W)
Data (0.019 W)
Logic (0.005 W)
I/O (0.877 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.973 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 29.9°C
Thermal Margin: 55.1°C (11.0 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
93%
7%
97%
Dynamic: 0.900 W (93%)
Signals: 0.019 W (2%)
Logic: 0.005 W (1%)
I/O: 0.877 W (97%)
Device Static: 0.072 W (7%)

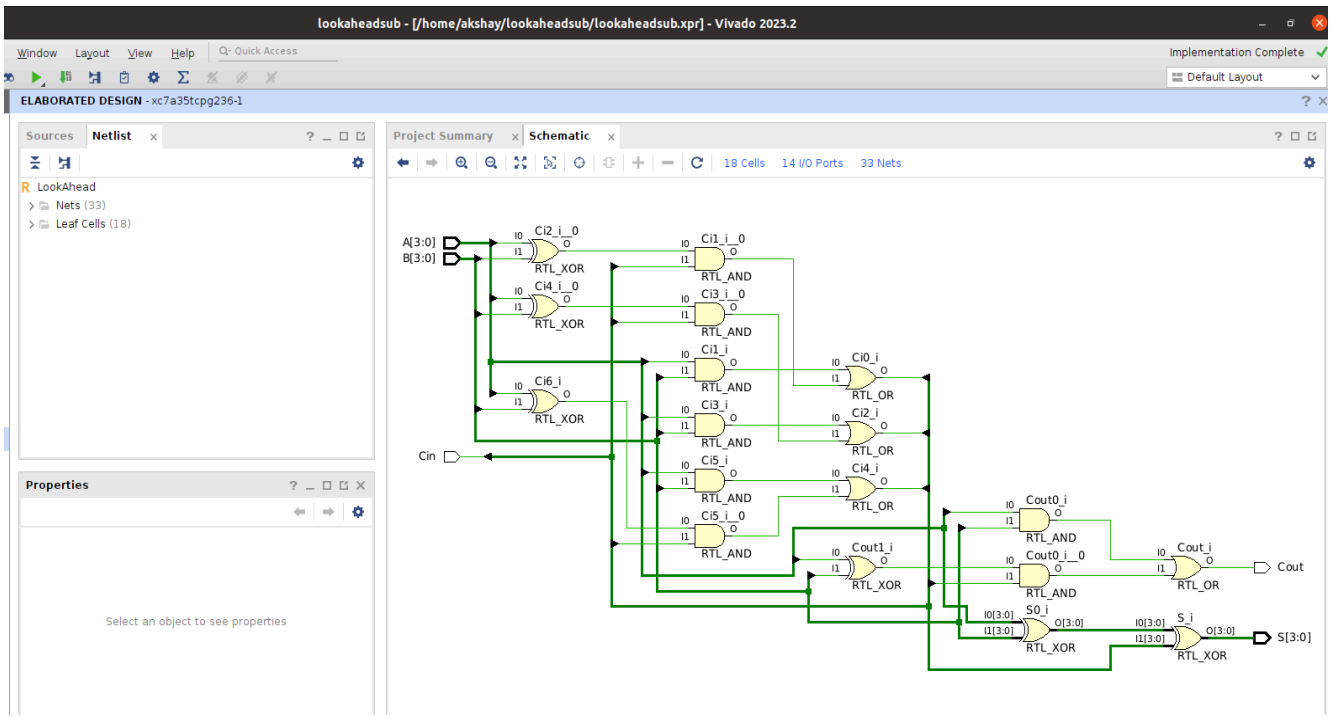
Q.9.> Write a Verilog Code for 4-bit carry look Adder.

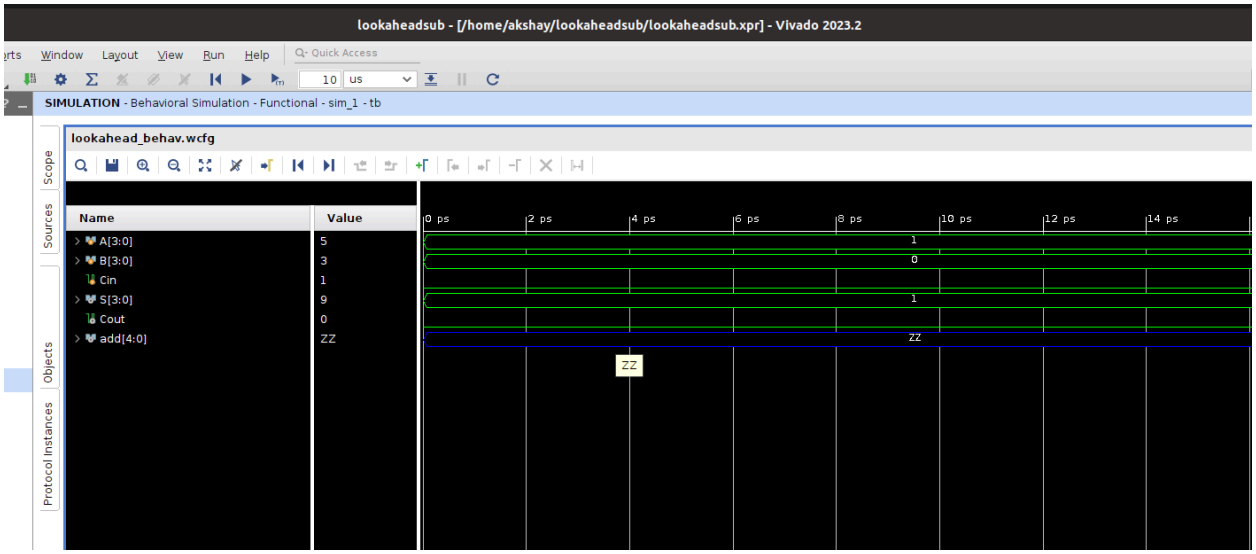
```
module LookAhead(
  input [3:0]A, B,
  input Cin,
  output [3:0] S,
  output Cout
);
  wire [3:0] Ci;
   assign Ci[0] = Cin;
  assign Ci[1] = (A[0] & B[0]) | ((A[0]^B[0]) & Ci[0]);
  assign Ci[2] = (A[1] & B[1]) | ((A[1]^B[1]) & ((A[0] & B[0]) | ((A[0]^B[0]) & Ci[0])));
  assign Ci[3] = (A[2] & B[2]) | ((A[2]^B[2]) & ((A[1] & B[1]) | ((A[1]^B[1]) & ((A[0] & B[0]) | ((A[0]^B[0]) & Ci[0])))));
  assign Cout  = (A[3] & B[3]) | ((A[3]^B[3]) & ((A[2] & B[2]) | ((A[2]^B[2]) & ((A[1] & B[1]) | ((A[1]^B[1]) & ((A[0] & B[0]) | ((A[0]^B[0]) & Ci[0])))))));
assign S = A^B^Ci;
  assign add = {Cout, S};
endmodule
```

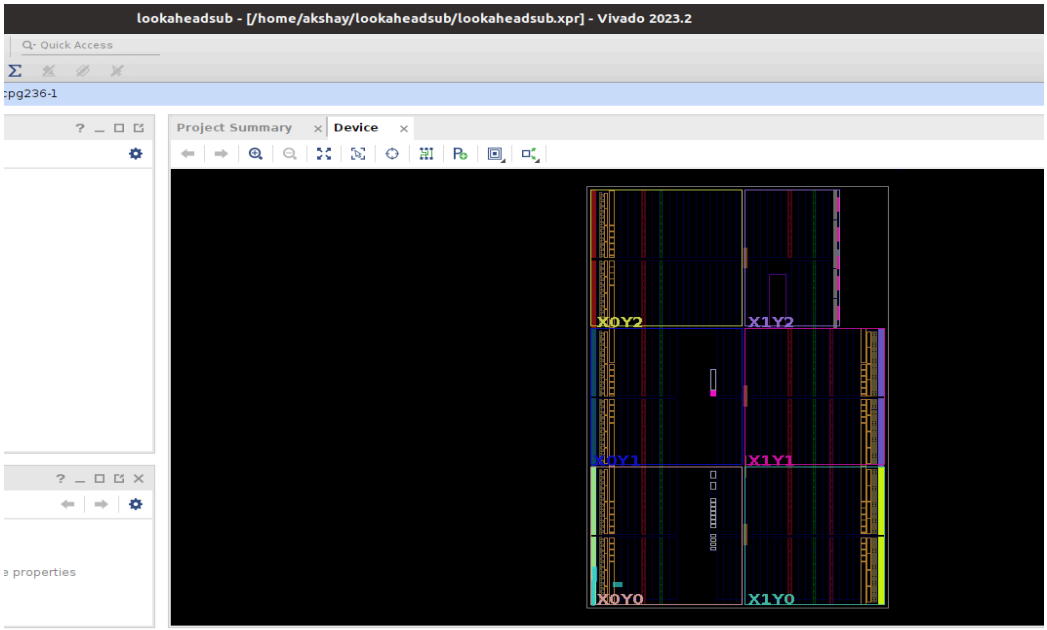
Testbench Code:

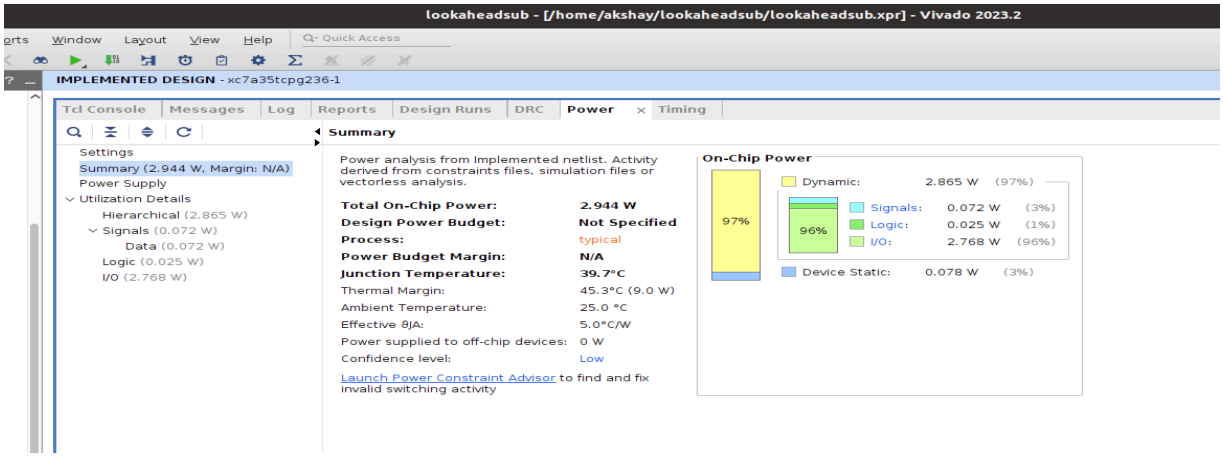
```
module tb;
  reg [3:0]A, B;
  reg Cin;
  wire [3:0] S;
  wire Cout;
```

```
 wire[4:0] add;

  LookAhead dut(A, B, Cin, S, Cout);

   initial begin

    $monitor("A = %b: B = %b, Cin = %b --> S = %b, Cout = %b, add = %0d", A, B,
Cin, S, Cout, add);

    A = 1; B = 0; Cin = 0; #3;

    A = 2; B = 4; Cin = 1; #3;

    A = 4'hb; B = 4'h6; Cin = 0; #3;

    A = 5; B = 3; Cin = 1;

  end

Endmodule
```




lookaheadsub - [/home/akshay/lookaheadsub/lookaheadsub.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb
lookahead_behav.wcfg
Scope
Sources
Objects
Protocol Instances
Name
Value
A[3:0]
5
B[3:0]
3
Cin
1
S[3:0]
9
Cout
0
add[4:0]
ZZ
0 ps
2 ps
4 ps
6 ps
8 ps
10 ps
12 ps
14 ps
ZZ


lookaheadsub - [/home/akshay/lookaheadsub/lookaheadsub.xpr] - Vivado 2023.2
Quick Access
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0


lookaheadsub - [/home/akshay/lookaheadsub/lookaheadsub.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Summary
Settings
Summary (2.944 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (2.865 W)
Signals (0.072 W)
Data (0.072 W)
Logic (0.025 W)
I/O (2.768 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 2.944 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 39.7°C
Thermal Margin: 45.3°C (9.0 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
97%
96%
Dynamic: 2.865 W (97%)
Signals: 0.072 W (3%)
Logic: 0.025 W (1%)
I/O: 2.768 W (96%)
Device Static: 0.078 W (3%)

Q.10.> Write a Verilog Code for

a.> 2:1 MUX b.> 4:1 MUX

Soln a.> for 2:1 MUX

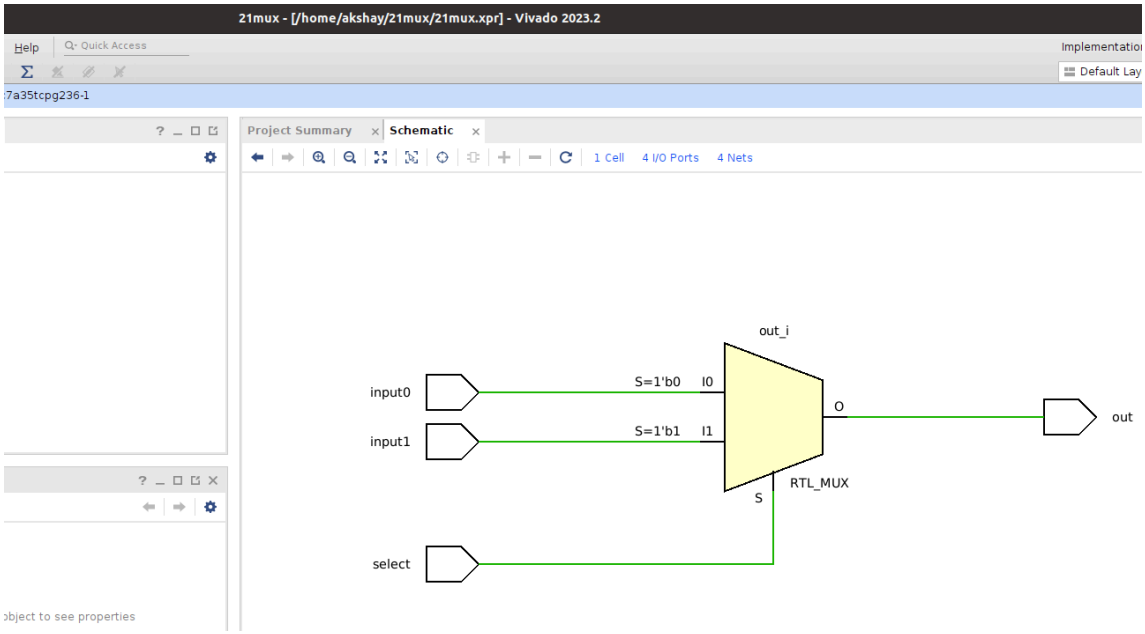
```
/module mux_2_1 (
//  input select,
//  input input0, input1,
//  output out
//);
//  assign out = select ? input1 : input0;
//endmodule


// module mux_2_1 (
//     input select,
//     input input0, input1,
//     output out
// );
//     wire w_sel_and_input0, w_sel_and_input1;
//     wire w_sel_and_not_sel, w_sel_and_input1_and_sel_and_not_sel;
//     and #(1) U1(w_sel_and_input0, select, input0);
//     and #(1) U2(w_sel_and_input1, select, input1);
//     not #(1) U3(w_sel_and_not_sel, select);
//     and #(1) U4(w_sel_and_input1_and_sel_and_not_sel, input1, select,
w_sel_and_not_sel);
//     or #(1) U5(out, w_sel_and_input0, w_sel_and_input1_and_sel_and_not_sel);
// endmodule
```

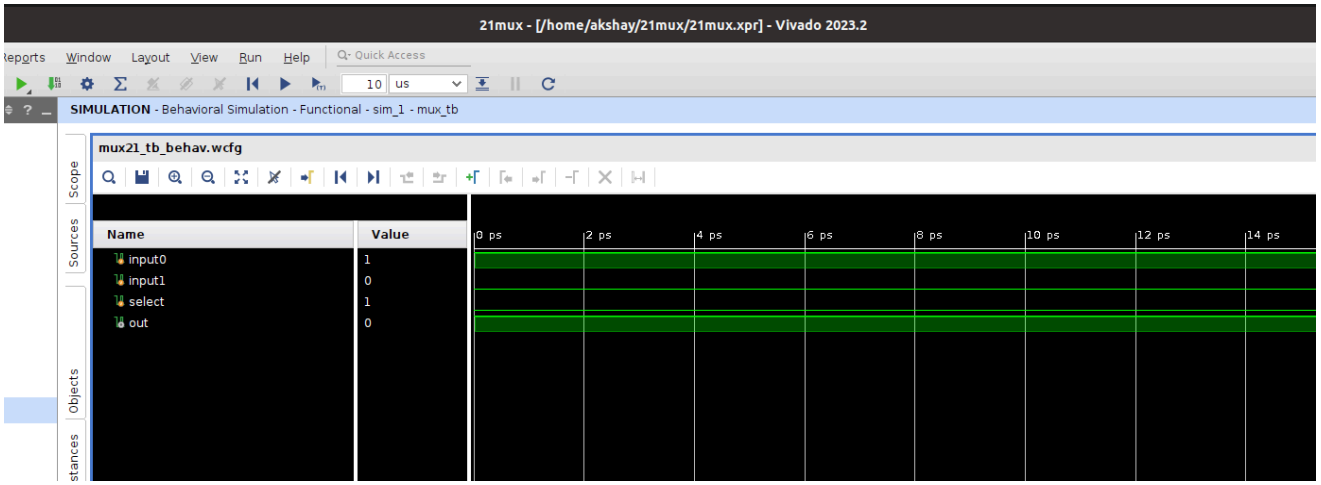
```
module mux_2_1 (
            input select,
            input input0, input1,
            output reg out
           );
 always @ (*)
              begin
              case(select)
                1'b0: out = input0;
                1'b1: out = input1;
                default: out = 1'bx; // Default case for unknown select value
              endcase
             end
endmodule
```

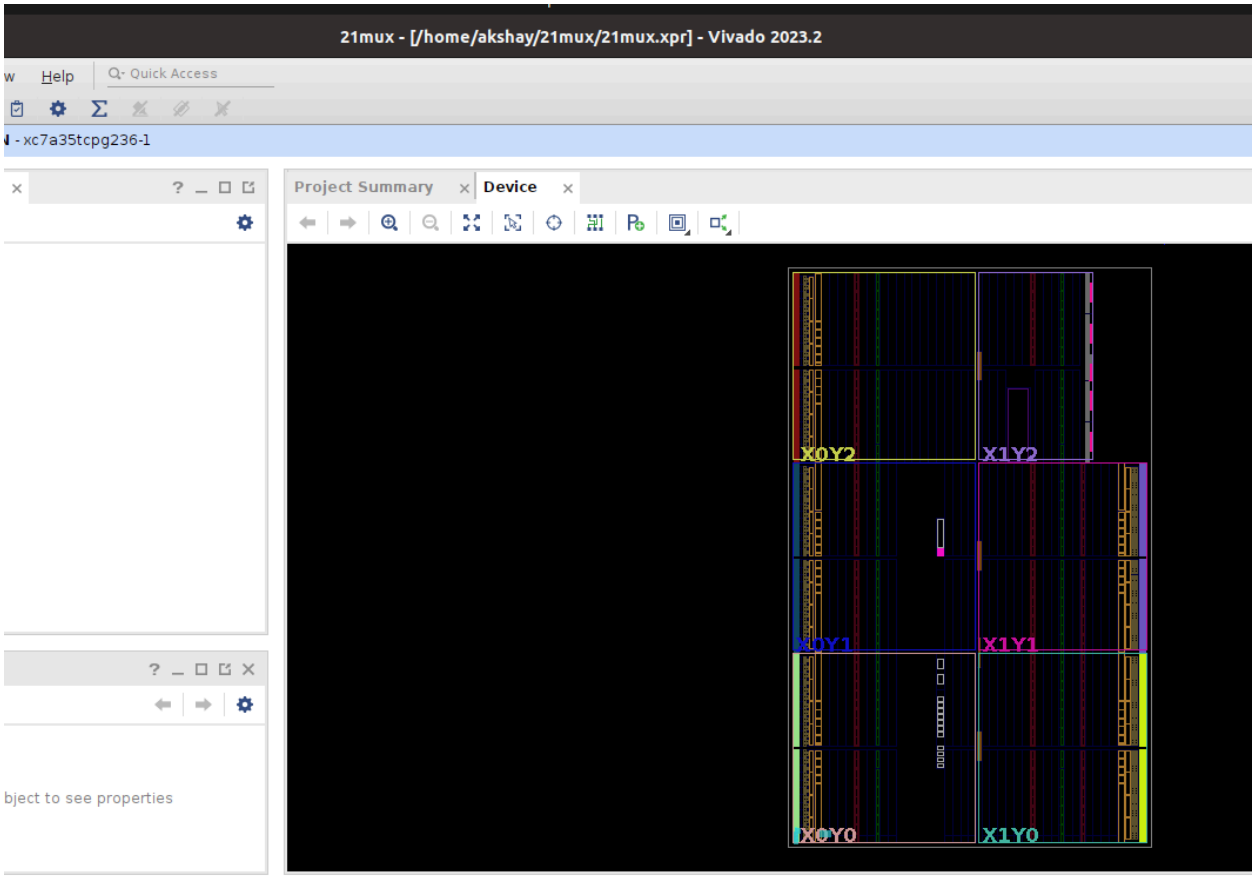
Testbench Code:

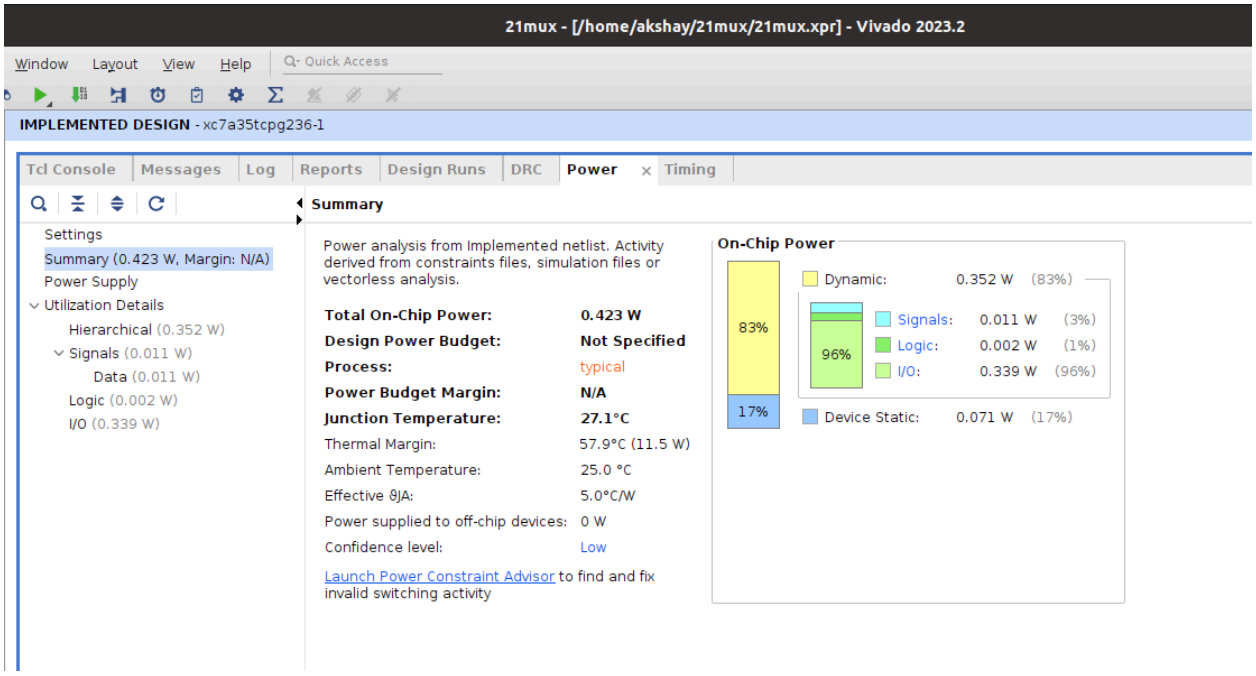
```
module mux_tb();
  reg input0, input1, select;
  wire out;
   mux_2_1   dut(select, input0, input1, out);
  initial begin
    $monitor("select = %h: input0 = %h, input1 = %h --> out = %h", select, input0,
input1, out);
    input0 = 1; input1 = 0;
```

```
    select = 0;
    #100;
    select = 1;
  end
endmodule
```






21mux - [/home/akshay/21mux/21mux.xpr] - Vivado 2023.2
Help
Quick Access
- xc7a35tcpg236-1
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
bject to see properties


21mux - [/home/akshay/21mux/21mux.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Settings
Summary (0.423 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.352 W)
Signals (0.011 W)
Data (0.011 W)
Logic (0.002 W)
I/O (0.339 W)
Summary
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.423 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 27.1°C
Thermal Margin: 57.9°C (11.5 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
83%
17%
96%
Dynamic: 0.352 W (83%)
Signals: 0.011 W (3%)
Logic: 0.002 W (1%)
I/O: 0.339 W (96%)
Device Static: 0.071 W (17%)

Soln b.> for 4:1 MUX

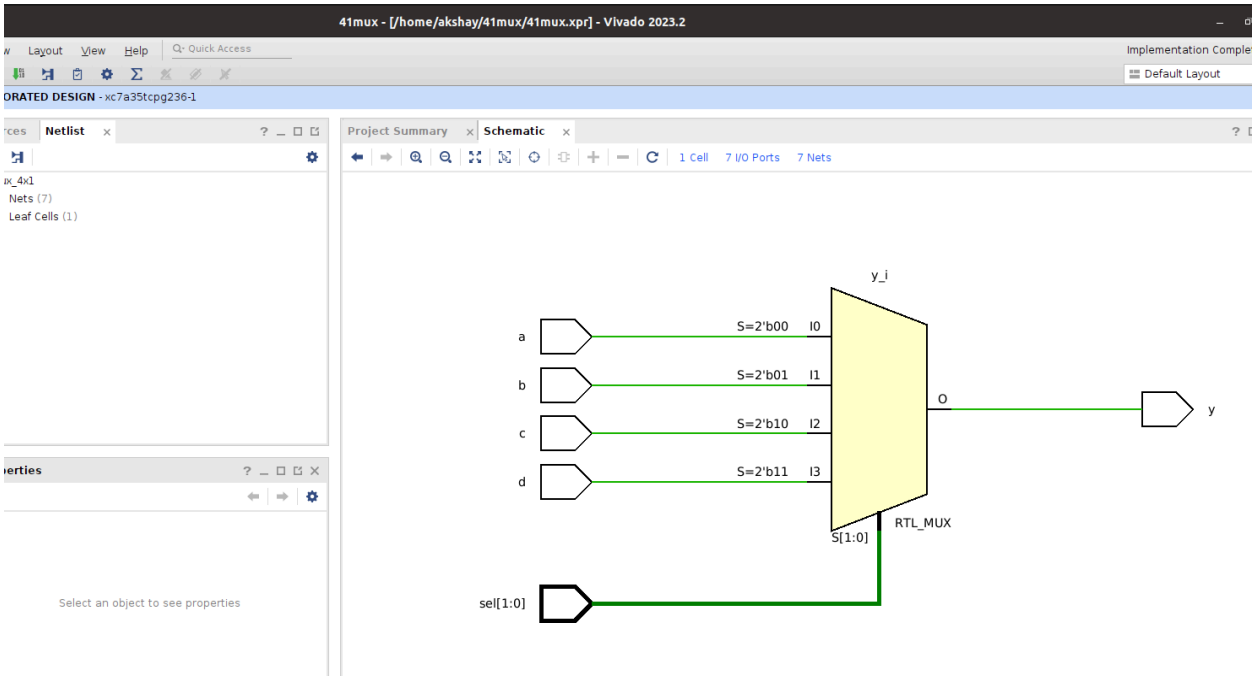
```
module mux_4x1 (
  input [1:0] sel,
  input  a,b,c,d,
  output reg y
 );
    always @(*) begin
    case(sel)
      2'h0: y = a;
      2'h1: y = b;
      2'h2: y = c;
      2'h3: y = d;
      default: $display("Invalid sel input");
    endcase
   end
endmodule

//module mux_4x1 (
//   input [1:0] sel,
//   input  a, b, c, d,
//   output reg y
// );
//   wire w_sel_inv_0, w_sel_inv_1;
//   wire w_sel_and_a, w_sel_and_b, w_sel_and_c, w_sel_and_d;
//   wire w_sel_and_inv_0, w_sel_and_inv_1;
```

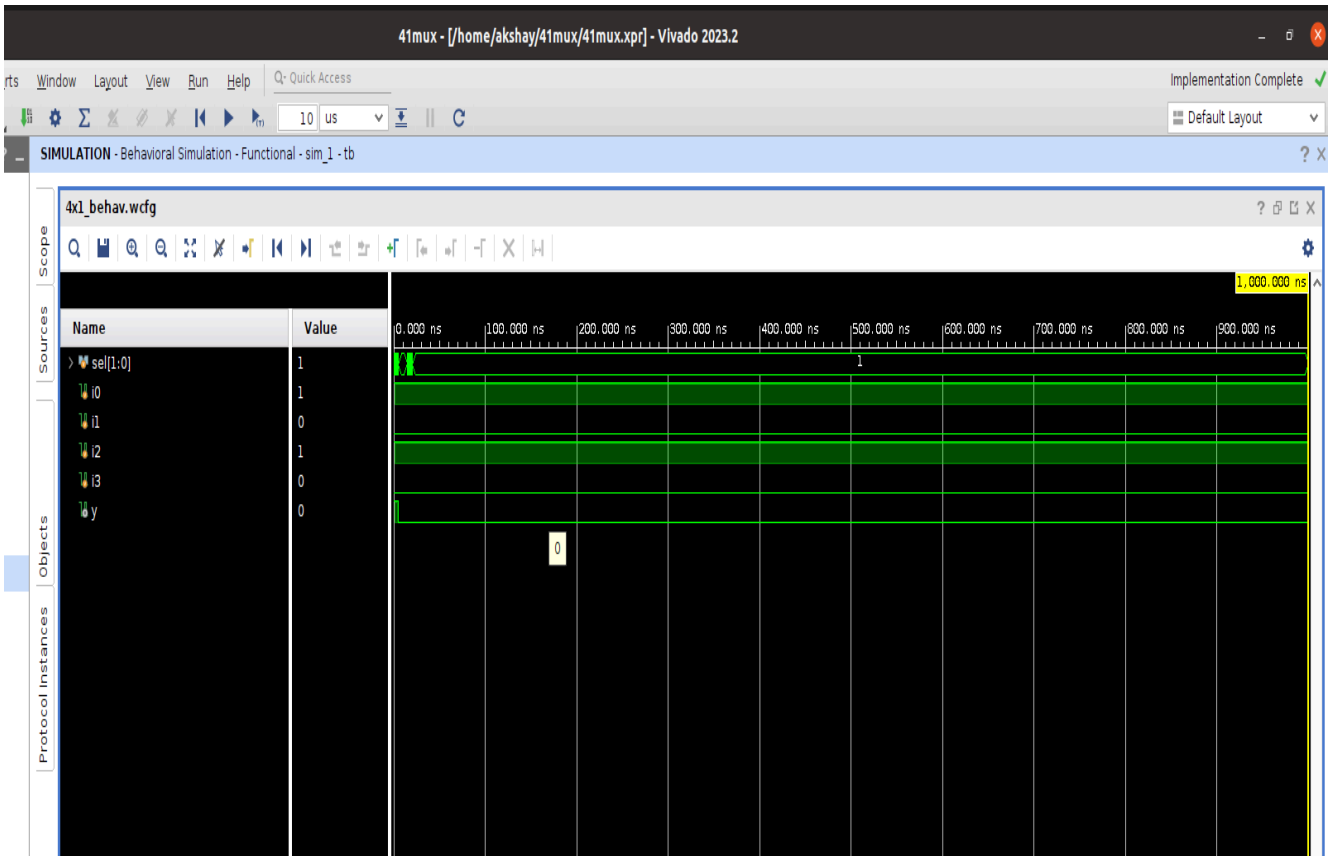
```
//   // Inverters for sel[0] and sel[1]

        //   not #(1) U_sel_inv_0(w_sel_inv_0, sel[0]);

        //   not #(1) U_sel_inv_1(w_sel_inv_1, sel[1]);

//   // AND gates for sel[0] and sel[1] with inputs

        //   and #(1) U_sel_and_a(w_sel_and_a, sel[0], a);

        //   and #(1) U_sel_and_b(w_sel_and_b, sel[0], b);

        //   and #(1) U_sel_and_c(w_sel_and_c, sel[0], c);

        //   and #(1) U_sel_and_d(w_sel_and_d, sel[0], d);

//   // AND gates for inverted sel[0] and sel[1]

        //   and #(1) U_sel_and_inv_0(w_sel_and_inv_0, w_sel_inv_0, a);

        //   and #(1) U_sel_and_inv_1(w_sel_and_inv_1, w_sel_inv_1, b);

//   // OR gate for final output

        //   or #(1) U_or_y(y, w_sel_and_a, w_sel_and_b, w_sel_and_c, w_sel_and_d,
        w_sel_and_inv_0, w_sel_and_inv_1);

// endmodule


        //module mux_example(

        //  input [1:0] sel,

        //  input  i0,i1,i2,i3,

        //  output reg y);

          //  always @(*) begin

        //    case(sel)

        //      2'h0: y = i0;

        //      2'h1: y = i1;

        //      2'h2: y = i2;
```

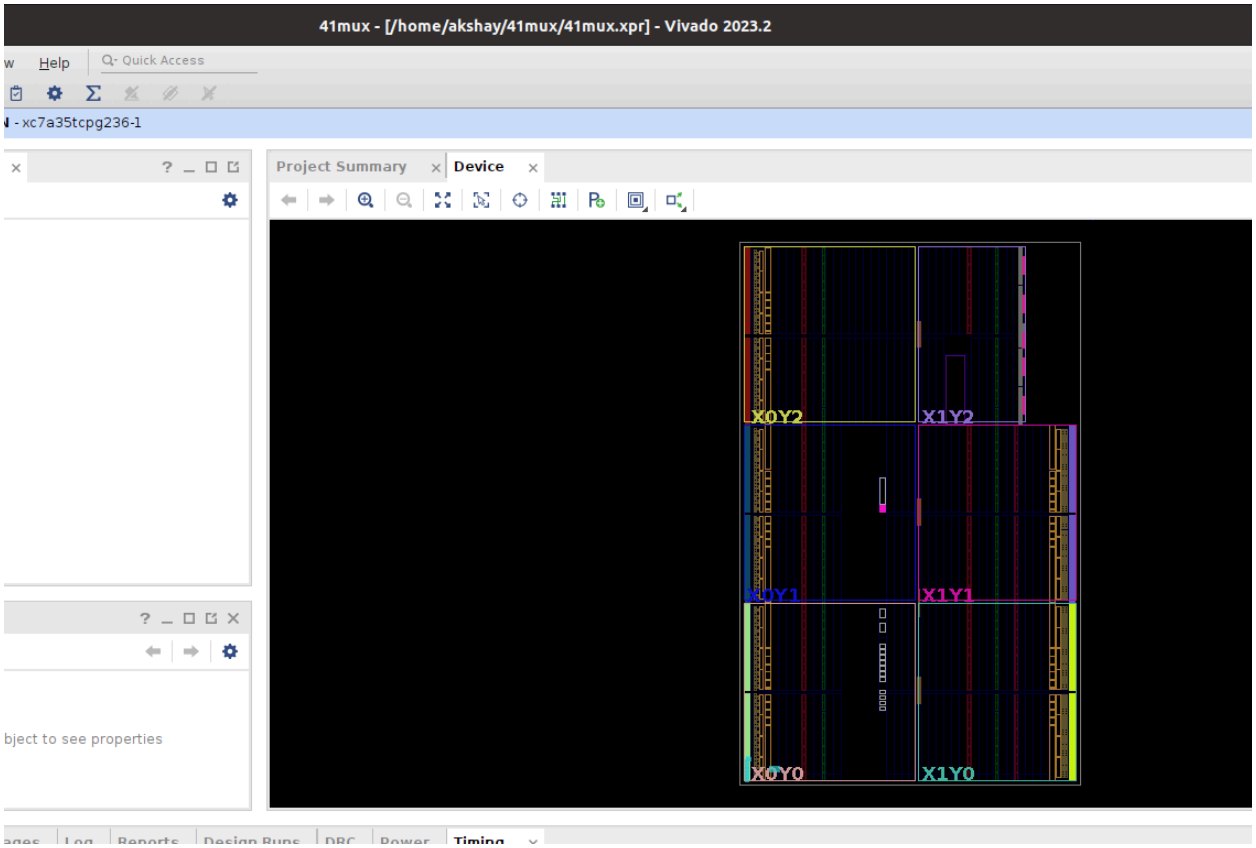
```
//      2'h3: y = i3;
//      default: $display("Invalid sel input");
//    endcase
//  end
//endmodule
```

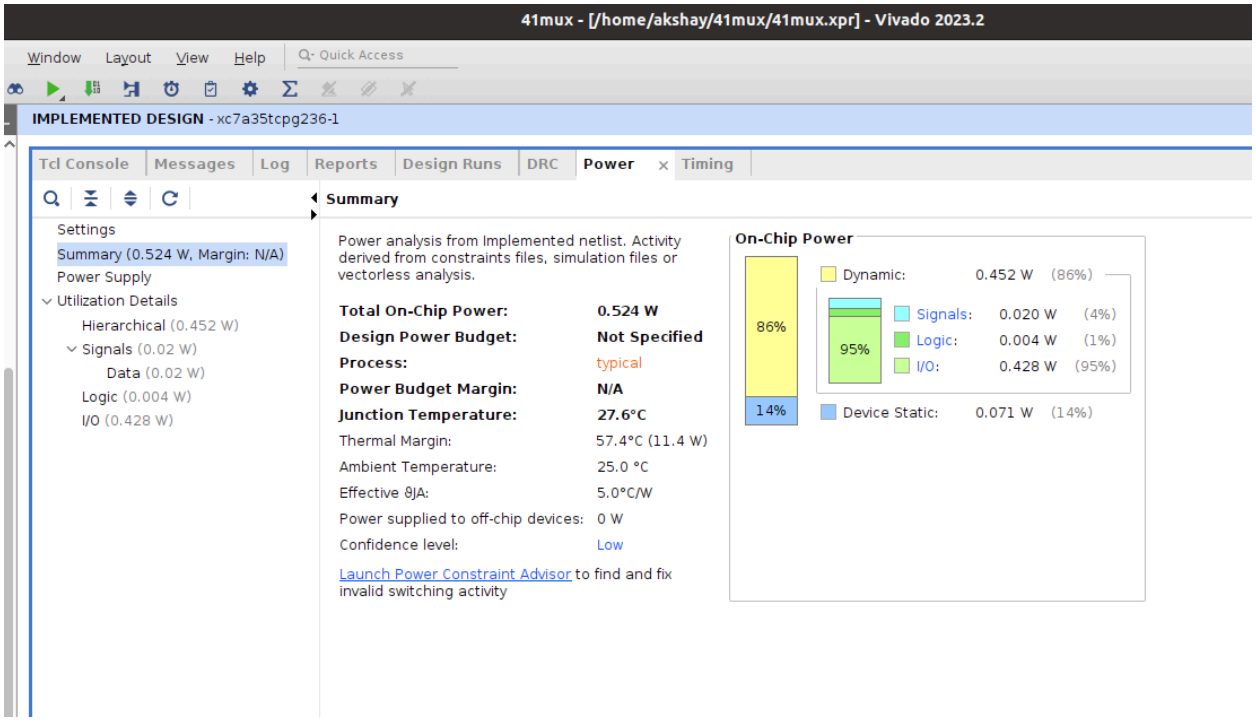
Testbench Code:

```
module tb;
  reg [1:0] sel;
  reg i0,i1,i2,i3;
  wire y;
   mux_example mux(sel, i0, i1, i2, i3, y);
  initial begin
    $monitor("sel = %b -> i3 = %0b, i2 = %0b ,i1 = %0b, i0 = %0b -> y = %0b", sel,i3,i2,i1,i0, y);
    {i3,i2,i1,i0} = 4'h5;
    repeat(6) begin
      sel = $random;
      #5;
    end
  end
endmodule
```


41mux - [/home/akshay/41mux/41mux.xpr] - Vivado 2023.2
Layout
View
Help
Quick Access
Implementation Comple
Default Layout
ORATED DESIGN - xc7a35tcpg236-1
Netlist
Nets (7)
Leaf Cells (1)
Project Summary
Schematic
1 Cell
7 I/O Ports
7 Nets
Select an object to see properties
y_i
a
b
c
d
S=2'b00
S=2'b01
S=2'b10
S=2'b11
I0
I1
I2
I3
O
y
S[1:0]
RTL_MUX
sel[1:0]


41mux - [/home/akshay/41mux/41mux.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Implementation Complete
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb
4x1_behav.wcfg
Scope
Sources
Objects
Protocol Instances
Name
Value
sel[1:0]
i0
i1
i2
i3
y
1
1
0
1
0
0
1,000.000 ns
0.000 ns
100.000 ns
200.000 ns
300.000 ns
400.000 ns
500.000 ns
600.000 ns
700.000 ns
800.000 ns
900.000 ns


41mux - [/home/akshay/41mux/41mux.xpr] - Vivado 2023.2
Help
Quick Access
- xc7a35tcpg236-1
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
bject to see properties


41mux - [/home/akshay/41mux/41mux.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Summary
Settings
Summary (0.524 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.452 W)
Signals (0.02 W)
Data (0.02 W)
Logic (0.004 W)
I/O (0.428 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.524 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 27.6°C
Thermal Margin: 57.4°C (11.4 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
86%
14%
95%
Dynamic: 0.452 W (86%)
Signals: 0.020 W (4%)
Logic: 0.004 W (1%)
I/O: 0.428 W (95%)
Device Static: 0.071 W (14%)

Assignment-4

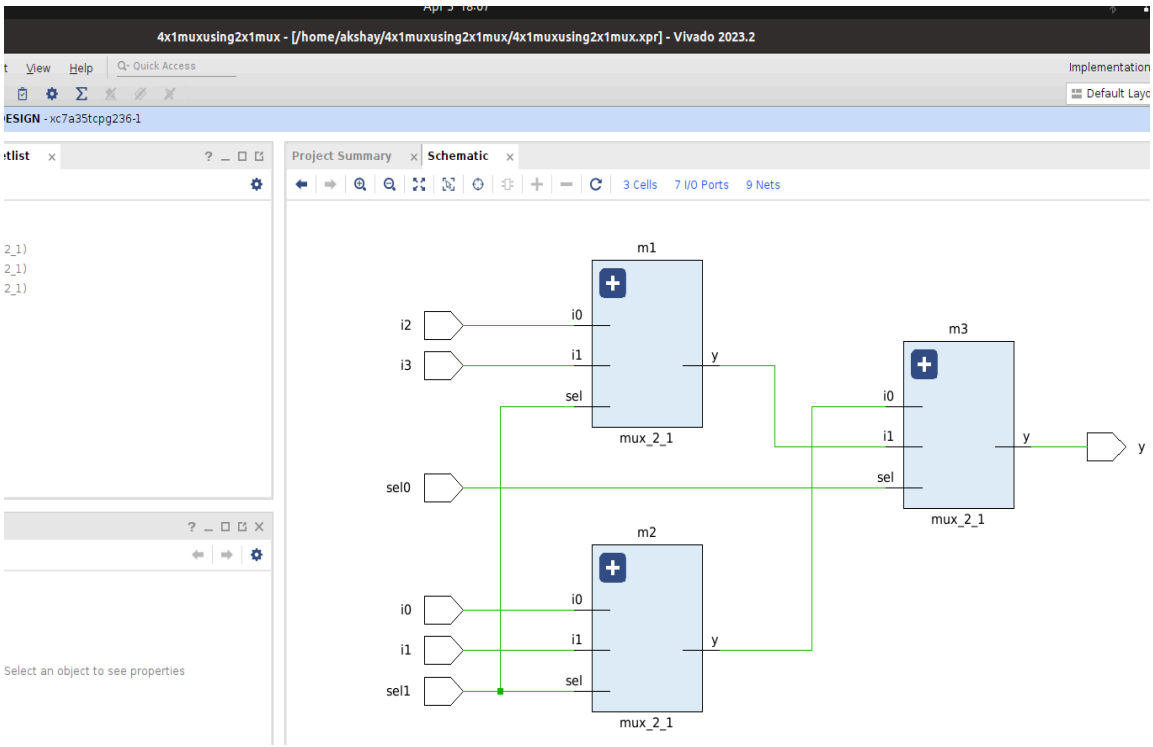
Q.11 Write a Verilog code for 4:1 MUX using 2:1 Mux.

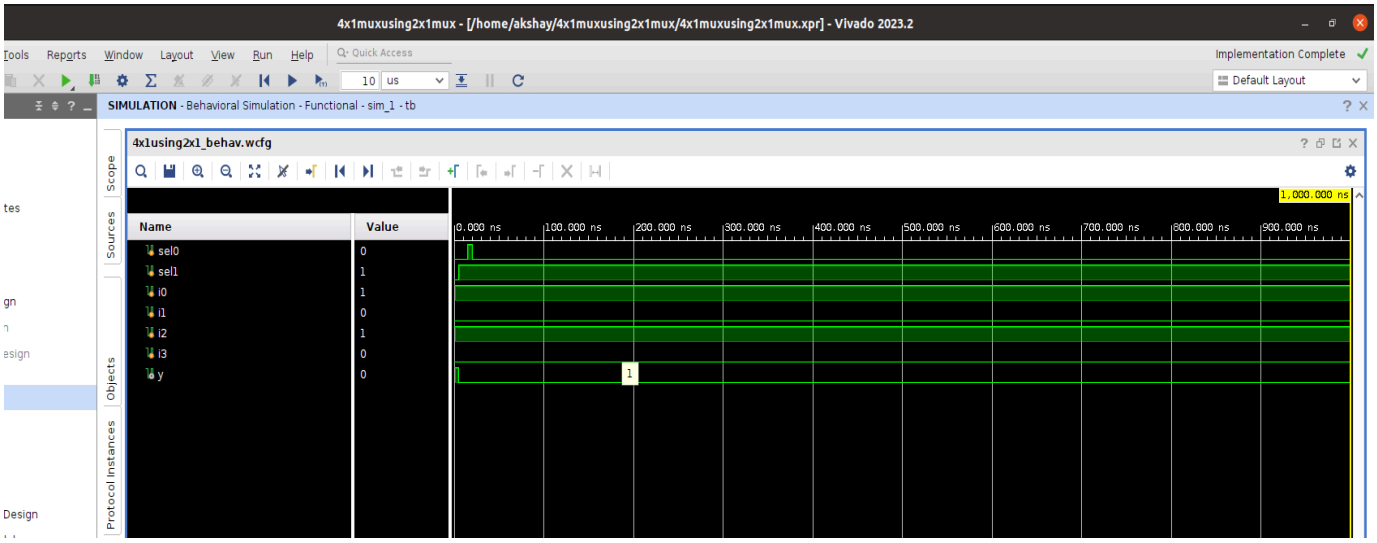
```
module mux_2_1(
  input sel,
  input i0, i1,
  output y);
  assign y = sel ? i1 : i0;
endmodule

module mux_4_1(
  input sel0, sel1,
  input  i0,i1,i2,i3,
  output  y);
   wire y0, y1;
   mux_2_1 m1(sel1, i2, i3, y1);
  mux_2_1 m2(sel1, i0, i1, y0);
  mux_2_1 m3(sel0, y0, y1, y);
endmodule
```

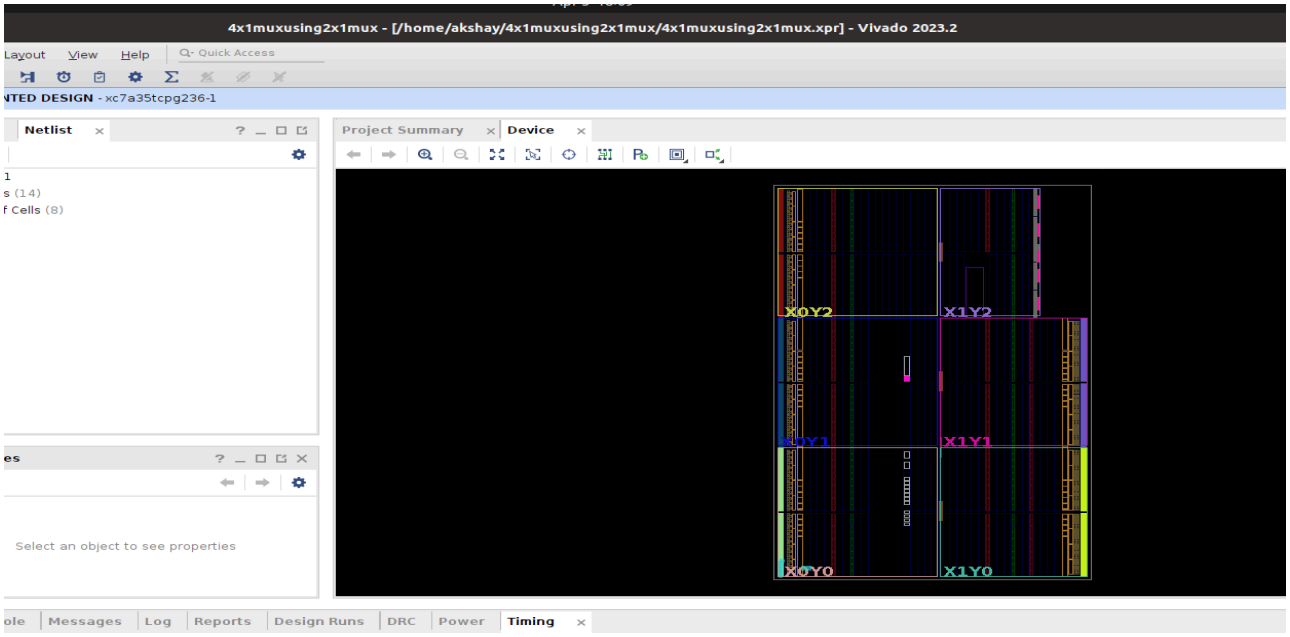
Testbench Code:

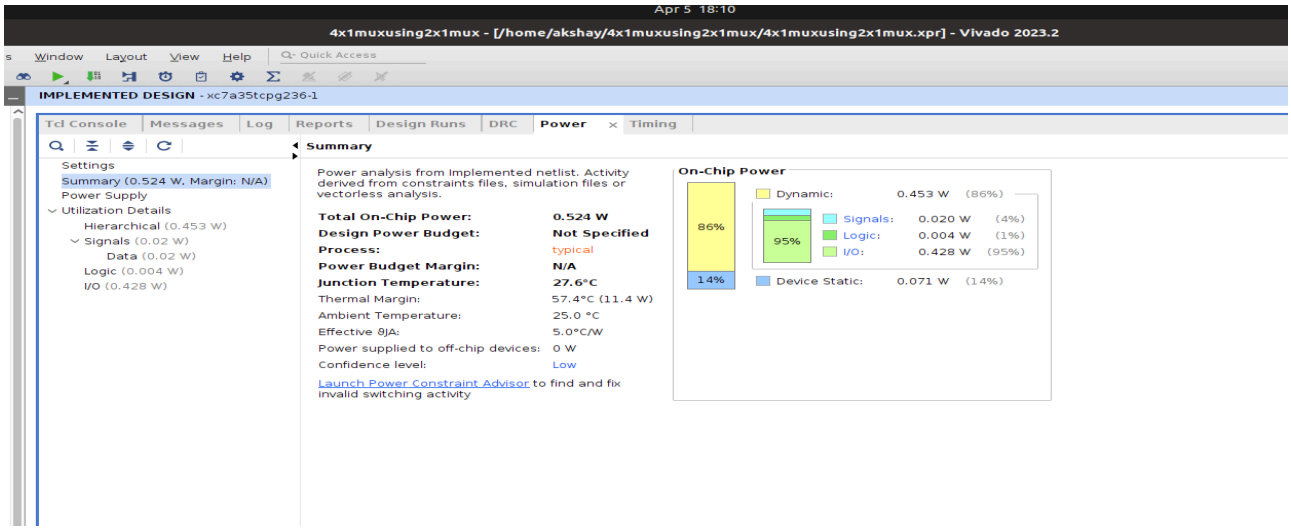
```
module tb;
  reg sel0, sel1;
  reg i0,i1,i2,i3;
  wire y;
```

```
 mux_4_1 mux(sel0, sel1, i0, i1, i2, i3, y);

  initial begin

   $monitor("sel0=%b, sel1=%b -> i3 = %0b, i2 = %0b ,i1 = %0b, i0 = %0b -> y = %0b",
sel0,sel1,i3,i2,i1,i0, y);

   {i3,i2,i1,i0} = 4'h5;

repeat(6) begin

     {sel0, sel1} = $random;

     #5;

   end

 end

endmodule
```




4x1muxusing2x1mux - [/home/akshay/4x1muxusing2x1mux/4x1muxusing2x1mux.xpr] - Vivado 2023.2
Implementation Complete
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb
4x1using2x1_behav.wcfg
Name
Value
sel0
sel1
i0
i1
i2
i3
y
1,000.000 ns


4x1muxusing2x1mux - [/home/akshay/4x1muxusing2x1mux/4x1muxusing2x1mux.xpr] - Vivado 2023.2
Netlist
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Select an object to see properties
Messages
Log
Reports
Design Runs
DRC
Power
Timing

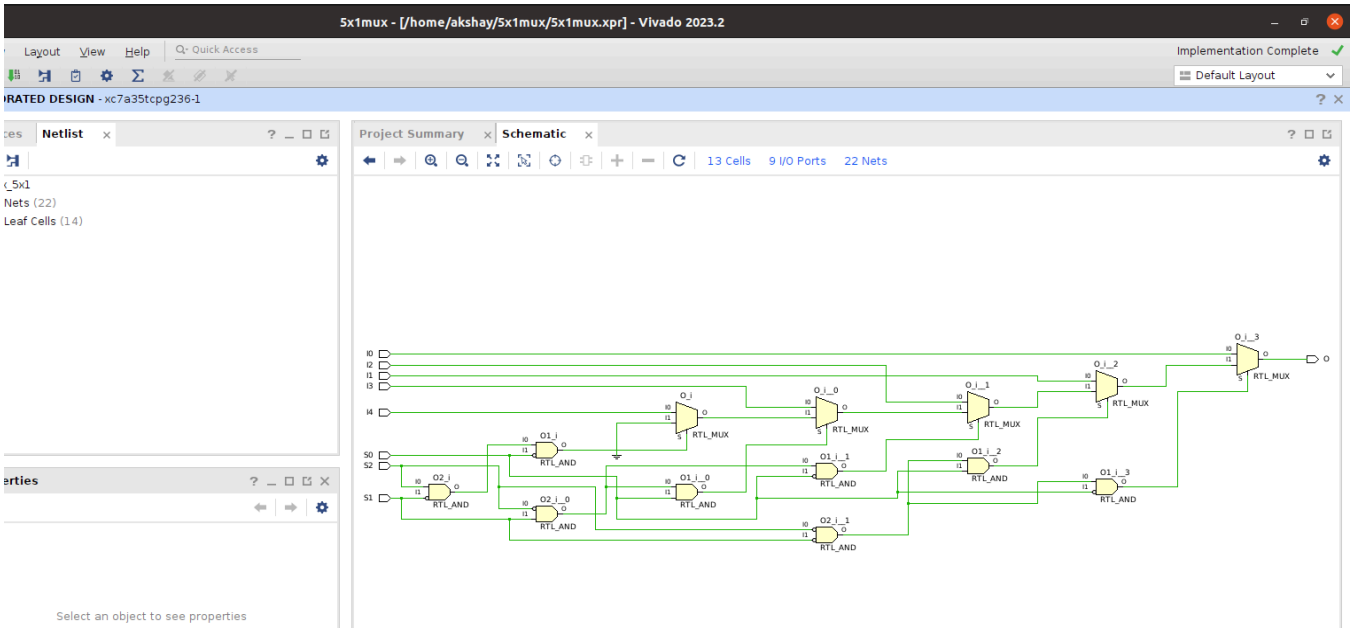

Apr 5 18:10
4x1muxusing2x1mux - [/home/akshay/4x1muxusing2x1mux/4x1muxusing2x1mux.xpr] - Vivado 2023.2
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Summary
Settings
Summary (0.524 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.453 W)
Signals (0.02 W)
Data (0.02 W)
Logic (0.004 W)
I/O (0.428 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.524 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 27.6°C
Thermal Margin: 57.4°C (11.4 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
Dynamic: 0.453 W (86%)
Signals: 0.020 W (4%)
Logic: 0.004 W (1%)
I/O: 0.428 W (95%)
Device Static: 0.071 W (14%)

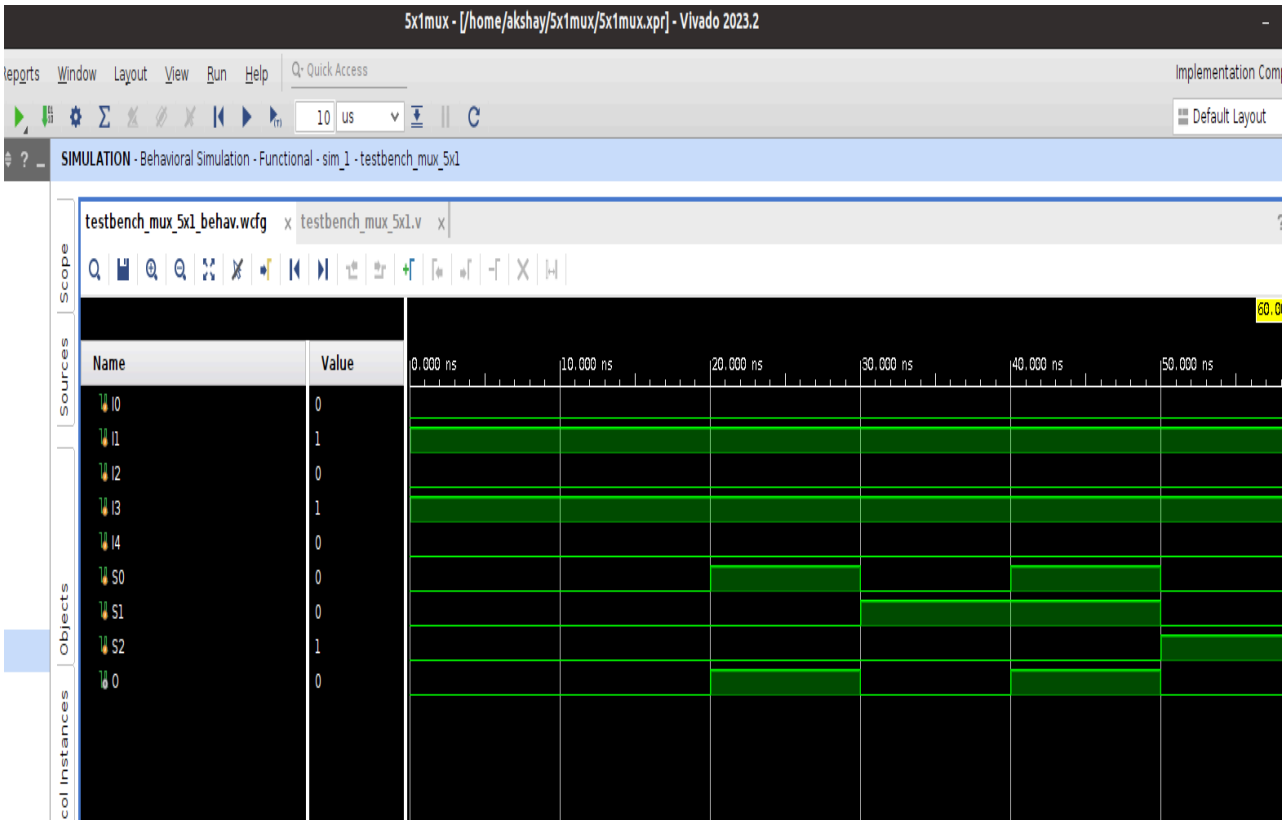
Q.12.> Write a Verilog code for 5:1 MUX.

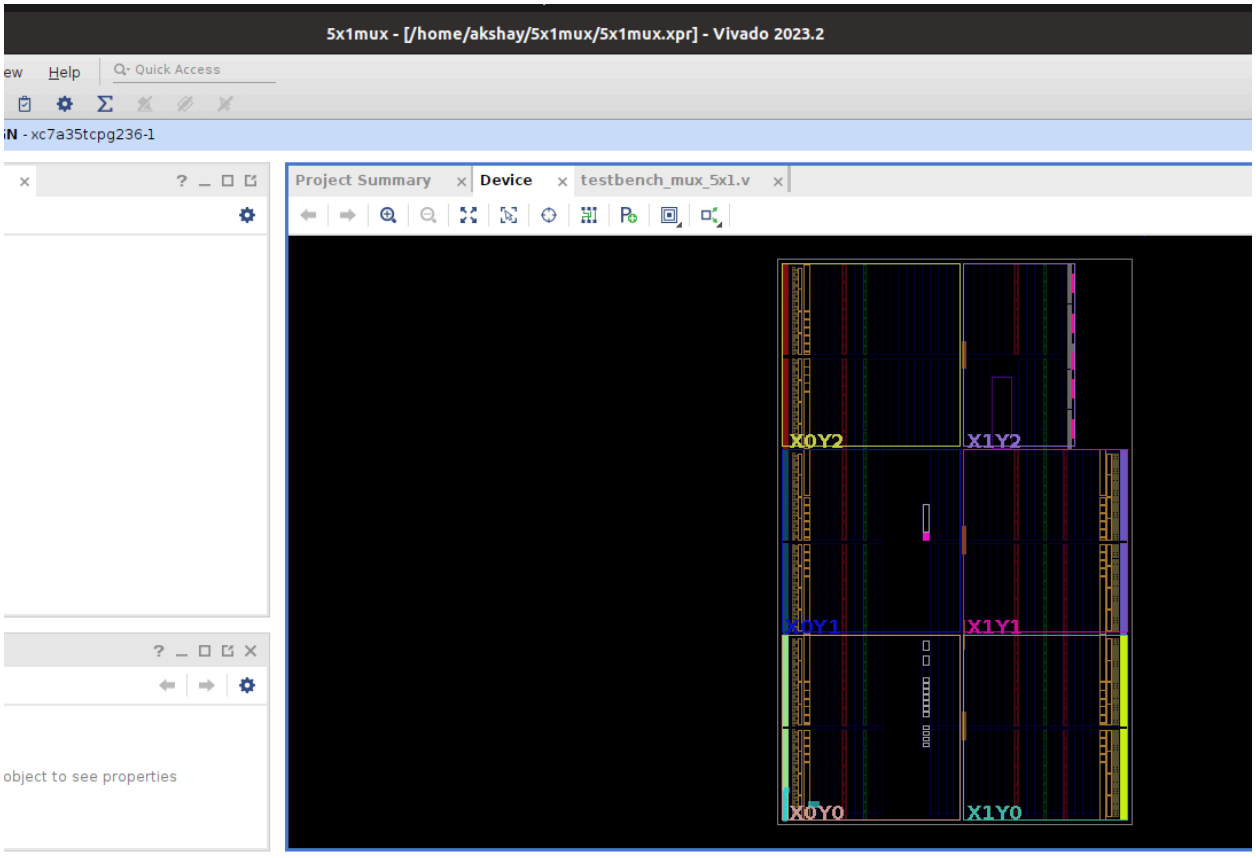
```
module mux_5x1(
  input I0, I1, I2, I3, I4,  // Inputs to select from
  input S0, S1, S2,          // Selection lines
  output reg O               // Output
);
reg not_S0, not_S1, not_S2;
always @* begin
  not_S0 = ~S0;
  not_S1 = ~S1;
  not_S2 = ~S2;
  if (~S2 & ~S1 & ~S0)
    O = I0;
  else if (~S2 & ~S1 & S0)
    O = I1;
  else if (~S2 & S1 & ~S0)
    O = I2;
  else if (~S2 & S1 & S0)
    O = I3;
  else if (S2 & ~S1 & ~S0)
    O = I4;
  else
    O = 0; // Default case
end
Endmodule
```

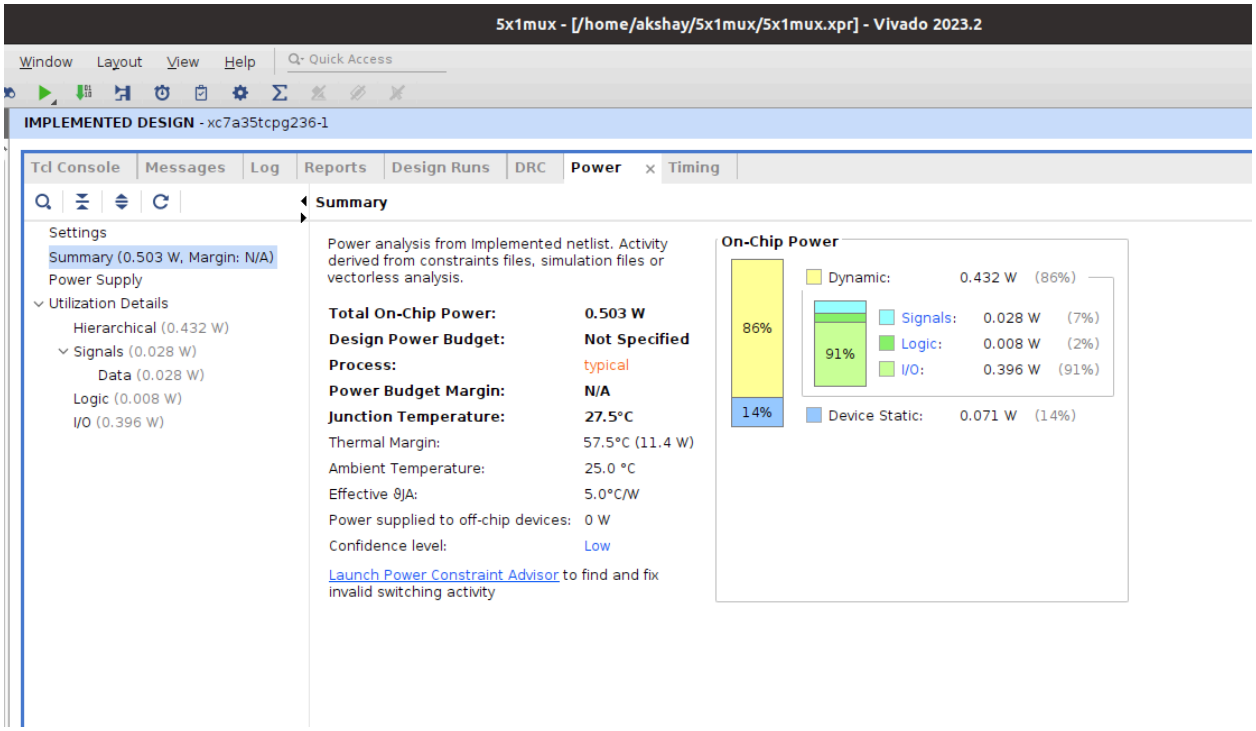
Testbench Code:

```
module testbench_mux_5x1;
  // Inputs  reg I0, I1, I2, I3, I4;
              reg S0, S1, S2;
  // Output    wire O;
  // Instantiate the 5x1 multiplexer module
  mux_5x1 dut(I0,I1,I2,I3,I4,S0,S1,S2,O);
  // Initialize inputs
  initial begin
    I0 = 1'b0;
    I1 = 1'b1;
    I2 = 1'b0;
    I3 = 1'b1;
    I4 = 1'b0;
    S0 = 1'b0;
    S1 = 1'b0;
    S2 = 1'b0;    #10;
    S0 = 1'b0; S1 = 1'b0; S2 = 1'b0;  #10;
    S0 = 1'b1; S1 = 1'b0; S2 = 1'b0; #10;
    S0 = 1'b0; S1 = 1'b1; S2 = 1'b0;   #10;
    S0 = 1'b1; S1 = 1'b1; S2 = 1'b0;  #10;
    S0 = 1'b0; S1 = 1'b0; S2 = 1'b1;     #10;
    $finish;
  end
Endmodule
```


5x1mux - [/home/akshay/5x1mux/5x1mux.xpr] - Vivado 2023.2
Layout
View
Help
Quick Access
Implementation Complete
Default Layout
RATED DESIGN - xc7a35tcpg236-1
Netlist
Nets (22)
Leaf Cells (14)
Project Summary
Schematic
13 Cells
9 I/O Ports
22 Nets
RTL_MUX
RTL_AND
Select an object to see properties


5x1mux - [/home/akshay/5x1mux/5x1mux.xpr] - Vivado 2023.2
Reports
Window
Layout
View
Run
Help
Quick Access
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - testbench_mux_5x1
testbench_mux_5x1_behav.wcfg
testbench_mux_5x1.v
Scope
Sources
Objects
Name
Value
I0
I1
I2
I3
I4
S0
S1
S2
O
0
1
0
1
0
0
0
1
0
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns


5x1mux - [/home/akshay/5x1mux/5x1mux.xpr] - Vivado 2023.2
Help
Quick Access
xc7a35tcpg236-1
Project Summary
Device
testbench_mux_5x1.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
object to see properties
Log
Reports
Design Runs
DRC
Power
Timing


5x1mux - [/home/akshay/5x1mux/5x1mux.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Summary
Settings
Summary (0.503 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.432 W)
Signals (0.028 W)
Data (0.028 W)
Logic (0.008 W)
I/O (0.396 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.503 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 27.5°C
Thermal Margin: 57.5°C (11.4 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
86%
14%
91%
Dynamic: 0.432 W (86%)
Signals: 0.028 W (7%)
Logic: 0.008 W (2%)
I/O: 0.396 W (91%)
Device Static: 0.071 W (14%)

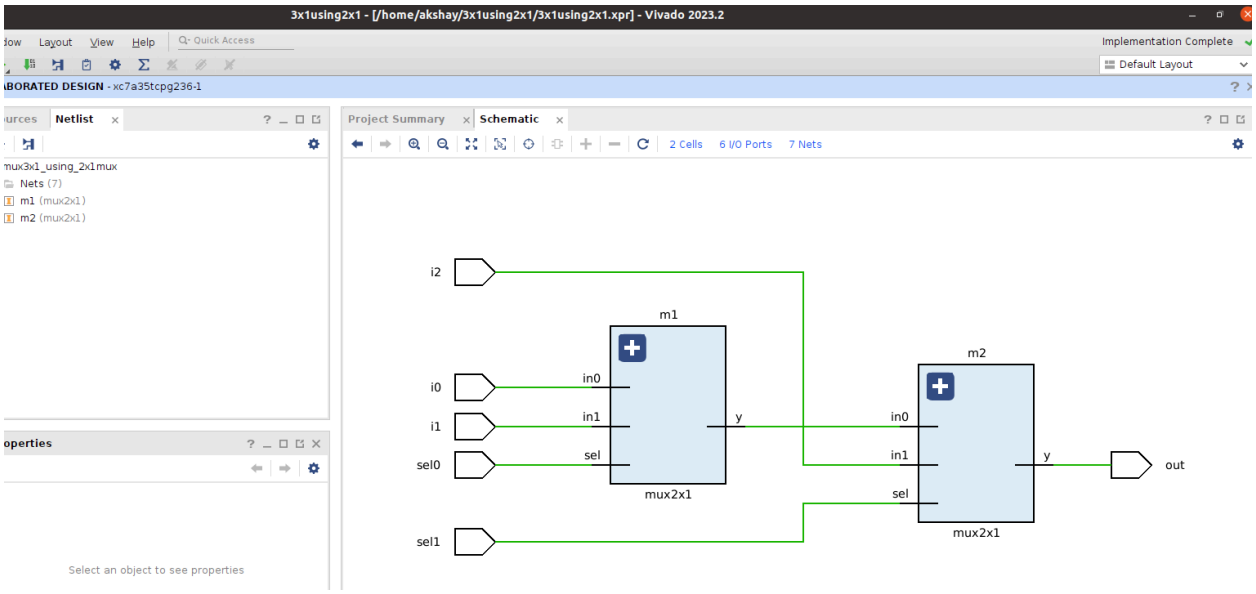
Q.13.> Write a Verilog code for 3:1 MUX using 2:1 MUX.

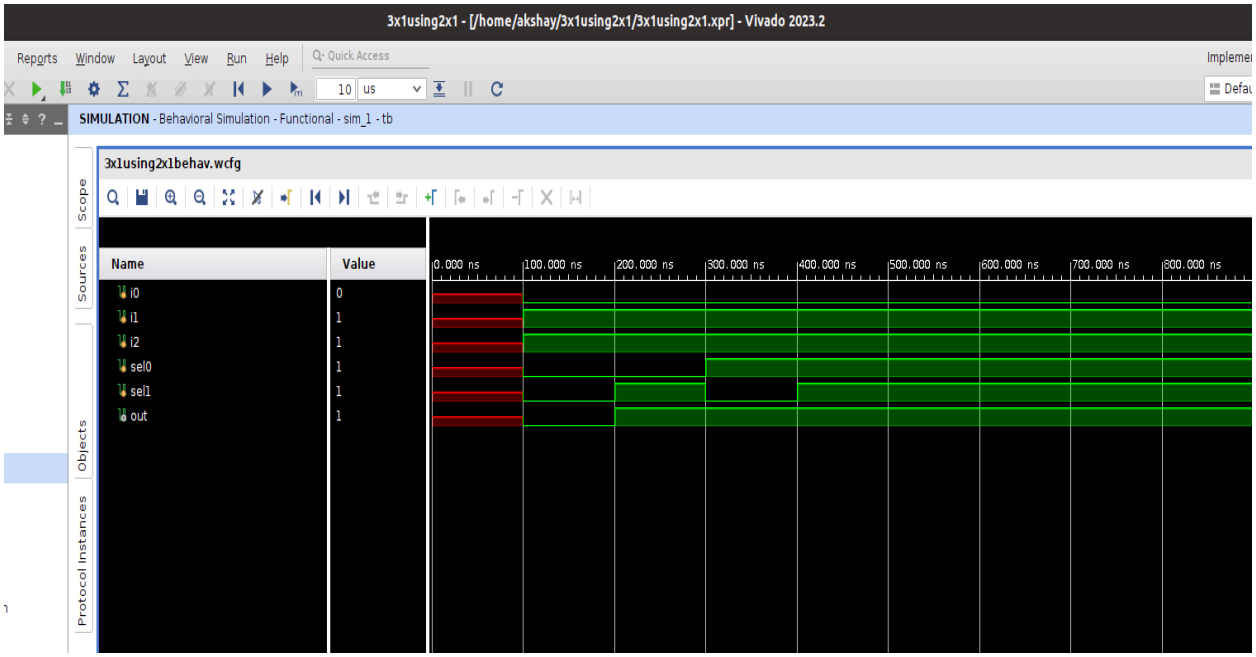
```
module mux2x1(y,sel,in0,in1);
  input in0,in1,sel;
  output y;
    assign y = sel ? in1 : in0;
  endmodule


module mux3x1_using_2x1mux(out,i0,i1,i2,sel0,sel1);
  input i0,i1,i2;
  input sel0,sel1;
  output out;
    wire o1;
  mux2x1 m1(o1,sel0,i0,i1);
  mux2x1 m2(out,sel1,o1,i2);
endmodule
```

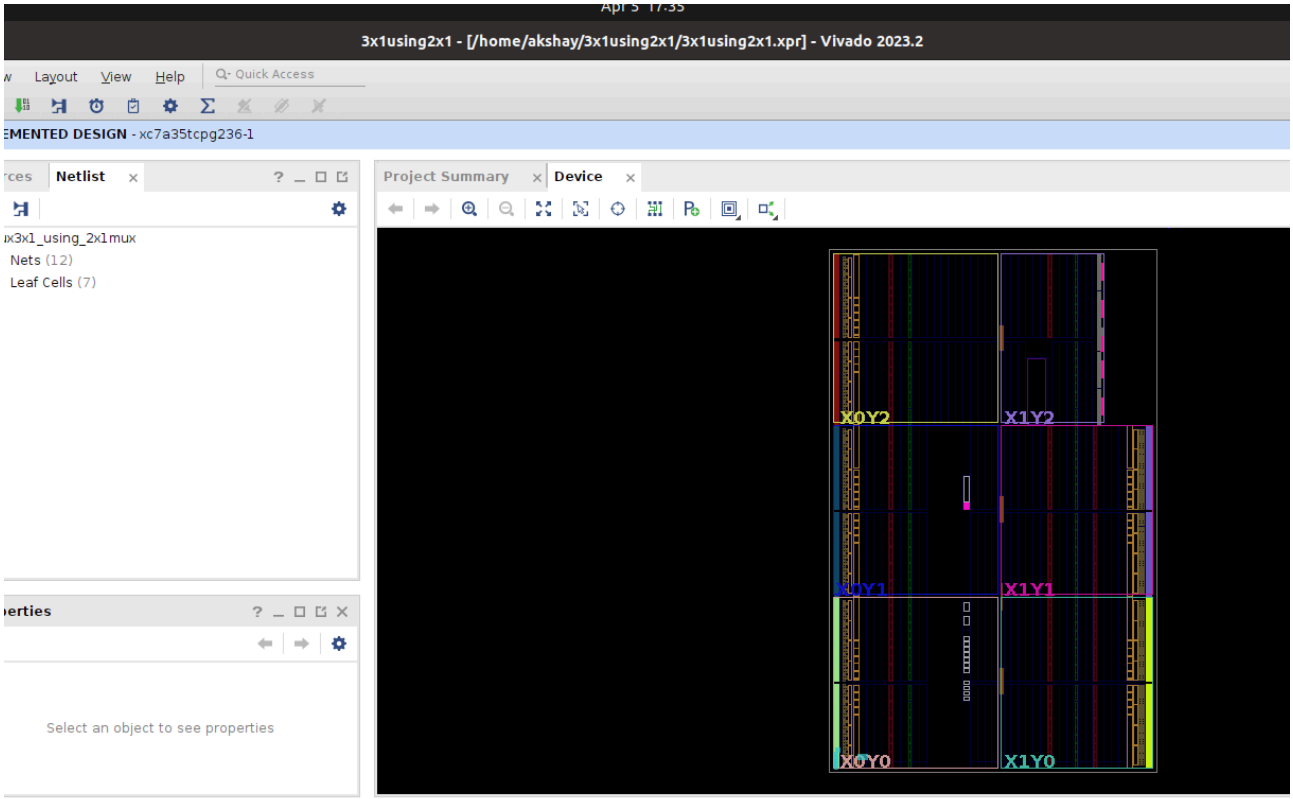
Testbench Code:

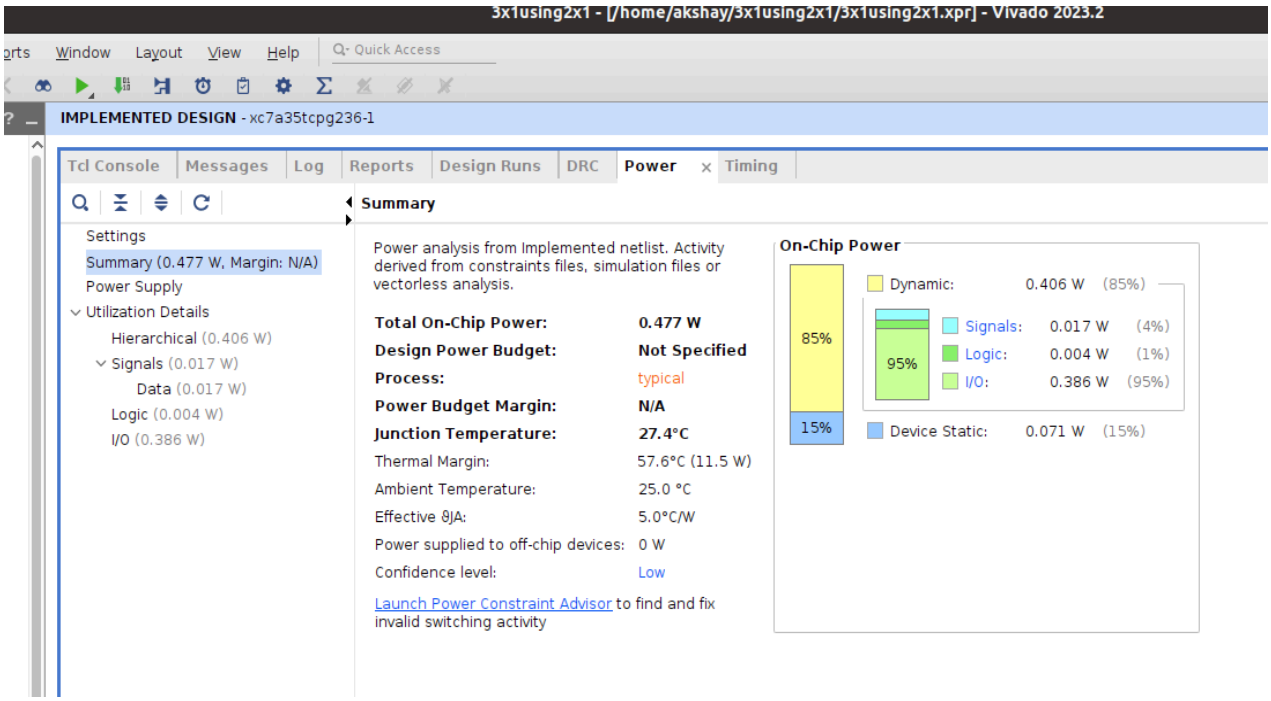
```
module tb;
  reg i0,i1,i2,sel0,sel1;
  wire out;
   mux3x1_using_2x1mux dut(out,i0,i1,i2,sel0,sel1);
  initial begin  #100;
    i0=0 ;i1=1; i2=1;
    sel0 =0; sel1=0;#100;
    sel0 =0; sel1=1;#100;
```

```
    sel0 =1; sel1=0;  #100;

    sel0 =1; sel1=1;    #100;

  end

endmodule
```






3x1using2x1 - [/home/akshay/3x1using2x1/3x1using2x1.xpr] - Vivado 2023.2
Layout
View
Help
Quick Access
IMENTED DESIGN - xc7a35tcpg236-1
Netlist
x3x1_using_2x1mux
Nets (12)
Leaf Cells (7)
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
perties
Select an object to see properties
Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing


3x1using2x1 - [/home/akshay/3x1using2x1/3x1using2x1.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Summary
Settings
Summary (0.477 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.406 W)
Signals (0.017 W)
Data (0.017 W)
Logic (0.004 W)
I/O (0.386 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.477 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 27.4°C
Thermal Margin: 57.6°C (11.5 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
85%
15%
95%
Dynamic: 0.406 W (85%)
Signals: 0.017 W (4%)
Logic: 0.004 W (1%)
I/O: 0.386 W (95%)
Device Static: 0.071 W (15%)

Q.14.> Write a Verilog code for DEMUX .

a.> 1:2 Demux b.> 1:4 Demux

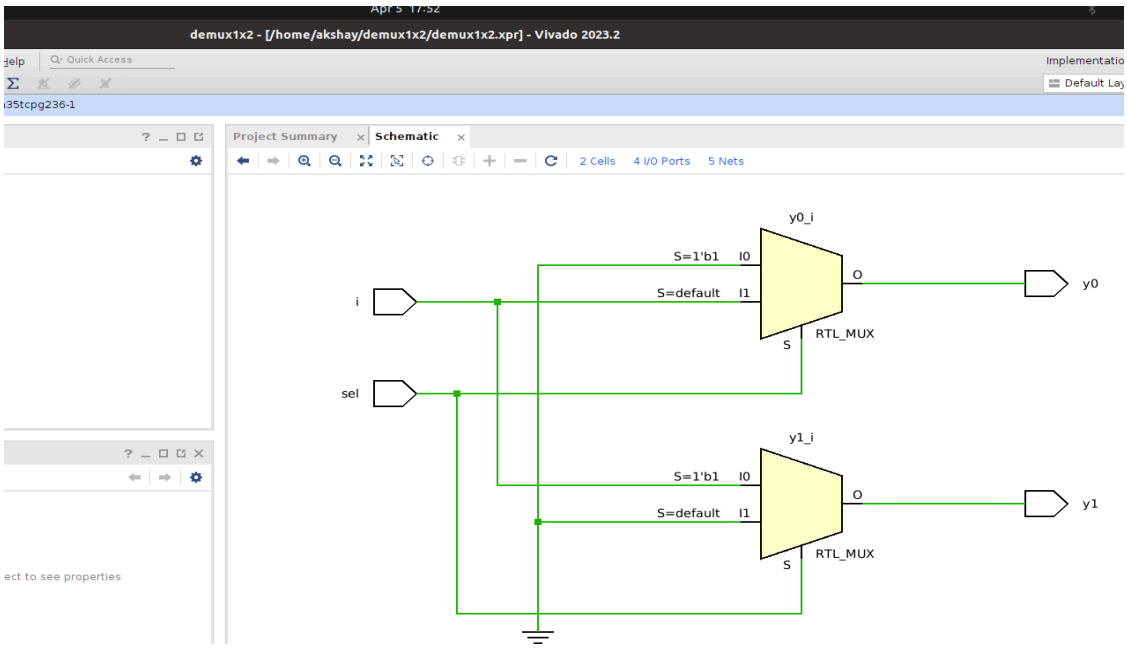
Soln for 1:2 Demux

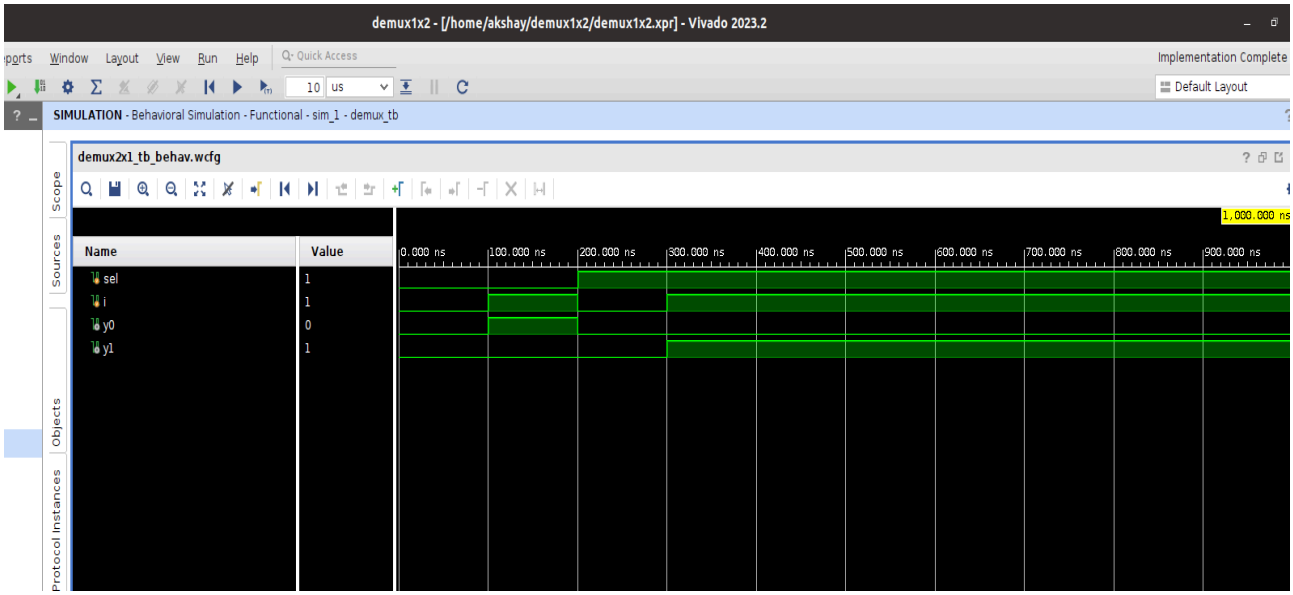
```
module demux_2_1(
  input sel,
  input i,
  output reg y0, y1
);
always @* begin
    if (sel) begin
      y0 = 1'b0;
      y1 = i;
    end
    else begin
      y0 = i;
      y1 = 1'b0;
    end
  end
  endmodule
```

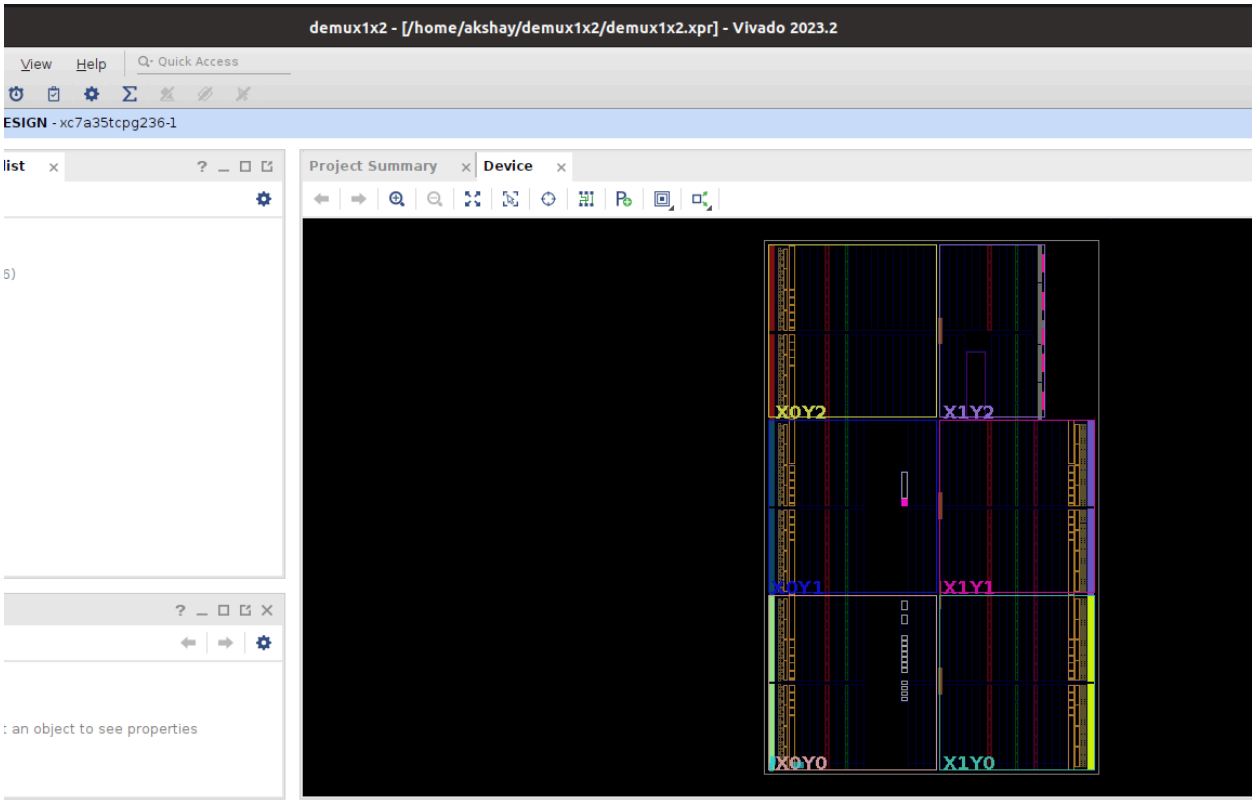
Testbench

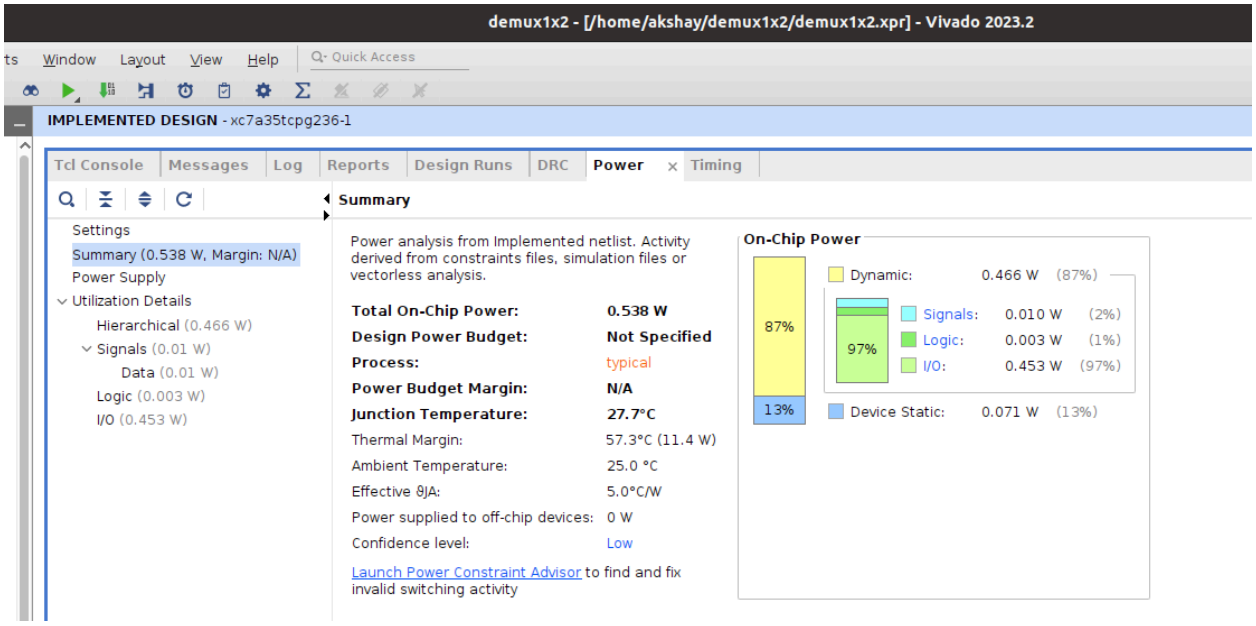
```
module demux_tb;
  reg sel, i;
  wire y0, y1;
    demux_2_1 dut(sel, i, y0, y1);
  initial begin
```

```
    $monitor("sel = %h: i = %h --> y0 = %h, y1 = %h", sel, i, y0, y1);
    sel=0; i=0; #100;
    sel=0; i=1; #100;
    sel=1; i=0; #100;
    sel=1; i=1; #100;
  end
Endmodule
```






demux1x2 - [/home/akshay/demux1x2/demux1x2.xpr] - Vivado 2023.2
View
Help
Quick Access
ESIGN - xc7a35tcpg236-1
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
: an object to see properties


demux1x2 - [/home/akshay/demux1x2/demux1x2.xpr] - Vivado 2023.2
ts
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Summary
Settings
Summary (0.538 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.466 W)
Signals (0.01 W)
Data (0.01 W)
Logic (0.003 W)
I/O (0.453 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.538 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 27.7°C
Thermal Margin: 57.3°C (11.4 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
87%
13%
97%
Dynamic: 0.466 W (87%)
Signals: 0.010 W (2%)
Logic: 0.003 W (1%)
I/O: 0.453 W (97%)
Device Static: 0.071 W (13%)

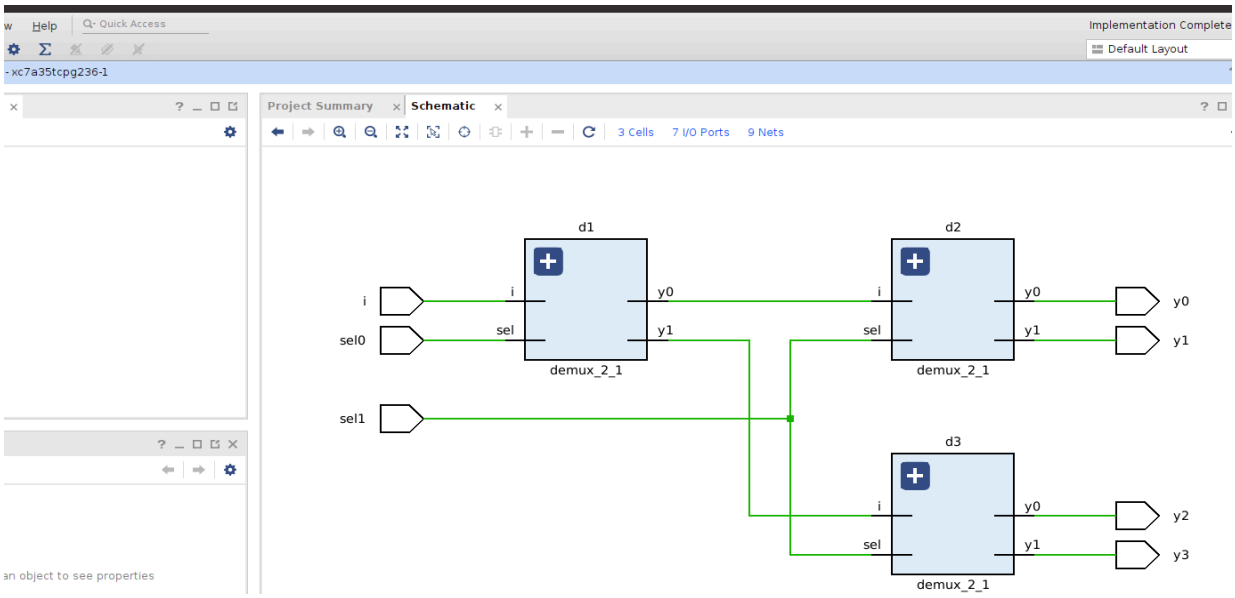
Soln for 1:4 Demux.

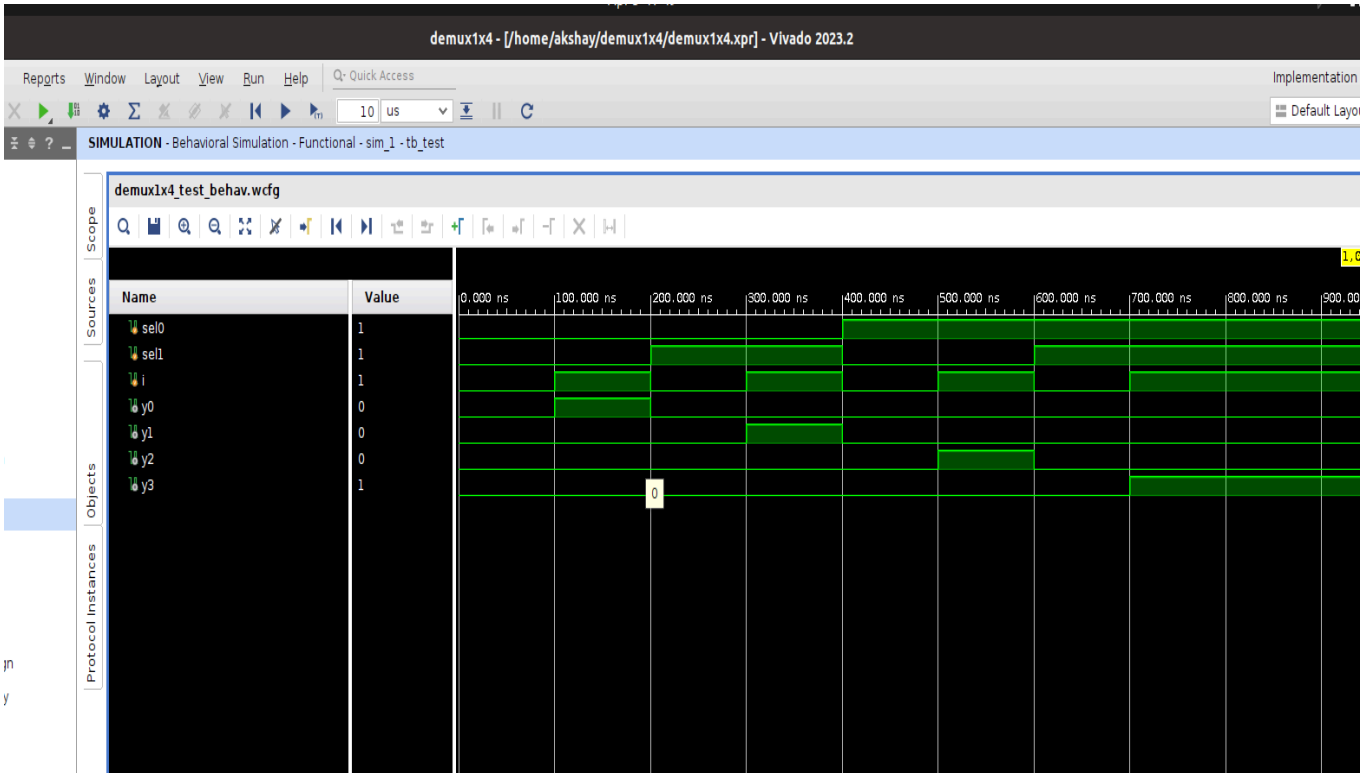
```
module demux_1_4(
  input [1:0] sel,
  input  i,
  output reg y0,y1,y2,y3);
     always @(*) begin
    case(sel)
      2'h0: {y0,y1,y2,y3} = {i,3'b0};
      2'h1: {y0,y1,y2,y3} = {1'b0,i,2'b0};
      2'h2: {y0,y1,y2,y3} = {2'b0,i,1'b0};
      2'h3: {y0,y1,y2,y3} = {3'b0,i};
      default: $display("Invalid sel input");
    endcase
  end
endmodule
```

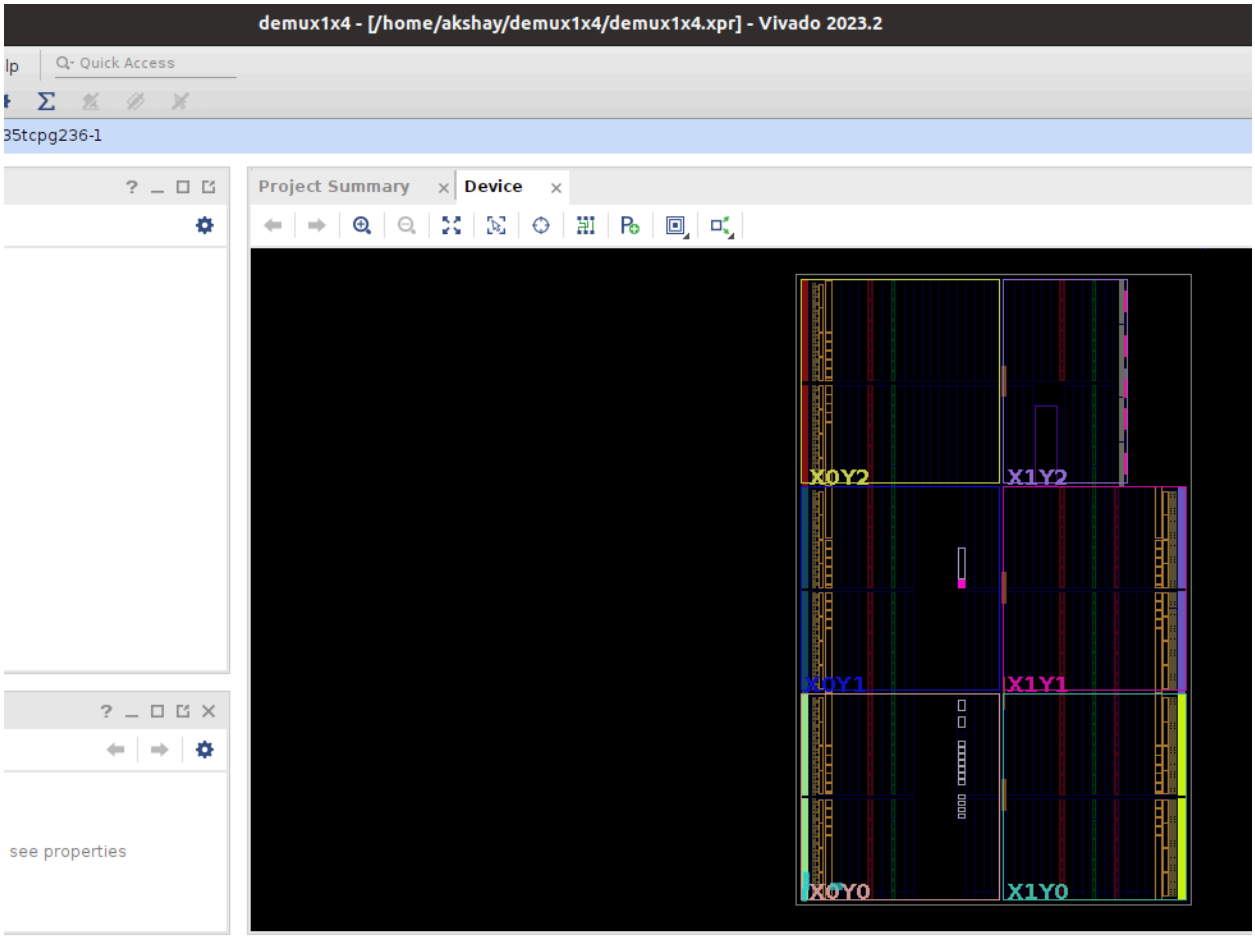
Testbench

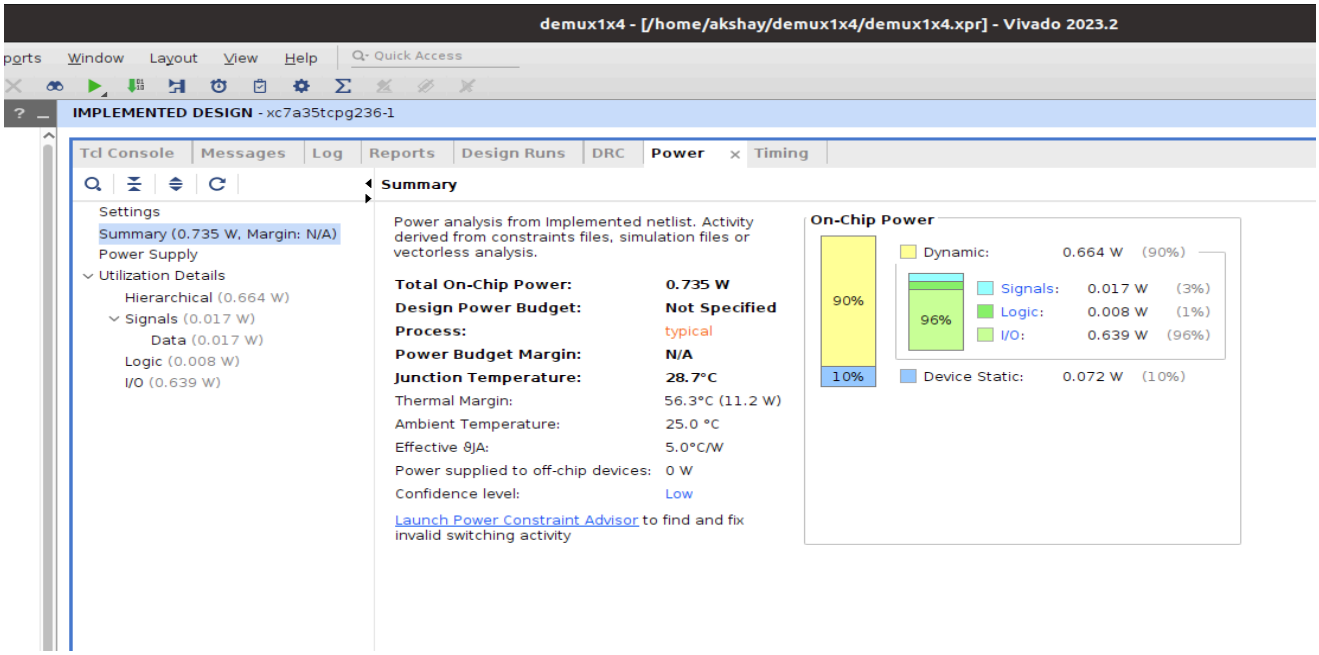
```
module tb;
  reg [1:0] sel;
  reg i;
  wire y0,y1,y2,y3;
  demux_1_4 dut(sel, i, y0, y1, y2, y3);
    initial begin
    $monitor("sel = %b, i = %b -> y0 = %0b, y1 = %0b ,y2 = %0b, y3 = %0b", sel,i, y0,y1,y2,y3);
    sel=2'b00; i=0; #100;      sel=2'b00; i=1; #100;
    sel=2'b01; i=0; #100;      sel=2'b01; i=1; #100;
```

```
    sel=2'b10; i=0; #100;      sel=2'b10; i=1; #100;
    sel=2'b11; i=0; #100;      sel=2'b11; i=1; #100;
  end
Endmodule
```






demux1x4 - [/home/akshay/demux1x4/demux1x4.xpr] - Vivado 2023.2
Quick Access
35tcpg236-1
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
see properties
Log
Reports
Design Runs
DRC
Power
Timing
Design Timing Summary


demux1x4 - [/home/akshay/demux1x4/demux1x4.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Summary
Settings
Summary (0.735 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.664 W)
Signals (0.017 W)
Data (0.017 W)
Logic (0.008 W)
I/O (0.639 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.735 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 28.7°C
Thermal Margin: 56.3°C (11.2 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
90%
10%
96%
Dynamic: 0.664 W (90%)
Signals: 0.017 W (3%)
Logic: 0.008 W (1%)
I/O: 0.639 W (96%)
Device Static: 0.072 W (10%)

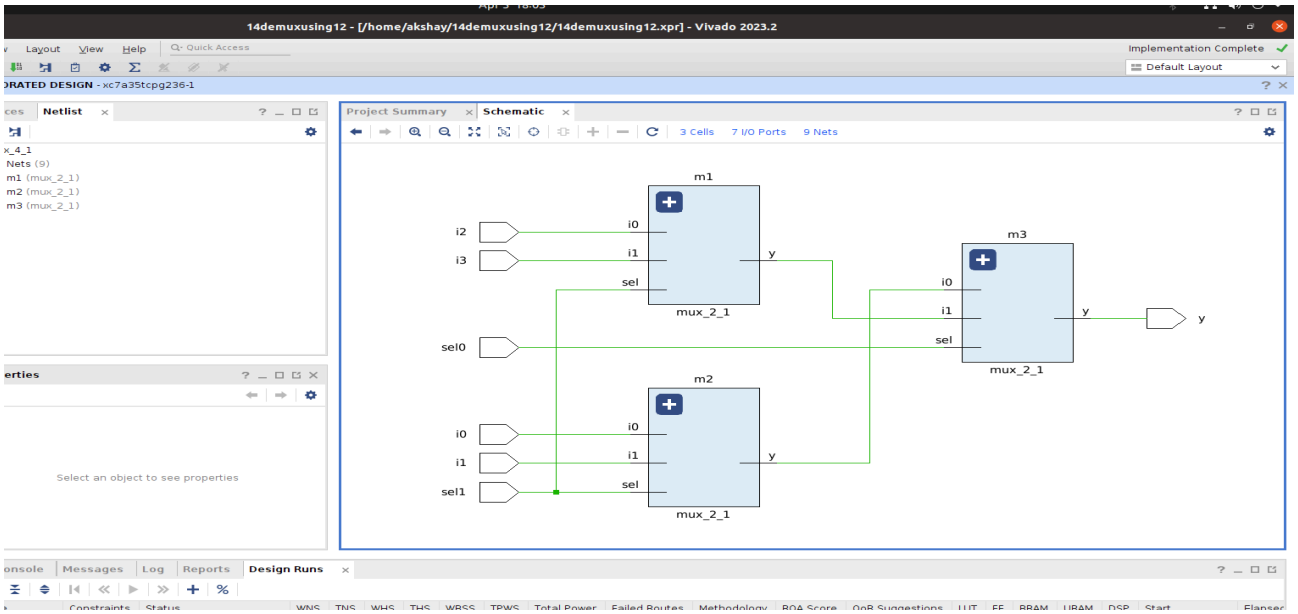
Q.15.> Write a Verilog code for 1:4 DEMUX using 1:2 DEMUX.

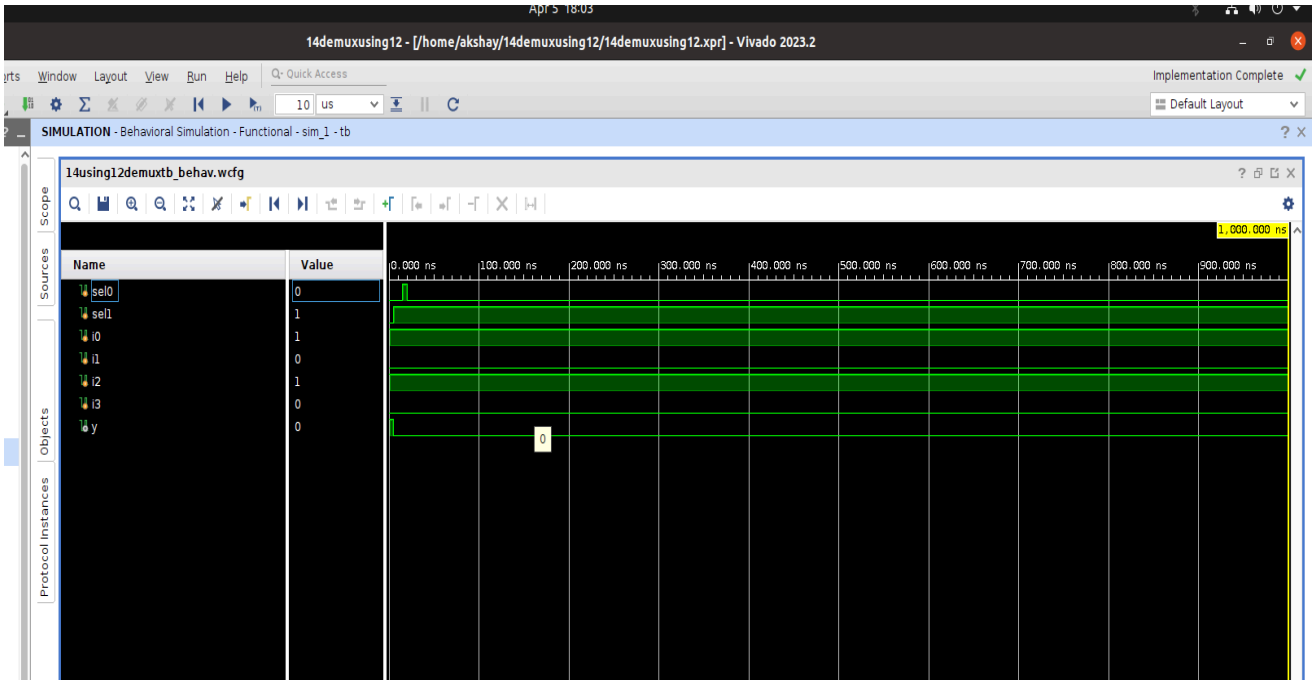
```
module mux_2_1(
  input sel,
  input i0, i1,
  output y);
   assign y = sel ? i1 : i0;
endmodule


module mux_4_1(
  input sel0, sel1,
  input  i0,i1,i2,i3,
  output  y);
  wire y0, y1;
    mux_2_1 m1(sel1, i2, i3, y1);
  mux_2_1 m2(sel1, i0, i1, y0);
  mux_2_1 m3(sel0, y0, y1, y);
endmodule
```

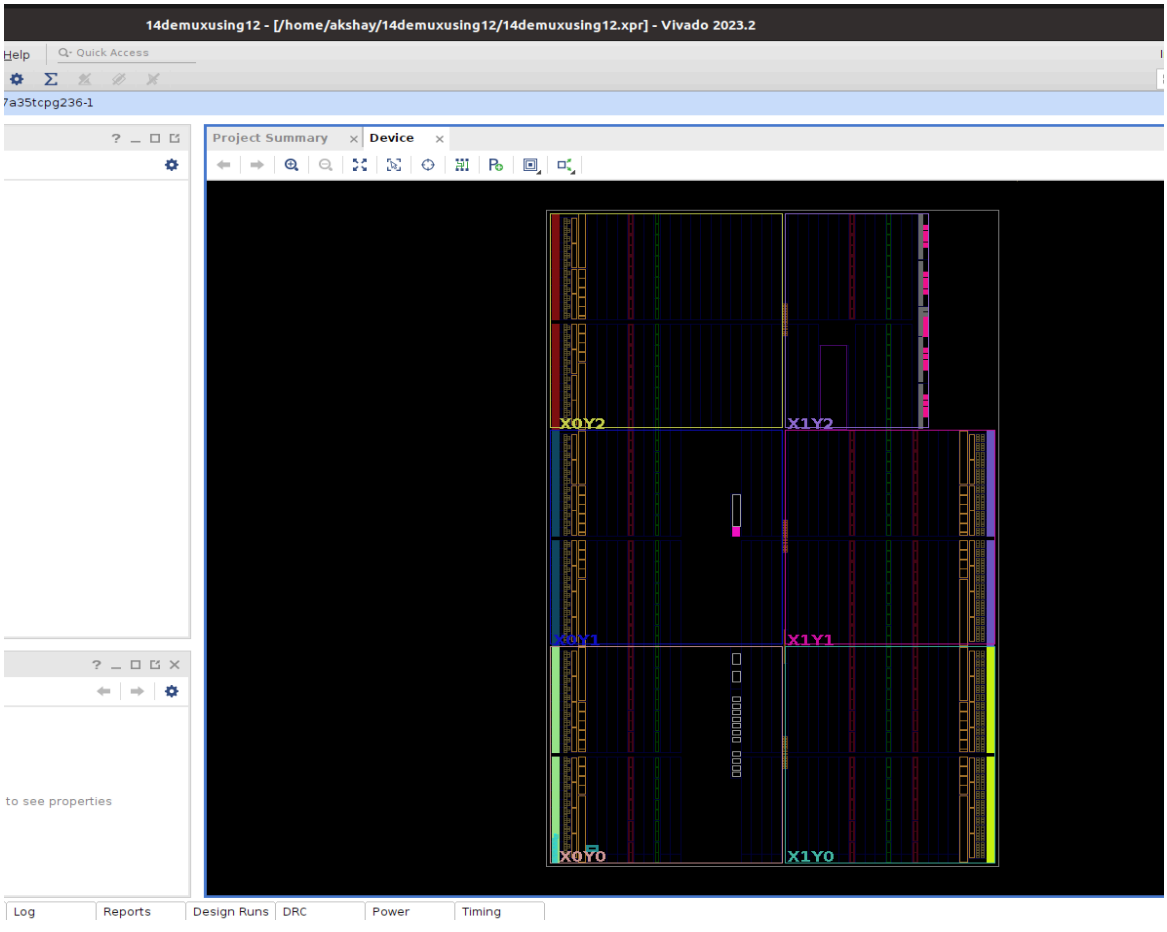
Testbench

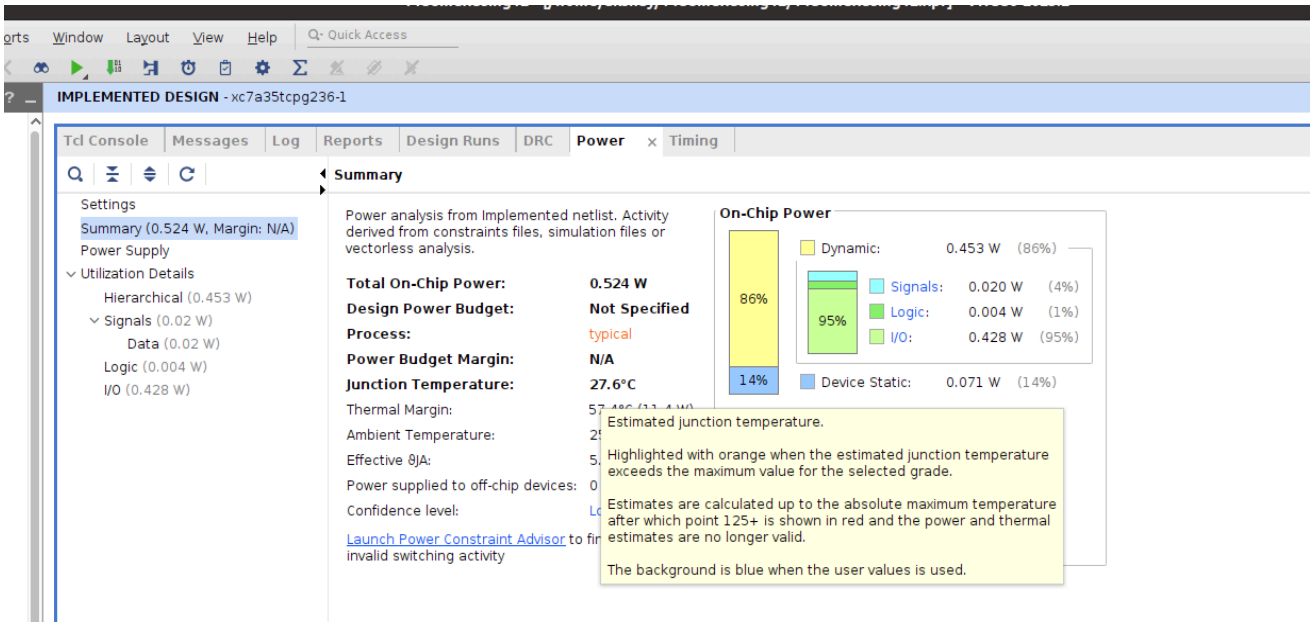
```
module tb;   reg sel0, sel1;  reg i0,i1,i2,i3;
  wire y;    mux_4_1 mux(sel0, sel1, i0, i1, i2, i3, y);
    initial begin
   $monitor("sel0=%b, sel1=%b -> i3 = %0b, i2 = %0b ,i1 = %0b, i0 = %0b -> y = %0b",
sel0,sel1,i3,i2,i1,i0, y);
    {i3,i2,i1,i0} = 4'h5;
    repeat(6) begin
```

```
{sel0, sel1} = $random;     #5;

   end

 end

Endmodule
```






14demuxusing12 - [/home/akshay/14demuxusing12/14demuxusing12.xpr] - Vivado 2023.2
Help
Quick Access
7a35tcpg236-1
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
to see properties
Log
Reports
Design Runs
DRC
Power
Timing


orts
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Settings
Summary (0.524 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.453 W)
Signals (0.02 W)
Data (0.02 W)
Logic (0.004 W)
I/O (0.428 W)
Summary
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.524 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 27.6°C
Thermal Margin:
Ambient Temperature:
Effective θJA:
Power supplied to off-chip devices:
Confidence level:
Launch Power Constraint Advisor to fi
invalid switching activity
On-Chip Power
86%
14%
95%
Dynamic: 0.453 W (86%)
Signals: 0.020 W (4%)
Logic: 0.004 W (1%)
I/O: 0.428 W (95%)
Device Static: 0.071 W (14%)
Estimated junction temperature.
Highlighted with orange when the estimated junction temperature exceeds the maximum value for the selected grade.
Estimates are calculated up to the absolute maximum temperature after which point 125+ is shown in red and the power and thermal estimates are no longer valid.
The background is blue when the user values is used.

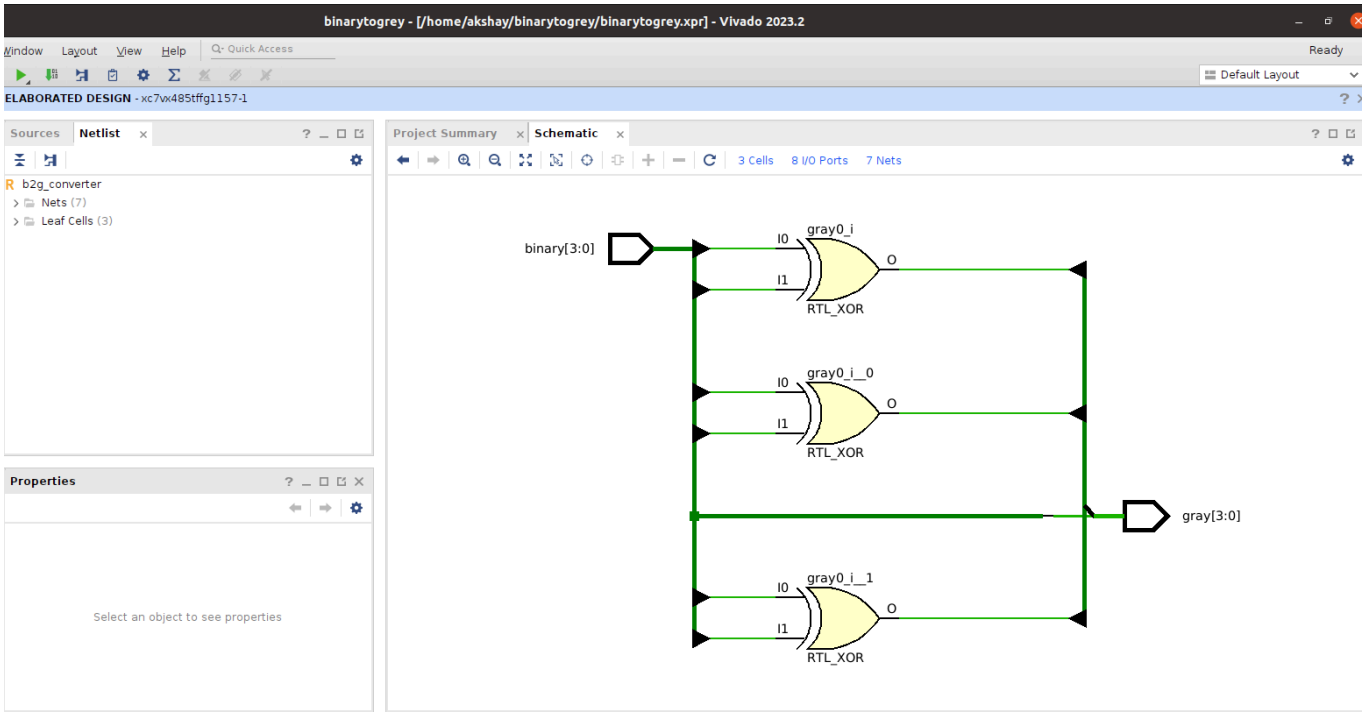
Q.16 Write Verilog code for the following code converters.

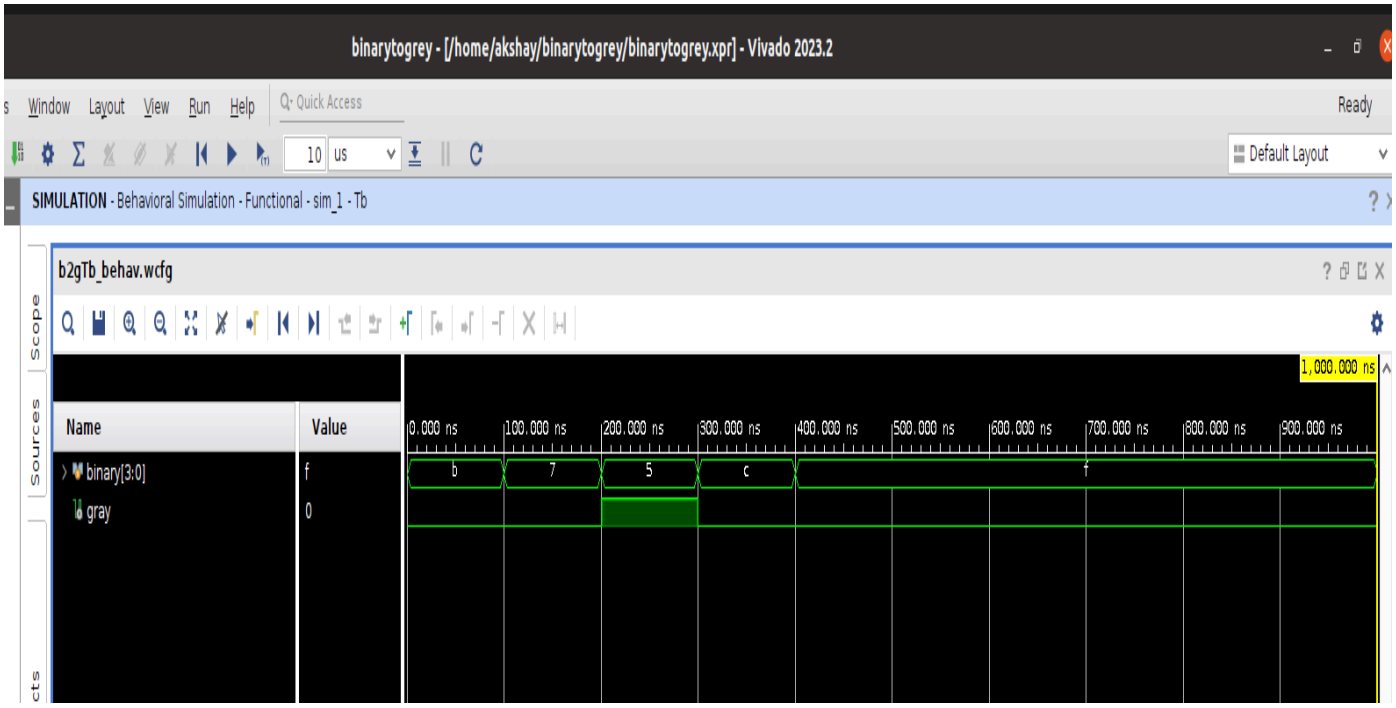
a. Binary to Gray Converter:

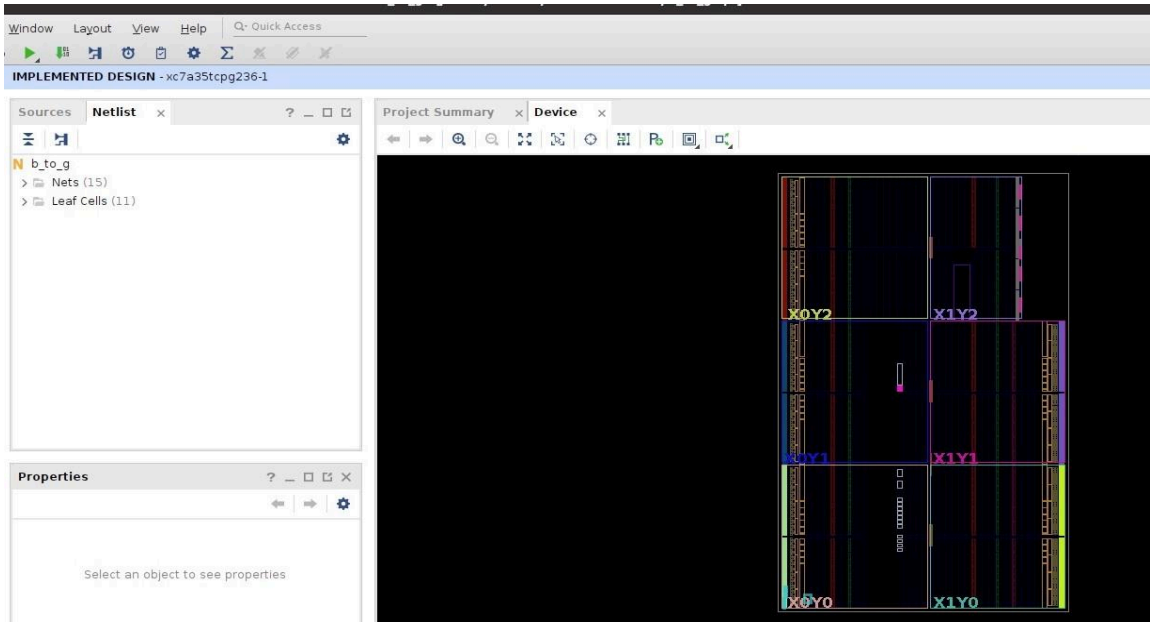
```
module b2g_converter #(parameter WIDTH=4) (input [WIDTH-1:0] binary, output [WIDTH-1:0] gray);

  genvar i;

  generate

    for(i=0;i<WIDTH-1;i=i+1) begin

      assign gray[i] = binary[i] ^ binary[i+1];

    end

  endgenerate

    assign gray[WIDTH-1] = binary[WIDTH-1];

endmodule
```

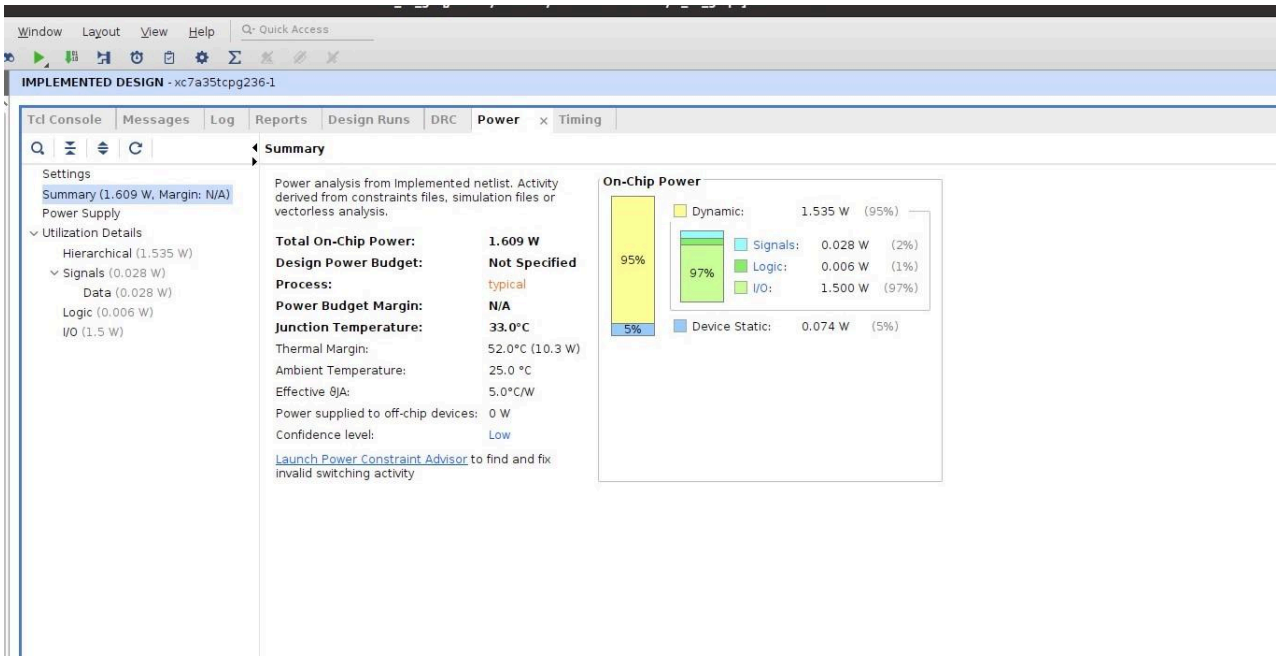
Testbench

```
module Tb();

  reg [3:0] binary;   wire gray;

  b2g_converter b2g(binary, gray);

    initial begin

    $monitor("Binary = %b --> Gray = %b", binary, gray);

    binary = 4'b1011; #100;

    binary = 4'b0111; #100;

    binary = 4'b0101; #100;

    binary = 4'b1100; #100;

    binary = 4'b1111;

  End

endmodule
```


binarytogrey - [/home/akshay/binarytogrey/binarytogrey.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
Ready
Default Layout
ELABORATED DESIGN - xc7vx485tffg1157-1
Sources
Netlist
b2g_converter
Nets (7)
Leaf Cells (3)
Properties
Select an object to see properties
Project Summary
Schematic
3 Cells
8 I/O Ports
7 Nets
binary[3:0]
gray0_i
gray0_i__0
gray0_i__1
I0
I1
O
RTL_XOR
gray[3:0]


binarytogrey - [/home/akshay/binarytogrey/binarytogrey.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Ready
10
us
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - Tb
b2gTb_behav.wcfg
Scope
Sources
Name
Value
binary[3:0]
gray
f
0
1,000.000 ns
0.000 ns
100.000 ns
200.000 ns
300.000 ns
400.000 ns
500.000 ns
600.000 ns
700.000 ns
800.000 ns
900.000 ns
b
7
5
c
f


Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Sources
Netlist
b_to_g
Nets (15)
Leaf Cells (11)
Properties
Select an object to see properties
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0

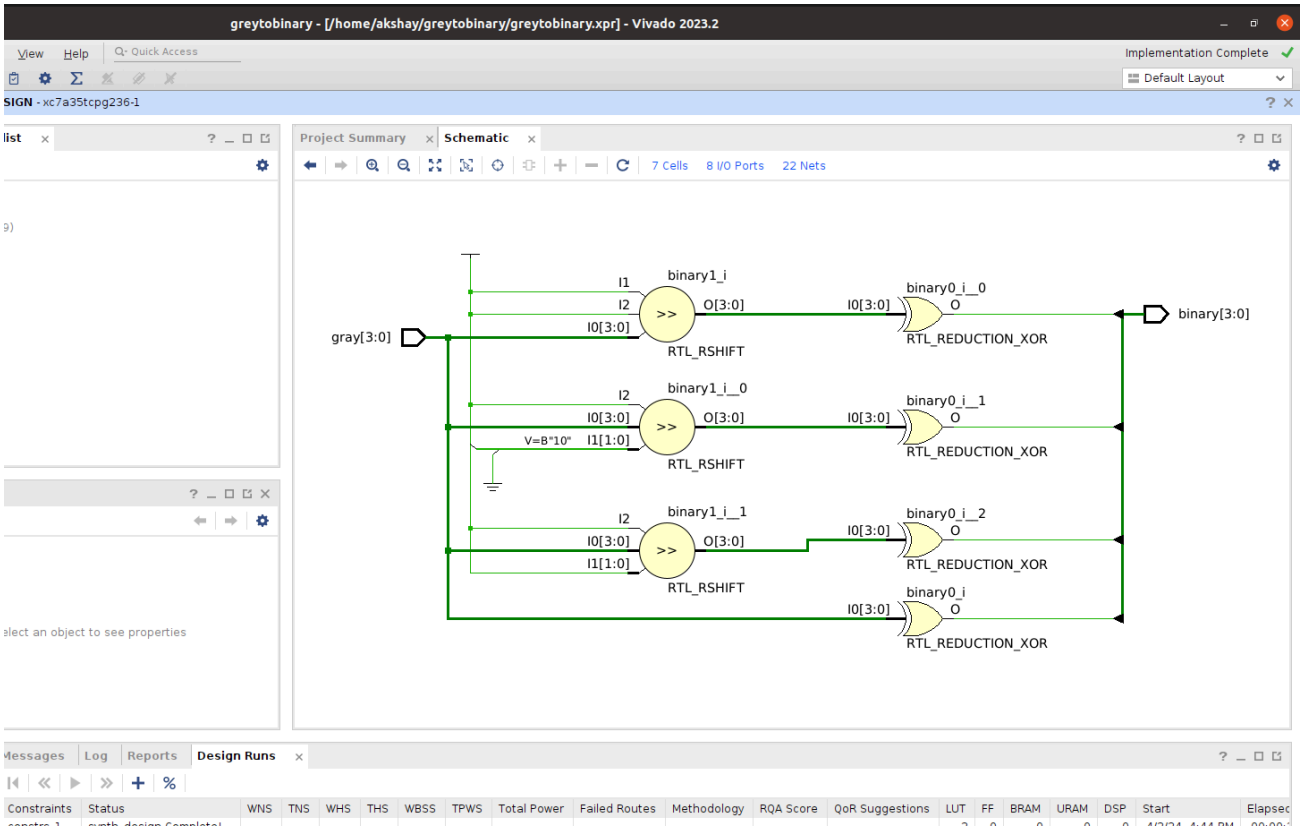

Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Settings
Summary (1.609 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (1.535 W)
Signals (0.028 W)
Data (0.028 W)
Logic (0.006 W)
I/O (1.5 W)
Summary
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 1.609 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 33.0°C
Thermal Margin: 52.0°C (10.3 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
95%
5%
97%
Dynamic: 1.535 W (95%)
Signals: 0.028 W (2%)
Logic: 0.006 W (1%)
I/O: 1.500 W (97%)
Device Static: 0.074 W (5%)

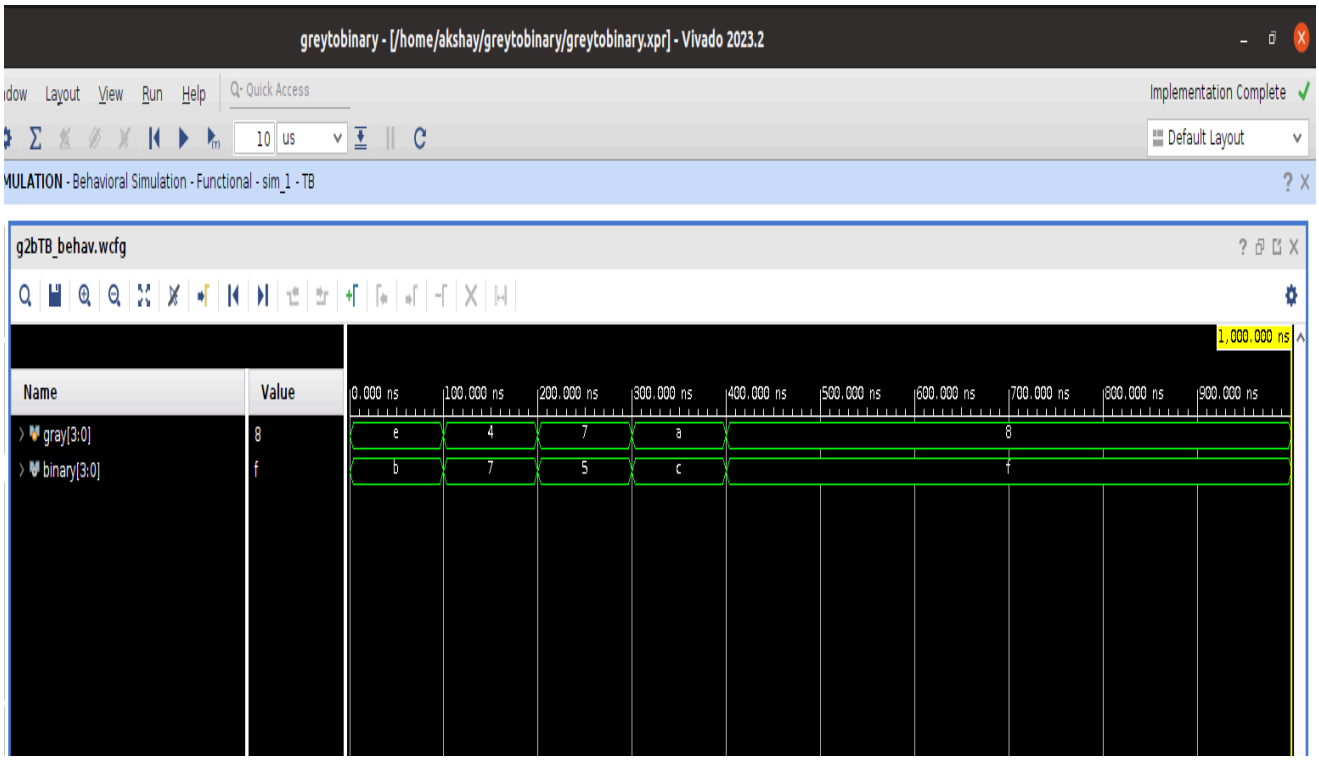
b. Grey to Binary Converter:

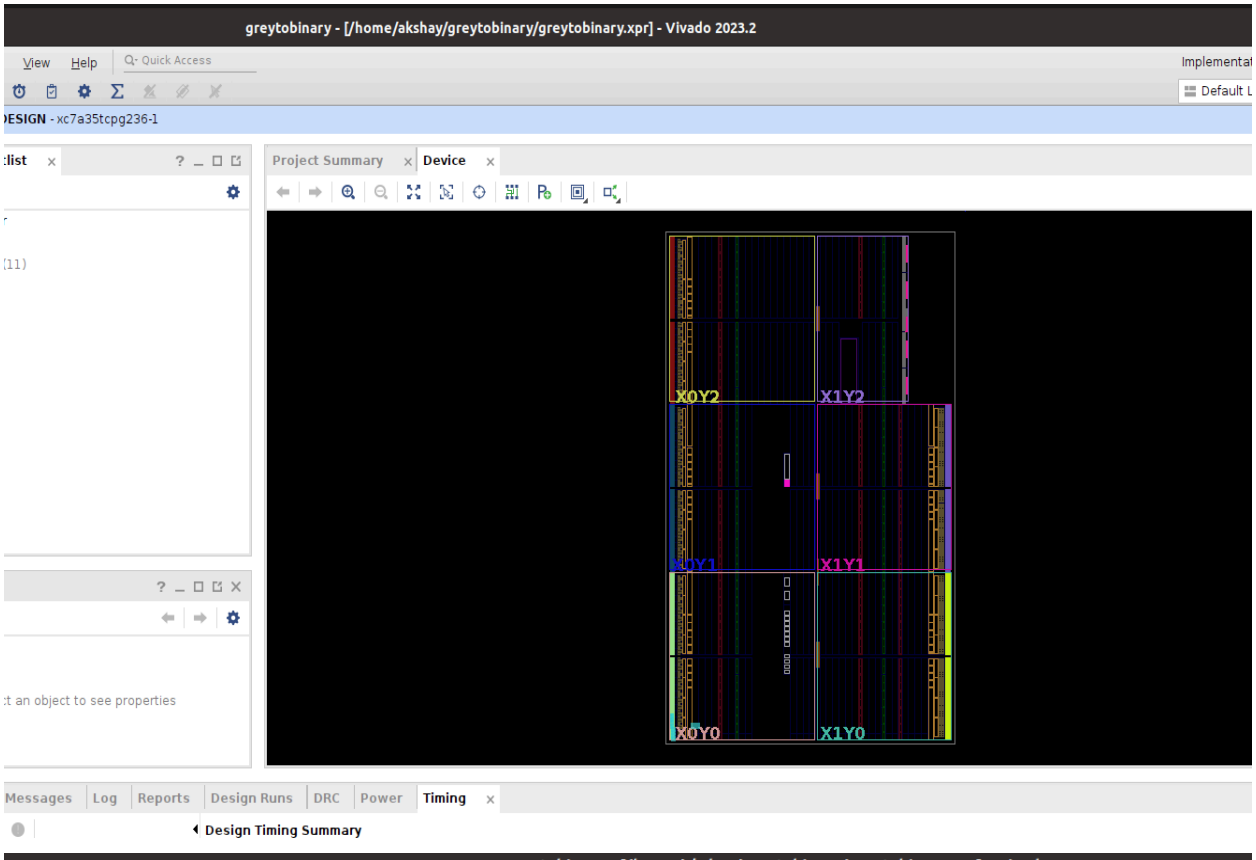
```
module g2b_converter #(parameter WIDTH=4) (input [WIDTH-1:0] gray, output [WIDTH-1:0] binary);

  genvar i;

  generate

    for(i=0;i<WIDTH;i=i+1) begin

      assign binary[i] = ^(gray >> i);

    end

  endgenerate

endmodule
```

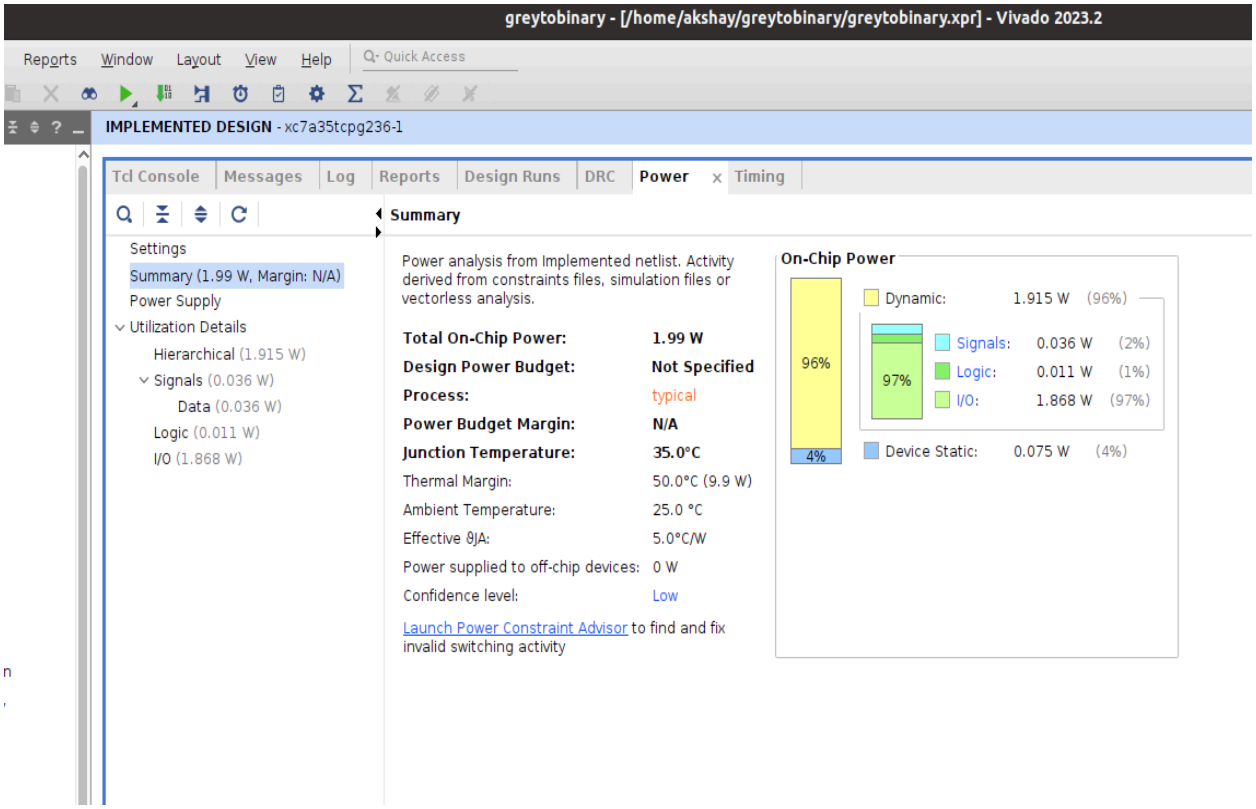
Testbench

```
module TB();

  reg [3:0] gray;    wire [3:0] binary;

  g2b_converter dut(gray, binary);

   initial

  begin

    $monitor("Gray = %b --> Binary = %b", gray, binary);

    gray = 4'b1110; #100;

    gray = 4'b0100; #100;

    gray = 4'b0111; #100;

    gray = 4'b1010; #100;

    gray = 4'b1000;

  end

endmodule
```


greytobinary - [/home/akshay/greytobinary/greytobinary.xpr] - Vivado 2023.2
Implementation Complete
Default Layout
Project Summary
Schematic
7 Cells
8 I/O Ports
22 Nets
gray[3:0]
binary1_i
binary1_i__0
binary1_i__1
RTL_RSHIFT
binary0_i__0
binary0_i__1
binary0_i__2
binary0_i
RTL_REDUCTION_XOR
binary[3:0]
Messages
Log
Reports
Design Runs
Constraints
Status
WNS
TNS
WHS
THS
WBSS
TPWS
Total Power
Failed Routes
Methodology
RQA Score
QoR Suggestions
LUT
FF
BRAM
URAM
DSP
Start
Elapsec


greytobinary - [/home/akshay/greytobinary/greytobinary.xpr] - Vivado 2023.2
Implementation Complete
Default Layout
MULATION - Behavioral Simulation - Functional - sim_1 - TB
g2bTB_behav.wcfg
1,000.000 ns
Name
Value
gray[3:0]
binary[3:0]
0.000 ns
100.000 ns
200.000 ns
300.000 ns
400.000 ns
500.000 ns
600.000 ns
700.000 ns
800.000 ns
900.000 ns


greytobinary - [/home/akshay/greytobinary/greytobinary.xpr] - Vivado 2023.2
View
Help
Quick Access
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Design Timing Summary


greytobinary - [/home/akshay/greytobinary/greytobinary.xpr] - Vivado 2023.2
Reports
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Summary
Settings
Summary (1.99 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (1.915 W)
Signals (0.036 W)
Data (0.036 W)
Logic (0.011 W)
I/O (1.868 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 1.99 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 35.0°C
Thermal Margin: 50.0°C (9.9 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
96%
4%
97%
Dynamic: 1.915 W (96%)
Signals: 0.036 W (2%)
Logic: 0.011 W (1%)
I/O: 1.868 W (97%)
Device Static: 0.075 W (4%)

c. BCD to Excess -3:

```
module BCD2Ex3(A,B,C,D,W,X,Y,Z);

input A,B,C,D;

output W,X,Y,Z;

assign W = A|(B&C)|(B&D);

assign X = (~B&C) | (~B&D) | (B&~C&~D);

assign Y = ~(C^D);

assign Z = ~D;

endmodule
```

Testbench

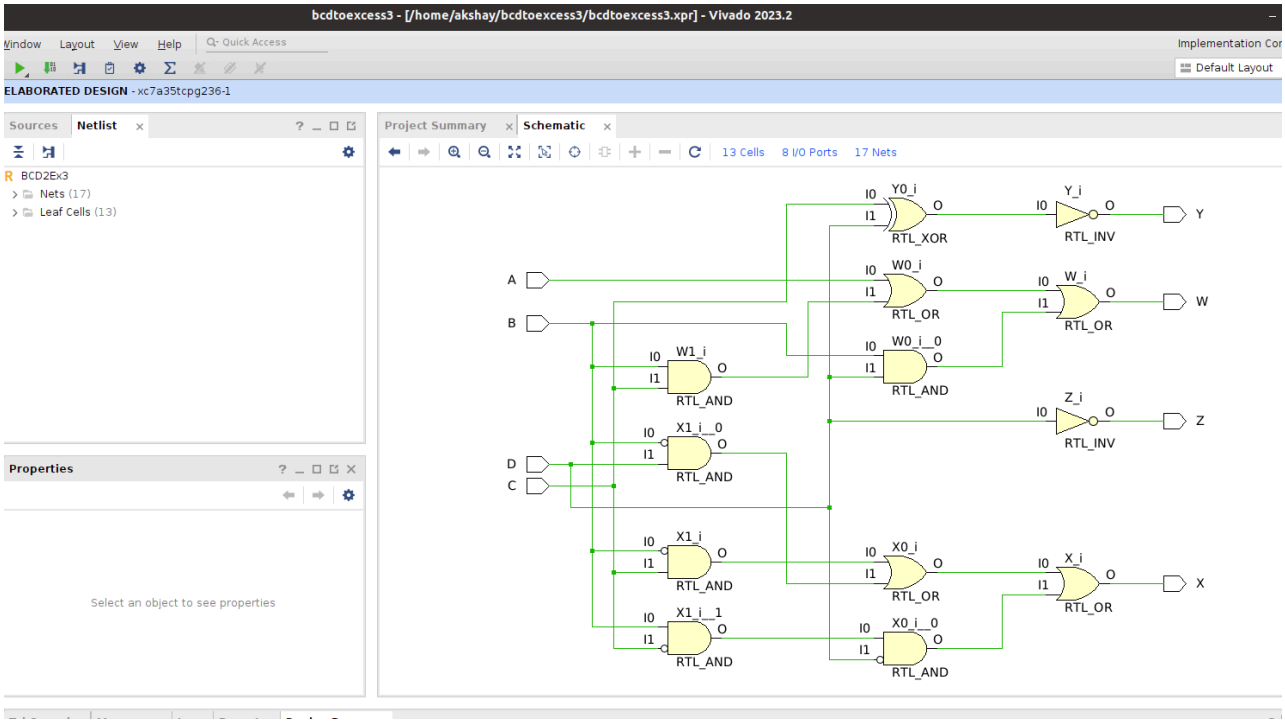
```
module test();

wire W,X,Y,Z;

reg A,B,C,D;

BCD2Ex3 dut(A,B,C,D,W,X,Y,Z);

initial

begin

A = 0; B = 0; C = 0; D = 0; #100;

A = 0; B = 0; C = 0; D = 1; #100;

A = 0; B = 0; C = 1; D = 0; #100;

A = 0; B = 0; C = 1; D = 1; #100;

A = 0; B = 1; C = 0; D = 0; #100;

A = 0; B = 1; C = 0; D = 1; #100;

A = 0; B = 1; C = 1; D = 0; #100;

A = 0; B = 1; C = 1; D = 1; #100;

A = 1; B = 0; C = 0; D = 0; #100;
```

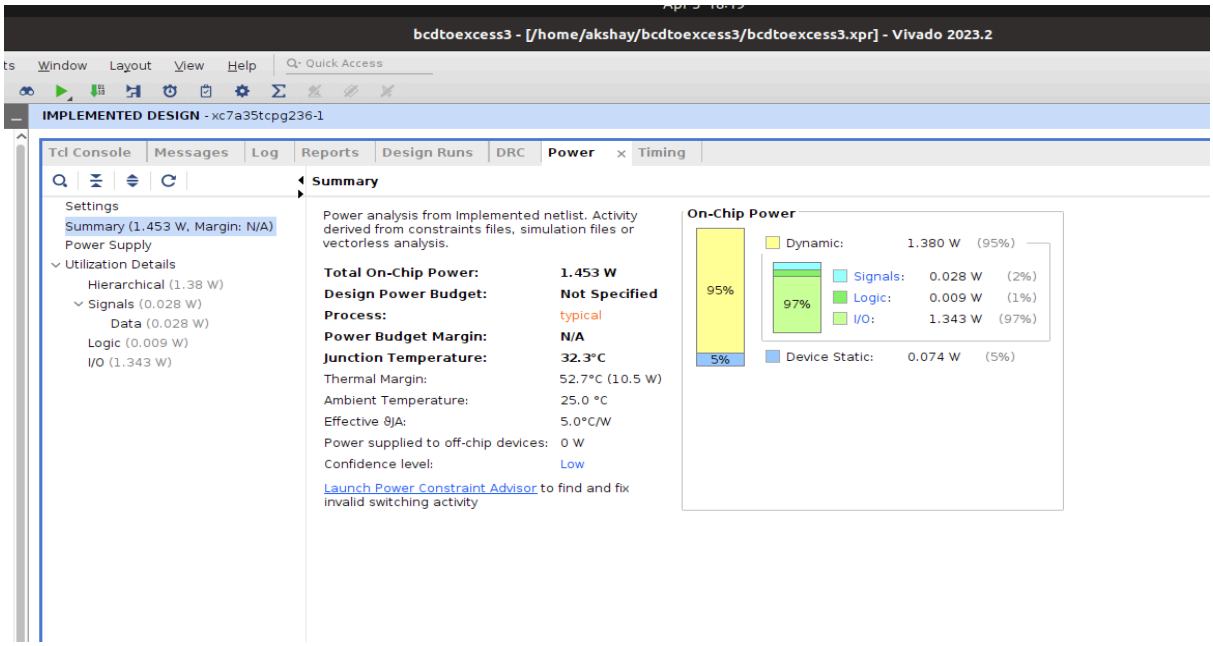
A = 1; B = 0; C = 0; D = 1; #100;

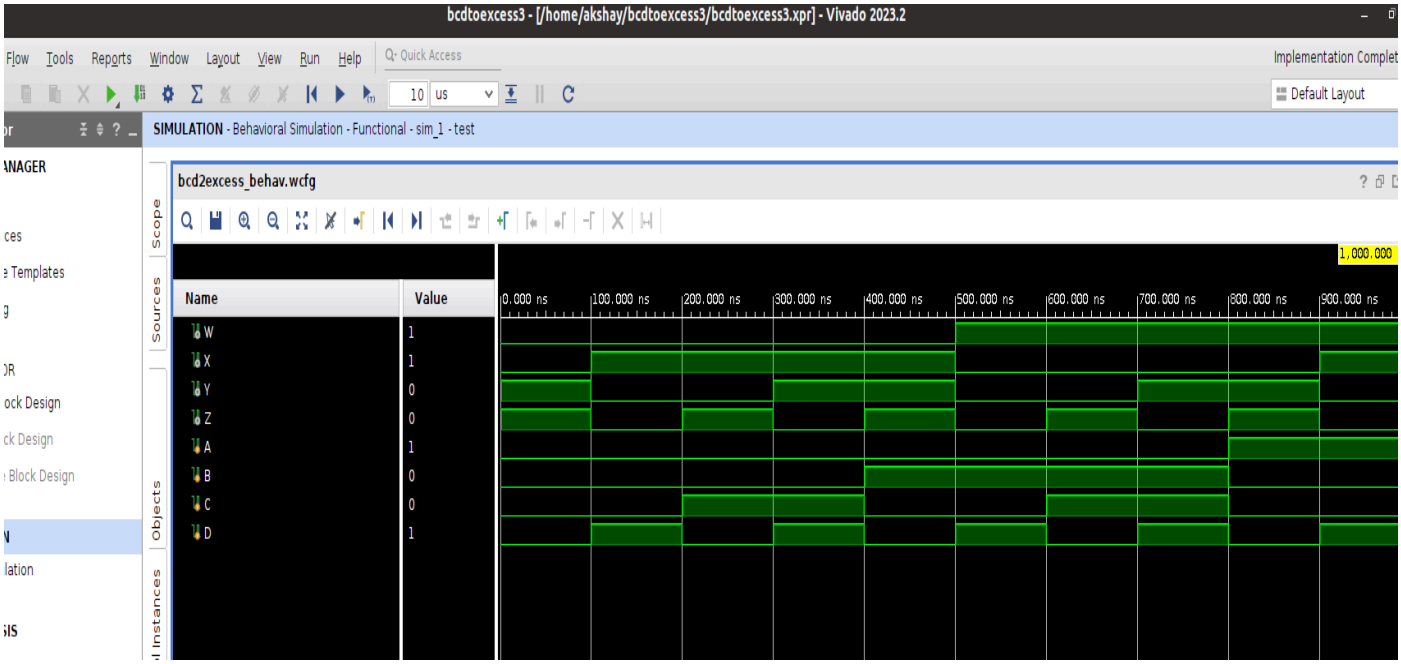
end

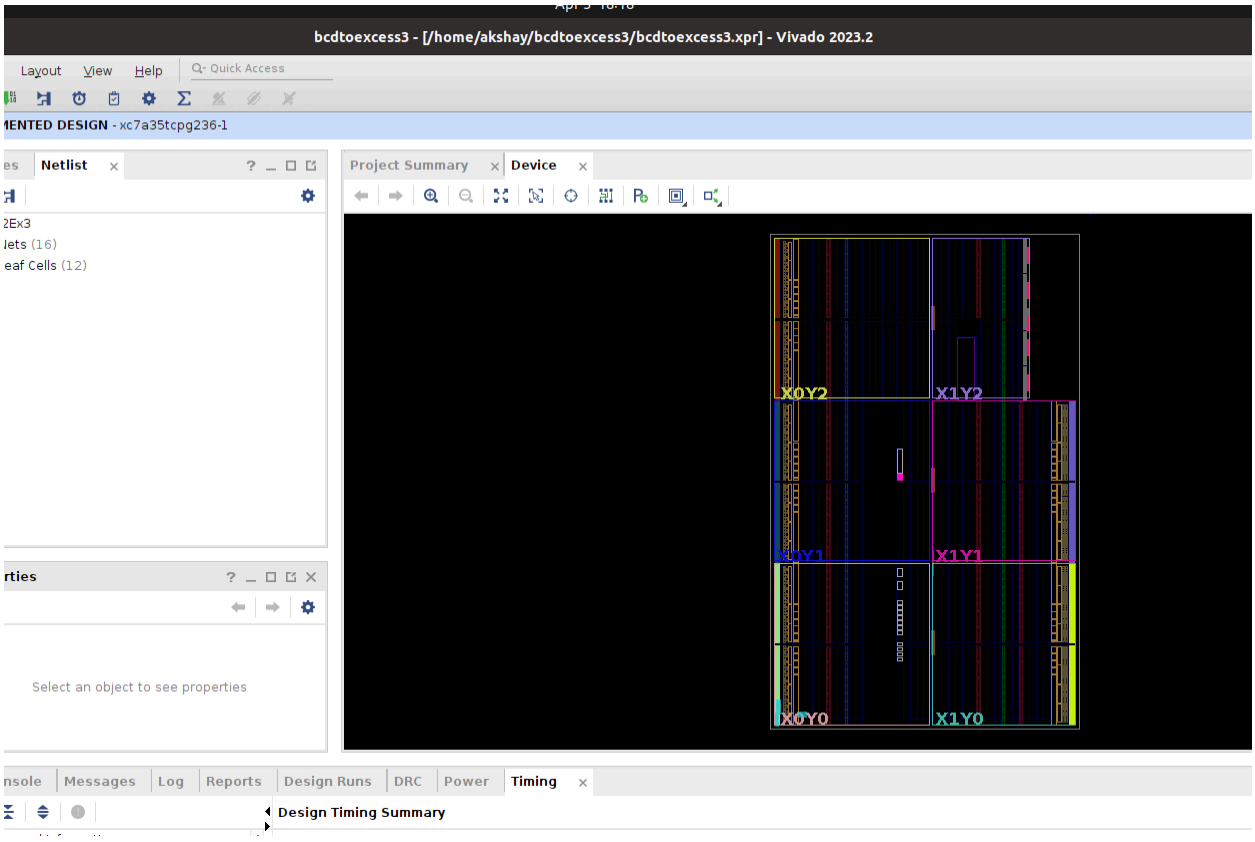
initial $monitor("A=%b, B=%b, C=%b, D=%b, W=%b, X=%b, Y=%b, Z=%b", A, B, C, D, W, X, Y, Z);

Endmodule






bcdtoexcess3 - [/home/akshay/bcdtoexcess3/bcdtoexcess3.xpr] - Vivado 2023.2
Flow Tools Reports Window Layout View Run Help
Quick Access
Implementation Complet
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - test
bcd2excess_behav.wcfg
Scope
Sources
Objects
Name
Value
W 1
X 1
Y 0
Z 0
A 1
B 0
C 0
D 1
0.000 ns
100.000 ns
200.000 ns
300.000 ns
400.000 ns
500.000 ns
600.000 ns
700.000 ns
800.000 ns
900.000 ns
1,000.000


bcdtoexcess3 - [/home/akshay/bcdtoexcess3/bcdtoexcess3.xpr] - Vivado 2023.2
Layout View Help
Quick Access
MENTED DESIGN - xc7a35tcpg236-1
Netlist
2Ex3
lets (16)
eaf Cells (12)
rties
Select an object to see properties
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
nsole
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Design Timing Summary

Assignment-5

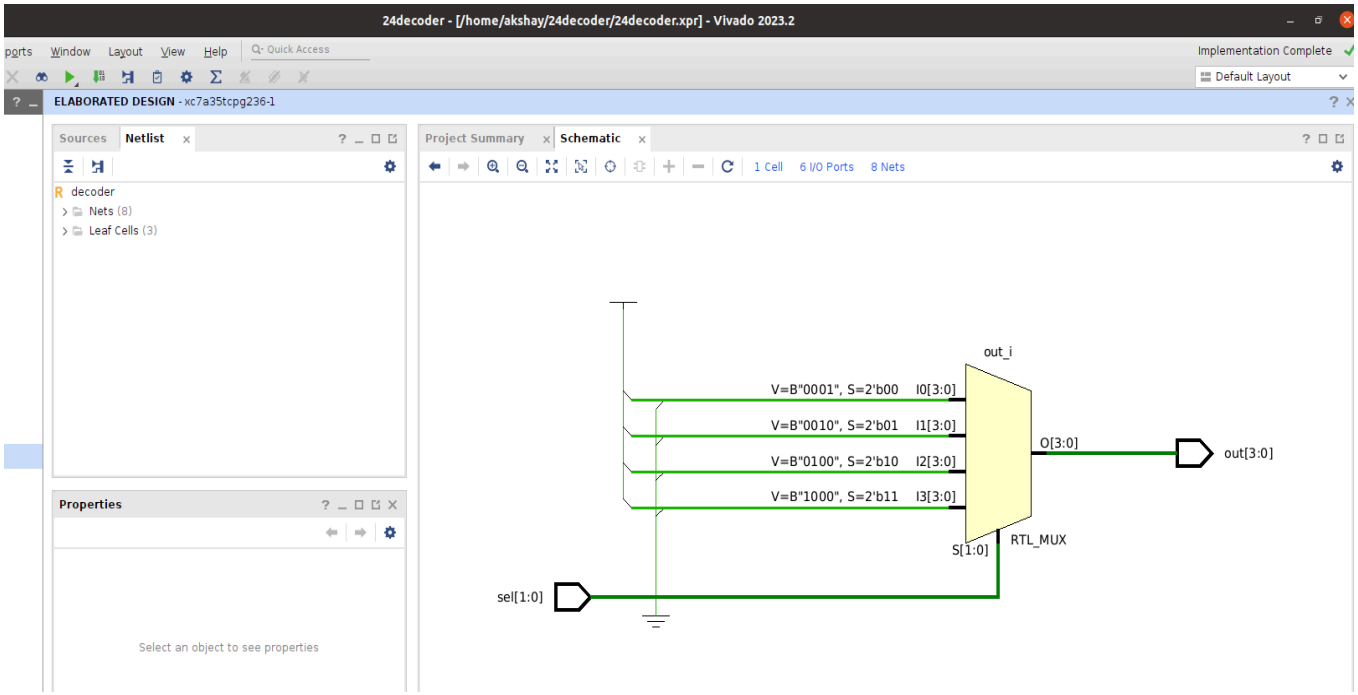
Q.17. Write Verilog code for 2:4 decoder.

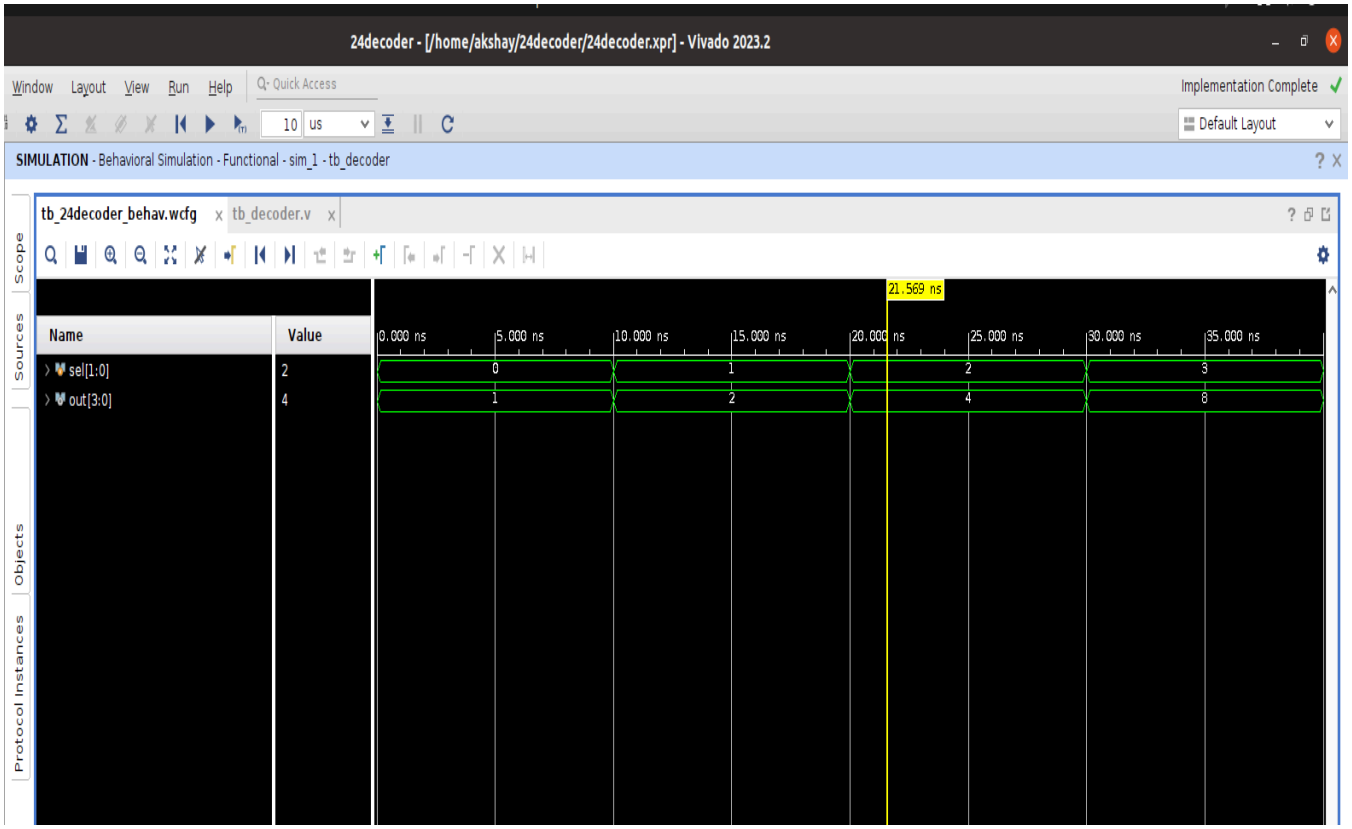
```
module decoder(
    input [1:0] sel,
    output reg [3:0] out     );
  always @(*)
    case(sel)
        2'b00: out = 4'b0001;
        2'b01: out = 4'b0010;
        2'b10: out = 4'b0100;
        2'b11: out = 4'b1000;
        default: out = 4'bxxxx; // Handle undefined input
    Endcase
endmodule
```

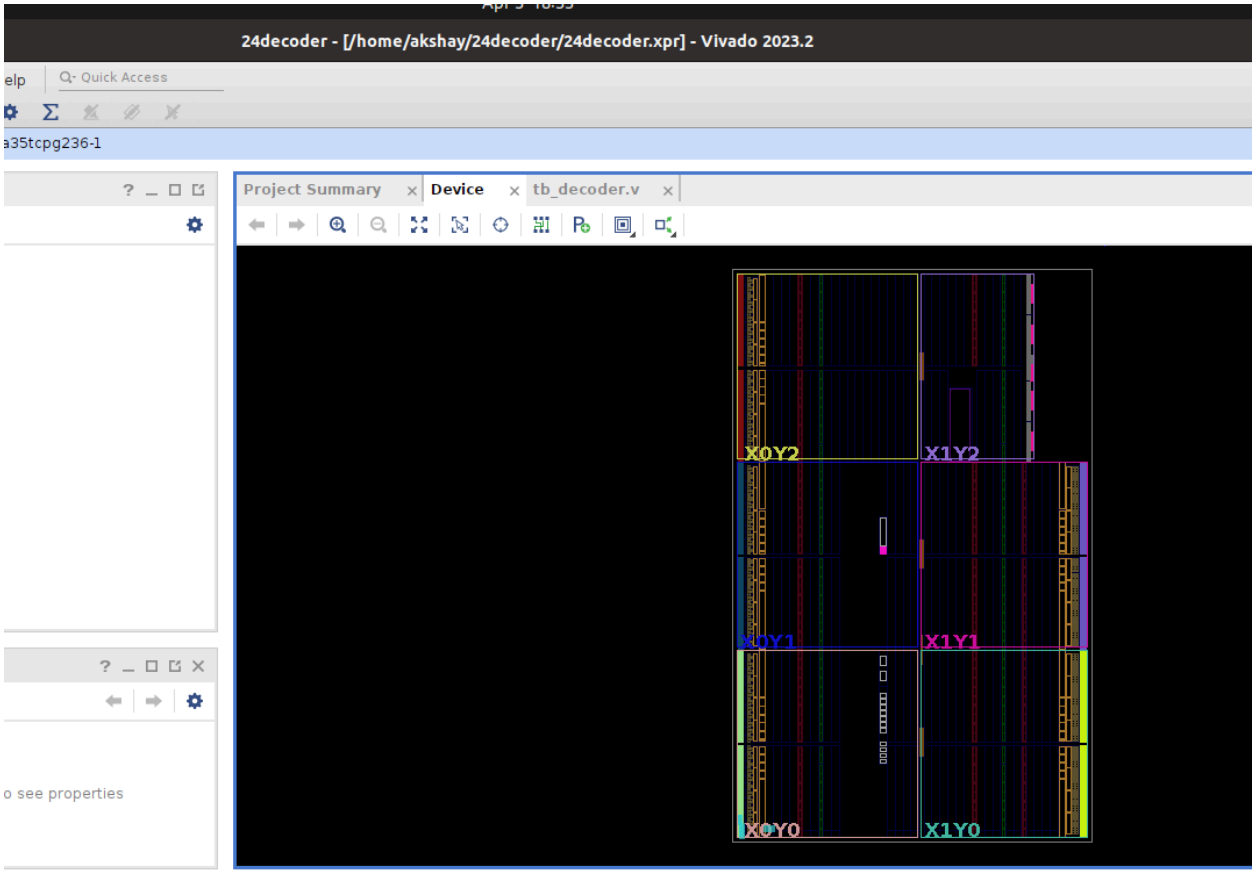
Testbench

```
module tb_decoder();


    reg [1:0] sel;
    wire [3:0] out;


    decoder dut (
        sel,
        out
    );
```

```
    initial begin
        // Test case 1: sel = 00
        sel = 2'b00;
        #10; // Wait for 10 time units
        $display("sel = %b, out = %b", sel, out);

        // Test case 2: sel = 01
        sel = 2'b01;
        #10; // Wait for 10 time units
        $display("sel = %b, out = %b", sel, out);

        // Test case 3: sel = 10
        sel = 2'b10;
        #10; // Wait for 10 time units
        $display("sel = %b, out = %b", sel, out);

        // Test case 4: sel = 11
        sel = 2'b11;
        #10; // Wait for 10 time units
        $display("sel = %b, out = %b", sel, out);
   // Add more test cases as needed
$finish; // Finish simulation
    End
endmodule
```


24decoder - [/home/akshay/24decoder/24decoder.xpr] - Vivado 2023.2
Implementation Complete
Default Layout
ELABORATED DESIGN - xc7a35tcpg236-1
Sources
Netlist
decoder
Nets (8)
Leaf Cells (3)
Properties
Select an object to see properties
Project Summary
Schematic
1 Cell
6 I/O Ports
8 Nets
out_i
V=B"0001", S=2'b00
I0[3:0]
V=B"0010", S=2'b01
I1[3:0]
V=B"0100", S=2'b10
I2[3:0]
V=B"1000", S=2'b11
I3[3:0]
O[3:0]
out[3:0]
S[1:0]
RTL_MUX
sel[1:0]

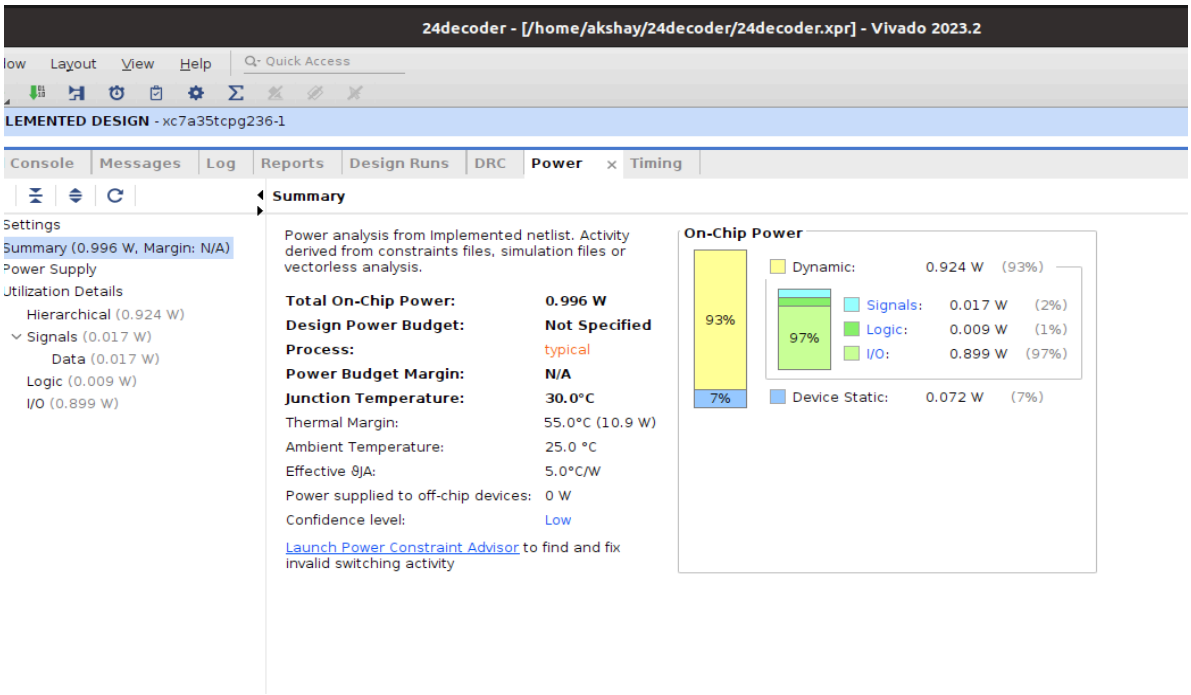

24decoder - [/home/akshay/24decoder/24decoder.xpr] - Vivado 2023.2
Implementation Complete
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_decoder
tb_24decoder_behav.wcfg
tb_decoder.v
Scope
Sources
Objects
Protocol Instances
21.569 ns
Name
Value
sel[1:0]
2
out[3:0]
4
0.000 ns
5.000 ns
10.000 ns
15.000 ns
20.000 ns
25.000 ns
30.000 ns
35.000 ns
0
1
2
3
1
2
4
8



Log | Reports | Design Runs | DRC | Power | Timing

Design Timing Summary

Setup	Hold	Pulse Width



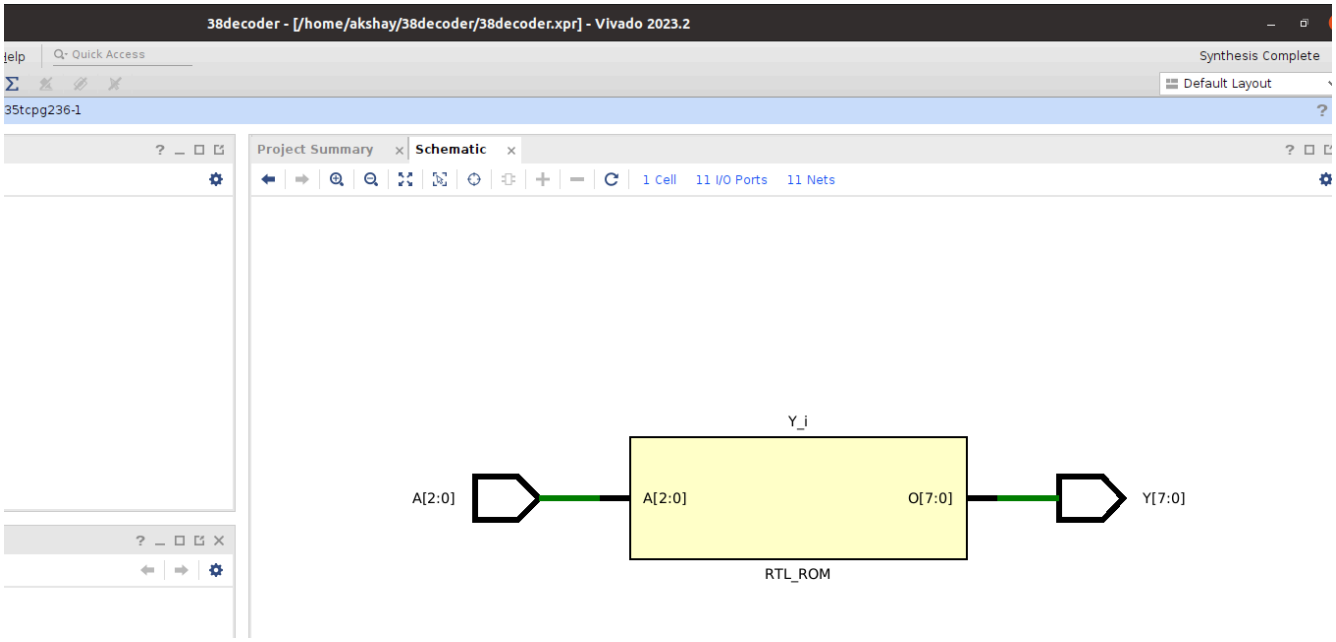
Q.18. Write Verilog code for 3:8 decoder.

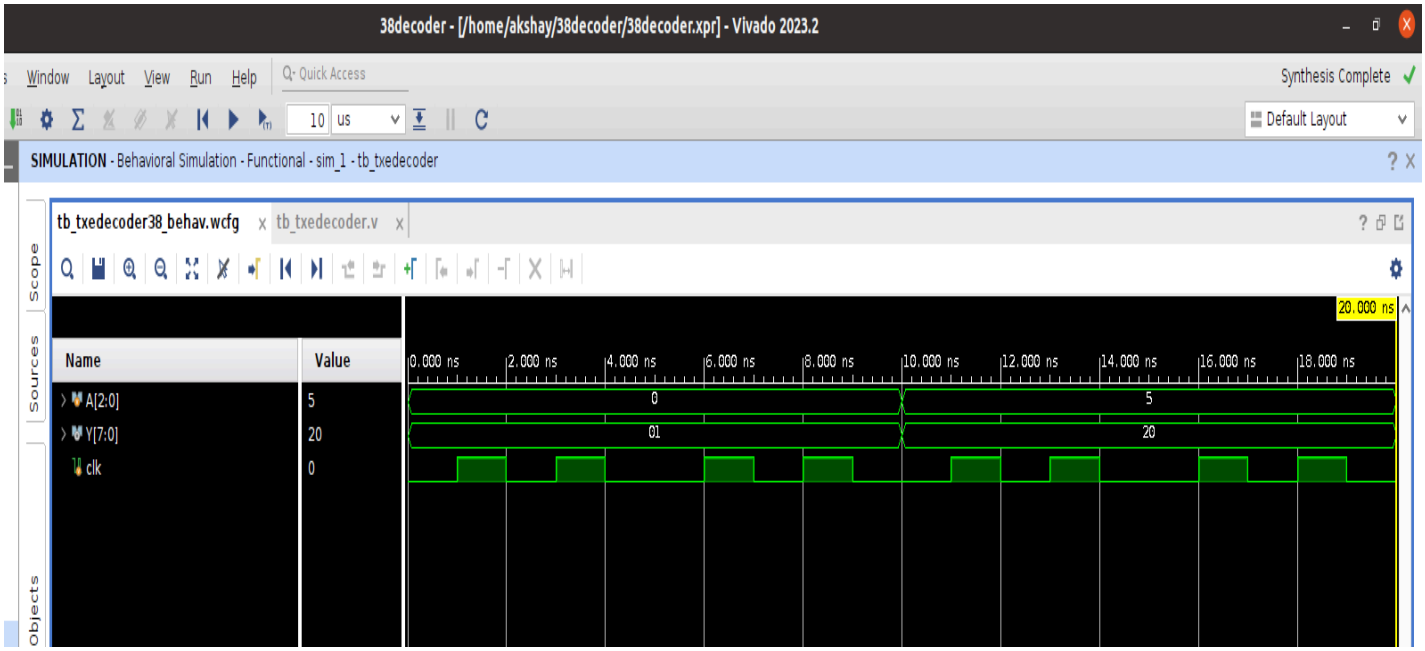
```
module txedecoder(input [2:0] A, output reg [7:0] Y);
always @*
begin
    case (A)
        3'b000: Y = 8'b00000001;
        3'b001: Y = 8'b00000010;
        3'b010: Y = 8'b00000100;
        3'b011: Y = 8'b00001000;
        3'b100: Y = 8'b00010000;
        3'b101: Y = 8'b00100000;
        3'b110: Y = 8'b01000000;
        3'b111: Y = 8'b10000000;
        default: Y = 8'b00000000; // Default case for invalid inputs
    endcase
End
endmodule
```

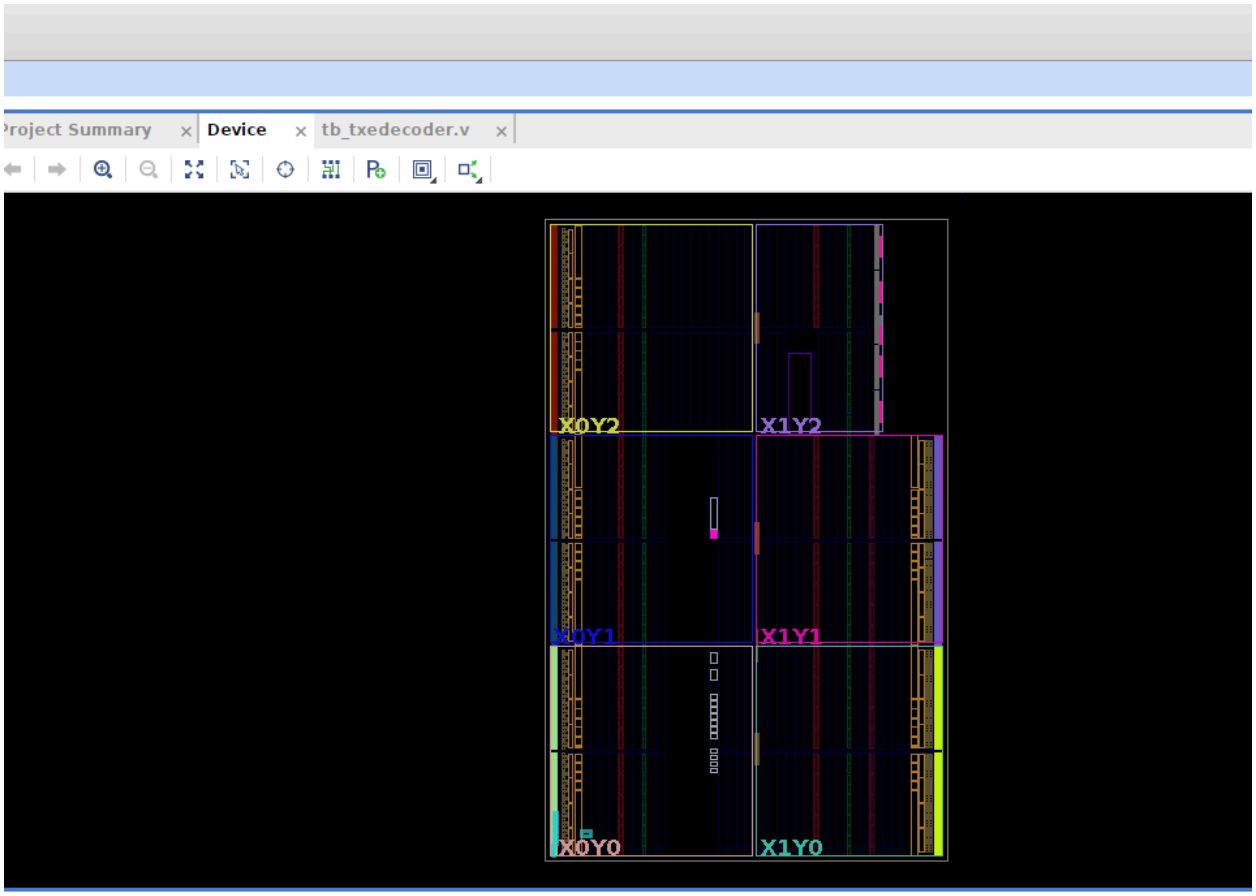
Testbench

```
module tb_txedecoder;
// Inputs
    reg [2:0] A;
       // Outputs
    wire [7:0] Y;
       // Instantiate the module under test
    txedecoder dut (
```

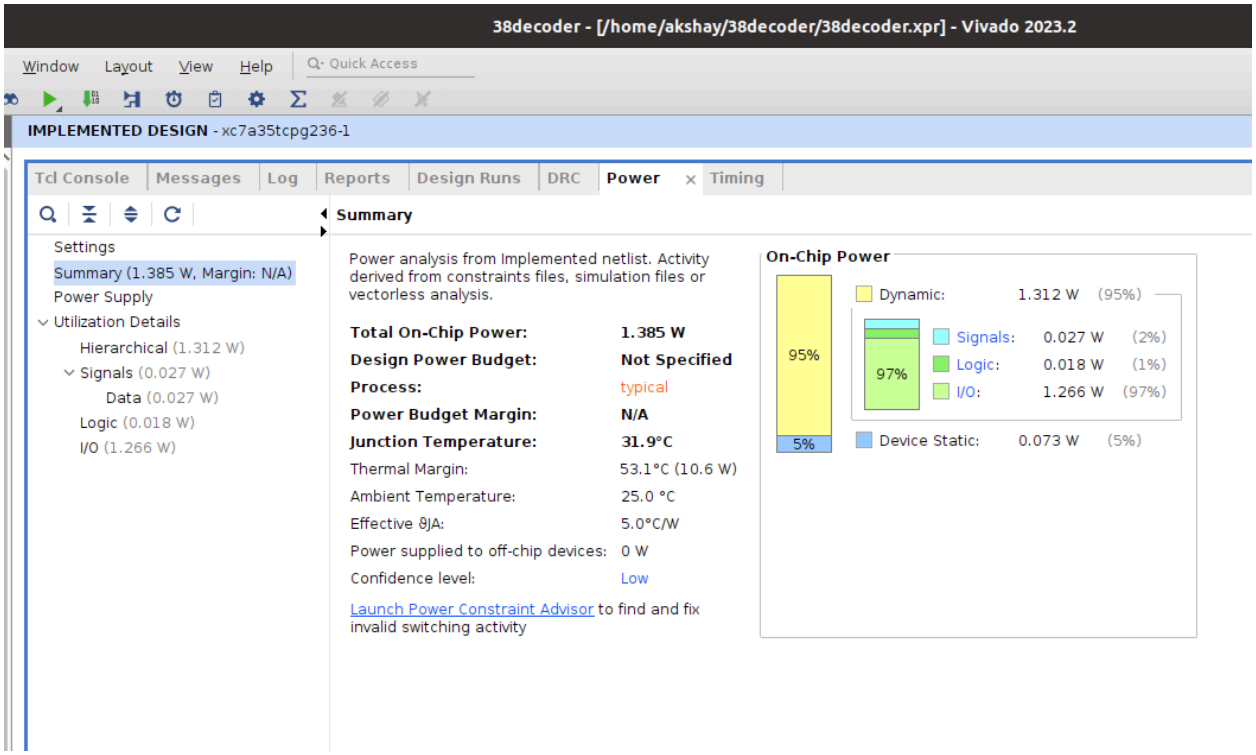
```
        .A(A),
        .Y(Y)
    );

    // Clock generation
    reg clk = 0;
    always #5 clk = ~clk; // Toggle clock every 5 time units

  // Test stimulus
    initial begin
        $monitor("Time=%t, A=%b, Y=%b", $time, A, Y);
         // Test case 1
        A = 3'b000;
        #10; // Wait for 10 time units

     // Test case 2
        A = 3'b101;
        #10; // Wait for 10 time units
           // Add more test cases as needed
        $stop; // Stop simulation
    end
       // Clock driver
    always #1 clk = ~clk; // Generate a clock with period 1 time unit
endmodule
```


38decoder - [/home/akshay/38decoder/38decoder.xpr] - Vivado 2023.2
Quick Access
Synthesis Complete
Default Layout
35tcpg236-1
Project Summary
Schematic
1 Cell
11 I/O Ports
11 Nets
Y_i
A[2:0]
A[2:0]
O[7:0]
Y[7:0]
RTL_ROM


38decoder - [/home/akshay/38decoder/38decoder.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Synthesis Complete
10
us
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_txedecoder
tb_txedecoder38_behav.wcfg
tb_txedecoder.v
Scope
Sources
Objects
20.000 ns
Name
Value
A[2:0]
5
Y[7:0]
20
clk
0
0.000 ns
2.000 ns
4.000 ns
6.000 ns
8.000 ns
10.000 ns
12.000 ns
14.000 ns
16.000 ns
18.000 ns
0
5
01
20



ns | DRC | Power | Timing



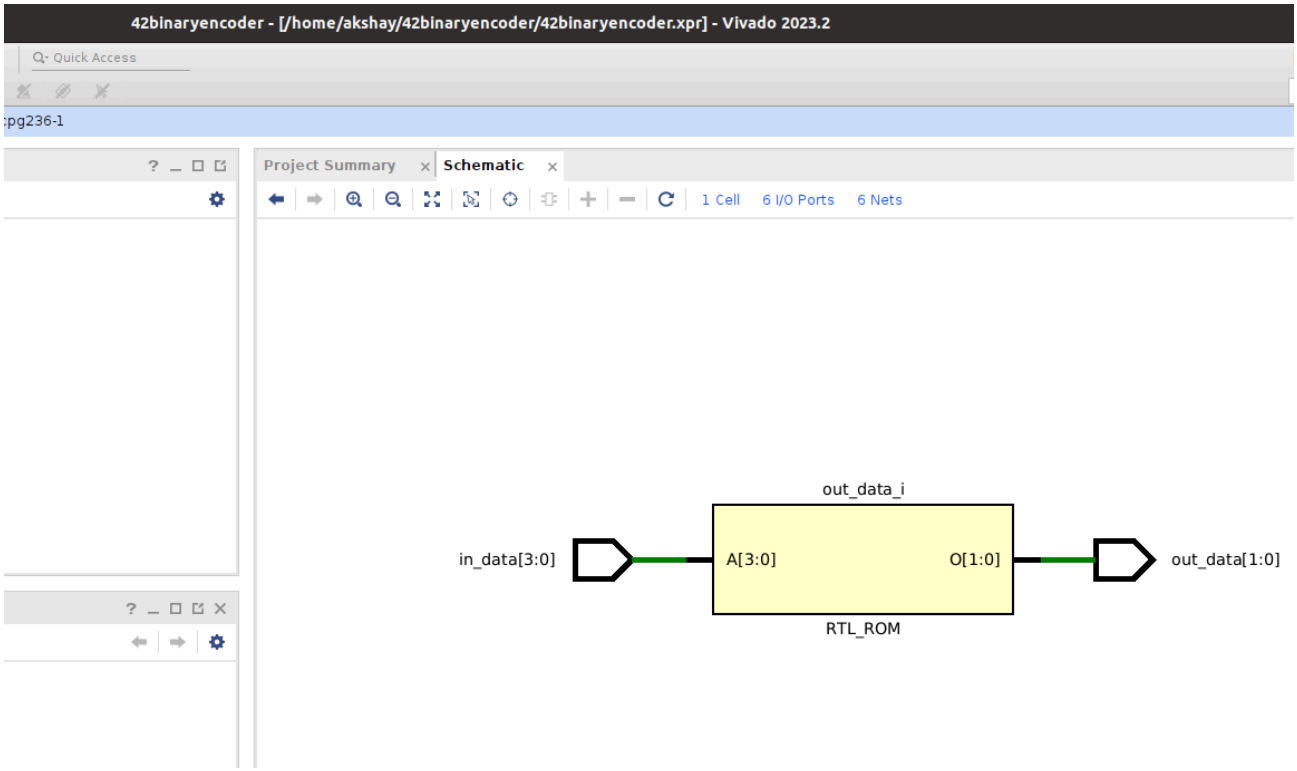
Q.19 Write Verilog code for 4:2 Binary Encoder.

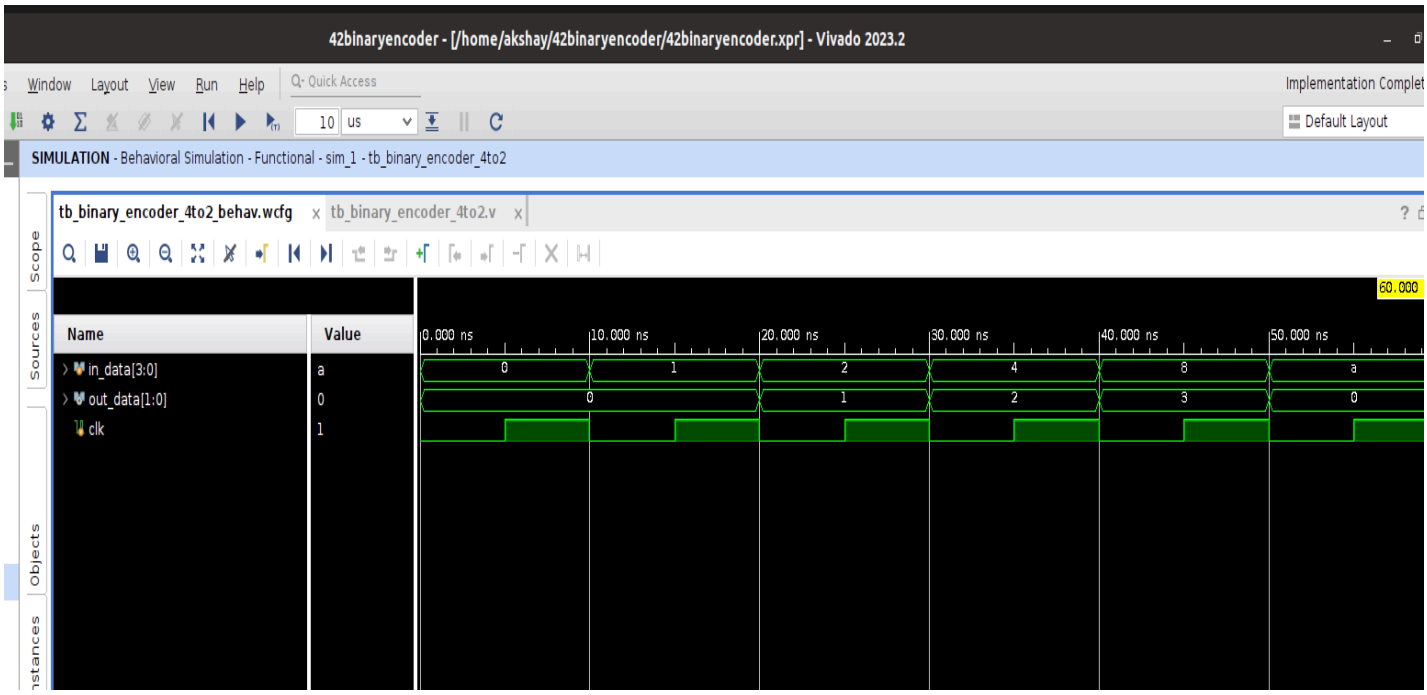
```
module binary_encoder_4to2 (
    input [3:0] in_data,
    output reg [1:0] out_data
);
always @* begin
    case (in_data)
        4'b0001: out_data = 2'b00;
        4'b0010: out_data = 2'b01;
        4'b0100: out_data = 2'b10;
        4'b1000: out_data = 2'b11;
        default: out_data = 2'b00; // Handle default case
    endcase
end
endmodule
```

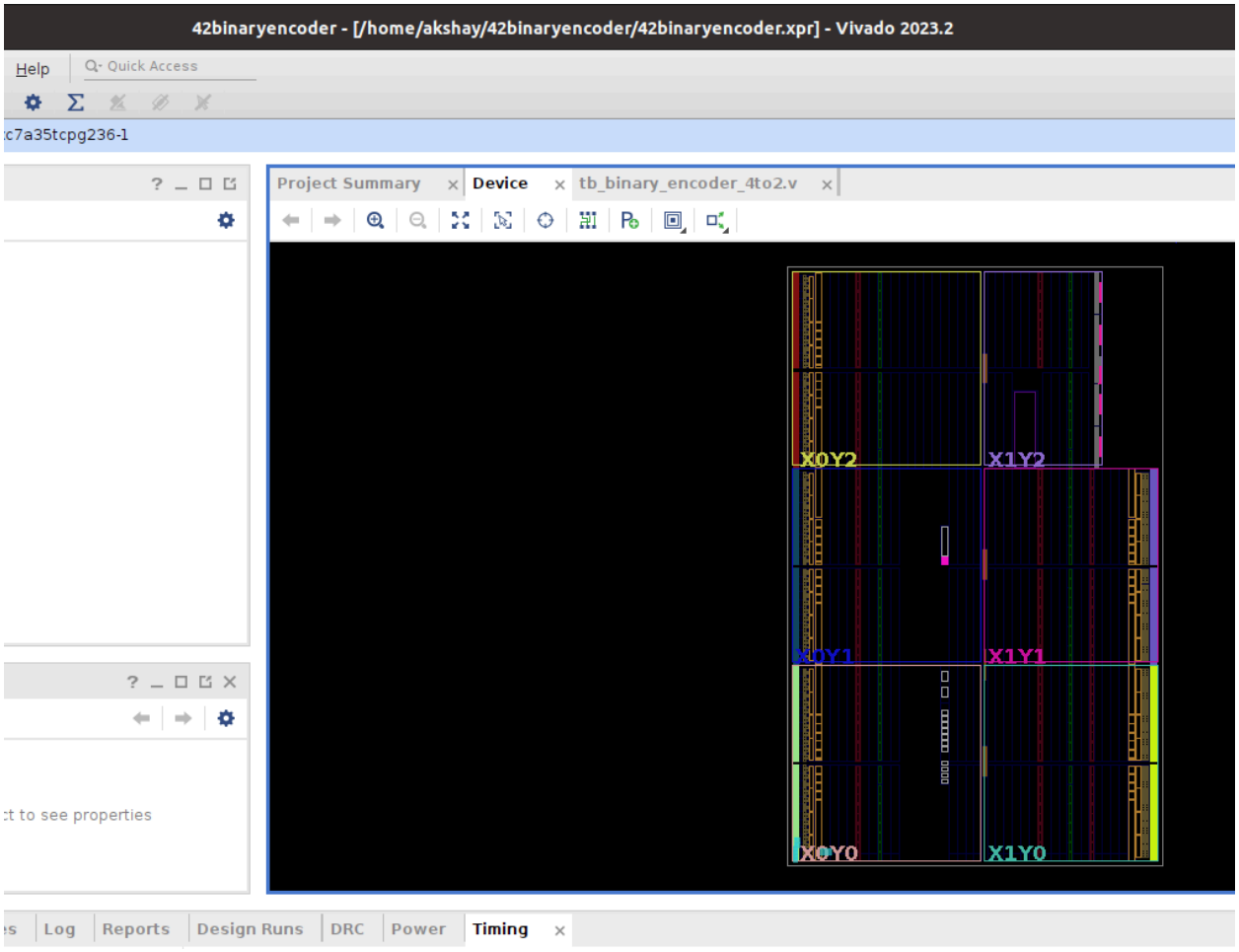
Testbench

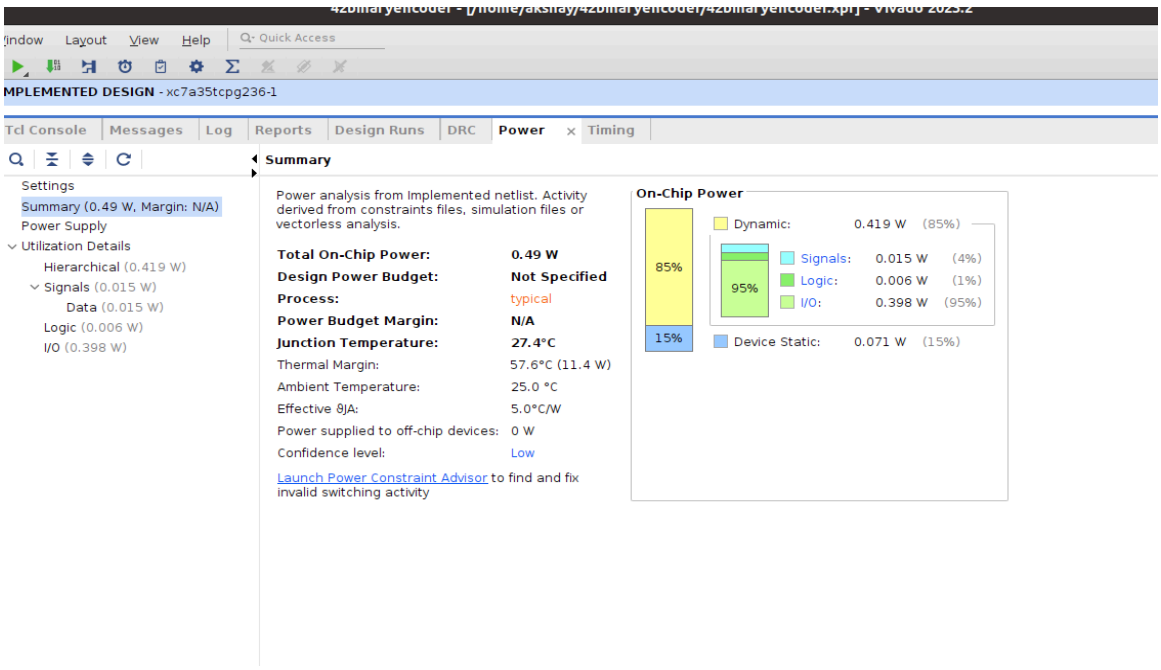
```
module tb_binary_encoder_4to2;
// Inputs
reg [3:0] in_data;
// Outputs
wire [1:0] out_data;
// Instantiate the binary encoder module
binary_encoder_4to2 dut (
    in_data,
    Out_data );
```

```
// Clock generation
reg clk = 0;
always #5 clk = ~clk;

// Stimulus generation
initial begin
    // Initialize inputs
    in_data = 4'b0000;

    // Apply stimulus
    #10 in_data = 4'b0001;
    #10 in_data = 4'b0010;
    #10 in_data = 4'b0100;
    #10 in_data = 4'b1000;
    #10 in_data = 4'b1010; // Test default case
   // End simulation
    #10 $finish;
end

// Display output
always @(posedge clk) begin
    $display("Input: %b, Output: %b", in_data, out_data);
end
endmodule
```


42binaryencoder - [/home/akshay/42binaryencoder/42binaryencoder.xpr] - Vivado 2023.2
Quick Access
pg236-1
Project Summary
Schematic
1 Cell
6 I/O Ports
6 Nets
out_data_i
in_data[3:0]
A[3:0]
O[1:0]
out_data[1:0]
RTL_ROM


42binaryencoder - [/home/akshay/42binaryencoder/42binaryencoder.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Implementation Complet
10
us
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_binary_encoder_4to2
tb_binary_encoder_4to2_behav.wcfg
tb_binary_encoder_4to2.v
Scope
Sources
Objects
Name
Value
in_data[3:0]
a
out_data[1:0]
0
clk
1
60.000
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
0
1
2
4
8
a
0
1
2
3
0


42binaryencoder - [/home/akshay/42binaryencoder/42binaryencoder.xpr] - Vivado 2023.2
Help
Quick Access
c7a35tcpg236-1
Project Summary
Device
tb_binary_encoder_4to2.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
t to see properties
Log
Reports
Design Runs
DRC
Power
Timing


Window
Layout
View
Help
Quick Access
MPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Settings
Summary (0.49 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.419 W)
Signals (0.015 W)
Data (0.015 W)
Logic (0.006 W)
I/O (0.398 W)
Summary
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.49 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 27.4°C
Thermal Margin: 57.6°C (11.4 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
85%
15%
95%
Dynamic: 0.419 W (85%)
Signals: 0.015 W (4%)
Logic: 0.006 W (1%)
I/O: 0.398 W (95%)
Device Static: 0.071 W (15%)

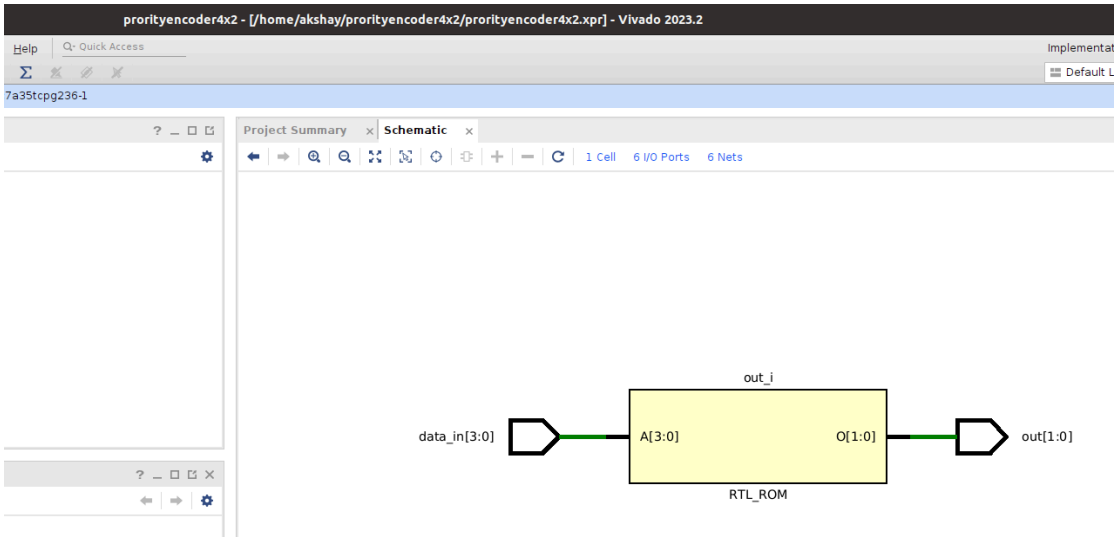
Q.20. Write Verilog code for 4:2 Priority Encoder.

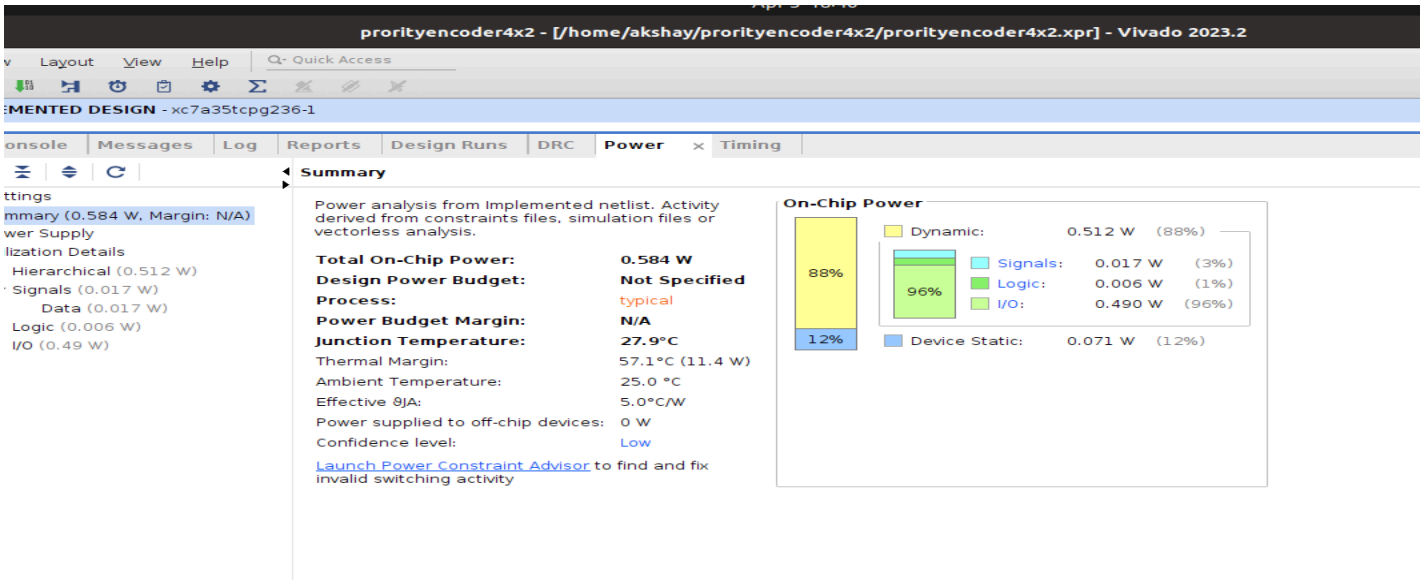
```
module priority_encoder_4x2 (
    input [3:0] data_in,   // Input data lines
    output reg [1:0] out    // Output lines );
always @(*) begin
    case(data_in)
        4'b0000: out = 2'b00;
        4'b0001: out = 2'b01;
        4'b0011: out = 2'b10; // Corrected output assignment
        4'b0110: out = 2'b10;
        4'b1111: out = 2'b11; // Corrected output assignment
        default: out = 2'b00; // Default case
    endcase
end
endmodule
```

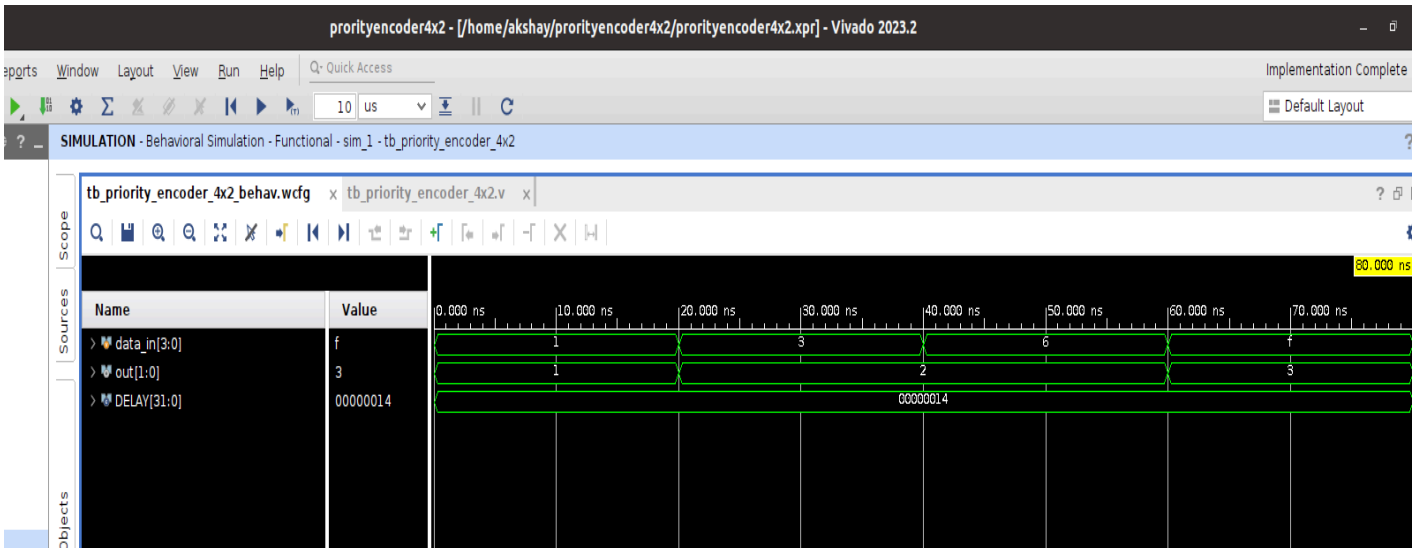
Testbench

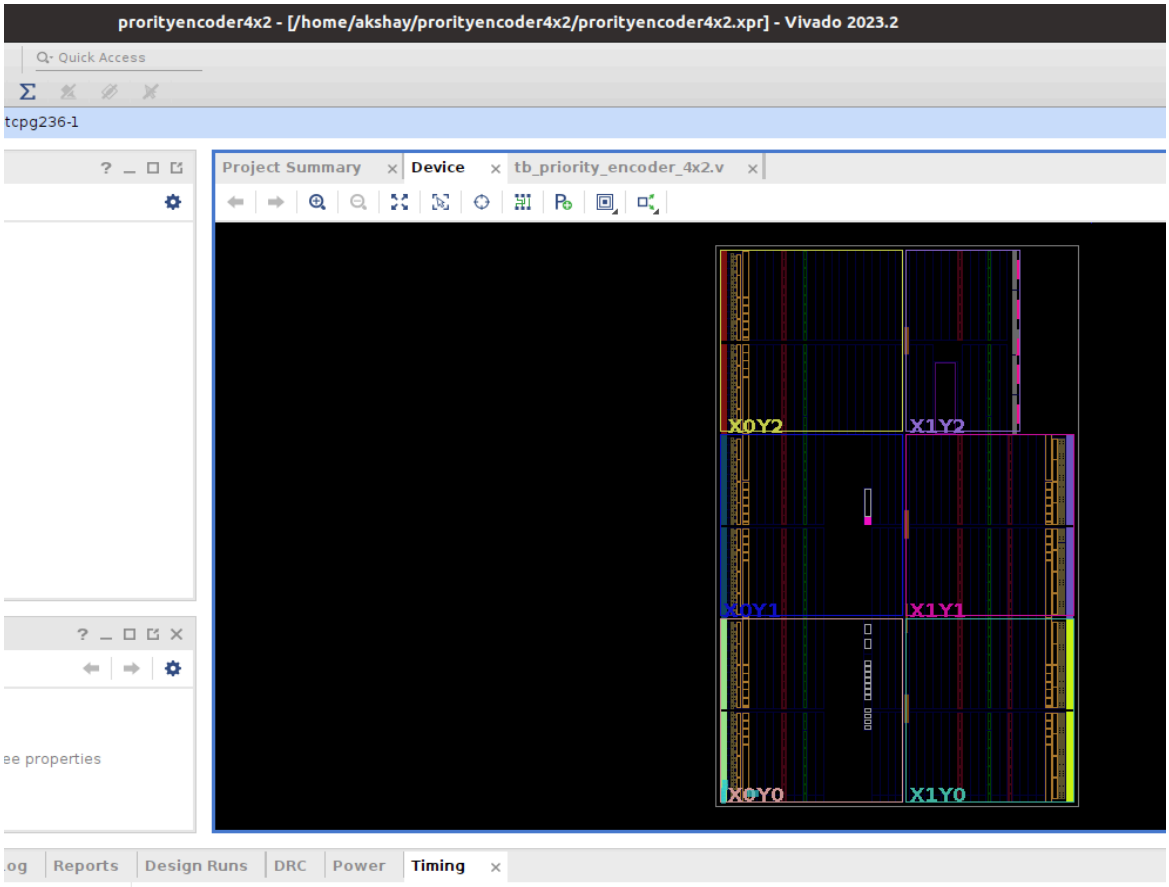
```
module tb_priority_encoder_4x2;
  parameter DELAY = 20;
 reg [3:0] data_in;   wire [1:0] out;
  priority_encoder_4x2 dut (
    .data_in(data_in),
    .out(out)  );
  initial begin
    data_in = 4'b0001;  #DELAY;
    data_in = 4'b0011;   #DELAY;
```

```
  data_in = 4'b0110;   #DELAY;
  data_in = 4'b1111;    #DELAY;
  $finish;
end
always @(*) begin
  $display("data_in = %b, out = %b", data_in, out);
end
Endmodule
```






prorityencoder4x2 - [/home/akshay/prorityencoder4x2/prorityencoder4x2.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Implementation Complete
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_priority_encoder_4x2
tb_priority_encoder_4x2_behav.wcfg
tb_priority_encoder_4x2.v
Scope
Sources
Objects
Name
Value
data_in[3:0]
out[1:0]
DELAY[31:0]
f
3
00000014
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
80.000 ns


prorityencoder4x2 - [/home/akshay/prorityencoder4x2/prorityencoder4x2.xpr] - Vivado 2023.2
Quick Access
tcpg236-1
Project Summary
Device
tb_priority_encoder_4x2.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Reports
Design Runs
DRC
Power
Timing

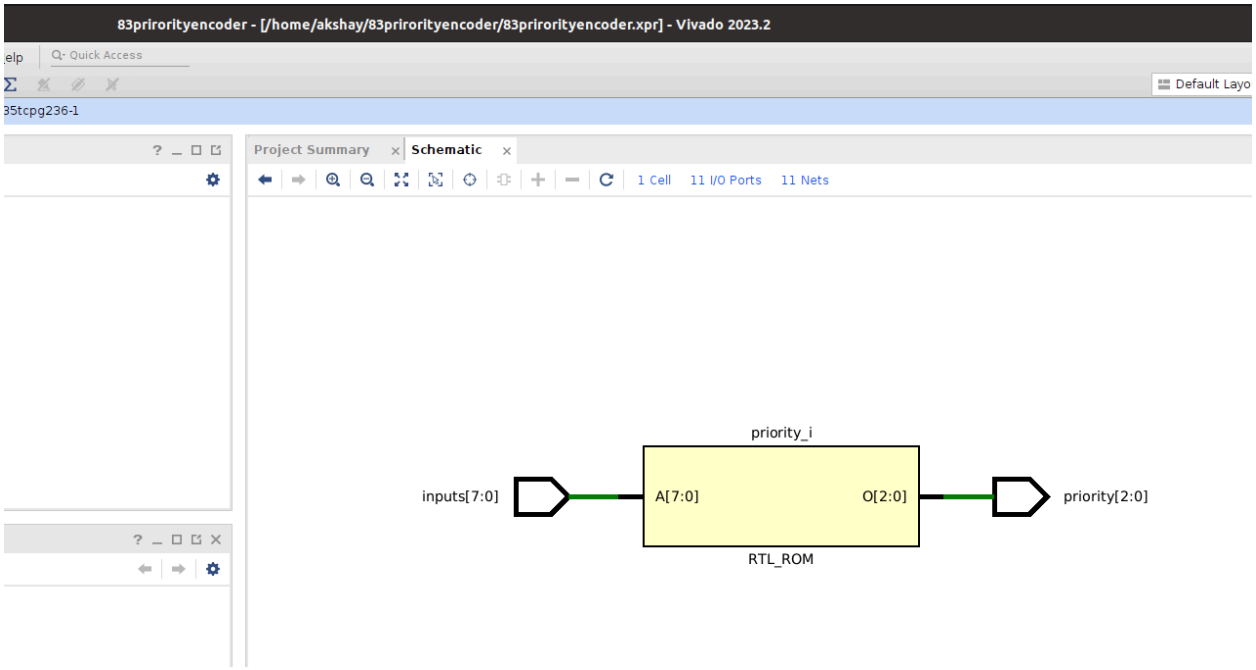
Q.21. Write Verilog code for 8:3 Priority Encoder.

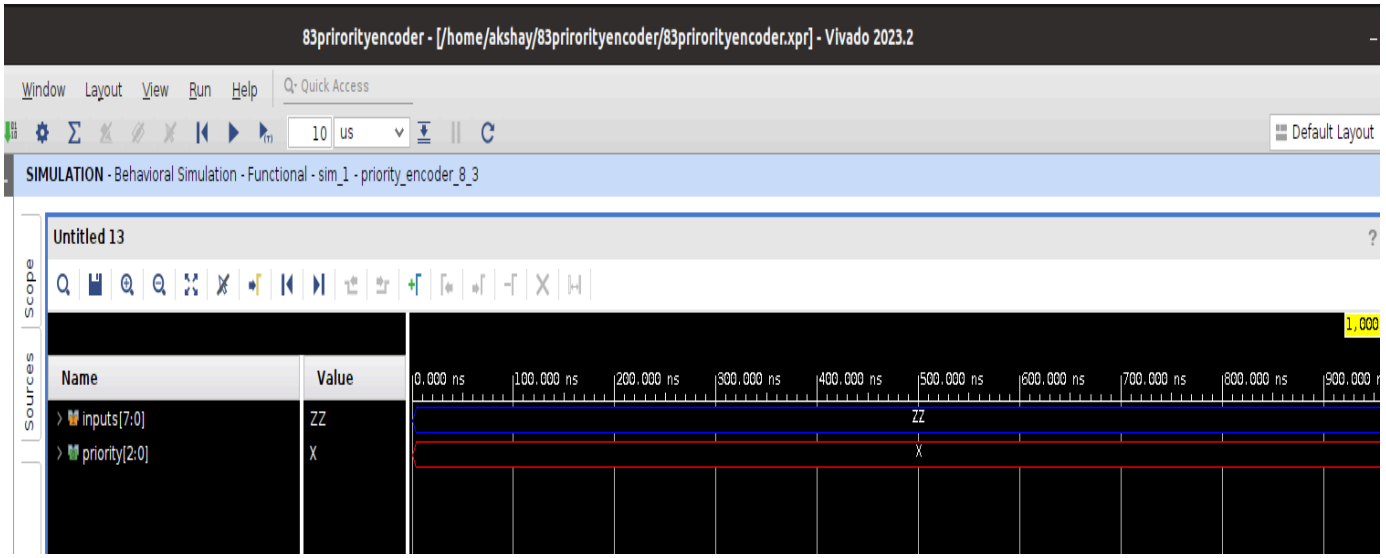
```
module priority_encoder_8_3(
    input [7:0] inputs,
    output reg [2:0] priority );
always @(*) begin
    case(inputs)
        8'b00000001: priority = 3'b000; // Input 0 has highest priority
        8'b00000010: priority = 3'b001; // Input 1 has higher priority than Input 0
        8'b00000100: priority = 3'b010; // Input 2 has higher priority than Input 0 and Input 1
        8'b00001000: priority = 3'b011; // Input 3 has higher priority than Input 0, 1, and 2
        8'b00010000: priority = 3'b100; // Input 4 has higher priority than Input 0-3
        8'b00100000: priority = 3'b101; // Input 5 has higher priority than Input 0-4
        8'b01000000: priority = 3'b110; // Input 6 has higher priority than Input 0-5
        8'b10000000: priority = 3'b111; // Input 7 has highest priority
        default: priority = 3'b000; // Default priority if no input is active
    endcase
end
endmodule
```

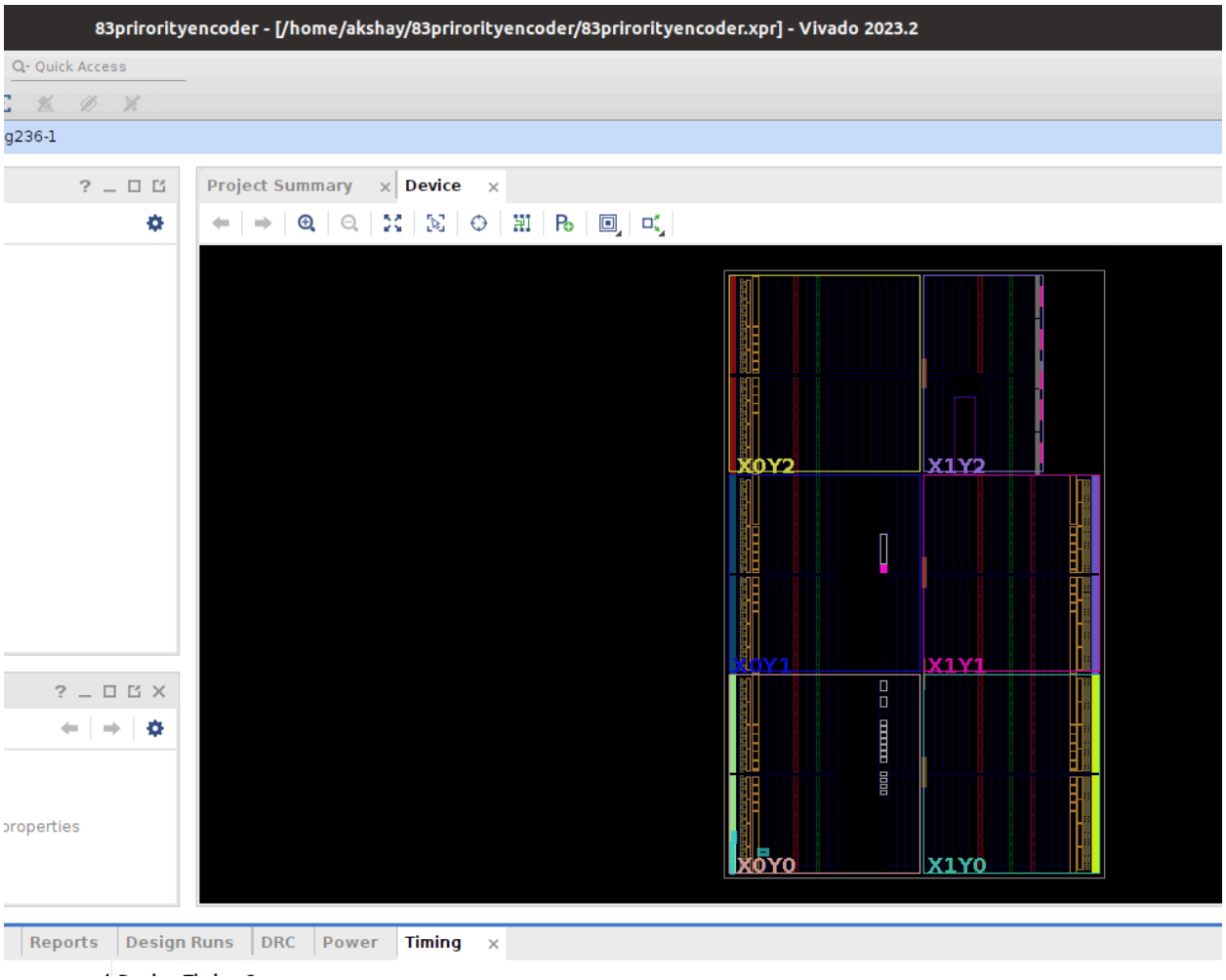
Testbench

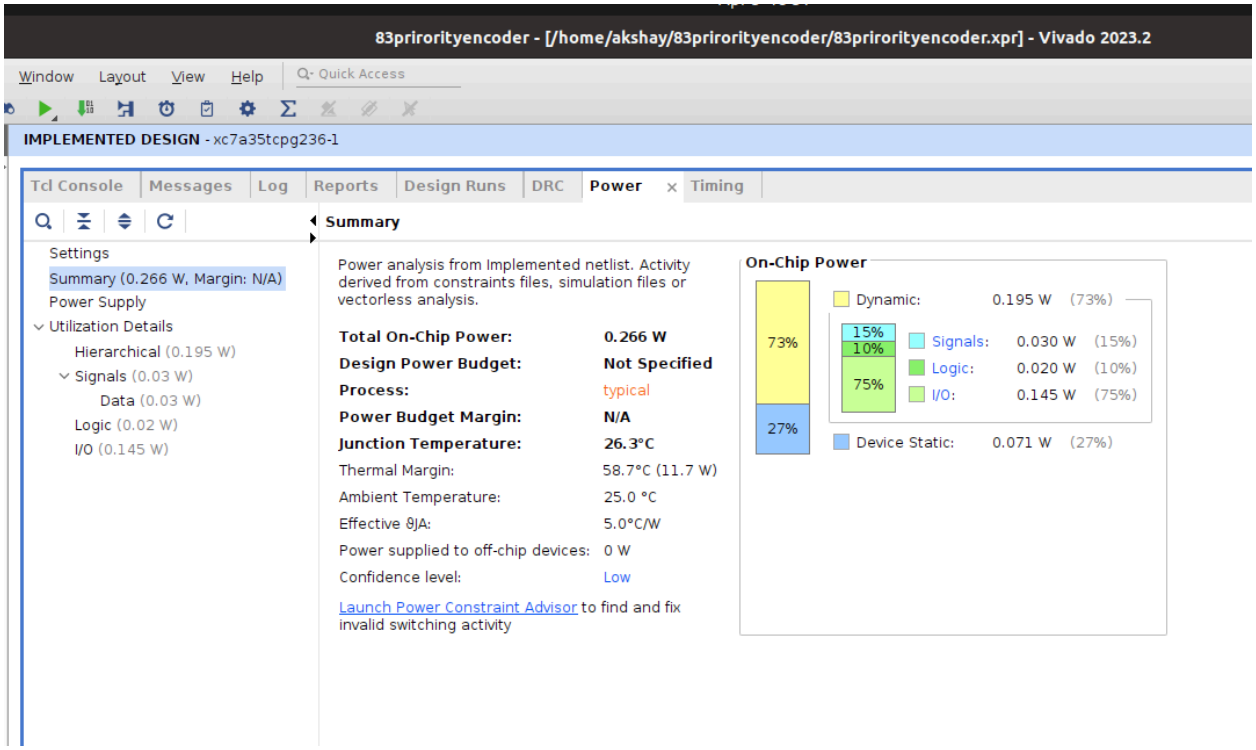
```
module tb;
  reg [7:0] D;
  wire [2:0] y;
    priority_encoder pri_enc(D, y);

  initial begin
```

```
    $monitor("D = %b -> y = %0b", D, y);
    repeat(5) begin
      D=$random; #1;
    end
  end
endmodule
```




83prirorityencoder - [/home/akshay/83prirorityencoder/83prirorityencoder.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
10
us
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - priority_encoder_8_3
Untitled 13
Scope
Sources
Name
Value
inputs[7:0]
ZZ
priority[2:0]
X
0.000 ns
100.000 ns
200.000 ns
300.000 ns
400.000 ns
500.000 ns
600.000 ns
700.000 ns
800.000 ns
900.000 ns
1,000


83prirorityencoder - [/home/akshay/83prirorityencoder/83prirorityencoder.xpr] - Vivado 2023.2
Quick Access
g236-1
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
roperties
Reports
Design Runs
DRC
Power
Timing


83prirorityencoder - [/home/akshay/83prirorityencoder/83prirorityencoder.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Settings
Summary (0.266 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.195 W)
Signals (0.03 W)
Data (0.03 W)
Logic (0.02 W)
I/O (0.145 W)
Summary
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.266 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 26.3°C
Thermal Margin: 58.7°C (11.7 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
73%
27%
Dynamic: 0.195 W (73%)
15%
10%
75%
Signals: 0.030 W (15%)
Logic: 0.020 W (10%)
I/O: 0.145 W (75%)
Device Static: 0.071 W (27%)

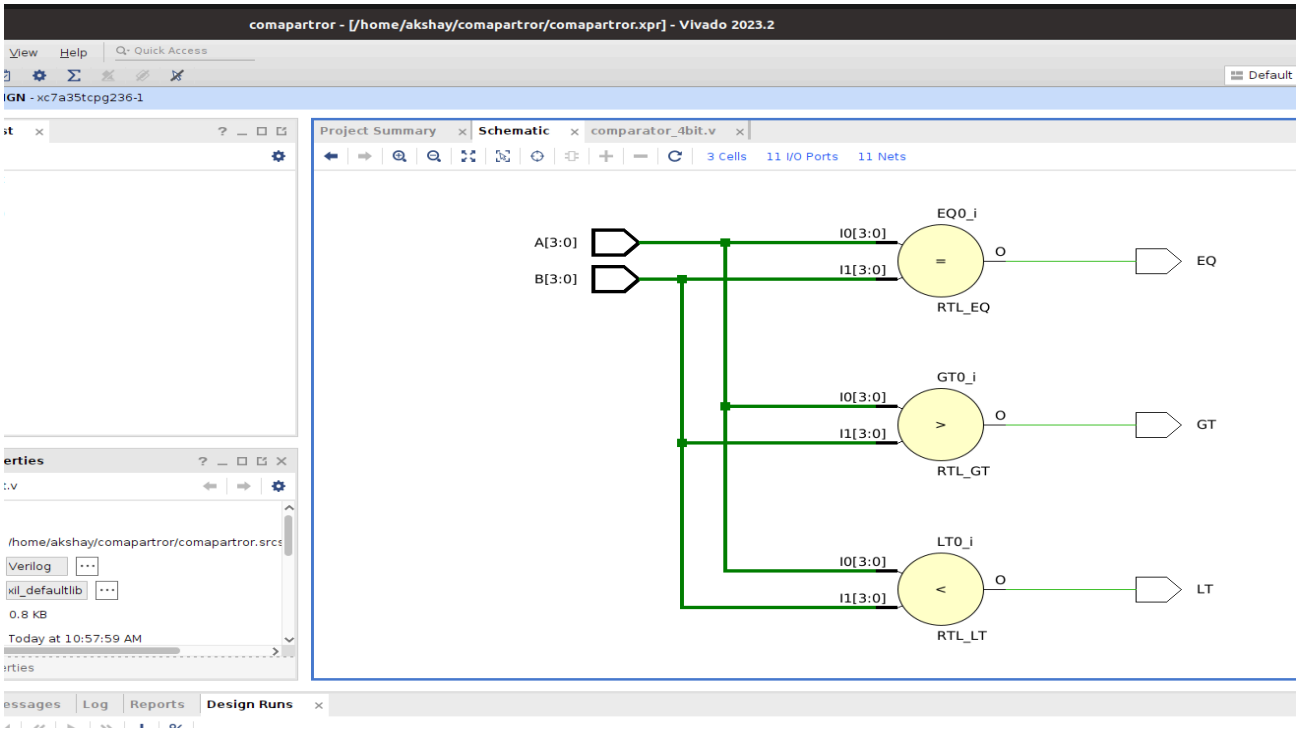
Q.22. Write Verilog code for 4-bit comparator.

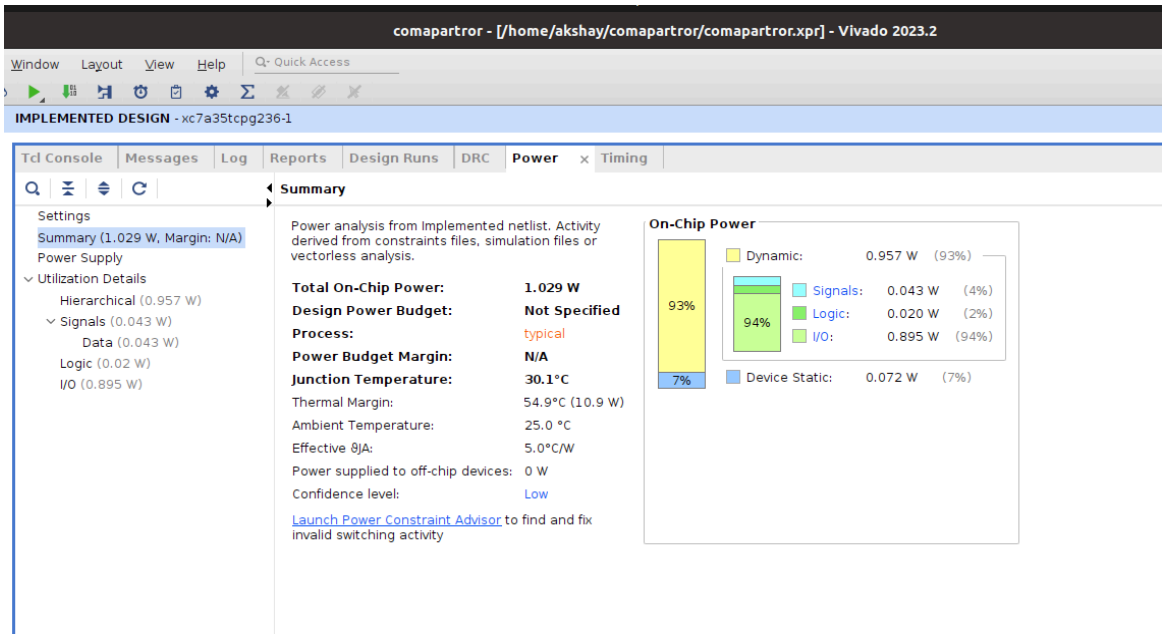
```
module comparator_4bit (
    input [3:0] A, // 4-bit input A
    input [3:0] B, // 4-bit input B
    output reg EQ, // Equal output
    output reg GT, // Greater Than output
    output reg LT  // Less Than output );
always @(*) begin
    EQ = (A == B);
    GT = (A > B);
    LT = (A < B);
End
endmodule
```

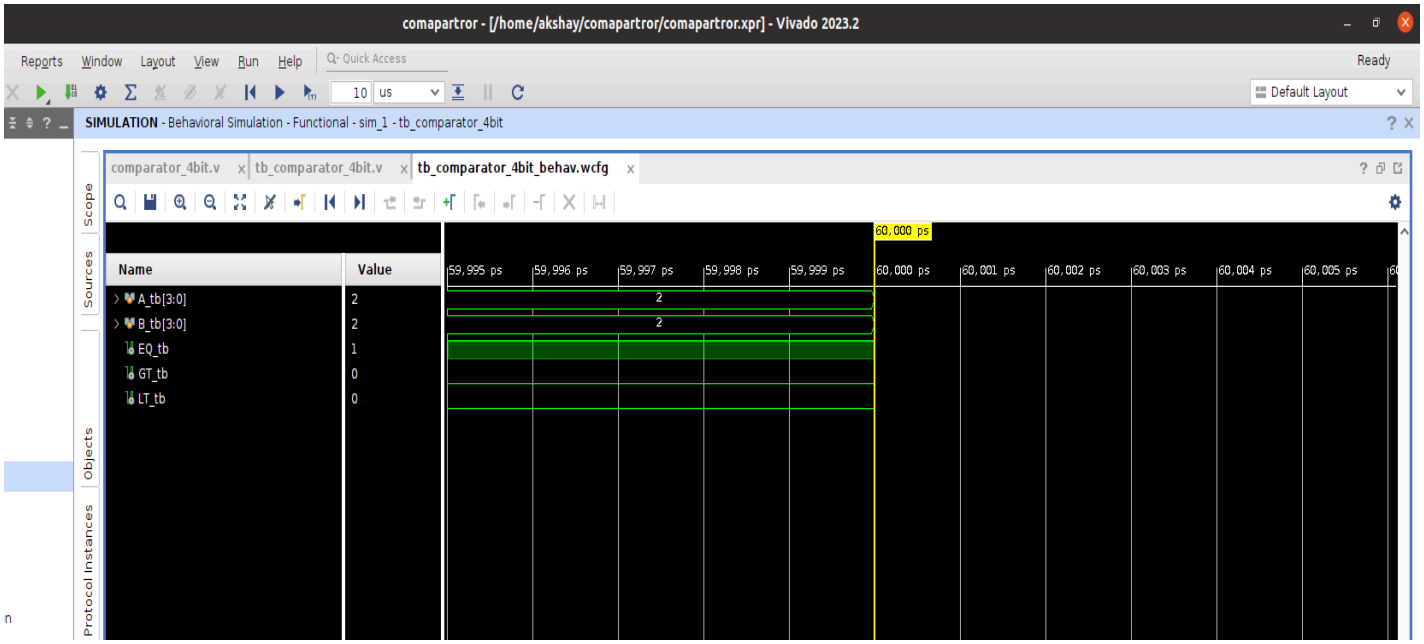
Testbench

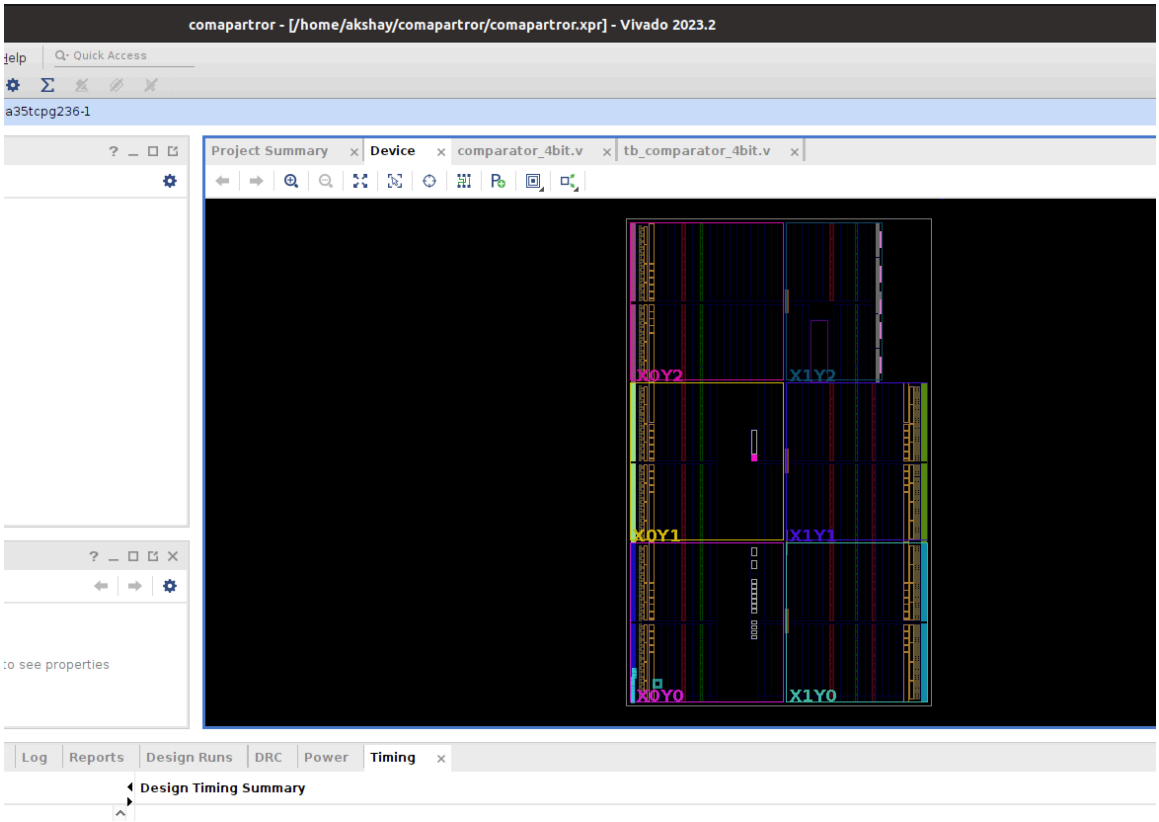
```
module tb_comparator_4bit;
reg [3:0] A_tb, B_tb;
wire EQ_tb, GT_tb, LT_tb;
comparator_4bit dut (
    (A_tb),  (B_tb), (EQ_tb), (GT_tb),  (LT_tb));
initial begin
    $display("A\tB\tEQ\tGT\tLT");
    A_tb = 4'b0000; B_tb = 4'b0000; #10;
    A_tb = 4'b0000; B_tb = 4'b0001; #10;
    A_tb = 4'b0001; B_tb = 4'b0000; #10;
    A_tb = 4'b0001; B_tb = 4'b0001; #10;
```

```
    A_tb = 4'b0010; B_tb = 4'b0001; #10;
    A_tb = 4'b0010; B_tb = 4'b0010; #10;
    $finish;
end
Endmodule
```


comapartror - [/home/akshay/comapartror/comapartror.xpr] - Vivado 2023.2
View
Help
Quick Access
Default
IGN - xc7a35tcpg236-1
Project Summary
Schematic
comparator_4bit.v
3 Cells
11 I/O Ports
11 Nets
A[3:0]
B[3:0]
EQ0_i
I0[3:0]
I1[3:0]
=
O
EQ
RTL_EQ
GT0_i
>
GT
RTL_GT
LT0_i
<
LT
RTL_LT
/home/akshay/comapartror/comapartror.srcs
Verilog
xil_defaultlib
0.8 KB
Today at 10:57:59 AM
Log
Reports
Design Runs


comapartror - [/home/akshay/comapartror/comapartror.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Summary
Settings
Summary (1.029 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.957 W)
Signals (0.043 W)
Data (0.043 W)
Logic (0.02 W)
I/O (0.895 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 1.029 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 30.1°C
Thermal Margin: 54.9°C (10.9 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
93%
7%
Dynamic: 0.957 W (93%)
94%
Signals: 0.043 W (4%)
Logic: 0.020 W (2%)
I/O: 0.895 W (94%)
Device Static: 0.072 W (7%)


comapartror - [/home/akshay/comapartror/comapartror.xpr] - Vivado 2023.2
Reports
Window
Layout
View
Run
Help
Quick Access
Ready
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_comparator_4bit
comparator_4bit.v
tb_comparator_4bit.v
tb_comparator_4bit_behav.wcfg
Scope
Sources
Objects
Protocol Instances
Name
Value
A_tb[3:0]
B_tb[3:0]
EQ_tb
GT_tb
LT_tb
60,000 ps
59,995 ps
59,996 ps
59,997 ps
59,998 ps
59,999 ps
60,000 ps
60,001 ps
60,002 ps
60,003 ps
60,004 ps
60,005 ps


comapartror - [/home/akshay/comapartror/comapartror.xpr] - Vivado 2023.2
Quick Access
a35tcpg236-1
Project Summary
Device
comparator_4bit.v
tb_comparator_4bit.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Log
Reports
Design Runs
DRC
Power
Timing
Design Timing Summary

Assignment-6 (sequential circuit)

Q.23. Write Verilog code for the following Latch:

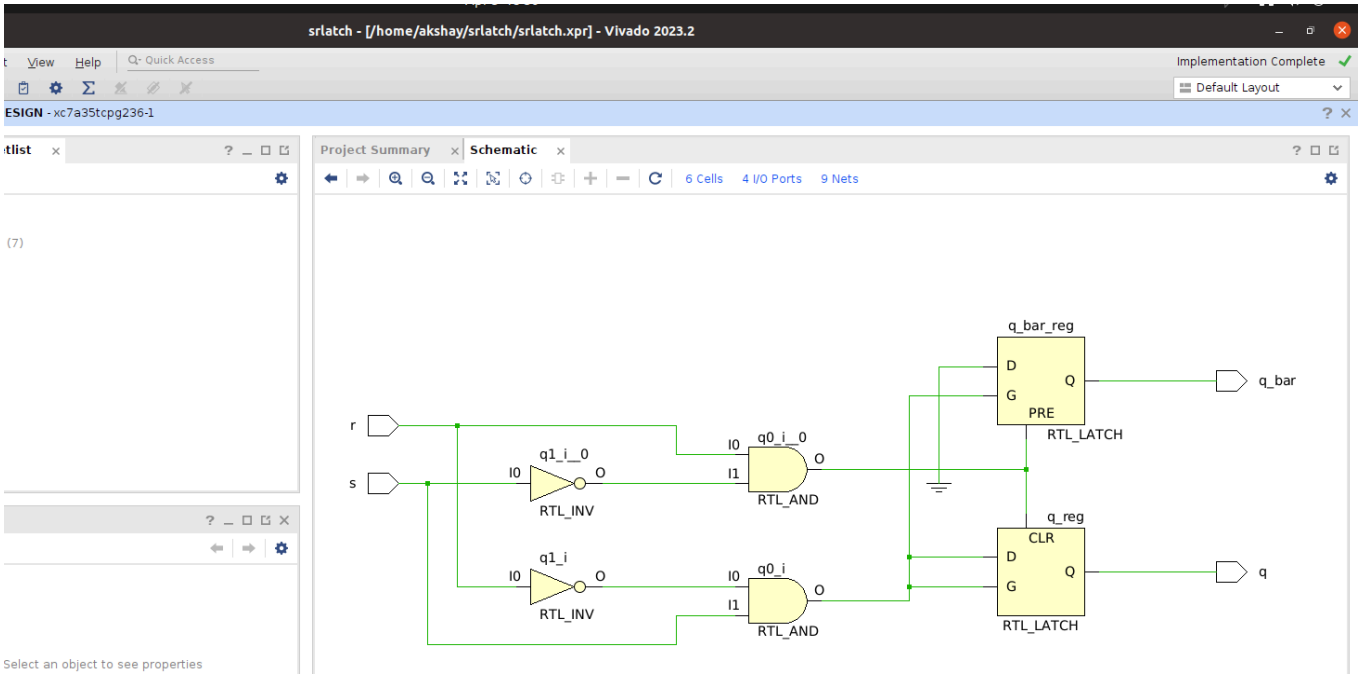
a. SR Latch :

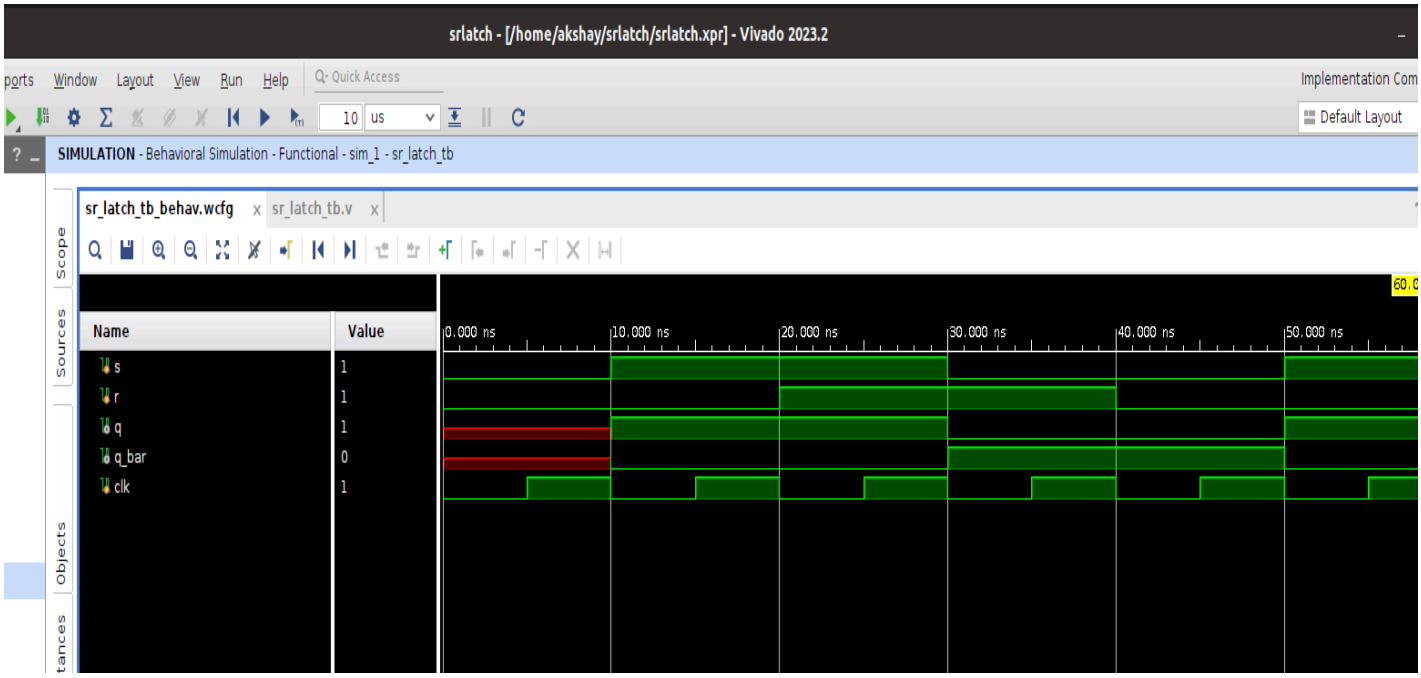
```
module sr_latch (
    input s, r, // Set and Reset inputs
    output reg q, q_bar // Outputs );
always @* begin
    if (r && !s)      // Reset has priority
        begin
            q <= 0;
            q_bar <= 1;
        end
    else if (!r && s) // Set
        begin
            q <= 1;
            q_bar <= 0;
        end
    // Else, maintain previous state
end
endmodule
```

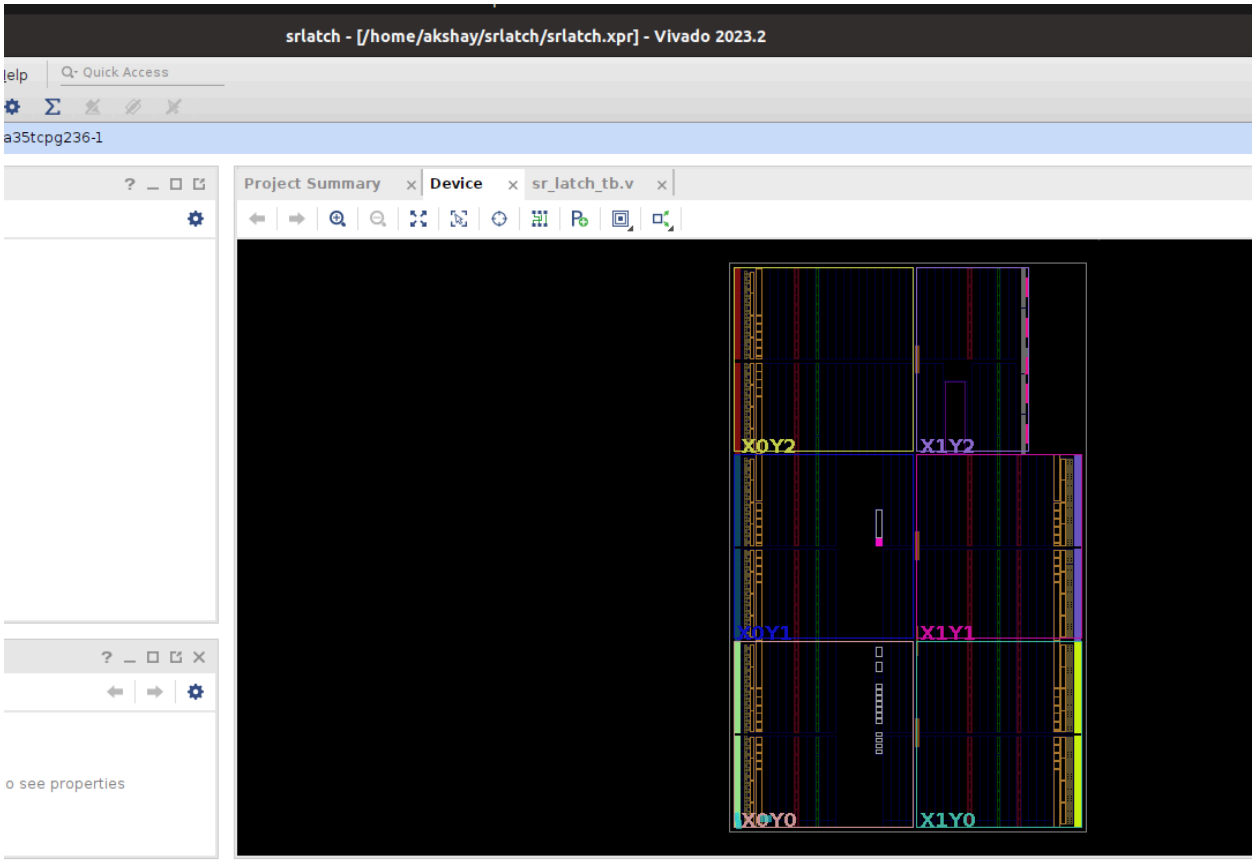
Testbench

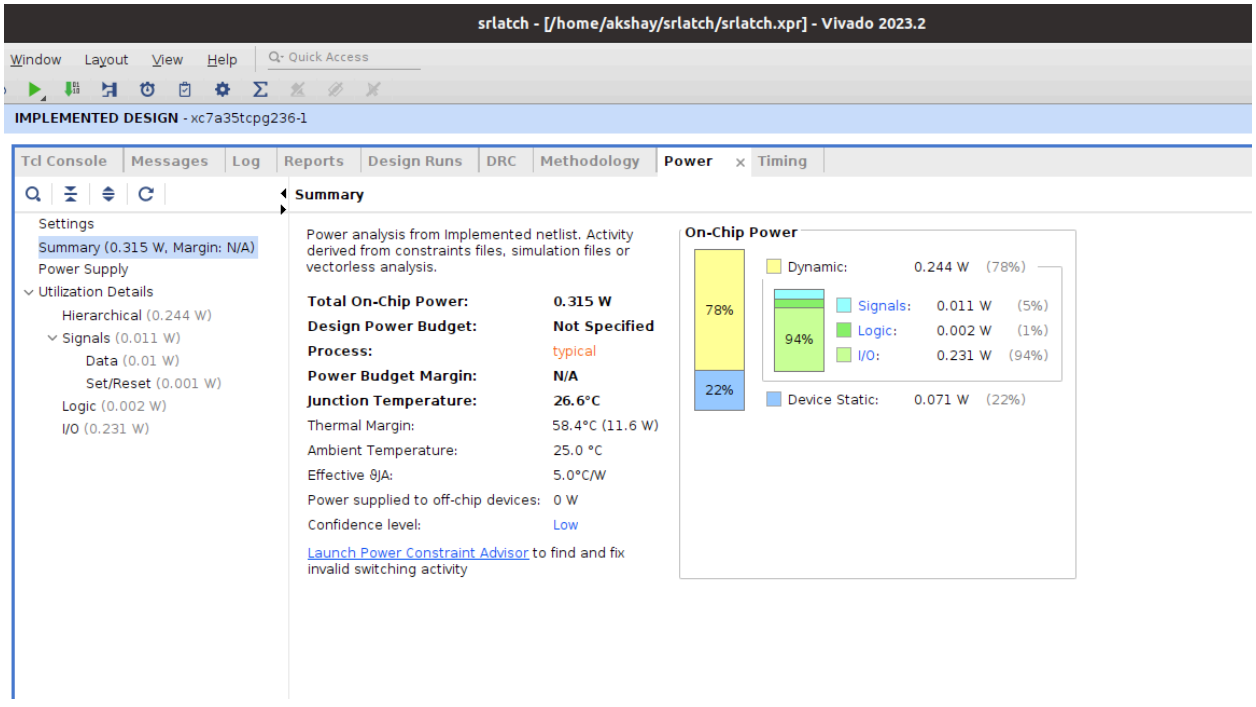
```
module sr_latch_tb;
    // Inputs
    reg s, r;
```

```
    // Outputs
    wire q, q_bar;
    // Instantiate the SR latch module
    sr_latch dut(
        s, r ,q,  q_bar)
 // Clock generation
    reg clk;
    always #5 clk = ~clk; // Toggle clock every 5 time units
// Stimulus generation
    initial begin
        // Initialize inputs
        s = 0 ;     r = 0;
        clk = 0;
   // Apply inputs and observe outputs
        #10 s = 1; // Set
        #10 r = 1; // Reset
        #10 s = 0; // Release set
        #10 r = 0; // Release reset
        #10 s = 1; // Set again
        #10 r = 1; // Reset again
        // Add more test cases as needed
    // Finish simulation
        $finish;
    end
endmodule
```


srlatch - [/home/akshay/srlatch/srlatch.xpr] - Vivado 2023.2
View
Help
Quick Access
Implementation Complete
Default Layout
ESIGN - xc7a35tcpg236-1
Project Summary
Schematic
6 Cells
4 I/O Ports
9 Nets
r
s
q1_i__0
RTL_INV
q0_i__0
RTL_AND
q_bar_reg
D
G
Q
PRE
RTL_LATCH
q_bar
q1_i
RTL_INV
q0_i
RTL_AND
q_reg
CLR
RTL_LATCH
q
Select an object to see properties


srlatch - [/home/akshay/srlatch/srlatch.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Implementation Com
10
us
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - sr_latch_tb
sr_latch_tb_behav.wcfg
sr_latch_tb.v
Scope
Sources
Objects
Name
Value
s
1
r
1
q
1
q_bar
0
clk
1
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns


srlatch - [/home/akshay/srlatch/srlatch.xpr] - Vivado 2023.2
Quick Access
a35tcpg236-1
Project Summary
Device
sr_latch_tb.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
o see properties
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Design Timing Summary


srlatch - [/home/akshay/srlatch/srlatch.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Settings
Summary (0.315 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.244 W)
Signals (0.011 W)
Data (0.01 W)
Set/Reset (0.001 W)
Logic (0.002 W)
I/O (0.231 W)
Summary
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.315 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 26.6°C
Thermal Margin: 58.4°C (11.6 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
78%
22%
94%
Dynamic: 0.244 W (78%)
Signals: 0.011 W (5%)
Logic: 0.002 W (1%)
I/O: 0.231 W (94%)
Device Static: 0.071 W (22%)

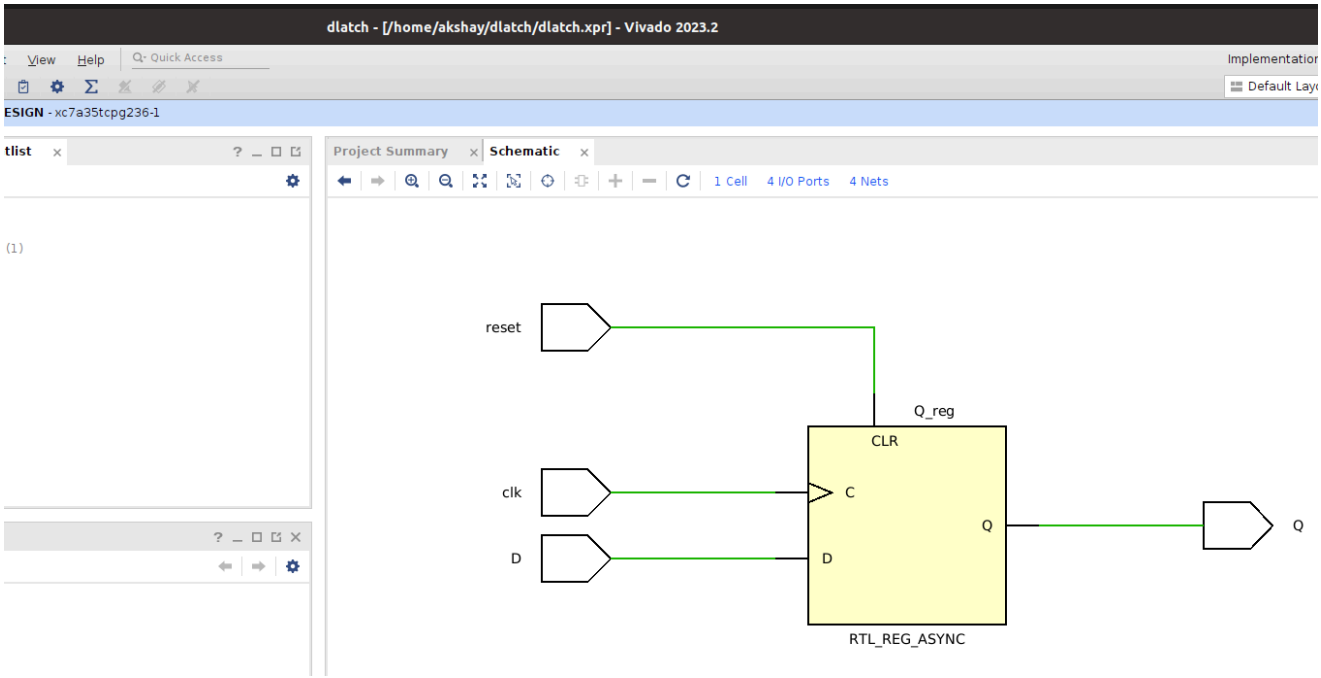
b. D Latch :

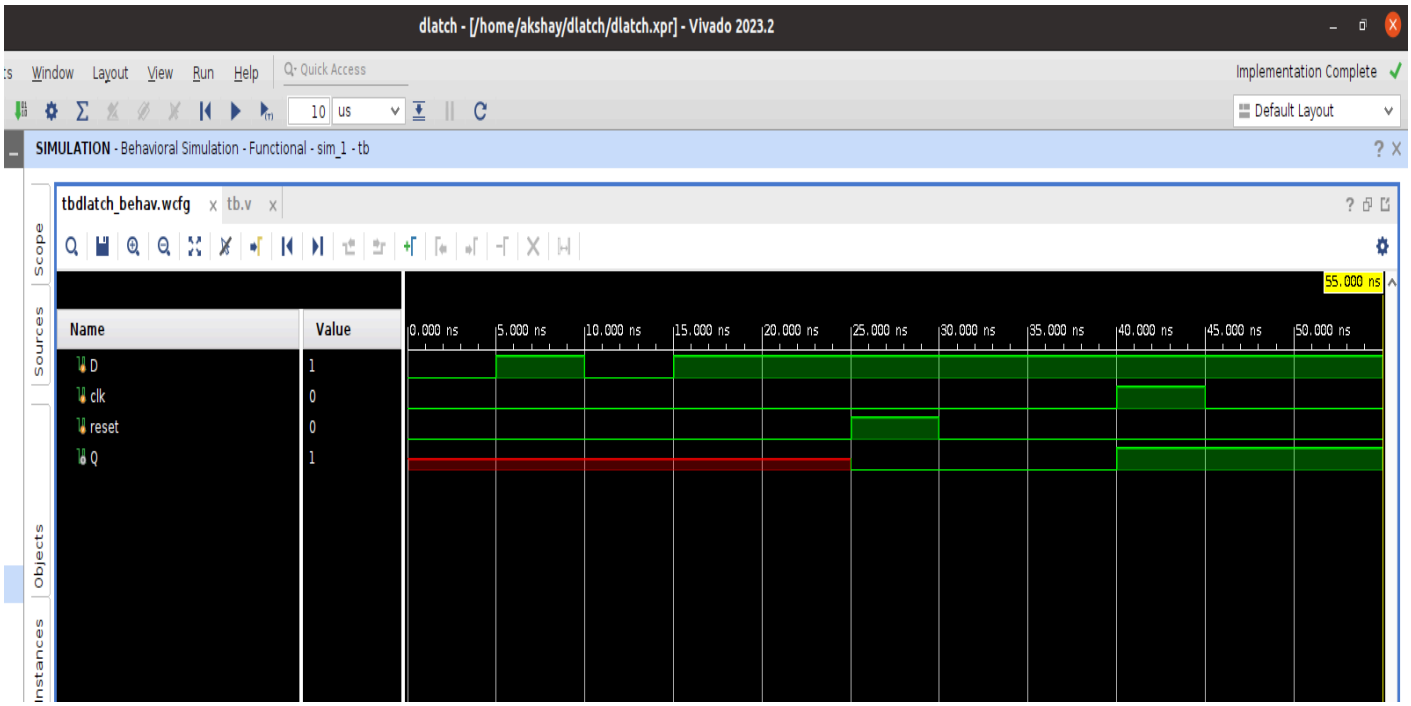
```
module D_Latch(
    input  D,      // Data input
    input  clk,    // Clock input
    input reset,  // Reset input
    output reg Q       // Output );
    always @(posedge clk or posedge reset) begin
        if (reset) begin
            Q <= 1'b0; // Reset the latch to 0 when reset is active
        end else begin
            Q <= D; // Store D input value on clock rising edge
        end
    end
endmodule
```

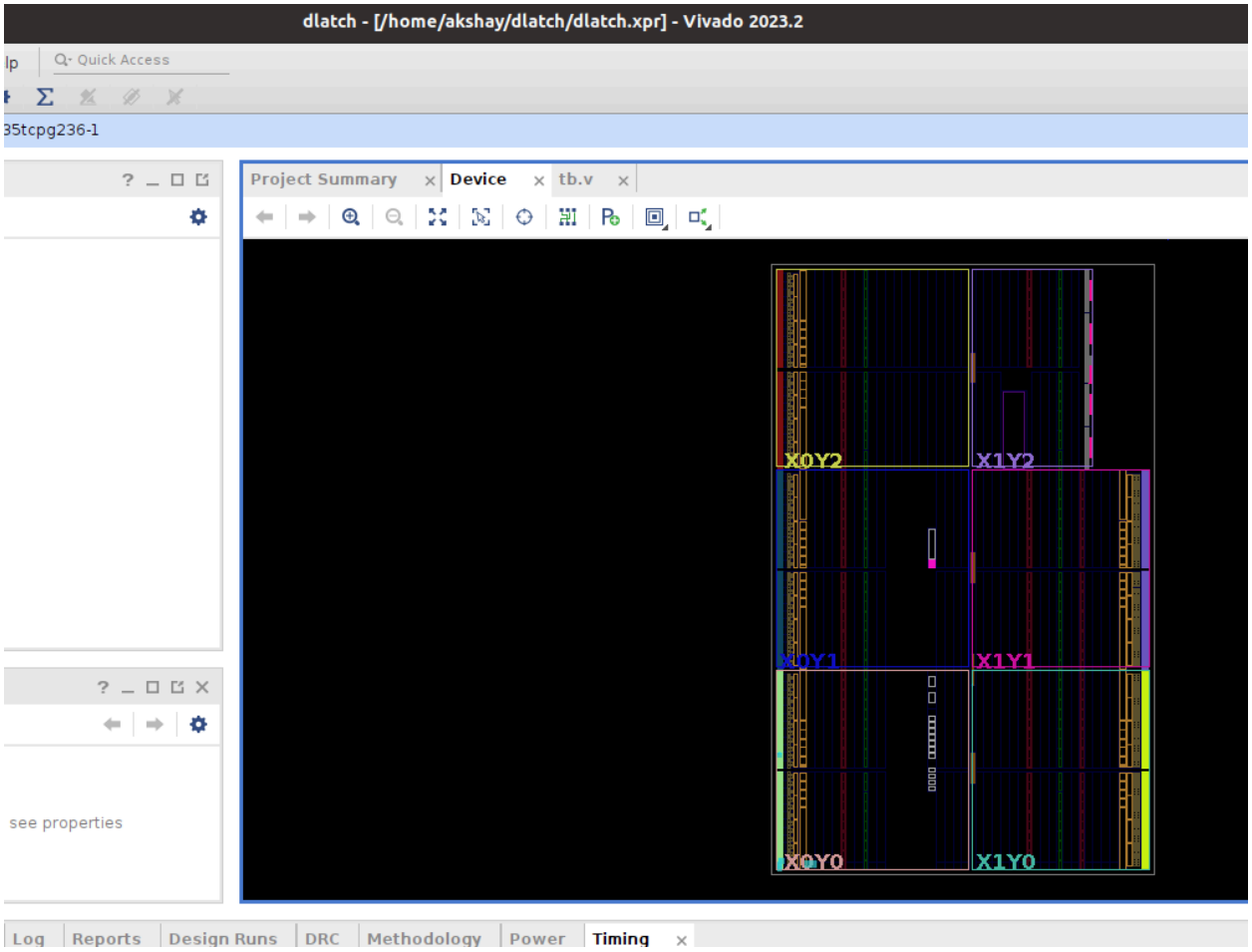
Testbench

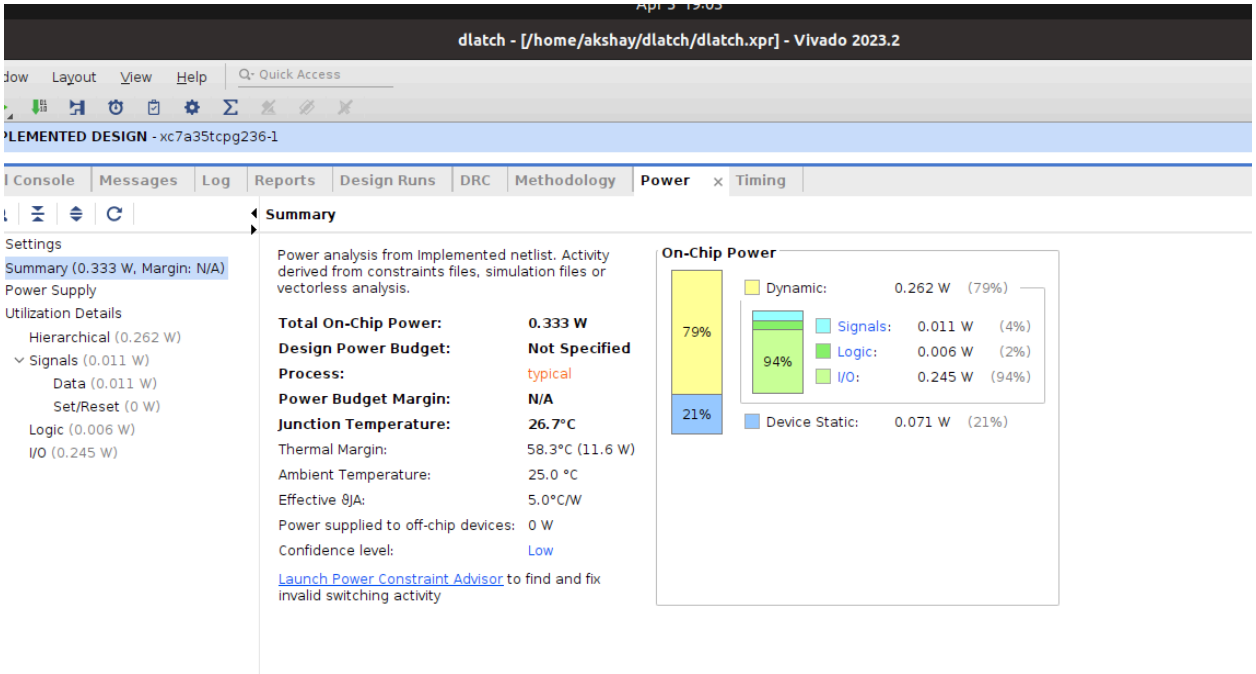
```
module tb;
    reg D;
    reg clk;
    reg reset;
    wire Q;
  D_Latch dut (
        D,
        (clk),
        (reset),
        (Q)    );
```

```
    initial begin
        // Initialize inputs
        D = 1'b0;
        clk = 1'b0;
        reset = 1'b0;

        // Toggle clock and D input
        #5 D = 1'b1;
        #5 D = 1'b0;
        #5 D = 1'b1;

        // Toggle reset
        #10 reset = 1'b1;
        #5 reset = 1'b0;

        // Toggle clock
        #10 clk = 1'b1;
        #5 clk = 1'b0;

    // Stop simulation
        #10 $finish;
    End
endmodule
```


dlatch - [/home/akshay/dlatch/dlatch.xpr] - Vivado 2023.2
View
Help
Quick Access
Implementation
Default Lay
ESIGN - xc7a35tcpg236-1
tlist
Project Summary
Schematic
1 Cell
4 I/O Ports
4 Nets
reset
Q_reg
CLR
clk
C
Q
D
D
Q
RTL_REG_ASYNC


dlatch - [/home/akshay/dlatch/dlatch.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Implementation Complete
10
us
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb
tbdlatch_behav.wcfg
tb.v
Scope
Sources
Objects
Instances
Name
Value
D
1
clk
0
reset
0
Q
1
55.000 ns
0.000 ns
5.000 ns
10.000 ns
15.000 ns
20.000 ns
25.000 ns
30.000 ns
35.000 ns
40.000 ns
45.000 ns
50.000 ns


dlatch - [/home/akshay/dlatch/dlatch.xpr] - Vivado 2023.2
Quick Access
35tcpg236-1
Project Summary
Device
tb.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
see properties
Log
Reports
Design Runs
DRC
Methodology
Power
Timing


dlatch - [/home/akshay/dlatch/dlatch.xpr] - Vivado 2023.2
Layout
View
Help
Quick Access
PLEMENTED DESIGN - xc7a35tcpg236-1
Console
Messages
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Settings
Summary (0.333 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.262 W)
Signals (0.011 W)
Data (0.011 W)
Set/Reset (0 W)
Logic (0.006 W)
I/O (0.245 W)
Summary
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.333 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 26.7°C
Thermal Margin: 58.3°C (11.6 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
79%
21%
94%
Dynamic: 0.262 W (79%)
Signals: 0.011 W (4%)
Logic: 0.006 W (2%)
I/O: 0.245 W (94%)
Device Static: 0.071 W (21%)

Q.24. Write Verilog code for the following flip flops:

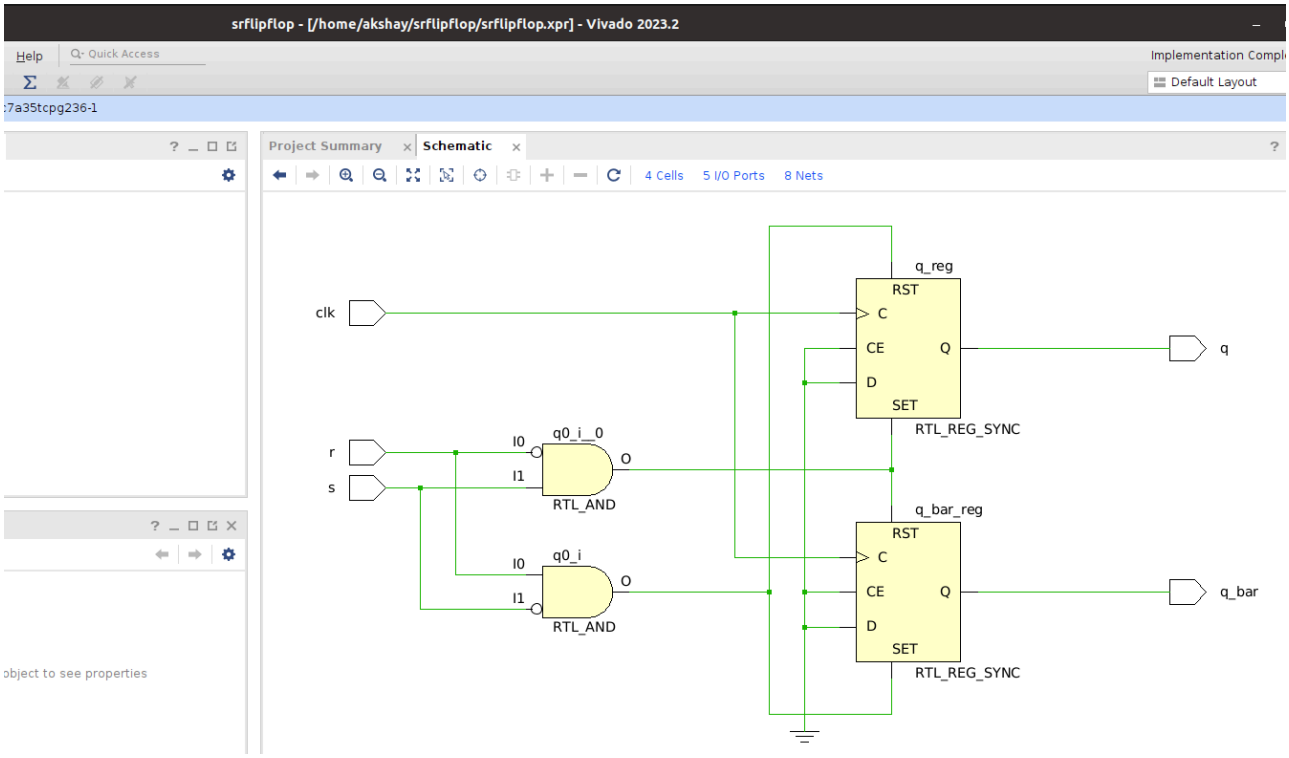
a. SR Flipflop :

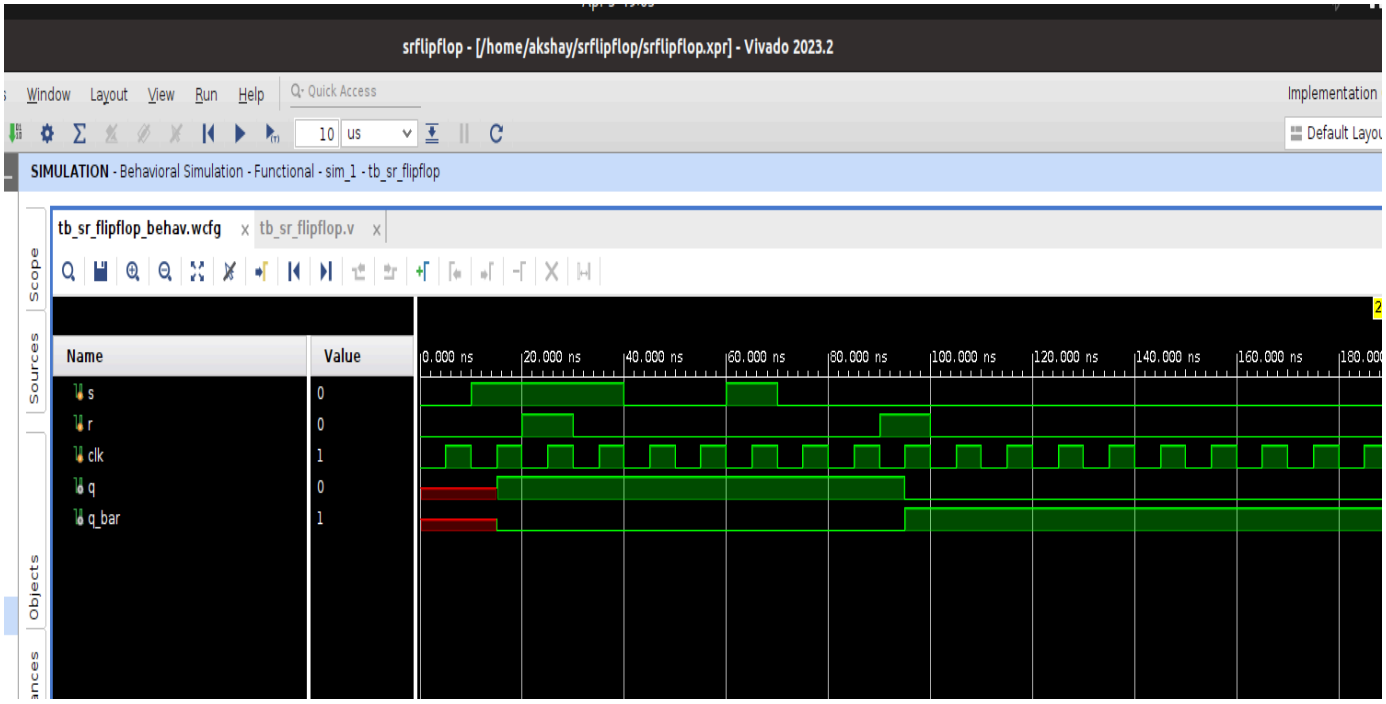
```
module sr_flipflop(
    input wire s, // Set input
    input wire r, // Reset input
    input wire clk, // Clock input
    output reg q, // Output Q
    output reg q_bar // Output Q-bar );
    always @(posedge clk) begin
        if (r && ~s) begin // Reset has priority
            q <= 0;
            q_bar <= 1;
        end else if (~r && s) begin // Set has priority
            q <= 1;
            q_bar <= 0;
        end else begin // No change
            q <= q;
            q_bar <= q_bar;
        end
    end
endmodule
```

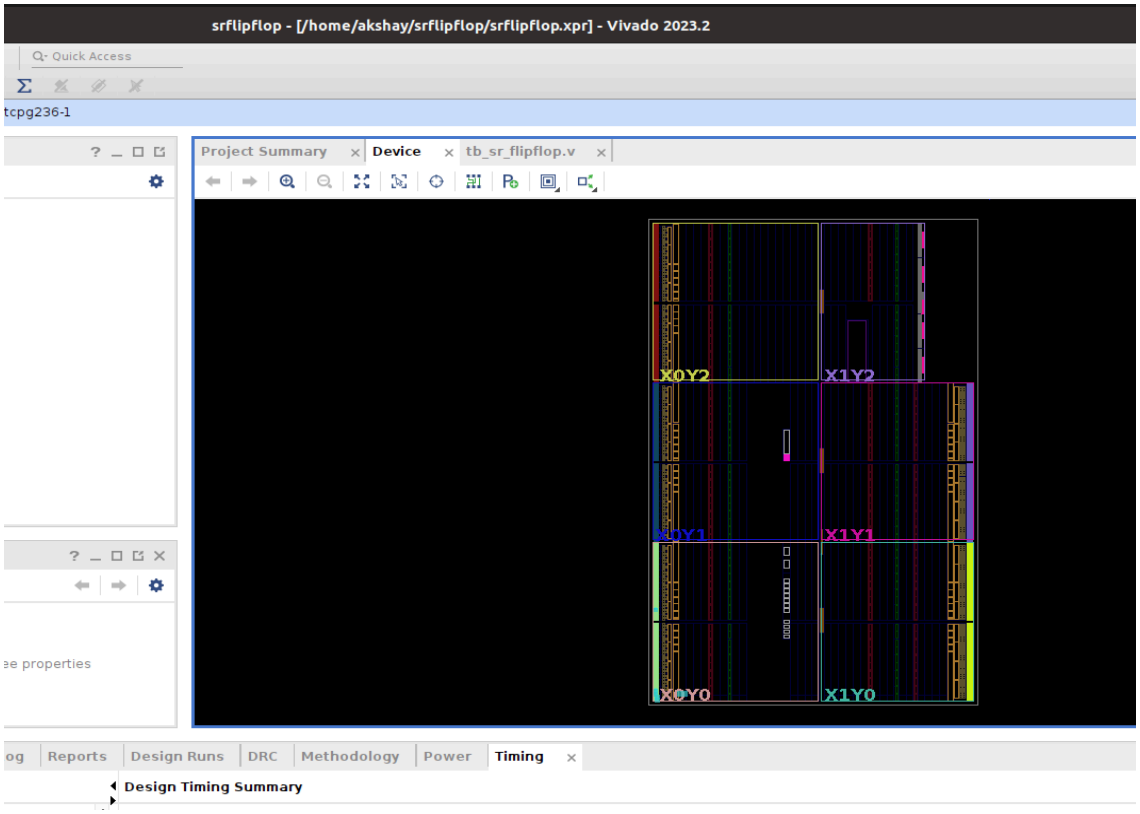
Testbench

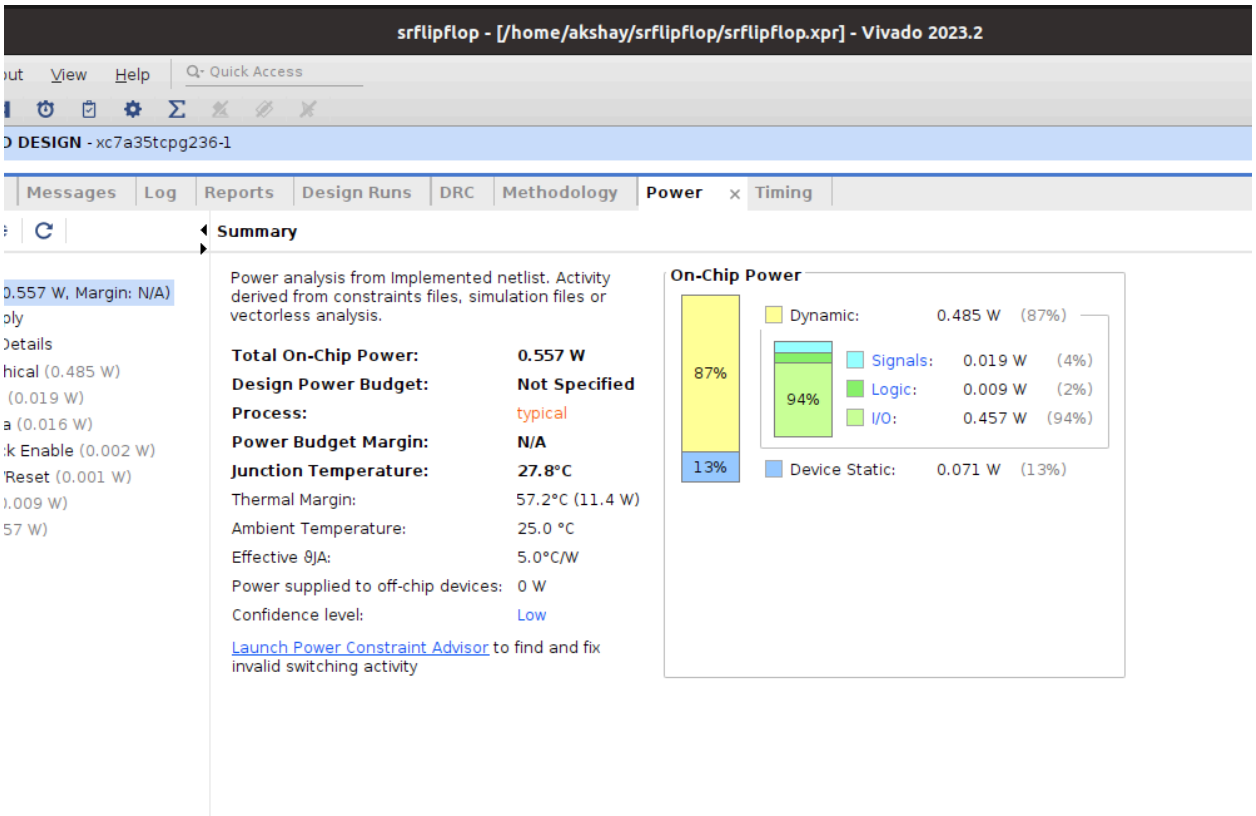
```
module tb_sr_flipflop();
  // Inputs
    reg s, r, clk;
```

```
    // Outputs
    wire q, q_bar;
     // Instantiate the sr_flipflop module
    sr_flipflop dut (
        s,r, clk, q,  q_bar);
// Clock generation
    always begin
        #5 clk = ~clk;
    end
   // Stimulus
    initial begin
        // Initialize inputs
        s = 0; r = 0;  clk = 0;
        // Apply stimulus
        #10 s = 1; // Set input
        #10 r = 1; // Reset input
        #10 r = 0;  #10 s = 0;
        #20 s = 1; // Set input
        #10 s = 0;
        #20 r = 1; // Reset input   #10 r = 0
        // Add more stimulus as needed
        #100 $finish; // Finish simulation
    end
endmodule
```


srflipflop - [/home/akshay/srflipflop/srflipflop.xpr] - Vivado 2023.2
Help
Quick Access
Implementation Compl
Default Layout
:7a35tcpg236-1
Project Summary
Schematic
4 Cells
5 I/O Ports
8 Nets
clk
r
s
q_reg
RST
C
CE
Q
D
SET
RTL_REG_SYNC
q
q0_i__0
I0
I1
O
RTL_AND
q_bar_reg
q0_i
q_bar
object to see properties


srflipflop - [/home/akshay/srflipflop/srflipflop.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Implementation
10
us
Default Layou
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_sr_flipflop
tb_sr_flipflop_behav.wcfg
tb_sr_flipflop.v
Scope
Sources
Objects
Name
Value
s
r
clk
q
q_bar
0
0
1
0
1
0.000 ns
20.000 ns
40.000 ns
60.000 ns
80.000 ns
100.000 ns
120.000 ns
140.000 ns
160.000 ns


srflipflop - [/home/akshay/srflipflop/srflipflop.xpr] - Vivado 2023.2
Quick Access
tcpg236-1
Project Summary
Device
tb_sr_flipflop.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Reports
Design Runs
DRC
Methodology
Power
Timing
Design Timing Summary


srflipflop - [/home/akshay/srflipflop/srflipflop.xpr] - Vivado 2023.2
View
Help
Quick Access
DESIGN - xc7a35tcpg236-1
Messages
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Summary
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.557 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 27.8°C
Thermal Margin: 57.2°C (11.4 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
87%
13%
Dynamic: 0.485 W (87%)
94%
Signals: 0.019 W (4%)
Logic: 0.009 W (2%)
I/O: 0.457 W (94%)
Device Static: 0.071 W (13%)

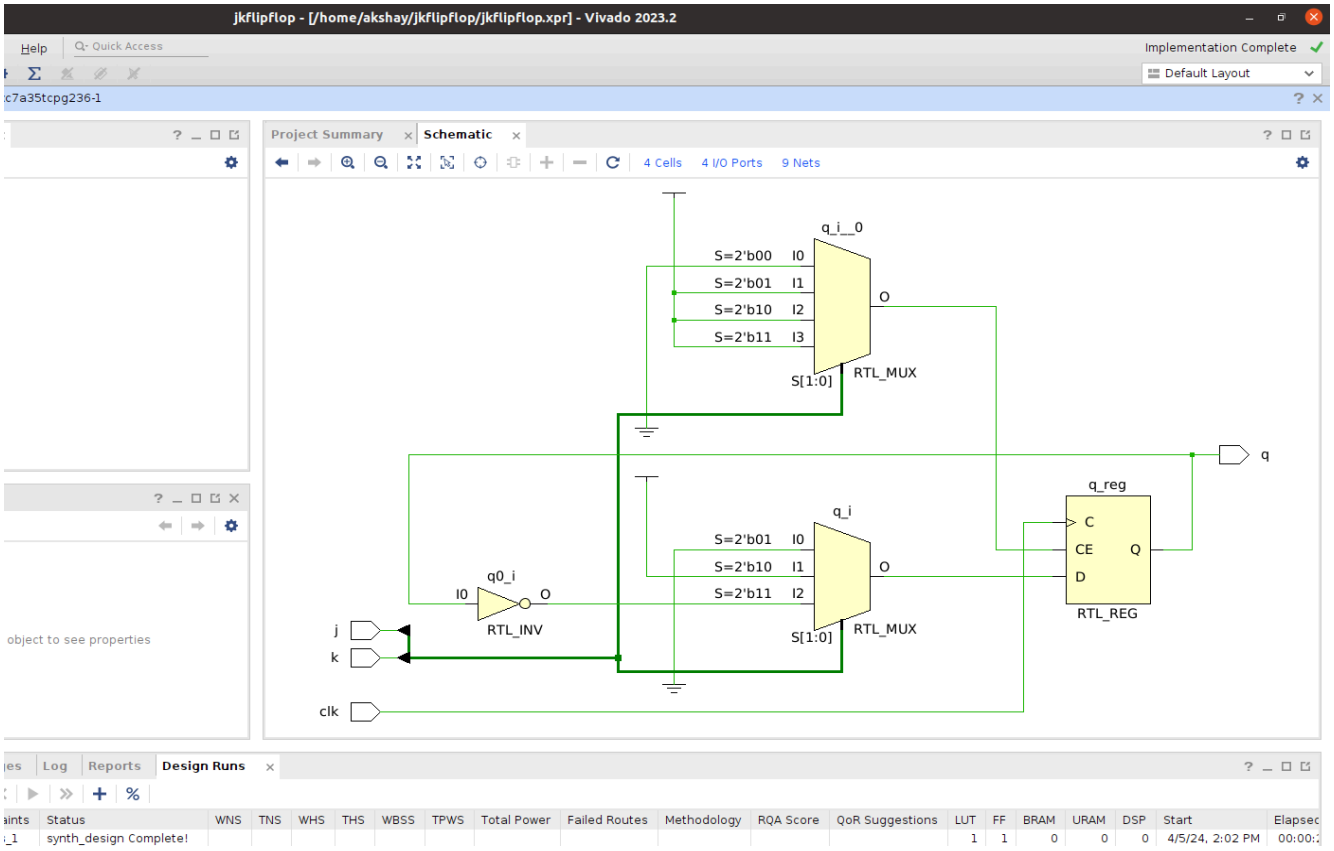
b. JK Flipflop :

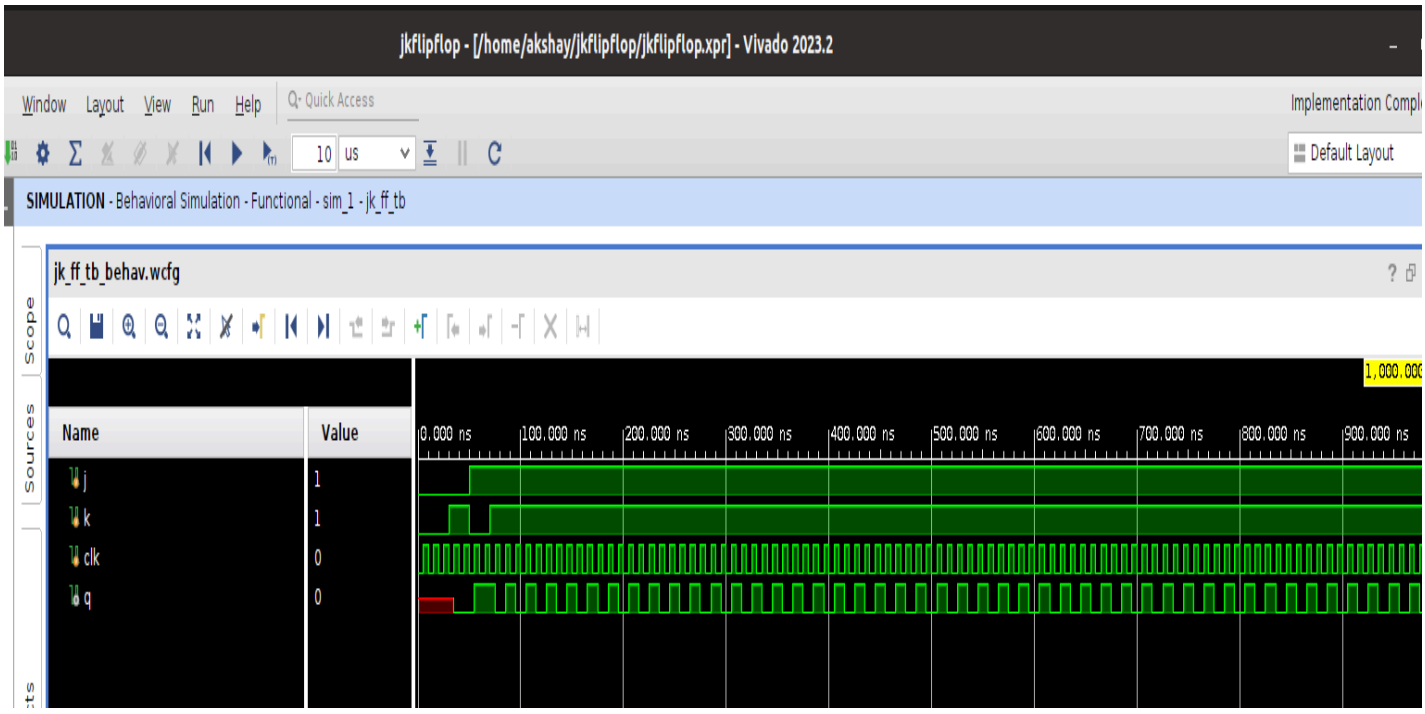
```
module jk_ff ( input j,
input k,
input clk,
output q);
reg q;
always @ (posedge clk)
case ({j,k})
2'b00 : q <= q;
2'b01 : q <= 0;
2'b10 : q <= 1;
2'b11 : q <= ~q;
endcase
endmodule
```

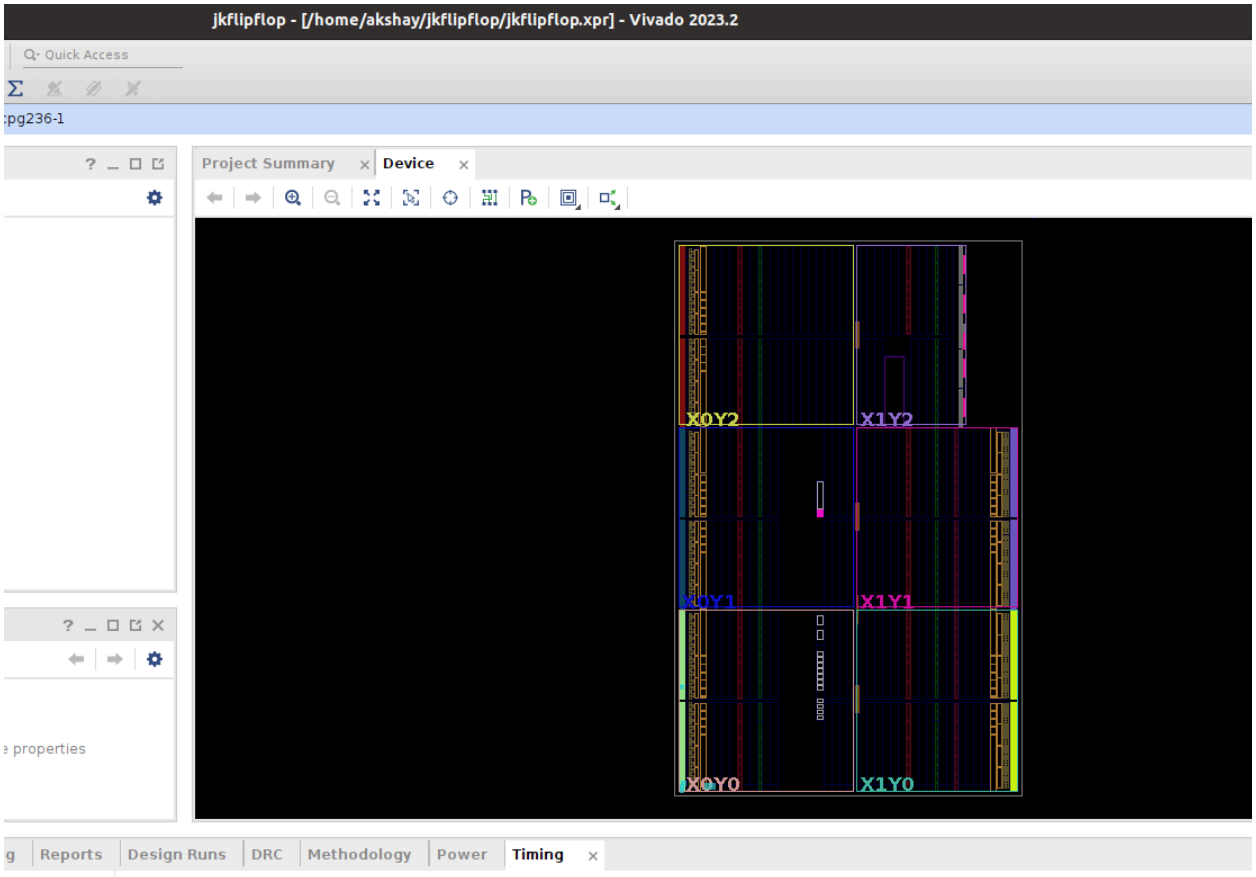
Testbench

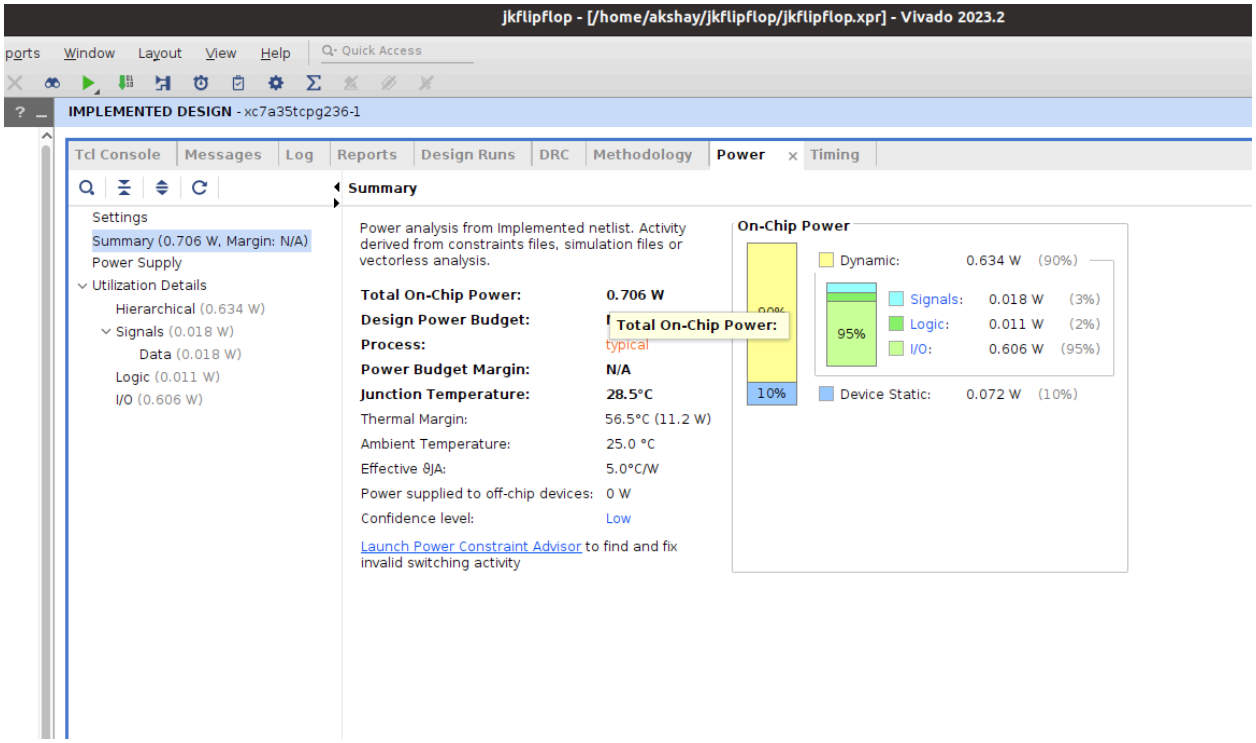
```
module jk_ff_tb;
    // Inputs
    reg j, k, clk;
    // Output
    wire q;
    // Instantiate the jk_ff module
    jk_ff dut (   j,     k,        clk,  q );
// Clock generation
    always begin
        #5 clk = ~clk;  // Toggle clock every 5 time units
```

```
    end
   // Stimulus
    initial begin
        j = 0; k = 0; clk = 0;  // Initialize inputs
        #10;  // Wait for a few time units


        // Test case 1: No change (00)
        j = 0; k = 0;
        #20;  // Wait for a few time units
        // Expected: q remains unchanged
        // Test case 2: Set q to 0 (01)
        j = 0; k = 1;
        #20;  // Wait for a few time units
        // Expected: q = 0
       // Test case 3: Set q to 1 (10)
        j = 1; k = 0;
        #20;  // Wait for a few time units
        // Expected: q = 1
 // Test case 4: Toggle q (11)
        j = 1; k = 1;
        #20;  // Wait for a few time units
        // Expected: q toggles its state
   // End simulation
    end
endmodule
```


jkflipflop - [/home/akshay/jkflipflop/jkflipflop.xpr] - Vivado 2023.2
Help
Quick Access
Implementation Complete
Default Layout
c7a35tcpg236-1
Project Summary
Schematic
4 Cells
4 I/O Ports
9 Nets
q_i__0
S=2'b00
S=2'b01
S=2'b10
S=2'b11
I0
I1
I2
I3
O
S[1:0]
RTL_MUX
q
q_reg
C
CE
D
Q
RTL_REG
q_i
q0_i
RTL_INV
j
k
clk
object to see properties
Log
Reports
Design Runs
Status
WNS
TNS
WHS
THS
WBSS
TPWS
Total Power
Failed Routes
Methodology
RQA Score
QoR Suggestions
LUT
FF
BRAM
URAM
DSP
Start
Elapsed
synth_design Complete!
4/5/24, 2:02 PM


jkflipflop - [/home/akshay/jkflipflop/jkflipflop.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Implementation Compl
10
us
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - jk_ff_tb
jk_ff_tb_behav.wcfg
Scope
Sources
Name
Value
j
k
clk
q
1
1
0
0
0.000 ns
100.000 ns
200.000 ns
300.000 ns
400.000 ns
500.000 ns
600.000 ns
700.000 ns
800.000 ns
900.000 ns


jkflipflop - [/home/akshay/jkflipflop/jkflipflop.xpr] - Vivado 2023.2
Quick Access
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Reports
Design Runs
DRC
Methodology
Power
Timing


jkflipflop - [/home/akshay/jkflipflop/jkflipflop.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Summary
Settings
Summary (0.706 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.634 W)
Signals (0.018 W)
Data (0.018 W)
Logic (0.011 W)
I/O (0.606 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.706 W
Design Power Budget:
Process: typical
Power Budget Margin: N/A
Junction Temperature: 28.5°C
Thermal Margin: 56.5°C (11.2 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
Total On-Chip Power:
On-Chip Power
Dynamic: 0.634 W (90%)
Signals: 0.018 W (3%)
Logic: 0.011 W (2%)
I/O: 0.606 W (95%)
95%
10%
Device Static: 0.072 W (10%)

c. D Flipflop :

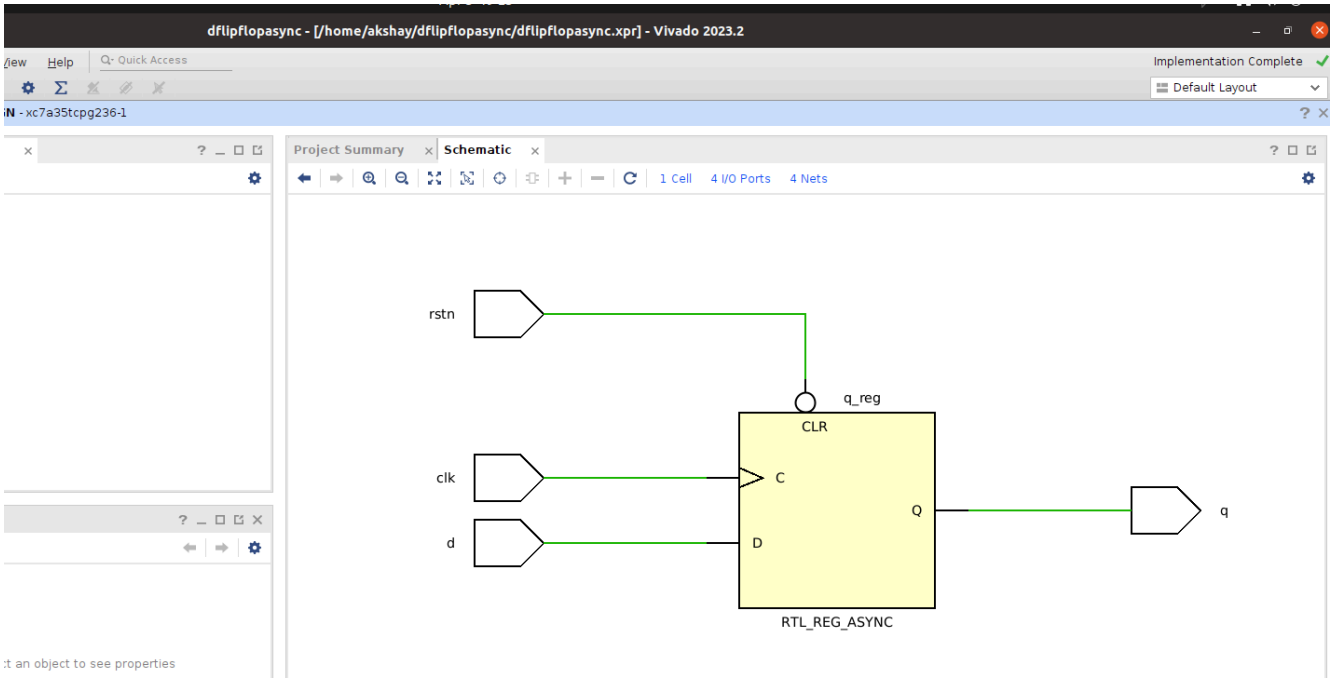
(i) Asynchronous Dff

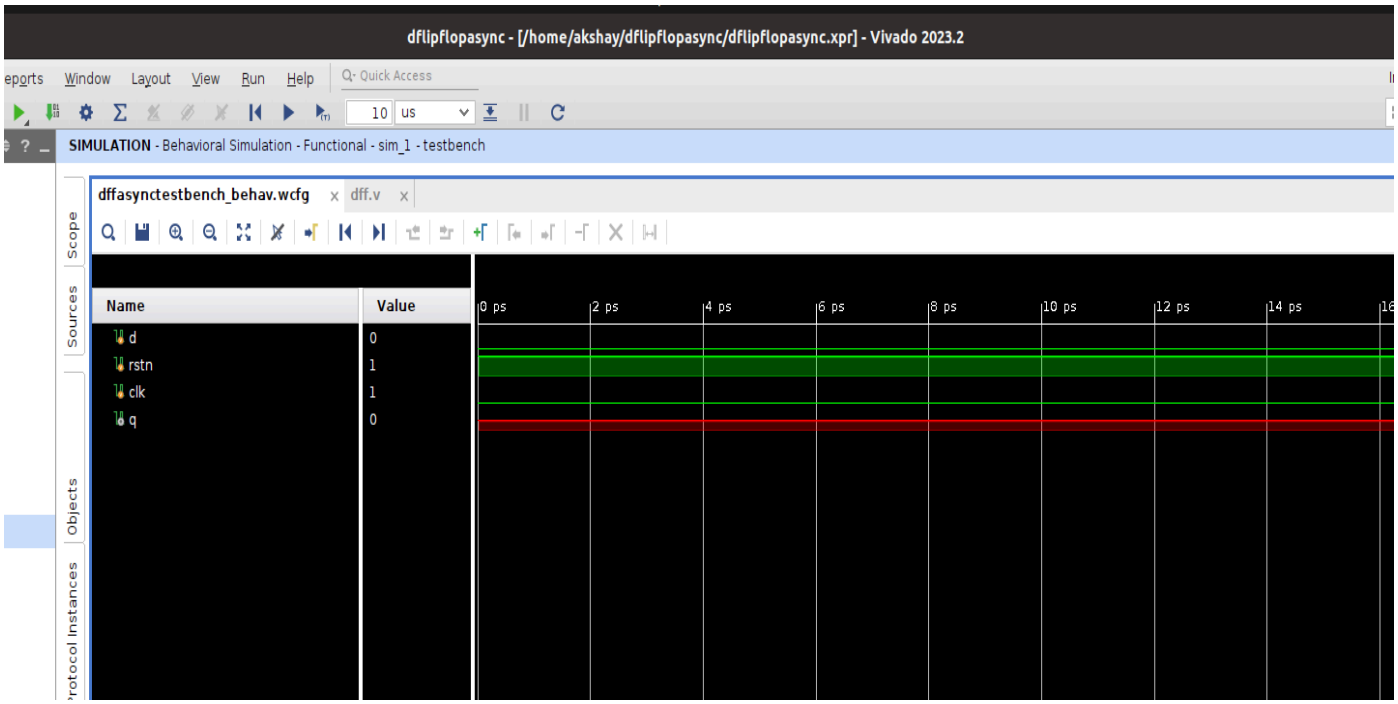
```
module dff ( input d,
input rstn,
input clk,
output reg q);
always @ (posedge clk or negedge rstn)
if (!rstn)
q <= 0;
else
q <= d;
endmodule
```

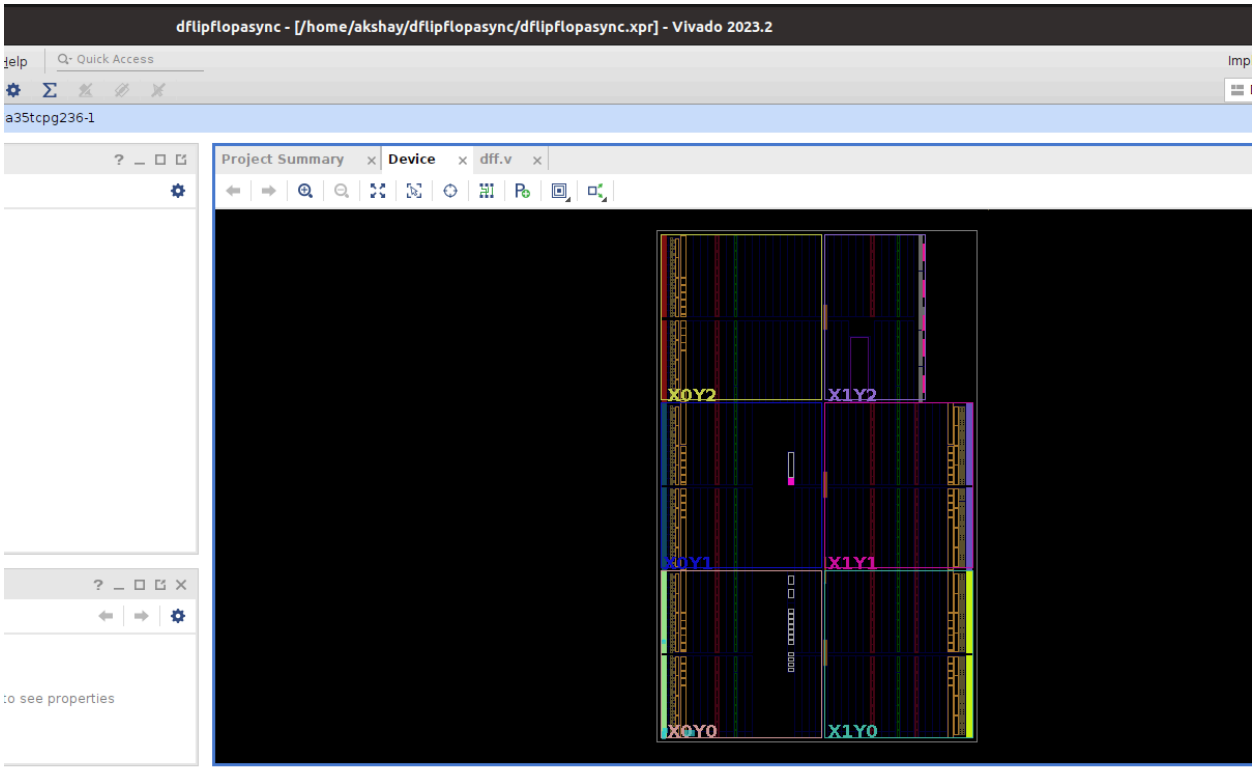
Testbench

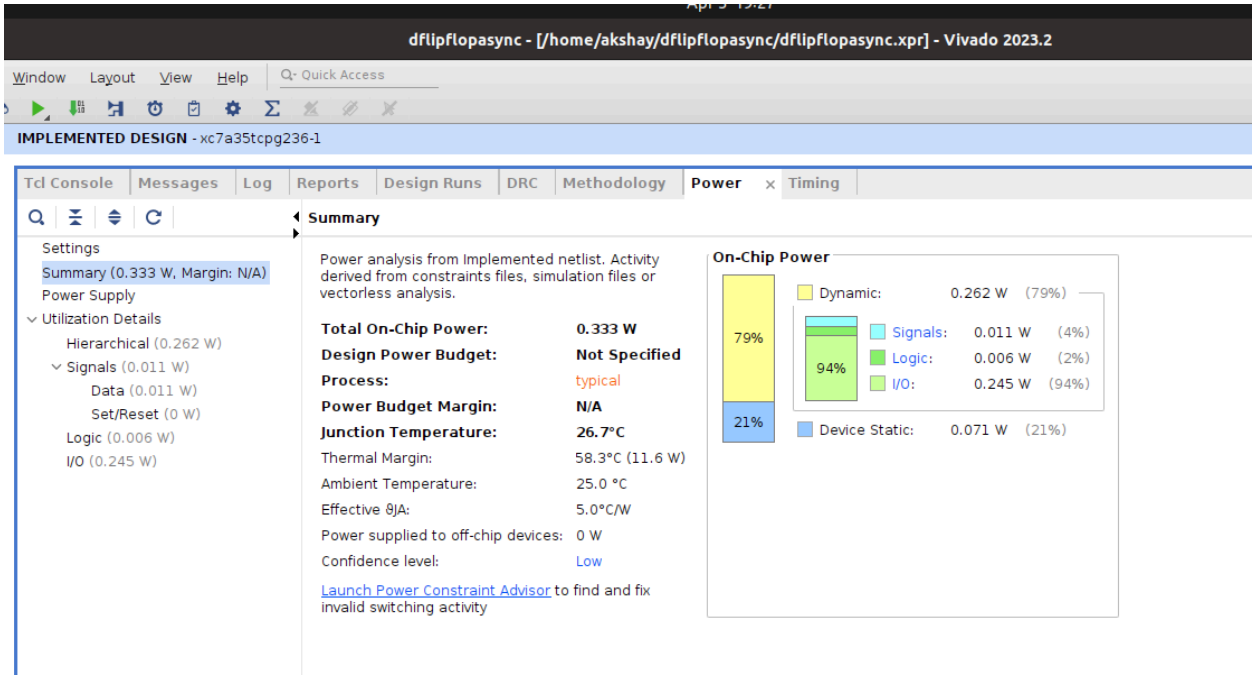
```
module testbench;
    // Inputs
    reg d;
    reg rstn;
    reg clk;
    // Outputs
    wire q;
    // Instantiate the DFF
    dff dut (
        d,
        rstn,
        clk,  q );
```

```
    // Clock generation
    always begin
        #5 clk = ~clk;
    end

    // Initial values
    initial begin
      // Initialize inputs
        d = 0;
        rstn = 1;
        clk = 0;
        // Apply inputs
        #10 d = 1;
        #10 d = 0;
        #10 d = 1;
        #10 d = 0;
        #10 rstn = 0; // Reset
        #10 rstn = 1; // Release reset
        #10 $finish; // End simulation
    end
endmodule
```


dflipflopasync - [/home/akshay/dflipflopasync/dflipflopasync.xpr] - Vivado 2023.2
Implementation Complete
Default Layout
Project Summary
Schematic
1 Cell
4 I/O Ports
4 Nets
rstn
q_reg
CLR
clk
C
Q
q
d
D
RTL_REG_ASYNC


dflipflopasync - [/home/akshay/dflipflopasync/dflipflopasync.xpr] - Vivado 2023.2
SIMULATION - Behavioral Simulation - Functional - sim_1 - testbench
dffasynctestbench_behav.wcfg
dff.v
Name
Value
d
0
rstn
1
clk
1
q
0
0 ps
2 ps
4 ps
6 ps
8 ps
10 ps
12 ps
14 ps


dflipflopasync - [/home/akshay/dflipflopasync/dflipflopasync.xpr] - Vivado 2023.2
Quick Access
a35tcpg236-1
Project Summary
Device
dff.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Design Timing Summary


dflipflopasync - [/home/akshay/dflipflopasync/dflipflopasync.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Summary
Settings
Summary (0.333 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.262 W)
Signals (0.011 W)
Data (0.011 W)
Set/Reset (0 W)
Logic (0.006 W)
I/O (0.245 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.333 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 26.7°C
Thermal Margin: 58.3°C (11.6 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
79%
21%
94%
Dynamic: 0.262 W (79%)
Signals: 0.011 W (4%)
Logic: 0.006 W (2%)
I/O: 0.245 W (94%)
Device Static: 0.071 W (21%)

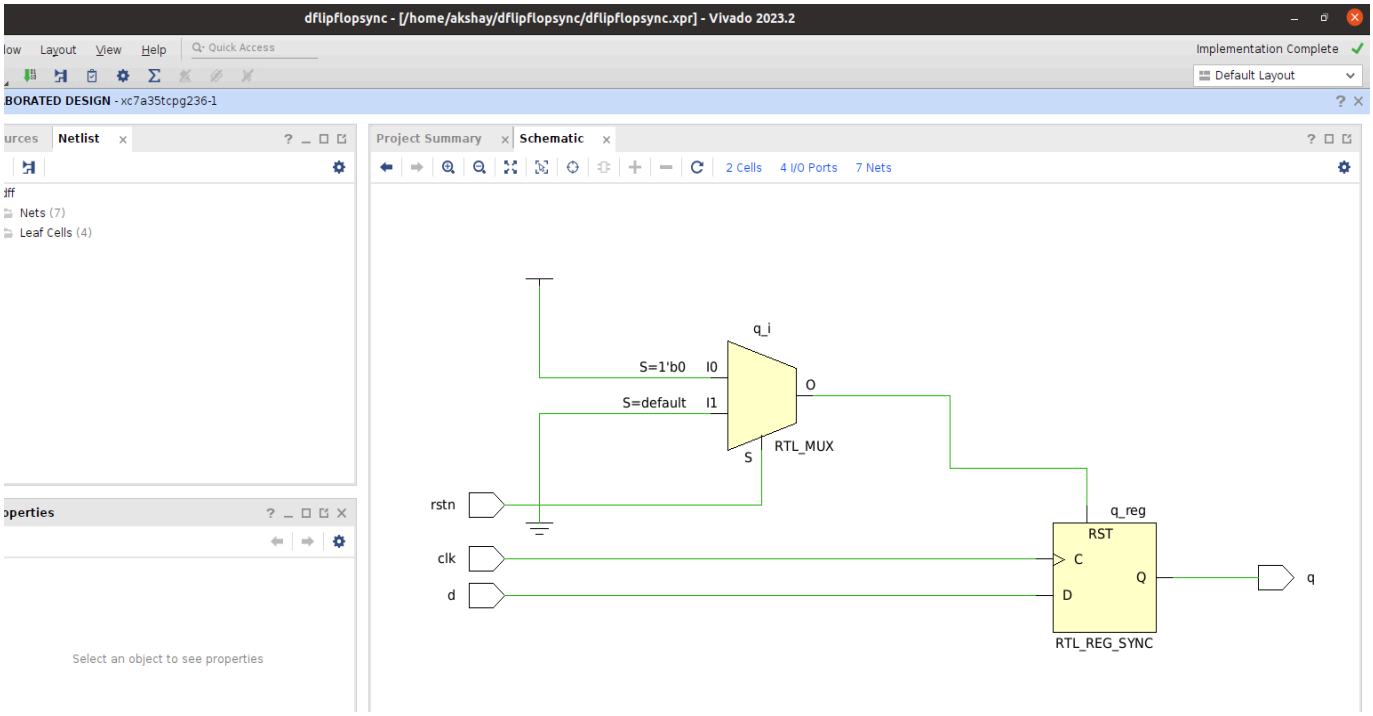
(i) Synchronous Dff

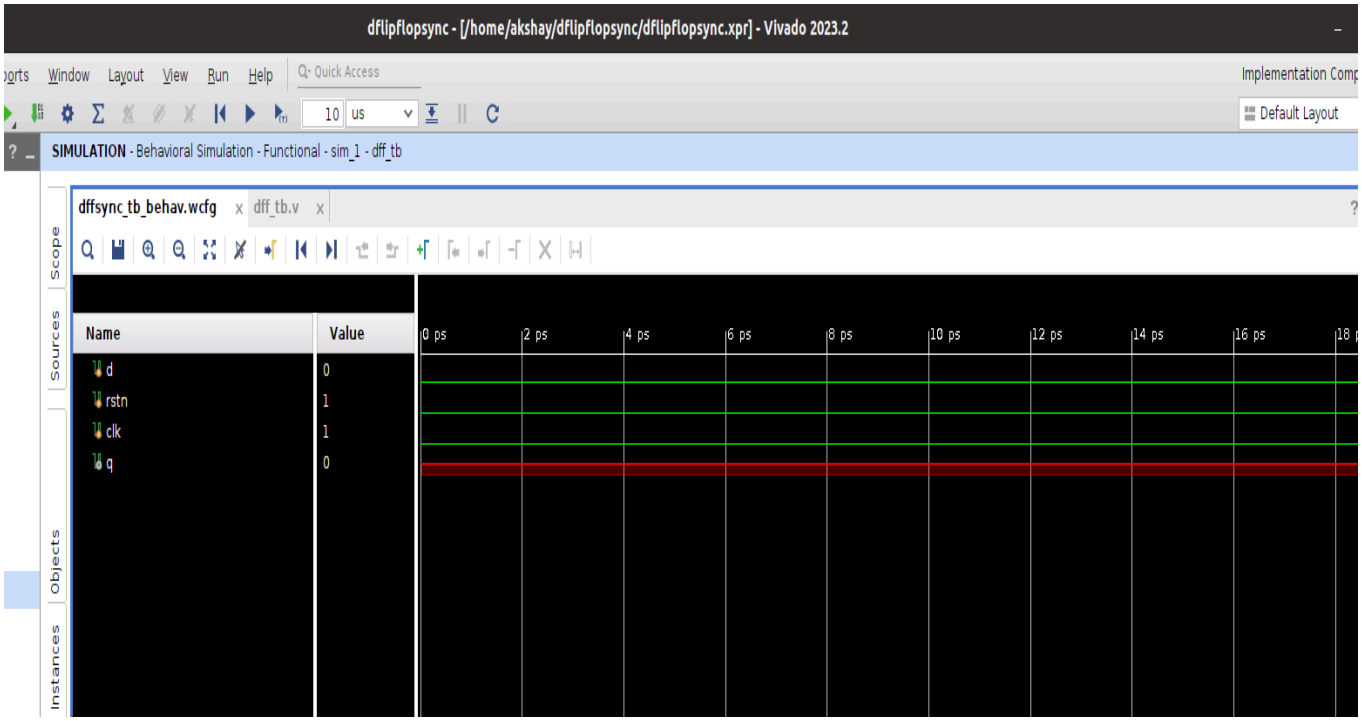
```
module dff ( input d,
input rstn,
input clk,
output reg q);
always @ (posedge clk)
if (!rstn)
q <= 0;
else
q <= d;
endmodule
```

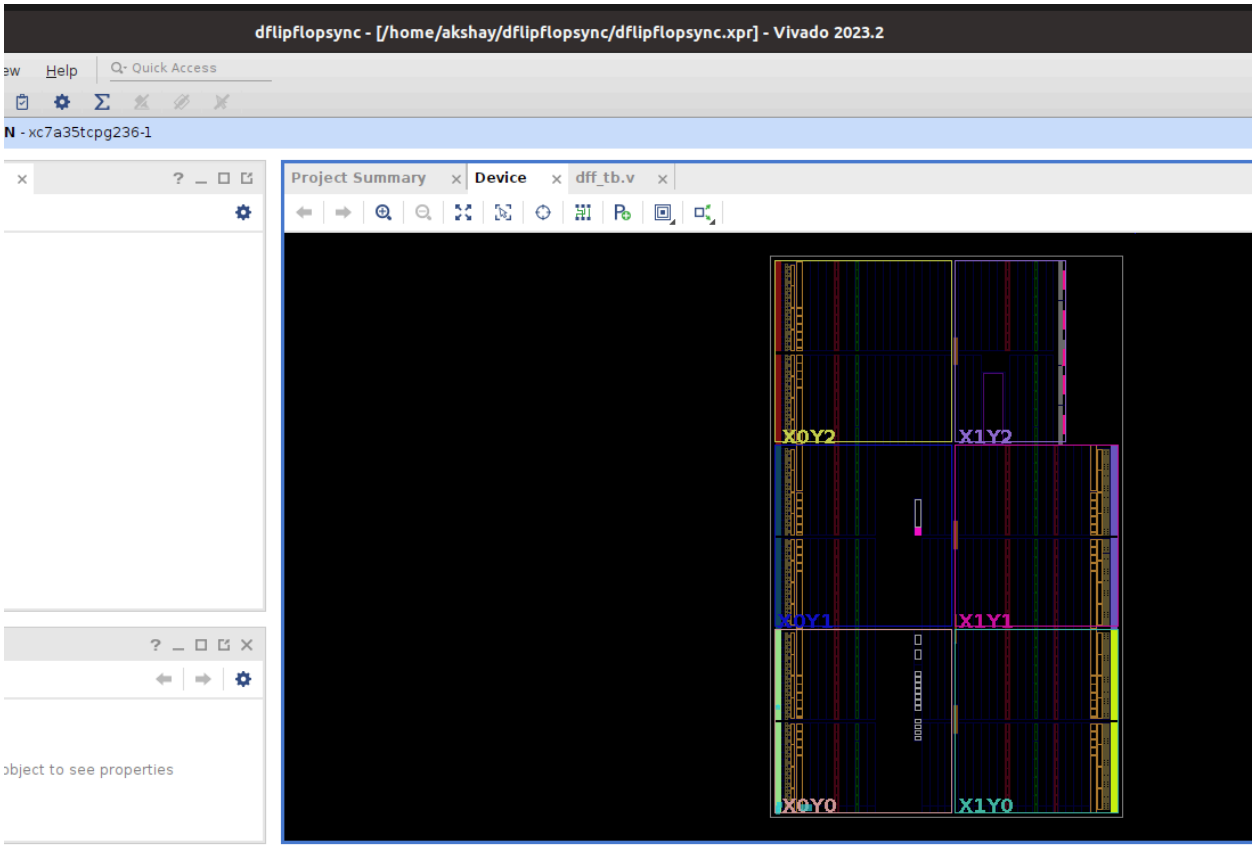
Testbench

```
module dff_tb;
  // Inputs
  reg d;
  reg rstn;
  reg clk;
  // Outputs
  wire q;
  // Instantiate the dff module
  dff dut(
    d,
    rstn,
    clk,
    q  );
```

```
  // Clock generation
  always begin
    #5 clk = ~clk; // Toggle the clock every 5 time units
  end

// Stimulus
  initial begin
    // Initialize inputs
    d = 0;
    rstn = 0;
    clk = 0;

    // Reset and then apply data input
    #10 rstn = 1;
    #5 d = 1;
    #5 d = 0;
    #5 d = 1;
    #5 d = 0;
    // Add more test cases as needed
    // Finish simulation
    #10 $finish;
  End
endmodule
```


dflipflopsync - [/home/akshay/dflipflopsync/dflipflopsync.xpr] - Vivado 2023.2
Implementation Complete
Default Layout
Netlist
Project Summary
Schematic
2 Cells
4 I/O Ports
7 Nets
Nets (7)
Leaf Cells (4)
Select an object to see properties
q_i
S=1'b0
I0
S=default
I1
O
S
RTL_MUX
rstn
clk
d
q_reg
RST
C
D
Q
q
RTL_REG_SYNC


dflipflopsync - [/home/akshay/dflipflopsync/dflipflopsync.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - dff_tb
dffsync_tb_behav.wcfg
dff_tb.v
Scope
Sources
Objects
Instances
Name
Value
d
0
rstn
1
clk
1
q
0
0 ps
2 ps
4 ps
6 ps
8 ps
10 ps
12 ps
14 ps
16 ps


dflipflopsync - [/home/akshay/dflipflopsync/dflipflopsync.xpr] - Vivado 2023.2
Help
Quick Access
N - xc7a35tcpg236-1
Project Summary
Device
dff_tb.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
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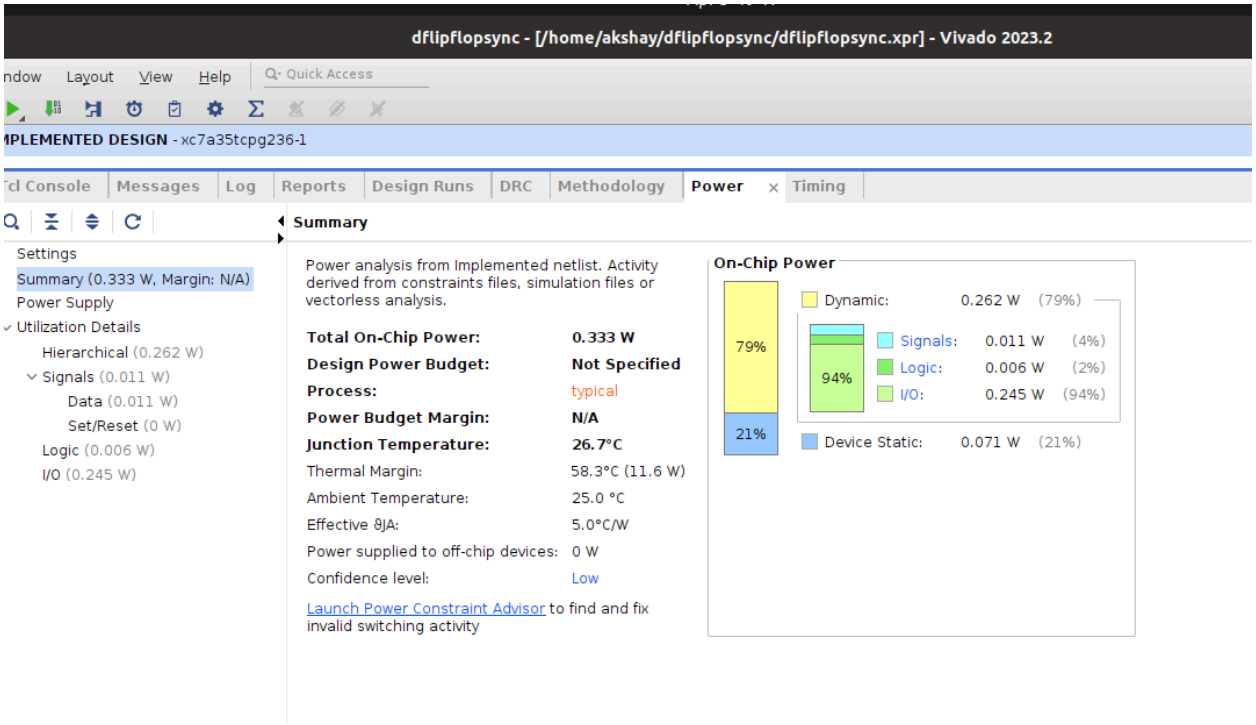
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Design Timing Summary


dflipflopsync - [/home/akshay/dflipflopsync/dflipflopsync.xpr] - Vivado 2023.2
ndow
Layout
View
Help
Quick Access
MPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Summary
Settings
Summary (0.333 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.262 W)
Signals (0.011 W)
Data (0.011 W)
Set/Reset (0 W)
Logic (0.006 W)
I/O (0.245 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.333 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 26.7°C
Thermal Margin: 58.3°C (11.6 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
79%
21%
94%
Dynamic: 0.262 W (79%)
Signals: 0.011 W (4%)
Logic: 0.006 W (2%)
I/O: 0.245 W (94%)
Device Static: 0.071 W (21%)

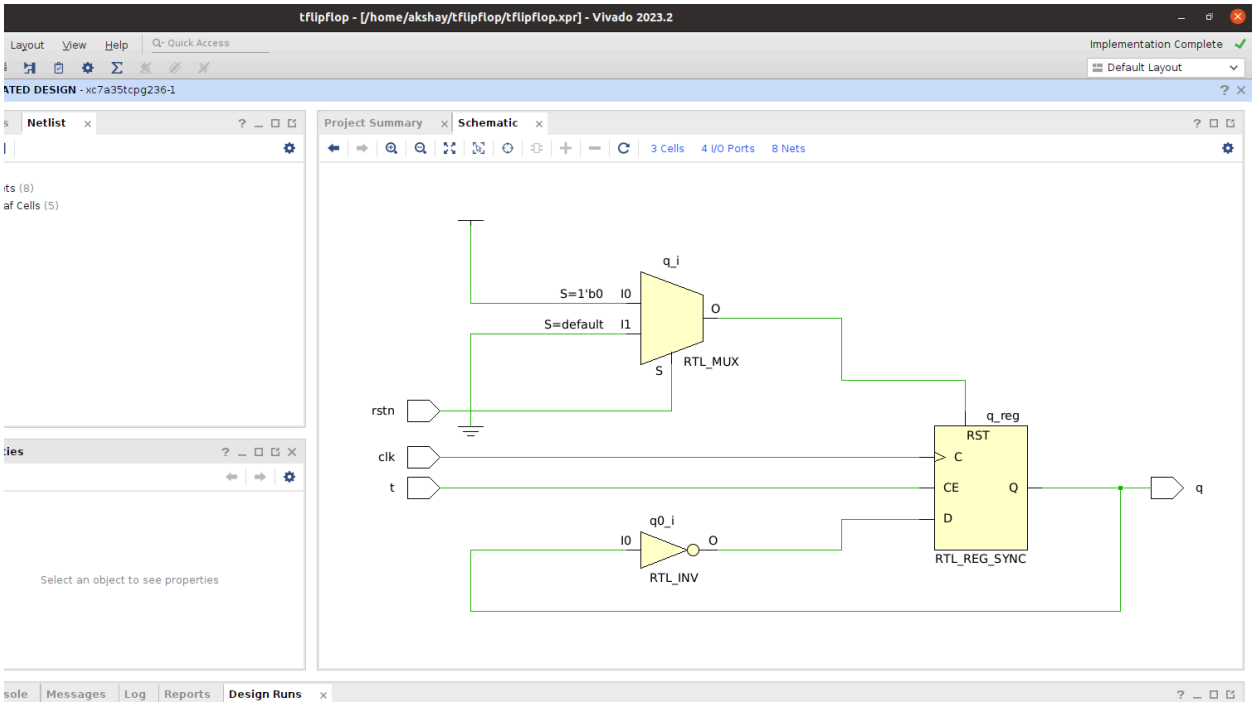
d. T Flipflop :

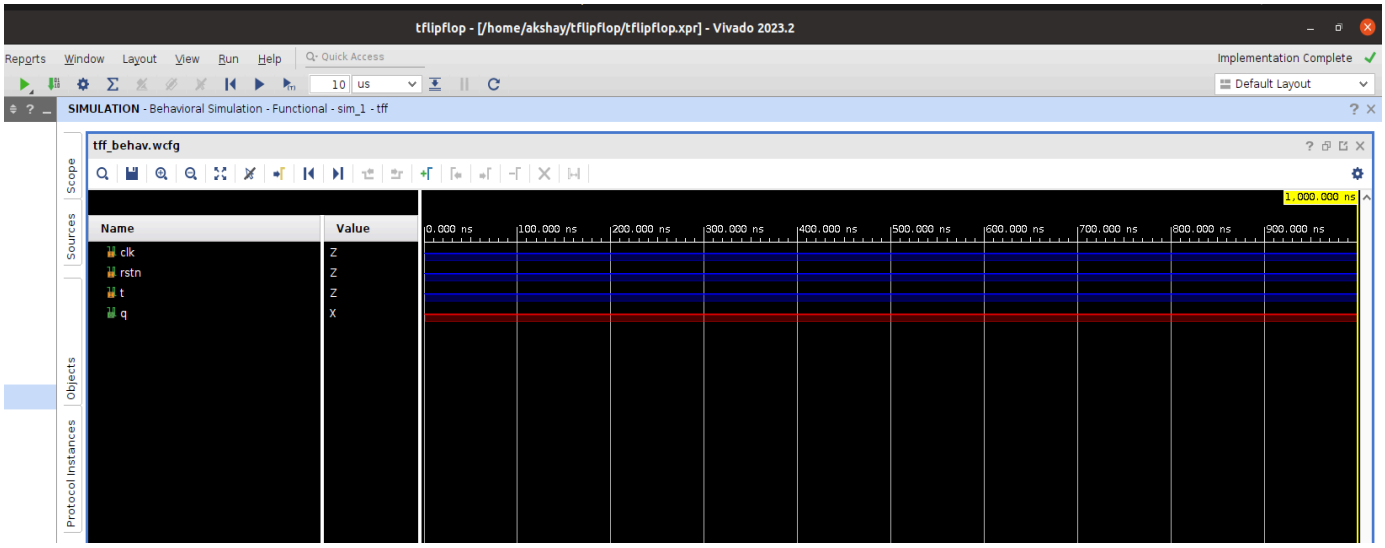
```
module tff (
input clk,
input rstn,
input t,
output reg q);
always @ (posedge clk) begin
if (!rstn)
q <= 0;
else
if (t)
q <= ~q;
else
q <= q;
end
endmodule
```

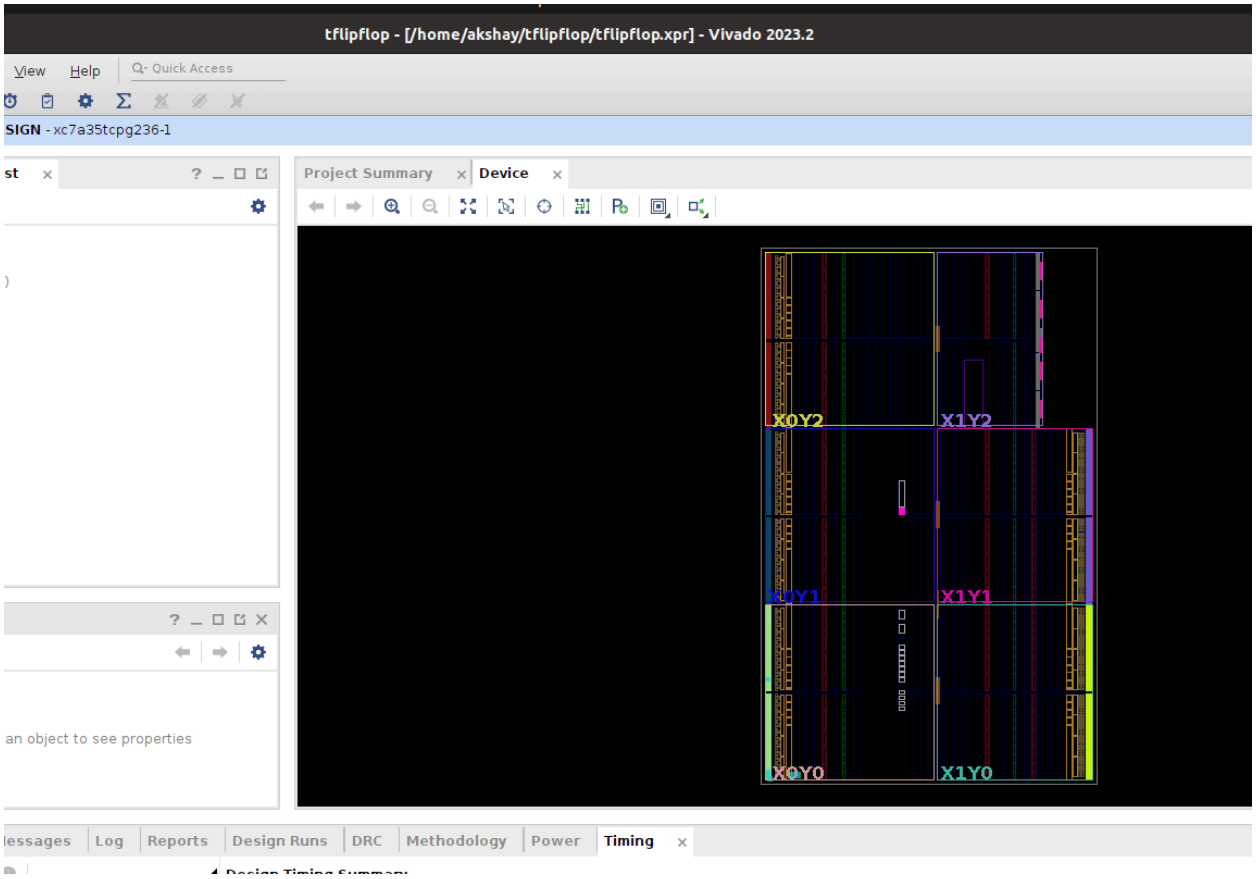
Testbench

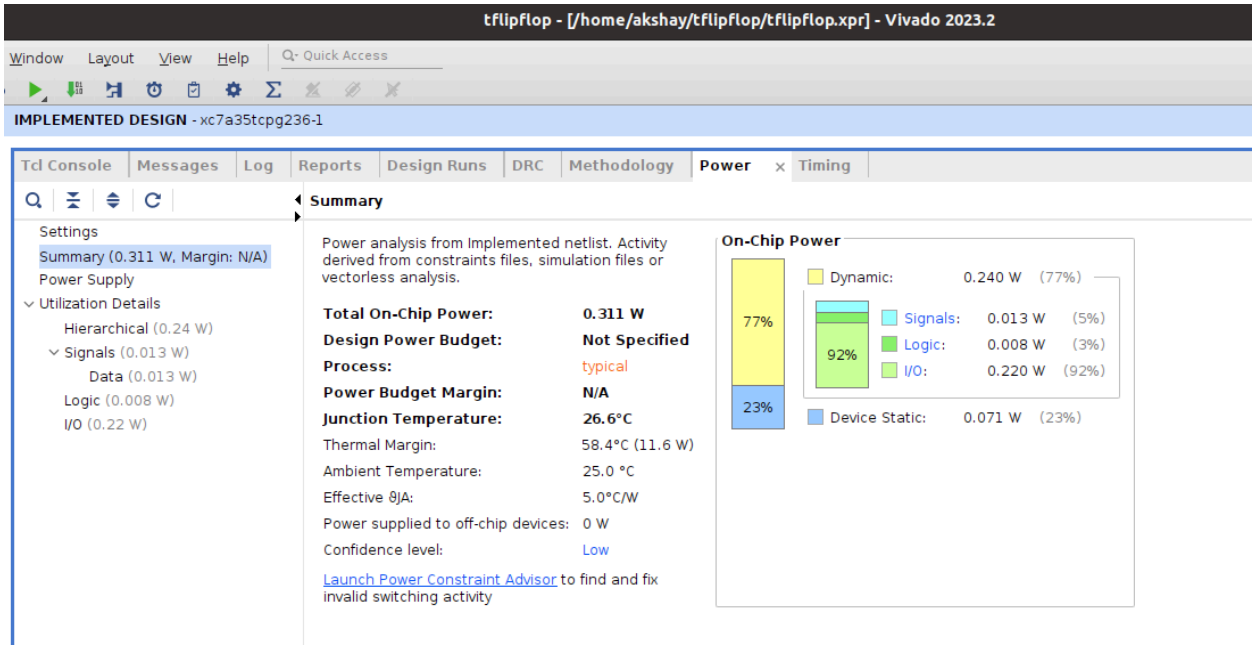
```
module tff (

input clk,
input rstn,
input t,
output reg q);
```

```
always @ (posedge clk) begin
if (!rstn)
q <= 0;
else
if (t)
q <= ~q;
else

q <= q;

end
endmodule
```


tflipflop - [/home/akshay/tflipflop/tflipflop.xpr] - Vivado 2023.2
Layout
View
Help
Quick Access
Implementation Complete
Default Layout
Netlist
Project Summary
Schematic
3 Cells
4 I/O Ports
8 Nets
q_i
S=1'b0
I0
S=default
I1
O
S
RTL_MUX
rstn
clk
t
q_reg
RST
C
CE
Q
D
q
q0_i
I0
O
RTL_INV
RTL_REG_SYNC
Select an object to see properties
Messages
Log
Reports
Design Runs


tflipflop - [/home/akshay/tflipflop/tflipflop.xpr] - Vivado 2023.2
Reports
Window
Layout
View
Run
Help
Quick Access
Implementation Complete
Default Layout
10
us
SIMULATION - Behavioral Simulation - Functional - sim_1 - tff
tff_behav.wcfg
Scope
Sources
Objects
Protocol Instances
Name
Value
clk
rstn
t
q
Z
Z
Z
X
0.000 ns
100.000 ns
200.000 ns
300.000 ns
400.000 ns
500.000 ns
600.000 ns
700.000 ns
800.000 ns
900.000 ns
1,000.000 ns


tflipflop - [/home/akshay/tflipflop/tflipflop.xpr] - Vivado 2023.2
View
Help
Quick Access
SIGN - xc7a35tcpg236-1
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
an object to see properties
lessages
Log
Reports
Design Runs
DRC
Methodology
Power
Timing


tflipflop - [/home/akshay/tflipflop/tflipflop.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Settings
Summary (0.311 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.24 W)
Signals (0.013 W)
Data (0.013 W)
Logic (0.008 W)
I/O (0.22 W)
Summary
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.311 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 26.6°C
Thermal Margin: 58.4°C (11.6 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
77%
23%
Dynamic: 0.240 W (77%)
92%
Signals: 0.013 W (5%)
Logic: 0.008 W (3%)
I/O: 0.220 W (92%)
Device Static: 0.071 W (23%)

Assignment-7 (sequential circuit)

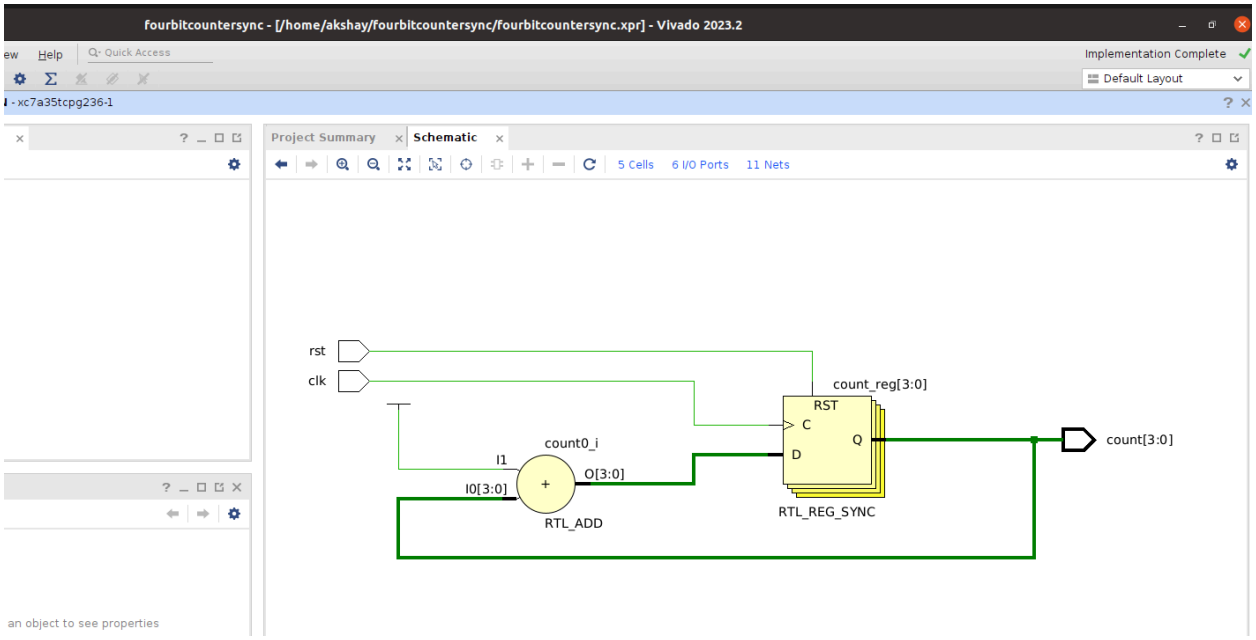
Q.25. Write Verilog code 4-bit UP/DOWN Synchronous Counter:

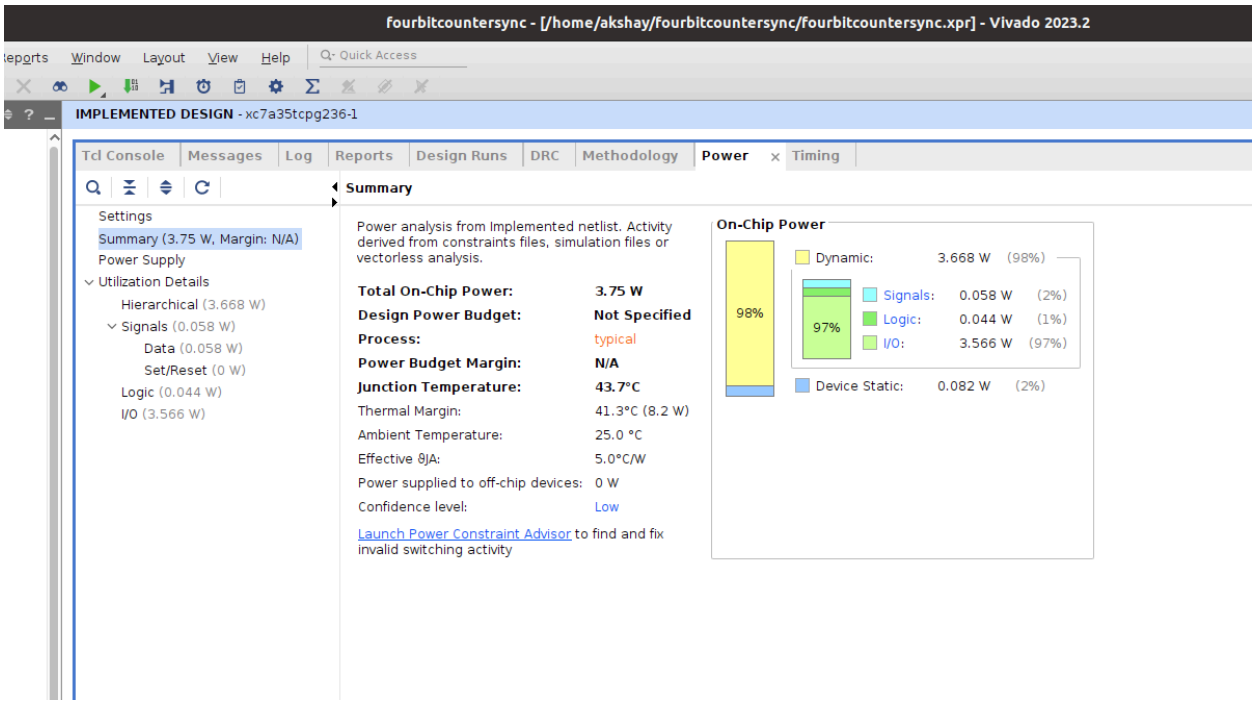
```
module FourBitCounter (
    input wire clk,  // Clock input
    input wire rst,  // Reset input
    output reg [3:0] count  // 4-bit counter output );
    always @(posedge clk) begin
        if (rst) begin
            count <= 4'b0000;  // Reset the counter to 0
        end else begin
            count <= count + 1;  // Increment the counter on each clock cycle
        end
    end
endmodule
```

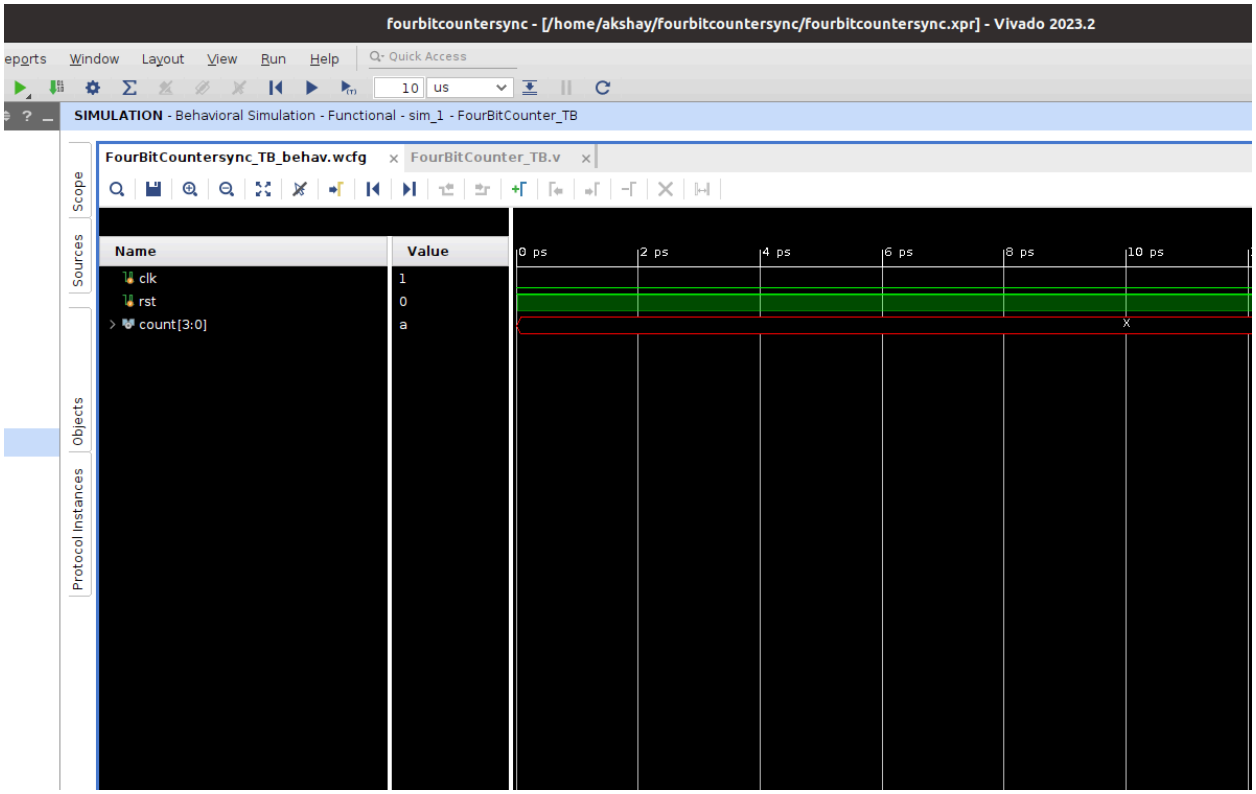
Testbench

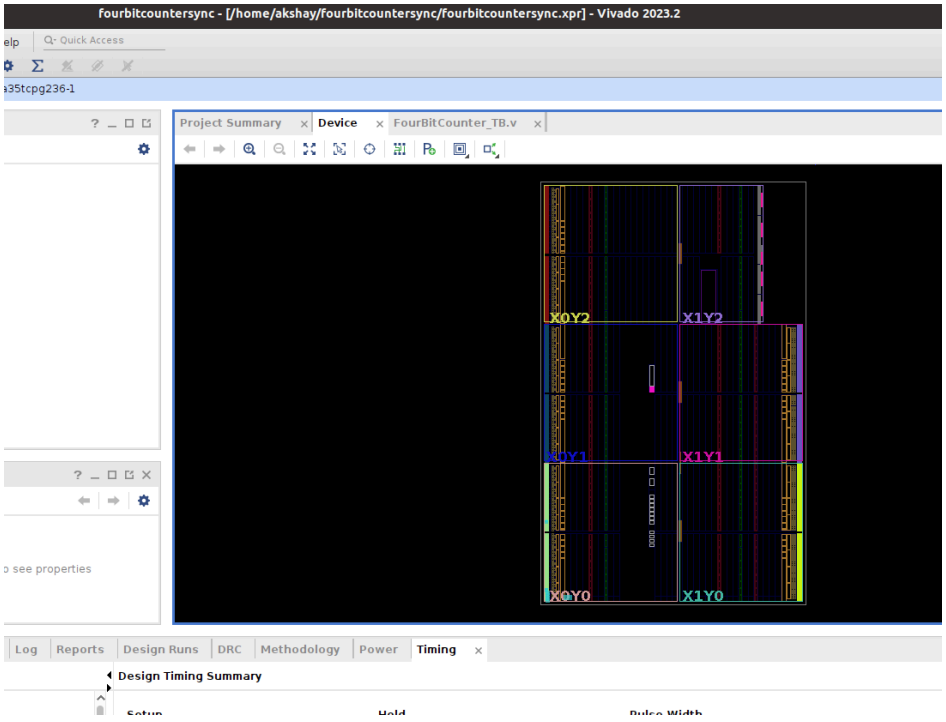
```
module FourBitCounter_TB;

    // Inputs
    reg clk;
    reg rst;

    // Outputs
    wire [3:0] count;

    // Instantiate the 4-bit synchronous counter module
    FourBitCounter dut (
        (clk),
        (rst),
        (count)
    );

    // Clock generation
```

```
always begin
    clk = 0;
    #5;  // Delay for half a clock cycle
    clk = 1;
    #5;  // Delay for half a clock cycle
end

// Reset generation
initial begin
    rst = 1;
    #10;  // Reset for a few clock cycles
    rst = 0;
    #100; // Wait for some cycles after releasing reset
    $finish; // End simulation
end

endmodule
```


fourbitcountersync - [/home/akshay/fourbitcountersync/fourbitcountersync.xpr] - Vivado 2023.2
Implementation Complete
Default Layout
Project Summary
Schematic
5 Cells
6 I/O Ports
11 Nets
rst
clk
count_reg[3:0]
RST
C
D
Q
count[3:0]
count0_i
I1
I0[3:0]
O[3:0]
RTL_ADD
RTL_REG_SYNC
an object to see properties


fourbitcountersync - [/home/akshay/fourbitcountersync/fourbitcountersync.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Summary
Settings
Summary (3.75 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (3.668 W)
Signals (0.058 W)
Data (0.058 W)
Set/Reset (0 W)
Logic (0.044 W)
I/O (3.566 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 3.75 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 43.7°C
Thermal Margin: 41.3°C (8.2 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
98%
97%
Dynamic: 3.668 W (98%)
Signals: 0.058 W (2%)
Logic: 0.044 W (1%)
I/O: 3.566 W (97%)
Device Static: 0.082 W (2%)


fourbitcountersync - [/home/akshay/fourbitcountersync/fourbitcountersync.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
10
us
SIMULATION - Behavioral Simulation - Functional - sim_1 - FourBitCounter_TB
FourBitCountersync_TB_behav.wcfg
FourBitCounter_TB.v
Scope
Sources
Objects
Protocol Instances
Name
Value
clk
1
rst
0
count[3:0]
a
0 ps
2 ps
4 ps
6 ps
8 ps
10 ps
x

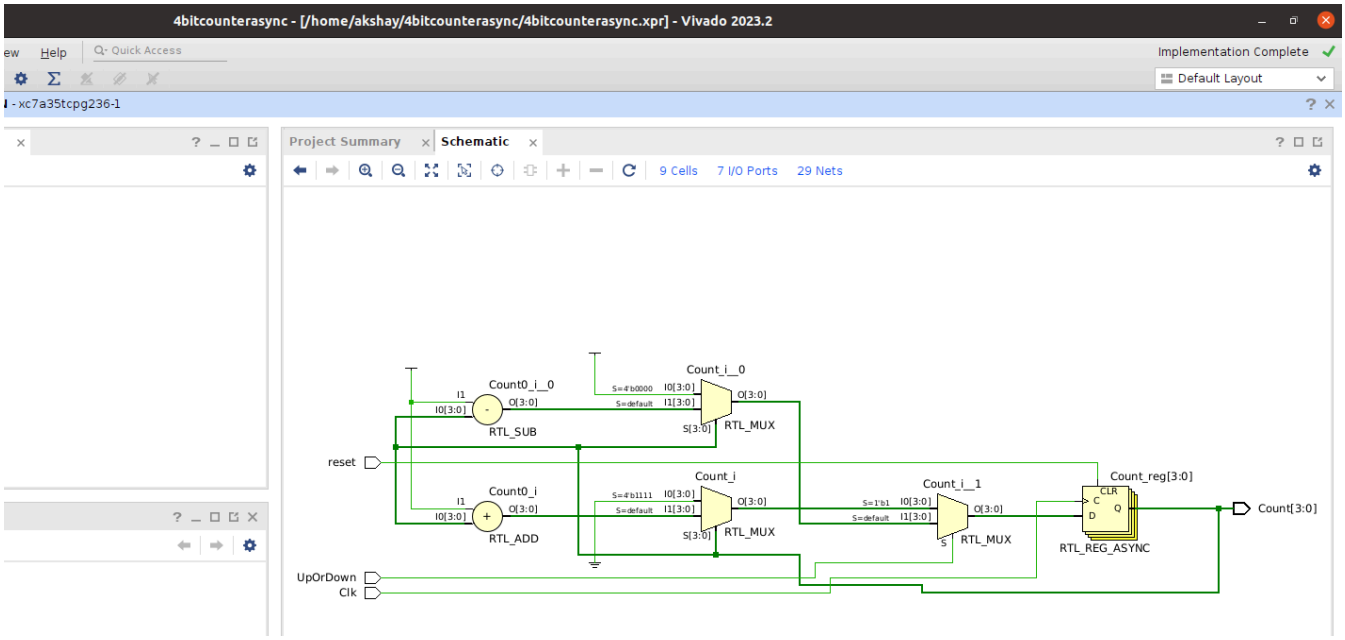

fourbitcountersync - [/home/akshay/fourbitcountersync/fourbitcountersync.xpr] - Vivado 2023.2
Quick Access
Project Summary
Device
FourBitCounter_TB.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Design Timing Summary

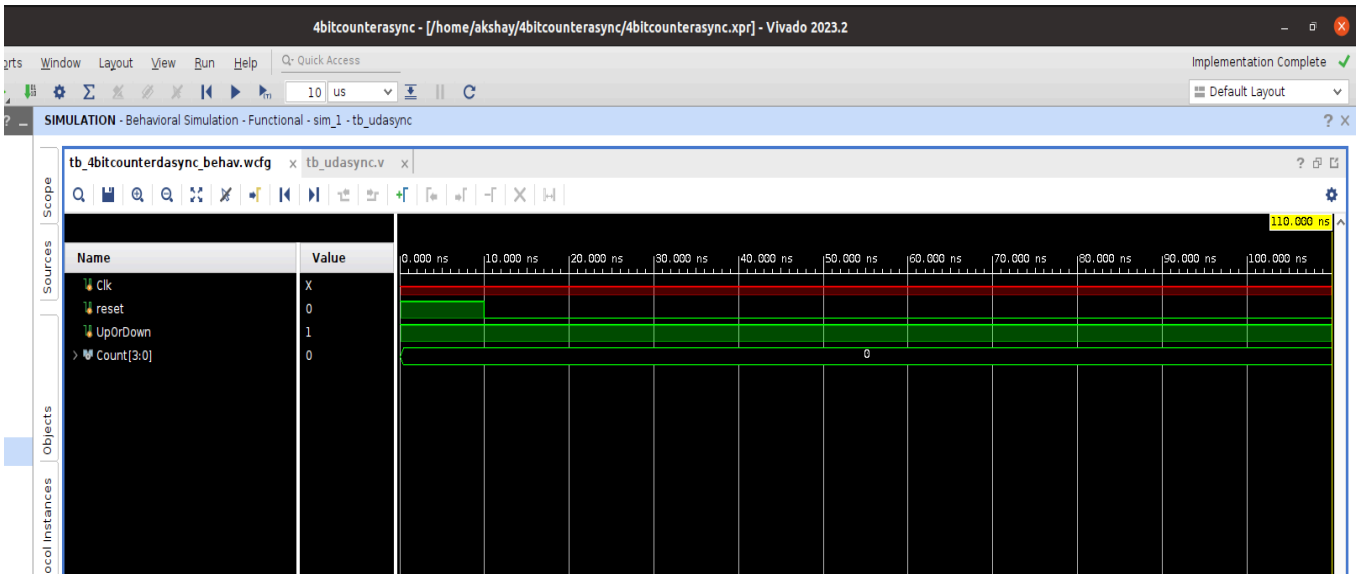
Q.26. Write Verilog code 4-bit UP/DOWN Asynchronous Counter:

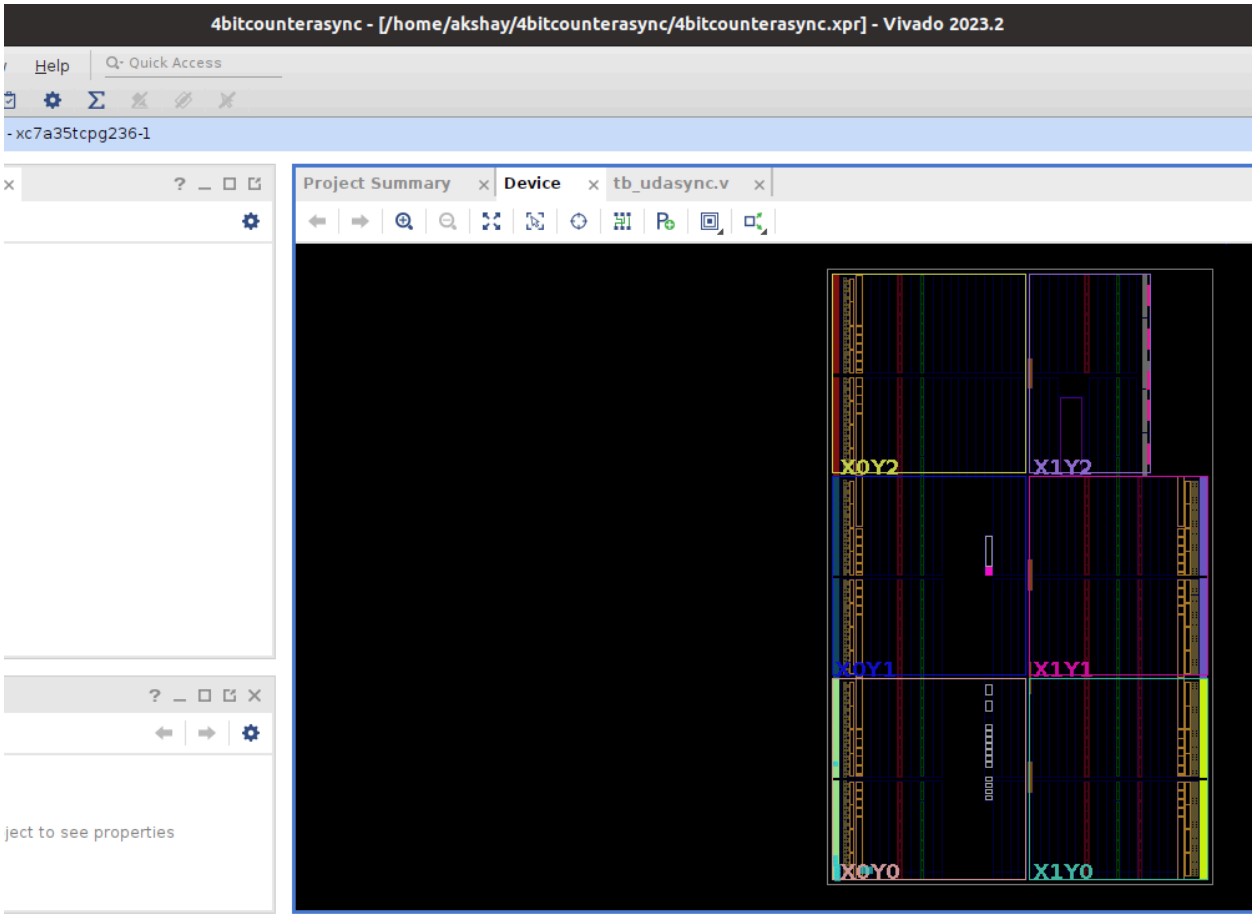
```
module udasync(   Clk,
   reset,
   UpOrDown,  //high for UP counter and low for Down counter
   Count    );
   input Clk,reset,UpOrDown;
   output [3 : 0] Count;
   reg [3 : 0] Count = 0;
    always @(posedge(Clk) or posedge(reset))
    begin
      if(reset == 1)
         Count <= 0;
      else
         if(UpOrDown == 1)   //Up
            if(Count == 15)
               Count <= 0;
            else
               Count <= Count + 1; //Incremend Counter
         else  //Down mode
            if(Count == 0)
               Count <= 15;
            else
               Count <= Count - 1; //Decrement counter
    end
   endmodule
```

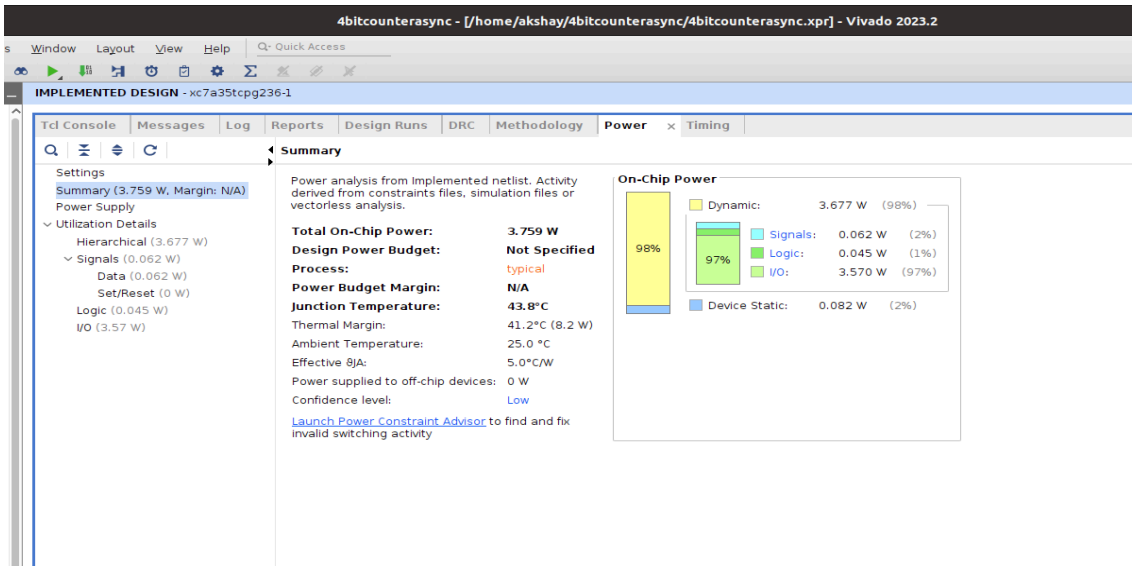
Testbench

```
module tb_udasync;
    reg Clk, reset, UpOrDown;
    wire [3:0] Count;

    // Instantiate the udasync module
    udasync dut (
        (Clk),
        (reset),
        (UpOrDown),
        (Count)
    );

    // Clock generation
    always begin
        #5 Clk = ~Clk;
    end

    // Reset generation
    initial begin
        reset = 1;
        UpOrDown = 1;
        #10 reset = 0;
        #100 $finish;
    end

    // Stimulus generation
    always begin
        #15 UpOrDown = 1; // Up counter mode
        #100 UpOrDown = 0; // Down counter mode
        #100 $finish;
    end

    // Display Count value
    always @(posedge Clk) begin
    end
endmodule
```


4bitcounterasync - [/home/akshay/4bitcounterasync/4bitcounterasync.xpr] - Vivado 2023.2
Help
Quick Access
Implementation Complete
Default Layout
xc7a35tcpg236-1
Project Summary
Schematic
9 Cells
7 I/O Ports
29 Nets
Count0_i__0
RTL_SUB
Count_i__0
RTL_MUX
reset
Count0_i
RTL_ADD
Count_i
RTL_MUX
Count_i__1
RTL_MUX
Count_reg[3:0]
RTL_REG_ASYNC
Count[3:0]
UpOrDown
Clk


4bitcounterasync - [/home/akshay/4bitcounterasync/4bitcounterasync.xpr] - Vivado 2023.2
Window
Layout
View
Run
Help
Quick Access
Implementation Complete
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_udasync
tb_4bitcounterdasync_behav.wcfg
tb_udasync.v
Scope
Sources
Objects
Name
Value
Clk
reset
UpOrDown
Count[3:0]
110.000 ns
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
80.000 ns
90.000 ns
100.000 ns


4bitcounterasync - [/home/akshay/4bitcounterasync/4bitcounterasync.xpr] - Vivado 2023.2
Help
Quick Access
- xc7a35tcpg236-1
Project Summary
Device
tb_udasync.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
ject to see properties
ges
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Design Timing Summary


4bitcounterasync - [/home/akshay/4bitcounterasync/4bitcounterasync.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Summary
Settings
Summary (3.759 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (3.677 W)
Signals (0.062 W)
Data (0.062 W)
Set/Reset (0 W)
Logic (0.045 W)
I/O (3.57 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 3.759 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 43.8°C
Thermal Margin: 41.2°C (8.2 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
98%
97%
Dynamic: 3.677 W (98%)
Signals: 0.062 W (2%)
Logic: 0.045 W (1%)
I/O: 3.570 W (97%)
Device Static: 0.082 W (2%)

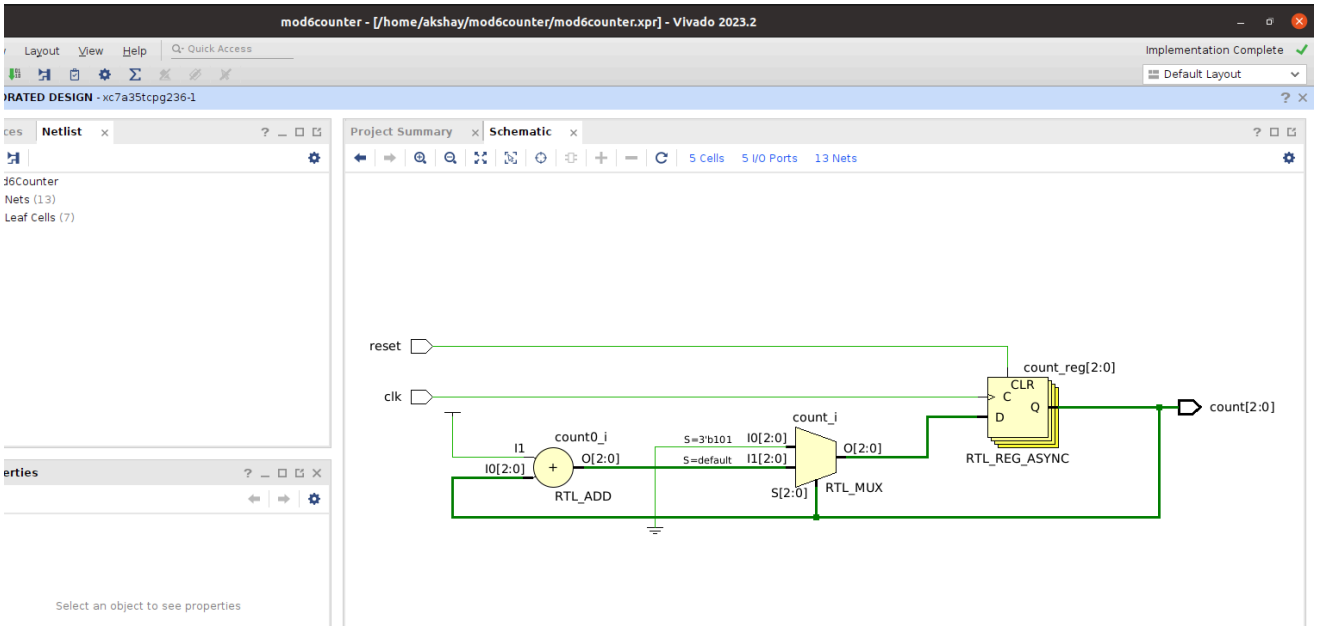
Q.27. Write Verilog code MOD-6 Counter:

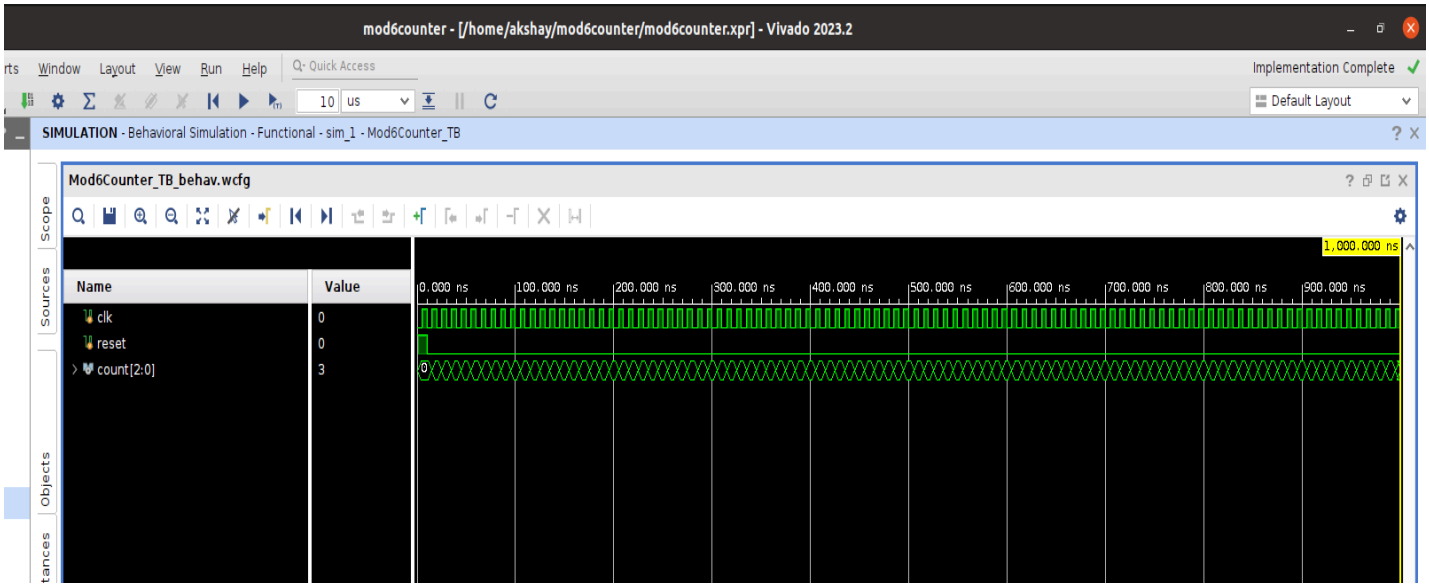
```
module Mod6Counter (
    input wire clk,
    input wire reset,
    output reg [2:0] count );
always @(posedge clk or posedge reset) begin
    if (reset) begin
        count <= 3'b000; // Reset to 0
    end else begin
        if (count == 3'b101) begin // Check if count is 5
            count <= 3'b000; // Reset to 0
        end else begin
            count <= count + 1; // Increment count
        end
    end
end
endmodule
```

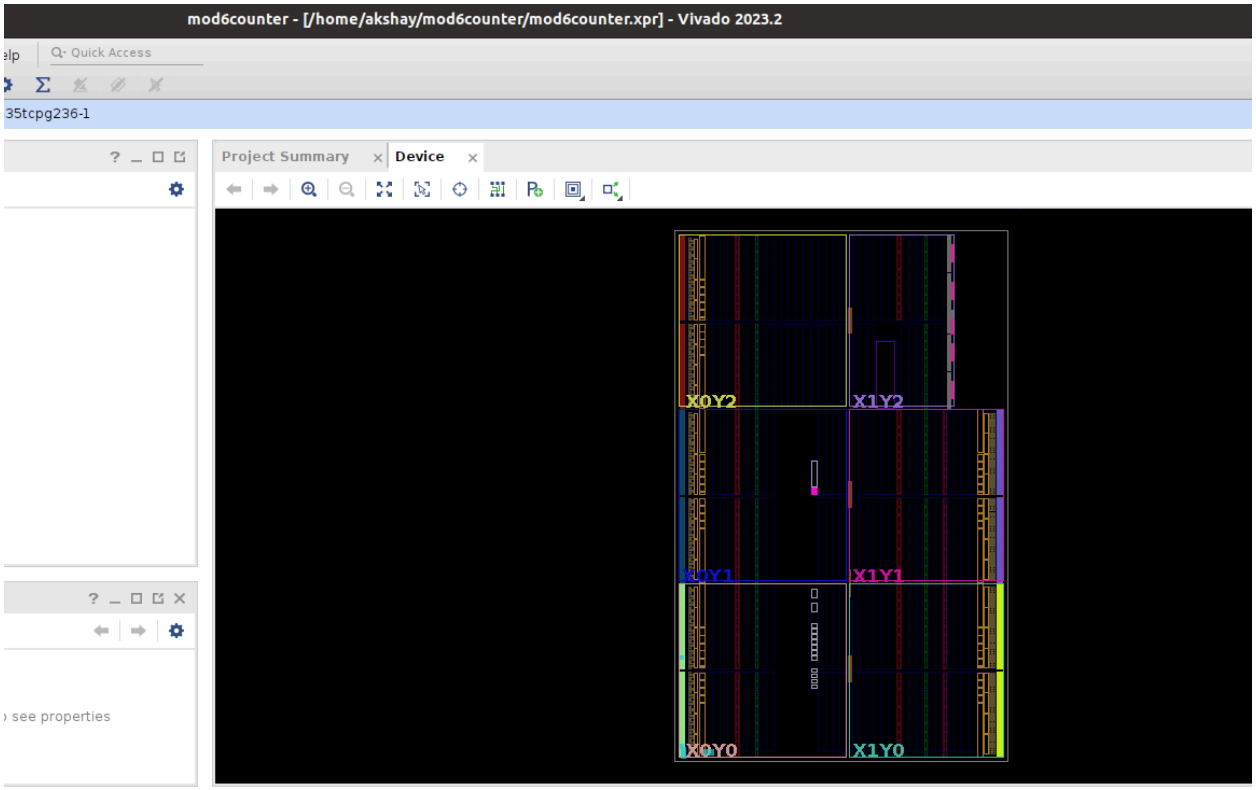
Testbench

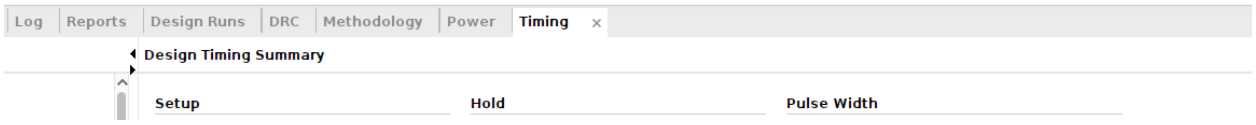
```
module Mod6Counter_TB;

    // Inputs
    reg clk;
    reg reset;

    // Outputs
    wire [2:0] count;

    // Instantiate the module
    Mod6Counter dut(
        (clk),
```

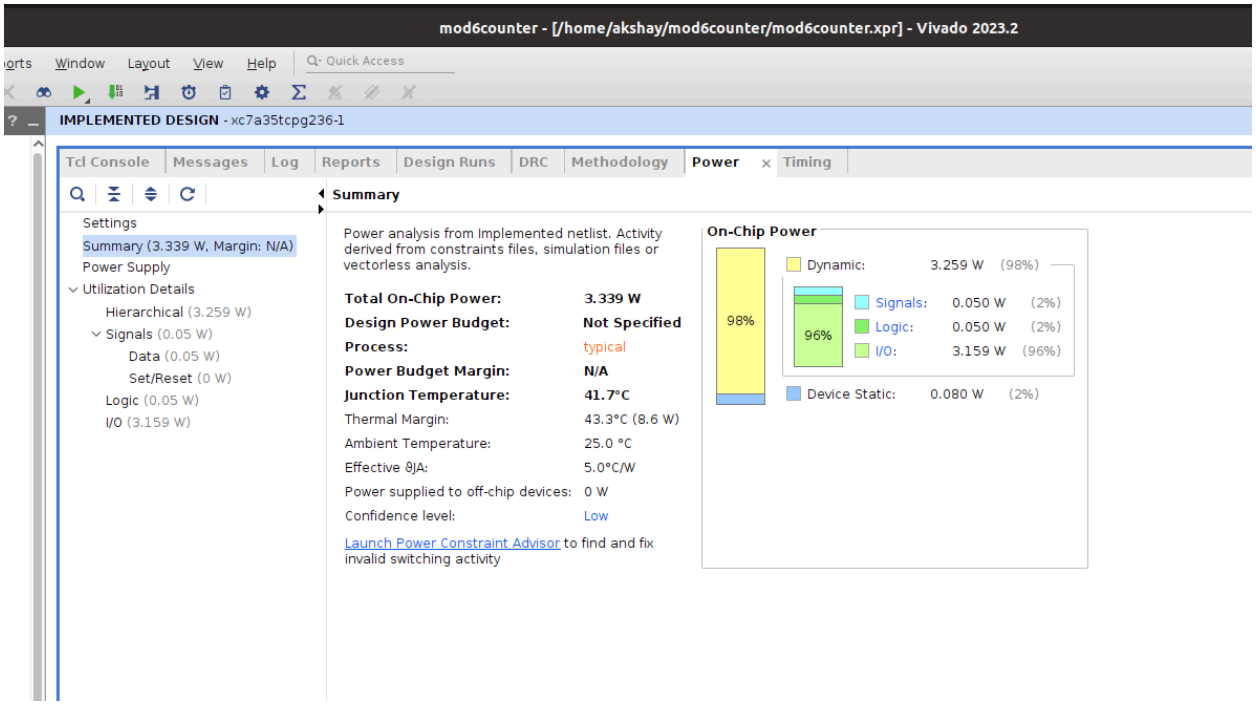
```
        (reset),
        (count)
    );

    // Clock generation
    always #5 clk = ~clk; // Toggle clock every 5 time units

    // Initial block
    initial begin
        clk = 0;
        reset = 1; // Reset active initially
        #10 reset = 0; // Deassert reset after 10 time units

        // Wait for some time
        #15;

        // Check counter values
        if (count !== 3'b000) begin
        end

        // Count for 18 clock cycles
        repeat (18) begin
            #5; // Wait for one clock cycle
        end

        // Check final counter value
        if (count !== 3'b110) begin
        end

    end

endmodule
```


mod6counter - [/home/akshay/mod6counter/mod6counter.xpr] - Vivado 2023.2
Layout View Help
Quick Access
Implementation Complete
Default Layout
RATED DESIGN - xc7a35tcpg236-1
Netlist
Nets (13)
Leaf Cells (7)
Project Summary
Schematic
5 Cells
5 I/O Ports
13 Nets
reset
clk
count_reg[2:0]
CLR
C
D
Q
count[2:0]
RTL_REG_ASYNC
count_i
S=3'b101
S=default
I0[2:0]
I1[2:0]
O[2:0]
S[2:0]
RTL_MUX
count0_i
I1
I0[2:0]
O[2:0]
RTL_ADD
Select an object to see properties


mod6counter - [/home/akshay/mod6counter/mod6counter.xpr] - Vivado 2023.2
Window Layout View Run Help
Quick Access
Implementation Complete
Default Layout
10 us
SIMULATION - Behavioral Simulation - Functional - sim_1 - Mod6Counter_TB
Mod6Counter_TB_behav.wcfg
Scope
Sources
Objects
Name
Value
clk
0
reset
0
count[2:0]
3
1,000.000 ns
0.000 ns
100.000 ns
200.000 ns
300.000 ns
400.000 ns
500.000 ns
600.000 ns
700.000 ns
800.000 ns
900.000 ns


mod6counter - [/home/akshay/mod6counter/mod6counter.xpr] - Vivado 2023.2
Quick Access
35tcpg236-1
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
see properties


Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Design Timing Summary
Setup
Hold
Pulse Width


mod6counter - [/home/akshay/mod6counter/mod6counter.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Summary
Settings
Summary (3.339 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (3.259 W)
Signals (0.05 W)
Data (0.05 W)
Set/Reset (0 W)
Logic (0.05 W)
I/O (3.159 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 3.339 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 41.7°C
Thermal Margin: 43.3°C (8.6 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
98%
96%
Dynamic: 3.259 W (98%)
Signals: 0.050 W (2%)
Logic: 0.050 W (2%)
I/O: 3.159 W (96%)
Device Static: 0.080 W (2%)

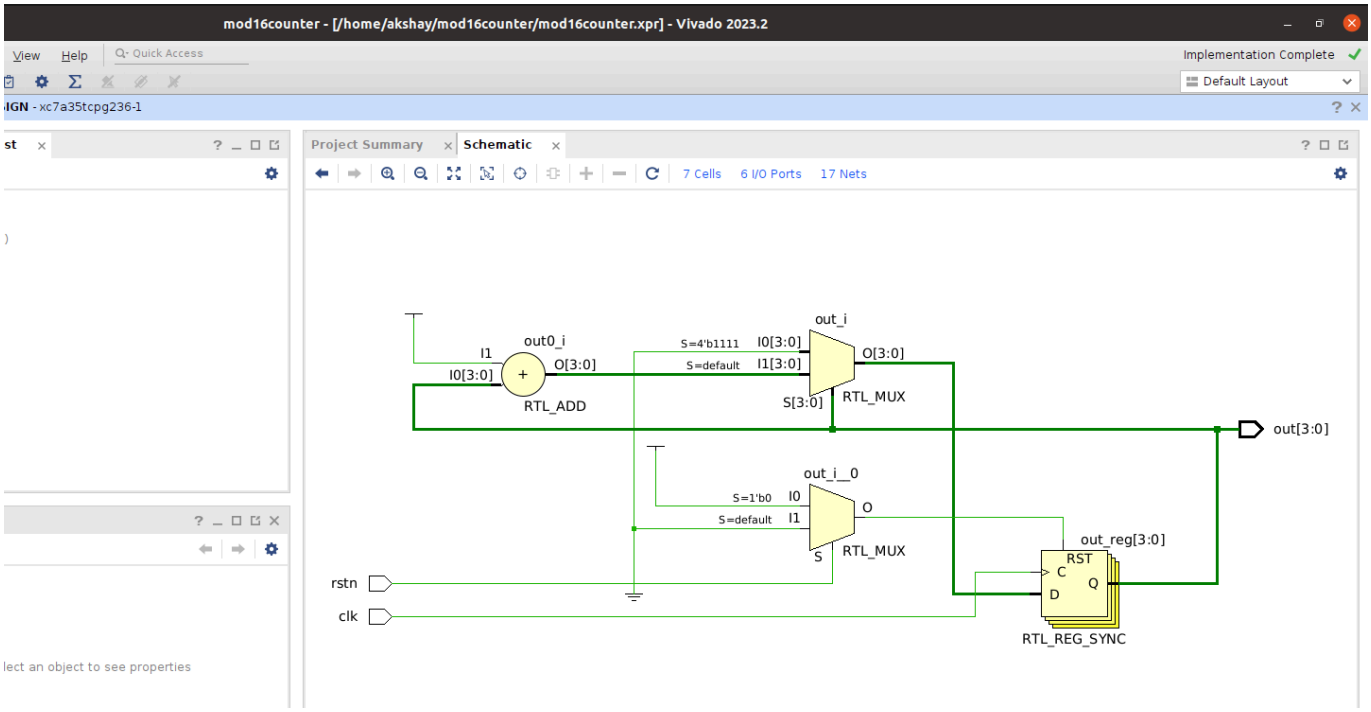
Q.28. Write Verilog code MOD-16 Counter:

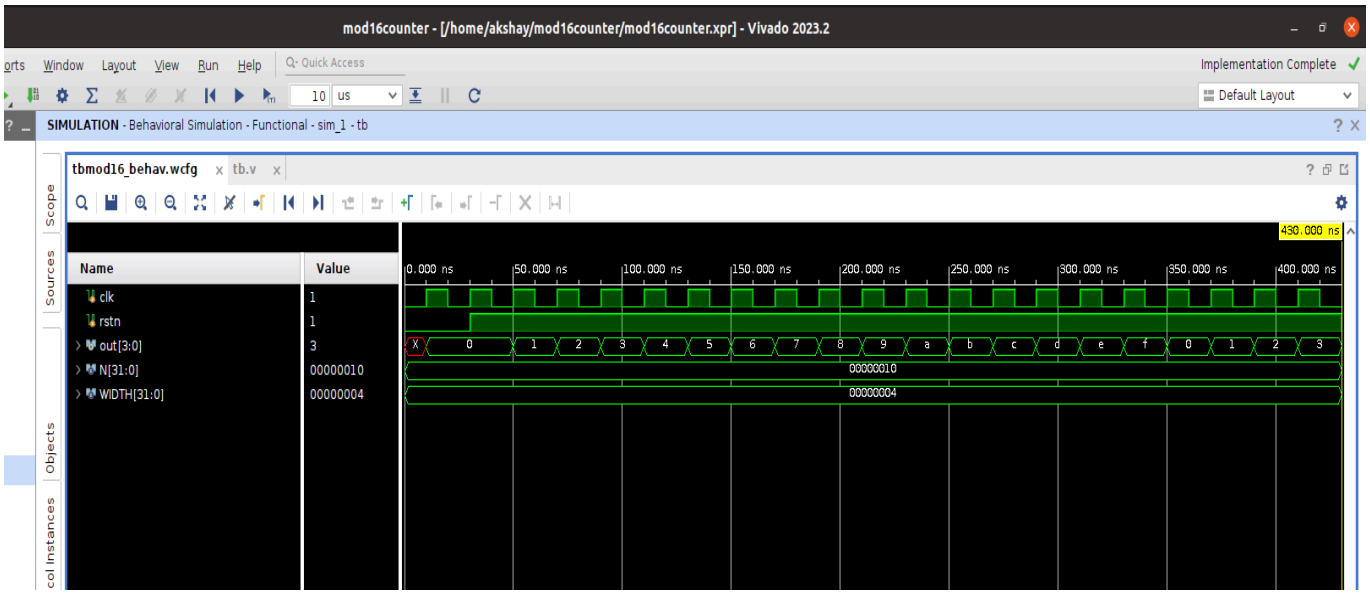
```
module mod16
  # (parameter N = 16,
     parameter WIDTH = 4)
  ( input   clk,
    input   rstn,
    output  reg[WIDTH-1:0] out);
    always @ (posedge clk) begin
    if (!rstn) begin
      out <= 0;
    end else begin
      if (out == N-1)
        out <= 0;
      else
        out <= out + 1;
    end
  end
endmodule
```

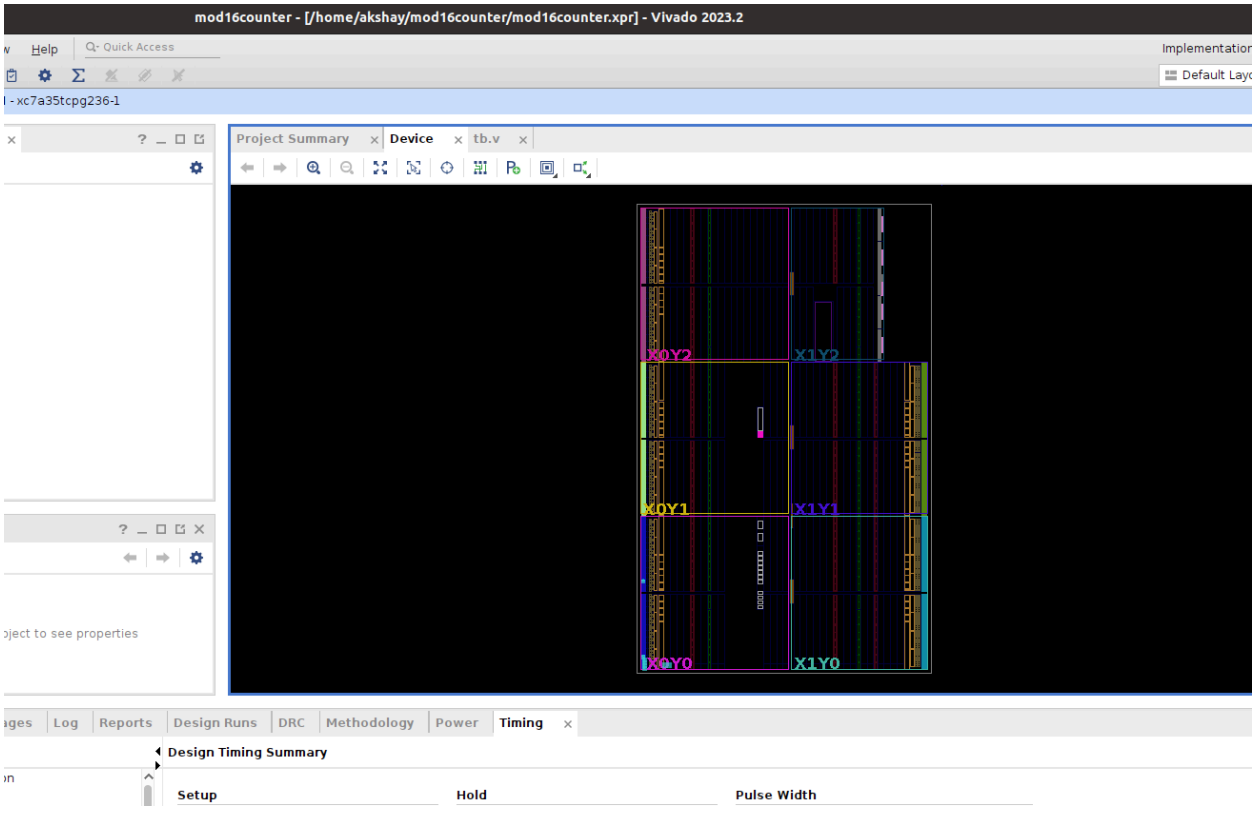
Testbench

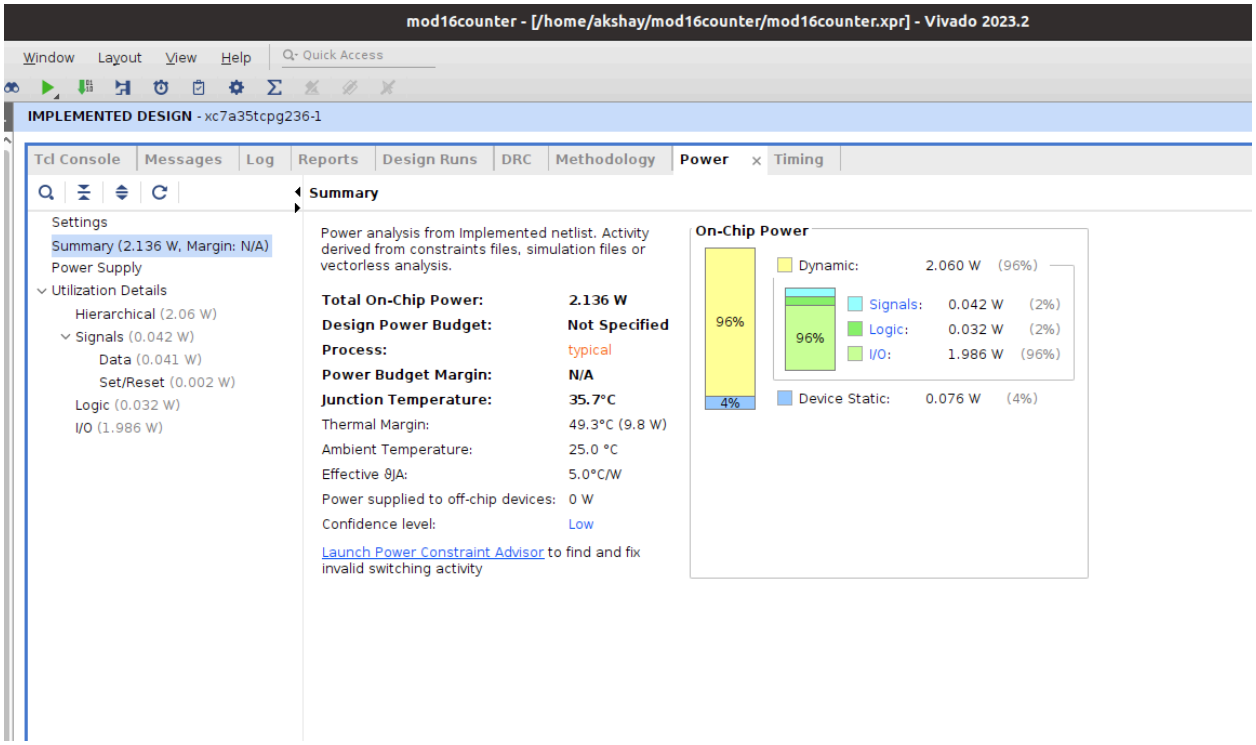
```
module tb(

    );
parameter N = 16;
  parameter WIDTH = 4;

  reg clk;
  reg rstn;
  wire [WIDTH-1:0] out;
```

```
  mod16 u0  (    .clk(clk),
                 .rstn(rstn),
                 .out(out));

  always #10 clk = ~clk;

  initial begin
    {clk, rstn} <= 0;

    $monitor ("T=%0t rstn=%0b out=0x%0h", $time, rstn, out);
    repeat(2) @ (posedge clk);
    rstn <= 1;

    repeat(20) @ (posedge clk);
    $finish;
  end
Endmodule
```


mod16counter - [/home/akshay/mod16counter/mod16counter.xpr] - Vivado 2023.2
View
Help
Quick Access
Implementation Complete
Default Layout
IGN - xc7a35tcpg236-1
Project Summary
Schematic
7 Cells
6 I/O Ports
17 Nets
out0_i
I1
I0[3:0]
O[3:0]
RTL_ADD
out_i
S=4'b1111
I0[3:0]
S=default
I1[3:0]
O[3:0]
S[3:0]
RTL_MUX
out[3:0]
out_i__0
S=1'b0
I0
S=default
I1
O
S
RTL_MUX
out_reg[3:0]
RST
C
D
Q
RTL_REG_SYNC
rstn
clk
lect an object to see properties


mod16counter - [/home/akshay/mod16counter/mod16counter.xpr] - Vivado 2023.2
orts
Window
Layout
View
Run
Help
Quick Access
Implementation Complete
10
us
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb
tbmod16_behav.wcfg
tb.v
Scope
Sources
Objects
col Instances
Name
Value
clk
1
rstn
1
out[3:0]
3
N[31:0]
00000010
WIDTH[31:0]
00000004
430.000 ns
0.000 ns
50.000 ns
100.000 ns
150.000 ns
200.000 ns
250.000 ns
300.000 ns
350.000 ns
400.000 ns
00000010
00000004


mod16counter - [/home/akshay/mod16counter/mod16counter.xpr] - Vivado 2023.2
Help
Quick Access
Implementation
Default Layo
- xc7a35tcpg236-1
Project Summary
Device
tb.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
oject to see properties
ges
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Design Timing Summary
Setup
Hold
Pulse Width


mod16counter - [/home/akshay/mod16counter/mod16counter.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Settings
Summary (2.136 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (2.06 W)
Signals (0.042 W)
Data (0.041 W)
Set/Reset (0.002 W)
Logic (0.032 W)
I/O (1.986 W)
Summary
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 2.136 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 35.7°C
Thermal Margin: 49.3°C (9.8 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
96%
4%
Dynamic: 2.060 W (96%)
96%
Signals: 0.042 W (2%)
Logic: 0.032 W (2%)
I/O: 1.986 W (96%)
Device Static: 0.076 W (4%)

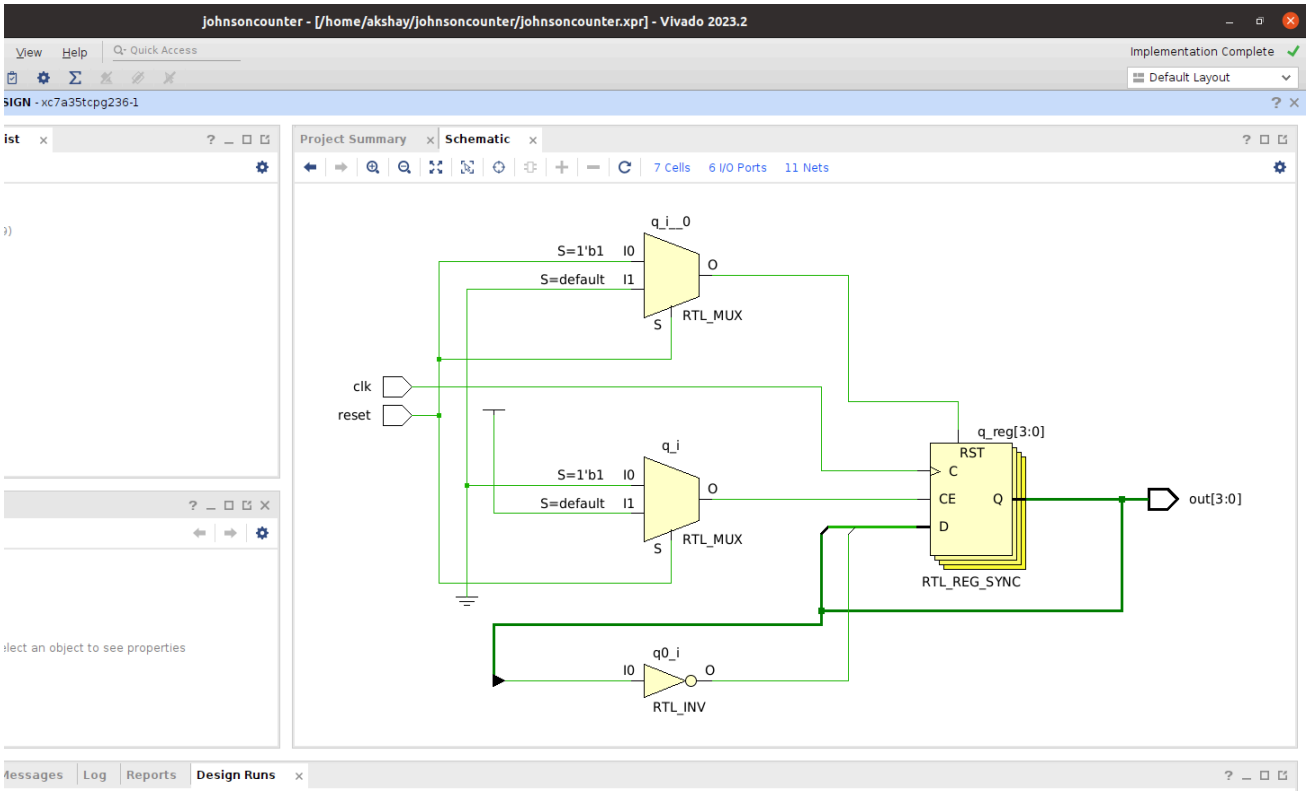
Q.29. Write Verilog code Synchronous 8-bit Johnson Counter:

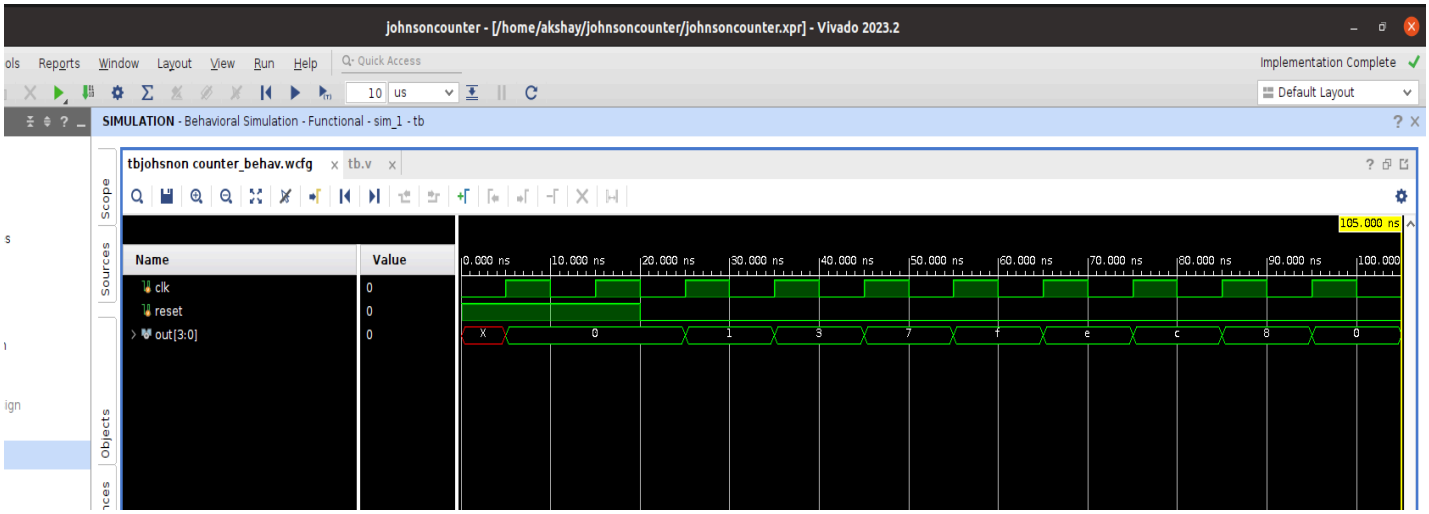
```
module bj( out,reset,clk);

input clk,reset;

output [3:0] out;

reg [3:0] q;

always @(posedge clk)

begin

if(reset)

 q=4'd0;

 else

        begin

                q[3]<=q[2];

                q[2]<=q[1];

                q[1]<=q[0];

                q[0]<=(~q[3]);

        end

 end

assign out=q;

endmodule

//////End////
```

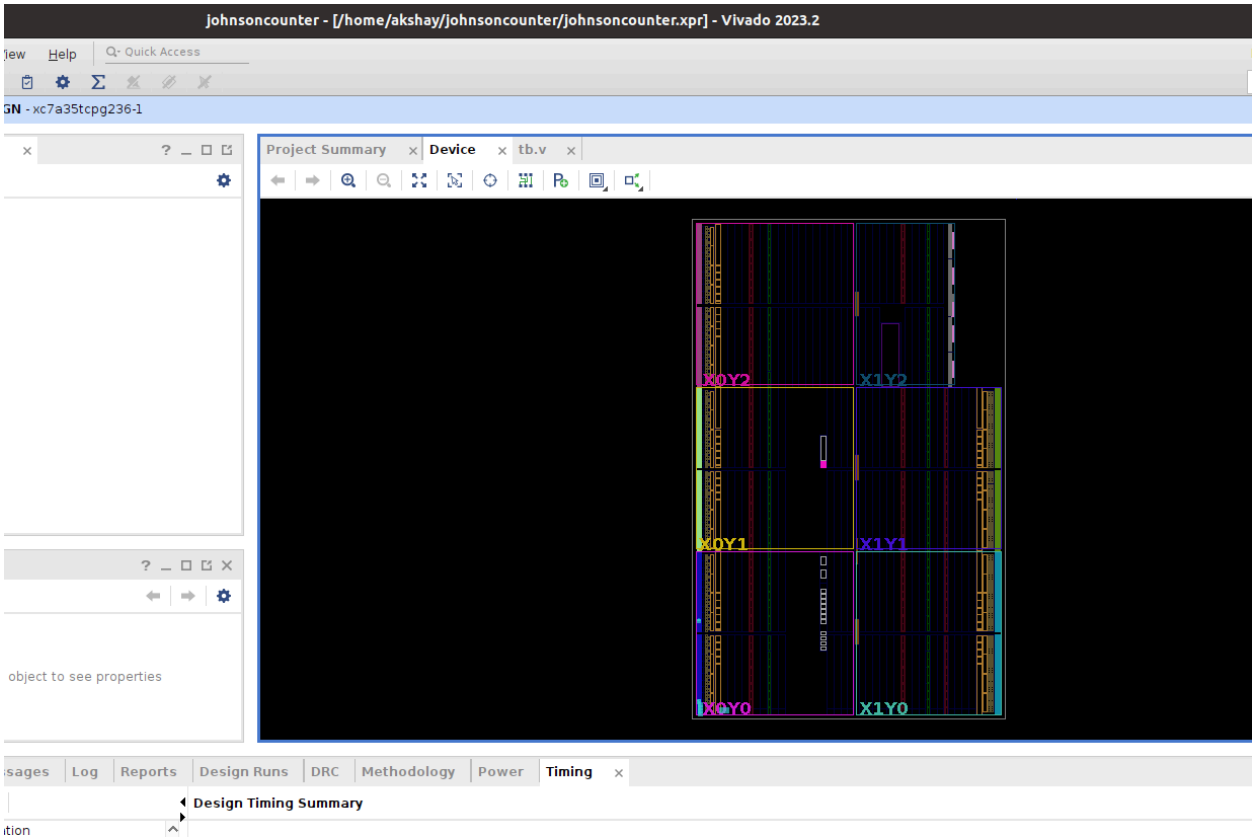
Testbench

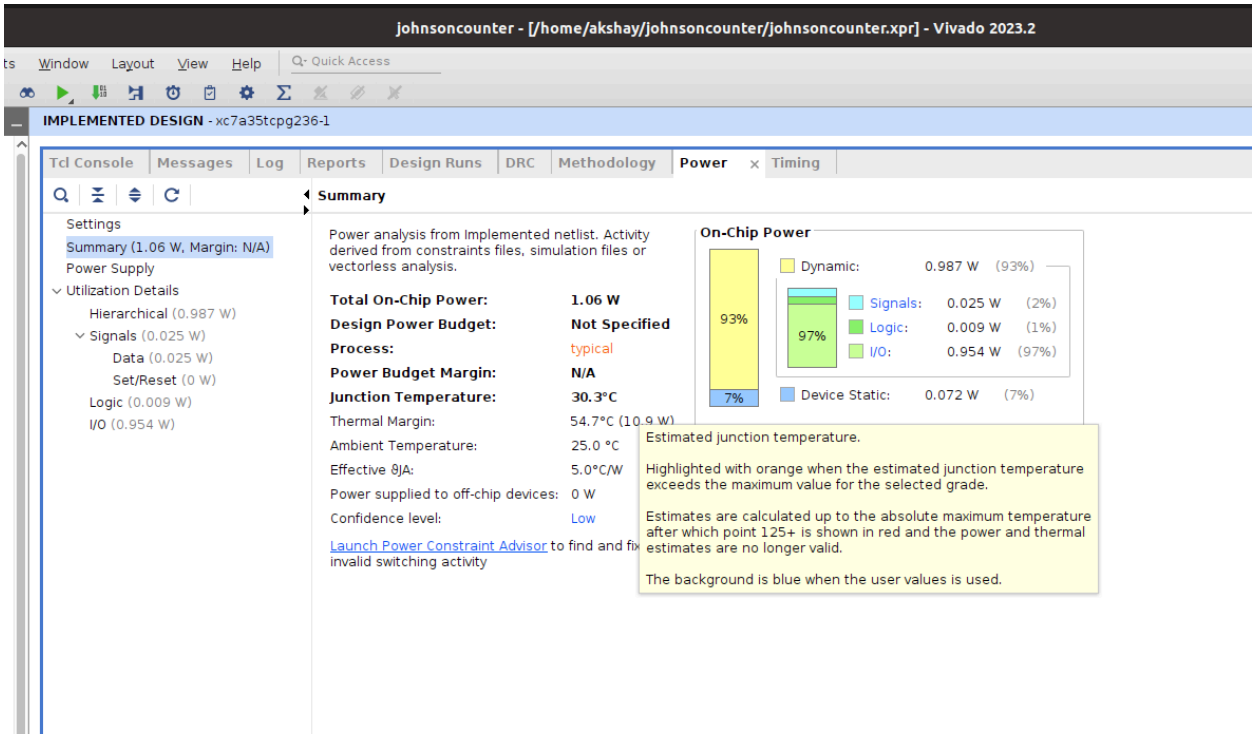
```
module tb(

    );
 reg clk,reset;
  wire [3:0] out;

  bj dut (.out(out), .reset(reset), .clk(clk));
```

```
 always
   #5 clk =~clk;

 initial begin
   reset=1'b1; clk=1'b0;
  #20 reset= 1'b0;
 end
   initial
   begin
          $monitor( $time, " clk=%b, out= %b, reset=%b", clk,out,reset);
          #105  $stop;
  end
endmodule
////End//////////
```




johnsoncounter - [/home/akshay/johnsoncounter/johnsoncounter.xpr] - Vivado 2023.2
Implementation Complete
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb
tbjohsnon counter_behav.wcfg
tb.v
Name
Value
clk
reset
out[3:0]
105.000 ns


johnsoncounter - [/home/akshay/johnsoncounter/johnsoncounter.xpr] - Vivado 2023.2
Project Summary
Device
tb.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
object to see properties
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Design Timing Summary


johnsoncounter - [/home/akshay/johnsoncounter/johnsoncounter.xpr] - Vivado 2023.2
Window
Layout
View
Help
Quick Access
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Settings
Summary (1.06 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.987 W)
Signals (0.025 W)
Data (0.025 W)
Set/Reset (0 W)
Logic (0.009 W)
I/O (0.954 W)
Summary
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 1.06 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 30.3°C
Thermal Margin: 54.7°C (10.9 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
93%
7%
97%
Dynamic: 0.987 W (93%)
Signals: 0.025 W (2%)
Logic: 0.009 W (1%)
I/O: 0.954 W (97%)
Device Static: 0.072 W (7%)
Estimated junction temperature.
Highlighted with orange when the estimated junction temperature exceeds the maximum value for the selected grade.
Estimates are calculated up to the absolute maximum temperature after which point 125+ is shown in red and the power and thermal estimates are no longer valid.
The background is blue when the user values is used.