Ferroelectric Negative Capacitances

Instrumentation And Applied Physics
Indian Institute Of Science

Student Name: Akshay Ranchhod Patil
Student Number: 19353
Course Centre: CENSE
Writeup Title: Ferroelectric Negative Capacitances
Instructor: Dr.Pavan Nukala

1 Abstract

Currently CMOS technology is facing two main fundamental problems/limitations in scaling down by both power disscipation and size -

1.Boltzmann Limit that limits the subthreshold swing S i.e (slope of the gate voltage vs log scale Drain Current) to 60 mV/decade.

2.The dimensional size of channel cannot be reduced below a certain range to avoid the kicking in of the tunnelling effects.

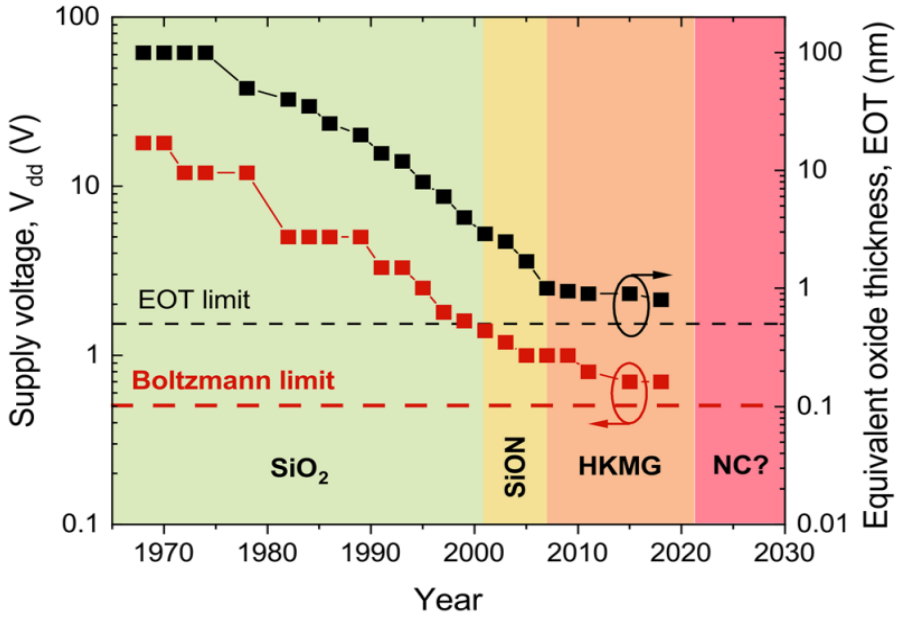

Figure 1: EOT(Black Line) and Supply Gate Voltage (Red line) Scaling in CMOS Technology

Accessing the Negative Capacitance regime of the ferroelectric oxides can essentially be one of the ways to overcoming the above two fundamental limits. This term paper will explain the basic concept of Negative Capacitances in detail and in particular the Ferroelectric type of Negative Capacitances and explore how to realize the Negative Capacitance in CMOS technology.

2 Introduction

Energy Efficiency improvements in nano-electronics have begun to slow down as the EOT limit and Boltzmannn limits are reached by the device as evident from the fig 1. EOT is defined as the equivalent SiO_2 thickness that is needed to achieve the same capacitance as a gate oxide (usually HfO_2) with higher ϵ_r and thickness d.

EOT = $t_{SiO2} + \alpha t_{Gateoxide} = \epsilon_{SiO_2}/(\epsilon_{Gateoxide}$*d).

Lower the EOT of the gate oxide,less voltage is needed to switch the device between "ON" and "OFF",Since voltage drop across gate oxide is reduced. For nearly 4 decades , SiO_2 was used as the gate dielectric material in Si based MOSFET due to ease of fabrication and high quality Si to SiO_2 interface.As SiO_2 was the oxide used EOT of the gate oxide is equal to physical length of the Silicon dioxide in the device. Below 3nm of EOT ,Quantum Mechanical Effects starts kicking in and hence leads to significant increase in the gate dielectric power consumption.Hence SiO_2 was replaced by $SiON$ to increase ϵ_r to 5 and reduce the EOT to 2nm. Further SiON was again replaced by an higher ϵ_r called as the high k metal gate HfO_2 with ϵ_r = 17 having EOT = 0.8nm. EOT scaling below 0.5 nm is practically impossible due to QM effects as thin layer of $SiO2$ is always present as an interface between $HfO2$ (High K dielectric and Si Channel) as SiO_2 is used to avoid lossy coupling between Si channel and High K dielectric.Reduction in EOT is needed to increase the electrostatic coupling between the gate and semiconductor channel.Hence the equivalent oxide thickness is one of the fundamental scaling limits that CMOS technology is approaching.The second and more fundamental limit that governs the scaling limit is the Boltzmann limit , even if the EOT can be reduced to zero,Boltmann Limit limits the further reduction of V_{dd} i.e the gate voltage which is more important parameter than EOT to improve the energy efficiency at the nanoscale in integrated circuits.

Performance of MOSFET is governed by the high I_{on}/I_{off} ratio for the drain current. As per the boltzmann distribution of electron energies at the source Q is directly proportional to exp ($q\psi_s/k_BT$) and $I_d = dQ/dt$, we can define a quantity subthreshold swing S as the amount of gate voltage required to change the current by 1 decade.

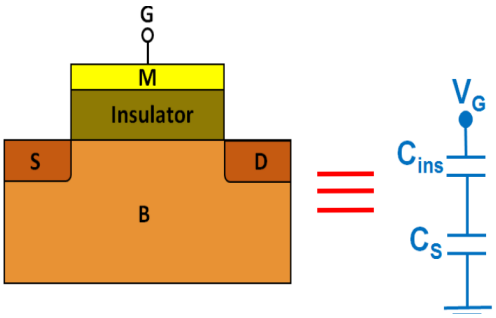

Figure 2: Present MOSFET Device Scematic Diagram and Equivalent Capacitance Diagram

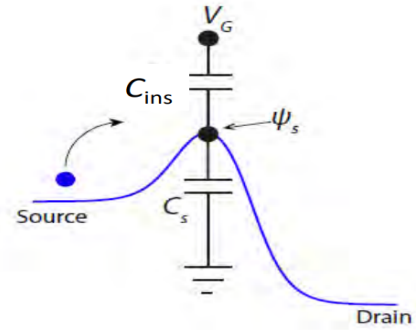

Figure 3: Equivalent Capacitance Diagram showing the Gate Voltage and the surface potential

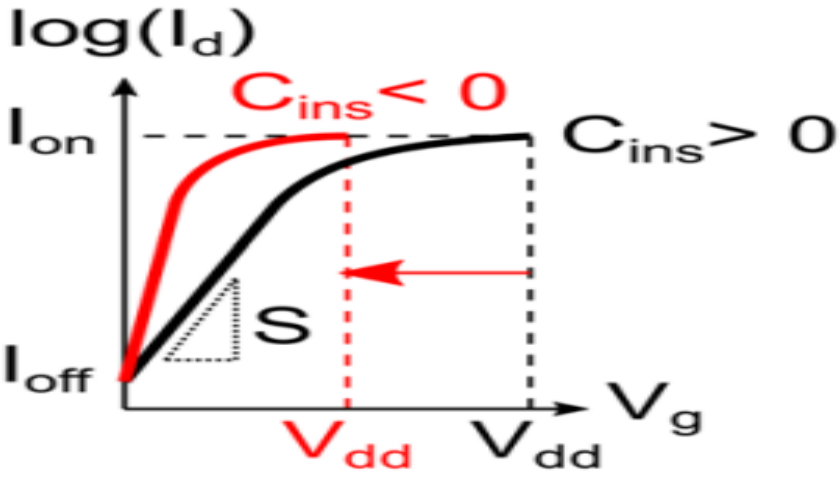

Figure 4: Subthreshold Swing Graph

The charge due to gate voltage, $Q_g = C_{eq}V_G$
$Q_g = (1/C_{in} + 1/C_s)^{-1} * V_G$
$Q_g = C_{in}(V_G - \psi_s) = C_s\psi_s$
$C_{ins}(V_G/\psi_s - 1) = C_s$
$V_G/\psi_s = C_s/C_{in} + 1$
$dV_G/d\psi_s = C_s/C_{ins} + 1$
$S = dV_G/d(log_{10}I_D)$ saa(as plotted in the graph)
= $dV_G/d\psi_s * d\psi_s/d(log_{10}I_D)$ = $dV_G/d\psi_s * 2.3k_B * T/q$ =$dV_G/d\psi_s$ * 60 mV/decade = (1 + C_s/C_{ins}) $* 60$
K_B = Boltzmann Constant

With Boltzmann's limit ,the gate supply voltage can't be reduced below 0.5 V in the conventional MOSFETs.So thus we are approaching the Boltzmann limit of 0.5 V V_d as the current technologies use 0.7 V and also EOT limit of 0.5 nm.So what could be a solution to overcome the Boltzmann's limit and the EOT limits? Use of Negative Capacitance concept. Historically it has been observed that $dV_G/d\psi_S$ = 1 + C_s/C_{ins} is always greater than 1 but what if $C_s/C_{ins} < 0$ i.e $C_{ins} < 0$, we could overcome the Boltzmann's Limit of 60 mV and the EOT limit of 0.5nm and hence improve MOSFET power disscipation i.e reduce it. As negative capacitance leads to voltage amplification and with smaller V_G we get larger charge on the capacitor and hence high current and low power disscipation. Hence the applications of such Negative Capacitance Field Effect Transistor (NCFET) can be tremendous -

1.Low power Computing
2.Neuromorphic and Intelligent Computing
3.Performance booster for Complementary MOS transistors.
4.Building SRAM of the computers
5.Reduce topological transistor Switching Energy.

3 Capacitance

1. Capacitance for two terminal device is defined in general as C = dQ/dV i.e Q = Charge on the terminals , V = Voltage between two terminals

2. Displacement Field in linear dielectric material is defined as,

D = $\epsilon E + P = \epsilon_0\epsilon_r E$
P = $\epsilon_0 E(\epsilon_r - 1) = X\epsilon_0 E$
X = Susceptibility of the medium = $(\epsilon_r - 1) = P/(\epsilon_0 E)$
$\epsilon_r = n^2$
Inserting a dielectric of ϵ_r leads to an increase in stored charge in the capacitor.

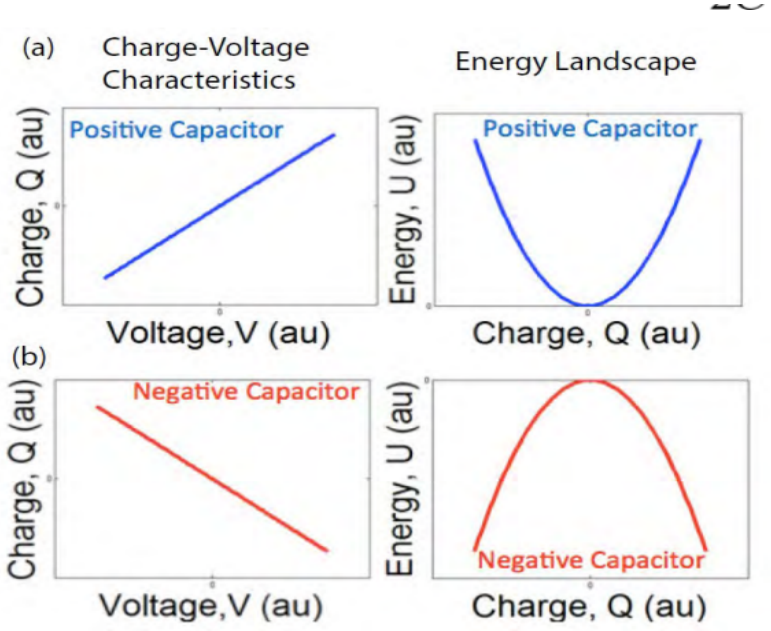

Figure 5: Charge Voltage Characteristics and Energy Landscape of Linear Capacitor

Energy landscape of Capacitor = $C_{ins} = [d^2G/dQ^2]^{-1} = dP/dE$

C = inverse of radius of curvature of energy landscape or free energy density or Slope of Polarization vs electric field curve = Capacitance of Capacitor.

Until Now we considered only linear dielectrics i.e Polarization P is linear function of E i.e observed in Paraelectric Phase of the material. Paraelectric Phase is phase in which we get No polarization when the electric field i.e $Q = P = \epsilon E$ is removed as shown in the fig.

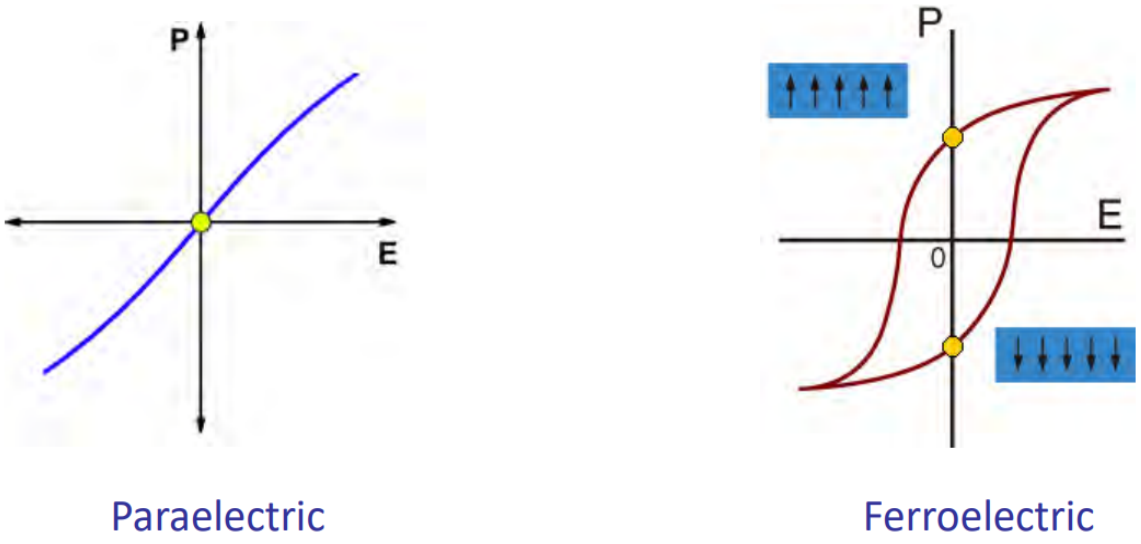

Figure 6: Paraelectric and Ferroelctric Phases of a Perovskite

Now Considering the nonlinear dielectrics i.e Polarization P is non - linear function of electric field E i.e considering the ferroelectric phase of the material we get two possible states of polarization when the electric field is removed - up and down state which is called as the spontaneous or the remnant polarization. For material to be in Ferroelectric phase,material should be non-centrosymmetric i.e it should have spontaneous polarization and polarization state can be reveresed by application of electric field. Examples of Ferroelectric Materials are Lead Titanate and HZO.

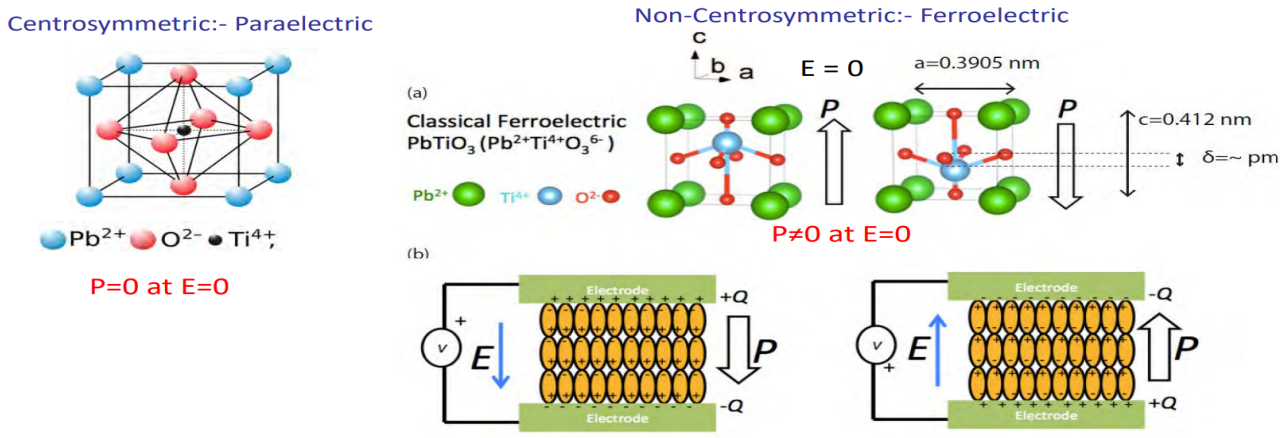

Figure 7: Centrosymmetric(Paraelectric) and Non-Centrosymmetric(Ferroelectric) Lead Titanate

Paraelectric to Ferroelectric Phase Transition in Perovskites occurs at the temperature above a critical temperature called as the Curie temperature.This is just an example explaining the transition from Paraelctric Phase to Ferroelectric Phase in Perovskites.But these Perovskites are not compatible with CMOS and hence generally HfO_2 is used as the CMOS chips already have HfO_2 created by

Atomic Layer Deposition as the gate dielectric of the transistor.

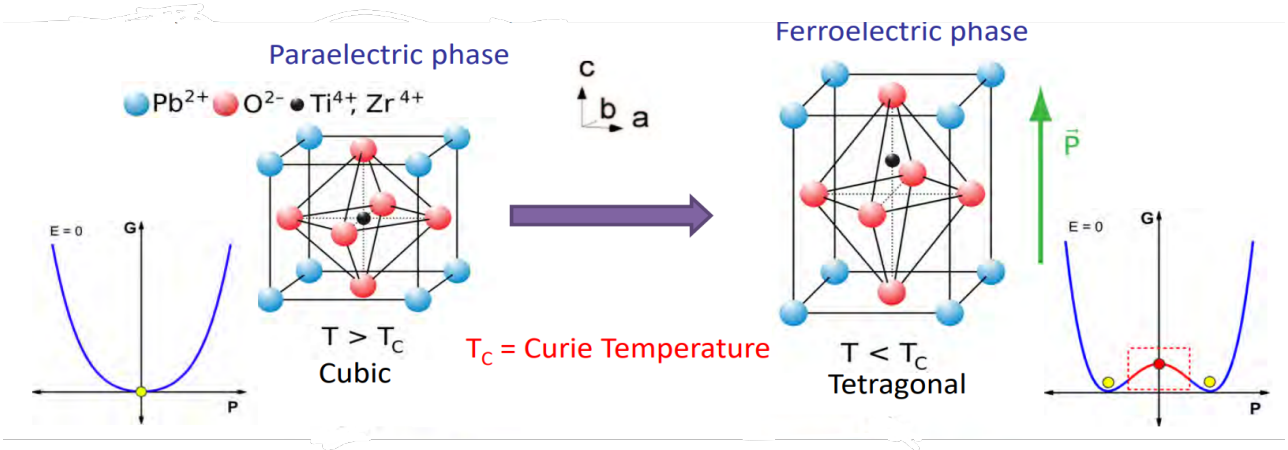

Figure 8: Paraelectric to Ferroelectric Phase Transition in PZT (Lead Zirconium Titanate)

Ferroelectrics pocess Polarization even when no electric field is applied ,this is the so called spontaneous polarization which is direct consequence of non-centrosymmetric crystal structure and can be reversed by application of an electric field larger than the coersive field , a minimum elctric field needed for polarization switching.This makes Ferroelectric ideally suited for non-volatile memory devices. Now considering the dielectric displacement, D = ϵE + P

dD/dE$_f$ = $dQ/dE_f = \epsilon_0 + dP_s/dE_f = dP_s/dE_f$.

When the polarization in Ferroelectrics change opposite to electric field i.e dP_s/dE_f = -ve i.e ϵ_f = -ve which implies that Capacitance becomes negative.

4 Landau Khalatnikov Theory Of Non-linear Dielectrics

Negative Capacitance was first observed by Landau in 1976.

1. Free Energy of non-linear dielectric as per Landau Theory is given as,

$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$

	α	β	γ
Positive	+	+	+
FE-1	−	+	+
FE-2	−	−	+
NEM AFE	+	−	+

Figure 9: Table Indicating the alpha,beta,gamma values for various types of Capacitances for stability reasons

δdP/dt = - dG/dP or C = $(d^2G/dP^2)^{-1}$

$C^{-1} = \alpha + \beta P^2 + \gamma P^4$

Assuming the second order phase transition,

for T< T_{curie} => α < 0 , β > 0 , $E_f = 0, P_{smax} = 0 => unstable.$

0 = $dG_f/dP_s = 2\alpha P_s + 4\beta {P_s}^3 - E_f$

$E_f = 2\alpha P_s + 4\beta {P_s}^3$

$dE_f/dP_s = 0 = (\epsilon_0 \epsilon_f)^{-1} = 2\alpha + 12\beta {P_s}^2$

for $\alpha < 0 =>$ and low values of $P_s => (\epsilon_0 \epsilon_f)^{-1} => -ve.$

But this simple ferroelctric model neglects the effect of nucleation and growth.

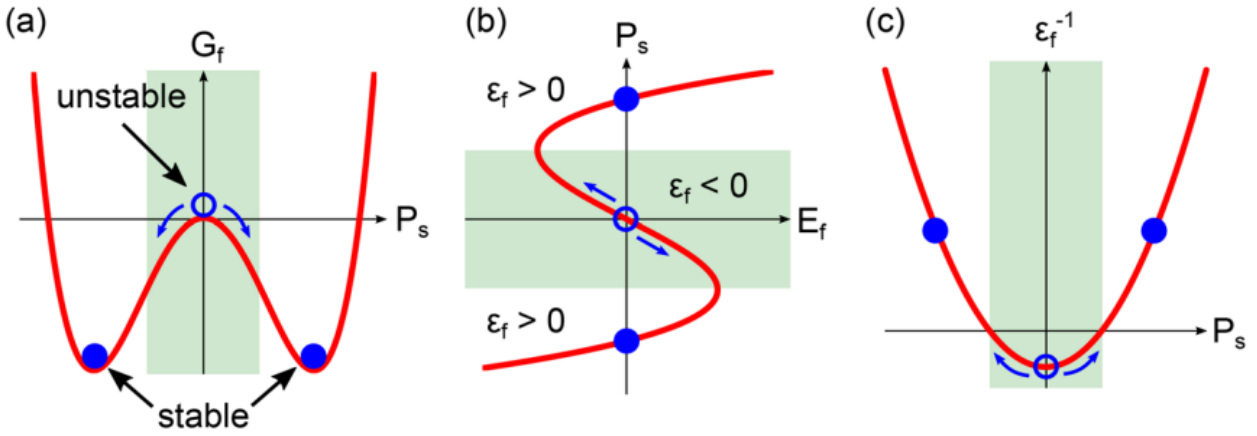

Figure 10: Gibbs Free Energy vs P_s,$P_s vs E_f$ and $1/\epsilon$ vs P_s as per the three above equations.

As indicated in figure 10(a) G_t is concave downwards and hence unstable in the negative capacitance region.

Two ways to access the unstable NC region are,

1.Switching the ferroelectric Polarization from one stable state to another one by applying an electric field we can access transient NC for limited time during switching. => Transient N.C

2. Integrating Ferroelectric into a larger structure such that NC become thermodynamically stable when G_{total} is minimized => Stable N.C.

Note => There are other ways to recognize Negative Capacitances other than Ferroelctric N.C as shown the figure below.

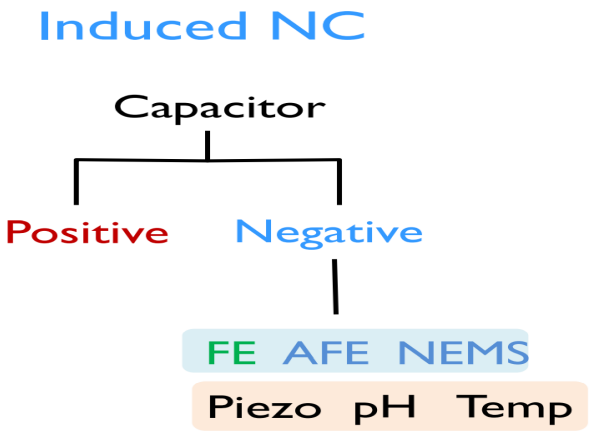

Figure 11: Other Ways to recognize Negative Capacitances

5 Transient Negative Capacitances

1. Consider a MFM capacitor that is switching from negative polarization state to positive one.

2. Initially for v=0 we get energy landscape i.e., Gf vs Ps as shown in the fig. as per Landau theory, it has two states of positive and negative polarization, the area shaded in green represents the region of negative capacitance.

3. Now, as we apply potential the energy landscape will tilt to the right such that the minimum free energy of the polarization increases as shown in the fig.

4. Now, if applied potential is greater than Vc i.e., coercive field the material is positive polarization state will traverse through the negative capacitance region unless it reaches the right minimum.

5. Now, again if we decrease the potential to zero the energy landscape returns to original position as in point 1 above, but now the potential is in positive polarization state.

6. Polarization will always increase with time in this experiment as we are getting from negative to positive Ps as we increase voltage.

Now, the charge in the nonlinear dielctric i.e the ferroelectric material can be defined as,

$$Q = D = \epsilon_0 E_F + P_s$$

$$\frac{dQ}{dt} = \frac{dD}{dt} = \epsilon_0 \frac{dE_f}{dt} \frac{+ dP_s}{dt} \Rightarrow \frac{dE_f}{dt} = \left(\frac{dQ}{dt} - \frac{dP_s}{dt} \right) / \epsilon_0$$

For,

$$\frac{dQ}{dt} < \frac{dP_s}{dt} \Rightarrow \frac{dE_f}{dt} < 0$$

i.e., region of negative capacitance. Change of P_s is faster then change of Q.

But, since the region of negative capacitance Gf is local minimum, hence unstable and hence we can't continuously access the negative capacitance region. One way is to use a circuit element such as resistor, dielectric capacitor or a gate of MOSFET in series with the MFM connection, which decreases the dQ/dt as well ad dEf/dt terms for increasing applied voltage, hence we can access the negative capacitance region.

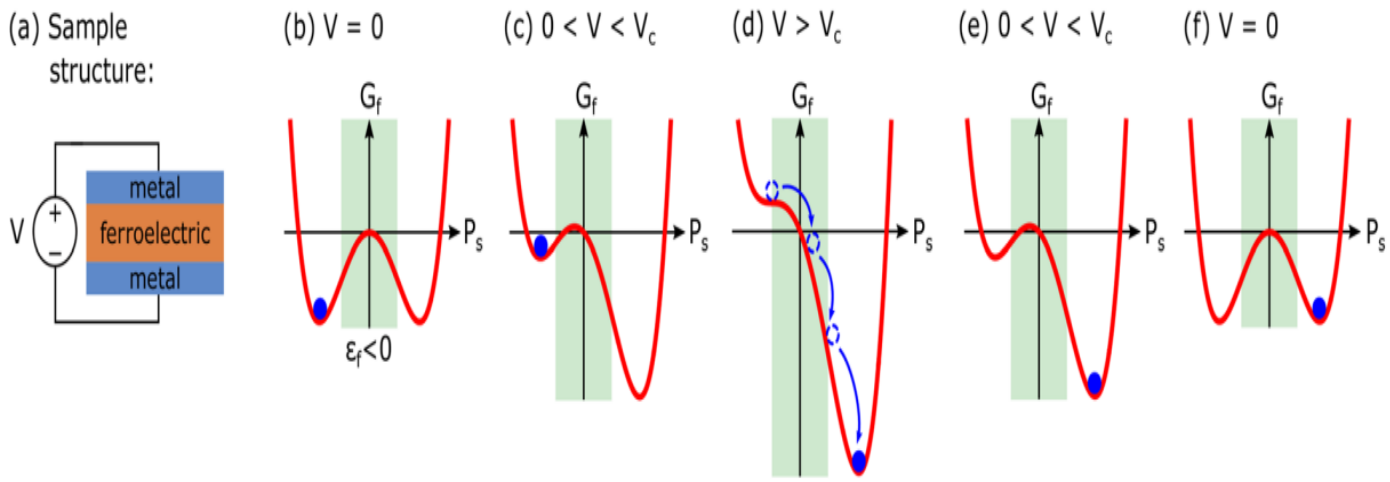

Figure 12: Transient Accessing Of Negative Capacitance Regime by chaniging the electric field

Use of transient negative capacitance in applications has two main disadvantages, 1. Large polarization hysteresis is observed due to irreversible domain nucleation and growth. This leads to power dissipation and hence we need to increase gate voltage. 2. Polarization switching can be fast or slow depending on the applied voltage, to access the negative capacitance region, it should be slow, but then it can't be used for high speed digital electronics operating at low voltage and GHz frequencies.

Let's look at stabilized negative capacitance to overcome the transient negative capacitance.

6 Stabilized Negative Capacitances

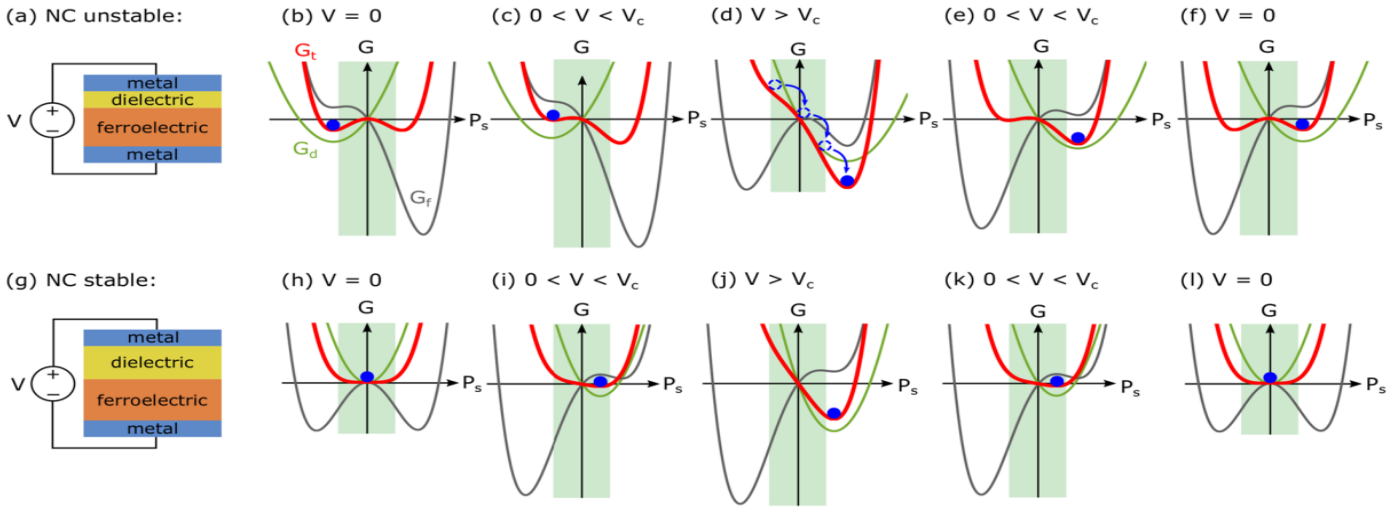

Figure 13: NC stable and NC unstable regime for Stabilzed Structure of Negative Capacitances

1.Add a positive dielectric capacitance layer to MFM to form MDFM layer as shown in the figure.

2.Free Energy of Dielectric with relative permittivity and $\varepsilon_d$lectric Field Ed is given as, $G_d = \frac{D^2}{2\varepsilon_0\varepsilon_d} - E_d D.$

3.Total free energy is given by, $G_t = G_f t_f + G_d t_d = \left(\alpha t_f + \frac{t_d}{2\varepsilon_0\varepsilon_d}\right)P_s^2 + t_f \beta P_s^4 - VP_s$

4.NC becomes stabilized when $t_f \leq t_{f,crit} = -\frac{t_d}{2\alpha\varepsilon_0\varepsilon_d}$ that is, the term in the bracket is positive

Because the Gd curvature is always +ve but Gf curvature becomes negative in NC region and hence Gd should balance out this curvature in NC region to give Gt as positive and concave upwards in NC region

Consider the following two cases.

1. t_f > $t_{fcritical}$, negative capacitance is stable (dielectric thickness is very low) Curvature of G_t with respect to P_s in negative capacitance region is concave downwards, hence unstable. The polarization switching in the energy landscapes of G_t, G_d G_f are shown for various voltages for both negative capacitance unstable and negative capacitance stable regions.

2. t_f <= $t_{fcritical}$, negative capacitance unstable (dielectric thickness is large) Maximum of G_f and minimum of G_d and G_t now coincide i.e., G_t becomes always concave upwards, no instability and hence we can access stable negative capacitance without hysteresis.

Here we neglected the formation of ferroelectric domains.

7 Ferroelectrics For NC Devices

For practical realization of NC devices following conditions by Ferroelectrics need to be satisfied –

A.Robust ferroelectricity at 5 nm thickness and below – 1.Stabilizes NC 2.Scaling Down

B.Compatibility with CMOS technology – HfO2 based ferroelectrics

C.Thermal stability on silicon – Should be able to withstand hydrogen Annealing and temperature above 500 C.

D.Conformal deposition on 3D substrates

E.Large electronic bandgap and conduction band offset to Si – To reduce gate leakage current.

Perovskites materials like Rochelle Salt,BaTiO3,Polymer Based,triglycine sulfate based materials have low electronic bandgap and hence leads to high gate leakage currents and also high processing and integration temperature of 500 C and hydrogen annealing is unfavourable.The most promising candidate for the practical realization of negative capacitances is Hafnium Dioxides.

8 Outlook

1.Landau Theory does not take in to account the nucleation and growth and also HfO2 can have non – idealities like Ferroelectric domains,defects etc . Hence detailed study on microstructure should be done as it is the most promising candidate that satifies the previous 5 criterions to realize NC practically.

2.If no subthreshold swing below the Boltzmann limit is observed, then electrical characteristics have to be compared to an appropriate reference device, which should have as few processing differences as possible, but must have a non-ferroelectric gate oxide.

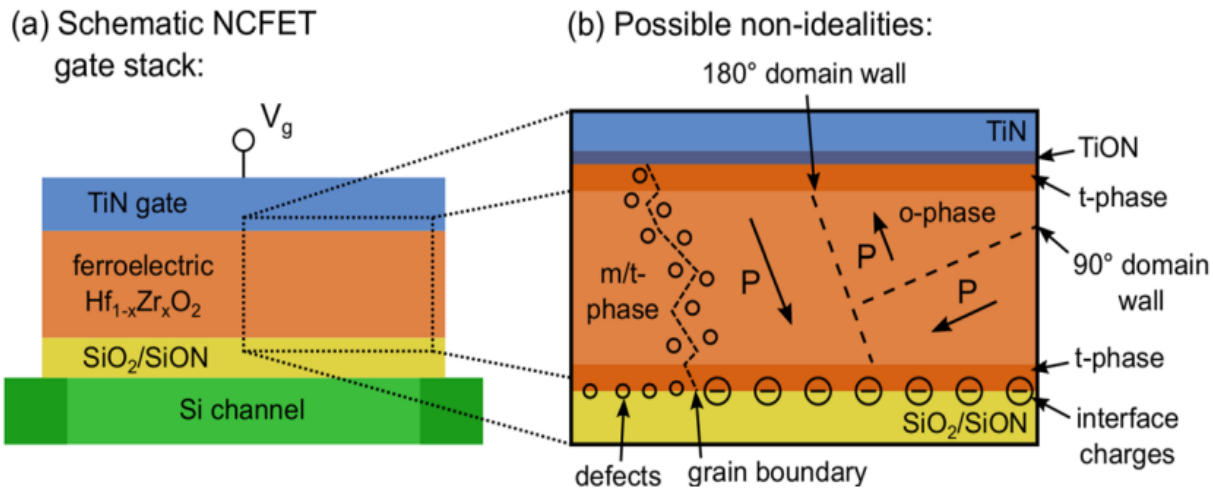

Figure 14: Non idealiites and defects in Practical Hafnium Dioxides

9 References

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