University of Maryland Baltimore County
Department of Computer Science and Electrical Engineering

CMSC 611 - Advanced Computer Architecture

Assignment #3 Due: Thursday 3/27/2014 in class

Question 1: *(100 Points)*

The goal of this exercise is to compare how a loop runs on a variety of pipelined versions of MIPS. The loop implements the vector operation Y = a × X + Y. Here is the MIPS code for the loop:

```
        DADDIU   R4, R1, #800      ; R1 = upper bound for X
Again:  L.D      F2, 0(R1)         ; Load X(i)
        MULT.D   F4, F2, F0        ; multiply a * X(i)
        L.D      F6, 0(R2)         ; load Y(i)
        ADD.D    F6, F4, F6        ; add a * X(i) + Y(i)
        S.D      0(R2), F6         ; store Y(i)
        DADDIU   R1, R1, #8        ; increment X index
        DADDIU   R2, R2, #8        ; increment Y index
        SLTIU    R3, R1, done      ; test if done
        BEQZ     R3, Again         ; loop if not done
```

The conditional branches are resolved in the ID stage. Use the FP latencies shown in the following table but assume that the FP unit is fully pipelined:

Instruction Producing Results	Instruction Using Results	Latency
Integer ALU and all loads	Any	2
FP add	FP ALU Op	4
FP multiply	FP ALU Op	6
FP add	FP Store	4
FP multiply	FP Store	5

A) Using a single issue MIPS pipeline show the number of stall cycles for each instruction and what clock cycle each instruction begins execution (i.e., enters its first EX cycle) on the first iteration of the loop. How many clock cycles does a loop iteration take?

B) Schedule the loop (i.e., reorder the instructions) in order to improve the performance in Part (A). Assume delayed branching. How many clock cycles does a loop iteration take?

C) Unroll the loop to make four copies of the body and schedule it. Re-order the instructions to maximize the performance. How many clock cycles does a loop iteration take? Note that there are only 1 FP adder, 1 FP Multiplier, and 1 Integer Unit.

D) Consider running the loop on a CDC scoreboard. What would be the state of scoreboard when the SLTIU instruction reaches the write result stage in the first iteration? Assume that issue and read operands stages each take one cycle. Assume that there are one integer functional unit, one FP multiplier, and one FP adder. The latency is as follows:

Functional unit	Latency	Functional unit	Latency
Integer ALU	0	FP add	4
Load (integer and FP loads)	2	FP multiply	6