University of Maryland Baltimore County
Department of Computer Science and Electrical Engineering

CMSC 611 - Advanced Computer Architecture

Assignment #4 Due: Thursday 5/1/2014 in class

Question 1: *(22 Points)*

Consider a branch-target buffer that has penalties of 0, 2, and 2 clock cycles for correct conditional branch prediction, incorrect prediction, and a buffer miss, respectively. Consider a branch-target buffer design that distinguishes conditional and unconditional branches, storing the target address for a conditional branch and the target instruction for an unconditional branch.

A) What is the penalty in clock cycles when an unconditional branch is found in the buffer?

B) Determine the improvement from branch folding for unconditional branches. Assume a 90% hit rate, an unconditional branch frequency of 5%, and a 2-cycle penalty for a buffer miss. How much improvement is gained by this enhancement? How high must the hit rate be for this enhancement to provide a performance gain?

Question 2: *(24 Points)*

One difference between a write through cache and write-back cache can be in the time it takes to write. During the first cycle, we detect whether a hit will occur, and during the second (assuming a hit) we actually write the data. Let's assume that 50% of the blocks are dirty for a write-back cache. For this question, assume that the write buffer for a write through will never stall the CPU (no penalty). Assume a read hit takes 1 clock cycle, the cache miss penalty is 50 clock cycles, and a block write from the cache to main memory takes 50 clock cycles. Finally, assume the instruction cache miss rate is 0.5 % and the data cache miss rate is 1%.

Use the instruction frequencies shown in the following table:

Instruction	load	store	add	sub	mul	compare	load imm	cond branch	jump	call	return	shift	and	or	other
Frequency	26%	9%	14.6%	0.5%	0.1%	12.4%	7.9%	11.5%	1.3%	1.1%	1.5%	6.2%	1.6%	4.2%	1.1%

A) Estimate the performance of a write–through cache with a two cycle write.

B) Repeat part (A) assuming the write–through cache pipelines the writes, as discussed in class, so that a write hit takes just one clock cycle.

Question 3: *(30 Points)*

Using the sequences of 32-bit memory references, given as word addresses in the following table:

1	4	8	1	5	20	17	19	56	9	11	4	43	5	6	9	17

A) For each of these references, identify the tag and index given a direct-mapped cache with 16 one-word blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.

B) Repeat part (A) for a direct-mapped cache with two-word blocks and a total size of eight blocks.

C) Repeat part (A) for a fully associative cache with one-word blocks and a total size of sixteen words. Use LRU replacement.

Question 4: *(24 Points)*

You are designing a write buffer between a write-through L1 cache and a write-back L2 cache. The L2 cache write data bus is 16 byte wide and can perform a write to an independent cache address every 4 cycles.

A) How many bytes wide should each write buffer entry be?

B) What speedup could be expected in the steady state by using a merging write buffer instead of a non-merging buffer when accessing memory by the execution of 64-bit stores if all other instructions could be issued in parallel with the stores and the blocks are present in the L2 cache?

C) What would be the effect of possible L1 misses be on the number of required write buffer entries for systems with blocking and non-blocking caches?