PROJECT IITB_RISC

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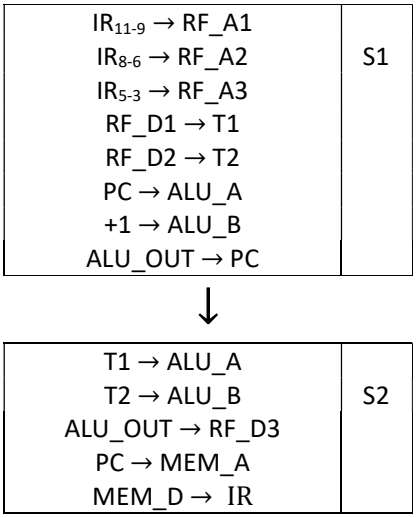
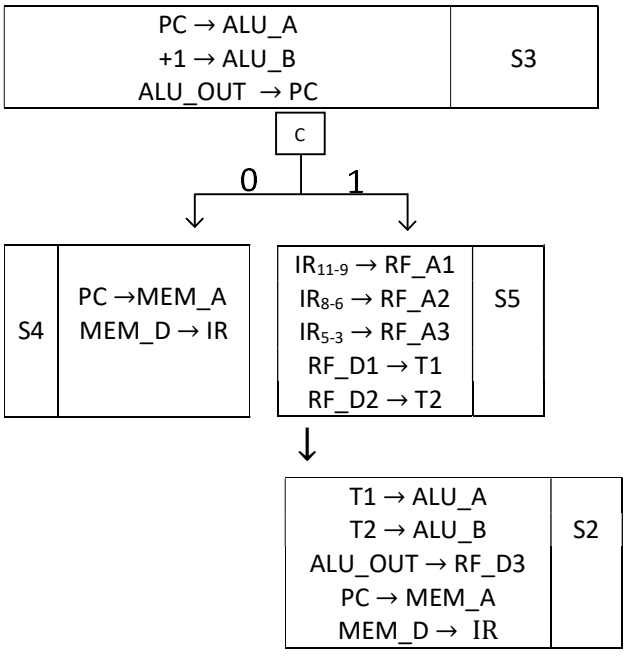
HARDWARE FLOW CHARTS

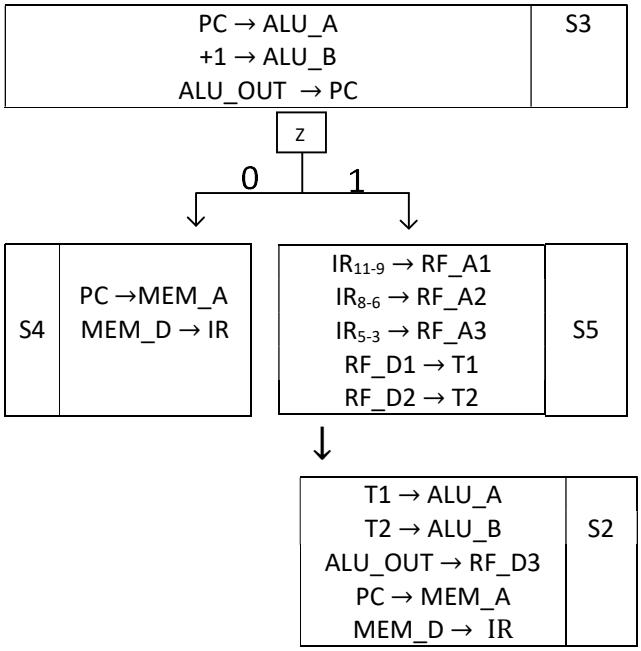
ADD:



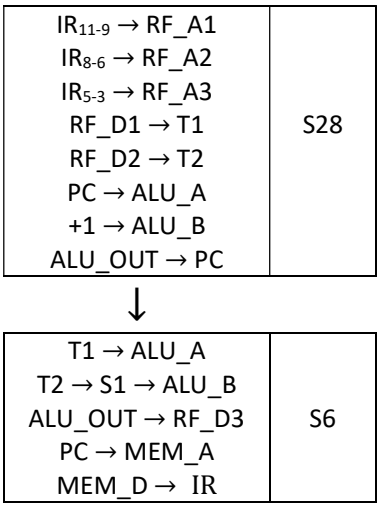
ADC:



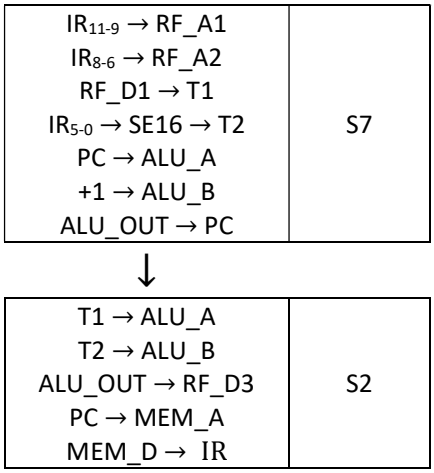
ADZ:


PC → ALU_A
+1 → ALU_B
ALU_OUT → PC
S3
Z
0
1
S4
PC →MEM_A
MEM_D → IR
IR11-9 → RF_A1
IR8-6 → RF_A2
IR5-3 → RF_A3
RF_D1 → T1
RF_D2 → T2
S5
T1 → ALU_A
T2 → ALU_B
ALU_OUT → RF_D3
PC → MEM_A
MEM_D → IR
S2

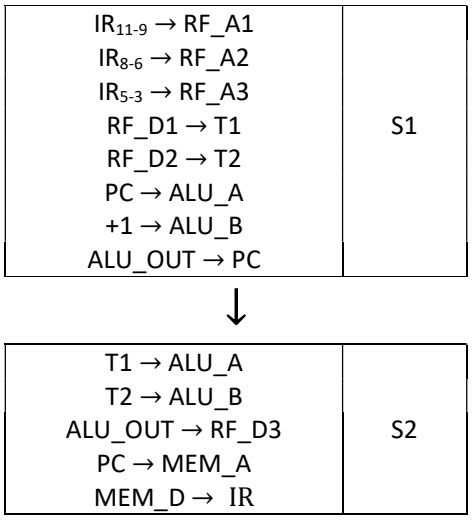
ADL:


IR11-9 → RF_A1
IR8-6 → RF_A2
IR5-3 → RF_A3
RF_D1 → T1
RF_D2 → T2
PC → ALU_A
+1 → ALU_B
ALU_OUT → PC
S28
T1 → ALU_A
T2 → S1 → ALU_B
ALU_OUT → RF_D3
PC → MEM_A
MEM_D → IR
S6

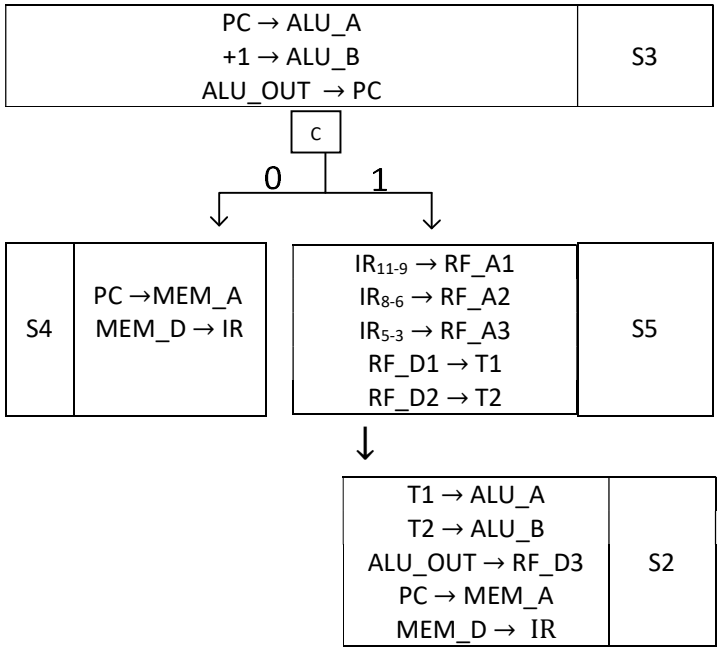
ADI:


IR11-9 → RF_A1
IR8-6 → RF_A2
RF_D1 → T1
IR5-0 → SE16 → T2
PC → ALU_A
+1 → ALU_B
ALU_OUT → PC
S7
T1 → ALU_A
T2 → ALU_B
ALU_OUT → RF_D3
PC → MEM_A
MEM_D → IR
S2

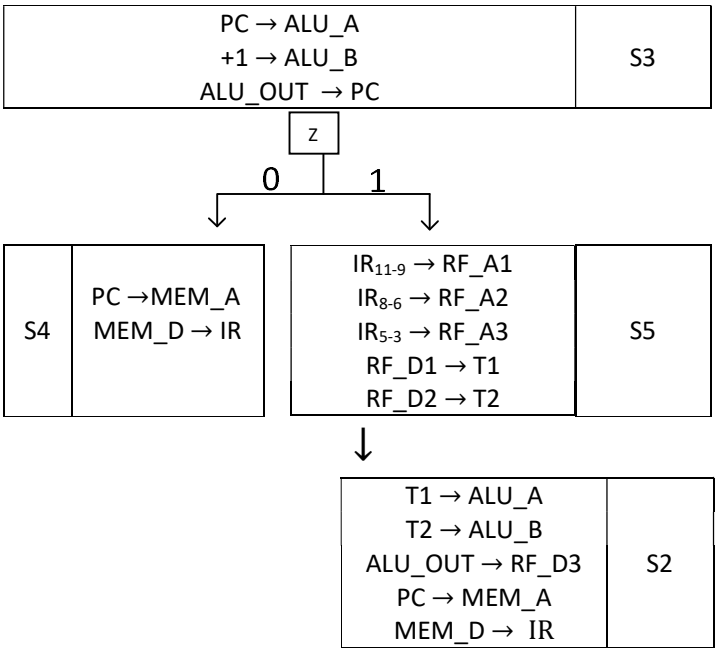
NDU:


$IR_{11-9} \rightarrow RF\_A1$
$IR_{8-6} \rightarrow RF\_A2$
$IR_{5-3} \rightarrow RF\_A3$
$RF\_D1 \rightarrow T1$
$RF\_D2 \rightarrow T2$
$PC \rightarrow ALU\_A$
$+1 \rightarrow ALU\_B$
$ALU\_OUT \rightarrow PC$
S1
$T1 \rightarrow ALU\_A$
$T2 \rightarrow ALU\_B$
$ALU\_OUT \rightarrow RF\_D3$
$PC \rightarrow MEM\_A$
$MEM\_D \rightarrow IR$
S2

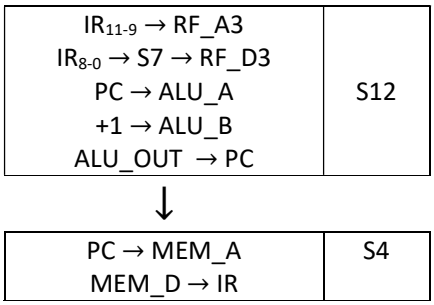
NDC:


$PC \rightarrow ALU\_A$
$+1 \rightarrow ALU\_B$
$ALU\_OUT \rightarrow PC$
S3
C
0
1
S4
$PC \rightarrow MEM\_A$
$MEM\_D \rightarrow IR$
$IR_{11-9} \rightarrow RF\_A1$
$IR_{8-6} \rightarrow RF\_A2$
$IR_{5-3} \rightarrow RF\_A3$
$RF\_D1 \rightarrow T1$
$RF\_D2 \rightarrow T2$
S5
$T1 \rightarrow ALU\_A$
$T2 \rightarrow ALU\_B$
$ALU\_OUT \rightarrow RF\_D3$
$PC \rightarrow MEM\_A$
$MEM\_D \rightarrow IR$
S2

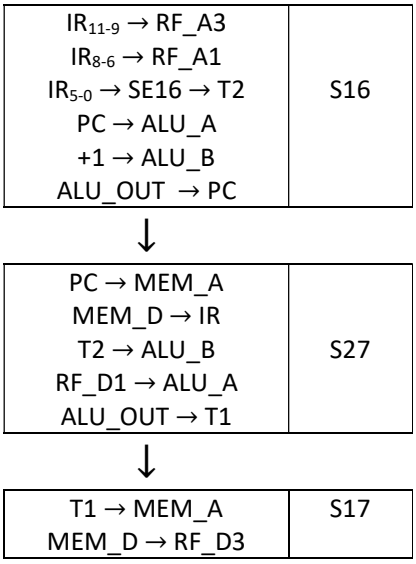
NDZ:


PC → ALU_A
+1 → ALU_B
ALU_OUT → PC
S3
Z
0
1
S4
PC →MEM_A
MEM_D → IR
IR11-9 → RF_A1
IR8-6 → RF_A2
IR5-3 → RF_A3
RF_D1 → T1
RF_D2 → T2
S5
T1 → ALU_A
T2 → ALU_B
ALU_OUT → RF_D3
PC → MEM_A
MEM_D → IR
S2

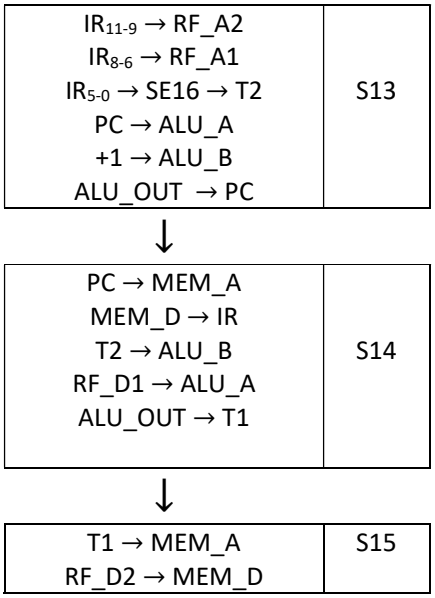
LHI:


IR11-9 → RF_A3
IR8-0 → S7 → RF_D3
PC → ALU_A
+1 → ALU_B
ALU_OUT → PC
S12
PC → MEM_A
MEM_D → IR
S4

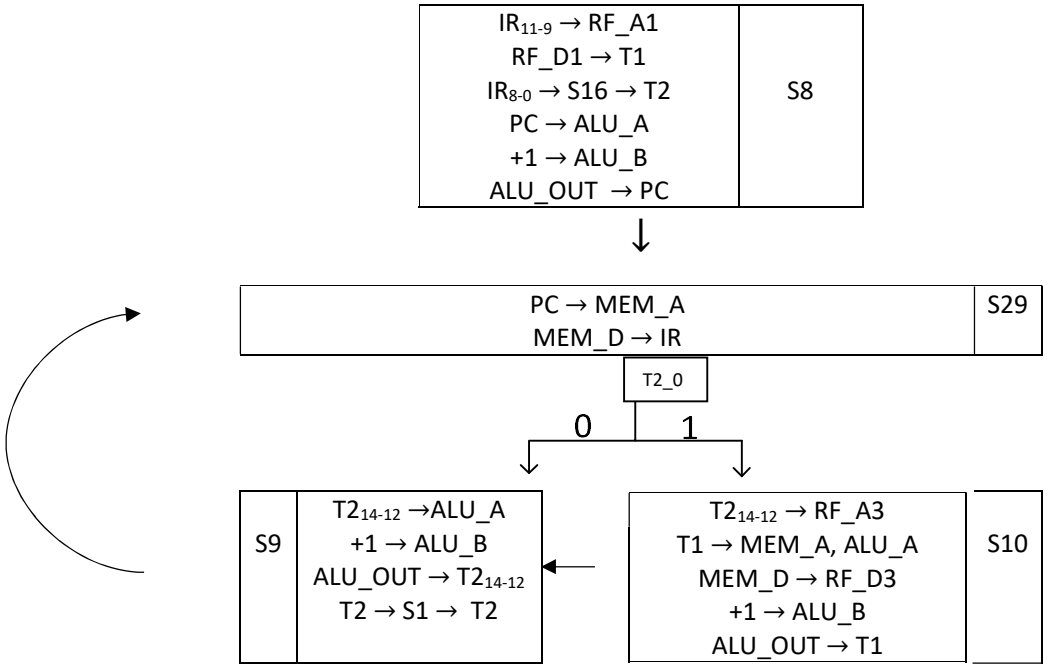
LW:


IR11-9 → RF_A3
IR8-6 → RF_A1
IR5-0 → SE16 → T2
PC → ALU_A
+1 → ALU_B
ALU_OUT → PC
S16
PC → MEM_A
MEM_D → IR
T2 → ALU_B
RF_D1 → ALU_A
ALU_OUT → T1
S27
T1 → MEM_A
MEM_D → RF_D3
S17

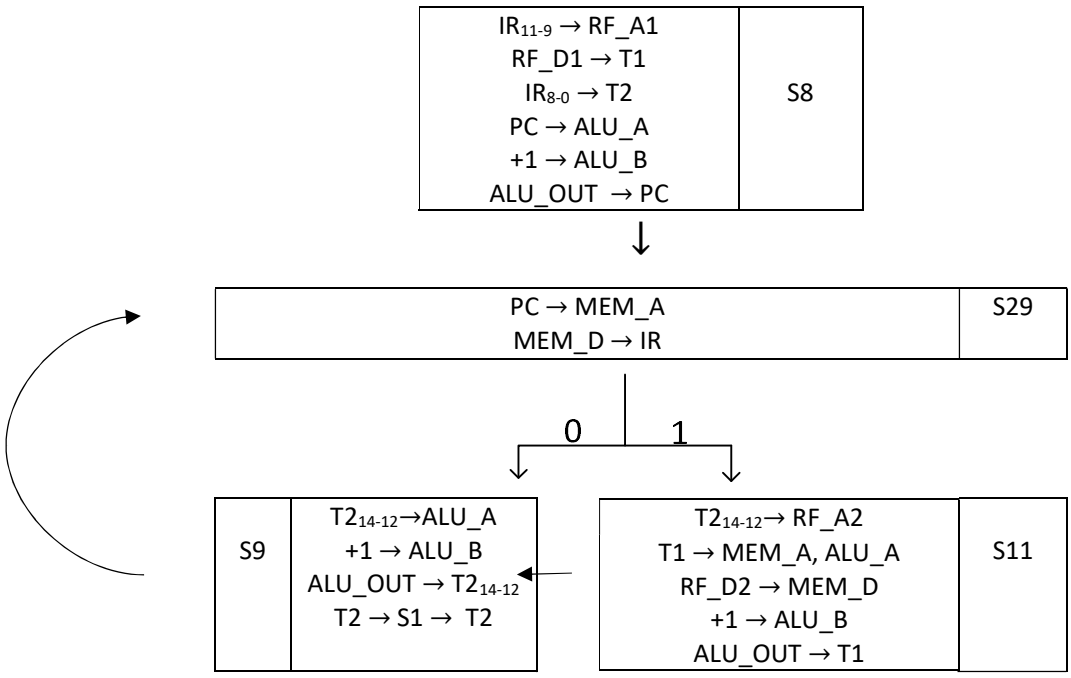
SW:


IR11-9 → RF_A2
IR8-6 → RF_A1
IR5-0 → SE16 → T2
PC → ALU_A
+1 → ALU_B
ALU_OUT → PC
S13
PC → MEM_A
MEM_D → IR
T2 → ALU_B
RF_D1 → ALU_A
ALU_OUT → T1
S14
T1 → MEM_A
RF_D2 → MEM_D
S15

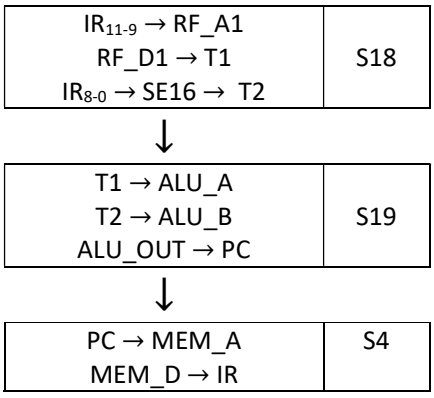
LM:


IR11-9 → RF_A1
RF_D1 → T1
IR8-0 → S16 → T2
PC → ALU_A
+1 → ALU_B
ALU_OUT → PC
S8
PC → MEM_A
MEM_D → IR
S29
T2_0
0
1
S9
T214-12 →ALU_A
+1 → ALU_B
ALU_OUT → T214-12
T2 → S1 → T2
T214-12 → RF_A3
T1 → MEM_A, ALU_A
MEM_D → RF_D3
+1 → ALU_B
ALU_OUT → T1
S10

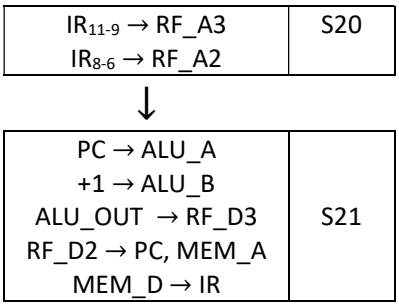
SM:


IR11-9 → RF_A1
RF_D1 → T1
IR8-0 → T2
PC → ALU_A
+1 → ALU_B
ALU_OUT → PC
S8
PC → MEM_A
MEM_D → IR
S29
0
1
S9
T214-12→ALU_A
+1 → ALU_B
ALU_OUT → T214-12
T2 → S1 → T2
T214-12→ RF_A2
T1 → MEM_A, ALU_A
RF_D2 → MEM_D
+1 → ALU_B
ALU_OUT → T1
S11

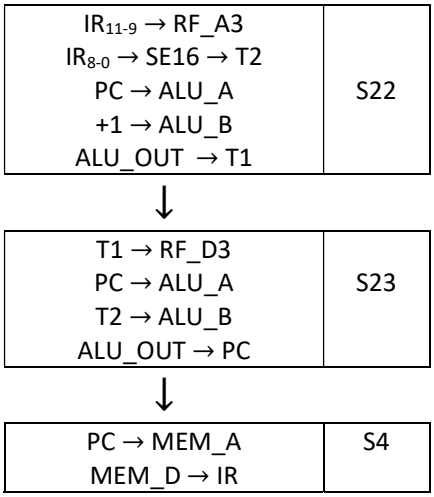
JRI:


IR11-9 → RF_A1
RF_D1 → T1
IR8-0 → SE16 → T2
S18
T1 → ALU_A
T2 → ALU_B
ALU_OUT → PC
S19
PC → MEM_A
MEM_D → IR
S4

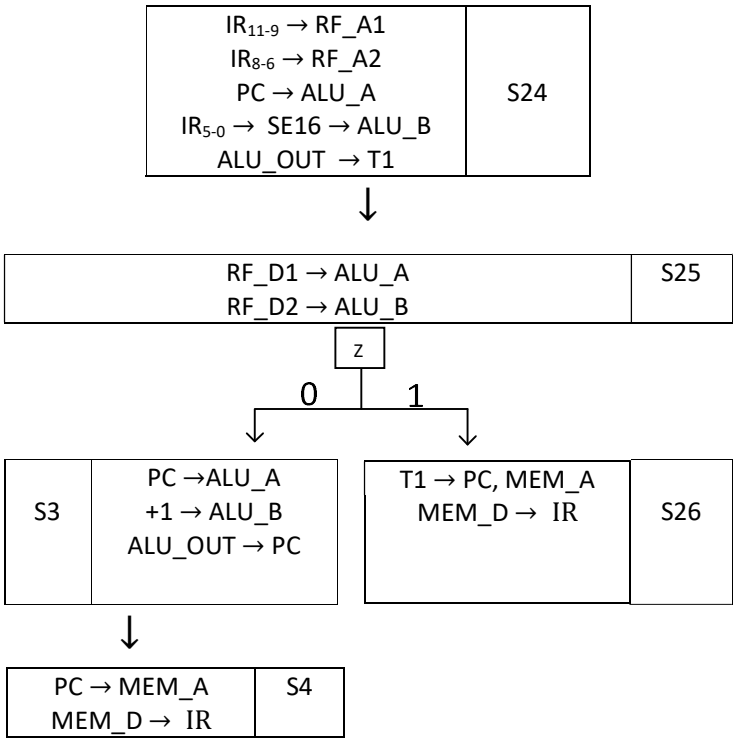
JLR:


IR11-9 → RF_A3
IR8-6 → RF_A2
S20
PC → ALU_A
+1 → ALU_B
ALU_OUT → RF_D3
RF_D2 → PC, MEM_A
MEM_D → IR
S21

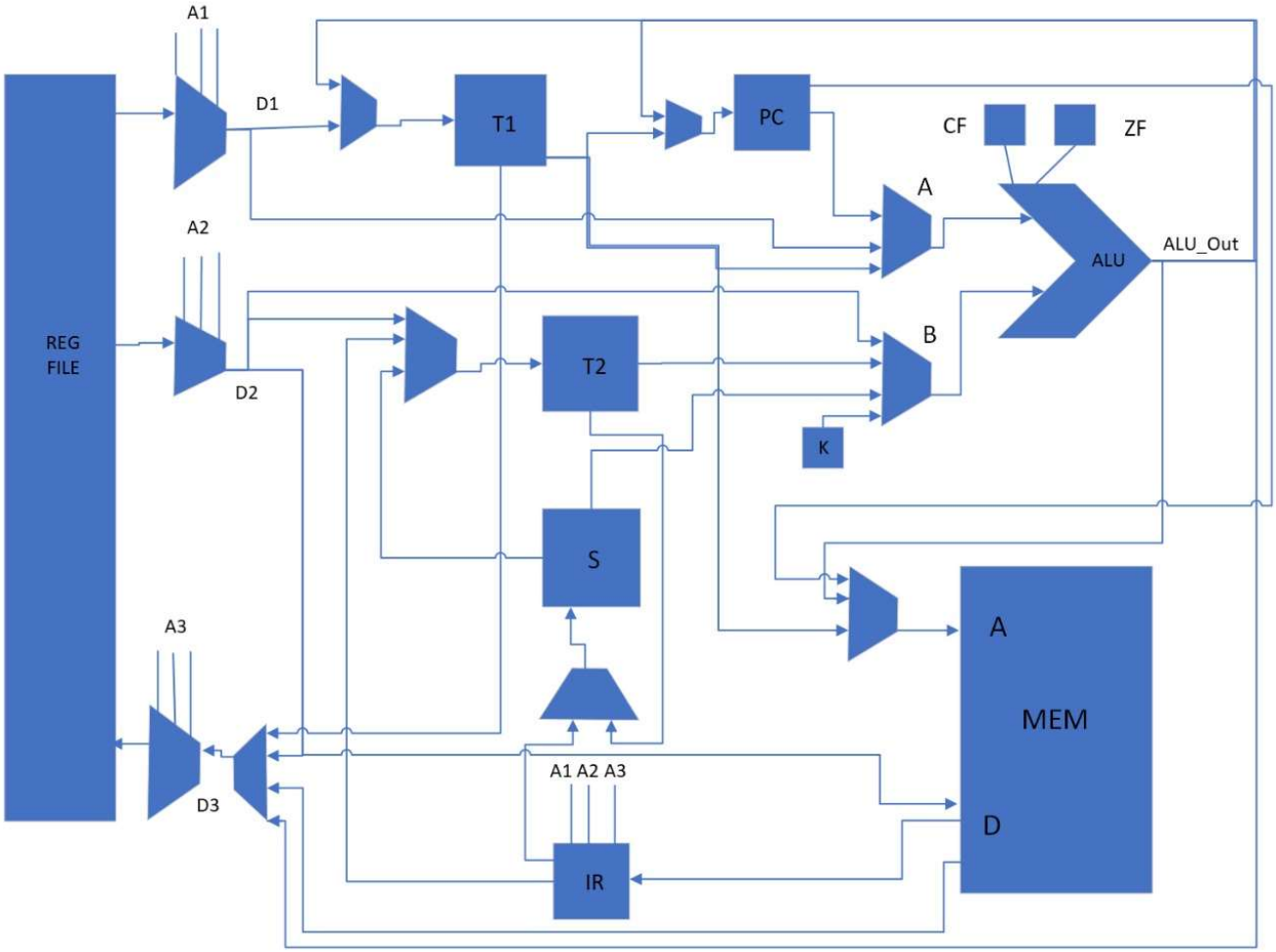
JAL:


IR11-9 → RF_A3
IR8-0 → SE16 → T2
PC → ALU_A
+1 → ALU_B
ALU_OUT → T1
S22
T1 → RF_D3
PC → ALU_A
T2 → ALU_B
ALU_OUT → PC
S23
PC → MEM_A
MEM_D → IR
S4

BEQ:

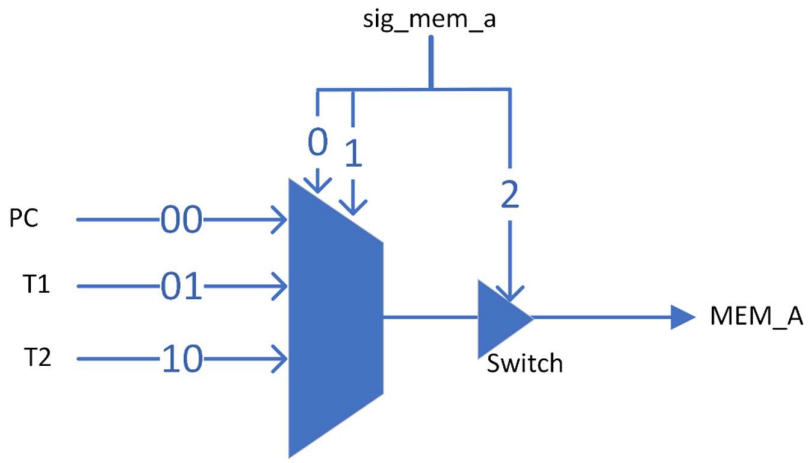

IR11-9 → RF_A1
IR8-6 → RF_A2
PC → ALU_A
IR5-0 → SE16 → ALU_B
ALU_OUT → T1
S24
RF_D1 → ALU_A
RF_D2 → ALU_B
S25
Z
0
1
S3
PC →ALU_A
+1 → ALU_B
ALU_OUT → PC
T1 → PC, MEM_A
MEM_D → IR
S26
PC → MEM_A
MEM_D → IR
S4

DATAPATH


A1
D1
T1
PC
CF
ZF
A
A2
ALU
ALU_Out
REG
FILE
B
T2
D2
K
S
A3
A
MEM
A1 A2 A3
D3
D
IR

CONTROL WORD DECODER

MEM_A

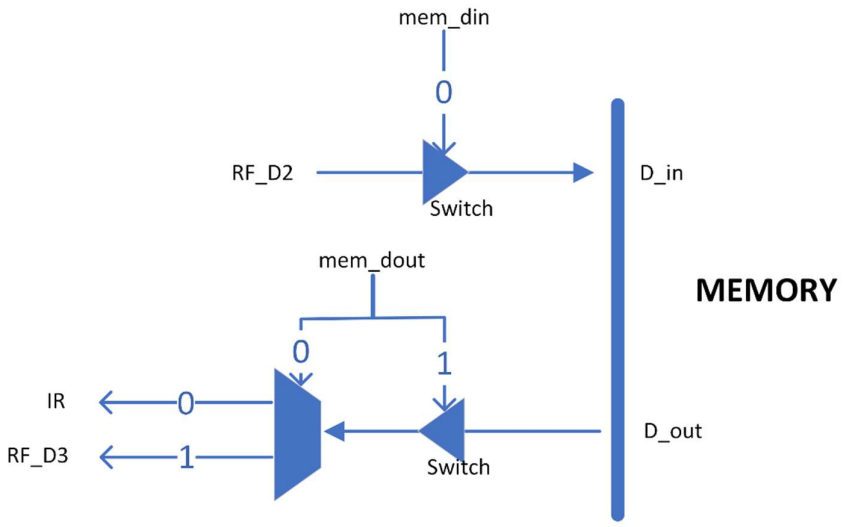


USAGE IN FLOWCHART	EXAMPLE STATE	CONTROL BITS (PQR)
PC → MEM_A	S4	000
RF_D2 → PC, MEM_A	S21	001
T1 → MEM_A	S26	010
T2 → MEM_A	S10	100
NONE	S8	110

Decoder Logic

SIG_MEM_A[1]	$P.\bar{Q}.\bar{R} + \bar{P}.\bar{Q}.R$
SIG_MEM_A[2]	$Q + R$
SIG_MEM_A[3]	$\bar{P}.\bar{Q} + \bar{Q}.\bar{R} + \bar{P}.\bar{R}$

MEM_D

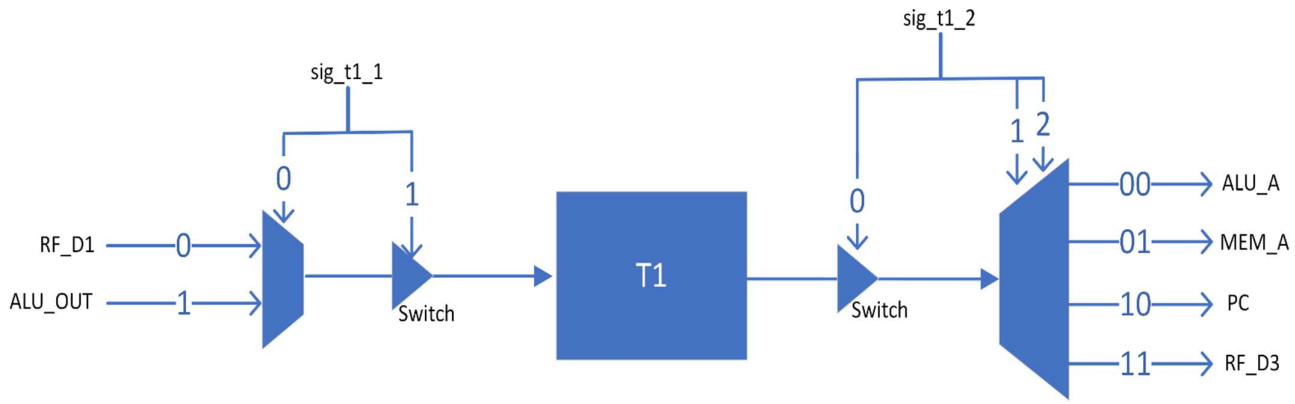


USAGE IN FLOWCHART	EXAMPLE STATE	CONTROL BITS (PQ)
MEM_D → IR	S4	00
MEM_D → RF_D3	S17	01
RF_D2 → MEM_D	S15	10
NONE	S1	11

Decoder Logic

SIG_MEM_DIN[1]	$P.\bar{Q}$
SIG_MEM_DOUT[2]	Q
SIG_MEM_DOUT[3]	$\bar{P}$

T1

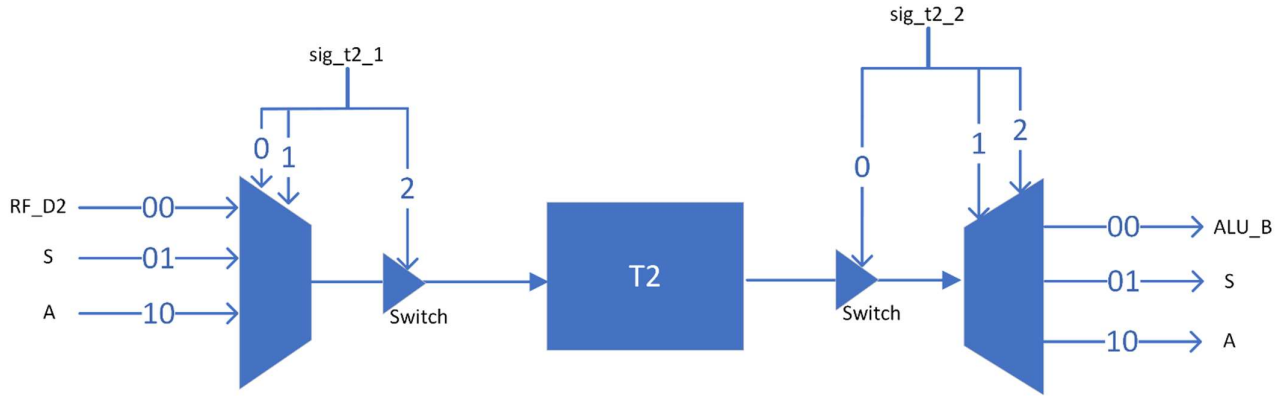


USAGE IN FLOWCHART	EXAMPLE STATE	CONTROL BITS (PQR)
RF_D1 → T1	S5	011
T1 → ALU_A	S2	001
ALU_OUT → T1	S27	100
T1 → MEM_A	S17	010
T1 → RF_D3	S23	101
T1 → PC, MEM_A	S26	110
NONE	S25	000

Decoder Logic

SIG_T1_1[1]	$P.\bar{Q}.\bar{R}$
SIG_T1_1[2]	$P.\bar{Q}.\bar{R} + \bar{P}.Q.R$
SIG_T1_2[3]	$Q\ xor\ R$
SIG_T1_2[4]	$P(Q\ xor\ R)$
SIG_T1_2[5]	$\bar{P}(Q\ xor\ R)$

T2

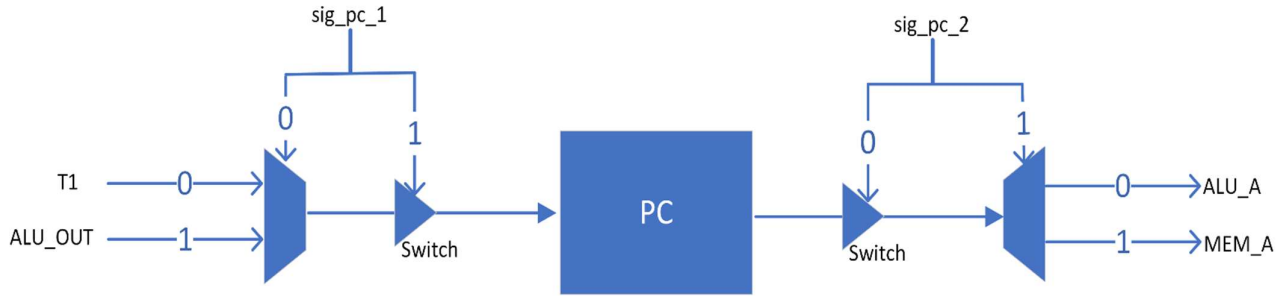


USAGE IN FLOWCHART	EXAMPLE STATE	CONTROL BITS (PQR)
RF_D2 → T2	S5	001
T2 → ALU_B	S2	010
T2 → S	S6	011
SE16 → T2	S7	100
IR8-0 → T2	S8	110
T2 → S1 → T2	S9	101
T2 → MEM_A, ALU_A ALU_OUT → T2	S10	111
NONE	S3	000

Decoder Logic

SIG_T2_1[1]	$P.Q$
SIG_T2_1[2]	$P + \bar{Q}.R$
SIG_T2_2[3]	$\bar{P}.Q + Q.R + P.R$
SIG_T2_2[4]	$(P\ xor\ Q)R$
SIG_T2_1[5]	$P(Q\ xnor\ R)$

PC

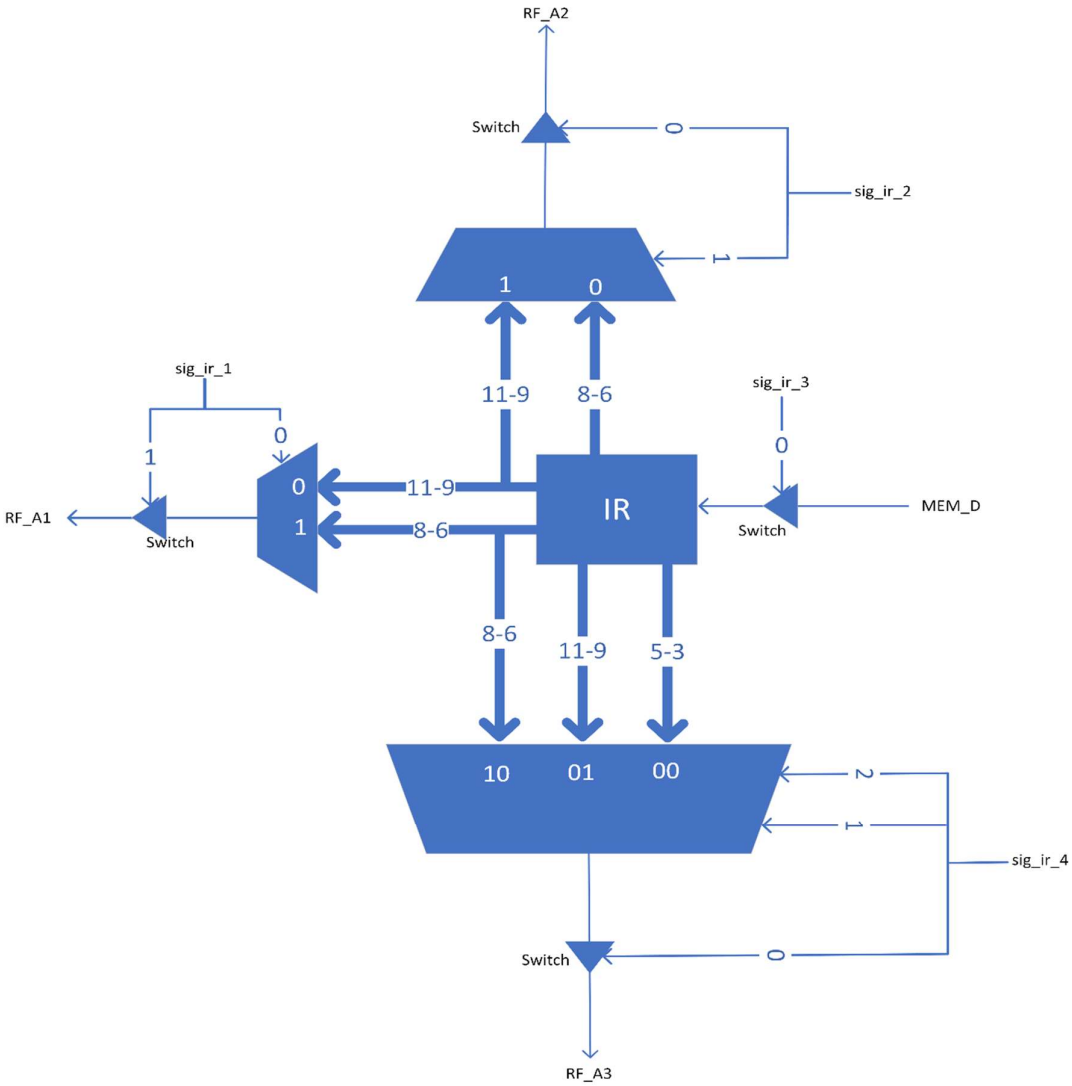


USAGE IN FLOWCHART	EXAMPLE STATE	CONTROL BITS (PQR)
PC → ALU_A ALU_OUT → PC	S1	110
PC → MEM_A	S2	010
PC → ALU_A	S22	011
ALU_OUT → PC	S19	001
T1 → PC	S26	100
RF_D2 → PC	S21	101
NONE	S5	000

Decoder Logic

SIG_PC_1[1]	$\bar{P}.\bar{Q}.R + P.Q.\bar{R}$
SIG_PC_1[2]	$P.\bar{R} + \bar{Q}.R$
SIG_PC_2[3]	$\bar{P}.Q + Q.\bar{R}$
SIG_PC_2[4]	$\bar{P}.Q.\bar{R}$

IR

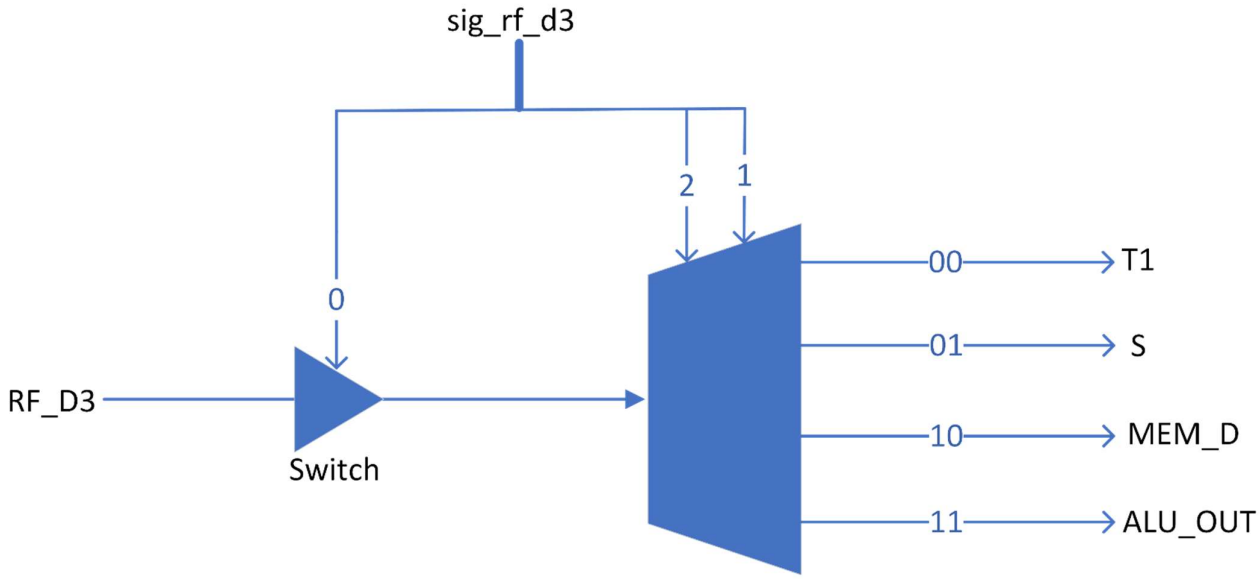


USAGE IN FLOWCHART	EXAMPLE STATE	CONTROL BITS (PQRS)
IR11-9 → RF_A1 IR8-6 → RF_A2 IR5-3 → RF_A3	S5	0001
MEM_D → IR	S4	0010
IR11-9 → RF_A1 IR8-6 → RF_A2 IR5-0 → SE16 → T2	S7	0011
IR11-9 → RF_A3 IR8-0 → S7 → RF_D3	S12	0100
IR11-9 → RF_A1 IR8-0 → T2	S8	0110
IR11-9 → RF_A1 IR8-0 → SE16 → T2	S18	0111
IR11-9 → RF_A3 IR8-6 → RF_A2	S20	1000
IR11-9 → RF_A3 IR8-0 → SE16 → T2	S22	1001
IR11-9 → RF_A2 IR8-6 → RF_A1 IR5-0 → SE16 → T2	S13	1011
NONE	S17	0000

Decoder Logic

SIG_IR_1[1]	$P + \bar{Q}.S + Q.R$
SIG_IR_1[2]	$\bar{P}.\bar{Q}.S + \bar{Q}.R.S + \bar{P}.Q.R$
SIG_IR_2[3]	$\bar{P}.\bar{Q}.S + \bar{Q}.R.S + \bar{P}.Q.R.\bar{S}$
SIG_IR_4[4]	$P.\bar{Q}.\bar{R} + \bar{P}.Q.\bar{R}.\bar{S}$
SIG_IR_4[5]	$\bar{Q}.\bar{R}.S + P.\bar{Q}.\bar{R} + \bar{P}.Q.\bar{R}.\bar{S}$
SIG_IR_3[6]	$\bar{P}.\bar{Q}.\bar{R}.S$

RF_D3

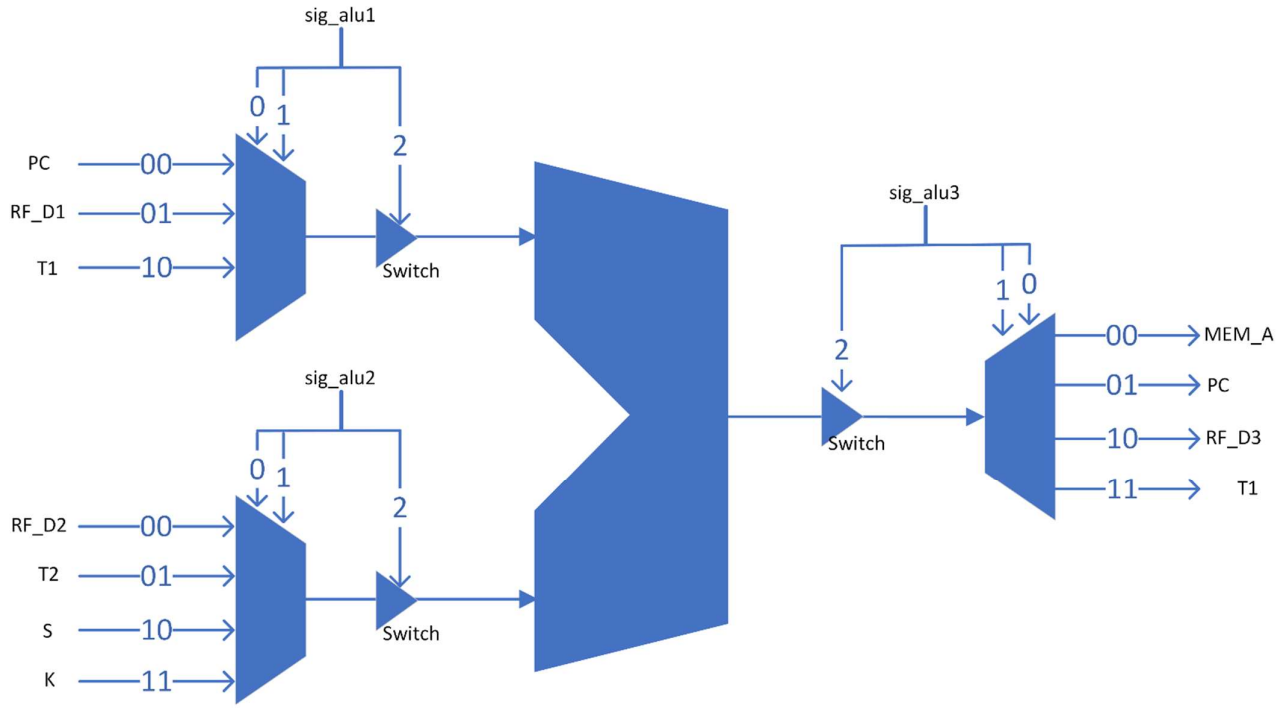


USAGE IN FLOWCHART	EXAMPLE STATE	CONTROL BITS (PQ)
MEM_D → RF_D3	S10	11
ALU_OUT → RF_D3	S21	01
T1 → RF_D3	S23	00
NONE	S4	10

Decoder Logic

SIG_RF_D3[1]	Q
SIG_RF_D3[2]	$\bar{P}.Q$
SIG_RF_D3[3]	$\bar{P} + Q$

ALU



USAGE IN FLOWCHART	EXAMPLE STATE	CONTROL BITS (PQRS)
PC → ALU_A +1 → ALU_B ALU_OUT → PC	S1	0000
T1 → ALU_A T2 → ALU_B ALU_OUT → RF_D3	S2	0001
T2 → ALU_B RF_D1 → ALU_A ALU_OUT → T1	S27	0011
T1 → MEM_A, ALU_A +1 → ALU_B ALU_OUT → T1	S10	1011
T1 → ALU_A T2 → ALU_B ALU_OUT → PC	S19	0100
PC → ALU_A +1 → ALU_B ALU_OUT → RF_D3	S21	0101
PC → ALU_A +1 → ALU_B ALU_OUT → T1	S22	0110
PC → ALU_A T2 → ALU_B ALU_OUT → PC	S23	0111
PC → ALU_A IR5-0 → SE16 → ALU_B ALU_OUT → T1	S24	1000
RF_D1 → ALU_A RF_D2 → ALU_B	S25	1001
NONE	S4	1010

Decoder Logic

SIG_ALU1[1]	$Q.\bar{R}.\bar{S} + P.R.S + \bar{P}.\bar{Q}.\bar{R}.S$
SIG_ALU1[2]	$\bar{P}.\bar{Q}.R$
SIG_ALU1[3]	$\bar{P}.\bar{R} + \bar{P}.Q + \bar{P}.S + P.\bar{Q}$
SIG_ALU2[4]	$\bar{Q}.\bar{R}.\bar{S} + \bar{P}.R.\bar{S} + P.R.S + Q.\bar{R}.S$
SIG_ALU2[5]	$\bar{P} + R.S$
SIG_ALU2[6]	$\bar{P}.\bar{R} + \bar{P}.Q + \bar{P}.S + P.\bar{Q}$
SIG_ALU3[7]	$\bar{P}.\bar{R} + \bar{P}.Q + \bar{Q}.R.S + P.\bar{Q}.\bar{S}$
SIG_ALU3[8]	$P.\bar{R}.\bar{S} + \bar{P}.\bar{R}.S + \bar{P}.R.\bar{S} + \bar{Q}.R.S$
SIG_ALU3[9]	$\bar{P}.\bar{S} + \bar{R}.\bar{S} + R.S$

THE CONTROL STORE

States	IR				RF_D3		MEM_A			PC			MEM_D		S			T1			ALU				T2				Next State				
S1	0	0	0	1	1	0	1	1	0	1	1	0	1	1	1	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	1	0
S2	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	0	1	0	0	X	X	X	X	X
S3	0	0	0	0	1	0	1	1	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	Branch Control				
S4	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	X	X	X	X	X
S5	0	0	0	1	1	0	1	1	0	0	0	0	1	1	1	0	0	0	1	1	1	0	1	0	0	0	1	0	0	0	0	1	0
S6	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	1	1	0	0	1	0	0	1	0	0	1	1	0	X	X	X	X	X
S7	0	0	1	1	1	0	1	1	0	1	1	0	1	1	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	0
S8	0	1	1	0	1	0	1	1	0	1	1	0	0	0	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1	0	1
S9	0	0	0	0	1	0	1	1	0	0	0	0	1	1	0	0	1	0	0	0	1	0	1	0	1	0	1	0	Branch Control				
S10	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	1	1	1	1	1	1	0	1	0	0	1
S11	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	1	1	1	1	1	0	1	0	0	1
S12	0	1	0	0	0	0	1	1	0	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
S13	1	0	1	1	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0
S14	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	1	0	1	0	0	0	1	1	1	1
S15	0	0	0	0	1	0	0	1	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	0	0	0	0	0	X	X	X	X	X
S16	0	1	0	1	1	0	1	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	1	1
S17	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	1	0	1	0	1	0	0	0	0	0	X	X	X	X	X
S18	0	1	1	1	1	0	1	1	0	0	0	0	1	1	1	0	1	0	1	1	1	0	1	0	1	0	0	0	1	0	0	1	1
S19	0	0	0	0	1	0	1	1	0	0	0	1	1	1	1	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	1	0	0
S20	1	0	0	0	1	0	1	1	0	0	0	0	1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	1
S21	0	0	1	0	0	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	X	X	X	X	X
S22	1	0	0	1	1	0	1	1	0	0	1	1	1	1	1	0	1	1	0	0	0	1	1	0	1	0	0	0	1	0	1	1	1
S23	0	0	0	0	0	0	1	1	0	1	1	0	1	1	1	0	0	1	0	1	0	1	1	1	0	1	0	0	0	0	1	0	0
S24	1	0	1	0	1	0	1	1	0	0	1	0	1	1	0	1	1	1	0	0	1	0	0	0	0	0	0	0	1	1	0	0	1
S25	0	0	0	0	1	0	1	1	0	0	1	1	1	1	1	0	0	0	0	0	1	0	0	1	0	0	0	0	Branch Control				
S26	0	0	1	0	1	0	0	1	0	1	0	0	0	0	1	0	0	1	1	0	1	0	1	0	0	0	0	0	X	X	X	X	X
S27	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	1	0	1	0	0	1	0	0	0	1
S28	0	0	0	1	1	0	1	1	0	1	1	0	1	1	1	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	1	1	0
S29	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	Branch Control				