

Introduction to C7x DSP

**Automotive Processor Business,
Texas Instruments**

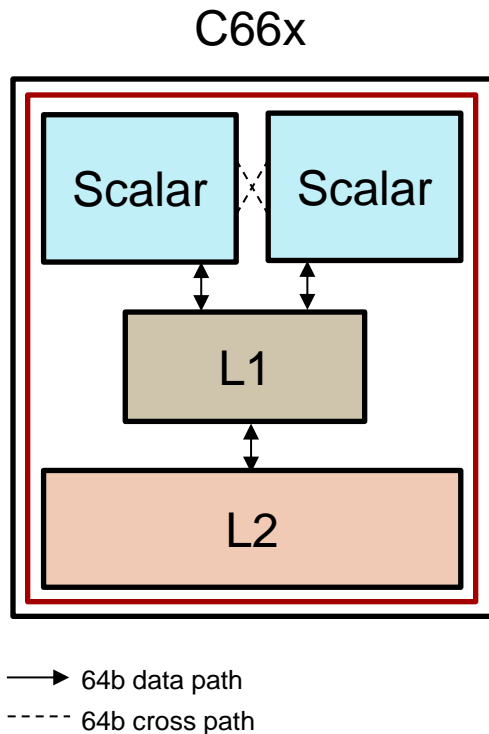
Outline

- C66x DSP today
- A bird's eye view of C7x DSP
- Under the hood of C7x DSP
 - Data path
 - Functional Units
 - Register File
 - Streaming Engine
 - Memory
 - LUT/Histogram
 - ISA



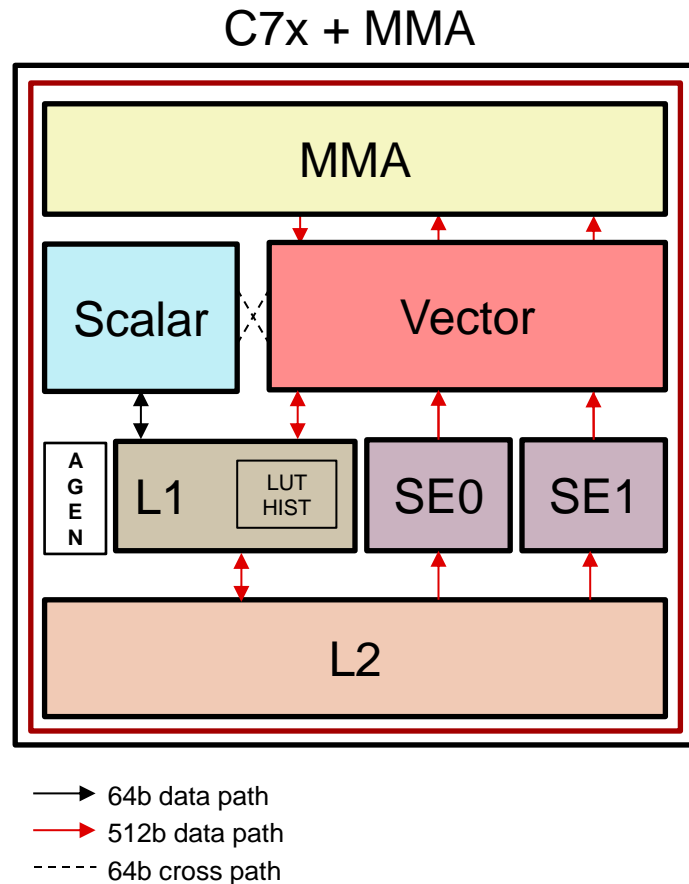
C66x DSP today

- True 32b floating point DSP
- Programmable functional units (.L1/.L2, .S1/.S2, .M1/.M2, .D1/.D2)
- Global register files (32x2, 32bit registers)
- Cache based memory system (L1D – 32KB, L1P-32KB, L2 – 256KB)
- Dual 64bit data-paths
- Packed SIMD operations (8bit, 16bit, 32bit, 64bit)
- Supports 16bit/32bit complex types
- Supports 128bit vector types (Quad 32bit)
- Supports 32 16bit multiply-accumulate per cycle
- Supports 16 single precision operations per cycle
- Supports 40bit operations
- Software pipelining, special SPLOOP HW



A bird's eye view

- True 64b DSP with dual data paths
- Programmable functional units
- Global and local register files
- Cache based memory system (L1, L2)
- Streaming Engine (SE0, SE1)
- Address generators (AGEN)
- Lookup table/Histogram (LUT, HIST)
- Matrix Multiply Accelerator (MMA) – bolt on



Under the hood

- **Data paths**

- Scalar path – 64 bits
- Vector path – 512 bits
- Cross path – 64 bits

- C7x Load-Store to L1

- 64 bits load || 64 bits store
- 64 bits load || 512 bits store
- 512 bits load || 64 bits store
- 512 bits load || 512 bits store

- C7x Load using SE from L2

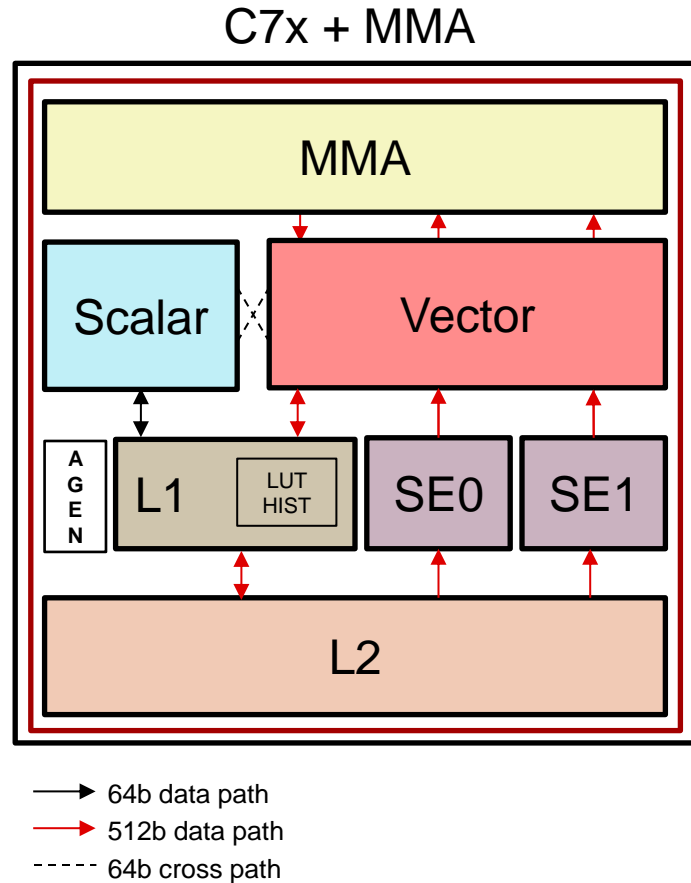
- “Read Only” 2 x 512 bits

- MMA Load using SE from L2

- “Read Only” 2 x 512 bits

- MMA Store using vector path to L1

- 512 bits store

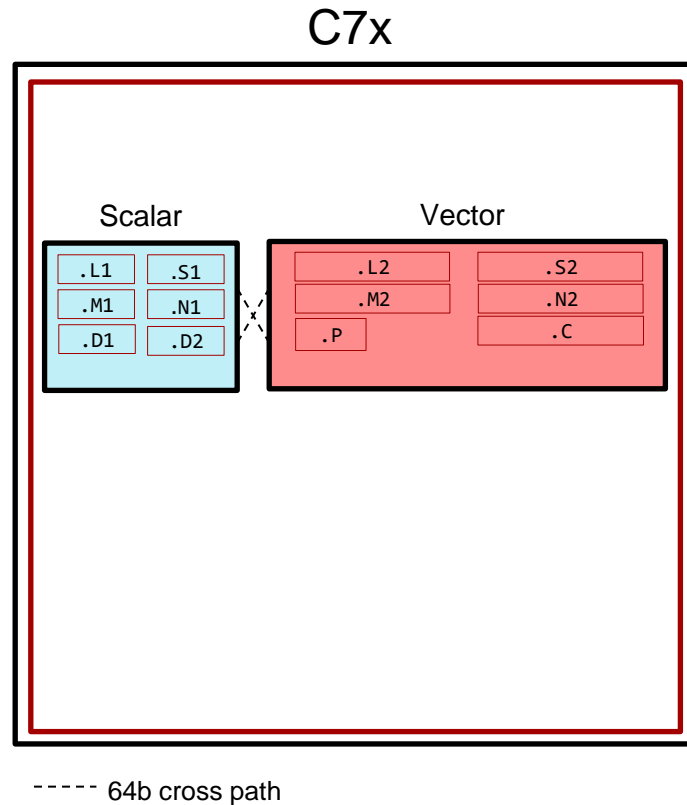


Under the hood

• Functional Units (13)

- .L1/.L2 – Add/Sub/Move/Logical/Bitwise/Shift
- .S1/.S2 – Add/Sub/Move/Logical/Bitwise/Shift
- .M1/.M2 – Add/Sub/Multiply
- .N1/.N2 – Multiply
- .D1/.D2 – Load/Store/LUT/HIST
- .C – Add/Permute/DOTP/SAD
- .P – Vector predication
- .B – Branch Predictor

Operation	Performance
16b fixed point MAC	128 MAC/cycle
32b multiply	32 multiply/cycle
32b Float ops	80 ops/cycle
8bit SAD	512 sad/cycle

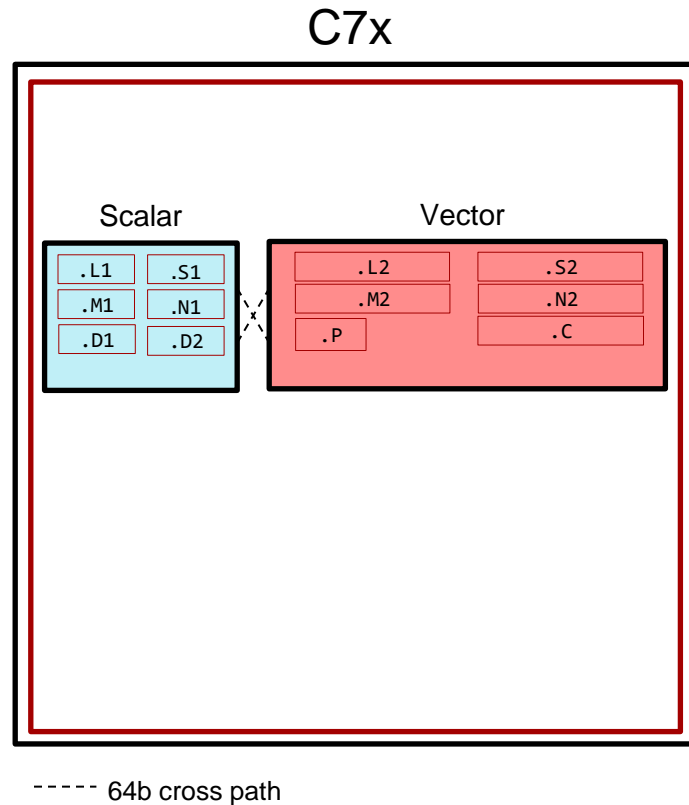


Under the hood

- Register file

Type	Scalar (64b)	Vector (512b)
Global registers all units	16	16
Local shared registers .L/.S	8	8
Local shared registers .M/.N/.C	8	8
Local shared registers .D1/.D2	8	NA
Predicate registers for .P	NA	8 (64b)

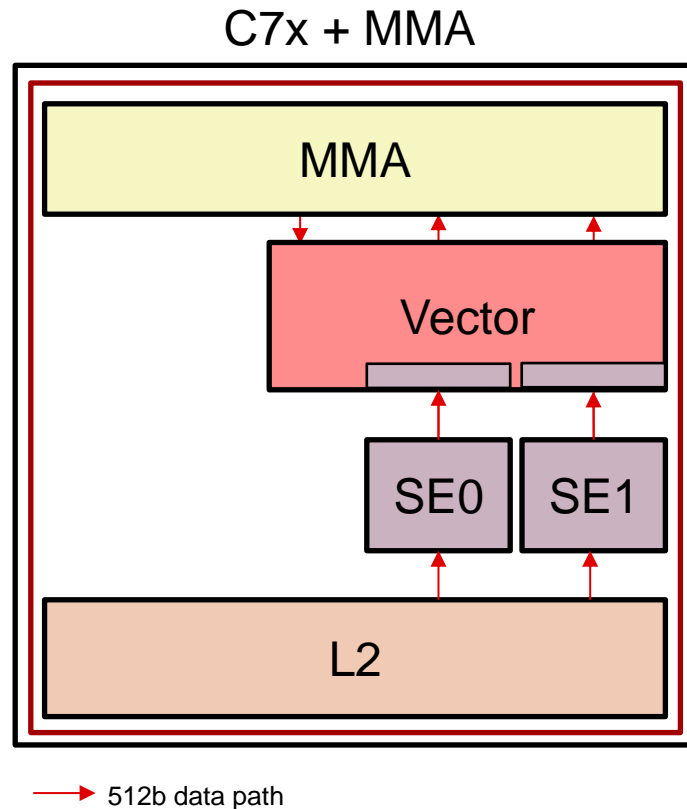
- Registers in scalar/vector side can be read via cross path but not written to
- Scalar instructions can access lower 64bits of Vector side registers



Under the hood

- **Streaming Engine**

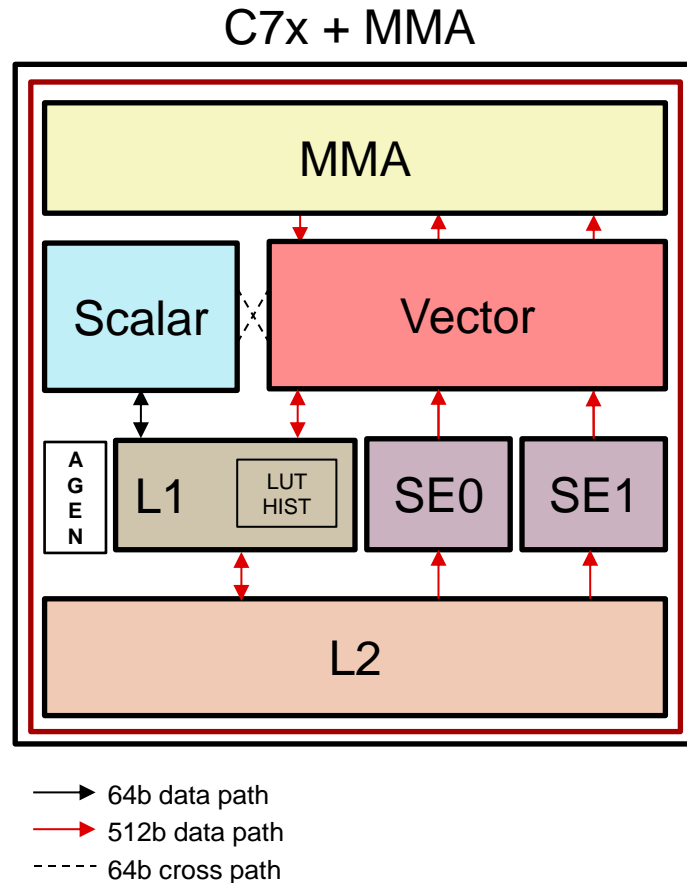
- Data forwarding engine not transfer engine
 - Forwards data from L2 and beyond directly to CPU boundary (C7x) or MMA memories (A and B)
- Data formatting engine
 - Supports element promotion, decimation, duplication, transpose loads, predication
- Provides 6D addressing
 - Access patterns up-to 6D can be programmed ahead.
 - 6D data is presented as 512bit vector per cycle.
- Communicates with L2 memory controller for requests beyond L2 (L3, DDR)
- Coherent with L1D data at stream open/close boundaries.
- It's a "Read Only" engine which feeds only vector path
- Local cache (2KB) for reduced traffic at L2



Under the hood

- **Memory**

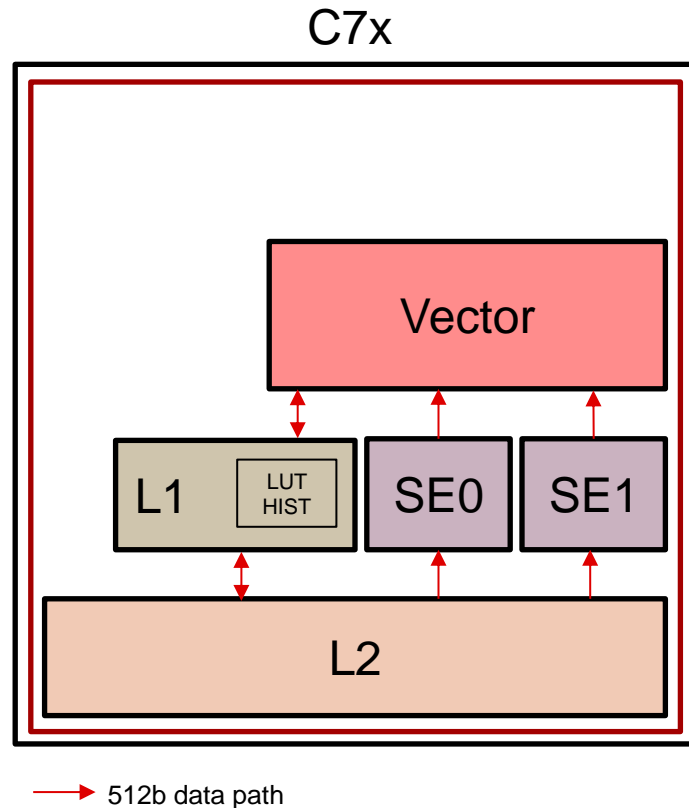
- Level 1 memory (L1) at CPU clock
 - Program memory (L1P) 32kb
 - Data memory (L1D) 48kb
 - Separate 16 x 512b entry victim cache for stores
 - 1024b data throughput, 16 x 64b banks
 - ECC mode SECDED
- Level 2 memory (L2) at CPU clock
 - Unified memory 512kb
 - Supports 4 masters (L1, SE0, SE1, DMA)
 - 2048b data throughput, 4 x 512b banks with 2 virtual banks each
 - ECC mode SECDED
- Cache modes
 - L1P – 32kb (max) no SRAM mode
 - L1D - 32kb (max), 8kb (min) remaining as SRAM
 - L2 - 64kb (min) to 512kb (max)



Under the hood

- **Lookup Table, Histogram**

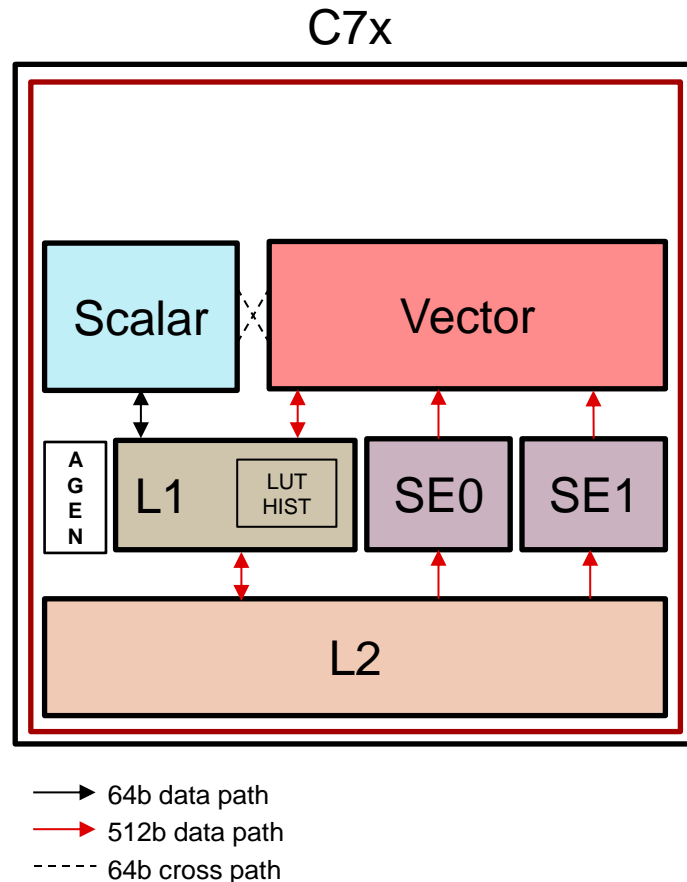
- Implemented in L1D, uses 16 x 64b banks
- Data and Index supplied by registers or SE
- Lookup table
 - Lookup in powers of 2 (1, 2, 4, 8, 16)
 - Supports - 8b, 16b, 32b
 - Table size (0.5KB, 1KB, 2KB, 4KB, 8KB, 16KB, 32KB)
 - Table size depends on number of ways
 - Eg. 16KB L1D SRAM split in 16 ways provides 1KB per way.
 - Number of bins depends on data type.
 - Eg. For 8b, 1KB table == 1024 bins
 - 1024 bit / cycle table initialization
- Histogram
 - Supports 16 way histogram,
 - Supports – 8b, 16b, 32b
 - Supports weighted histogram



Under the hood of C7x DSP

• ISA

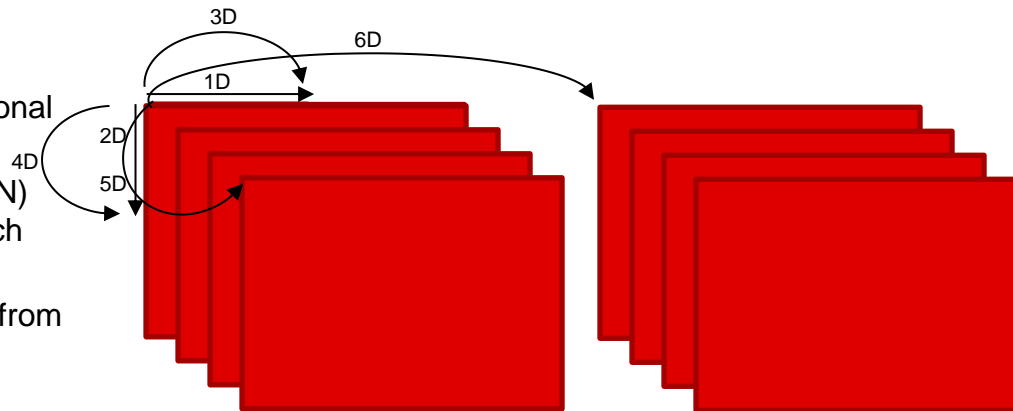
- Arithmetic, Shift, Logical instructions
- Fixed point, Floating point, Complex type multipliers
- Horizontal SIMD instructions, ADD, MIN/MAX
- Byte permutation across SIMD lanes
- Dedicated FIR instructions
 - FIR4 (4 tap), FIR8 (8 tap)
- Dedicated DOTP instructions
 - DOTP2, DOTP4, DOTP8, DOTPMPN (flexible)
- Sum of Absolute Differences (SAD)
 - 512 – 8bit, 256 16bit with stride support
- SORT16 instruction, ascending/descending
- Galois Field multiply functions
- WCDMA “Rake and Search” instructions
 - Up to 512 2-bit PN * 8-bit I/Q complex multiplies



Under the hood

- **Address generators (AGEN)**

- Computer vision applications have multi-dimension access patterns which take up registers and functional units
- C7x core has dedicated Address GENERator (AGEN) unit which computes multi dimensional offsets which can be used with regular load/store instructions
- Up to 4 AGEN units supported in each core. Apart from 2 in Streaming Engine.
- Supports up to 6D addressing



$$\text{offset} = \text{ICNT0} + \text{ICNT1} * \text{DIM1} + \text{ICNT2} * \text{DIM2} + \dots$$
$$\text{val} = \text{pSrc}[\text{offset}]$$

C66x vs C7x - Summary

	C66x DSP	C7x DSP
DSPTYPE	True 32 bit 32bit/64bit floating point types 6bit/32bit complex types	True 64 bit 32bit/64bit floating point types 6bit/32bit complex types
Functional Units	8 functional units (.L1/.L2, .S1/.S2, .M1/.M2, .D1/.D2)	12 functional units (.L1/.L2, .S1/.S2, .M1/.M2, .N1/.N2, .D1/.D2, .C, .P)
Data paths	2 x 64 bit , 64 bit cross path	64 bit + 512 bit + 2x512 (read only), 64 bit cross path
Registers	32x2 – 32 bit registers	16-64 bit global, 24-64 bit local, 16-512 bit global, 24-512 bit local, 8-64 bit local (.P)
Cache	32KB L1P + 32KB L1D, 256KB L2	32KB L1P + 32KB L1D + 16KB L1SRAM, 512KB L2
Multipliers	32 -16bit fixed, 8 – 32bit fixed / floating	128 - 16bit fixed, 32 – 32bit fixed / floating
Operations	32-GMAC, 16-GFLOPS at 1 GHz	128-GMAC*, 80-GFLOPS at 1 GHz
Transfer engines	IDMA (2 channels), 1D – 32bit	Streaming Engines (2 sets), 6D – 512bit, read-only
Coherency	Coherent with L2	Fully coherent with L2, L3, DDR
Safety	ECC – SED, L1	ECC – SECCDED, L1/L2, SE FIFO
SIMD	Packed SIMD (8b, 16, 32b, 64bit) Inter or Vertical SIMD (.L, .S, .M, .D)	Packed SIMD (8b, 16, 32b, 64bit) Inter or Vertical SIMD (.L, .S, .M, .N, .C, .D) Intra or Horizontal SIMD (.C)
HW Acceleration	SPLOOP HW	NLC (Nested Loop Controller), branch predictor Lookup Table, Histogram

*Excluding MMA mac