.wrap_target

bitloop:

    out x,1   side 0 $[T_3-1]$ L.1

    jmp !x do_zero side 1 $[T_1-1]$ L.2

do_one:

    jmp bitloop side 1 $[T_2-1]$ L3

do_zero:

    nop   side 0 $[T_2-1]$ L4

.wrap

$$L_1 \rightarrow L_2 \rightarrow L_3$$
$$\searrow L_4$$
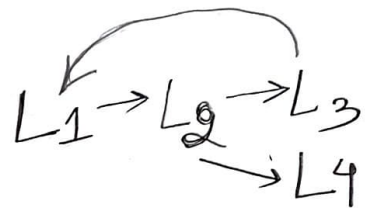
Loop

Current Instruct?	Is Data in FIFO (Y/N)	Is SM stalled? (Y/N)	no. of delay cycles	Value of OSR Register	Value of SMX	LED pin state
L1	Y	N	2	0x 007F8000	0	0
L2	Y	N	1	0X 007F8000	0	1
L3	Y	N	4	0X 007F8000	0	0
L4	Y	N	2	0X 003FC000	0	0

for 0
1 2 3 4 5 6 7 8 9 10 11 12 13
$\leftarrow T_3 \rightarrow | \leftarrow T_1 \rightarrow | \leftarrow \quad T_2 \quad \times \quad T_3 \rightarrow$

for 1
1 2 3 4 5 6 7 8 9 10 11 12 13