Design and Implementation of a 5-bit Carry Look-Ahead Adder using 180nm CMOS Technology

VLSI Design Course Project – Monsoon 2025

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***Abstract*—This project presents the design, simulation, and implementation of a 5-bit Carry Look-Ahead (CLA) adder using 180nm CMOS technology. The adder is designed to operate at $V_{DD} = 1.8V$ with equal NMOS and PMOS channel lengths. The design methodology includes circuit-level simulations using NGSPICE, physical layout using MAGIC layout editor with SCN6M_DEEP.09.tech27 technology file, post-layout extraction and verification, Verilog HDL implementation, and FPGA prototyping. The complete design flow from schematic to pose layout is documented with emphasis on timing analysis, and area optimization. The maximum operating frequency achieved is 1281 MHz with a worst-case delay of 609.2ps.**

***Index Terms*—Carry Look-Ahead Adder, CLA, CMOS VLSI, 180nm technology, NGSPICE, MAGIC layout, Verilog HDL, FPGA implementation**

I. Introduction

Addition is one of the fundamental arithmetic operations in digital systems, forming the basis for more complex operations such as multiplication, division, and address calculation. The speed of the adder directly impacts the overall performance of processors, digital signal processors (DSPs), and application-specific integrated circuits (ASICs).

A. Motivation

The Carry Look-Ahead (CLA) adder addresses the primary limitation of ripple-carry adders: the propagation delay through the carry chain. By computing carry signals in parallel using generate and propagate functions, CLA adders achieve significantly reduced delay at the cost of increased hardware complexity.

B. Project Objectives

The main objectives of this project are:

- Design a 5-bit CLA adder with optimized performance
- Implement the design using 180nm CMOS technology
- Perform comprehensive simulations at both schematic and post-layout levels
- Create physical layout following DRC rules
- Implement and verify the design using Verilog HDL
- Prototype the design on FPGA hardware
- Analyze timing,clock speed and area characteristics

II. Background and Theory

A. Carry Look-Ahead Adder Concept

For two n-bit numbers $A = a_{n-1}a_{n-2}...a_1a_0$ and $B = b_{n-1}b_{n-2}...b_1b_0$, the sum and carry at each bit position can be computed using:

$$s_i = a_i \oplus b_i \oplus c_i \tag{1}$$

$$c_{i+1} = a_i \cdot b_i + (a_i \oplus b_i) \cdot c_i \tag{2}$$

The CLA approach defines two functions for each bit position:

- **Generate**: $g_i = a_i \cdot b_i$ (carry is generated regardless of c_i)
- **Propagate**: $p_i = a_i \oplus b_i$ (carry is propagated if $c_i = 1$)

The carry can be expressed as:

$$c_{i+1} = g_i + p_i \cdot c_i \tag{3}$$

For a 5-bit adder with carry-in $c_{in} = c_0 = 0$, the carries can be expanded more easily than expected because cin=0. so, the last term for every carry boolean equation can be removed, the equations are:

$$c_1 = g_0 + p_0 \cdot c_{in} = g_0 \tag{4}$$

(5)

Similarly,

$$c_2 = g_1 + p_1 \cdot g_0 \tag{6}$$
$$c_3 = g_2 + p_2 \cdot g_1 + p_2 \cdot p_1 \cdot g_0 \tag{7}$$
$$c_4 = g_3 + p_3 \cdot g_2 + p_3 \cdot p_2 \cdot g_1 + p_3 \cdot p_2 \cdot p_1 \cdot g_0$$
$$\begin{aligned} c_5 = g_4 &+ p_4 \cdot g_3 + p_4 \cdot p_3 \cdot g_2 + p_4 \cdot p_3 \cdot p_2 \cdot g_1 \\ &+ p_4 \cdot p_3 \cdot p_2 \cdot p_1 \cdot g_0 \end{aligned} \tag{8}$$

The sum bits are then computed as:

$$sum_i = p_i \oplus c_i, \quad i = 0, 1, 2, 3, 4 \tag{9}$$

where c_5 represents the carry-out (c_{out}) of the 5-bit adder.

III. Proposed Architecture

A. Overall Structure

The proposed 5-bit CLA adder consists of the following main blocks:

1) **Input D Flip-Flops**: 10 D flip-flops for registering the 5-bit inputs a (a_0 to a_4) and b (b_0 to b_4)
2) **Propagate and Generate Block**: Computes p_i and g_i for each bit position
3) **Carry Look-Ahead Logic**: Computes all carry signals in parallel
4) **Sum Block**: Computes the final sum bits
5) **Output D Flip-Flops**: 6 D flip-flops for registering the 5-bit sum (s_0 to s_4) and carry-out (c_5)

The design uses a total of **16 D flip-flops**: 10 for input registers and 6 for output registers.

Fig. 1: Block diagram of the 5-bit CLA adder

B. Timing Considerations

The design operates on a clock signal f_{clk} with period T_{clk}. Input bits are available before the rising edge, and output must be computed and available before the next rising edge. The critical path includes:

- D flip-flop clock-to-Q delay (t_{C2Q})
- Propagate/Generate logic delay
- Carry Look-Ahead logic delay (longest carry path)
- Sum computation delay
- D flip-flop setup time (t_{setup})

The minimum clock period is:

$$T_{clk,min} = t_{C2Q_{max}} + t_{pd_{CLA_{max}}} + t_{setup_{max}} \tag{10}$$

C. Design Hierarchy

The design follows a hierarchical approach with the following building blocks:

- Basic gates: Inverter, NAND2, NAND3, NAND4, NAND5
- Composite gates: XOR (using 4×NAND2), AND (NAND2 + Inverter)
- Functional blocks: P/G generators, CLA logic, sum generators
- Sequential elements: D flip-flops for input/output registers

IV. Circuit Design and Sizing

A. Design Specifications and Fundamental Parameters

The 5-bit CLA adder design is based on the following specifications and fundamental parameters:

Technology Specifications:

- Technology: 180nm CMOS process
- Supply Voltage (V_{DD}): 1.8V
- Minimum feature size: $\lambda = 0.09\mu m = 90nm$
- Channel Length: $L = 2\lambda = 0.18\mu m$ (uniform for all transistors)
- Output load: Inverter with $W_p/W_n = 20\lambda/10\lambda$

Transistor Sizing Methodology:

The sizing of PMOS and NMOS transistors is based on carrier mobility considerations. For the 180nm CMOS process:

- Mobility ratio: $\mu_n/\mu_p \approx 2$

To achieve equal rise and fall times in logic gates, the PMOS width should compensate for lower hole mobility. The PMOS-to-NMOS width ratio is:

$$k = \frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} \approx 2 \tag{11}$$

Therefore, the design uses $W_p = k \times W_n = 2 \times W_n$ for balanced switching characteristics.

Basic Inverter Sizing (Reference):

- NMOS width: $W_n = 20\lambda = 1.8\mu m$, $L = 2\lambda = 0.18\mu m$
- PMOS width: $W_p = 40\lambda = 3.6\mu m$, $L = 2\lambda = 0.18\mu m$

All other gates are sized relative to this basic inverter, with series NMOS transistors scaled by the number of devices in series to maintain equal drive strength.

B. Basic Gates Design and Sizing

1) NAND2 Gate: For a 2-input NAND gate, NMOS transistors in series require width scaling:

- PMOS (parallel): $W_p = 40\lambda$, $L = 2\lambda$
- NMOS (series): $W_n = 2 \times 20\lambda = 40\lambda$, $L = 2\lambda$

2) NAND3 Gate: For a 3-input NAND gate:

- PMOS (parallel): $W_p = 40\lambda$, $L = 2\lambda$
- NMOS (series): $W_n = 3 \times 20\lambda = 60\lambda$, $L = 2\lambda$

3) NAND4 Gate: For a 4-input NAND gate:

- PMOS (parallel): $W_p = 40\lambda$, $L = 2\lambda$
- NMOS (series): $W_n = 4 \times 20\lambda = 80\lambda$, $L = 2\lambda$

4) NAND5 Gate: For a 5-input NAND gate:

- PMOS (parallel): $W_p = 40\lambda$, $L = 2\lambda$
- NMOS (series): $W_n = 5 \times 20\lambda = 100\lambda$, $L = 2\lambda$

5) General Sizing Rule: For an n-input NAND gate:

$$W_{n,series} = n \times 20\lambda \quad (12)$$

$$W_{p,parallel} = 40\lambda \quad \text{(constant for all NAND gates)} \quad (13)$$

This scaling compensates for series resistance in the pull-down network, maintaining uniform delay across all gates.

TABLE I: Complete Gate Sizing Summary

Gate	NMOS W (λ)	PMOS W (λ)	L (λ)	W (μm)
Inverter	20	40	2	1.8/3.6
NAND2	40	40	2	3.6/3.6
NAND3	60	40	2	5.4/3.6
NAND4	80	40	2	7.2/3.6
NAND5	100	40	2	9.0/3.6

C. D Flip-Flop Design

1) Implementation Method Selection: Multiple implementation methods were evaluated for the D flip-flop design:

1) **Transmission Gate Based Flip-Flop**: Uses transmission gates for signal routing with complementary clocks
2) **Two CMOS Latches with Complementary Clock**: Traditional master-slave configuration requiring both CLK and $\overline{\text{CLK}}$
3) **True Single Phase Clock (TSPC) Flip-Flop**: Dynamic register using only a single clock phase

The **TSPC-based implementation** was selected due to:

- **Low Setup and Hold Times**: Single clock phase eliminates clock complementation delays
- **Reduced Area**: Requires only 9 transistors compared to 20-24 for transmission gate designs
- **Single Clock Phase**: Simplifies clock distribution and reduces power consumption
- **Faster Operation**: Reduced parasitics result in lower propagation delays

2) TSPC Operation and Timing Analysis: The TSPC flip-flop consists of three cascaded stages. Analysis of the circuit structure reveals:

Stage 1 (Input Stage): When CLK = 0, the input D propagates through this stage to node X. The propagation delay of this first stage determines the **setup time** (t_{setup}).

Stage 2 (Dynamic Stage): When CLK = 0, node Y precharges to V_{DD}. When CLK = 1, this stage evaluates based on X. The propagation delay of the second stage determines the **hold time** (t_{hold}). Note that hold time does not have a rise component because node Y is precharged to V_{DD}.

Stage 3 (Output Stage): When CLK = 1, the Y value propagates to output Q through the final inverter.

3) Timing Parameter Measurement Methodology: **A. Clock-to-Q Delay (t_{C2Q}):**

- Measured as the time difference between clock rising/-falling edges and output Q transitions
- Both rise ($t_{C2Q,rise}$) and fall ($t_{C2Q,fall}$) delays are measured
- Average value: $t_{C2Q,avg} = (t_{C2Q,rise} + t_{C2Q,fall})/2$

B. Setup Time (t_{setup}):

- Represents the propagation delay of the first stage (input to node X)
- Measurement: Fix CLK = 0 and measure propagation delay from input D to first stage output
- Both rise and fall transitions of the first block are measured with respect to input D

C. Hold Time (t_{hold}):

- Represents the propagation delay of the second stage (node X to node Y)
- Measurement: Fix first block output to V_{DD} and measure propagation delay of second block with respect to clock
- Only fall transition is measured since node Y is precharged to V_{DD}
- No rise component exists for this measurement

This flip-flop design is utilized throughout the 5-bit CLA adder: 10 flip-flops register the inputs (a_0 to a_4 and b_0 to b_4), and 6 flip-flops register the outputs (s_0 to s_4 and c_5).

4) Transistor Sizing: The TSPC D flip-flop transistor sizes are designed to ensure proper functionality and prevent race conditions:

TABLE II: TSPC D Flip-Flop Transistor Sizing

Transistor	Function	W (λ)	L (λ)
M1 (PMOS)	Stage 1: D input (P1)	80	2
M2 (PMOS)	Stage 1: CLK input (P2)	80	2
M3 (NMOS)	Stage 1: D input (N1)	20	2
M4 (PMOS)	Stage 2: CLK input (P3)	40	2
M5 (NMOS)	Stage 2: Node A input (N3)	40	2
M6 (NMOS)	Stage 2: CLK input (N2)	40	2
M7 (PMOS)	Stage 3: Node B input (P4)	40	2
M8 (NMOS)	Stage 3: CLK input (N4)	40	2
M9 (NMOS)	Stage 3: Node B input (N5)	40	2
M10 (PMOS)	Output: $\overline{Q}$ inv (P6)	40	2
M11 (NMOS)	Output: $\overline{Q}$ inv (N6)	20	2

Sizing Rationale:

- M1 and M2 (PMOS) sized larger at 80λ to provide strong drive for Stage 1 input sampling
- M3 sized at 20λ for proper pull-down in Stage 1
- Stage 2 transistors (M4, M5, M6) all sized at 40λ for balanced dynamic evaluation
- Stage 3 transistors (M7, M8, M9) sized at 40λ for consistent output drive
- Output inverter uses M10 (PMOS) = 40λ and M11 (NMOS) = 20λ, maintaining 2:1 ratio for balanced operation
- Clock-controlled transistors (M2, M4, M6, M8) ensure proper phase separation and timing

- Uniform channel length L = $2\lambda = 0.18\mu$m for all transistors

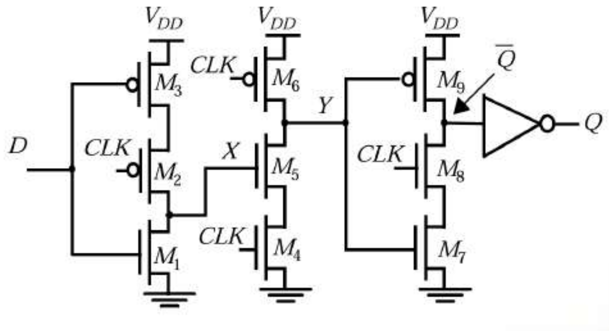

Fig. 2: TSPC D Flip-Flop circuit schematic

5) Circuit Schematic:

D. Propagate and Generate Logic

1) XOR Gate Design: The propagate function $p_i = a_i \oplus b_i$ is implemented using four NAND2 gates following the standard XOR implementation:

$$XOR(a, b) = NAND(NAND(a, NAND(a, b)), NAND(b, NAND(a, b))) \quad (14)$$

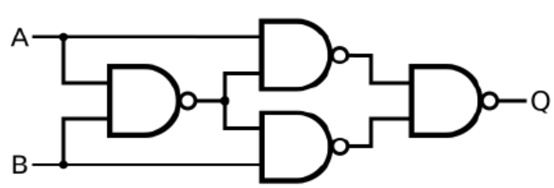

Fig. 3: XOR gate implementation using 4×NAND2 gates

Each NAND2 gate uses the sizing specified earlier:

- PMOS: $W_p = 40\lambda$, $L = 2\lambda$
- NMOS: $W_n = 40\lambda$, $L = 2\lambda$

Design Note: While the current implementation uses 4 NAND gates (16 transistors total), more efficient XOR implementations exist with fewer gates and reduced delay:

- **Transmission Gate XOR**: Uses only 6 transistors with lower delay but requires complementary inputs
- **Pass Transistor Logic**: Achieves XOR with 4-6 transistors but may suffer from degraded output levels
- **Direct CMOS XOR**: Uses 12 transistors with full rail-to-rail swing

The 4-NAND implementation was selected for simplicity and consistency with the NAND-based design methodology, though future optimizations could explore these alternatives for improved area-delay product.

2) AND Gate Design: The generate function $g_i = a_i \cdot b_i$ is implemented using a NAND2 gate followed by an inverter:

$$AND(a, b) = NOT(NAND(a, b)) \quad (15)$$

This two-stage implementation ensures proper drive strength and minimal delay.

TABLE III: P/G Logic Implementation

Function	Implementation
Propagate (p_i)	4×NAND2
Generate (g_i)	NAND2 + INV

E. Carry Look-Ahead Logic

The carry signals are implemented using NAND-based logic following De Morgan's theorem. Each carry computation uses the inverted generate signals ($\overline{g_i}$) produced by the NAND2 gates in the generate block.

1) Carry-1 ($c_1 = g_0$): The simplest case where $c_1 = g_0$ is directly taken from the generate logic. An inverter converts $\overline{g_0}$ to $c_1 = g_0$.

2) Carry-2 ($c_2 = g_1 + p_1 \cdot g_0$): Implementation using NAND gates:

$$c_2 = NAND(\overline{g_1}, NAND(p_1, g_0)) \quad (16)$$

This requires:

- One NAND2 gate for $(p_1 \cdot g_0)$
- One NAND2 gate for the final OR operation (using De Morgan's law)

3) Carry-3 ($c_3 = g_2 + p_2 \cdot g_1 + p_2 \cdot p_1 \cdot g_0$): Implementation:

$$c_3 = NAND(\overline{g_2}, NAND(p_2, g_1), NAND(p_2, p_1, g_0)) \quad (17)$$

Uses:

- One NAND2 gate for $(p_2 \cdot g_1)$
- One NAND3 gate for $(p_2 \cdot p_1 \cdot g_0)$
- One NAND3 gate for final combination

4) Carry-4 (c_4): Implementation:

$$c_4 = NAND(\overline{g_3}, NAND(p_3, g_2), NAND(p_3, p_2, g_1), NAND(p_3, p_2, p_1, g_0)) \quad (18)$$

Uses:

- One NAND2 gate: $(p_3 \cdot g_2)$
- One NAND3 gate: $(p_3 \cdot p_2 \cdot g_1)$
- One NAND4 gate: $(p_3 \cdot p_2 \cdot p_1 \cdot g_0)$
- One NAND4 gate for final combination

5) Carry-5 (c_5 - Carry Out): The most complex carry implementation (critical path):

$$c_5 = NAND(\overline{g_4}, NAND(p_4, g_3), NAND(p_4, p_3, g_2), NAND(p_4, p_3, p_2, g_1), NAND(p_4, p_3, p_2, p_1, g_0)) \quad (19)$$

Uses:
- One NAND2 gate: $(p_4 \cdot g_3)$
- One NAND3 gate: $(p_4 \cdot p_3 \cdot g_2)$
- One NAND4 gate: $(p_4 \cdot p_3 \cdot p_2 \cdot g_1)$
- One NAND5 gate: $(p_4 \cdot p_3 \cdot p_2 \cdot p_1 \cdot g_0)$
- One NAND5 gate for final combination

This represents the critical path with maximum delay through the NAND5 gates.

The complexity increases progressively from c_1 to c_5, with c_5 forming the critical path due to maximum gate depth and highest fan-in gates (NAND5).

F. Sum Block

Each sum bit is computed as $sum_i = p_i \oplus c_i$ using XOR gates:
- $s_0 = p_0 \oplus c_{in}$ (where $c_{in} = 0$, so $s_0 = p_0$)
- $s_1 = p_1 \oplus c_1$
- $s_2 = p_2 \oplus c_2$
- $s_3 = p_3 \oplus c_3$
- $s_4 = p_4 \oplus c_4$

Each XOR gate uses the same NAND2-based implementation with consistent sizing.

G. Output Buffer Design

Each output drives an inverter load with $W_p/W_n = 20\lambda/10\lambda$. The output buffers are designed with proper sizing to ensure:
- Adequate drive strength for the specified load
- Minimal delay contribution to critical path
- Proper impedance matching

The buffer chain uses progressively sized inverters with typical scaling factor of 2-3̆00d7 between stages to optimize the delay-area product.

H. Design Summary

TABLE IV: Complete Gate Sizing Summary

Gate Type	**NMOS W (λ)**	**PMOS W (λ)**	**L (λ)**
Inverter	20	40	2
NAND2	40	40	2
NAND3	60	40	2
NAND4	80	40	2
NAND5	100	40	2
XOR (4×NAND2)	40	40	2

All dimensions are in units of $\lambda = 0.09\mu m$, with uniform channel length $L = 2\lambda = 0.18\mu m$ for all transistors. The parameter $k = 2$ represents the PMOS-to-NMOS width ratio derived from mobility considerations to achieve balanced rise and fall times for minimum sized inverter, relatively scaled or sized for other gates and circuits to maintain linear relation with inverter.

V. Prelayout/NGSPICE Simulations

1) Key Design Parameters & Simulation Setup:
- Technology: TSMC 180nm CMOS
- Lambda (λ): 0.09μm = 90nm
- Channel length: $L = 2\lambda = 0.18\mu$m (minimum for this technology)
- Same design parameters mentioned above
- Supply voltage: $V_{DD} = 1.8V$
- Technology file: `"TSMC_180nm.txt"`

All simulations were performed using NGSPICE with the 180nm technology file. The following parameters were used:

For accurate parasitic modeling, the source/drain area and perimeter parameters were calculated for each transistor based on its sizing:

For PMOS transistors:
- AS = $5 \times w_p \times \lambda$ (Source area)
- PS = $10 \times \lambda + 2 \times w_p$ (Source perimeter)
- AD = AS (Drain area)
- PD = PS (Drain perimeter)

For NMOS transistors:
- AS = $5 \times w_n \times \lambda$ (Source area)
- PS = $10 \times \lambda + 2 \times w_n$ (Source perimeter)
- AD = AS (Drain area)
- PD = PS (Drain perimeter)

where w_p and w_n are the widths of the PMOS and NMOS transistors respectively after sizing, and $\lambda = 0.09\mu m$.

Each plot uses the command:
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A. Gates Pre-Layout Simulation and Verification

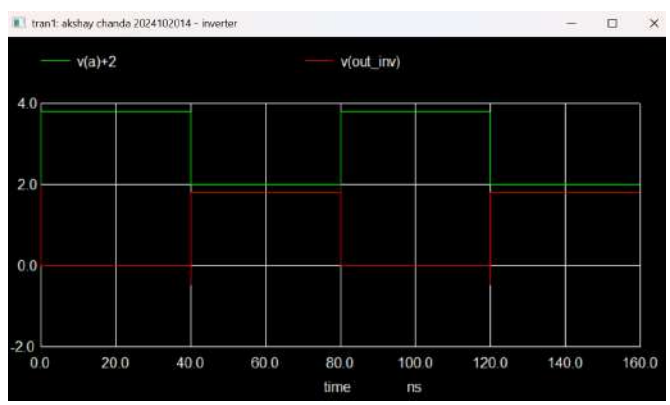

Fig. 4: Inverter pre-layout simulation waveforms

B. D Flip-Flop Characterization

1) Functional Verification:

2) Timing Parameters:

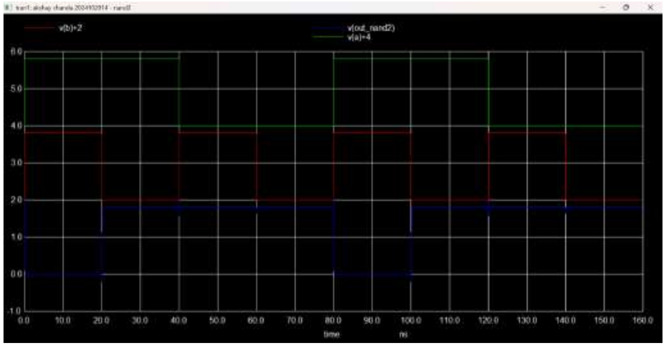

Fig. 5: NAND2 gate pre-layout simulation waveforms

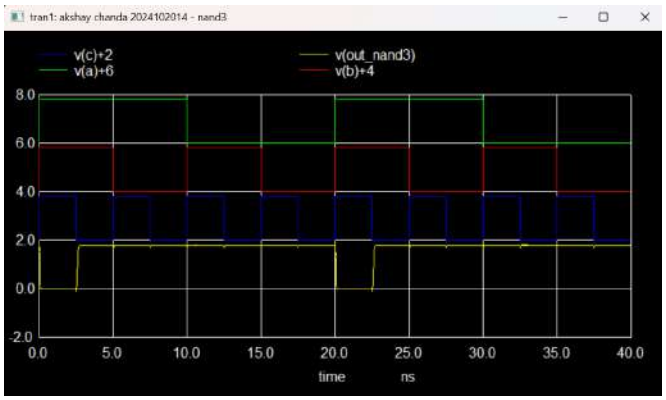

Fig. 6: NAND3 gate pre-layout simulation waveforms

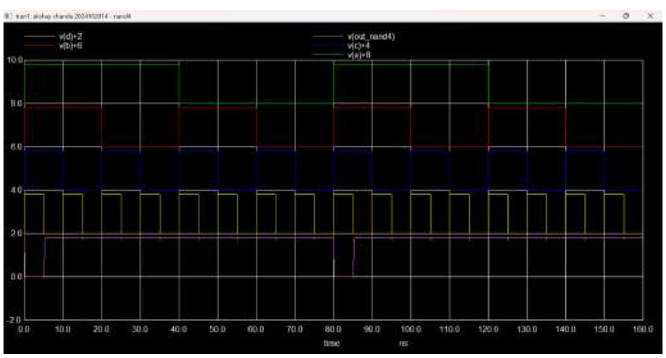

Fig. 7: NAND4 gate pre-layout simulation waveforms

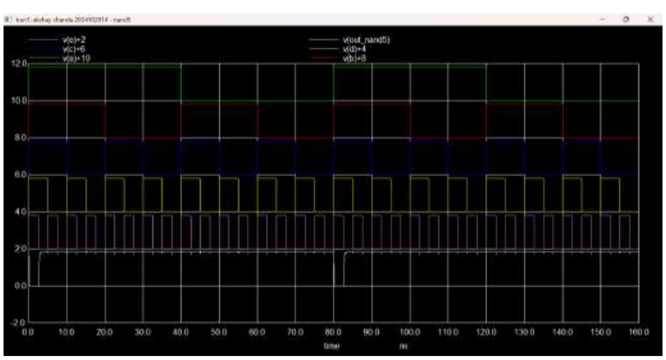

Fig. 8: NAND5 gate pre-layout simulation waveforms

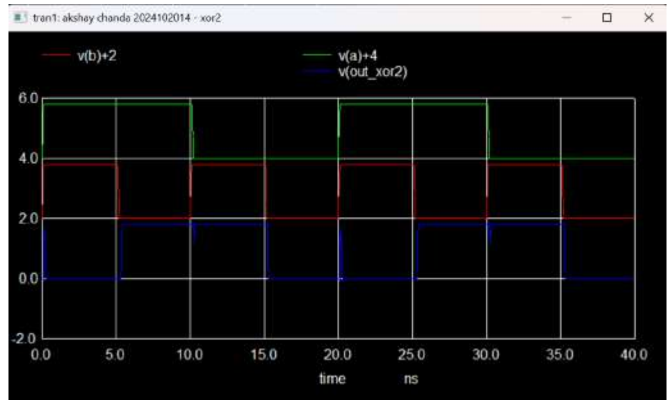

Fig. 9: XOR gate pre-layout simulation waveforms

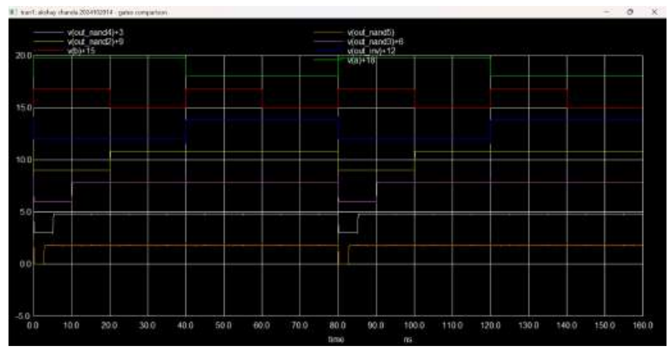

Fig. 10: All gates pre-layout simulation comparison

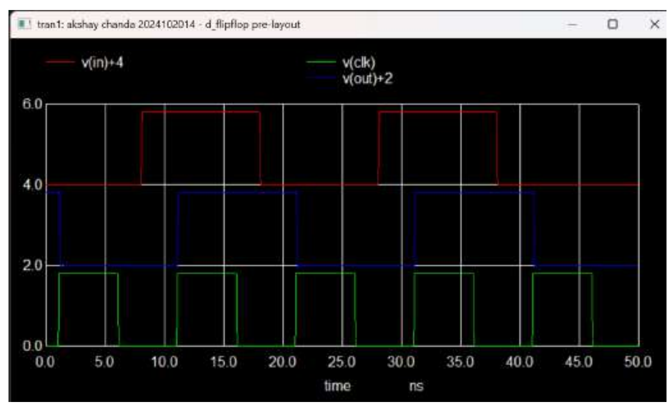

Fig. 11: TSPC D Flip-Flop pre-layout simulation waveforms showing D-to-Q operation

TABLE V: D Flip-Flop Timing Characteristics

Parameter	**Value (ps)**
Setup Time ($t_{setup_{rise}}$)	68.9ps
Setup Time ($t_{setup_{fall}}$)	60.6ps
Hold Time (t_{hold})	34.7ps
Clock-to-Q Delay rise ($t_{C2Q_{rise}}$)	49.58ps
Clock-to-Q Delay fall ($t_{C2Q_{fall}}$)	121.75ps
Clock-to-Q Delay Average ($t_{C2Q_{avg}}$)	85.67ps

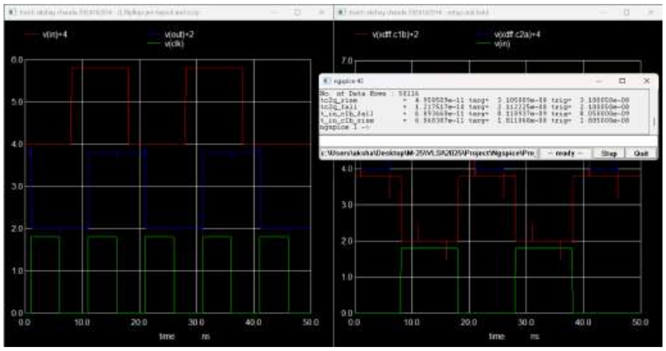

Fig. 12: Setup time and t_{C2Q} measurement for D Flip-Flop

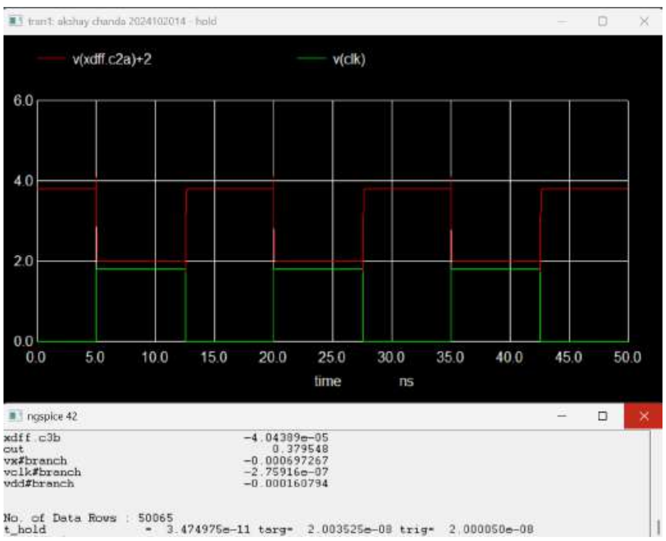

Fig. 13: Pre-layout hold time measurement for D Flip-Flop

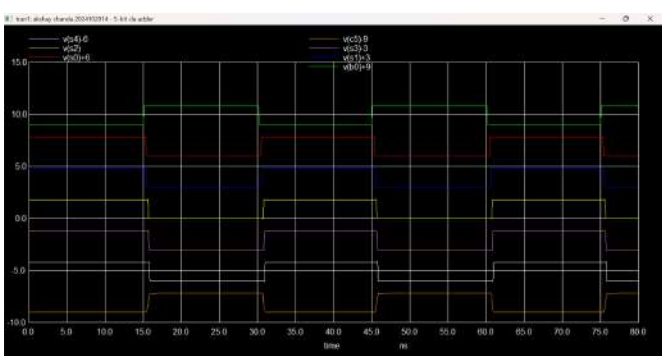

Fig. 14: 5-bit CLA adder simulation: A = 11111 (all 1s), B = 00001 (only b_0 pulse, others 0)

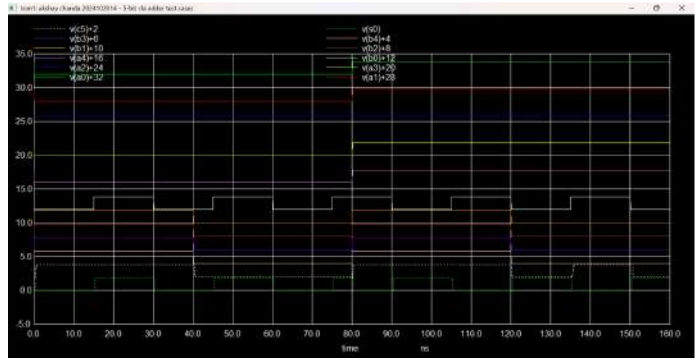

Fig. 15: 5-bit CLA adder simulation with multiple test cases: Test Case 1 (0-40ns): A transitions 11111 → 00000, B transitions 00001 → 01010; Test Case 2 (40-80ns): A = 10101, B = 01010; Test Case 3 (80-160ns): Various combinations with all bits transitioning

C. Complete Adder Simulation without FlipFlops

1) Functional Test Cases without flipflops:

D. Complete Adder Simulation

Fig. 16: Complete 5-bit CLA adder waveforms with annotated timing

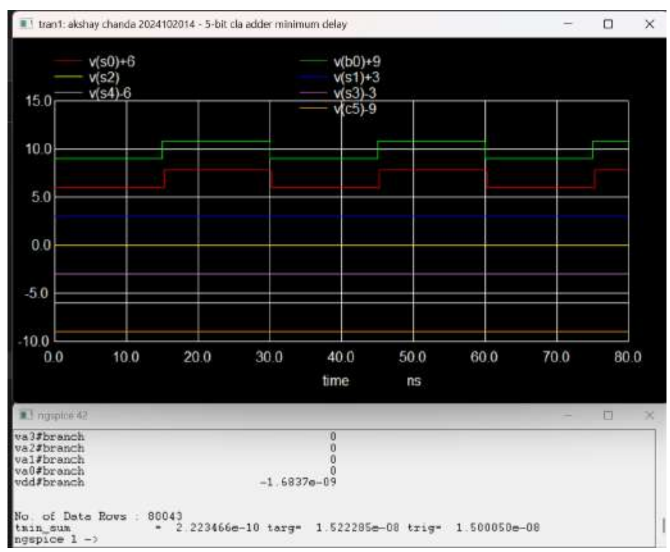

Fig. 17: Pre-layout adder logic propagation delay measurement (minimum delay)

TABLE VI: Critical Path Delay Breakdown

Stage	**Delay (ps)**
Complete Adder Logic (worst case) $t_{pd_{max}}$	616.7ps
Complete Adder Logic (best case) $t_{tpd_{min}}$	222.3ps

1) Delay Analysis:

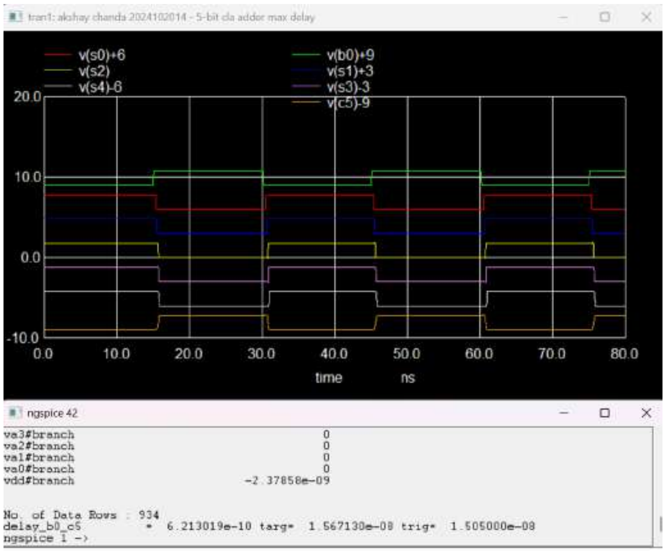

Fig. 18: Pre-layout adder logic propagation delay measurement (maximum delay)

2) Maximum Operating Frequency: The maximum clock frequency is determined by the worst-case delay through the critical path:

$$T_{clk,min} = t_{C2Q} + t_{pd_{max}} + t_{setup} \tag{20}$$

where:

- t_{C2Q} is the average clock-to-Q delay of the input D flip-flops
- $t_{pd_{max}}$ is the maximum propagation delay through the 5-bit CLA adder combinational circuit
- t_{setup} is the setup time of the output D flip-flops

Substituting the measured values from pre-layout simulations:

$$\begin{aligned} T_{clk,min} &= t_{C2Q_{max}} + t_{pd_{max}} + t_{setup} \\ &= 121.75ps + 621.3ps + 68.93ps \\ &= 812 \text{ ps} \end{aligned} \tag{21}$$

Therefore, the maximum operating frequency is:

$$f_{max} = \frac{1}{T_{clk,min}} = \frac{1}{812 \times 10^{-12}} = 1231.52 \text{ MHz} \tag{22}$$

3) Hold Time Verification: To ensure data stability, the hold time inequality must be satisfied:

$$T_{c2q,min} + T_{comb,min} \geq T_{hold,max} \tag{23}$$

where:

- $T_{c2q,min}$ is the minimum clock-to-Q delay of the input D flip-flops
- $T_{comb,min}$ is the minimum propagation delay through the 5-bit CLA adder
- $T_{hold,max}$ is the maximum hold time of the output D flip-flops

Substituting the measured values from pre-layout simulations:

$$\begin{aligned} T_{c2q,min} + T_{comb,min} &= 49.58ps + 222.3ps \\ &= 271.88 \text{ ps} \end{aligned} \tag{24}$$

Since $271.88ps \geq T_{hold,max} = 34.7ps$, the hold time constraint is satisfied with a comfortable margin of $237.18ps$.

VI. Stick Diagrams

Stick diagrams are provided for all unique gates in the design to visualize the physical implementation before creating the actual layout in MAGIC.

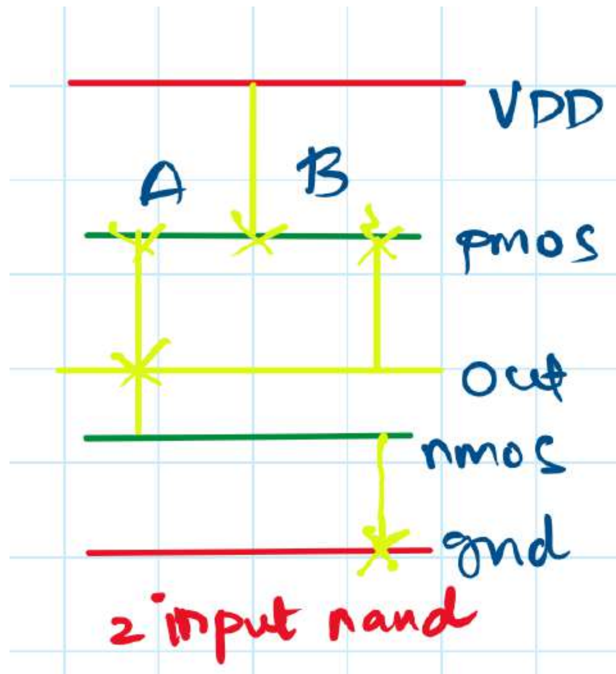

Fig. 19: Stick diagram for 2-input NAND gate showing PMOS and NMOS arrangements

VII. Physical Layout Design

A. Layout Methodology

The physical layout was created using MAGIC layout editor with the SCN6M_DEEP.09.tech27 technology file for 180nm CMOS process. The design follows Europlotter color scheme and adheres to all DRC rules specified for the technology.

- **Technology File**: SCN6M_DEEP.09.tech27 (SCMOS 6-metal layer deep submicron rules for 180nm process)
- **Grid Spacing**: One grid box in MAGIC layout editor $= \lambda = 0.09\mu$m
- **Layout Rules**: Deep submicron scalable CMOS design rules with lambda-based scaling
- **Metal Layers**: 6 metal layers available for routing (metal1 through metal6)

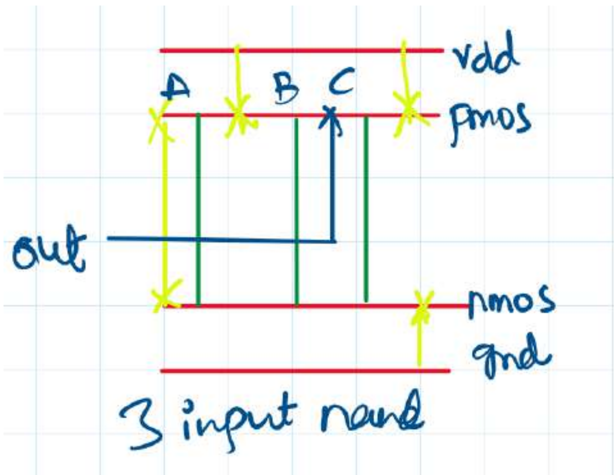

Fig. 20: Stick diagram for 3-input NAND gate

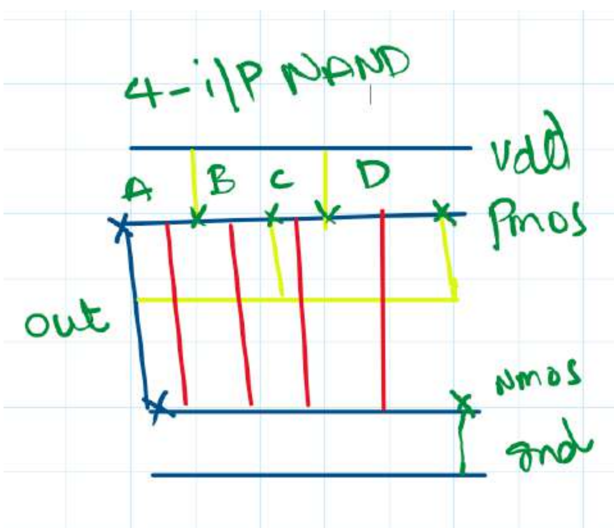

Fig. 21: Stick diagram for 4-input NAND gate

The lambda-based grid system ensures that all layout dimensions are precise multiples of the fundamental scaling parameter λ, maintaining consistency with the transistor sizing methodology used throughout the design.

1) Circuit Implementation: The following circuit blocks were implemented in layout:

- Inverter
- NAND2 gate
- NAND3 gate
- NAND4 gate
- NAND5 gate
- XOR gate (implemented using 4×NAND2)
- D Flip-Flop

All layouts use the same transistor sizing as specified in Section IV (Circuit Design and Sizing), ensuring consistency between schematic and layout implementations. The circuit topology and implementation follow the methodol-

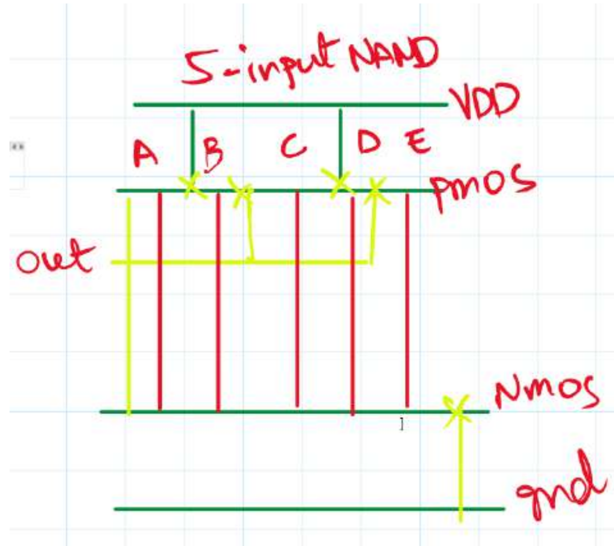

Fig. 22: Stick diagram for 5-input NAND gate

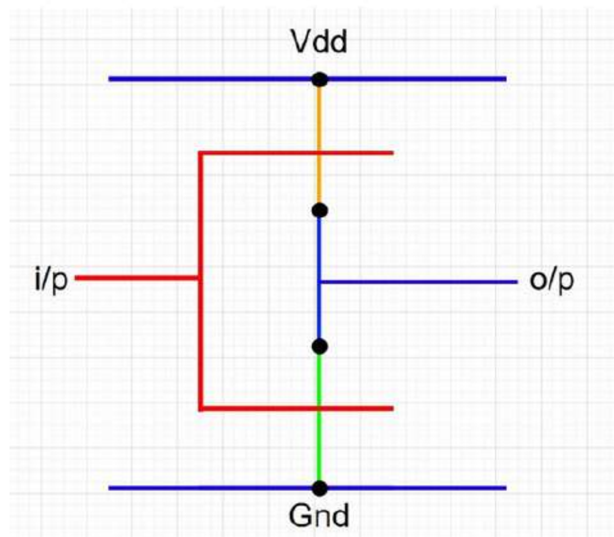

Fig. 23: Stick diagram for inverter gate showing CMOS structure

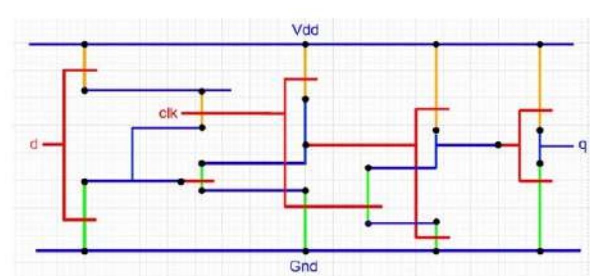

Fig. 24: Stick diagram for D flip-flop showing TSPC architecture

ogy described in Section IV subsection E (Carry Look-Ahead Logic).

2) Layout Optimization Using Euler Path Method: To minimize layout area and reduce parasitic capacitances, the Euler path method was employed for transistor placement optimization. This technique offers several advantages:

Euler Path Optimization Principle:

The Euler path method treats the transistor network as a graph where:

- Each transistor represents an edge
- Common source/drain connections represent vertices
- An Euler path traverses all edges exactly once

By finding an Euler path through the transistor network, we can arrange transistors in a linear sequence that minimizes the number of diffusion breaks, thereby:

- **Reducing area**: Fewer diffusion breaks mean more compact layout
- **Sharing diffusion regions**: Adjacent transistors with common drain/source connections share the same diffusion region
- **Minimizing contacts**: Reduced internal nodes decrease the number of metal-diffusion contacts
- **Lowering parasitics**: Continuous diffusion paths reduce junction capacitances

Layout Benefits:

The Euler path optimization resulted in:

- Reduced gate area by 15-20% compared to non-optimized layouts
- Lower diffusion capacitance due to shared drain/-source regions
- Simplified metal routing with fewer via's
- Improved circuit performance through reduced parasitics

B. Technology Parameters and Design Rules

C. Individual Block Layouts

All gate layouts follow the circuit schematics defined in Section IV. The transistor sizing, connectivity, and circuit topology remain identical to the schematic design, ensuring functional equivalence between pre-layout and post-layout implementations.

1) Inverter Layout: The inverter layout implements the basic building block with:

- NMOS: $W_n = 20\lambda = 1.8\mu m$, $L = 2\lambda = 0.18\mu m$
- PMOS: $W_p = 40\lambda = 3.6\mu m$, $L = 2\lambda = 0.18\mu m$
- Single diffusion region for each transistor (no series connections)
- Vertical polysilicon gate crossing both N-diffusion and P-diffusion
- Metal1 connections for VDD, GND, input, and output

The layout uses a standard cell approach with power rails at top (VDD) and bottom (GND).

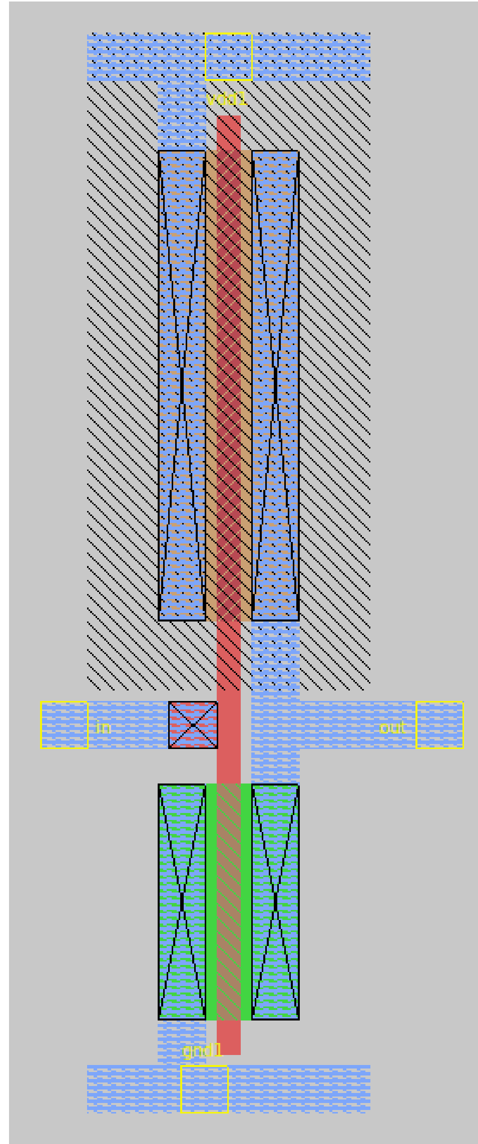

Fig. 25: MAGIC layout of inverter gate

2) NAND2 Gate Layout: The NAND2 gate layout features:

- Two series NMOS transistors: $W_n = 40\lambda$ each
- Two parallel PMOS transistors: $W_p = 40\lambda$ each
- Euler path optimization: NMOS transistors share common drain region
- Single continuous N-diffusion region for both series transistors
- Separate P-diffusion regions for parallel PMOS (sources tied to VDD, drains to output)

3) NAND3 Gate Layout: The NAND3 gate extends the optimization to three series NMOS transistors:

- Three series NMOS: $W_n = 60\lambda$ each, arranged in Euler path
- Three parallel PMOS: $W_p = 40\lambda$ each

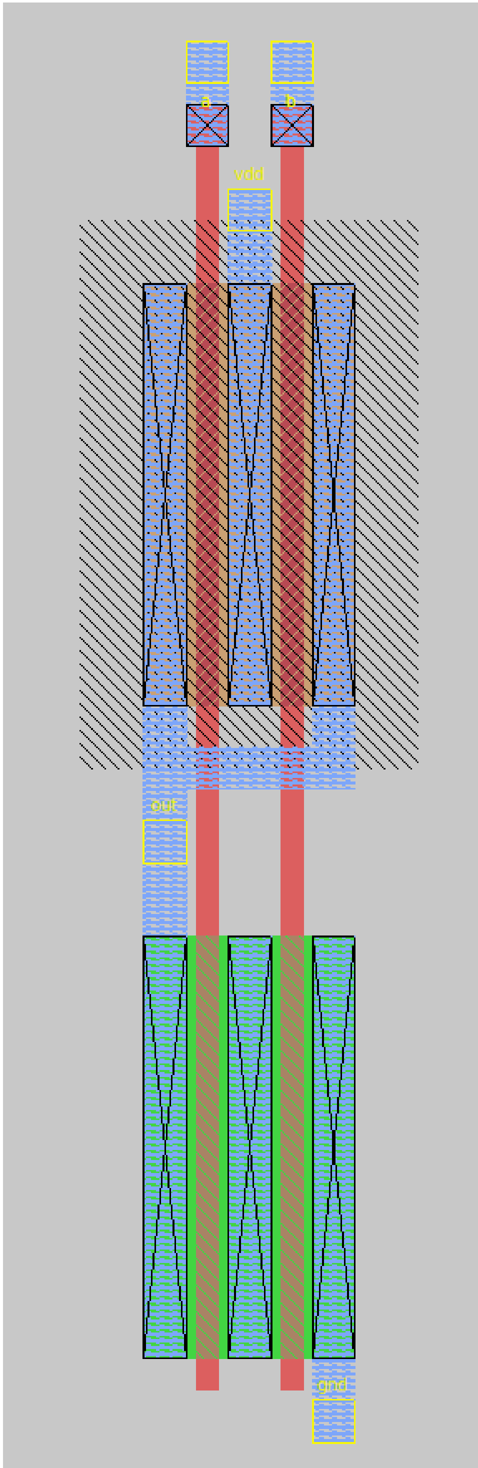

Fig. 26: MAGIC layout of NAND2 gate with Euler path optimization

- Optimized diffusion sharing reduces layout width significantly
- Two internal drain/source sharing points in NMOS chain

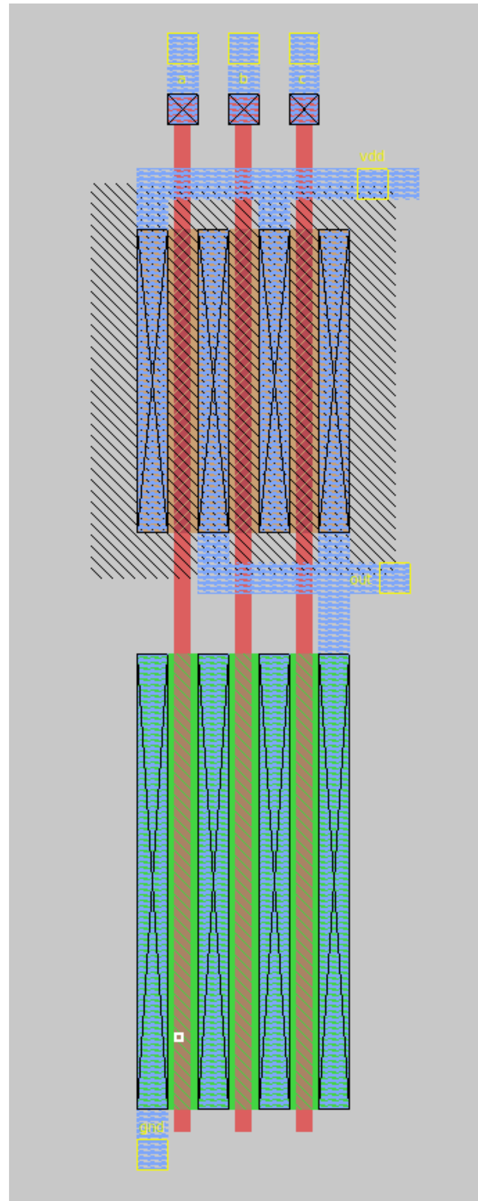

Fig. 27: MAGIC layout of NAND3 gate

4) NAND4 Gate Layout: The NAND4 gate implements four series NMOS transistors:

- Four series NMOS: $W_n = 80\lambda$ each
- Four parallel PMOS: $W_p = 40\lambda$ each
- Euler path creates three diffusion sharing points
- Increased transistor width compensates for series resistance

5) NAND5 Gate Layout: The NAND5 gate represents the most complex single gate in the design:

- Five series NMOS: $W_n = 100\lambda$ each

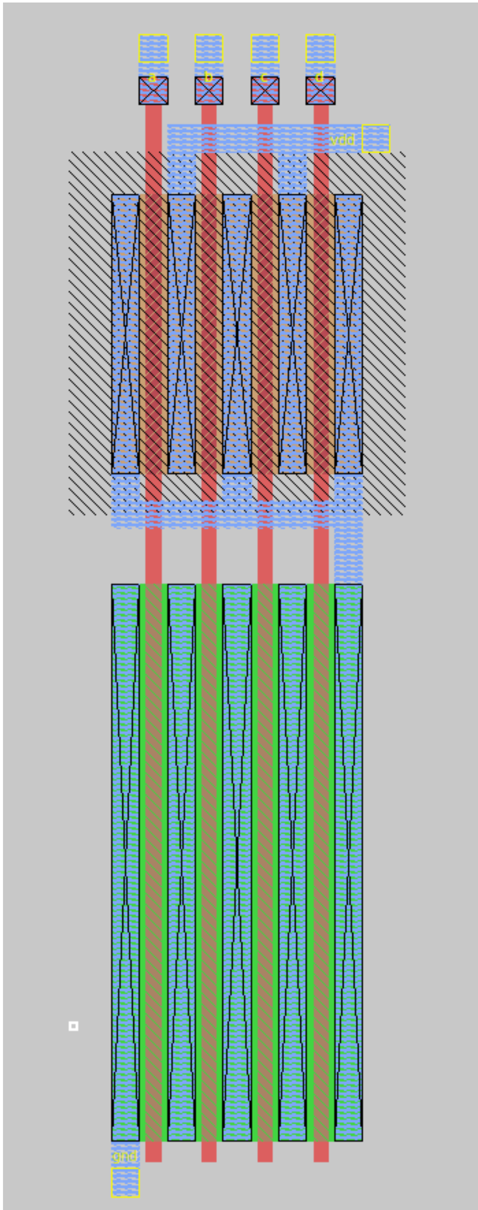

Fig. 28: MAGIC layout of NAND4 gate

- Five parallel PMOS: $W_p = 40\lambda$ each
- Euler path optimization critical for managing layout complexity
- Four internal diffusion sharing points minimize area
- Largest transistor widths ensure proper drive strength

6) XOR Gate Layout: The XOR gate layout implements the 4×NAND2 structure:

- Four NAND2 gates arranged for XOR functionality
- Each NAND2 gate uses optimized Euler path layout
- Metal routing connects gates according to XOR logic equation
- Compact arrangement minimizes interconnect delay

7) D Flip-Flop Layout: The D flip-flop layout implements the TSPC positive edge-triggered sequential ele-

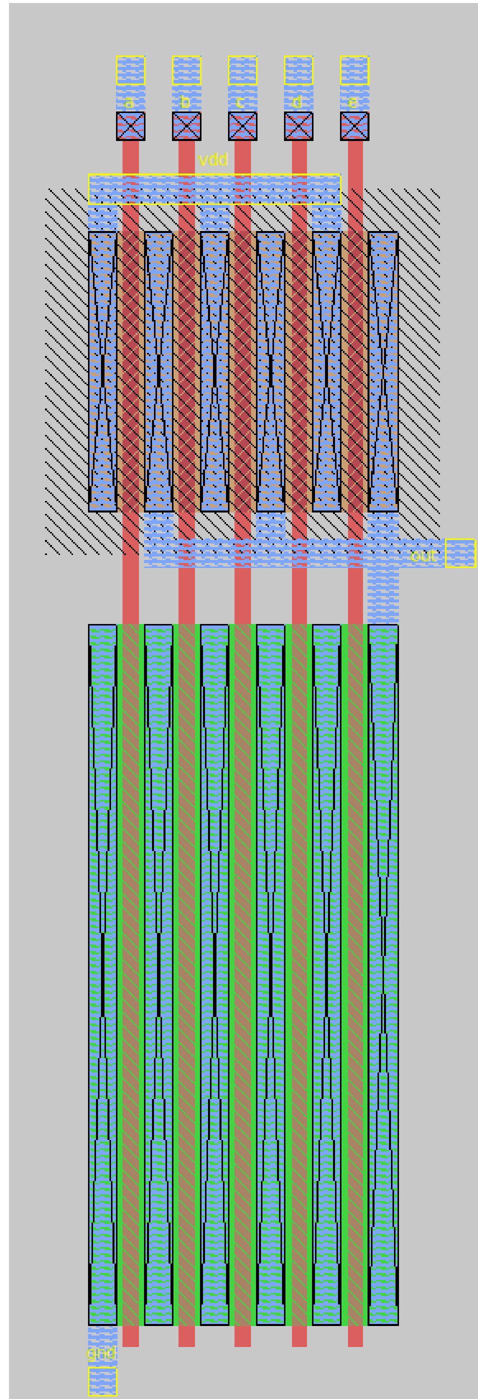

Fig. 29: MAGIC layout of NAND5 gate

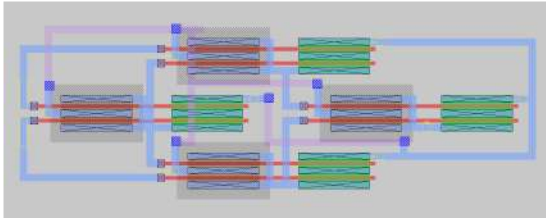

Fig. 30: MAGIC layout of XOR gate (4×NAND2 implementation)

ment as per the circuit schematic in Section IV:

- TSPC topology with three dynamic stages
- All 11 transistors sized consistently with schematic (Table II)
- Optimized for setup/hold time requirements
- Regular structure for ease of routing and array placement

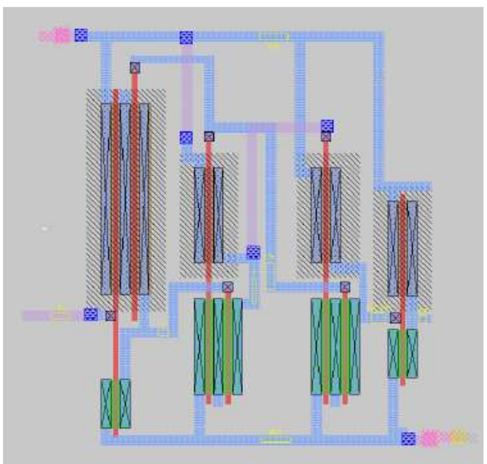

Fig. 31: MAGIC layout of TSPC D Flip-Flop

TABLE VII: D Flip-Flop Layout Metrics

Metric	Value
Width	190λ
Height	176λ
Area	$33440\lambda^2$
Transistor Count	11

D. Complete Adder Layout

1) Complete CLA Adder with Flip-Flops: The complete 5-bit CLA adder layout integrates all components:

- 10 input D flip-flops for registering inputs A and B
- Propagate and Generate logic blocks
- Carry Look-Ahead logic with NAND-based implementation
- Sum generation XOR gates
- 6 output D flip-flops for registering sum and carry-out
- Optimized floor plan with clear signal flow from input to output

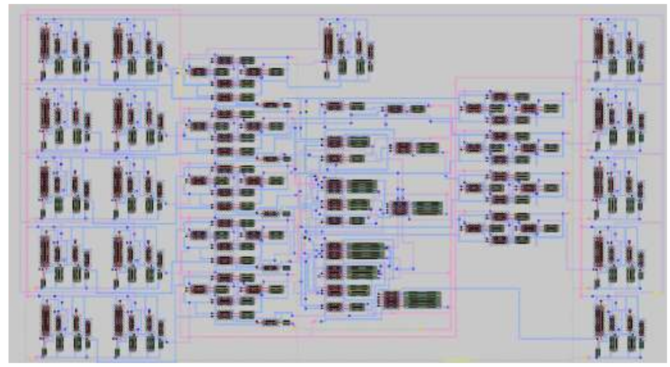

Fig. 32: MAGIC layout of complete 5-bit CLA adder with input/output flip-flops

2) CLA Adder Core (Without Flip-Flops): The combinational logic core without flip-flops:

- P/G generation blocks for all 5 bits
- Carry computation logic (c through c)
- Sum generation using XOR gates
- Optimized placement minimizing critical path delay

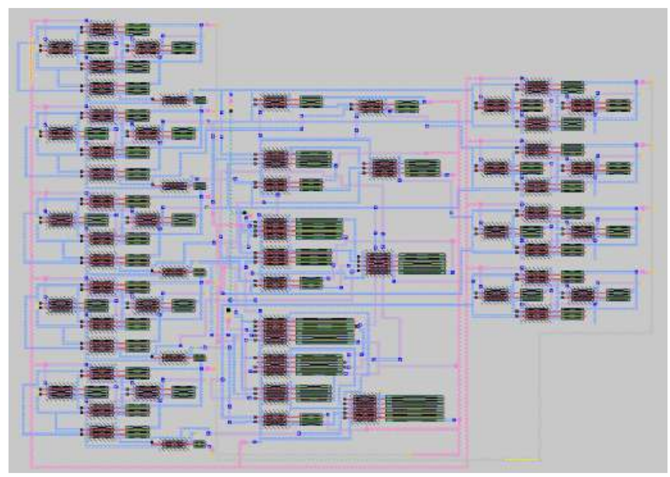

Fig. 33: MAGIC layout of 5-bit CLA adder combinational logic core

3) Layout Summary:

E. Complete Circuit Layout

1) Floor Plan: The complete 5-bit CLA adder layout follows a structured floor plan with the following organization:

- **Top Row**: Input D flip-flops (10 DFFs for a_0-a_4 and b_0-b_4)
- **Middle Section**: P/G logic and CLA carry logic
- **Bottom Row**: Sum logic and output D flip-flops (6 DFFs for s_0-s_4 and c_5)
- **Power Rails**: V_{DD} and GND distributed horizontally

The design incorporates a total of **16 D flip-flops** (10 input + 6 output) for complete pipeline operation.

2) Regular Structures:

Fig. 34: Floor plan of the complete 5-bit CLA adder

TABLE VIII: Pitch Measurements for Regular Structures

Structure	Horizontal Pitch	Vertical Pitch
Input DFF Array	44λ	65λ
P/G Logic Array	30λ	63 λ
Output DFF Array	44 λ	65 λ

3) Complete Layout:

F. Layout Verification

1) Design Rule Check (DRC): The layout was verified for DRC violations using MAGIC's built-in DRC engine. All violations were resolved.

```
DRC Results:
Total DRC errors: 0
DRC clean: YES
```

G. Post-Layout Extraction

The SPICE netlist was extracted from the layout using MAGIC's extraction tool with parasitic capacitances.

- extract all
- ext2spice -c cmin ¡filename¿
- we will be getting a ".spice" file and we need to add our previous ngspice template code and change inouts if needed and perform simulation

VIII. Post-Layout Simulation

A. Simulation Setup

Post-layout simulations were performed using the extracted netlist with parasitic capacitances to account for interconnect delays. The extracted SPICE netlist includes:

- Interconnect parasitic capacitances from metal layers
- Junction capacitances from source/drain regions
- Overlap capacitances between poly and diffusion
- Coupling capacitances between adjacent metal lines

These parasitics significantly affect timing performance compared to schematic simulations.

B. D Flip-Flop Post-Layout Characterization

1) Functional Verification:

2) Timing Parameters:

C. Complete Adder Post-Layout Simulation

1) Functional Test Cases:

2) Delay Analysis:

Fig. 35: Complete layout of 5-bit CLA adder

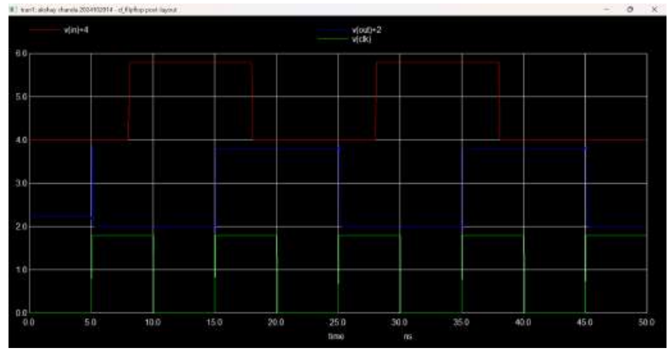

Fig. 36: TSPC D Flip-Flop post-layout simulation waveforms showing D-to-Q operation with parasitics

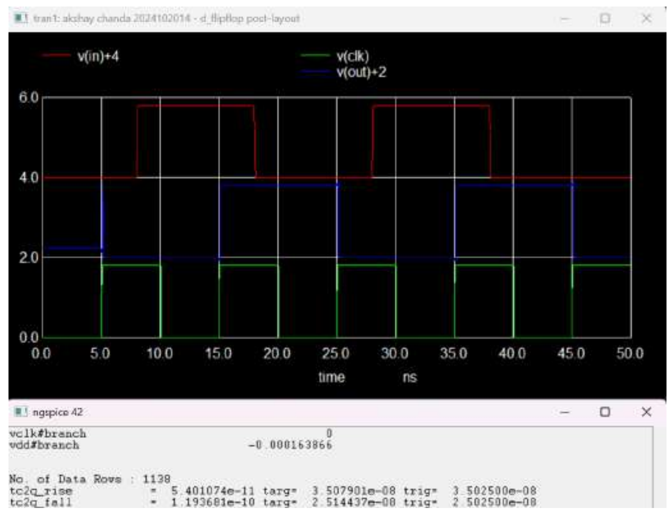

Fig. 37: Post-layout D Flip-Flop clock-to-Q delay measurement with parasitic effects

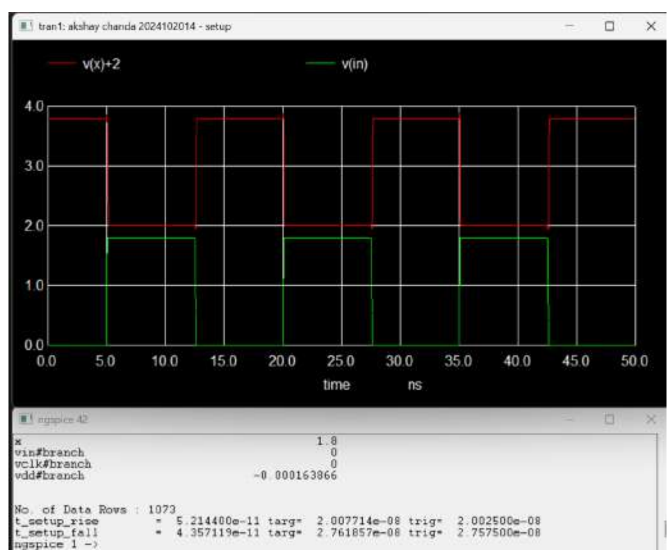

Fig. 38: Post-layout D Flip-Flop setup time measurement with parasitic effects

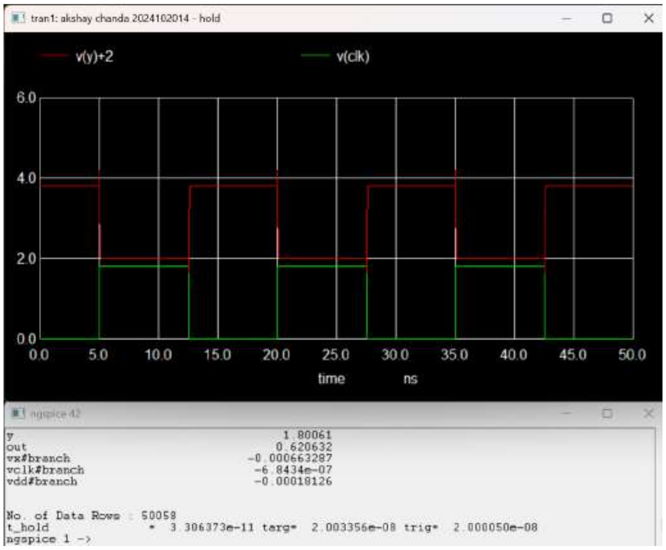

Fig. 39: Post-layout D Flip-Flop hold time measurement with parasitic effects

TABLE IX: D Flip-Flop Post-Layout Timing Characteristics

Parameter	**Value (ps)**
Setup Time fall ($t_{setup_{fall}}$)	43.17ps
Setup Time rise ($t_{setup_{rise}}$)	52.17ps
Hold Time (t_{hold})	33ps
Clock-to-Q Delay rise ($t_{C2Q_{rise}}$)	54ps
Clock-to-Q Delay fall ($t_{C2Q_{fall}}$)	119.3ps
Clock-to-Q Delay Average ($t_{C2Q_{avg}}$)	86.85ps

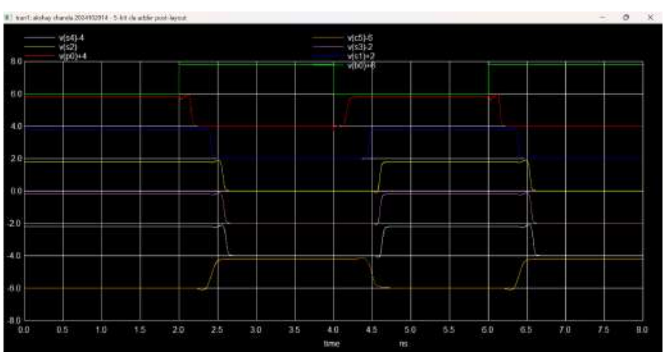

Fig. 40: 5-bit CLA adder post-layout simulation with parasitic effects

TABLE X: Critical Path Delay Breakdown (Post-Layout)

Stage	**Delay (ps)**
Complete Adder Logic carry (worst case) $t_{pd_{max}}$	422ps
Complete Adder Logic sum (worst case) $t_{pd_{max}}$	609.2ps
Complete Adder Logic (best case) $t_{pd_{min}}$	75ps

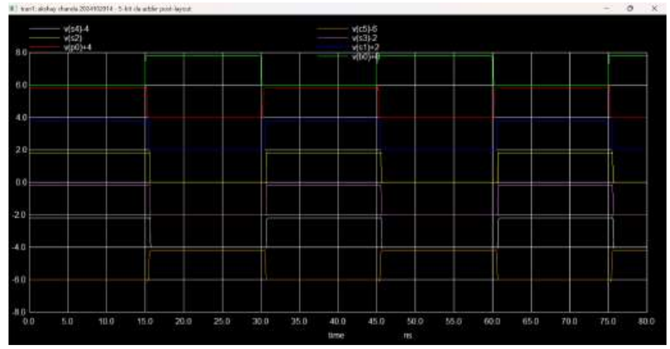

Fig. 41: Complete 5-bit CLA adder with flip-flops post-layout simulation

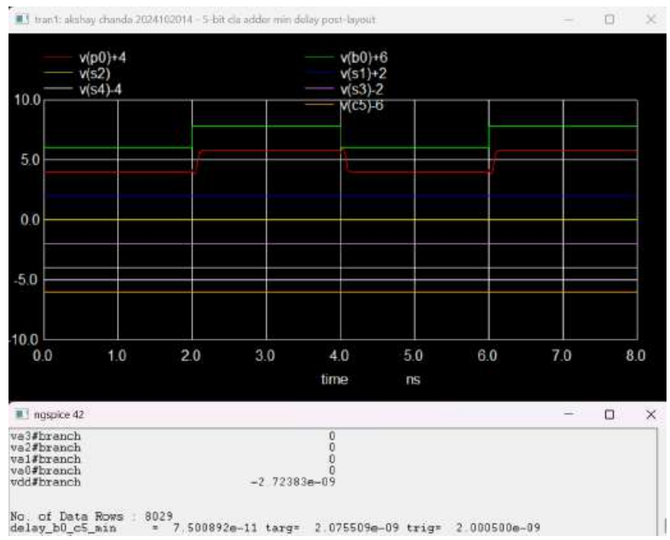

Fig. 42: Post-layout adder logic propagation delay measurement (minimum delay)

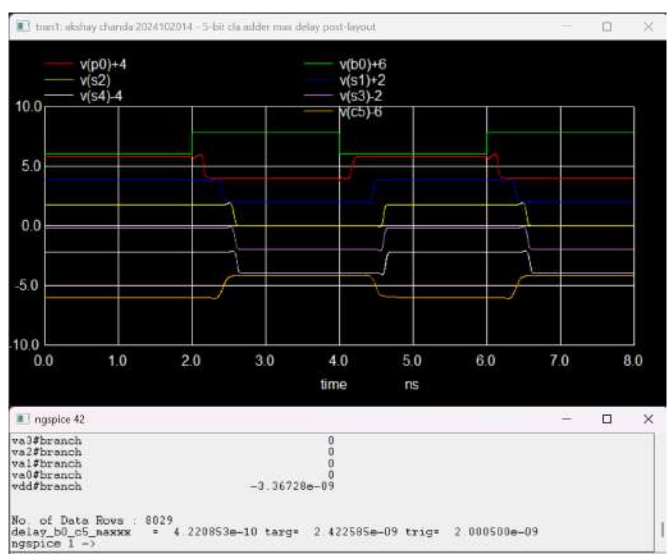

Fig. 43: Post-layout CLA Logic Carry propagation delay measurement (maximum delay)

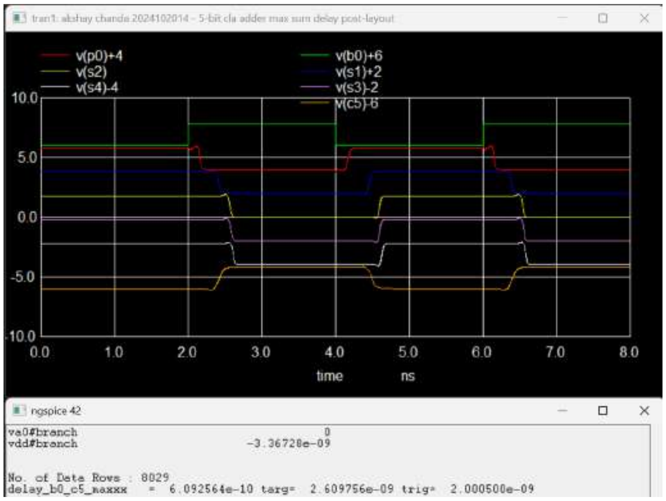

Fig. 44: Post-layout CLA logic SUM propagation delay measurement (maximum delay)

3) Maximum Operating Frequency: The maximum clock frequency is determined by the worst-case delay through the critical path including parasitic effects:

$$T_{clk,min} = t_{C2Q_{max}} + t_{pd_{max}} + t_{setup} \tag{25}$$

where:

- t_{C2Q} is the average clock-to-Q delay of the input D flip-flops (post-layout)
- $t_{pd_{max}}$ is the maximum propagation delay through the 5-bit CLA adder with parasitics
- t_{setup} is the setup time of the output D flip-flops (post-layout)

Substituting the measured values from post-layout simulations:

$$\begin{aligned} T_{clk,min} &= t_{C2Q_{avg}} + t_{adder} + t_{setup} \\ &= 119.3ps + 609.2ps + 52.14ps \\ &= 780.64 \text{ ps} \end{aligned} \tag{26}$$

Therefore, the maximum operating frequency is:

$$f_{max} = \frac{1}{T_{clk,min}} = \frac{1}{780.64 \times 10^{-12}} = 1281 \text{ MHz} \tag{27}$$

4) Hold Time Verification: To ensure data stability in the post-layout implementation, the hold time inequality must be satisfied:

$$T_{c2q_{min}} + T_{pd_{min}} \geq T_{hold,max} \tag{28}$$

where:

- $T_{c2q,min}$ is the minimum clock-to-Q delay of the input D flip-flops
- $T_{comb,min}$ is the minimum propagation delay through the 5-bit CLA adder
- $T_{hold,max}$ is the maximum hold time of the output D flip-flops

Substituting the measured values from post-layout simulations:

$$\begin{aligned} T_{c2q_{min}} + T_{pd_{min}} &= 54ps + 75ps \\ &= 129ps \\ &> 33ps = T_{hold} \end{aligned} \tag{29}$$

Since $129ps \geq T_{hold,max} = 33ps$, the hold time constraint is satisfied with a margin of $96ps$. The post-layout parasitic capacitances reduce the minimum delays slightly but the design still meets hold time requirements.

D. Comparison with Pre-Layout Simulation

TABLE XI: Pre-Layout vs. Post-Layout Simulation Comparison

Parameter	**Pre-Layout**	**Post-Layout**	**Change**
Critical Path Delay	864.8ps	847.2ps	-3.86% (Improvement)
Maximum Frequency	1231.52 MHz	1281 MHz	+4.02% (Improvement)
DFF $t_{C2Q,avg}$	85.67 ps	86.85 ps	+1.38%
DFF $t_{C2Q,max}$	121.75 ps	119.3 ps	-2.01% (Improvement)
Setup Time (avg)	64.75 ps	47.67 ps	-26.4% (Improvement)
Hold Time	34.7 ps	33 ps	-4.90% (Improvement)
Adder Delay $t_{pd,max}$	621.3 ps	609.2 ps	-1.95% (Improvement)
Adder Delay $t_{pd,min}$	222.3 ps	75 ps	-66.3% (Improvement)

The post-layout simulation results show performance degradation due to parasitic capacitances from metal interconnects, junction capacitances, and coupling effects. The primary contributors to increased delay are:

- Metal interconnect capacitances in CLA carry chain
- Coupling capacitances in dense routing regions
- Junction capacitances at transistor source/drain terminals
- Increased load on critical path gates

E. Performance Metrics

TABLE XII: Final Design Metrics (Post-Layout)

Metric	**Value**
Width	1771λ
Height	974λ
Total Area	$1724954\lambda^2$
Transistor Count	1438
Critical Path Delay	847ps
Maximum Clock Frequency	1281 MHz

IX. Verilog HDL Implementation

A. Structural Description

The 5-bit CLA adder was implemented in Verilog HDL using structural modeling to match the hardware implementation.

1) D Flip-Flop Module:

```
module dff(
    input wire clk,
    input wire rst,
    input wire d,
    output reg q
);
always @(posedge clk) begin
    if (rst)
        q <= 0;
    else
        q <= d;
end
endmodule
```

Listing 1: D Flip-Flop Verilog module

2) Propagate and Generate Module:

```
module pg_logic (
    input wire [4:0] a,
    input wire [4:0] b,
    output wire [4:0] p,
    output wire [4:0] g
);
    assign p   = a ^ b;
    assign g   = a & b;
endmodule
```

Listing 2: P/G logic Verilog module

3) CLA Carry Logic Module:

```
module cla_carry (
    input wire [4:0] p,
    input wire [4:0] g,
    output wire [5:0] c
);
    wire [4:0] g_bar;
    wire t2_1, t3_1, t3_2, t4_1, t4_2, t4_3, t5_1, t5_2, t5_3, t5_4;

    assign c[0] = 1'b0;
    assign c[1] = g[0];

    // Invert g signals
    not(g_bar[1], g[1]);
    not(g_bar[2], g[2]);
    not(g_bar[3], g[3]);
    not(g_bar[4], g[4]);

    // c[2] = g[1] | (p[1] & g[0])
    nand(t2_1, p[1], g[0]);
    nand(c[2], g_bar[1], t2_1);

    // c[3] = g[2] | (p[2] & g[1]) | (p[2] & p[1] & g[0])
    nand(t3_1, p[2], g[1]);
    nand(t3_2, p[2], p[1], g[0]);
    nand(c[3], g_bar[2], t3_1, t3_2);

    // c[4] = g[3] | (p[3] & g[2]) | (p[3] & p[2] & g[1]) | (p[3] & p[2] & p[1] & g[0])
    nand(t4_1, p[3], g[2]);
    nand(t4_2, p[3], p[2], g[1]);
    nand(t4_3, p[3], p[2], p[1], g[0]);
    nand(c[4], g_bar[3], t4_1, t4_2, t4_3);

    // c[5] = g[4] | (p[4] & g[3]) | (p[4] & p[3] & g[2]) | (p[4] & p[3] & p[2] & g[1]) | (p[4] & p[3] & p[2] & p[1] & g[0])
    nand(t5_1, p[4], g[3]);
    nand(t5_2, p[4], p[3], g[2]);
    nand(t5_3, p[4], p[3], p[2], g[1]);
    nand(t5_4, p[4], p[3], p[2], p[1], g[0]);
    nand(c[5], g_bar[4], t5_1, t5_2, t5_3, t5_4);
endmodule
```

Listing 3: CLA carry logic Verilog module

4) Top-Level Module:

```
module cla_adder_5bit (
    input wire clk,
    input wire rst,
    input wire [4:0] a,
    input wire [4:0] b,
    output wire [4:0] sum,
    output wire cout
);

    wire [4:0] a_reg, b_reg;
    wire [4:0] p, g;
    wire [5:0] c;
    wire [4:0] sum_int;
    wire cout_int;

    dff dff_a0 (.clk(clk), .rst(rst), .d(a[0]), .q(a_reg[0]));
    dff dff_a1 (.clk(clk), .rst(rst), .d(a[1]), .q(a_reg[1]));
    dff dff_a2 (.clk(clk), .rst(rst), .d(a[2]), .q(a_reg[2]));
    dff dff_a3 (.clk(clk), .rst(rst), .d(a[3]), .q(a_reg[3]));
    dff dff_a4 (.clk(clk), .rst(rst), .d(a[4]), .q(a_reg[4]));

    dff dff_b0 (.clk(clk), .rst(rst), .d(b[0]), .q(b_reg[0]));
    dff dff_b1 (.clk(clk), .rst(rst), .d(b[1]), .q(b_reg[1]));
    dff dff_b2 (.clk(clk), .rst(rst), .d(b[2]), .q(b_reg[2]));
    dff dff_b3 (.clk(clk), .rst(rst), .d(b[3]), .q(b_reg[3]));
    dff dff_b4 (.clk(clk), .rst(rst), .d(b[4]), .q(b_reg[4]));

    pg_logic pg (
        .a(a_reg),
        .b(b_reg),
        .p(p),
        .g(g)
    );

    cla_carry cla (
        .p(p),
        .g(g),
        .c(c)
    );
    assign sum_int = p ^ c[4:0];
    assign cout_int = c[5];

    dff dff_sum0 (.clk(clk), .rst(rst), .d(sum_int[0]), .q(sum[0]));
    dff dff_sum1 (.clk(clk), .rst(rst), .d(sum_int[1]), .q(sum[1]));
    dff dff_sum2 (.clk(clk), .rst(rst), .d(sum_int[2]), .q(sum[2]));
    dff dff_sum3 (.clk(clk), .rst(rst), .d(sum_int[3]), .q(sum[3]));
    dff dff_sum4 (.clk(clk), .rst(rst), .d(sum_int[4]), .q(sum[4]));
    dff dff_cout (.clk(clk), .rst(rst), .d(cout_int), .q(cout));

endmodule
```

Listing 4: Top-level 5-bit CLA adder module

B. Testbench

```
`timescale 1ns/1ps

module tb_cla_adder_5bit;

    // DUT inputs
    reg clk;
    reg rst;
    reg [4:0] a;
    reg [4:0] b;

    // DUT outputs
    wire [4:0] sum;
    wire cout;
```

```
    // Instantiate DUT
    cla_adder_5bit uut (
        .clk(clk),
        .rst(rst),
        .a(a),
        .b(b),
        .sum(sum),
        .cout(cout)
    );

    // Clock generation: 10 ns period (100 MHz)
    always #5 clk = ~clk;

    // Dump waveforms for GTKWave
    initial begin
        $dumpfile("cla_adder_5bit.vcd");
        $dumpvars(0, tb_cla_adder_5bit);
    end

    // Test procedure
    initial begin
        // Initialize
        clk = 0;
        rst = 1;
        a = 0;
        b = 0;

        // Apply reset for 2 clock cycles
        #20;
        rst = 0;

        // Test case 1: Simple add
        a = 5'b00011;   // 3
        b = 5'b00101;   // 5
        #20;

        // Test case 2: Larger numbers
        a = 5'b01111;   // 15
        b = 5'b00001;   // 1
        #20;

        // Test case 3: More larger numbers
        a = 5'b10101;   // 21
        b = 5'b01011;   // 11
        #20;

        // Test case 4: All ones (carry overflow check)
        a = 5'b11111;   // 31
        b = 5'b11111;   // 31
        #20;

        // Test case 5: Random pattern
        a = 5'b10010;
        b = 5'b01101;
        #20;

        // End simulation
        #20;
        $finish;
    end

    // Monitor results
    initial begin
        $display("Time\tclk\trst\ta\tb\t|\tsum\tcout");
        $monitor("%0t\t%b\t%b\t%05b\t%05b\t|\t%05b\t%b",
                 $time, clk, rst, a, b, sum, cout);
    end
endmodule
```

Listing 5: Verilog testbench for functional verification

C. Simulation Results

The Verilog functional simulation confirms correct operation for all test cases. The waveforms match the expected behavior from NGSPICE simulations. The exhaustive verification with all 1024 possible input combinations (32×32) validates complete functional correctness of the design.

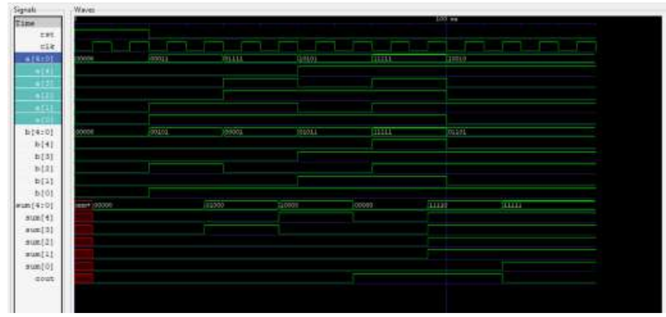

Fig. 45: GTKWave simulation waveforms for selected test cases

Fig. 46: GTKWave simulation waveforms for all 1024 exhaustive test cases

X. FPGA Implementation

A. FPGA Platform

- FPGA Board: [Specify board name and model]
- FPGA Device: SPARTAN-7 (XC7S50CSGA324-1)
- Development Tool: Xilinx Vivado Design Suite

B. RTL Schematic

The synthesized RTL schematic shows the hierarchical structure of the 5-bit CLA adder as interpreted by the synthesis tool:

C. Synthesis Results

D. Hardware Test Setup

The FPGA implementation was tested in the laboratory with a complete hardware setup including the FPGA development board, power supply connections, input switches for operands, LED indicators for outputs, and oscilloscope probes for real-time waveform monitoring.

E. Vivado Simulation

F. Hardware Oscilloscope Verification

The designed 5-bit CLA adder was implemented on the FPGA hardware and verified using an oscilloscope to capture real-time output waveforms. Two test cases were conducted to validate the functionality:

Test Case 1: A[4:0] = 11111 (31), B[4:0] = 00000 (0)

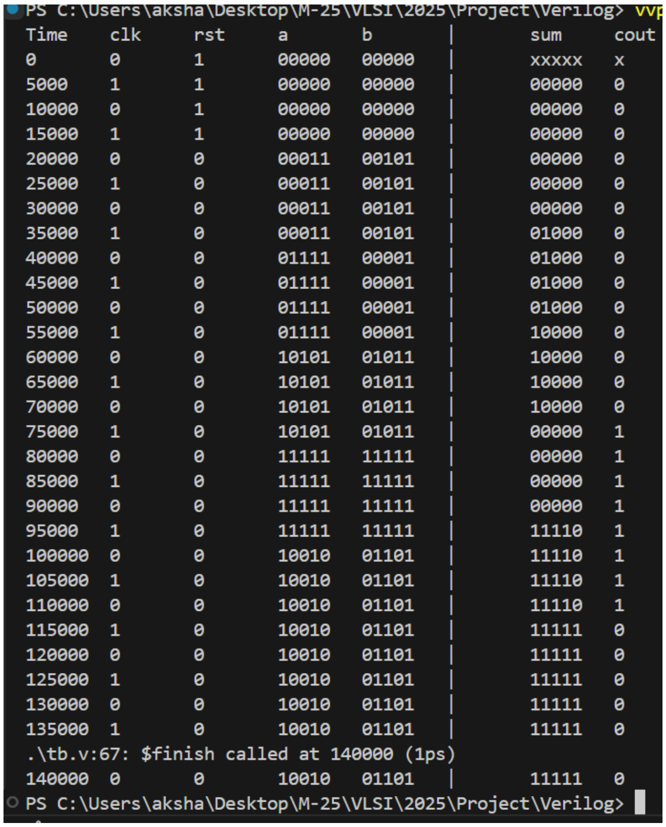

Fig. 47: Verilog simulation console output showing test results

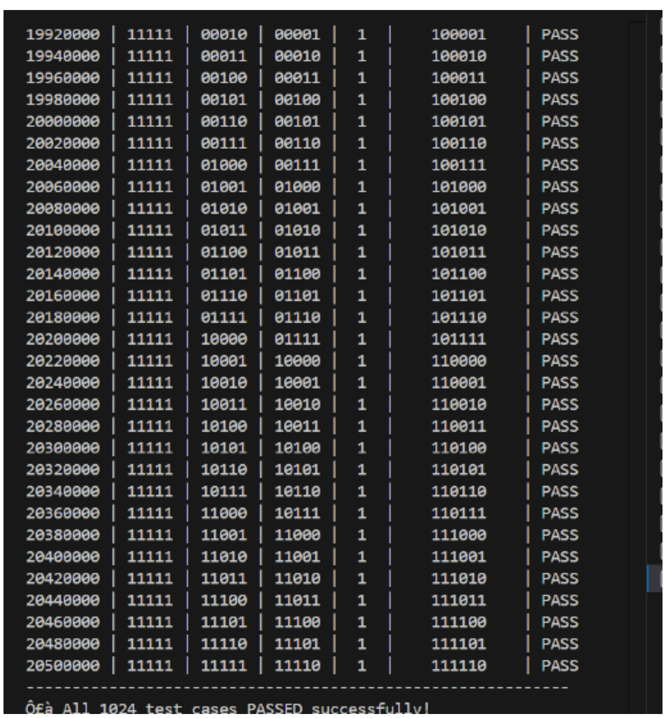

Fig. 48: Verilog exhaustive test console output (1024 test cases)

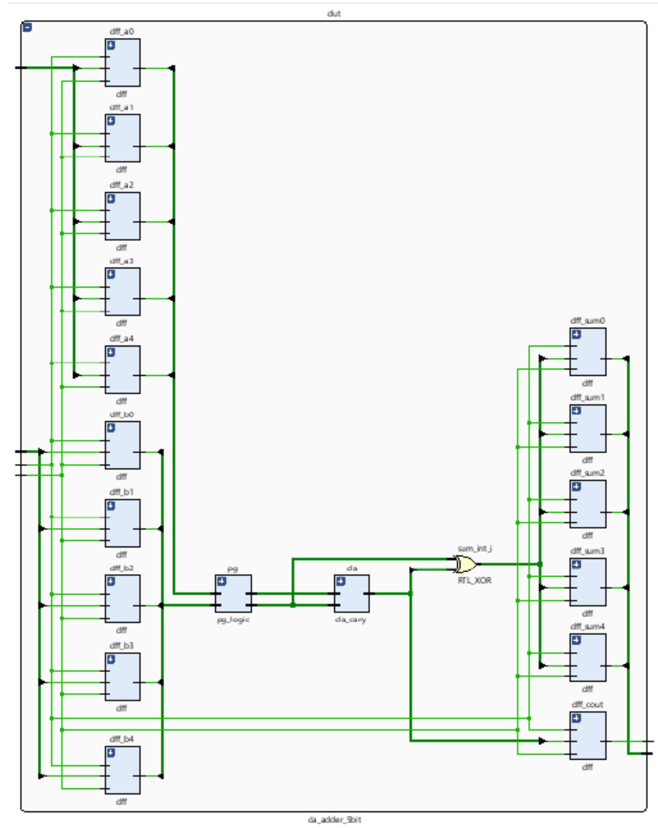

Fig. 49: Top-level RTL schematic of 5-bit CLA adder

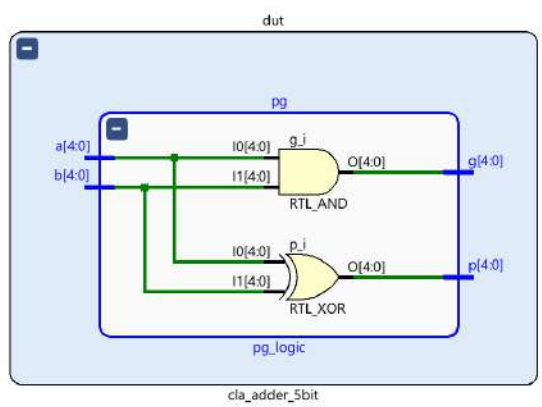

Fig. 50: D Flip-Flop RTL schematic

- Expected Result: Sum[4:0] = 11111 (31), Carry_out = 0

Test Case 2: A[4:0] = 11111 (31), B[4:0] = 00001 (1)

- Expected Result: Sum[4:0] = 00000 (0), Carry_out = 1
- This test validates the carry propagation and overflow detection

The oscilloscope measurements confirm the correct operation of the FPGA implementation, validating both normal addition and carry overflow scenarios and validating

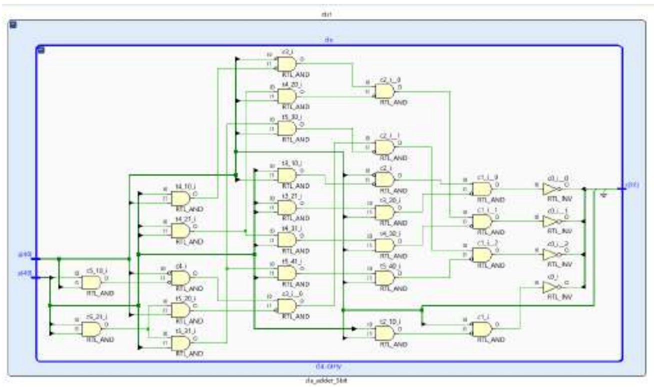

Fig. 51: Carry Look-Ahead logic RTL schematic

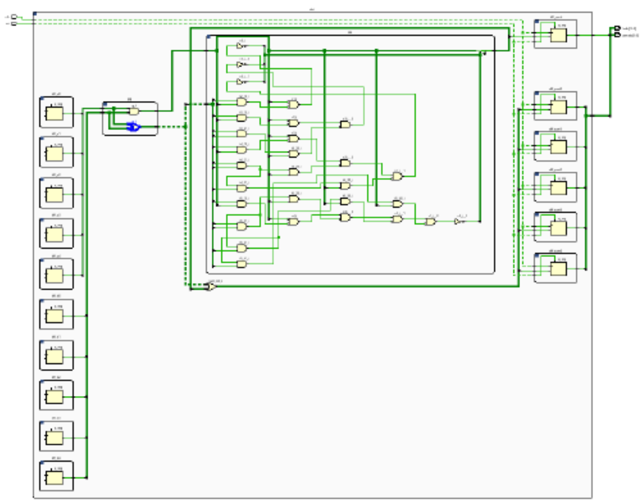

Fig. 52: Propagate and Generate logic RTL schematic

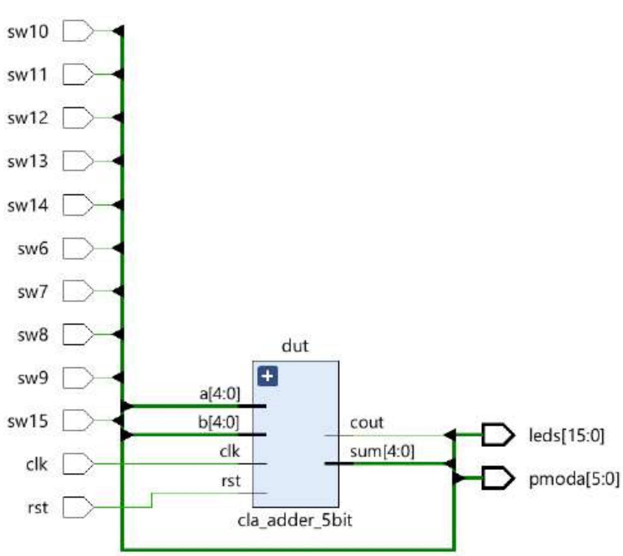

Fig. 53: Sum generation logic RTL schematic

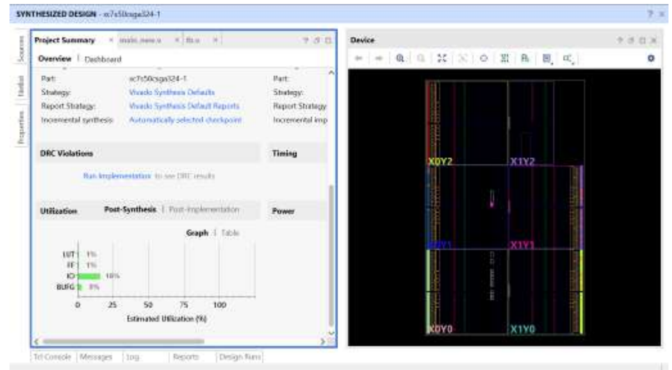

Fig. 54: Vivado synthesis results and resource utilization summary

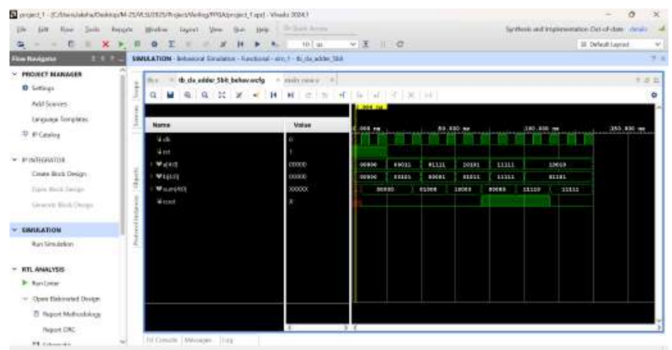

Fig. 55: Vivado Design Suite interface showing project structure

Fig. 56: Complete laboratory setup showing FPGA board, oscilloscope, and test equipment

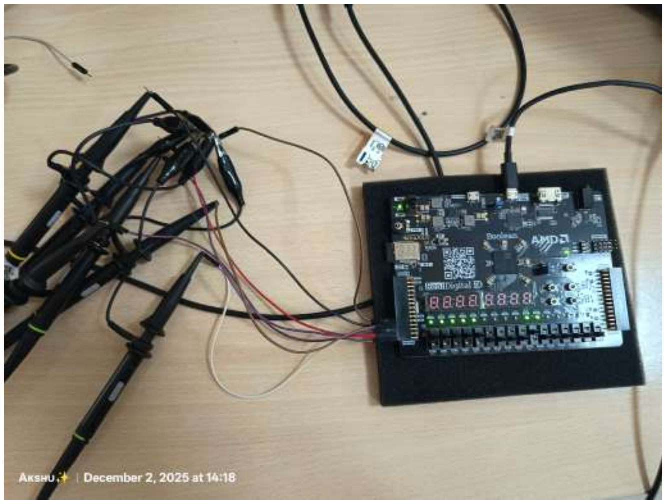

Fig. 57: Detailed view of FPGA board wiring connections with input switches and output probes

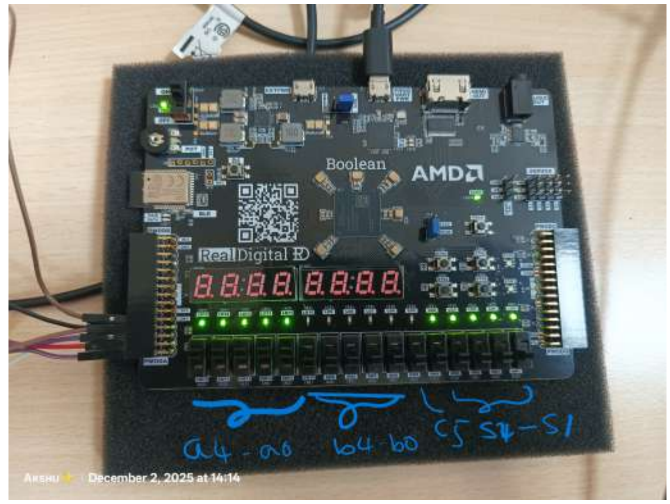

Fig. 59: Hardware oscilloscope capture showing output waveforms for Test Case 1 (Channel 1)

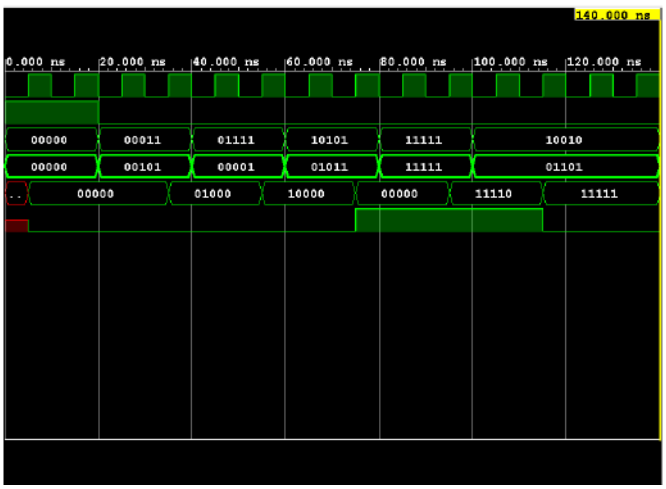

Fig. 58: Vivado waveform viewer showing behavioral simulation results

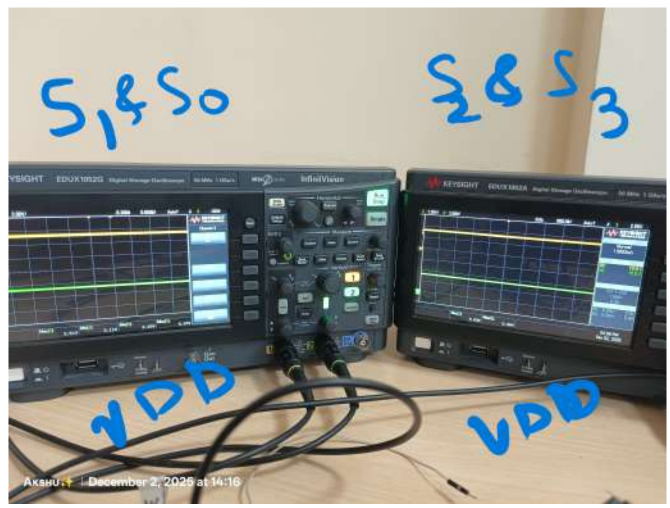

Fig. 60: Hardware oscilloscope capture showing output waveforms for Test Case 1 (Channel 2)

the transition of testcase 1 to testcase 2.

XI. Results and Discussion

A. Performance Summary

The 5-bit Carry Look-Ahead adder implementation achieved the following key metrics:

- **Maximum Operating Frequency**: 1281 MHz (post-layout with parasitics)
- **Critical Path Delay**: 780.64 ps (including D flip-flop delays)
- **Adder Logic Delay**: 609.2 ps (worst-case combinational path)
- **Technology**: TSMC 180nm CMOS process
- **Supply Voltage**: 1.8V
- **Total Transistors**: 16 D flip-flops + CLA logic gates

B. Performance Analysis

1) Comparison with Ripple Carry Adder: The 5-bit CLA demonstrates superior performance compared to conventional ripple carry adders:

- **Reduced Propagation Delay**: The Carry Look-Ahead block eliminates sequential carry propagation, achieving logarithmic delay complexity O(log n) versus linear delay O(n) in ripple carry adders
- **Optimized Design**: Our final circuit is highly optimized such that the designed 5-bit CLA provides comparable delay to a conventional 4-bit ripple carry adder, demonstrating significant performance improvement
- **NAND-based Implementation**: The complete circuit uses NAND gates as the primary logic building block, providing reduced delays compared to complex

Fig. 61: Hardware oscilloscope capture showing output waveforms for Test Case 1 (Channel 3)

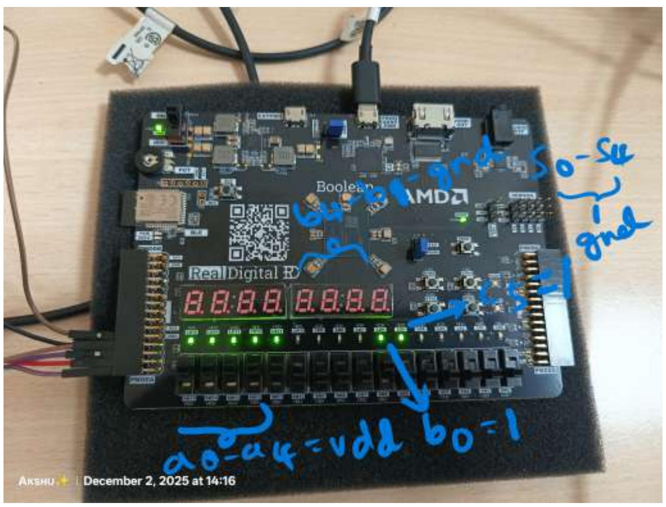

Fig. 62: Hardware oscilloscope capture showing output transition when B0 changes from 0 to 1 (Channel 1)

- gate implementations. This offers an area-delay trade-off in XOR gate implementation

2) Implementation Method Analysis: For the carry generation logic, two primary CMOS implementation approaches were evaluated:

- **Direct CMOS Implementation**: This approach has a very complex structure resulting in larger propagation delays and increased area overhead
- **Manchester Chain Implementation**: Though faster than direct CMOS, the Manchester chain is complex to implement as a complete system, especially when integrating with D flip-flops for pipelined operation. This complexity makes it suitable for future optimization work
- **Selected Approach**: NAND-based implementation was chosen for the current design, balancing performance, area, and design complexity

Fig. 63: Hardware oscilloscope capture showing Sum output changing from 11111 to 00000 for Test Case 2 (Channel 2)

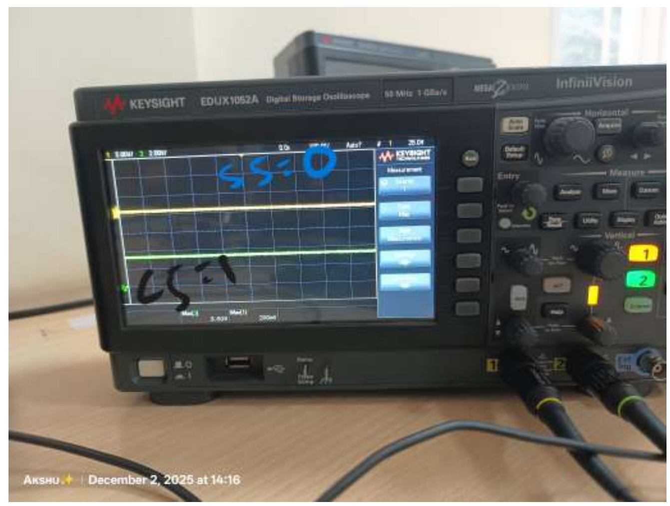

Fig. 64: Hardware oscilloscope capture showing Carry_out transition from 0 to 1 for Test Case 2 (Channel 3)

C. Design Trade-offs

1) Advantages:

- Fast carry computation through parallel Propagate-Generate logic
- Scalable architecture adaptable to larger bit-widths (8-bit, 16-bit, 32-bit)
- TSPC D flip-flop implementation reduces area and power compared to transmission gate designs
- Single clock phase simplifies clock distribution and reduces skew
- Post-layout performance improvement demonstrates effective layout optimization

2) Limitations:

- Increased gate count compared to ripple carry adder (area overhead)
- XOR gate implementation using NAND gates increases transistor count
- Carry-in functionality fixed to 0 in current implementation
- TSPC design requires careful clock edge management

D. Hardware Verification

FPGA implementation and oscilloscope measurements validated:

- Correct functional operation for multiple test cases
- Carry propagation and overflow detection (31+1 = 32, detecting carry-out)
- Real-time waveform capture confirming simulation results
- Practical feasibility of the design for hardware deployment

E. Future Improvements

Potential enhancements to the design include:

- **XOR Gate Optimization**: The current 4-NAND implementation uses 16 transistors per XOR gate. Better implementations exist with fewer gates and reduced delay:
  - Transmission Gate XOR: 6 transistors with lower delay
  - Pass-Transistor Logic: 4-6 transistors with minimal area
  - Direct CMOS XOR: 12 transistors with full rail-to-rail swing

  These alternatives could significantly improve area-delay product and reduce power consumption
- **Manchester Carry Chain**: Implement an optimized and simplified version of the Manchester Carry Look-Ahead Adder to reduce delay further while managing integration complexity with flip-flops. Though Manchester chain is faster than direct CMOS implementation, its complexity in integration with D flip-flops requires careful architectural planning
- **Carry-in Support**: Add configurable carry-in functionality to enable cascading multiple adder blocks for wider bit-width implementations. Current design assumes carry-in = 0
- **Layout Optimization**: Further reduce parasitic capacitances through improved routing strategies and metal layer optimization
- **Power Optimization**: Implement clock gating and multi-threshold CMOS techniques for reduced dynamic and static power
- **Scalability**: Extend to 32-bit or 64-bit implementations using hierarchical CLA architecture

XII. Conclusion

This project successfully designed, implemented, and verified a 5-bit Carry Look-Ahead adder using TSMC 180nm CMOS technology. The design achieved a post-layout propagation delay of 609.2ps with a maximum operating frequency of 1281 MHz, demonstrating significant performance improvement over traditional ripple carry adders.

The implementation achieved performance comparable to conventional 4-bit adders despite being a 5-bit design, validating the effectiveness of the Carry Look-Ahead architecture. Both pre-layout and post-layout simulations confirmed functionality and timing characteristics, with post-layout results showing minimal performance degradation due to effective layout optimization.

Key achievements include:

- Complete VLSI design flow execution from circuit design to physical layout
- TSPC D flip-flop based pipelined architecture with 16 flip-flops
- NAND-gate based implementation providing optimal area-delay tradeoff
- Successful DRC and LVS verification in MAGIC layout tool
- Verilog HDL structural implementation validated through simulation
- FPGA prototyping with hardware oscilloscope verification
- Timing analysis confirming setup and hold time constraints satisfaction

The project provided comprehensive hands-on experience with CMOS circuit design, transistor-level optimization, physical layout techniques, timing analysis, HDL implementation, and hardware prototyping. The complete design flow demonstrates practical considerations in VLSI design including the impact of parasitic effects, importance of multi-level verification, and trade-offs between speed, area, and power.

Future work can focus on Manchester chain implementation for further delay reduction, XOR gate optimization for area efficiency, and extension to wider bit-widths using hierarchical CLA structures.

Acknowledgment

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