ANALOG ELECTRONIC CIRCUITS

LAB REPORT-5

BJT Amplifiers

1) DC Analysis :

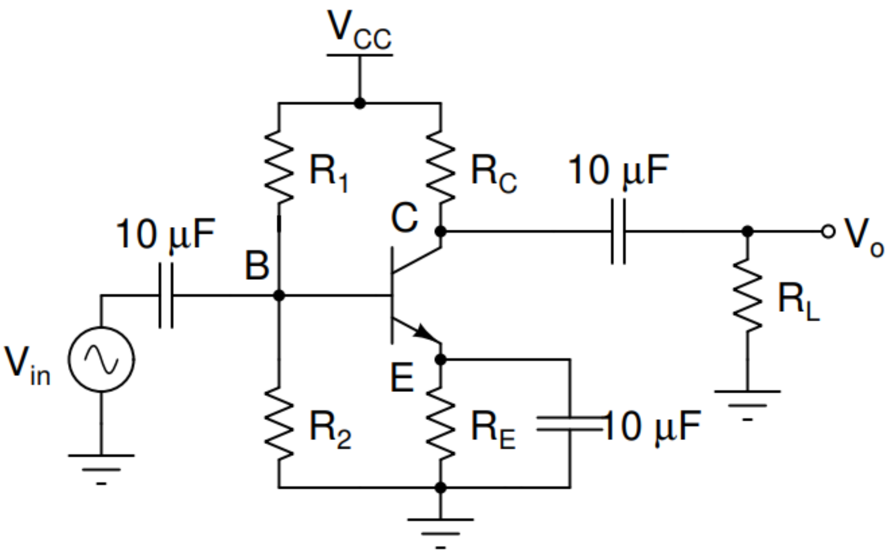

Figure 1: Single stage common emitter voltage amplifier

R1=5.6 k ohm and R2= 1k ohm [Given] ;

Collector- current(Ic)=1.5m A ;

RL = 1 kΩ and VCC = 12 V

Mid-band voltage gain(Vout/Vin) = 5

We need to find values of Rc and RE .

To achieve a collector current of 1.5 mA and a midband voltage gain of 5 using DC signal analysis, the values of resistors RC and RE need to be determined.

To get Mid Band Voltage Gain of 5V, We have formula**,**

Av = -gm * (RC || RL)

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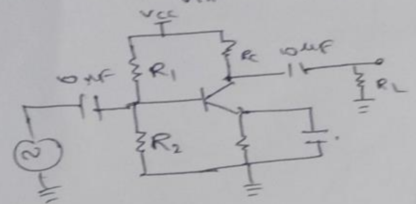
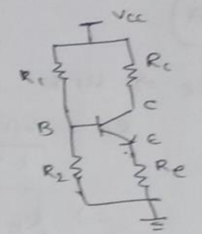
mid-band voltage gain $\Rightarrow \left(\frac{V_{out}}{V_{in}}\right)$

$$A_m = \frac{V_{out}}{V_{in}} = -g_m * (R_C \parallel R_L)$$



$\Rightarrow$ equivalent to



$R_C = ?$, $R_E = ?$

$$V_B = \left(\frac{R_2}{R_1+R_2}\right)V_{cc}$$

$$= \frac{12 \times (1K)}{5.6+1K\Omega} = \frac{12}{6.6} = 1.81V \Rightarrow \boxed{V_B = 1.81V}$$

$$V_{BE} = V_B - V_E$$

$$V_E = V_B - V_{BE}$$

$$= 1.81 - 0.7 \Rightarrow \boxed{V_E = 1.118\,V}$$

We know $I_E = I_B + I_C$

Given, β is high $\therefore I_B \approx 0 \Rightarrow I_E = I_C$

$$V_C = V_{CC} - I_C R_C \Rightarrow 12 - \frac{V_E}{R_E}(R_C) = \quad \left[I_C = I_E = \frac{V_E}{R_E}\right]$$

$$\boxed{I_C = \frac{\beta}{\beta+1} I_E}$$

as Given $I_E = 1.5$, $\Rightarrow I_E = 1.5 \times \frac{151}{150}$ $\left(I_E = \frac{\beta+1}{\beta} I_C\right)$

$$= \boxed{I_E = 1.51\,mA}$$

Hence $I_E \approx I_C$

$I_B = \frac{I_C}{\beta} = \frac{1.51}{151} \simeq 0.01\,mA$

$\therefore I_B = 10^{-2}\,mA$

$= 10^{-5}\,A$

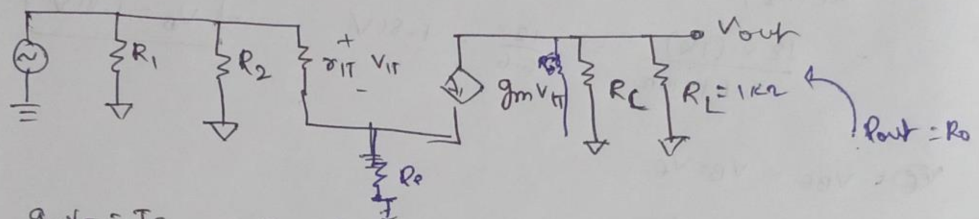
$\therefore \boxed{I_B = 10^{-2}\,mA}$

$V_E = I_E R_e \Rightarrow 1118$

$R_e = \frac{1118}{1.51} \times 10^3$

$\Rightarrow \boxed{R_e = 740.397\,\Omega}$

Small signal Analysis of Given circuit:



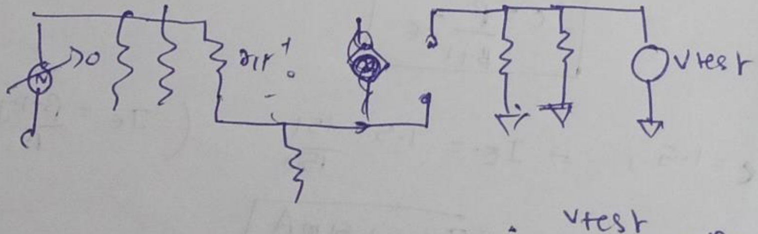
$g_m V_\pi = I_C \Rightarrow I_C = \frac{g_m}{V_\pi}$ $\quad V_\pi = V_{BE}$

$\Rightarrow$

$\therefore \cancel{I_C = 1.5m}$

$g_m = \frac{I_C}{V_\pi} \Rightarrow \frac{1.5\,mA}{25\,mV} = 15/250 = 0.06$

For calculating Rout



$\frac{V_{test}}{I_{test}} = R_{out} = R_C \parallel R_L$

low distortion → means good quality of producing output.

THD → rms ~~value~~ of total harmonics / rms of fundamental wave

→ calculate noise

* unitless

THD ≥ 0 (always)

for $R_L = 980\,\Omega$

& $R_c = 100\,\Omega$

gain = 5.44 (Affirm)

vin - 2mv

five harmonic THD

freq ?

vin - - -

all THD's calculated

gain = $g_m R_o$, $g_m = \frac{I_c}{V_T}$

$= \frac{1.5 \times 10^{-3}}{26 \times 10^{-3}} = \frac{1.5}{26} \Rightarrow$

$= 0.0576$

$(V_T = 26mV$

$\frac{V_{out}}{V_{in}} = g_m R_o \Rightarrow \frac{5}{0.057} = \boxed{87.719 = R_o}$

$\Rightarrow g_m V_{be} = 0.057 \times 0.7$

$= 0.0399 \approx 0.04$

$R_c \parallel R_L = 87.719$

$R_L = 1000\,\Omega$

$\frac{R_c R_L}{R_c + R_L} = 87.719 \Rightarrow \frac{1 \times 10^3 \times R_c}{10^3 + R_c} = 87.719$

$R_c = 87.719 \times 10^3 + 87.719 R_c = 1000 R_c$

$= 912.3 R_c = 87.719 \times 10^3$

$R_c = 87.719$

$= 96.1514\,\Omega$

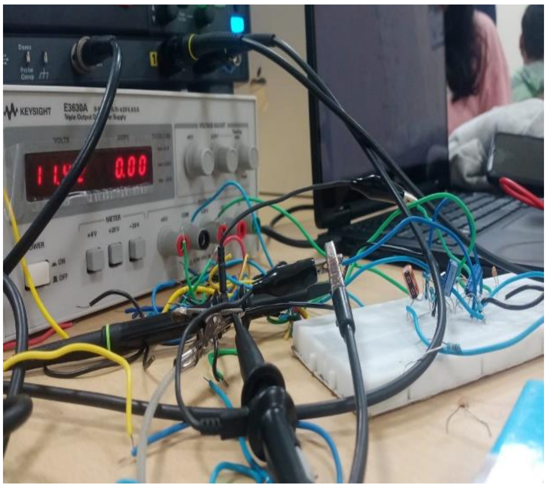
From the DC Analysis we got values of R_E and R_C

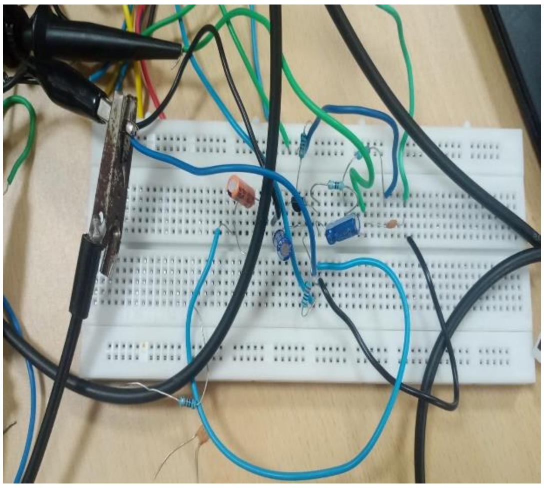
R_E =740.397 ohm

R_C = 96.1514 ohm

2) Transient Response and Total Harmonic Distortion:

a) Connected the circuit as given in figure (Lab Manual):





b)

Input:

Vin= Sine wave of amplitude 25 mV

Freq=1 kHz

RL =1 k ohm

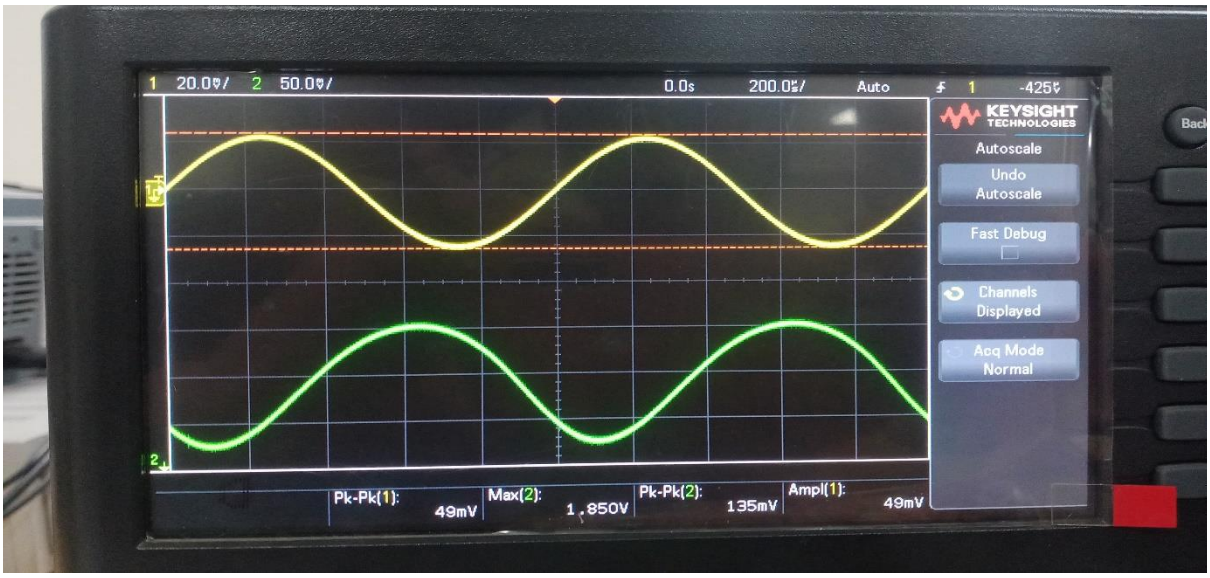
c)

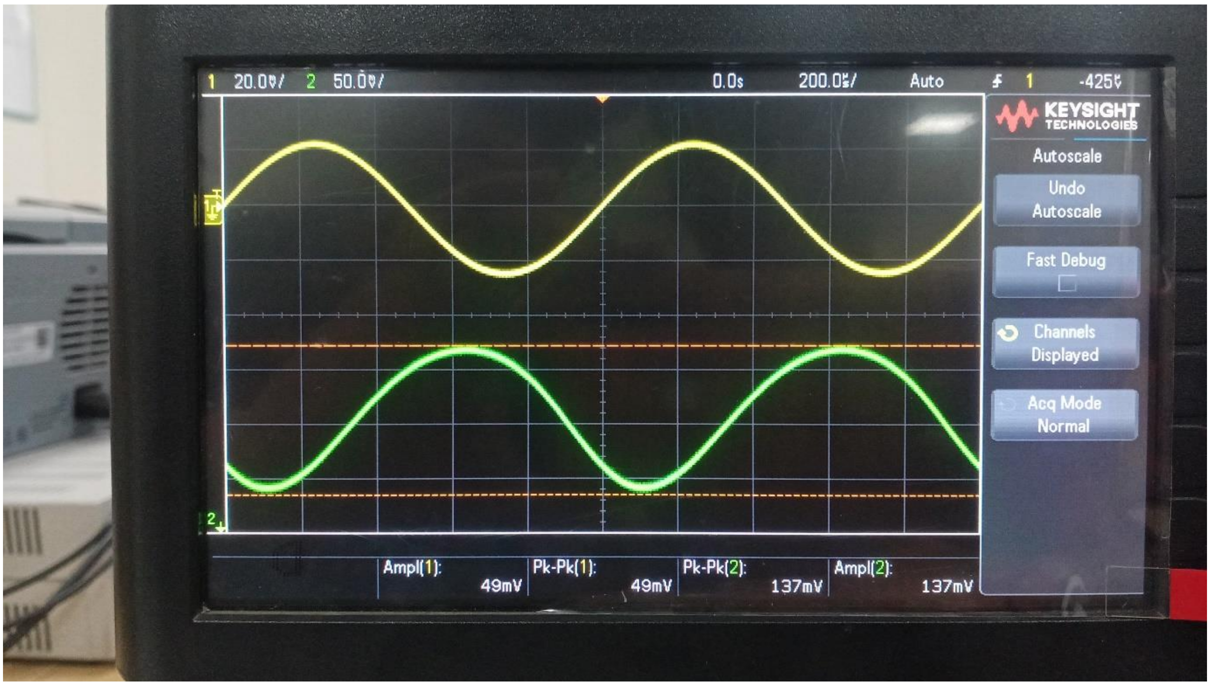
Now measure the amplitude of the output voltage (Vo) produced by the amplifier. Then, calculate the voltage gain (Av) of the amplifier by dividing the output voltage amplitude by the input voltage amplitude.

gain=gm * Ro =IC/VT(RC||RL)

=1.5/25 * (980* 100)/1080=5.44

Theoretical gain=5.44.





From above Aanlysis:

Vo=137mV

Vin=49mV

Therefore gain =V0/Vin =>137/49=2.795

Hence gain= 2.795

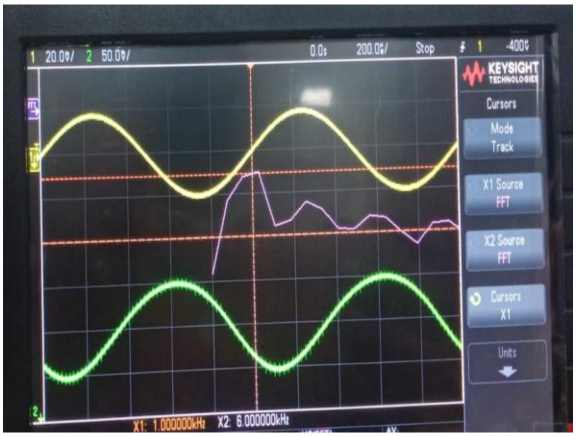
d)

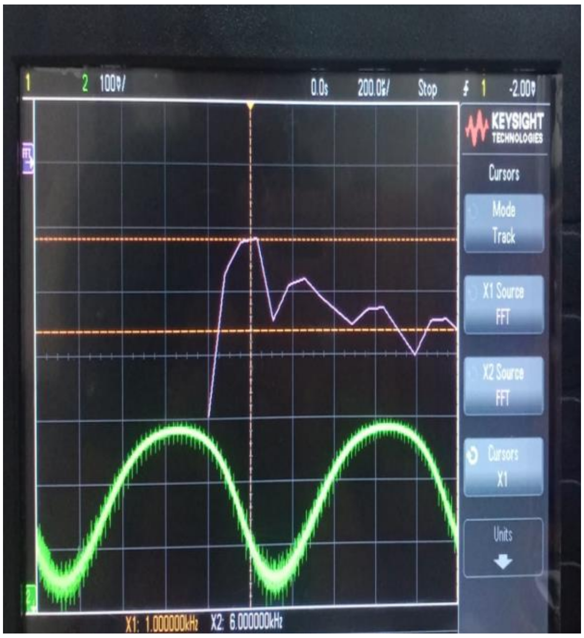
Now record the amplitudes of the fundamental component (V1) and the 2nd to 5th harmonics for various amplitudes (Vin) of the input signal.

The suggested values for Vin are 2 mV, 10 mV, 20 mV, 50 mV, 100 mV, 500 mV, and 1 V.

Then use FFT analysis to measure the harmonics.

THD= sqrt(($V2^2$)+($V3^2$)+($V4^2$)+($V5^2$)/$V1^2$)

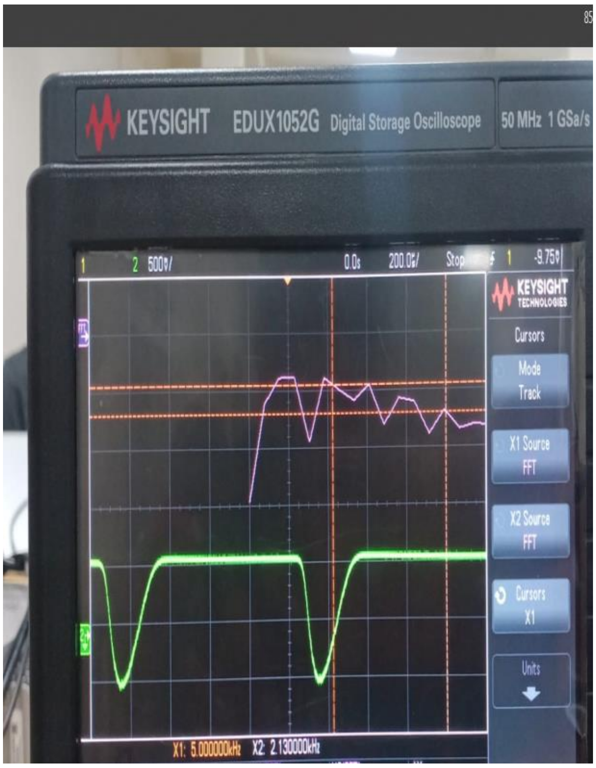


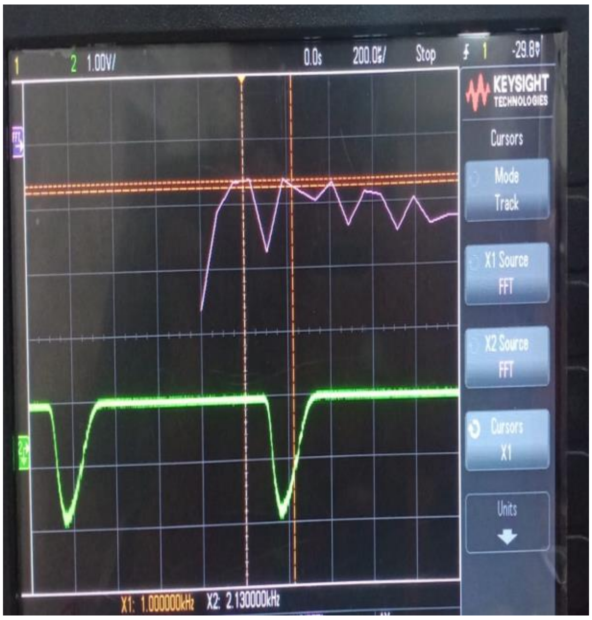



200mV/
0.0s
200.0µs/
Stop
KEYSIGHT TECHNOLOGIES
Cursors
Mode Track
X1 Source FFT
X2 Source FFT
Cursors X1
Units
X1: 1.000000kHz X2: 2.230000kHz


200mV/
0.0s
200.0µs/
Stop
-6.00V
KEYSIGHT TECHNOLOGIES
Cursors
Mode Track
X1 Source FFT
X2 Source FFT
Cursors X1
Units
X1: 5.340000kHz X2: 2.230000kHz


500mV/
0.0s
Stop
KEYSIGHT TECHNOLOGIES
Cursors
Mode Track
X1 Source FFT
X2 Source FFT
Cursors X1
Units
X1: 1.000000kHz X2: 2.130000kHz


KEYSIGHT EDUX1052G Digital Storage Oscilloscope 50 MHz 1 GSa/s
500mV/
0.0s
200.0µs/
Stop
-9.75V
KEYSIGHT TECHNOLOGIES
Cursors
Mode Track
X1 Source FFT
X2 Source FFT
Cursors X1
Units
X1: 5.000000kHz X2: 2.130000kHz



Vin	V1	V2	V3	V4	V5	THD
2mV	-46.3	-62.180	-73.23	-77.43	-80.119	0.1692
10 mV	-35.623	-51.25	-56.25	-60.24	-70.021	0.1996
20 mV	-29.37	-44.37	-50.625	-54.09	-56.873	0.2118
50 mV	-23.12	-37.49	-43.75	-49.38	-49.38	0.2283
100mV	-16.25	-30.624	-36.875	-43.129	-43.12	0.2258
500mV	-3.125	-16.876	-23.124	-31.874	-31.87	0.237
1 V	-1.875	-10.09	-17.55	-23.131	-23.124	0.465

3)Frequency Response:

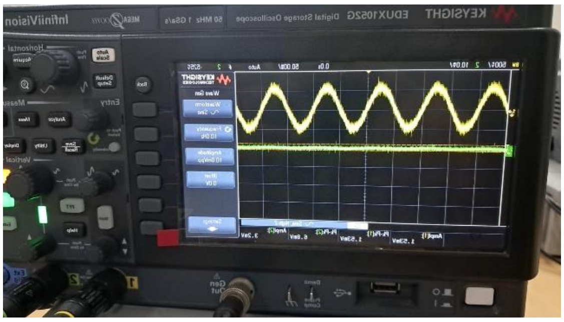
a)

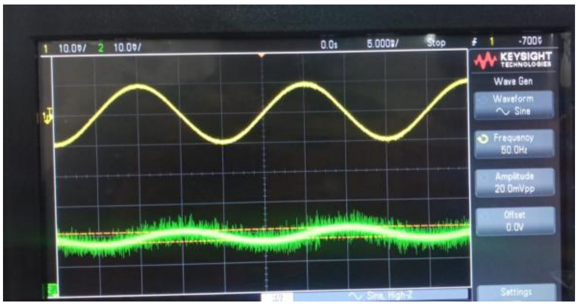
Input :

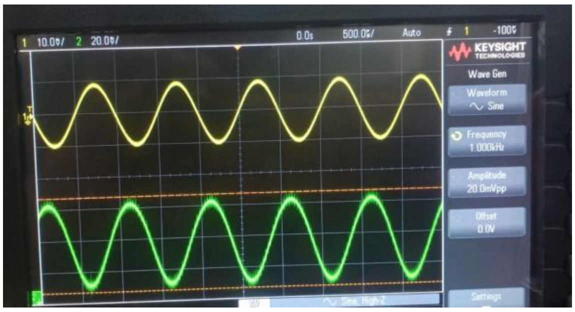
R(Load)=1 k ohm

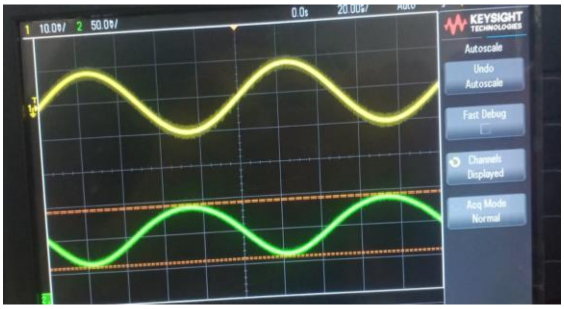
Vin=10 mV

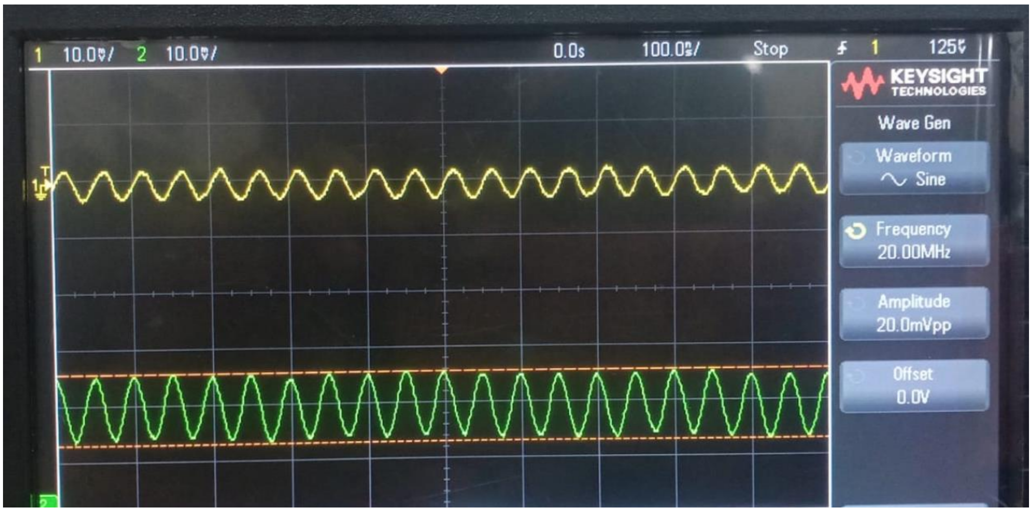
Vary Fin from 10 Hz to 20 MHz

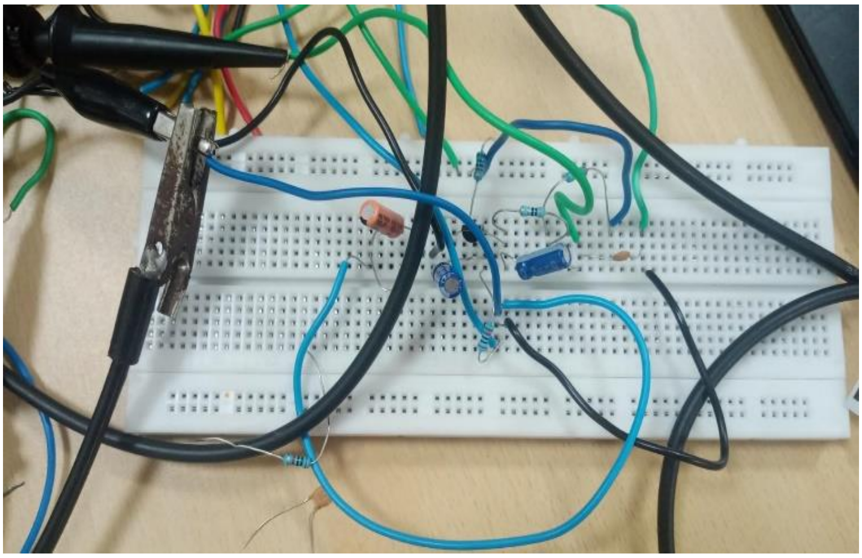










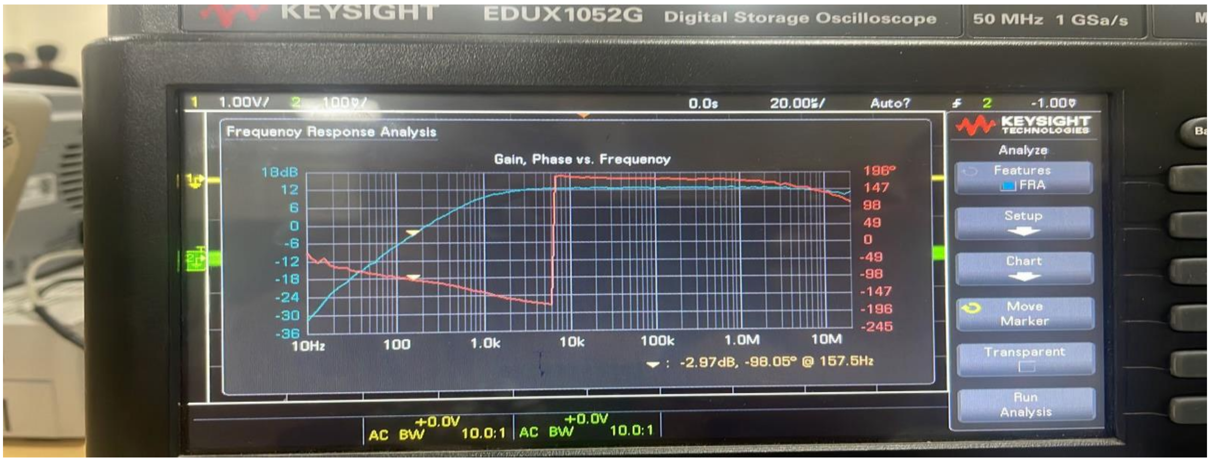


The readings are noted under the table below.

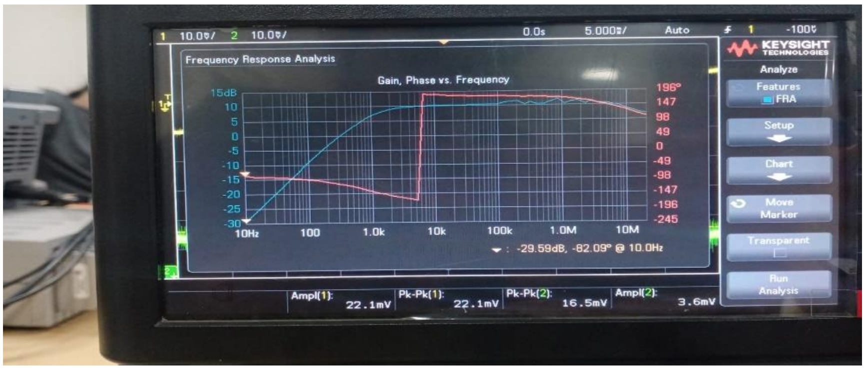
Freq(in)	V(in) mV	V(out) mV	Av=V(out)/V(in)	Av(db.)
100Hz	10.7	10.9	1	0
500Hz	10.5	23.4	2.32	7.3
1KHz	10.8	32.23	3.15	8.87
10KHz	10.6	45.2	4.31	12.43
100KHz	10.6	45.2	4.31	11.95
1MHz	10.3	41	3.88	11.96
10MHz	10.9	58	5.50	14.13
20MHz	7	26	3.28	10.45

b)

F_L= 156.8 (approx)



Fin	Av(in dB)
100	-9.59
500	5.11
1k	11.59
10k	16.56
100k	16.40
1m	15.66
10m	11
20m	8.3



The graph does not show the -3dB cutoff frequency at higher frequencies because the parasitic capacitance in the circuit is typically very low.

This low capacitance value results in a high cutoff frequency that exceeds the maximum frequency range supported by the Digital storage oscilloscope (DSO) in use.

$$F=1/2*pi*RC$$

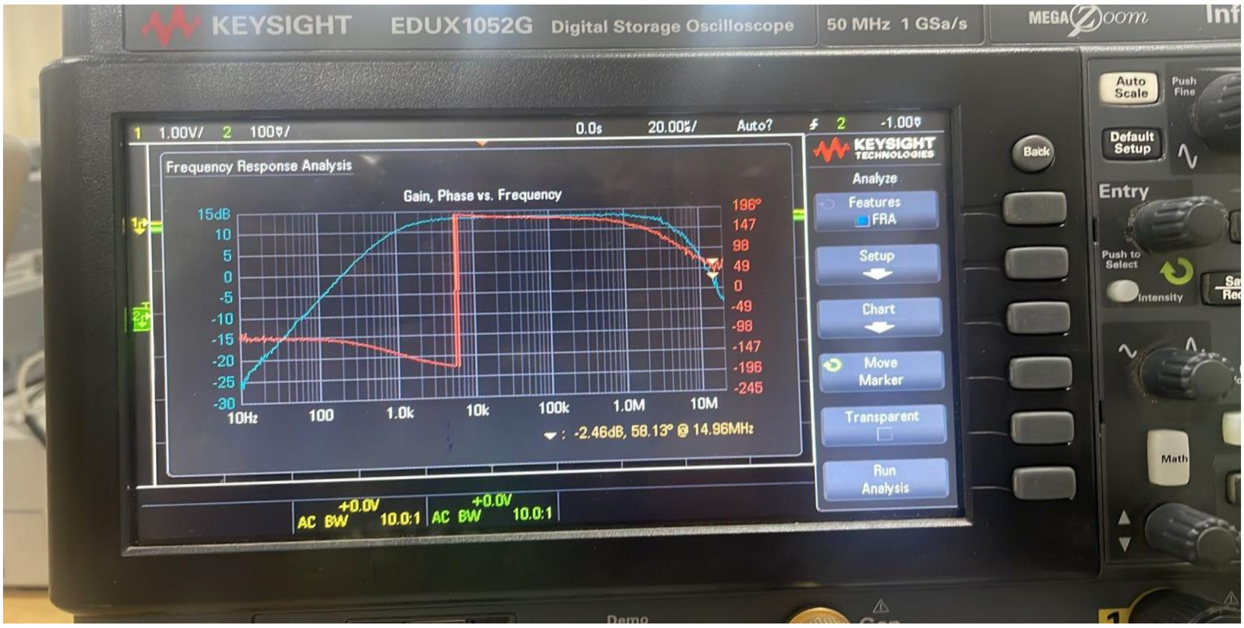
As a result, the high-frequency cutoff region of the graph, where the voltage gain begins to decrease, is not visible in DSO. The equipment's limitations prevent us from observing the circuit's entire frequency response, especially at higher frequencies due to the high cutoff frequency caused by the low parasitic capacitance.

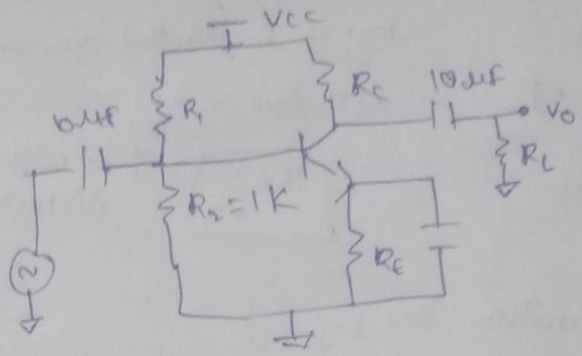
c)

Measured value of F_L and F_H:

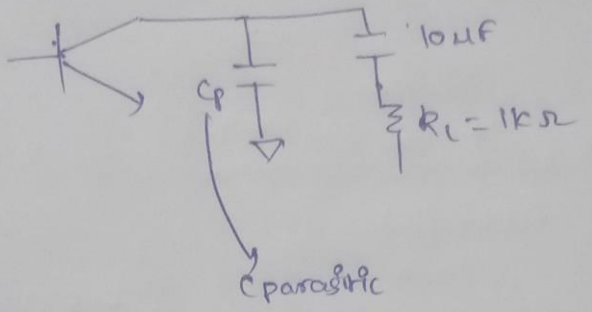
F_L=136.33 Hz (approx.)

F_H= 15 M Hz (approx.)





Parasitic capacitances will be there,



* f_H can't be ~~oth~~ ~~belo~~ calculated for with R_L.

With capacitor

From Datasheet

parasitic capacitance = 1.7 PF

$$f_H = \frac{1}{2\pi (R_C \| R_L) C_{parasitic}}$$

f_H = → We can calculate from Here

$f_H \approx$ ~~calc~~ Experimental value $\approx 15\ Hz$.

$$f_L = \frac{1}{2\pi (R_{in}) C_{eq}}$$

↳ can calculate f_L.

Fin	Av (in dB)
10	-24.05
50	-10.79
100	-7.86
500	6.28
1k	12.7
10k	17.64
100k	17.45
1M	16.55
10M	-2.49
20M	-12.95

d)

In this case, we are able to observe the cutoff frequency because of the presence of the capacitor at the load (CL). This capacitor, due to its configuration, acts as a low-pass filter, allowing only lower frequencies to pass through while attenuating higher frequencies.

The capacitor limits the circuit's bandwidth by reducing the amplitude of higher frequencies.

The frequency response graph shows how high-frequency components are cut off. The capacitor at the load affects the cutoff frequency and overall frequency response of the circuit.