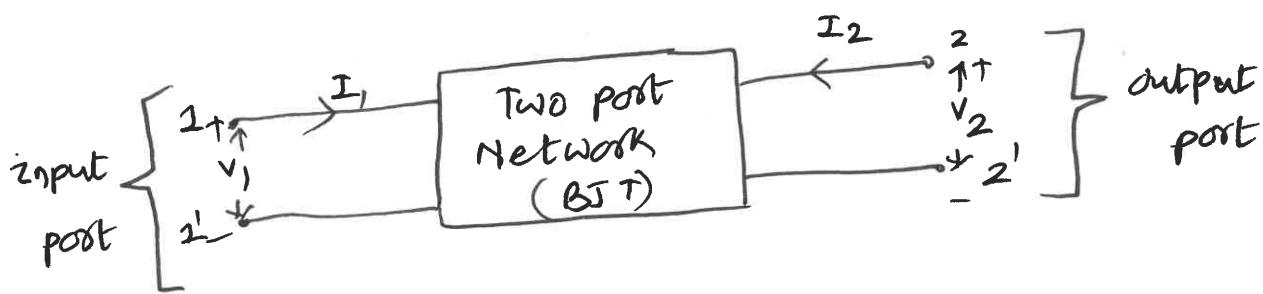


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# Analysis of Transistor (BJT) amplifier using h-parameters.



Hybrid parameters:

$$V_1 = h_{11} I_1 + h_{12} V_2$$

$$I_2 = h_{21} I_1 + h_{22} V_2$$

$$\begin{matrix} 11 & h_1 \\ 12 & h_2 \\ 21 & h_3 \\ 22 & h_4 \end{matrix}$$

$$h_{11} = \left. \frac{V_1}{I_1} \right|_{V_2=0} = h_i \quad [\text{input impedance } i^{\circ}\text{s}]$$

(Output port is short circuited)

$$h_{12} = \left. \frac{V_1}{V_2} \right|_{I_1=0} = h_\pi \quad [\text{Reverse Voltage gain}]$$

(Input port is open circuit)

$$h_{21} = \left. \frac{I_2}{I_1} \right|_{V_2=0} = h_f \quad [\text{Forward current gain}]$$

$$h_{22} = \left. \frac{I_2}{V_2} \right|_{I_1=0} = h_o \quad [\text{output admittance}] [v^{-1}]$$

∴

$$\boxed{V_1 = h_i I_1 + h_\pi V_2}$$

$$\boxed{I_2 = h_f I_1 + h_o V_2}$$

Depending on transistor configuration, add a second subscript to the h-parameters.

CE →  $h_{ie}$ ,  $h_{re}$ ,  $h_{fe}$ ,  $h_{oe}$   
 CB →  $h_{ib}$ ,  $h_{rb}$ ,  $h_{fb}$ ,  $h_{ob}$   
 CC →  $h_{ic}$ ,  $h_{rc}$ ,  $h_{fc}$ ,  $h_{oc}$

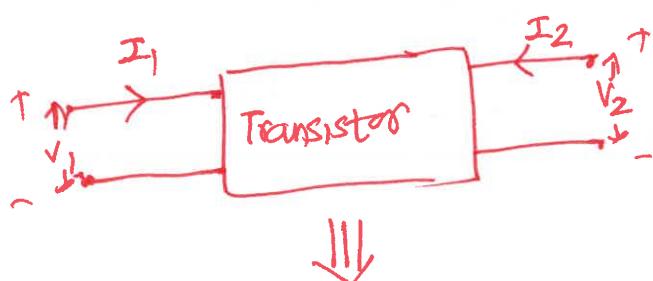
All the h-parameters at room temperature are:

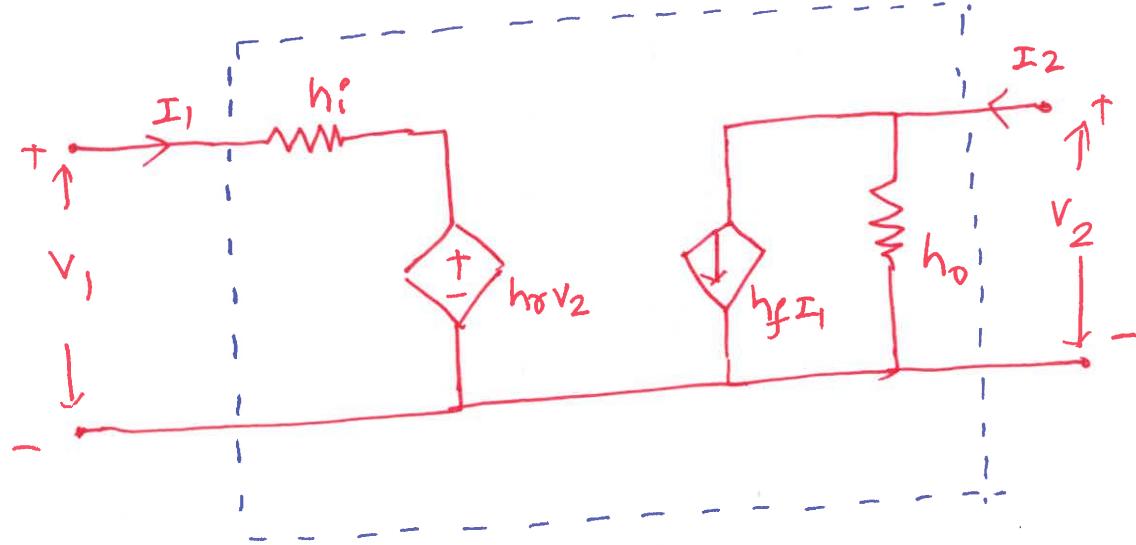
	CE	CB	CC
11	$h_i$	$1100\Omega$	$22\Omega(21.6)$
12	$h_{re}$	$2.5 \times 10^{-4}$	$2.9 \times 10^{-4}$
21	$h_f$	50	-0.98
22	$h_o$	$25MA/V = 25MV$	$0.5MA/V = 0.5MV$
	$\frac{1}{h_{oe}}$	$40k\Omega$	$2M\Omega$
			$40k\Omega$

The Equivalent circuit of transistor  
(or)

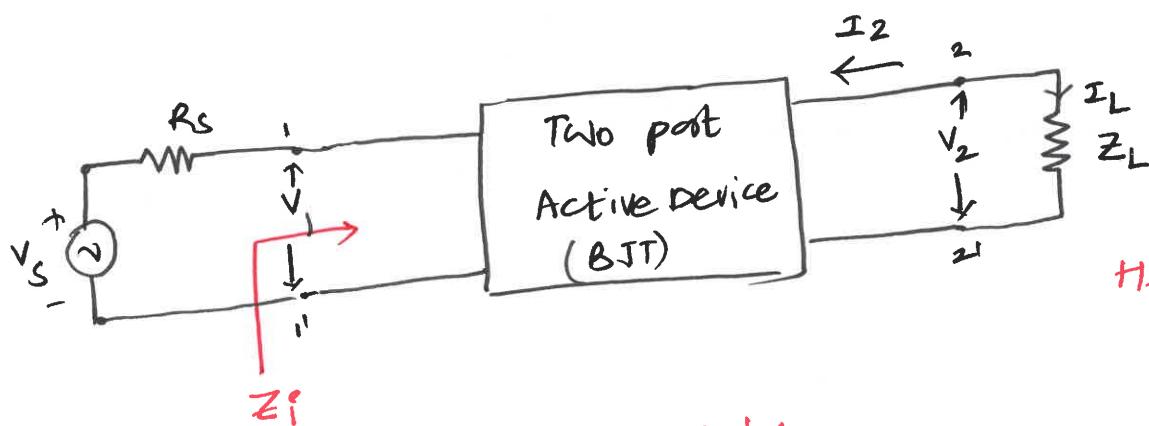
Small signal model of transistor

[This model is valid only for low frequency only]



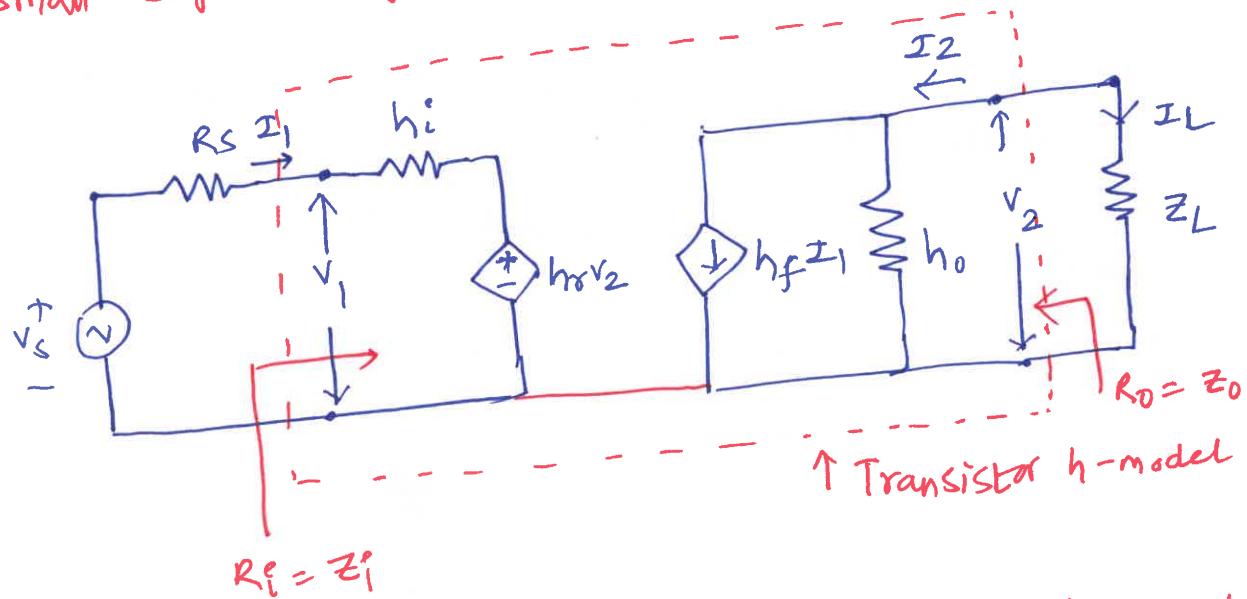


**ANALYSIS OF TRANSISTOR AMPLIFIER USING h-parameters:**



Here  $I_L = -I_2$   
(As per KCL)

**Small signal hybrid model:**



The analysis of transistor amplifier includes the calculation of following

- current gain  $A_I = \frac{I_L}{I_1}$

(ii) Input Impedance :

$$Z_i = \frac{V_1}{I_1}$$

(iii) Voltage gain :

$$A_v = \frac{V_2}{V_1}$$

(iv) Voltage amplification :

$$A_{VS} = \frac{V_2}{V_S}$$

(v) Current amplification :

$$A_{IS} = \frac{I_L}{I_S}$$

(vi) Output impedance

$$Z_o = \frac{V_2}{I_2}$$

(i) Current gain : It is defined as the ratio of output current to the input current.

$$A_I = \frac{I_L}{I_1} = -\frac{I_2}{I_1}$$

From the output circuit

$$I_2 = h_f I_1 + h_o V_2$$

$$\text{since } V_2 = I_L Z_L = -I_2 Z_L$$

$$\therefore I_2 = h_f I_1 + h_o [-I_2 Z_L]$$

$$I_2 + h_o I_2 Z_L = h_f I_1$$

$$I_2 [1 + h_o Z_L] = h_f I_1$$

$$\frac{I_2}{I_1} = \frac{h_f}{1 + h_o Z_L}$$

$$\therefore \text{current gain } (A_I) = \frac{I_L}{I_1} = \frac{-I_2}{I_1} = \frac{-h_f}{1 + h_o Z_L} *$$

(ii) Input Impedance

$$Z_i = \frac{V_1}{I_1}$$

from the input circuit

Apply KVL

$$-V_1 + h_i I_1 + h_\pi V_2 = 0$$

$$V_1 = h_i I_1 + h_\pi V_2$$

$$\frac{V_1}{I_1} = h_i + h_\pi \frac{V_2}{I_1} \rightarrow (1)$$

$$\text{since } V_2 = I_L Z_L = -I_2 Z_L$$

$$\text{we know current gain } A_I = -\frac{I_2}{I_1}$$

$$A_I \times I_1 = -I_2$$

$$\therefore V_2 = -I_2 Z_L = A_I I_1 Z_L$$

$$\therefore \frac{V_2}{I_1} = A_I Z_L$$

From Eq(1)

$$\begin{aligned} Z_i &= \frac{V_1}{I_1} = h_i + h_\pi (A_I Z_L) \\ &= h_i + h_\pi A_I Z_L \rightarrow (2) \end{aligned}$$

$$\therefore Z_i = h_i + h_r \left[ \frac{-h_f}{1+h_o Z_L} \right] Z_L$$

$$= h_i - \frac{h_f h_r Z_L}{1+h_o Z_L}$$

$$= h_i - \frac{h_f h_r}{Y_L + h_o} \rightarrow (3)$$

(iii) Voltage gain

$$A_v = \frac{V_2}{V_1}$$

We know  $V_2 = A_I I_1 Z_L$

$$\therefore A_v = \frac{A_I I_1 Z_L}{V_1} = A_I \times \frac{Z_L}{Z_i}$$

(or)

$$Z_i = \frac{V_1}{I_1} \Rightarrow V_1 = Z_i I_1$$

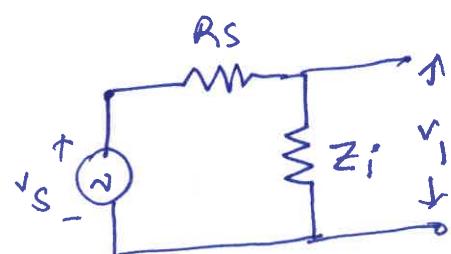
$$\therefore A_v = \frac{V_2}{V_1} = \frac{-I_2 Z_L}{Z_i I_1} = -\frac{I_2}{I_1} \frac{Z_L}{Z_i}$$

$$\boxed{A_v = A_I \times \frac{Z_L}{Z_i}}$$

(iv) Voltage amplification :

$$A_{VS} = \frac{V_2}{V_S}$$

$$A_{VS} = \frac{V_2}{V_1} \times \frac{V_1}{V_S}$$



$$A_{VS} = A_V \times \frac{V_1}{V_S} =$$

$$V_1 = V_S \times \frac{Z_i}{Z_i + R_s} \quad \text{from circuit.}$$

$$\frac{V_1}{V_S} = \frac{Z_i}{Z_i + R_s}$$

$$\therefore A_{VS} = A_V \times \frac{Z_i}{Z_i + R_s}$$

$$\therefore A_{VS} < A_V$$

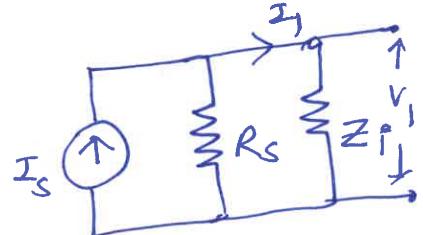
For an ideal voltage source  $R_s = 0 \Rightarrow A_{VS} = A_V$

(V) Current amplification:

$$A_{IS} = \frac{I_L}{I_S}$$

$$A_{IS} = \frac{I_L}{I_I} \times \frac{I_I}{I_S}$$

$$A_{IS} = A_I \times \frac{R_s}{R_s + Z_i}$$



$$I_1 = I_S \times \frac{R_s}{R_s + Z_i}$$

$$A_{IS} < A_I$$

For an ideal current source  $R_s = \infty$

$$A_{IS} = A_I$$

This method of analysis is called exact analysis method.

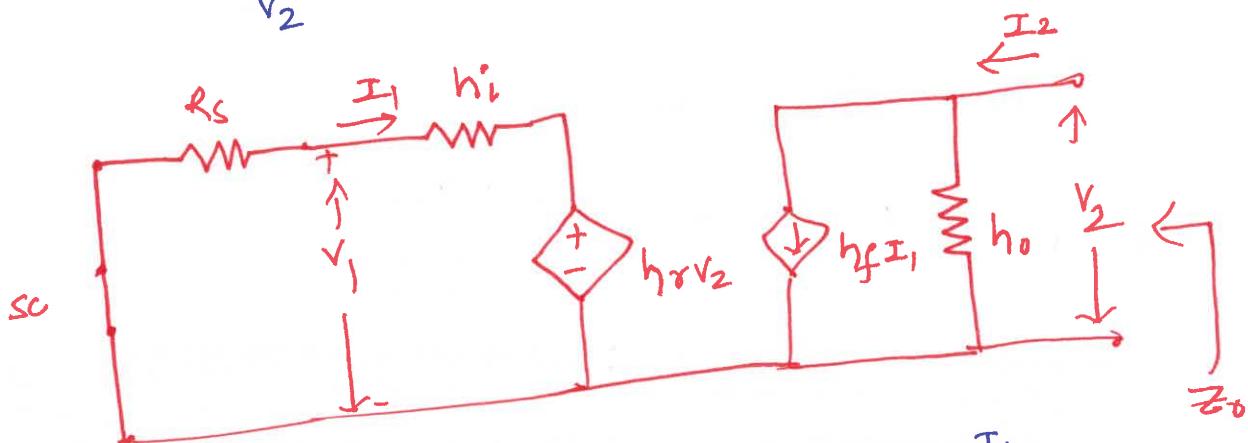
### (vi) output Impedance ( $Z_o$ ):

$$Z_o = \frac{V_2}{I_2} \quad \left| \begin{array}{l} (\text{All sources set equal to zero}) \\ \text{only independent sources} \end{array} \right.$$

$$Y_o = \frac{I_2}{V_2}$$

$$I_2 = h_f I_1 + h_o V_2$$

$$\therefore \frac{I_2}{V_2} = h_f \left( \frac{I_1}{V_2} \right) + h_o$$



To calculate  $Y_o$ , first calculate  $\frac{I_1}{V_2}$

Apply KVL to the input side

$$(R_s + h_i) I_1 + h_r V_2 = 0$$

$$(R_s + h_i) I_1 = -h_r V_2$$

$$\frac{I_1}{V_2} = \frac{-h_r}{R_s + h_i}$$

$$\therefore Y_o = \frac{I_2}{V_2} = h_f \left[ \frac{-h_r}{R_s + h_i} \right] + h_o$$

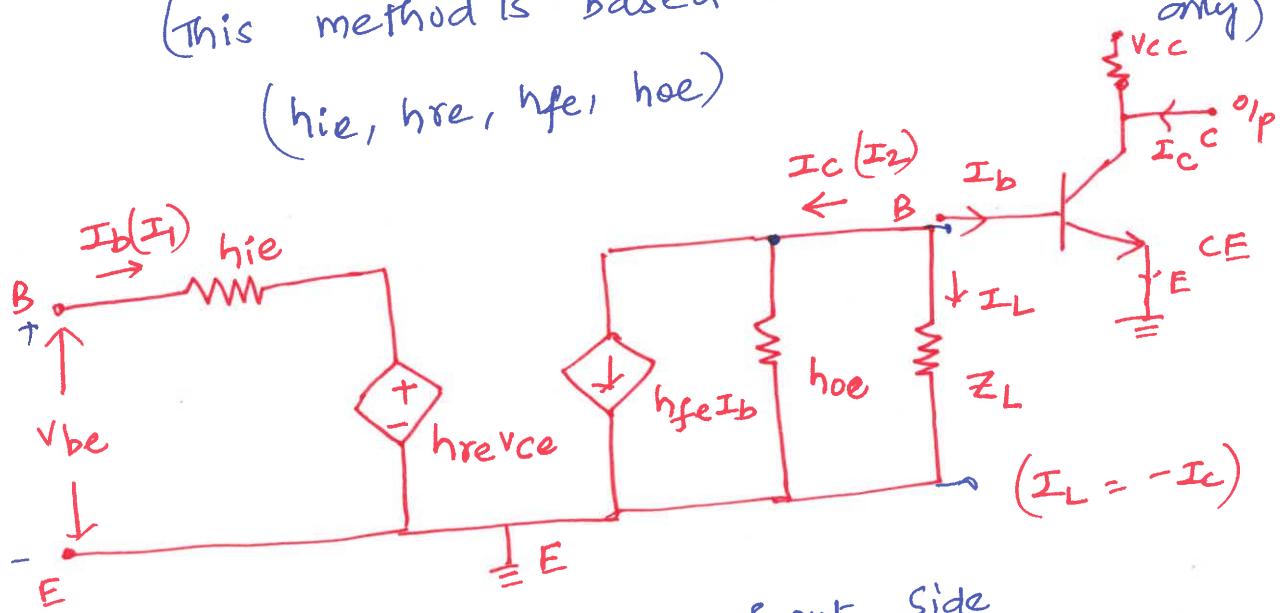
(output admittance)

$$Y_o = h_o - \frac{h_f h_r}{R_s + h_i}$$

$$Z_0 = \frac{1}{Y_0}$$

### SIMPLIFIED (OR) APPROXIMATE METHOD:

(This method is based on CE h-parameters  
( $h_{ie}$ ,  $h_{re}$ ,  $h_{fe}$ ,  $h_{oe}$ )



Writing KVL to the Input Side

$$-V_{BE} + h_{ie}I_B + h_{re}V_{CE} = 0$$

$$V_{BE} = h_{ie}I_B + h_{re}V_{CE} \rightarrow (1)$$

Writing KCL to the Output Circuit

$$I_C = h_{fe}I_B + \frac{V_{CE}}{\left(\frac{1}{h_{oe}}\right)}$$

$$I_C = h_{fe}I_B + h_{oe}V_{CE} \rightarrow (2)$$

In Simplified model of transistor, neglect  $h_{oe}V_{CE}$  and  $h_{re}V_{CE}$ .

Reason for neglecting  $h_{oe}V_{CE}$ :

$$h_{oe} = 25 \mu V$$

In general : In amplifiers  $Z_L \leq 5k\Omega$

$$\frac{1}{h_{oe}} = \frac{1}{25 \times 10^{-6}} = 40 \text{ k}\Omega$$

$$\frac{1}{h_{oe}} \parallel Z_L \approx Z_L$$

$\frac{1}{h_{oe}}$  is very high, the current passing through it is very low.

$\therefore h_{oe} v_{ce} \rightarrow$  neglected (0.v)

$$\therefore \boxed{I_C = h_{fe} I_B}$$

Reason for neglecting  $h_{re} v_{ce}$ :

$$h_{re} v_{ce} = h_{re} (I_L Z_L)$$

$$= h_{re} (-I_C) Z_L$$

$$= -h_{fe} I_C Z_L \quad (I_C = h_{fe} I_B)$$

$$= -h_{re} h_{fe} I_B Z_L$$

$$= -2.5 \times 10^{-4} \times 50 \times I_B \times Z_L$$

$$= -12.5 \times 10^{-3} \times I_B \times Z_L$$

$$\text{We know } v_{be} = h_{ie} I_B + h_{re} v_{ce}$$

$$= h_{ie} I_B - \underbrace{12.5 \times 10^{-3} I_B Z_L}_{\text{in order of mV}}$$

As the transistor responds only for low value signals. so neglected

$v_{be} \rightarrow (\text{mV})$

$h_{ie} \rightarrow (\text{k}\Omega)$

$I_B \rightarrow (\text{mA})$

## PROCEDURE TO DRAW THE A.C EQUIVALENT CIRCUIT OF A GIVEN AMPLIFIER:

- (i) Replace the transistor by its equivalent circuit.
- (ii) Connect circuit components at first common terminal, input and output terminals.
  - (a) Resistors are connected directly
  - (b) calculate reactance of each capacitor

$$X_C = \frac{1}{\omega C} = \frac{1}{2\pi f C}$$

If  $X_C$  is high, 'c' is replaced by open circuit (o.c.)

If  $X_C$  is low, 'c' is replaced by short circuit (sc)

when frequency of signal (or) capacitances ( $\alpha$ ) both are not given : All capacitors replaced by short circuit

- (iii) All the d.c sources set equal to zero in the

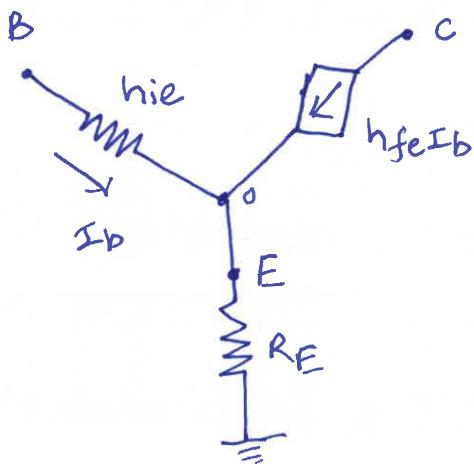
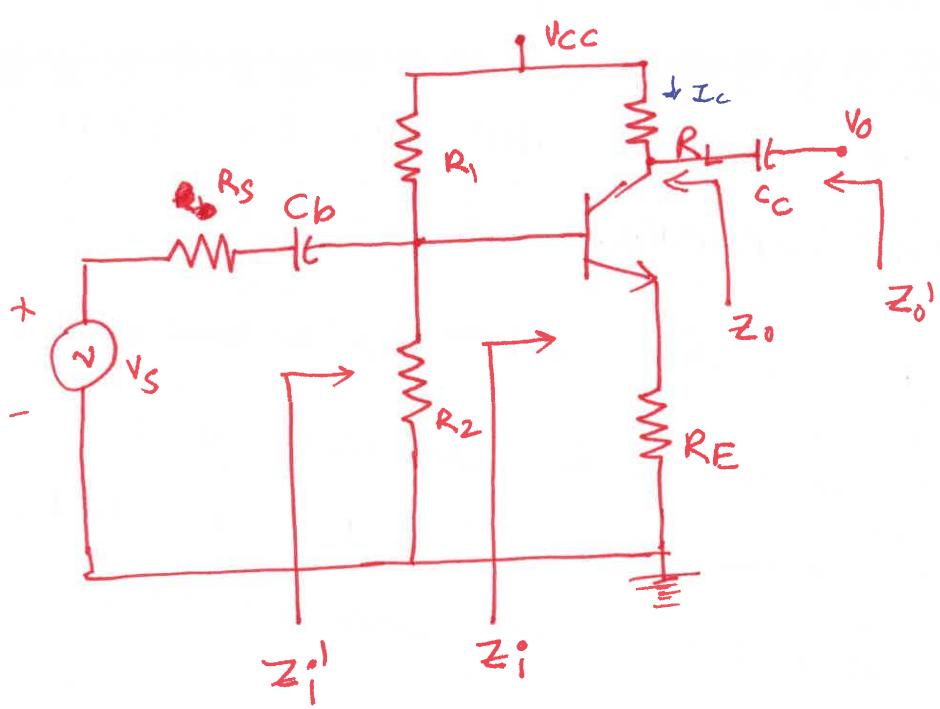
A.C equivalent circuit.

$C_b$  : Blocking Capacitor

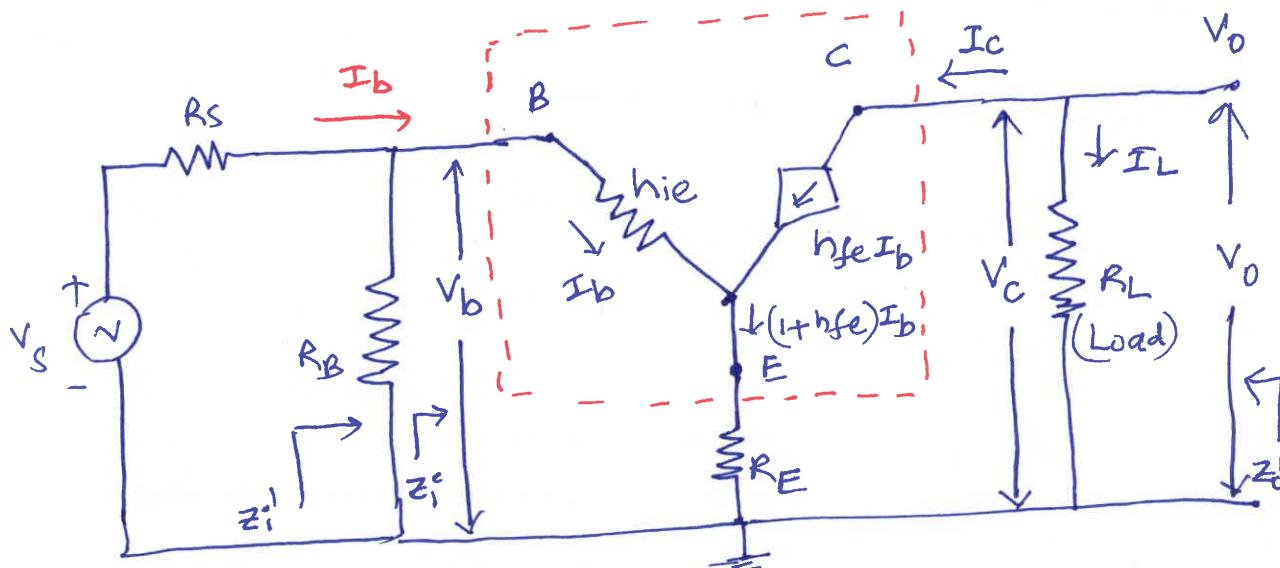
$C_c$  : Coupling Capacitor.

For a.c analysis, short ckt the voltage source (d.c)  
and open the current source (d.c)

Q.



Equivalent circuit:



$$R_B = R_1 \parallel R_2$$

$$I_L = -I_C$$

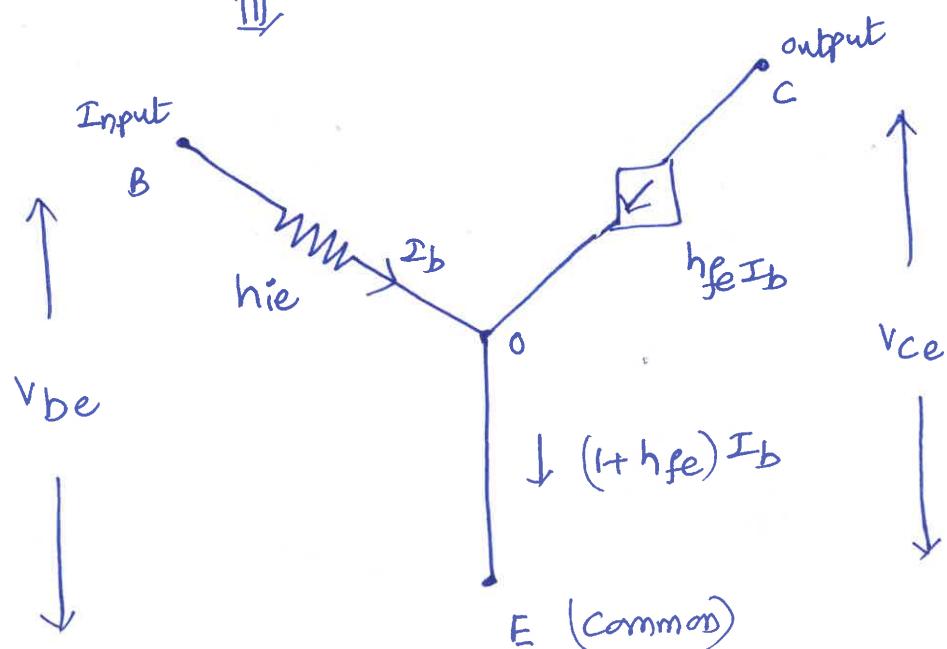
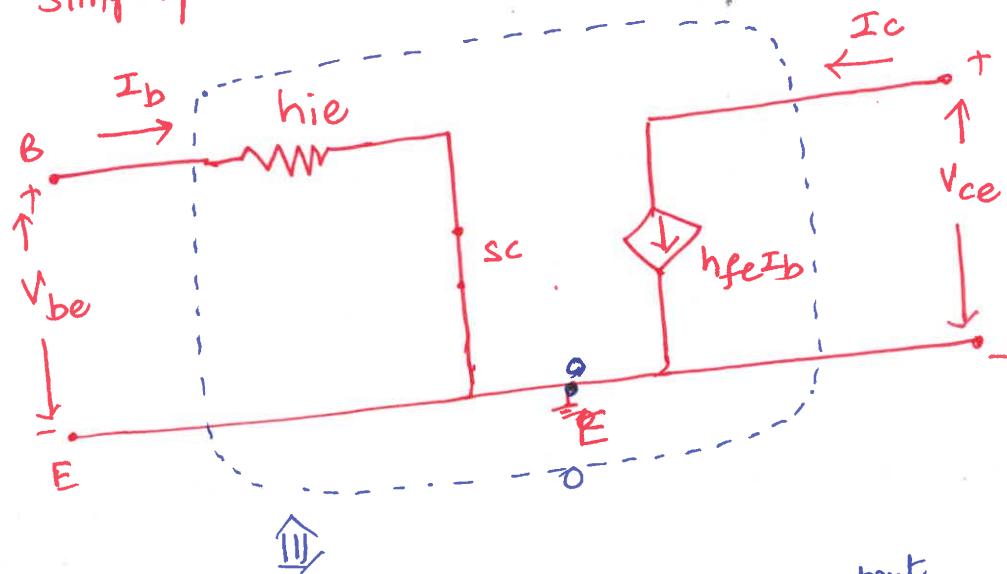
$$= -h_{fe}I_B$$

$$Z_L \rightarrow (\infty)$$

$\therefore h_{oe} v_{ce} \rightarrow$  Very low and neglected (So C)

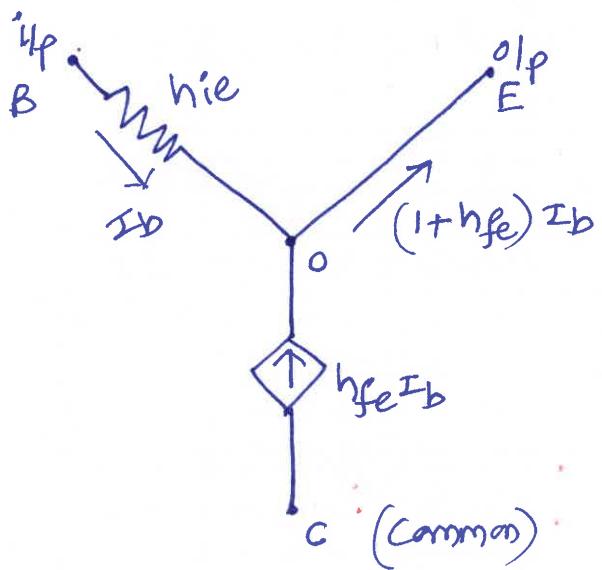
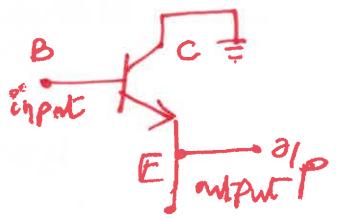
$$\therefore V_{be} = h_{ie} I_b$$

The Simplified model of transistor:

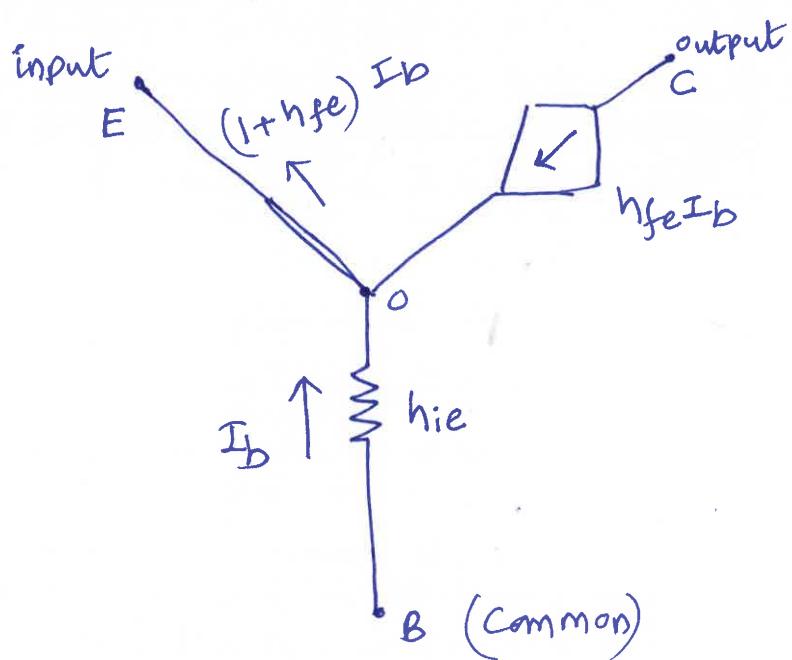
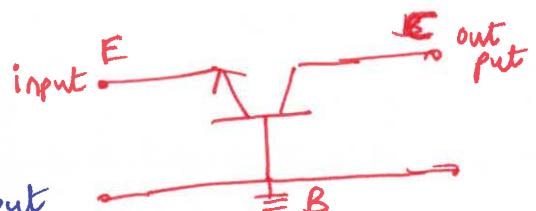


simplified CE hybrid model

Simplified CC Hybrid model:



Simplified CB Hybrid model



(a) Current gain

$$A_I = \frac{I_L}{I_b} = -\frac{I_C}{I_b} = -\frac{h_{fe} I_b}{I_b} = -h_{fe}$$

$$A_I = -h_{fe}$$

-ve sign represents  $180^\circ$  of phase shift between  $i_p$  &  $i_o$

(b) Input Impedance

$$Z_i = \frac{V_b}{I_b}$$

Writing KVL to the input side

$$-V_b + I_b h_{ie} + (1+h_{fe}) I_b R_E = 0$$

$$V_b = [h_{ie} + (1+h_{fe}) R_E] I_b$$

$$Z_i = \frac{V_b}{I_b} = h_{ie} + (1+h_{fe}) R_E$$

$Z_i$  is very high

$$Z_i' = Z_i \parallel R_B \quad (R_B = R_1 \parallel R_2)$$

(c) Voltage gain

$$A_V = \frac{V_o}{V_b}$$

( $R_C \gg R_L$ )

$$V_o = I_L R_C = -I_C R_C$$

$$= -h_{fe} I_b R_C$$

$$A_V = \frac{-h_{fe} I_b R_C}{(h_{ie} + (1+h_{fe}) R_E) I_b}$$

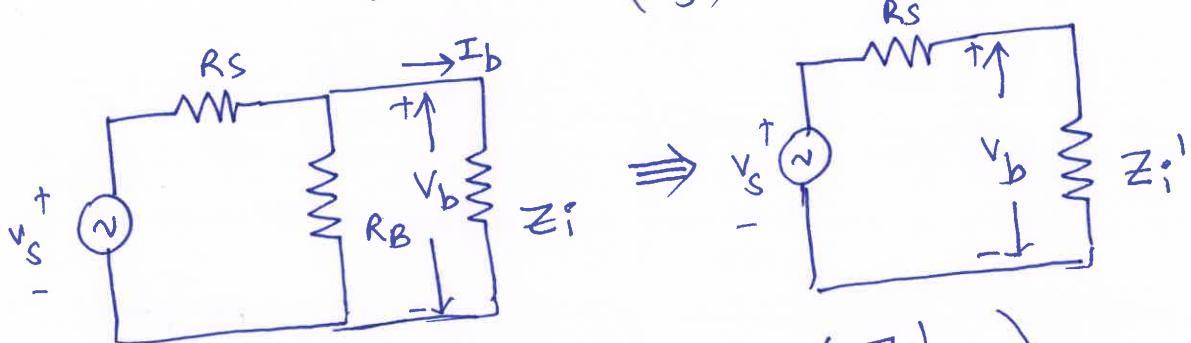
$$\text{Voltage gain } (A_V) = \frac{-h_{FE} R_L}{h_{IE} + (1+h_{FE}) R_E}$$

\*  $A_V$  is very low.

### (d) Voltage amplification

$$A_{VS} = \frac{V_O}{V_S} = \frac{V_O}{V_B} \times \frac{V_B}{V_S}$$

$$A_{VS} = A_V \times \left( \frac{V_B}{V_S} \right)$$



$$V_B = V_S \times \left( \frac{Z_i'}{Z_i' + R_S} \right)$$

$$Z_i' = Z_i \parallel R_B$$

$A_{VS}$  also very low.

### (e) output impedance ( $Z_o$ )

$$Z_o = \left. \frac{V_C}{I_C} \right|_{V_S=0}$$

As  $V_C$  is not possible to calculate,

Calculate the  $I_C$ .

$$I_C = h_{FE} I_B$$

To calculate  $I_C$  first calculate  $I_B$

Value. To calculate  $I_B$ ,  
apply KVL to the input loop

$$R_S' I_B + h_{ie} I_B$$

$$+ (1+h_{fe}) I_B R_E = 0$$

$$I_B [ (R_S' + h_{ie}) + (1+h_{fe}) R_E ] = 0$$

To satisfy the above condition,  $I_B$  must be zero.

$$I_B = 0$$

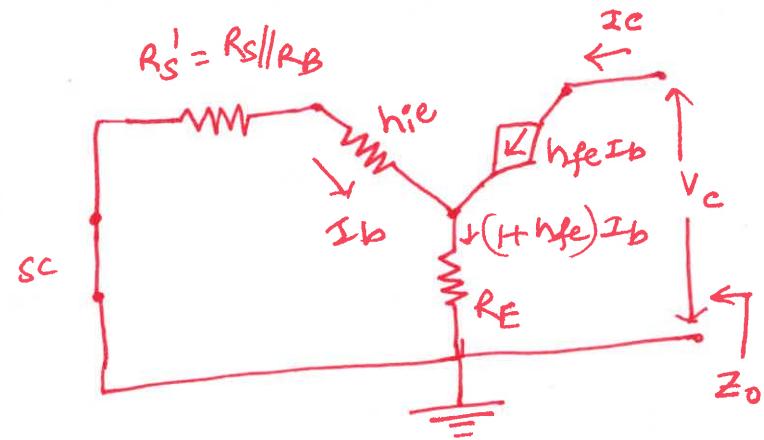
$$\therefore I_C = h_{fe} I_B = 0$$

$$Z_0 = \frac{V_C}{I_C} = \infty \rightarrow O_{IP} \text{ impedance of device.}$$

$$Z'_0 = Z_0 \parallel R_L$$

$$Z'_0 = R_L \rightarrow O_{AP} \text{ impedance of amplifier.}$$

\* To increase the gain and amplification of the  
above circuit, connect a capacitor across the emitter  
resistor and it is called bypass capacitor.



Q For amplifier shown in figure

$$I_C = 1.3 \text{ mA}, R_C = 2 \text{ k}\Omega, R_E = 500 \Omega$$

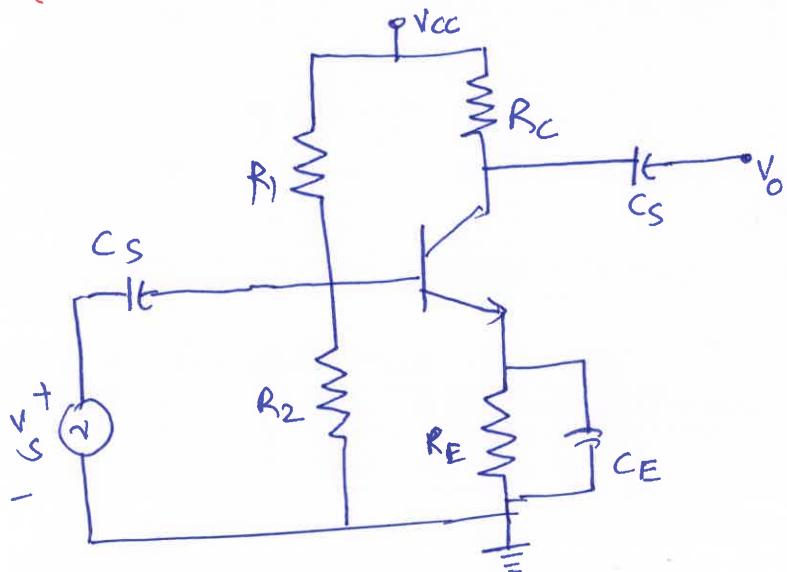
$$V_T = \frac{kT}{q} = 26 \text{ mV}, \beta = 100, V_{CC} = 15 \text{ V}$$

$$v_s = 0.01 \sin \omega t, C_B = C_E = 10 \mu\text{F}$$

(i) what is the small signal voltage gain  $A_v = \frac{V_o}{V_s}$ .

(ii) what is the approximate  $A_v$  (voltage gain) if  $C_E$  is removed.

(iii) what will be  $V_o$  if  $C_B$  is short circuited.



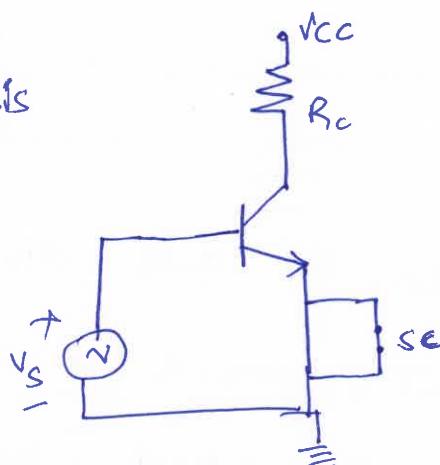
Sol: For A.C analysis

∴ Voltage gain

$$A_v = \frac{-h_{FE} R_C}{h_{ie}}$$

$$\text{Given } \beta = h_{FE} = 100$$

$$\text{Transconductance } g_m = \frac{|I_e|}{V_T} \approx \frac{|I_E|}{V_T} \quad (\text{A/V})$$



$I_C$ : d.c value

$$\text{We Know } h_{fe} = g_m h_{ie} \Rightarrow h_{fe} = g_m h_{ie} \\ = A_{vV} \times V_A$$

$$A_V = -\frac{h_{fe} R_C}{h_{ie}} \quad \bullet h_{fe} = \text{gain} \\ \beta(\infty) h_{fe}$$

$$h_{ie} = \frac{h_{fe}}{g_m} = \frac{100}{\left( \frac{1.3m}{26m} \right)} = 2000$$

$$\therefore \text{Voltage gain } (A_V) = -\frac{100 \times 2k}{2k} = -100$$

(ii) If  $C_E$  is removed

$$A_V = \frac{-h_{fe} R_C}{h_{ie} + (1+h_{fe}) R_E} \approx \frac{-R_C}{R_E} \\ \approx -\frac{2k}{500} = -4$$

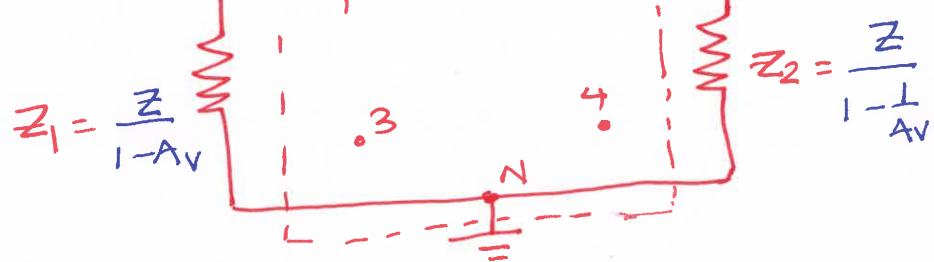
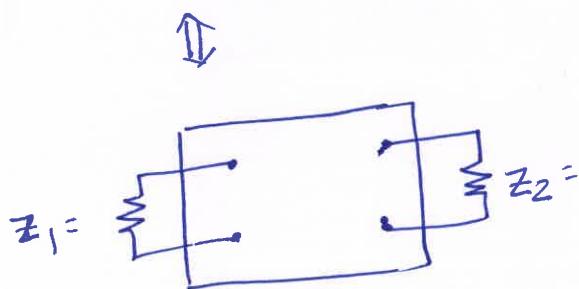
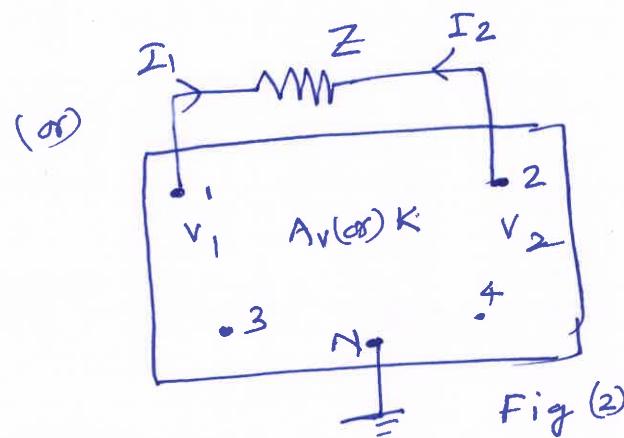
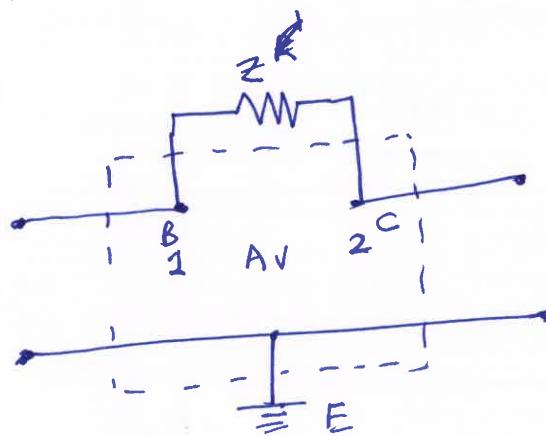
(iii) If  $C_B$  is short circuited,  $C_E$  is also short circuited because same values.

$$\therefore A_V = \frac{V_O}{V_S} \Rightarrow V_O = A_V \times V_S \\ = -100 \times 0.01 \\ = -1 \text{ volt}$$

## Miller's theorem:

Miller's theorem is used whenever there is a feedback element between input and output.

\* Using this theorem the feedback element is replaced a part in the input section and a part in the output section.



## Proof:

From Figure (2) : According to KCL

$$I = \frac{v_1 - v_2}{Z}$$

$$I_1 = \frac{v_1 \left[ 1 - \frac{v_2}{v_1} \right]}{Z}$$

$$Z_1 = \frac{v_1}{I_1} = \frac{Z}{1 - A_v} \text{ (or)} \frac{Z}{1 - K}$$

Gain  
 $A_v(\text{or}) K = \frac{v_2}{v_1}$

Now

~~KCL at port 2~~

$$I_2 = \frac{V_2 - V_1}{Z}$$

$$I_2 = \frac{V_2 \left[ 1 - \frac{V_1}{V_2} \right]}{Z}$$

$$K = \frac{V_2}{V_1} = A_V$$

$$\frac{1}{K} = \frac{V_1}{V_2}$$

$$Z_2 = \frac{V_2}{I_2} = \left[ \frac{Z}{1 - \frac{1}{A_V}} \right]$$

$\{K \text{ or } A_V\}$   
Both same.

Note :

If  $Z = R$

$$(i) \quad Z_1 = \frac{R}{1 - A_V} ; \quad Z_2 = \frac{R}{1 - \left( \frac{1}{A_V} \right)}$$

(ii) If  $Z$  is capacitor

$$Z = \frac{1}{s_C} = \frac{1}{j\omega C}$$

$$Z_1 = \frac{1}{j\omega C_1} \quad \text{and} \quad Z_2 = \frac{1}{j\omega C_2}$$

$$\therefore Z_1 = \frac{Z}{1 - A_V} \Rightarrow \frac{1}{j\omega C_1} = \frac{\frac{1}{j\omega C}}{1 - A_V} = \frac{1}{j\omega C(1 - A_V)}$$

$$\boxed{C_1 = C(1 - A_V)}$$

$$Z_2 = \frac{Z}{1 - \left( \frac{1}{A_V} \right)}$$

$$\frac{1}{j\omega C_2} = \frac{\frac{1}{j\omega C}}{1 - \left( \frac{1}{A_V} \right)} = \frac{1}{j\omega C \left[ 1 - \frac{1}{A_V} \right]}$$

$$\boxed{C_2 = C \left[ 1 - \frac{1}{A_V} \right]}$$

(iii) If  $z$  is inductor

$$z = j\omega L, \quad z_1 = j\omega L_1 \quad \text{and} \quad z_2 = j\omega L_2$$

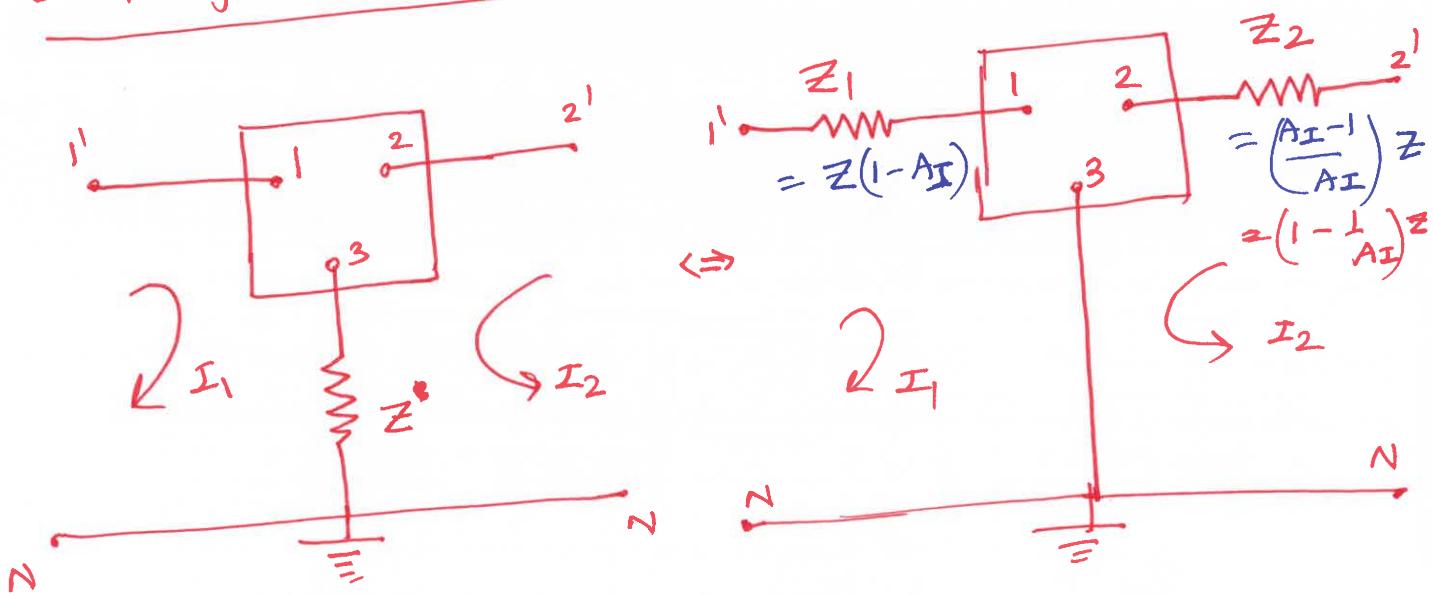
$$z_1 = \frac{z}{1 - A_V} \Rightarrow j\omega L_1 = \frac{j\omega L}{(1 - A_V)}$$

$L_1 = \frac{L}{1 - A_V}$

$$z_2 = \frac{z}{1 - \frac{1}{A_V}} \Rightarrow j\omega L_2 = \frac{j\omega L}{1 - \frac{1}{A_V}}$$

$L_2 = \frac{L}{1 - \frac{1}{A_V}}$

Dual of Miller's theorem:



Proof: By definition current gain ( $A_I$ ) =  $\frac{-I_2}{I_1}$

$$I_1 z_1 = (I_1 + I_2) z$$

$$z_1 = \left(\frac{I_1 + I_2}{I_1}\right) z = \left(1 + \frac{I_2}{I_1}\right) z$$

$$z_1 = (1 - A_I) z$$

$$A_I = -\frac{I_2}{I}$$

Now:  $I_2 z_2 = (I_1 + I_2) z$

$$z_2 = \left( \frac{I_1 + I_2}{I_2} \right) z$$

$$= \left( 1 + \frac{I_1}{I_2} \right) z$$

$$= \left( 1 - \frac{1}{A_I} \right) z$$

$$z_2 = \frac{(A_I - 1)}{A_I} z$$

$$A_I = -\frac{I_2}{I}$$

$$\frac{1}{A_I} = \frac{-I_2}{I_2}$$

$$\therefore z_1 = (1 - A_I) z \quad \text{and} \quad z_2 = \left( 1 - \frac{1}{A_I} \right) z$$

Note:

Case(i) If  $z = R$

$$z_1 = (1 - A_I) R \quad \text{and} \quad z_2 = \left( 1 - \frac{1}{A_I} \right) R$$

(ii) If  $z$  is capacitor

$$z = \frac{1}{j\omega C} \quad z_1 = \frac{1}{j\omega C_1} ; z_2 = \frac{1}{j\omega C_2}$$

$$\frac{1}{j\omega C_1} = (1 - A_I) \frac{1}{j\omega C}$$

$$C = (1 - A_I) C_1 \Rightarrow$$

$$C_1 = \frac{C}{1 - A_I}$$

$$Z_2 = \left(1 - \frac{1}{AI}\right) Z$$

$$Z_2 = \frac{1}{j\omega C_2} \quad Z = \frac{1}{j\omega C}$$

$$\frac{1}{j\omega C_2} = \left(1 - \frac{1}{AI}\right) \frac{1}{j\omega C} = \frac{(AI-1)}{AI} \frac{1}{j\omega C}$$

$$C = C_2 \frac{(AI-1)}{AI}$$

$$\therefore C_2 = C \left[ \frac{\frac{1}{AI}}{\frac{1}{AI}-1} \right] = \left[ \frac{C}{1 - \frac{1}{AI}} \right]$$

Case(iii)  
If  $Z$  is inductor.

$$Z = j\omega L \quad Z_1 = j\omega L_1 \quad Z_2 = j\omega L_2$$

$$Z_1 = (1 - AI) Z$$

$$j\omega L_1 = (1 - AI) j\omega L$$

$$L_1 = (1 - AI) L$$

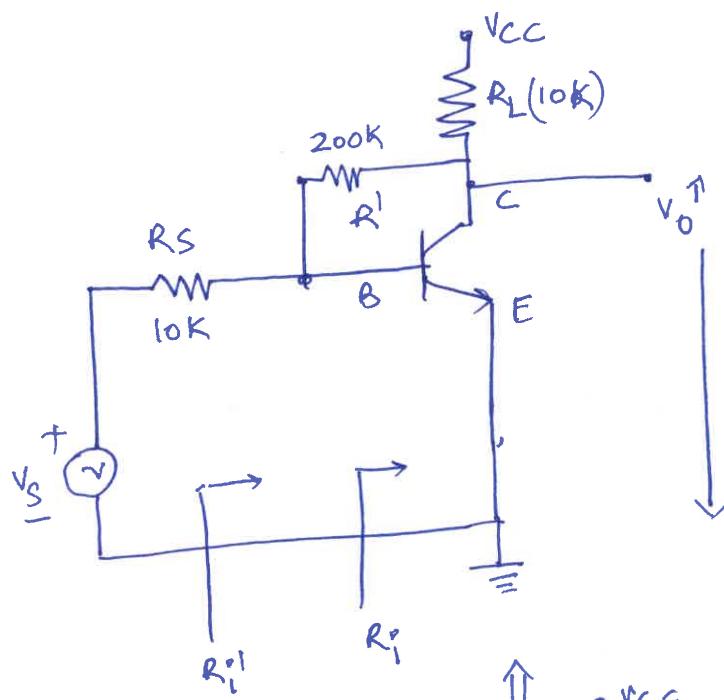
$$Z_2 = \left(1 - \frac{1}{AI}\right) Z$$

$$j\omega L_2 = \left(1 - \frac{1}{AI}\right) j\omega L$$

$$L_2 = \left(1 - \frac{1}{AI}\right) L$$

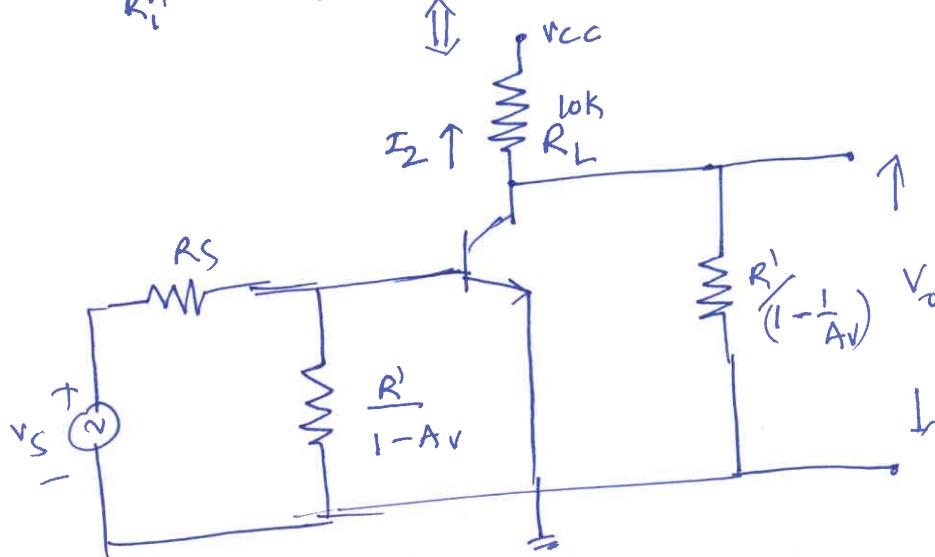
Q For Amplifier circuit shown in figure calculate  $R_i$ ,  $R_o$

$$A_V, A_{VS} \text{ and } A_I = -\frac{I_2}{I_1}$$

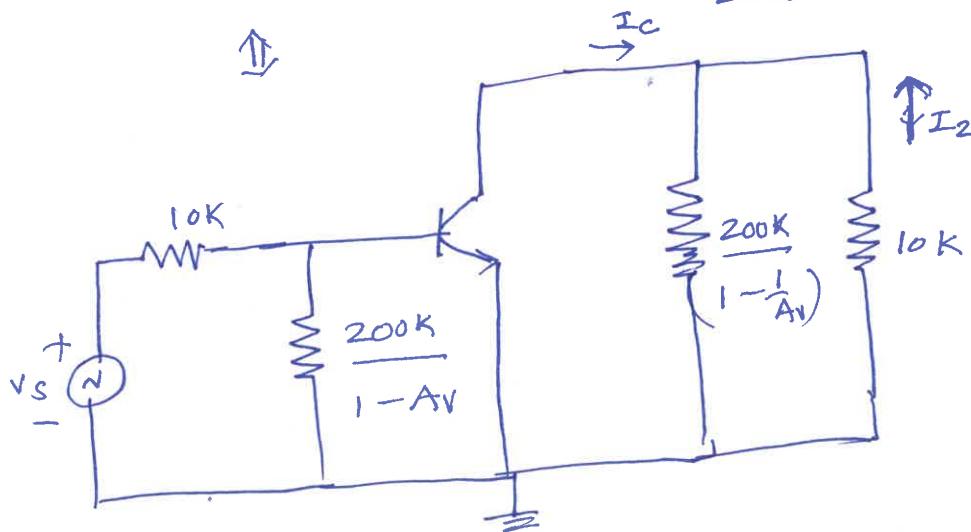


We know the miller's theorem

$$R_1 = \frac{R_1}{1-A_V} \quad R_2 = \frac{R_L}{(1-\frac{1}{A_V})}$$



For A.C analysis, all the d.c sources set equal to zero means (grounded)



$$I_2 = -\frac{v_o}{10k}$$

Since the Amplifier is Connected in CE Configuration

$A_V$  (Voltage gain) is very high  $\frac{1}{A_V} \rightarrow 0$

$$A_I = \frac{-h_{fe}}{1 + h_{oe} R_L'}$$

$$R_L' = R_L \parallel \left( \frac{R'}{1 - \frac{1}{A_V}} \right)$$

$$\therefore R_L' = 10K \parallel 200K \quad \frac{1}{A_V} \rightarrow 0$$

$$\therefore A_I = \frac{-50}{1 + \frac{1}{40K} (10K \parallel 200K)} = -40.3$$

$$\begin{aligned} R_i^* &= h_{ie} + h_{re} A_I R_L' \\ &= 1100 + 2.5 \times 10^{-4} \times (-40.3) \times (10K \parallel 200K) \\ &= 1.007K\Omega \end{aligned}$$

$$\begin{aligned} \therefore \text{Voltage gain } (A_V) &= A_I \times \frac{R_L'}{R_i^*} \\ &= \frac{-40.3 \times (10K \parallel 200K)}{1K} \\ &= -384.4 \end{aligned}$$

$$\text{Voltage amplification } (A_{VS}) = A_V \times \frac{R_L'}{R_i^* + R_S}$$

$$R_i^* = R_i \parallel \frac{R'}{1 - A_V}$$

$$R_i^o = 1K \parallel \frac{200K}{1 - (-384)}$$

$$A_{VS} = -384 \times \frac{343}{343 + 10K} = -12.7$$

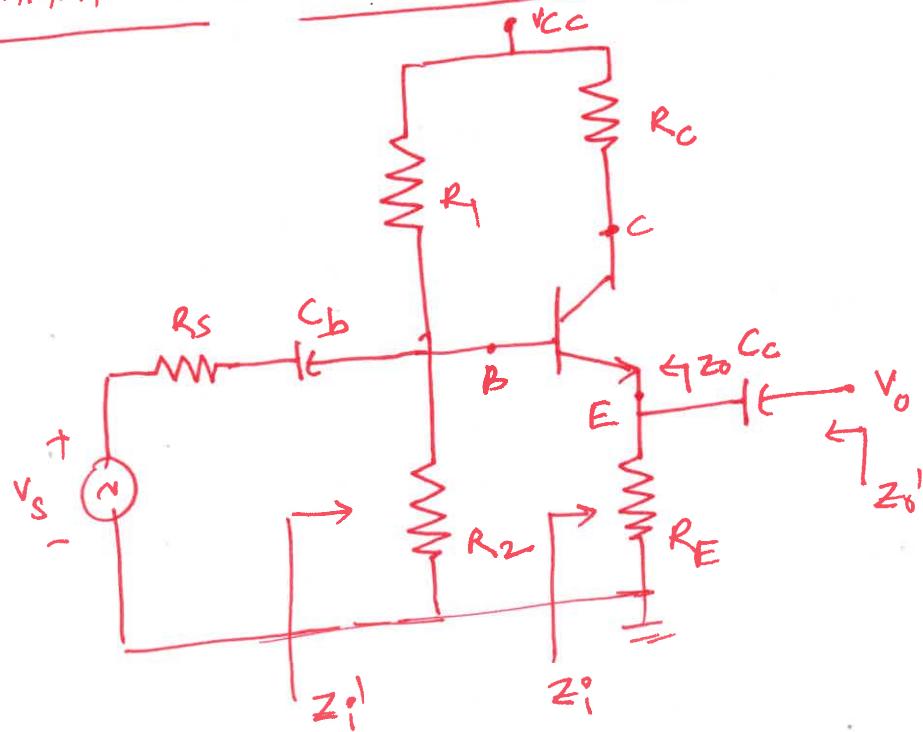
$$A_I^I = -\frac{I_2}{I_1}$$

$$I_1 = \frac{V_S}{R_S + R_i^o}$$

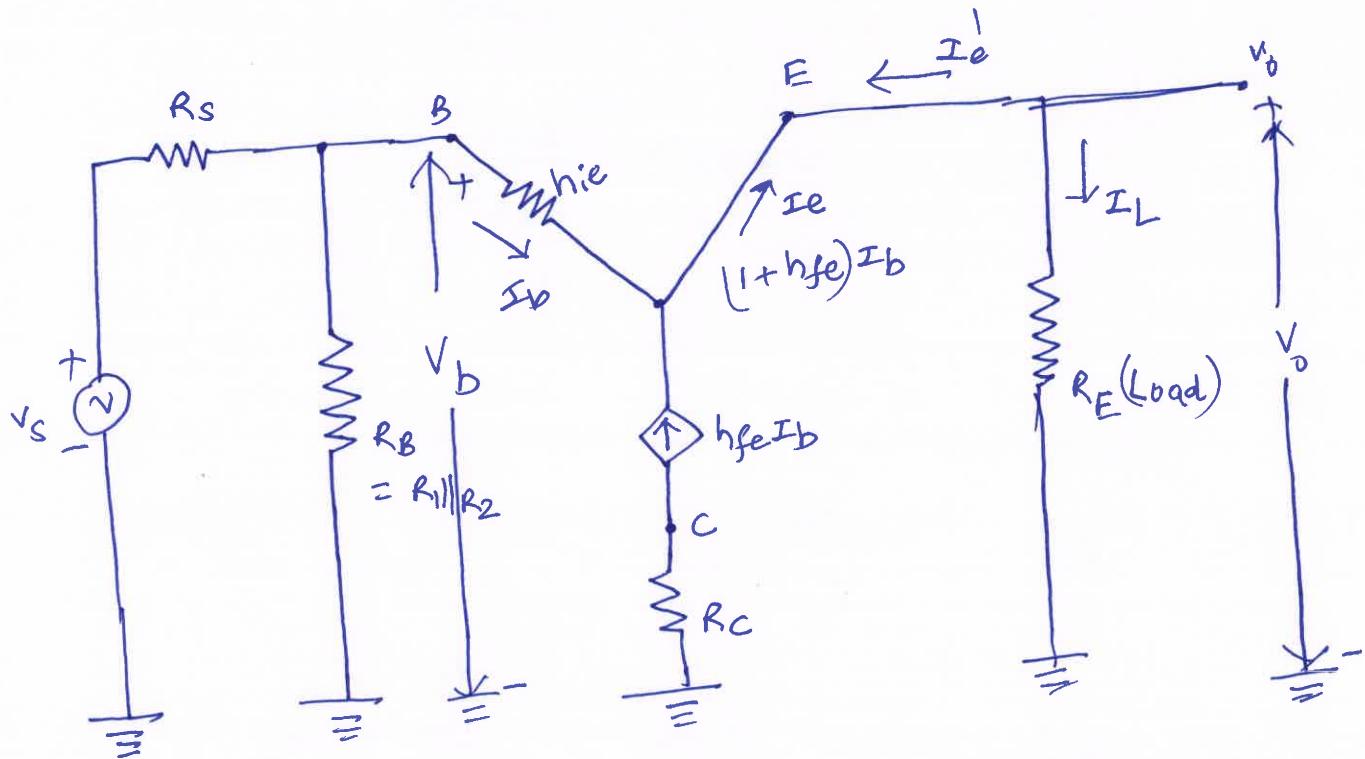
$$A_I^I = -\frac{I_2}{I_1} = \frac{-\frac{V_o}{R_L}}{\frac{V_S}{R_S + R_i^o}} = -\frac{V_o}{V_S} \times \frac{R_S + R_i^o}{R_L}$$

$$A_I^I = -A_{VS} \left[ \frac{R_S + R_i^o}{R_L} \right] = 13.15$$

### Common Collector Configuration analysis:



## Small signal model:



$$\begin{aligned}
 \text{(i) current gain } (A_I) &= \frac{I_L}{I_b} = -\frac{I_e'}{I_b} \\
 &= \frac{(1+h_{fe}) I_b}{I_b} \\
 &= 1+h_{fe}
 \end{aligned}$$

+ve sign represents  $0^\circ$  phase shift between  
Input and output.

**(ii) Input Impedance ( $Z_i$ )**

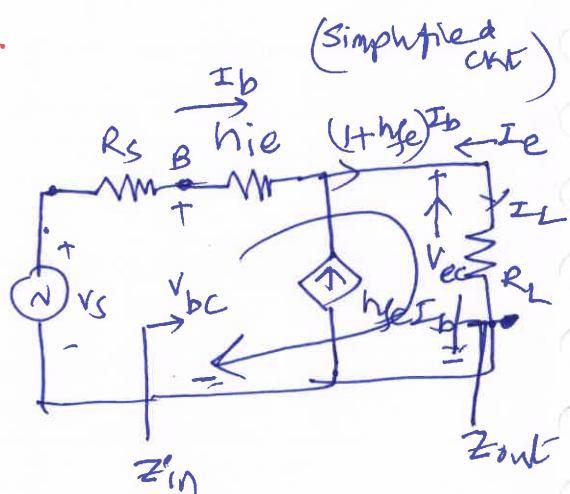
$$Z_i = \frac{V_b}{I_b}$$

$$V_b = h_{ie}I_b + I_L R_E$$

Writing KVL equation

$$-V_b + h_{ie}I_b + (1+h_{fe})I_b R_E = 0$$

$$V_b = [h_{ie} + (1+h_{fe})R_E] I_b$$



$$\therefore Z_i = \frac{V_b}{I_b} = h_{ie} + (1+h_{fe})R_E$$

$$\boxed{\therefore Z_i = h_{ie} + (1+h_{fe})R_E}$$

$Z_i$  is very high for CC.

$$Z_{i'} = Z_i \parallel R_B$$

Voltage gain

$$A_V = \frac{V_o}{V_b}$$

$$A_V = \frac{I_L R_E}{h_{ie} I_b + V_o} = \frac{(1+h_{fe}) I_b R_E}{h_{ie} I_b + (1+h_{fe}) I_b R_E}$$

$$A_V = \frac{(1+h_{fe}) R_E}{h_{ie} + (1+h_{fe}) R_E}$$

As den > numerator, the voltage gain  $A_V \approx 1$  always

As  $(1+h_{fe}) R_E \gg h_{ie}$

$$\therefore \boxed{A_V \approx 1}$$

$\therefore$  The o/p voltage  $\approx$  i/p voltage

This circuit is called Voltage follower circuit (or)

Voltage buffer circuit (or) Emitter follower circuit.

$$\therefore A_V = \frac{(1+h_{fe}) R_E}{h_{ie} + (1+h_{fe}) R_E}$$

$$\therefore A_V = 1 - \frac{h_{ie}}{h_{ie} + (1+h_{fe})R_E}$$

$$A_V = 1 - \frac{h_{ie}}{Z_i}$$

Voltage amplification:

$$A_{VS} = A_V \times \left( \frac{Z_i'}{Z_i' + R_S} \right)$$

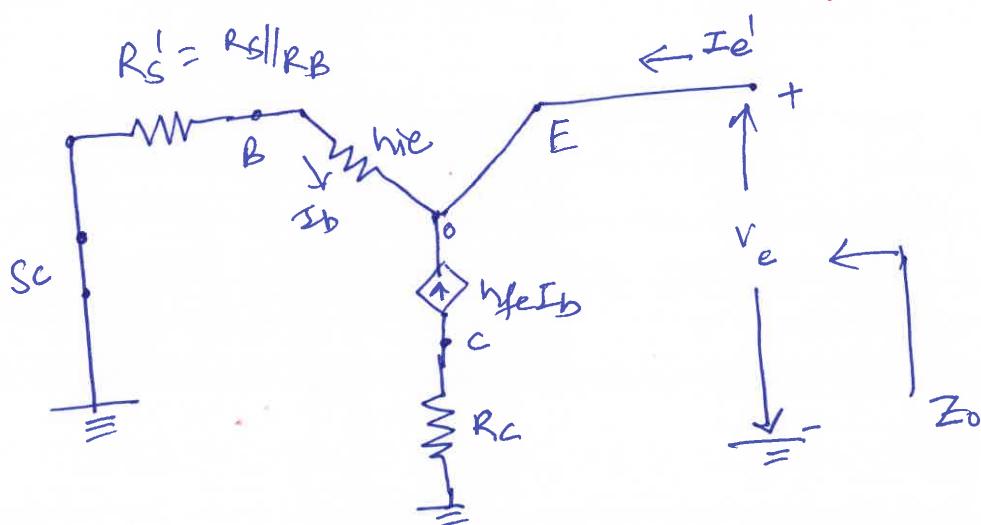
$A_{VS} < 1$  always.

$\therefore$  The common collector <sup>ckt</sup> cannot be used for voltage amplification and is used as voltage follower circuit only.

Output impedance:

$$Z_o = \left. \frac{V_e}{I_e'} \right|_{V_s=0}$$

Method 1:



$$Z_0 = \frac{V_e}{I_e}$$

$$V_e = -I_b (R_s + h_{ie})$$

$$Z_0 = \frac{-I_b (R_s + h_{ie})}{-I_b (1 + h_{fe})} = \frac{R_s + h_{ie}}{1 + h_{fe}}$$

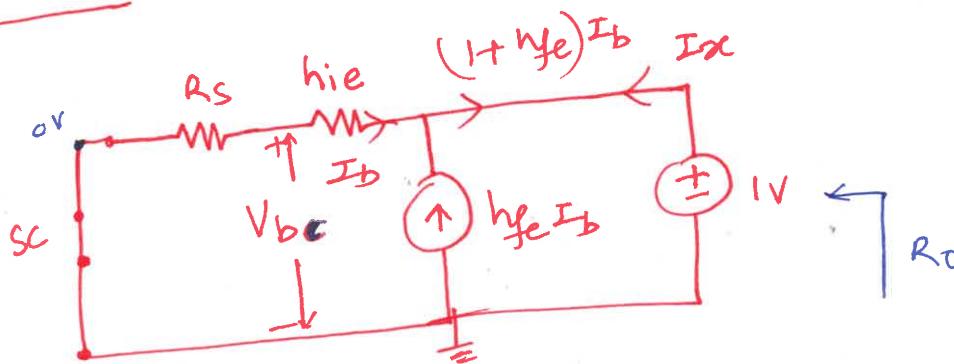
$$Z_0 = \frac{R_s + h_{ie}}{1 + h_{fe}}$$

$Z_0$  is very low

$$Z'_0 = Z_0 \parallel R_E$$

$\therefore Z'_0$  is also very low.

### Method - 2:



$$R_o = \frac{V}{I_x} = \left( \frac{V}{I} \right)$$

$$\text{KCL: } i_b + i_x = 0 \\ i_x = -i_b$$

$$i_b = \frac{0 - I}{R_s + h_{ie}}$$

$$\text{here } i_x = -(1 + h_{fe}) I_b$$

$$i_x = \frac{-(1 + h_{fe}) \times -1}{(R_s + h_{ie})}$$

$$-(1 + h_{fe}) I_b = -I_b$$

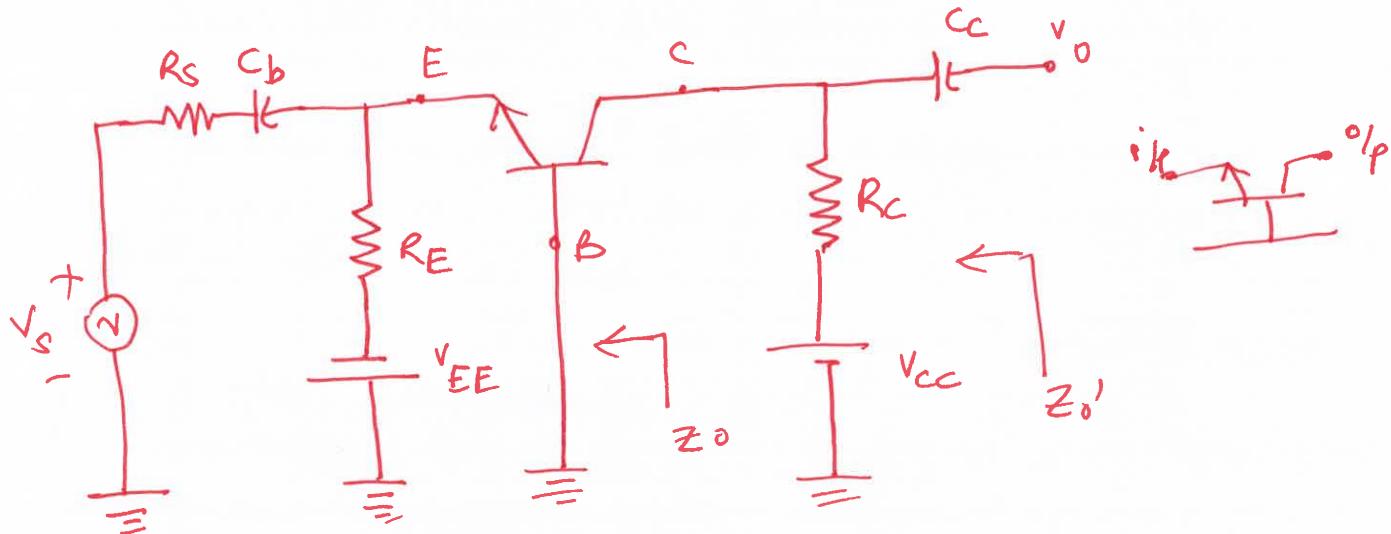
$$\therefore R_o = \frac{1}{i_x} = \left[ \frac{1}{\frac{1 + h_{fe}}{R_s + h_{ie}}} \right]$$

$$i_x = \frac{(1 + h_{fe})}{R_s + h_{ie}}$$

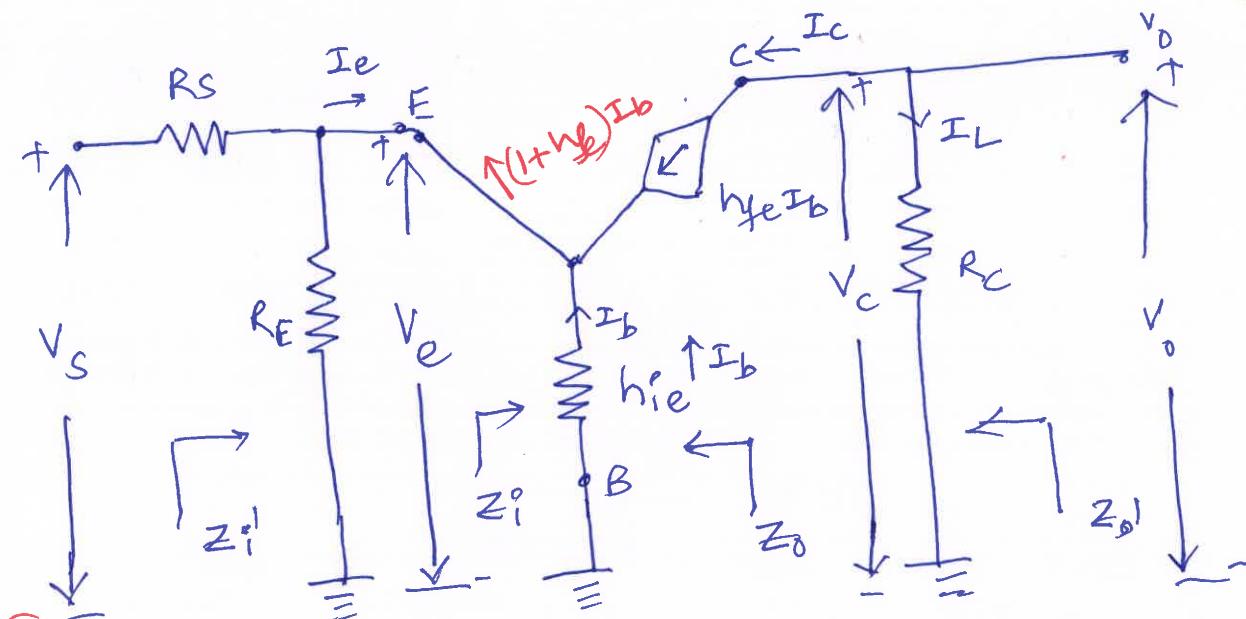
$$\therefore R_o = \frac{R_s + h_{ie}}{1 + h_{fe}}$$

output resistance

Common base Configuration analysis:



Small signal model:



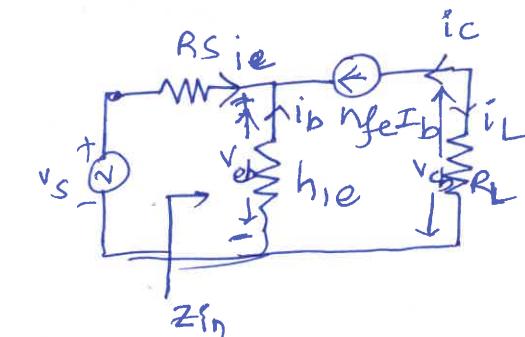
$$\begin{aligned}
 \text{current gain } (A_I) &= \frac{I_L}{I_e} = -\frac{I_C}{I_e} \\
 &= -\frac{h_{fe} I_B}{-(1+h_{fe}) I_B} \\
 &= \frac{h_{fe}}{1+h_{fe}}
 \end{aligned}$$

\* By Comparing CE, CC, CB . The Common Emitter only (CE) used for voltage amplification .

- \* The Common Collector (CC) used as Voltage Buffer.
- \* The Common Base (CB) used as Current Buffer.

$$A_I = \frac{h_{fe}}{1+h_{fe}} = \frac{\beta}{1+\beta} = \alpha = (0.9 \text{ to } 0.999)$$

Input Impedance ( $Z_i$ ) =  $\frac{V_e}{I_e} (\infty) \quad \frac{v_{eb}}{I_e}$



$$Z_i = \frac{-I_b h_{ie}}{-I_b(1+h_{fe})} = \frac{h_{ie}}{1+h_{fe}}$$

$$Z'_i = Z_i \| R_E$$

$$\text{Voltage gain (AV)} = \frac{V_o}{V_e} = \frac{I_L R_C}{-I_b h_{ie}} = \frac{-I_C R_C}{-I_b h_{ie}}$$

$$AV = \frac{-h_{fe} I_b R_C}{-I_b h_{ie}} = \frac{h_{fe} R_C}{h_{ie}}$$

[We know  $g_m = \frac{h_{fe}}{h_{ie}}$ ]

$$AV = g_m R_C$$

Method - 2:

$$\text{Voltage gain (AV)} = A_I \times \frac{Z_L}{Z'_i} = \frac{h_{fe}}{1+h_{fe}} \times \frac{R_C}{\frac{h_{ie}}{1+h_{fe}}} \left( \frac{\frac{R_C}{h_{ie}}}{1+h_{fe}} \right)$$

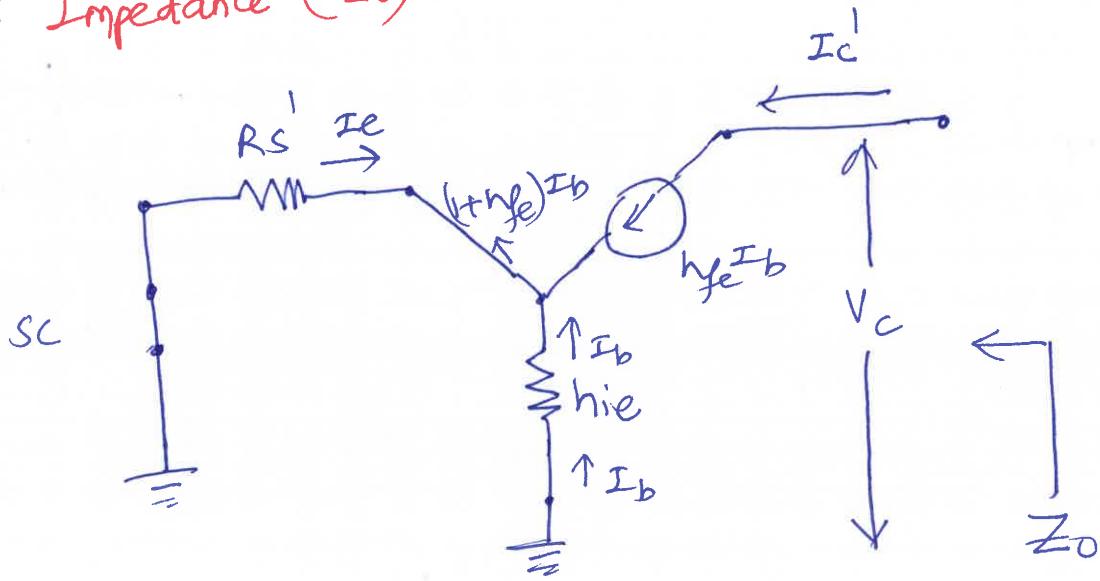
$$* \quad | A_V = \frac{h_{fe}}{h_{ie}} R_L | *$$

$$g_m = \frac{h_{fe}}{h_{ie}} "$$

## Voltage amplification

$$A_{VS} = A_V \times \left[ \frac{Z_i'}{Z_i' + R_S} \right]$$

output Impedance ( $Z_o$ ):



$$Z_o = \frac{V_C}{I_C'} \mid V_S = 0$$

writing KVL to the input Loop

$$R_S' I_e - h_{ie} I_b = 0$$

$$-R_S' (1+h_{fe}) I_b - h_{ie} I_b = 0$$

$$I_b' = 0$$

$$I_C' = 0$$

$$\text{Output Impedance}$$

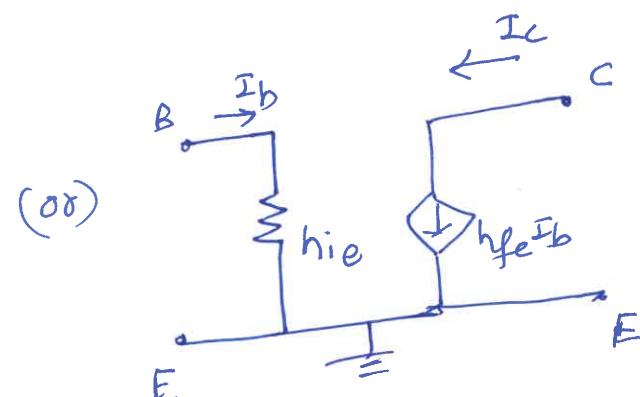
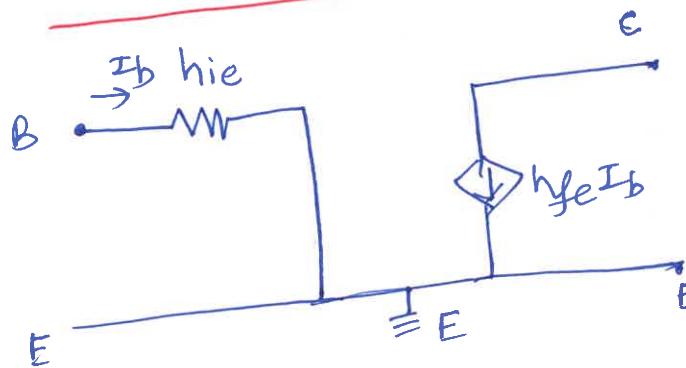
$Z_o = \infty$

$$Z'_o = Z_o / R_C = \infty / R_C = R_C$$

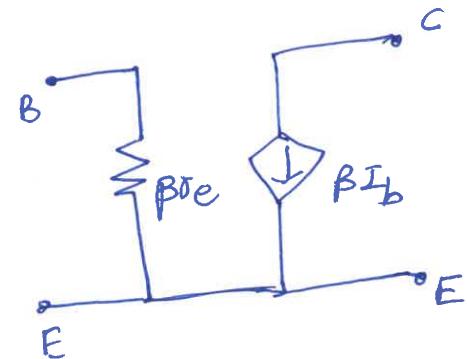
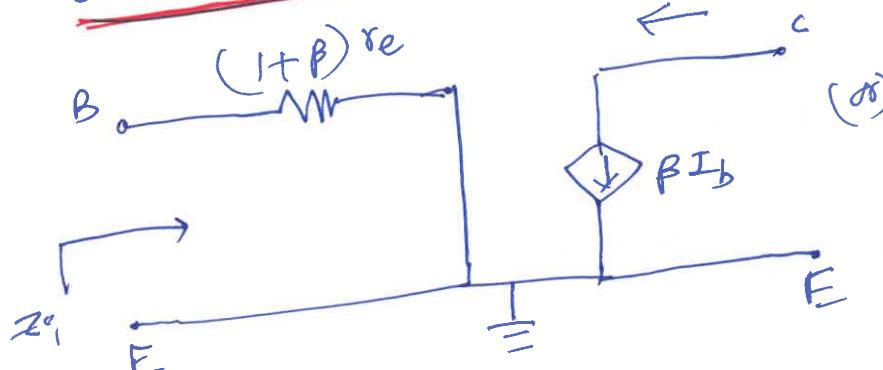
$$Z'_o = R_C$$

## Amplifier Models in BJT:

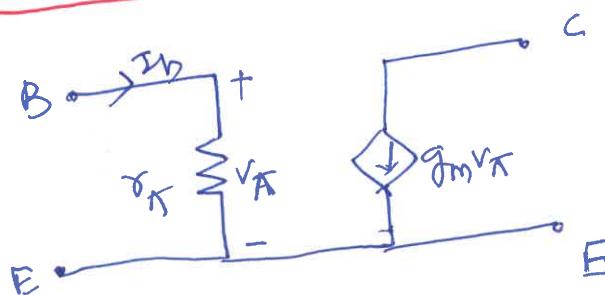
### h-parameter model:



### 'r\_e' model:



### 'r\_K' Model



At low frequency, hybrid-T model, h-parameter model,  
 $r_e$ -ce model are same.

$$I_C = h_{fe} I_B = \beta I_B = g_m V_B' e$$

$$\boxed{h_{fe} = \beta}$$

$$h_{fe} I_B = g_m V_B' e$$

$$h_{fe} I_B = g_m I_B r_{be}' e$$

$$h_{fe} = g_m r_{be}' e = \beta$$

$$h_{ie} = (1 + \beta) r_e = r_{bb}' + r_{be}' e$$

$$h_{ie} = (1 + \beta) r_e ; \quad r_e = \frac{V_T}{I_E}$$

$$h_{ie} \approx \beta r_e$$

$$h_{ie} \approx g_m r_{be}' e \times r_e \approx \frac{I_C}{V_T} r_{be}' e \times \frac{V_T}{I_E} \quad [g_m \approx \frac{1}{r_e}]$$

$$\therefore h_{ie} \approx r_{be}' e$$

$$\therefore h_{ie} \approx r_{be}' e \approx \beta r_e$$

$$h_{fe} = \beta = g_m r_{be}' e$$

$$h_{fe} \approx g_m h_{ie}$$

$$\boxed{\begin{array}{c} g_m \approx \\ \vdash \end{array} \begin{array}{c} h_{fe} \\ \hline h_{ie} \end{array}} \rightarrow \text{Transconductance.}$$

## HIGH FREQUENCY RESPONSE OF AMPLIFIER

The high frequency response of amplifier is the calculation of upper cut off frequency of amplifier.

At high frequency,

$$X_C = \frac{1}{2\pi f C} ; C = \underbrace{C_e, C_b, C_{ce}}_{MF}$$

$X_C \rightarrow$  very low

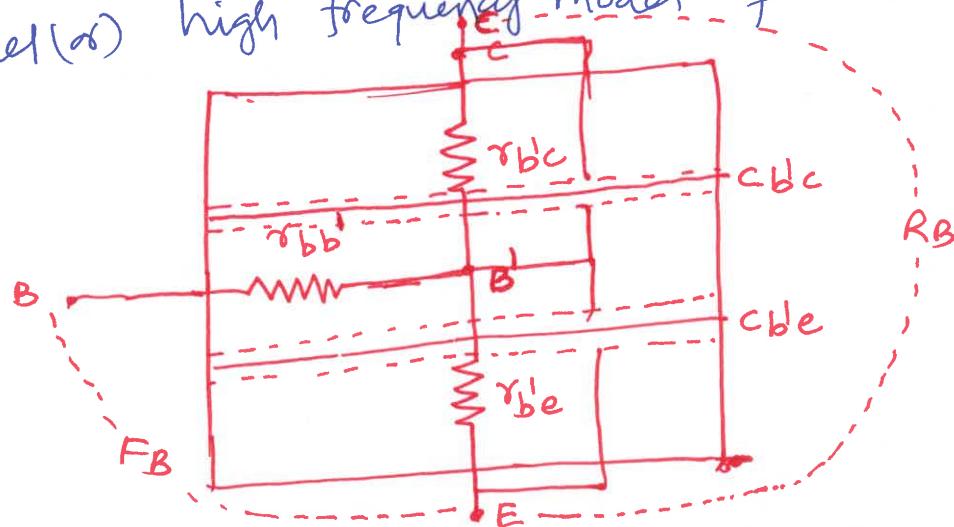
$C \rightarrow$  acts as short circuit.

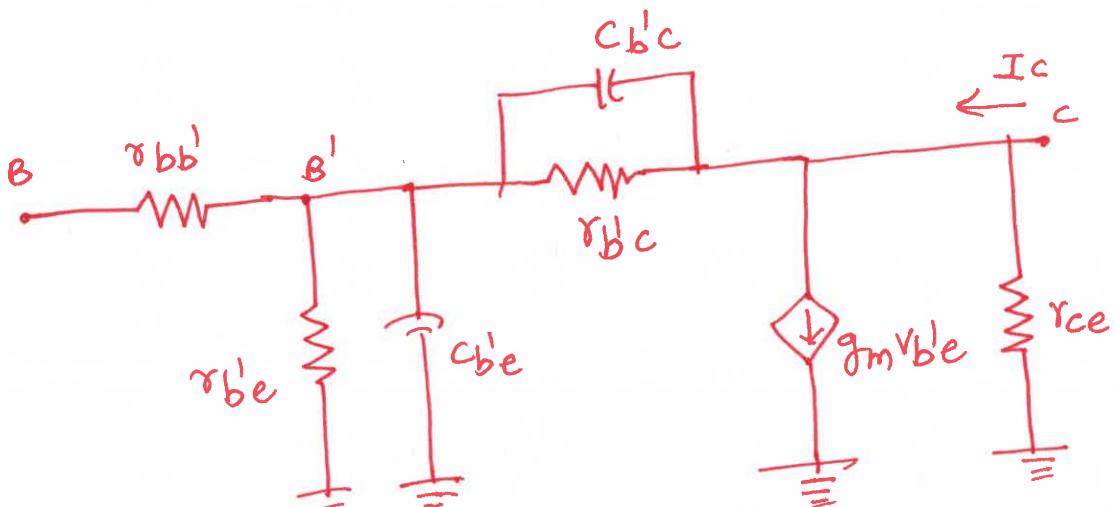
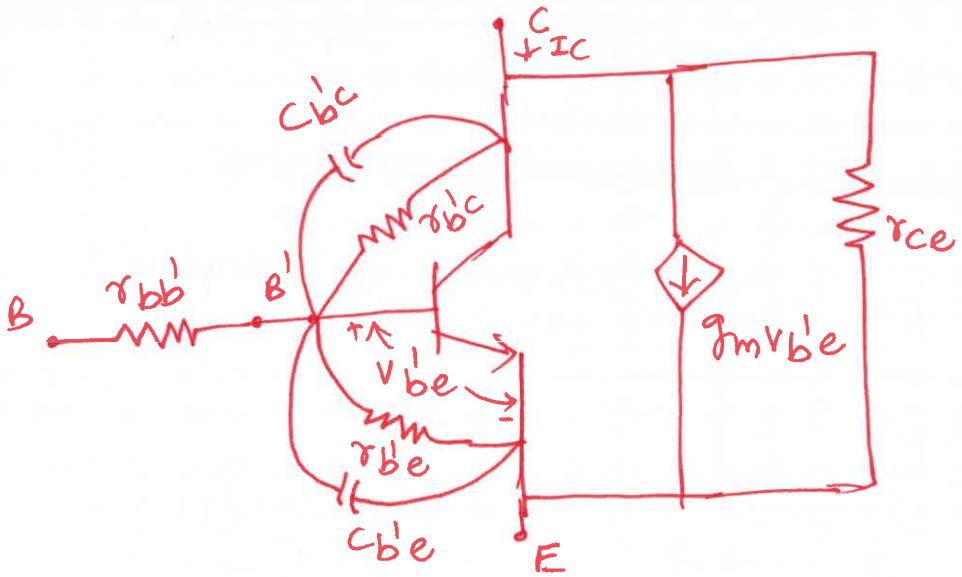
At high frequency the cut-off frequency provided by parasitic ( $\infty$ ) inter electrode capacitances. These are capacitances at terminals and junctions.

At high frequencies, the h-parameters becomes complex in nature and varies with frequency so that h-parameter model is not valid at high frequencies.

At high frequencies, hybrid - $\pi$  ( $\infty$ ) GIACOLETTO

Model ( $\infty$ ) high frequency model of transistor is used.





Hybrid -  $\pi$  Parameters:

$r_{bb'}$  → Base Spreading Resistance (Least Impedance)  
 $(r_{bb'} \leq 100\Omega \text{ always})$

$g_m$  → Transconductance  $\approx \frac{I_c}{V_T}$  D.C (I<sub>c</sub>) current

$r_{be}$  → Input resistance ( $1K\Omega$ ) ( $r_\pi$ )

$r_{b'e}$  → Feedback resistance ( $4M\Omega$ ) (o.c)  
 $(\infty)$  Highest impedance

Reverse bias resistance  
 $(\text{It is very high} = 4M\Omega)$

- $r_{ce} \rightarrow$  output resistance ( $80\text{ k}\Omega$ ) [Very high] ( $r_o$ )  
 $C_{be}' \rightarrow$  diffusion capacitance ( $100\text{ pF}$ ), ( $C_\pi$ ), ( $C_D$ )  
 $C_{bc} \rightarrow$  transition capacitance ( $3\text{ pF}$ ) ( $C_M$ ) ( $C_T$ )  
 $g_m \rightarrow$  transconductance ( $50\text{ mA/V}$ )

Notation:

$$r_{be}' \rightarrow r_\pi, r_{be}, r_e$$

$$c_{be}' \rightarrow C_\pi, C_{be}, C_e$$

$$v_{be}' \rightarrow v_\pi, v_{be}, v_e$$

$$r_{bc}' \rightarrow r_M, r_{bc}, r_c$$

$$C_{bc}' \rightarrow C_M, C_{bc}, C_c$$

At Low frequency, hybrid - $\pi$  model, h-parameter

models,  $r_e$ -ce model are same.

At low frequency

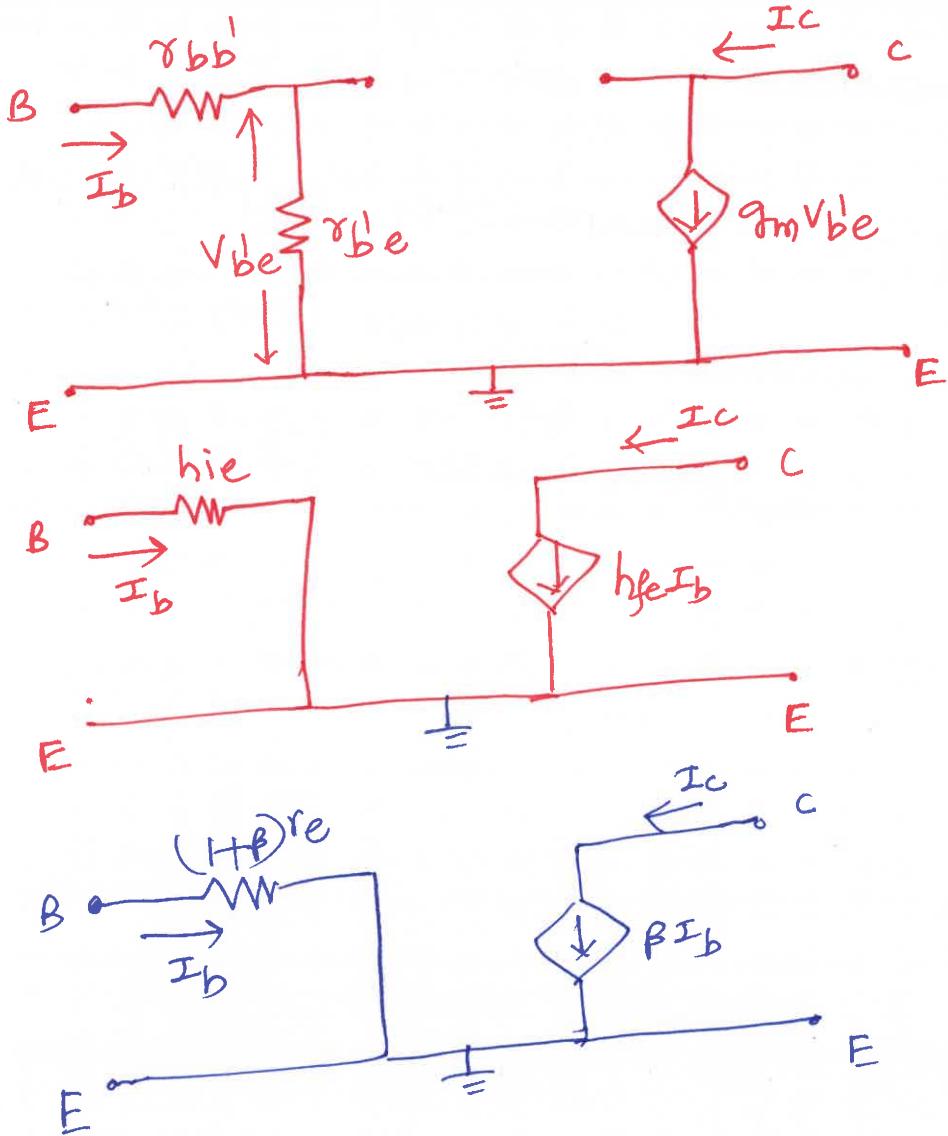
$$x_c = \omega$$

$$[x_c = \frac{1}{\omega c} = \frac{1}{2\pi f c}]$$

$$= \frac{1}{\omega} = \omega$$

$$c_{be}' \& C_{bc}' \Rightarrow 0 \cdot C$$

$r_{bc}'$  and  $r_{ce}$   $\rightarrow$  neglected  
[Very high]



$$I_C = h_{fe} I_B = \beta I_B = g_m V_{BE}$$

$$\boxed{h_{fe} = \beta}$$

$$h_{fe} I_B = g_m V_{BE} = g_m [I_B r_{be}']$$

$$h_{fe} = g_m r_{be}' = \beta$$

$$h_{ie} = (1 + \beta) r_e = r_{bb}' + r_{be}'$$

$$h_{ie} = (1 + \beta) r_e ; r_e = \frac{V_T}{I_E}$$

$$h_{ie} \approx \beta r_e$$

$$h_{ie} \approx g_m r_{be}' \times r_e \approx \frac{I_C}{V_T} r_{be}' \times \frac{V_T}{I_E} \quad \left[ g_m = \frac{1}{r_e} \right]$$

$$h_{ie} \approx r_{b'e}$$

( $r_{bb'}$  is neglected)

$$\therefore h_{ie} \approx r_{b'e} \approx r_{re}$$

$$h_{fe} = \beta = g_m r_{b'e}$$

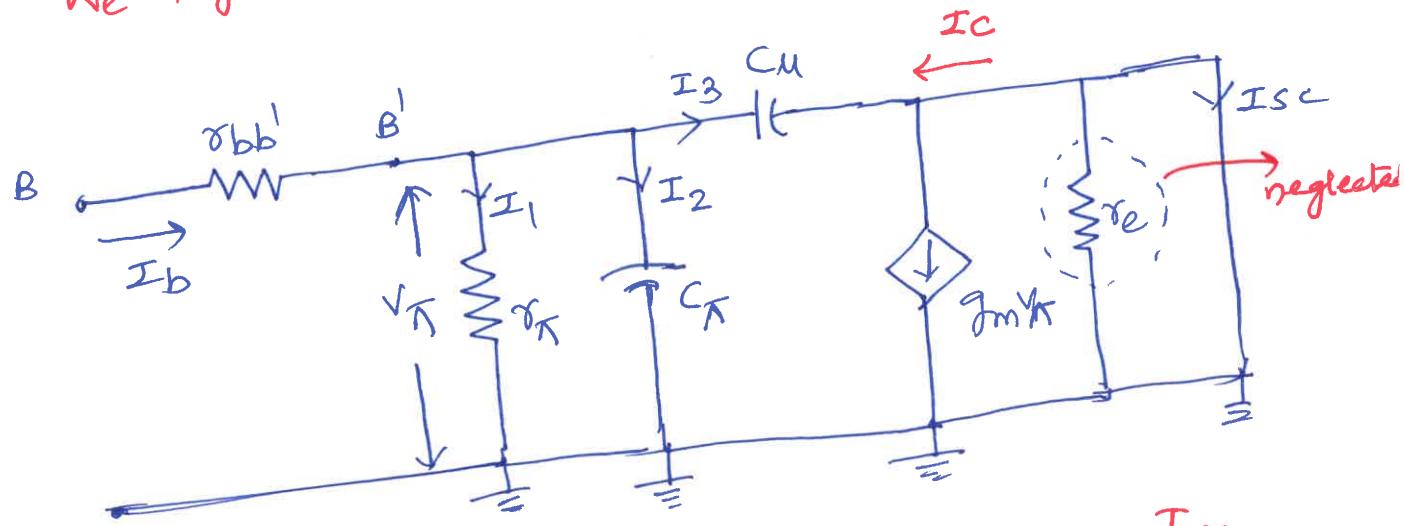
$$h_{fe} \approx g_m h_{ie}$$

$$g_m \approx \frac{h_{fe}}{h_{ie}}$$

→ Transconductance.

Short circuit current gain of given amplifier:

We neglect  $r_{b'e}$  as it is very high value.



$$\text{Short circuit current gain } A_{ISC} = \frac{I_{SC}}{I_b} = -\frac{I_C}{I_b}$$

Apply KCL at  $B'$ ,

$$I_B = I_1 + I_2 + I_3$$

$$I_b = \frac{V_T}{r_T} + \left( \frac{V_T}{\frac{1}{j\omega C_T}} \right) + \frac{\frac{V_T}{1}}{\left( j\omega C_L \right)}$$

$$I_b = \frac{v_\pi}{r_\pi} + v_\pi [j\omega C_\pi + j\omega C_M]$$

$$\begin{aligned} I_b &= \frac{v_\pi}{r_\pi} + v_\pi j\omega [C_\pi + C_M] \\ &= \frac{v_\pi}{r_\pi} \left[ 1 + j\omega r_\pi (C_\pi + C_M) \right] \end{aligned}$$

Apply KCL at (C),

$$I_C + I_3 = g_m v_\pi$$

$$I_C \approx g_m v_\pi$$

The short-circuit current gain

$$A_{ISC} = -\frac{I_C}{I_b} = \frac{-g_m v_\pi}{\frac{v_\pi}{r_\pi} \left[ 1 + j\omega r_\pi (C_\pi + C_M) \right]}$$

$$A_{ISC} = \frac{-g_m r_\pi}{1 + j\omega r_\pi (C_\pi + C_M)}$$

$$= \frac{-g_m r_\pi}{1 + j(\frac{\omega}{\omega_B})}$$

$$\text{where } \omega_B = \frac{1}{r_\pi (C_\pi + C_M)}$$

$$f_B = \frac{1}{2\pi r_\pi (C_\pi + C_M)}$$

$$A_{ISC} = \frac{-g_m r_\pi}{1 + j(f/f_B)}$$

The magnitude of  $A_{Isc}$  is

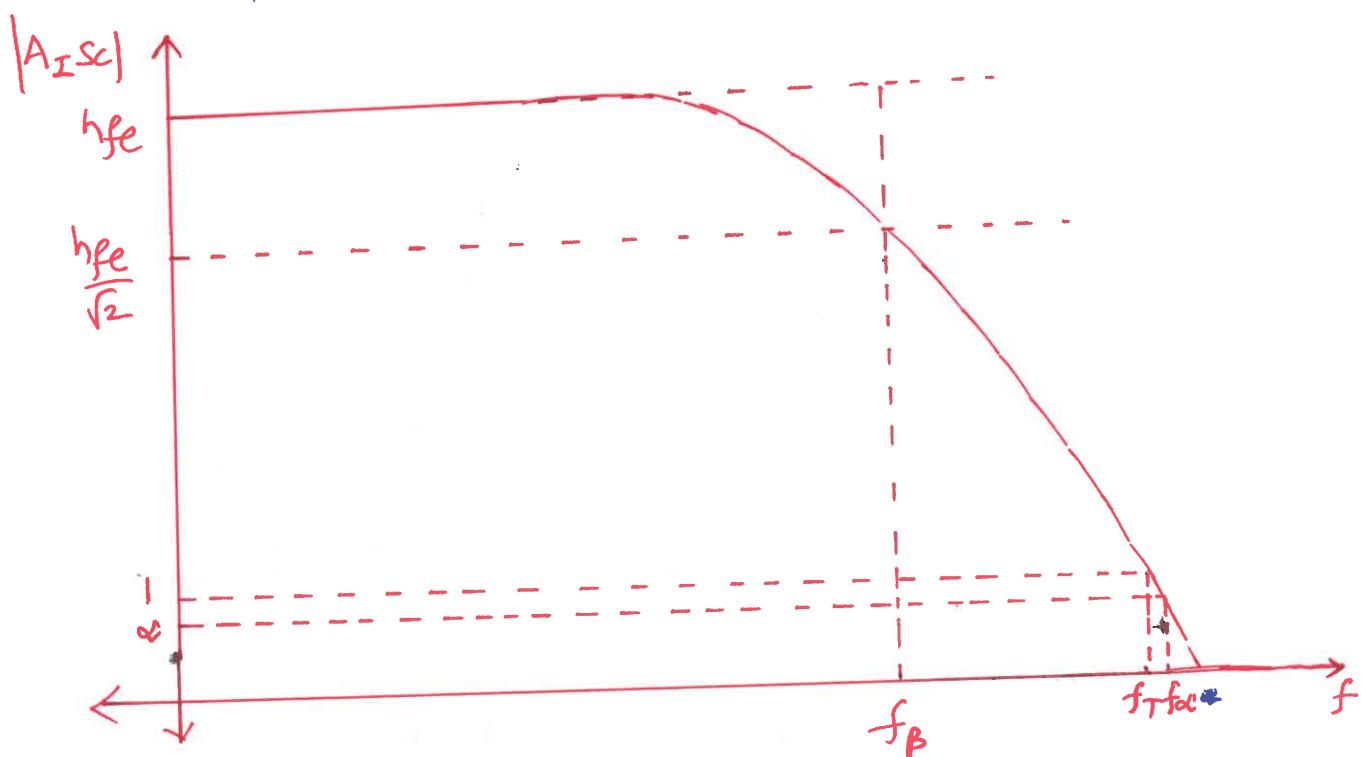
$$|A_{Isc}| = \frac{g_m r_\pi}{\sqrt{1 + \left(\frac{f}{f_B}\right)^2}}$$

when  $f=0$ ,  $|A_{Isc}| = g_m r_\pi = h_{fe} = \beta$

$$f=f_B, |A_{Isc}| = \frac{g_m r_\pi}{\sqrt{2}} = \frac{h_{fe}}{\sqrt{2}} = \frac{\beta}{\sqrt{2}}$$

$f_B \rightarrow$  upper cut-off (or)  $\beta$ -cut off frequency

when  $f=\infty$ ,  $|A_{Isc}| = 0$



$f_T \rightarrow$  unity gain frequency

$$|A_{Isc}| = 1 = \frac{g_m r_\pi}{\sqrt{1 + \left(\frac{f_T}{f_B}\right)^2}}$$

As  $f_T/f_B \gg 1 \Rightarrow \left(\frac{f_T}{f_B}\right)^2 \gg 1$

$$(A_{Isc}) = 1 \simeq \frac{g_m r_\pi}{(f_T/f_B)}$$

$$f_T \simeq f_B (g_m r_\pi)$$

$$f_T \simeq h_{fe} f_B \simeq \beta f_B$$

$$g_m r_\pi = h_{fe} \\ = \beta$$

The gain bandwidth product of any system is

Constant

$f_T$  → also called as unity gain bandwidth.

From this

$$f_T = h_{fe} f_B = \alpha f_\alpha$$

$$\Rightarrow \beta f_B = \alpha f_\alpha$$

$$\Rightarrow \beta f_B = \frac{\beta}{1+\beta} f_\alpha$$

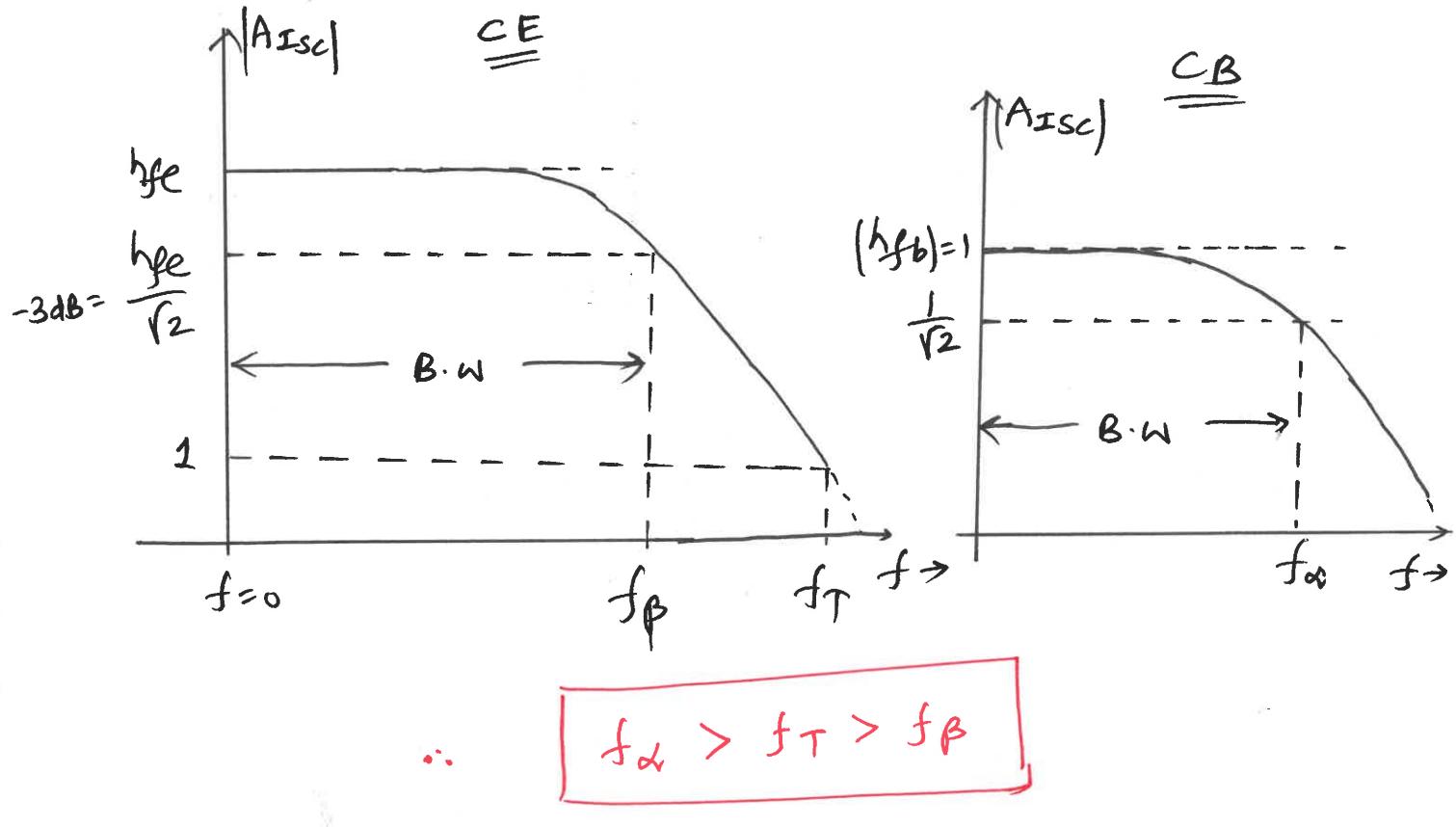
$$f_B = \frac{1}{1+\beta} f_\alpha$$

$$f_\alpha = (1+\beta) f_B$$

$$f_\alpha = f_B + \frac{\beta f_B}{1+\beta}$$

$$f_\alpha = f_B + f_T$$

$f_\alpha$  →  $\alpha$ -cut off frequency



Conclusion:

hybrid  $\pi$ -parameters depends on three important parameters.

- (i) collector current ( $I_c$ )  $\alpha$
- (ii) Temperature ( $T$ )
- (iii) Collector to Emitter voltage ( $V_{CE}$ )

$$\Rightarrow g_m = \frac{I_c}{V_{be}} = \frac{I_c}{I_b r_{be}} = \frac{I_c}{I_b \times (\beta \alpha e)} = \frac{1}{r_e} = \frac{(I_c)_{\alpha}}{V_T}$$

$$g_m = \frac{(I_c)_{\alpha}}{V_T} = \frac{(I_c)_{\alpha}}{T} \times 11,600$$

As  $T \uparrow$   $g_m \downarrow$

As  $(I_c)_{\alpha} \uparrow$   $g_m \uparrow$  //

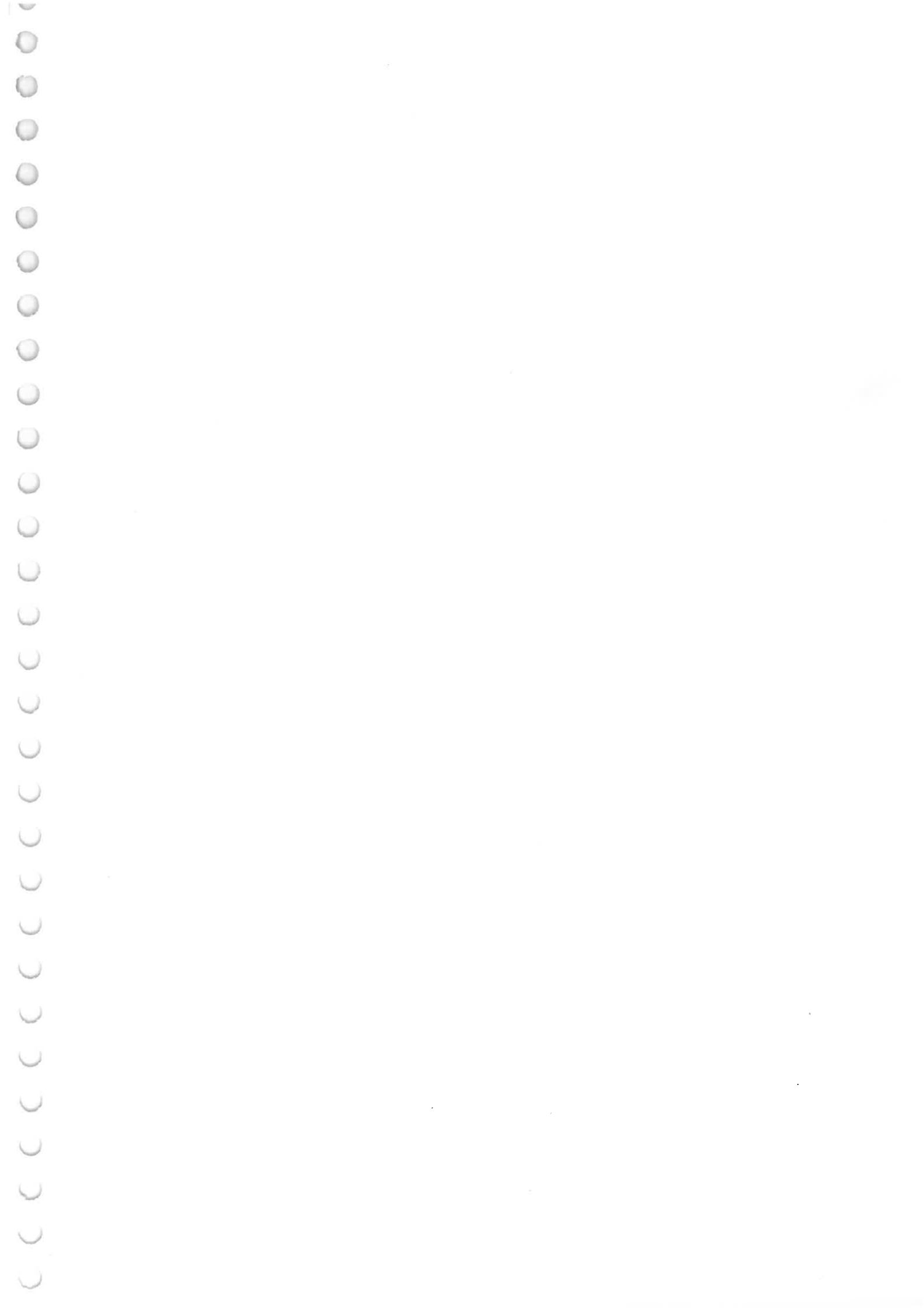
Eg: with  $g_m = 50 \text{ mA/V}$ ,  $r_{be} = 1 \text{ k}\Omega$ ,  $C_e = 1 \text{ pF}$  &  $C_C = 0.2 \text{ pF}$

determine the values of  $f_B$  and  $f_T$ .

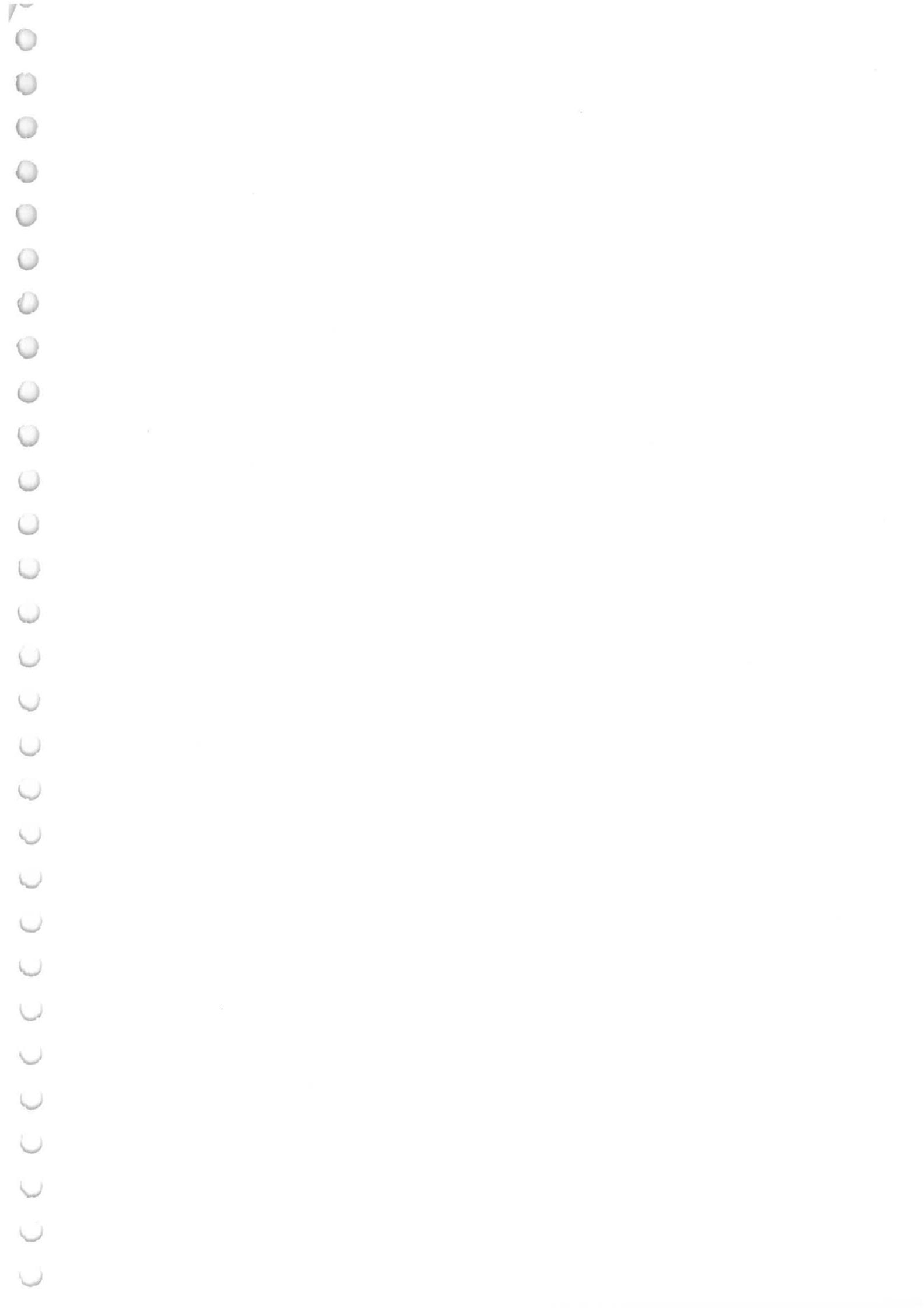
$$f_B = \frac{1}{2\pi r_{be}(C_C + C_e)} = \frac{1}{2\pi \times (1 \cdot 2 \text{ pF})} = \frac{1}{2\pi \times (1 \cdot 2 \text{ pF})} \\ = 133 \text{ MHz}$$

$$f_T = \frac{g_m}{2\pi(C_C + C_e)} = \frac{50 \text{ mA/V}}{2\pi \times (1 \cdot 2 \text{ pF})} = 6.6 \text{ GHz.}$$

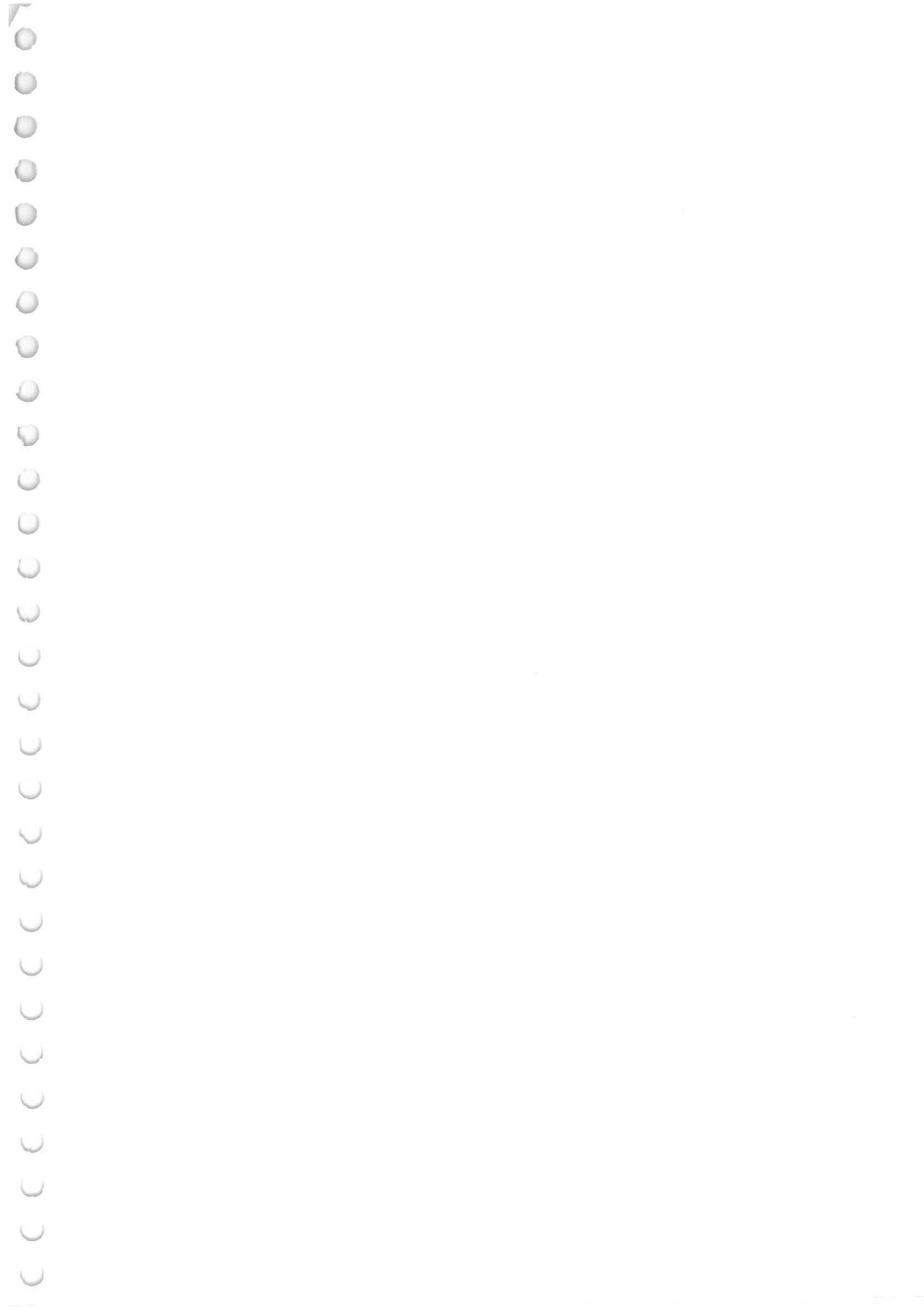
\*  $f_T$  represents the highest freq at which a transistor will provide a gain.









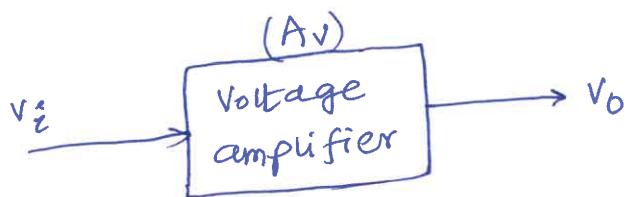




# operational Amplifier (OP-AMP):

Sudhakar Busi

ECE

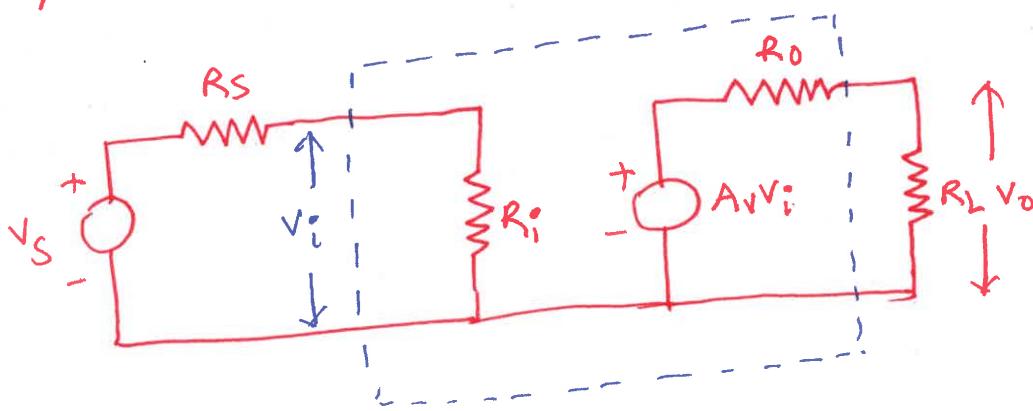


$$\text{Voltage gain } (A_v) = \frac{V_o}{V_i}$$

OP-AMP is a "VCVS"



Equivalent circuit of any Voltage amplifier.



$R_i$  = input resistance of amplifier.

$R_o$  = output resistance of amplifier.

\*  $R_i \ggg R_s$  so that  $V_s = V_i$

\*  $R_o \ll R_L$ , so that  $V_o = A_v V_i$

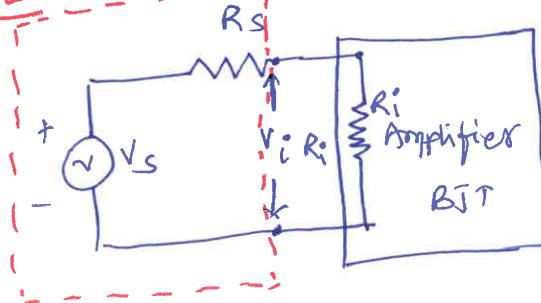
$$V_i = V_s \times \frac{R_i}{R_s + R_i}$$

If  $R_i \ggg R_s$   
then  $V_s = V_i$

$$V_o = \frac{R_L}{R_o + R_L} \times A_v V_i$$

If  $R_o \ll R_L$   
 $V_o = A_v V_i$

Example:



Here  
source (s) may be an antenna.

$V_i = V_s$  [ The total signal in the antenna transformed to the amplifier proper terminal)

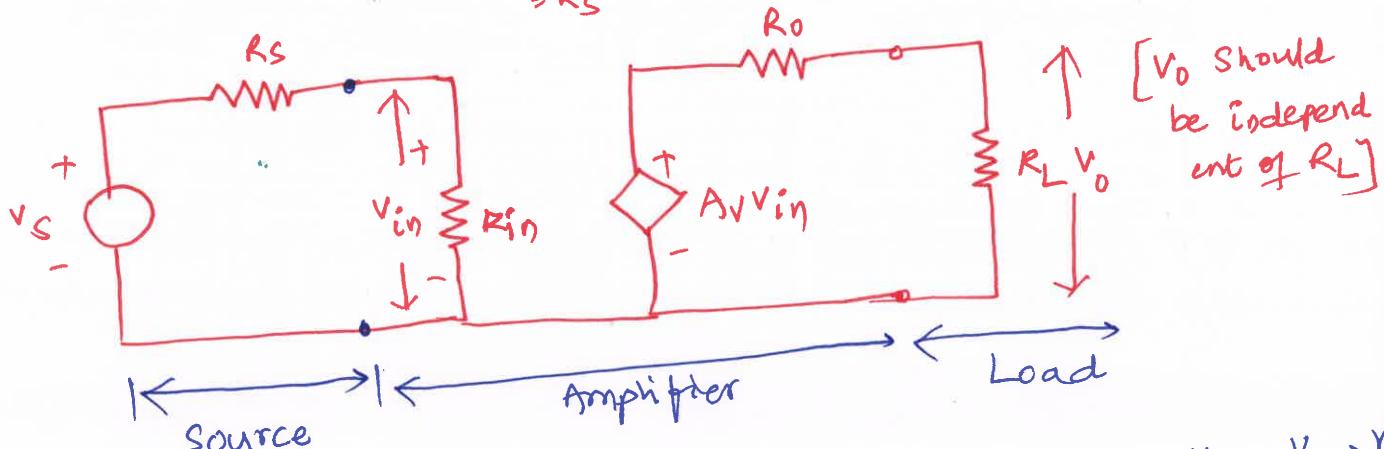
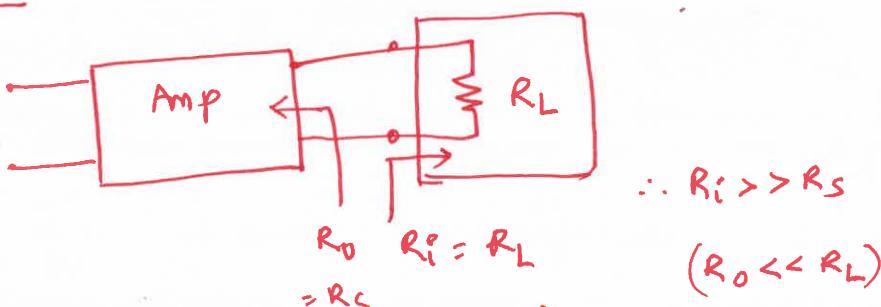
$$V_i = V_s \times \frac{R_i}{R_i + R_s} = V_s \times \frac{1}{1 + \frac{R_s}{R_i}}$$

$[R_s \ll R_i]$

that's the reason making  $R_i$  is very Large  
 $[R_i \gg R_s]$ .

High input resistance for Voltage amplifiers.

Output Side:



High Input impedance (Resistance) {  $R_{in} = \infty \rightarrow V_{in} = V_S \rightarrow V_C$   
 Low Output impedance {  $R_o = 0 \rightarrow V_o = A_v V_S \rightarrow V_S$   
 $\{ \text{So } V_C V_S \}$

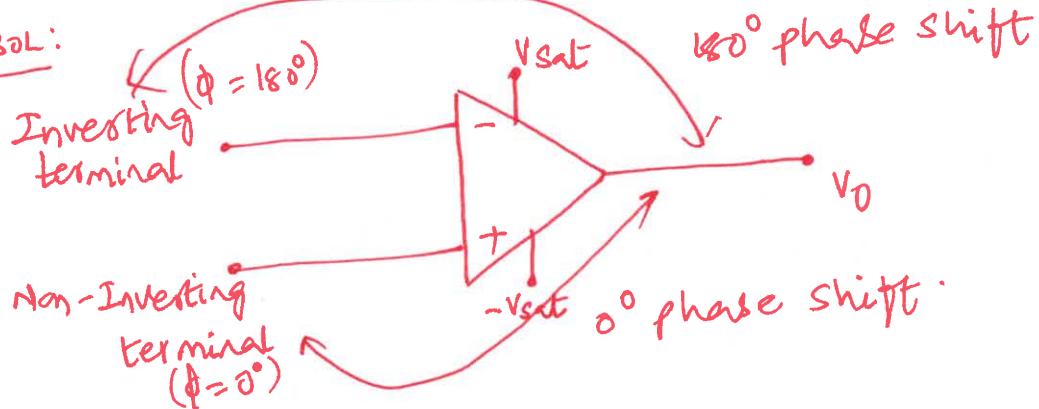
op-amp and Common-collector ckt's are voltage controlled Voltage sources i.e. (VCVS)

## OP-AMP CHARACTERISTICS:

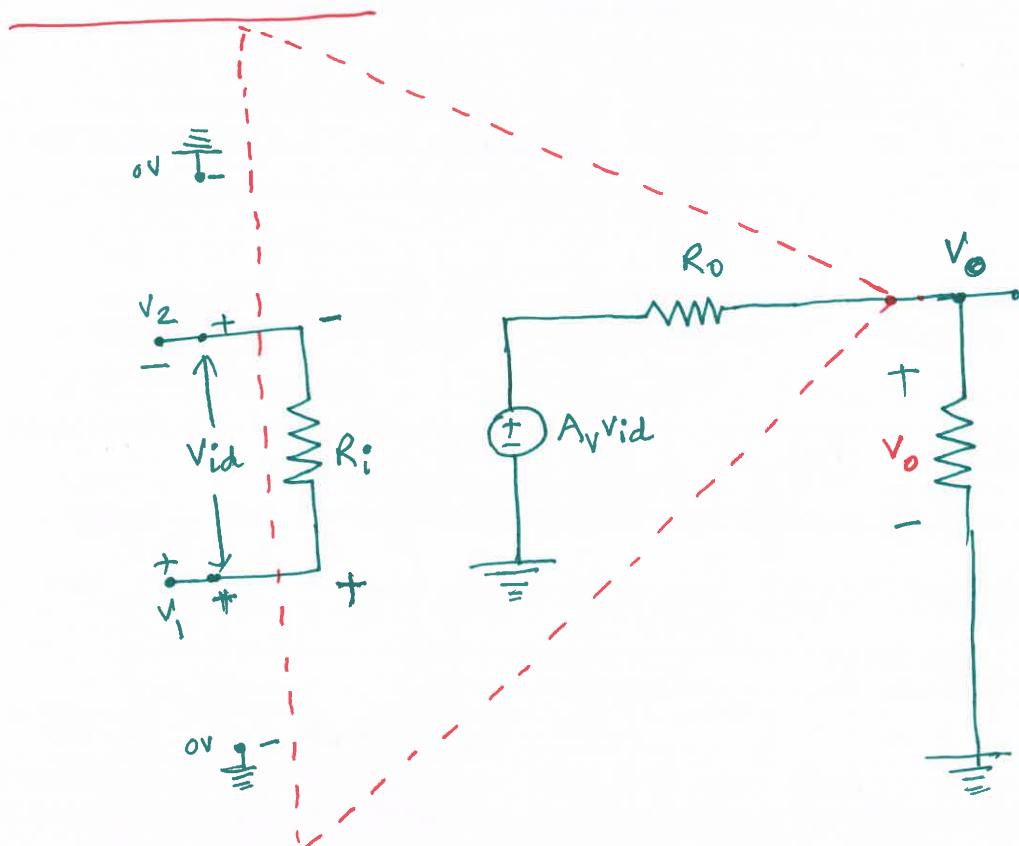
Characteristic	Ideal	Practical
1. Input resistance ( $R_{in}$ )	Very high ( $\infty$ )	$10^6 = 1M\Omega$
2. Output Resistance ( $R_o$ )	Very low (0)	$10 - 100 \Omega$
3. Voltage gain (open loop gain) ( $A_{OL}$ )	Very high ( $\infty$ )	$10^6$
4. Bandwidth (BW)	Very high ( $\infty$ )	$10^6 \text{ Hz}$ (for gain=1)
5. Gain Bandwidth $G \times (B \cdot W)$	$\infty$	$10^6 \text{ Hz}$
6. CMRR (Common Mode Rejection Ratio)	$\infty$	$10^6 (\infty) / 120 \text{ dB.}$
7. Slew rate (SR)	$\infty$	$80 \text{ V/Msec}$
8. Offset voltages	Very low (0)	

\* It is also referred as Basic Linear integrated circuit

### SYMBOL:



## Ideal Op-Amp:

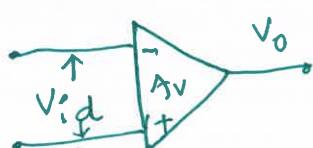


By writing KVL at the input side

$$-V_1 + V_{id} + V_2 = 0$$

$$V_{id} = V_1 - V_2$$

For any open loop Voltage amplifier



$$V_o = A_v V_{id}$$

implies

$$V_{id} = \frac{V_o}{A_v}$$

For an ideal op-amp:

$$A_v = \infty \text{ means } V_{id} = 0$$

$$\therefore V_1 - V_2 = 0$$

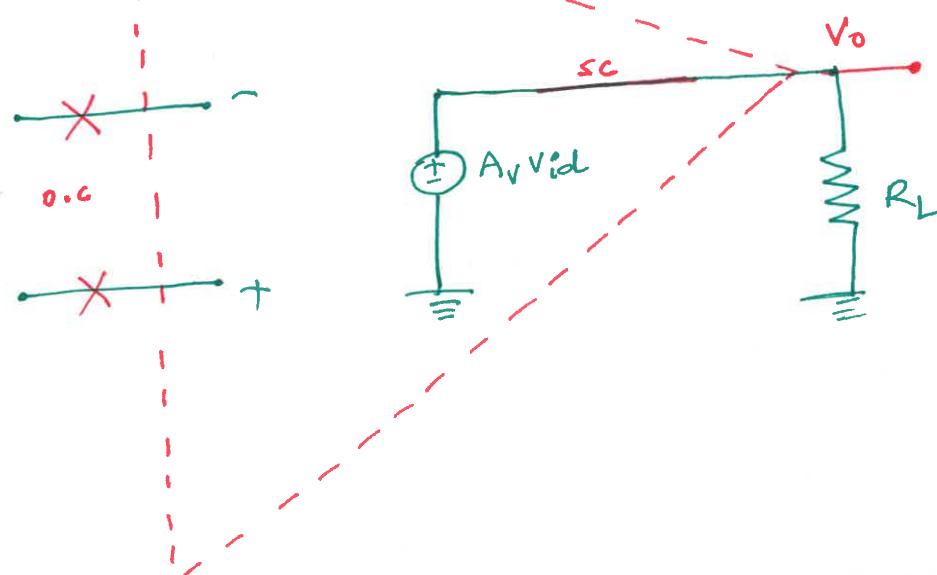
$$V_1 = V_2$$

So for an ideal op-amp the voltage at the Non-inverting terminal is always equal to the voltage at the inverting terminal.

\* For an ideal op-amp

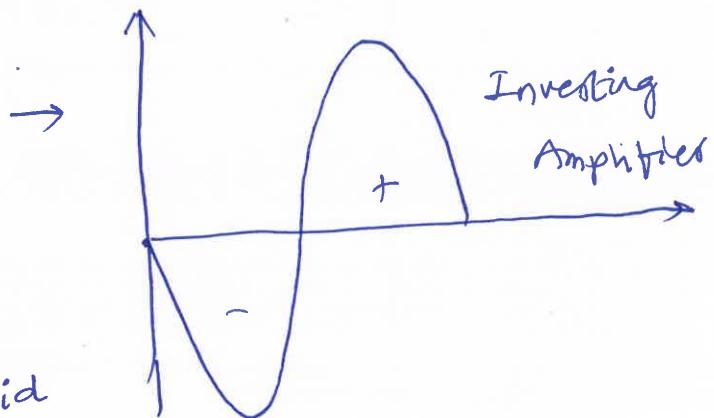
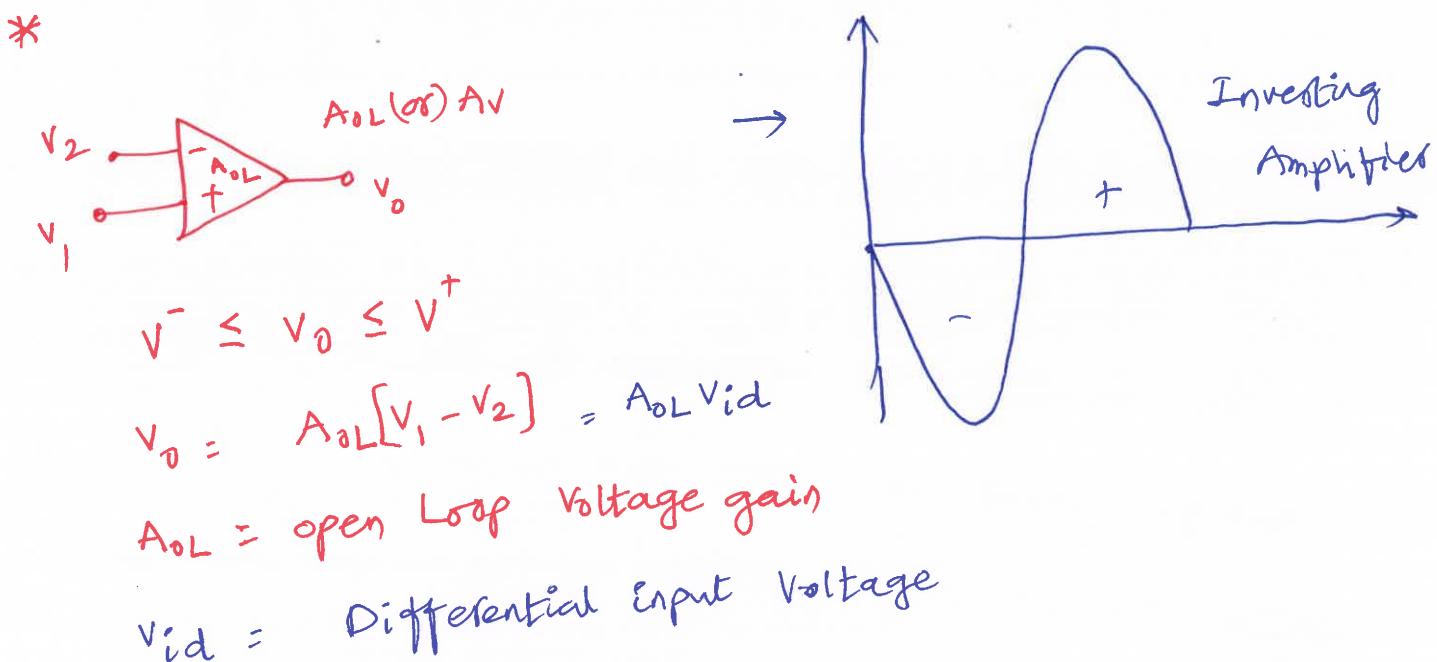
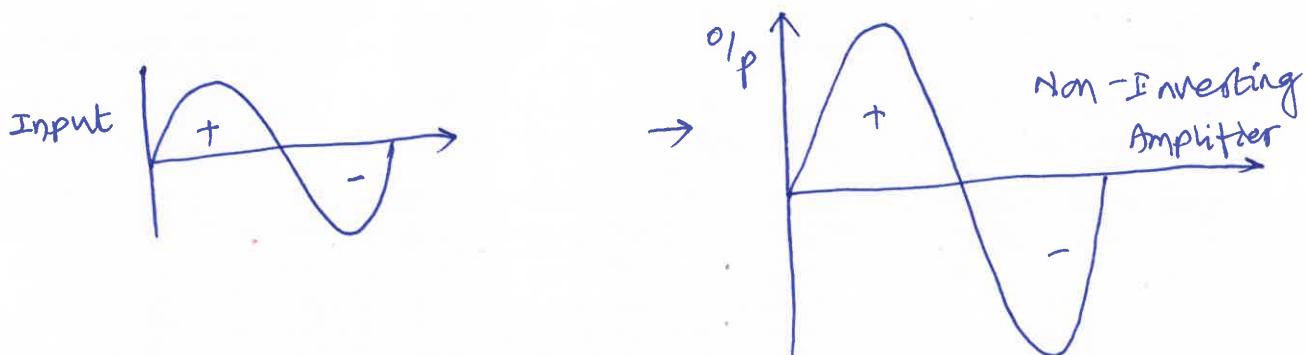
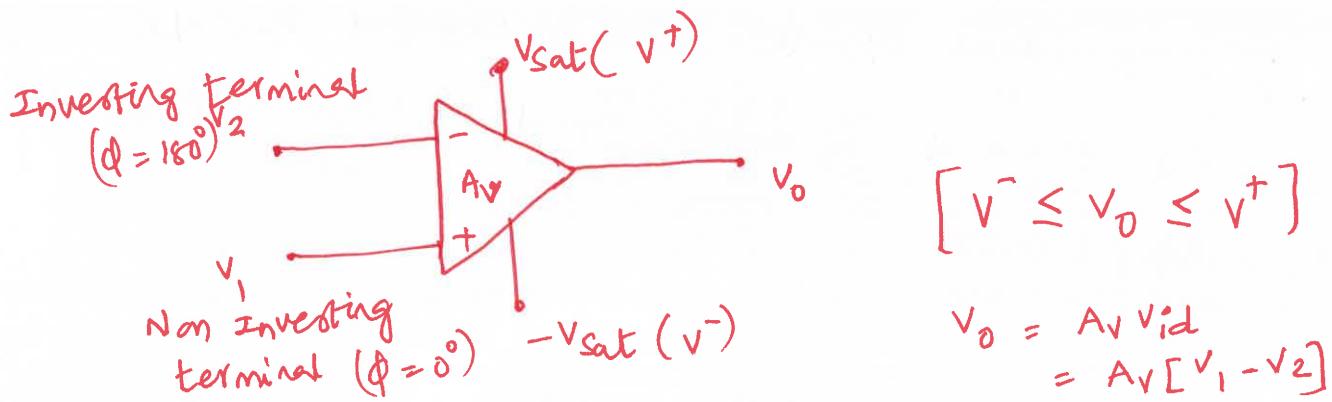
$$R_i = \infty \quad \text{and} \quad R_o = 0$$

Implies



So the input current accepted by the ideal op-amp is always equal to zero and hence it is possible to write the nodal equations at the input side of an ideal op-amp.

→ Since  $R_o = 0\Omega$ , there exists an ideal voltage source at the output side and current through it can be any value. It is not possible to write the nodal equations at the output side of an ideal op-amp.



For an op-amp,  $A_{OL} \rightarrow \text{Very high}; v_{id} \rightarrow \text{Very low}$   
 $v_{id} \rightarrow 0$

always  $A_{OL} > 10^6$  for properly designed op-amp

then 
$$v_0 = A_{OL} v_{id}$$

{  $A_{OL}$  or  $A_v$  }

$v_0 \rightarrow \text{finite}$  &  $v^- \leq v_0 \leq v^+$

For an ideal op-amp,  $A_{OL} = \infty$

$$V_{id} = 0$$

$$V_o = A_{OL} V_{id}$$

The  $o/p$  of the op-amp is not equal to zero in the open-loop mode.

- \* The output of the op-amp depends on differential input voltage and common mode (average voltage) voltage.

### Differential Amplifier:

Ideal:

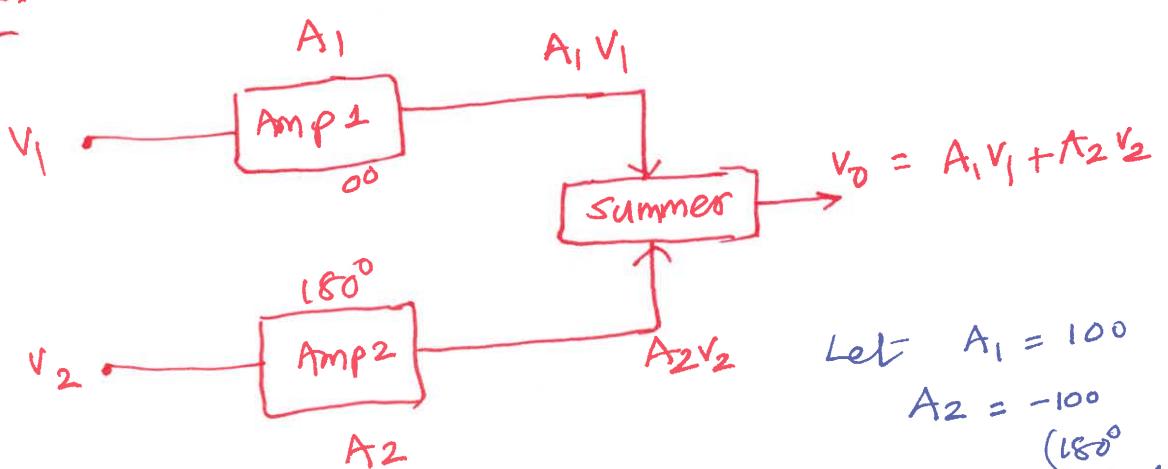


$$V_o = A_d V_{id}$$

$$V_{id} = v_1 - v_2 = \text{Difference Voltage}$$

$A_d$  = Differential gain

Practical:



$$\begin{aligned} \text{Let } A_1 &= 10^0 \\ A_2 &= -10^0 \\ (180^\circ \text{ phase shift}) \end{aligned}$$

$$\therefore \frac{V_o}{V_{id}} = \frac{100}{A_d} (v_1 - v_2)$$

\* To write the above equation,  $A_1$  and  $A_2$  should be equal with  $180^\circ$  phase difference, but it is not possible to have identical amplifiers.

$$V_o = 100V_1 - 90V_2 = 90(V_1 - V_2) + \text{noise}$$

\* If there is some noise signal is present at both terminals and ideally it should cancel out but for unidentical amplifiers.

$$\begin{aligned} V_o &= 100(V_1 + V_n) - 90(V_2 + V_n) \\ &= 90(V_1 - V_2) + \text{noise} \end{aligned}$$

For practical Amplifier:

$$V_o = A_d V_d + A_c V_c$$

error

→ (1)

where  $V_d = V_1 - V_2$  = Differential input voltage

$$V_c = \frac{V_1 + V_2}{2} = \text{Common mode Signal (po)}$$

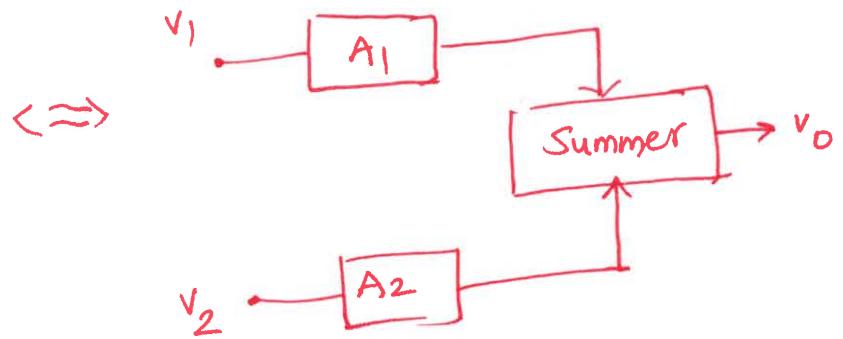
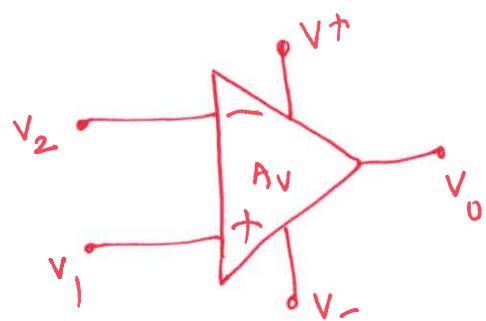
$A_c$  = Common mode gain

Common mode input voltage

Ideally  $A_c \rightarrow 0$

practically  $A_c$  is very small.

$A_d$  = Differential mode gain.



From above Figures

$$V_0 = A_1 V_1 + A_2 V_2$$

$V_1$  → Non-Inverting terminal Voltage

$V_2$  → Inverting terminal Voltage

$A_1$  → Gain of the op-amp due to  $V_1$  alone

$A_2$  → Gain of the op-amp due to  $V_2$  alone.

The total op Voltage of the Op Amp is

$$V_0 = A_1 V_1 + A_2 V_2 \quad \text{--- (2)}$$

We Know  $V_d = V_1 - V_2 \quad \text{--- (3)}$

$V_d$  = Differential input Voltage

$$V_c = \frac{V_1 + V_2}{2} \quad \text{--- (4)}$$

$V_c$  = Common Mode input Voltage.

$$v_d = v_1 - v_2 \rightarrow (3)$$

$$2v_c = v_1 + v_2 \rightarrow (4)$$

Adding (3) & (4)

$$2v_c + v_d = 2v_1$$

$$v_1 = v_c + \frac{1}{2}v_d \rightarrow (5)$$

Subtracting (3) from (4)

$$2v_c - v_d = 2v_2$$

$$v_2 = v_c - \frac{1}{2}v_d \rightarrow (6)$$

Substitute eq(5) and eq(6) in eq(2)

$$v_o = A_1 v_1 + A_2 v_2$$

$$v_o = A_1 \left[ v_c + \frac{1}{2}v_d \right] + A_2 \left[ v_c - \frac{1}{2}v_d \right]$$

$$v_o = \left( \frac{A_1 - A_2}{2} \right) v_d + (A_1 + A_2) v_c \rightarrow (7)$$

Comparing eq(1) and eq(7)

\*  $A_d = \frac{A_1 - A_2}{2}$

$$A_c = A_1 + A_2$$

$A_d$  : Differential mode voltage gain

$A_c$  : Common mode voltage gain

\* When  $V_d = 0$  i.e.  $V_1 = V_2$

$$V_c = V_1 = V_2$$

$$V_o = Ad \cancel{V_d} + Ac V_c$$

$$V_o = Ac V_c \neq 0$$

Second Method:

Calculation of  $A_c$ :

$$\text{put } V_1 = V_2 = V_s \Rightarrow V_c = \frac{V_1 + V_2}{2} = \frac{2V_s}{2} = V_s$$
$$\therefore V_c = V_s$$

$$\therefore V_d = V_1 - V_2 = 0 \Rightarrow V_o = Ad V_d + Ac V_c$$

$$V_o = 0 + Ac V_s$$

$$\therefore \boxed{A_c = \frac{V_o}{V_s}}$$

Calculation of  $A_d$ :

$$\text{put } V_1 = \frac{V_s'}{2} \text{ and } V_2 = -\frac{V_s'}{2}$$

$$\therefore V_d = V_1 - V_2 = \frac{V_s'}{2} - \left(-\frac{V_s'}{2}\right) = V_s'$$

$$\text{and } V_c = 0$$

$$\therefore \boxed{A_d = \frac{V_o}{V_s'}}$$

## CMRR:

CMRR is the ratio of magnitudes of differential mode gain to Common mode gain.

$$CMRR = \frac{|A_d|}{|A_c|}$$

$$\begin{aligned} CMRR &= \frac{\left| \frac{A_1 - A_2}{2} \right|}{|A_1 + A_2|} \\ &= \frac{1}{2} \left| \frac{A_1 - A_2}{A_1 + A_2} \right| \end{aligned}$$

$A_1$  is always +ve and  $A_2$  is always -ve value.  
 $\therefore$  we get very high CMRR.

\* For a general purpose op-amp, CMRR is upto 100dB

$$(CMRR)_{dB} = 20 \log_{10} \left| \frac{A_d}{A_c} \right| = 100$$

$$\left| \frac{A_d}{A_c} \right| = 10^5$$

\* The output of the op-amp mainly depends on the differential input voltage only.

So Op-amp is a differential amplifier also

$$|A_d| = 10^5 |A_c|$$

$$\text{as } |A_d| \gg |A_c|$$

$$A_d V_d \gg A_c V_c$$

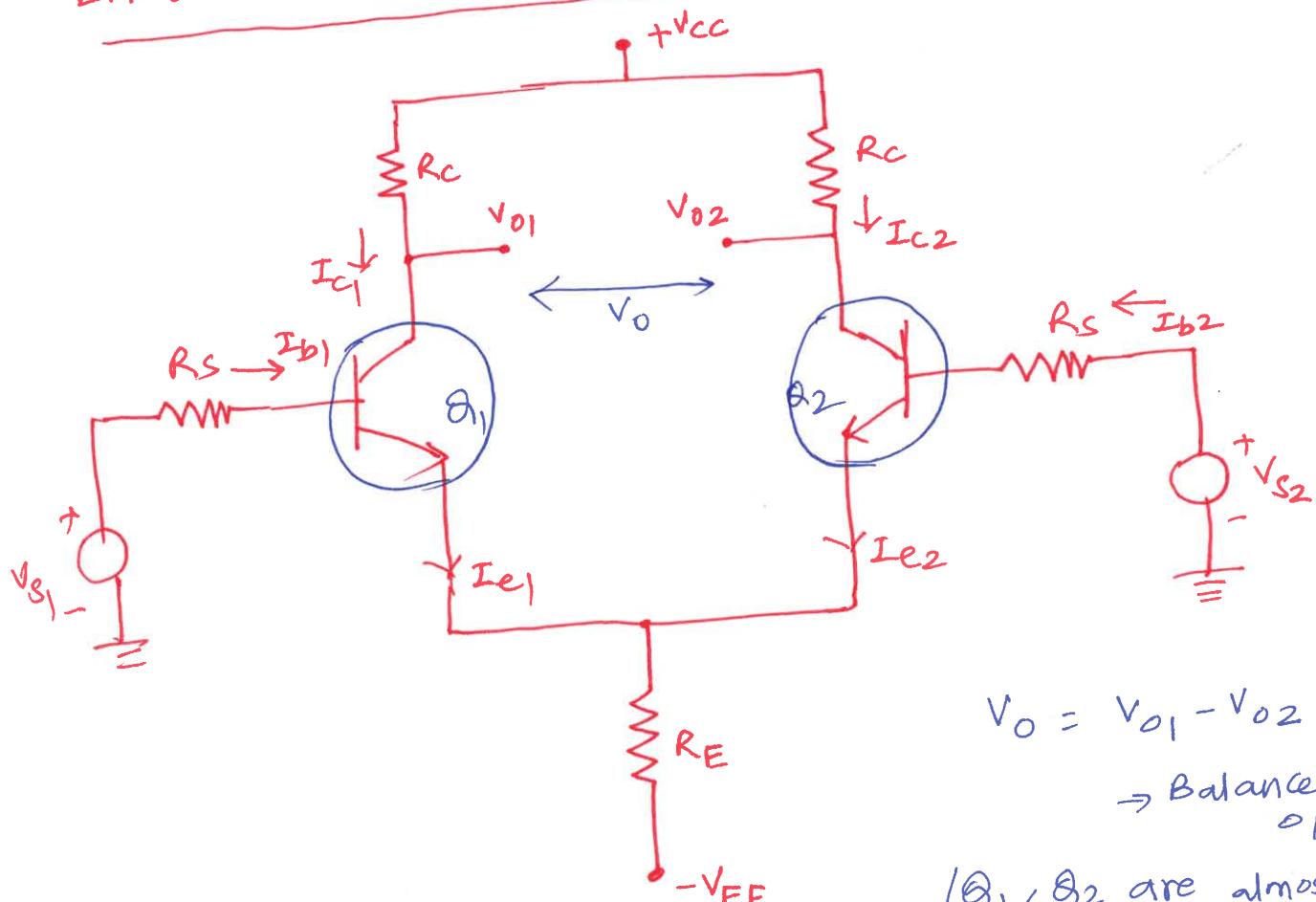
$$V_o = A_d V_d + A_c V_c$$

$\therefore V_o \approx A_d V_d$

for op-amp ,  $A_{OL} \rightarrow$  very high  
 $V_{id}(\infty) V_d \approx 0$ .

- \* The ability of the Op-amp to reject the output Voltage due to Common mode Signal is CMRR.

### Emitter Coupled Differential Amplifier:



$$V_O = V_{O1} - V_{O2}$$

$\rightarrow$  Balanced  
Op

(Q<sub>1</sub>, Q<sub>2</sub> are almost identical)

It has following characteristics:

1. High CMRR

2. High Input Resistance ( $R_i$ )

3. Low drift because of its

Symmetrical Construction.

The circuit is an excellent differential amplifier if  $R_E$  is Large.

This statement can be justified as follows

If  $V_{S1} = V_{S2} = V_S$ ; then  $V_d = V_{S1} - V_{S2} = 0$

and  $V_o = A_c V_S$ .

However if  $R_E = \infty$ , because of symmetry of figure, we obtain  $I_{E1} = I_{E2} = 0$ .

If  $I_{BQ} \ll I_{C2}$  then  $I_{C2} \approx I_{E2}$  and it follows

that  $V_o = 0$ . Hence the Common mode gain  $A_c$  becomes very small and CMRR is very

large.

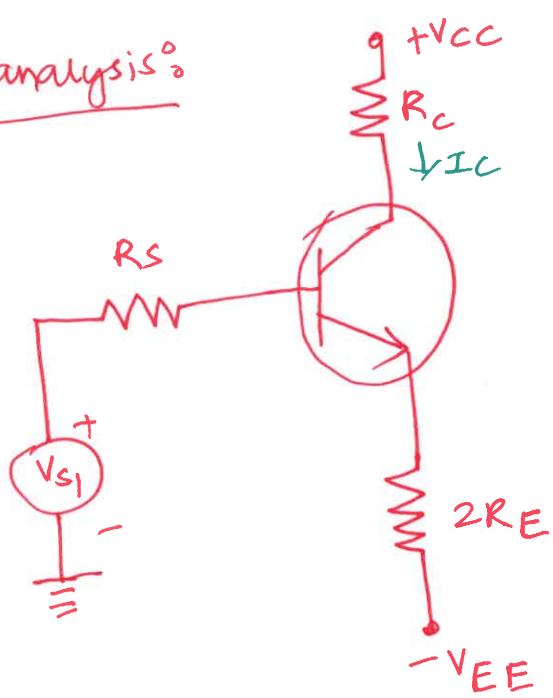
\* We have to analyse the Emitter Coupled

circuit for a finite value of  $R_E$ .  $A_c$  can be

evaluated by setting  $V_{S1} = V_{S2} = 0$  and making use of symmetry of fig. It can be bisected

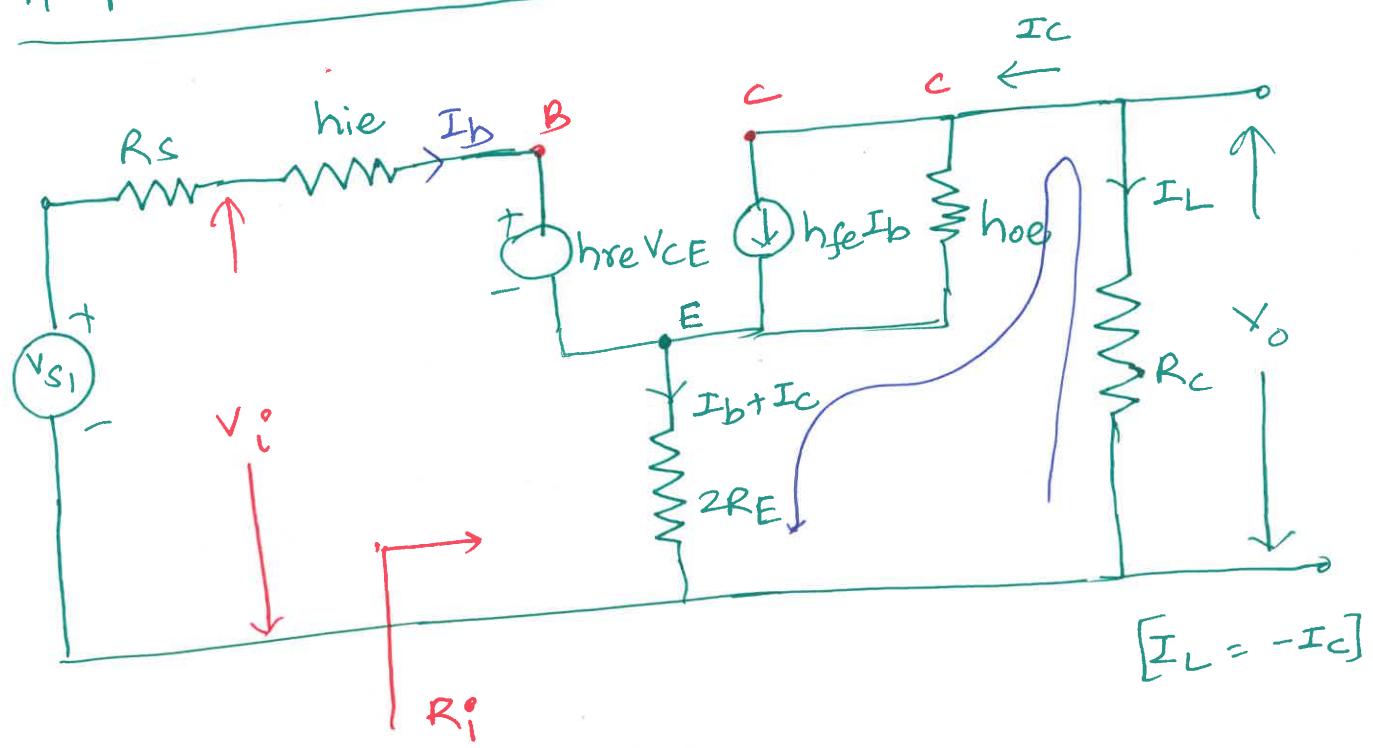
due to its symmetrical construction for the analysis purpose.

AC analysis:



$A_{CE}$

h-parameter model:



From the output circuit  $V_O = I_L R_C = -I_C R_C$

From the input side

$$-V_S + (R_S + R_I) I_B = 0$$

$$V_S = (R_S + R_I) I_B$$

$$A_I = \frac{I_L}{I_B} = \frac{-I_C}{I_B}$$

$$\therefore A_C = \frac{V_O}{V_S} = \frac{-I_C R_C}{(R_S + R_I) I_B} = A_I \left( \frac{R_C}{R_S + R_I} \right)$$

$$\text{Voltage drop across } h_{oe} = \frac{1}{h_{oe}} (I_c - h_{fe} I_b)$$

Writing KVL around output circuit,

$$I_c R_c + \frac{(I_c - h_{fe} I_b)}{h_{oe}} + (I_b + I_c) 2R_E = 0$$

$$I_c \left[ \frac{1}{h_{oe}} + 2R_E + R_c \right] = I_b \left[ \frac{h_{fe} - 2R_E}{h_{oe}} \right]$$

$$I_c \left[ \frac{1 + h_{oe} (2R_E + R_c)}{h_{oe}} \right] = I_b \left[ \frac{h_{fe} - 2R_E (h_{oe})}{h_{oe}} \right]$$

$$\therefore \text{Current gain } A_I = -\frac{I_c}{I_b}$$

$$= \frac{2R_E h_{oe} - h_{fe}}{1 + h_{oe} (2R_E + R_c)}$$

$$\text{Now } R_i \text{ (Input Resistance)} = \frac{V_i}{I_b}$$

Writing KVL to the input circuit (loop)

$$-V_i + h_{ie} I_b + h_{oe} V_{CE} + (I_b + I_c) 2R_E = 0$$

$$\therefore V_i = h_{ie} I_b + h_{oe} V_{CE} + (I_b + I_c) 2R_E$$

$$\therefore R_i = \frac{V_o}{I_b} = h_{ie} + \frac{h_{re} V_{CE}}{I_b} + \left( \frac{I_b + I_c}{I_b} \right) 2R_E$$

$$\begin{aligned} \text{But } V_{CE} &= V_C - V_E \\ &= I_L R_C - (I_b + I_c) 2R_E \\ &= -I_C R_C - (I_b + I_c) 2R_E \end{aligned}$$

$$\begin{aligned} \therefore \frac{V_{CE}}{I_b} &= -\frac{I_C}{I_b} R_C - \frac{(I_b + I_c) 2R_E}{I_b} \\ &= A_I R_C - (1 - A_I) 2R_E \end{aligned}$$

$$\therefore R_i = h_{ie} + h_{re} [A_I R_C - (-A_I) 2R_E] + (1 - A_I) 2R_E$$

$$R_i = h_{ie} + A_I [h_{re} (R_C + 2R_E) - 2R_E]$$

-  $h_{re} 2R_E + 2R_E$

$h_{re} 2R_E$        $+ 2R_E$   
*neglect*

$$\therefore R_i = h_{ie} + A_I [h_{re} (R_C + 2R_E) - 2R_E] + 2R_E$$

$$\therefore A_C = A_I \times \left[ \frac{R_C}{R_S + R_i} \right]$$

$$A_C = \frac{\left[ \frac{2RE_{hoe} - hfe}{1 + hoe(2RE + RC)} \right] \times RC}{R_S + hie + AI \left[ \frac{hoe(R_C + 2RE) - 2RE}{+ 2RE} \right]}$$

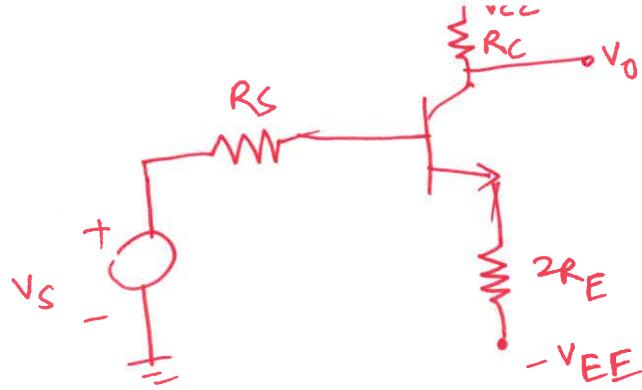
If  $hoe(R_C + 2RE) \ll 2RC$  and

$$hoeRC \ll 1$$

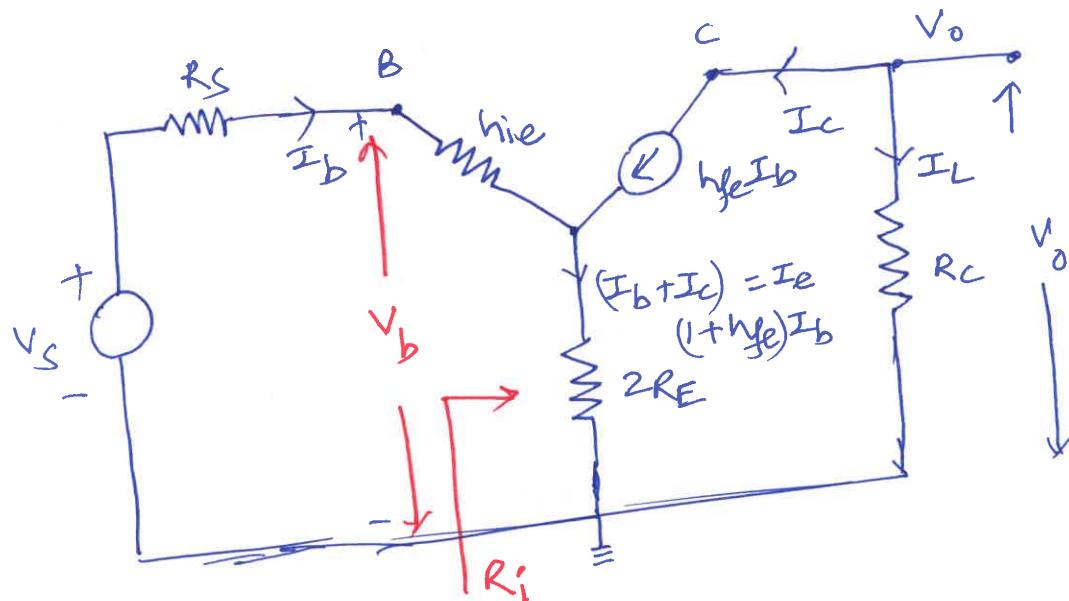
$$\therefore A_C = \frac{\left( \frac{(2RE_{hoe} - hfe)}{1 + hoe(2RE)} \right) \times RC}{(R_S + hie) - 2RE \left[ \frac{2RE_{hoe} - hfe}{1 + hoe(2RE)} \right] + 2RE}$$

$$A_C = \frac{(2RE_{hoe} - hfe) RC}{(R_S + hie) \left[ 1 + hoe(2RE) \right] + 2RE \left[ (1 + hfe) \right]}$$

Simplified Model :



Simplified hybrid Model:



$$\text{From Circuit } A_I = \frac{I_L}{I_B} = \frac{-I_C}{I_B} = \frac{-h_{fe}I_B}{I_B} = -h_{fe}$$

$$R_i = \frac{V_b}{I_B}$$

Writing KVL to the input circuit

$$-V_b + h_{ie}I_B + (1+h_{fe})I_B(2R_E) = 0$$

$$\therefore V_b = h_{ie}I_B + (1+h_{fe})I_B(2R_E)$$

$$R_i = \frac{V_b}{I_B} = h_{ie} + (1+h_{fe})2R_E.$$

$$A_C = \frac{V_o}{V_S} = \frac{-I_C R_C}{(R_S + R_i) I_B} = A_I \left( \frac{R_C}{R_S + R_i} \right)$$

$$\therefore A_C = \frac{-h_{fe} R_C}{R_S + h_{ie} + (1+h_{fe})^2 R_E}$$

$$\therefore A_C = \frac{-h_{fe} R_C}{h_{ie} + (1+h_{fe})^2 R_E}$$

Approximate:

$$A_C = \frac{-R_C}{2R_E}$$

when  $h_{fe} \gg 1$

\* Ideally  $A_C = 0 \Rightarrow R_E \rightarrow \infty$  (possible with current mirror ckt)

\*  $\boxed{\text{As } R_E \uparrow, A_C \downarrow}$

2. Analysis to find out  $A_d$ :

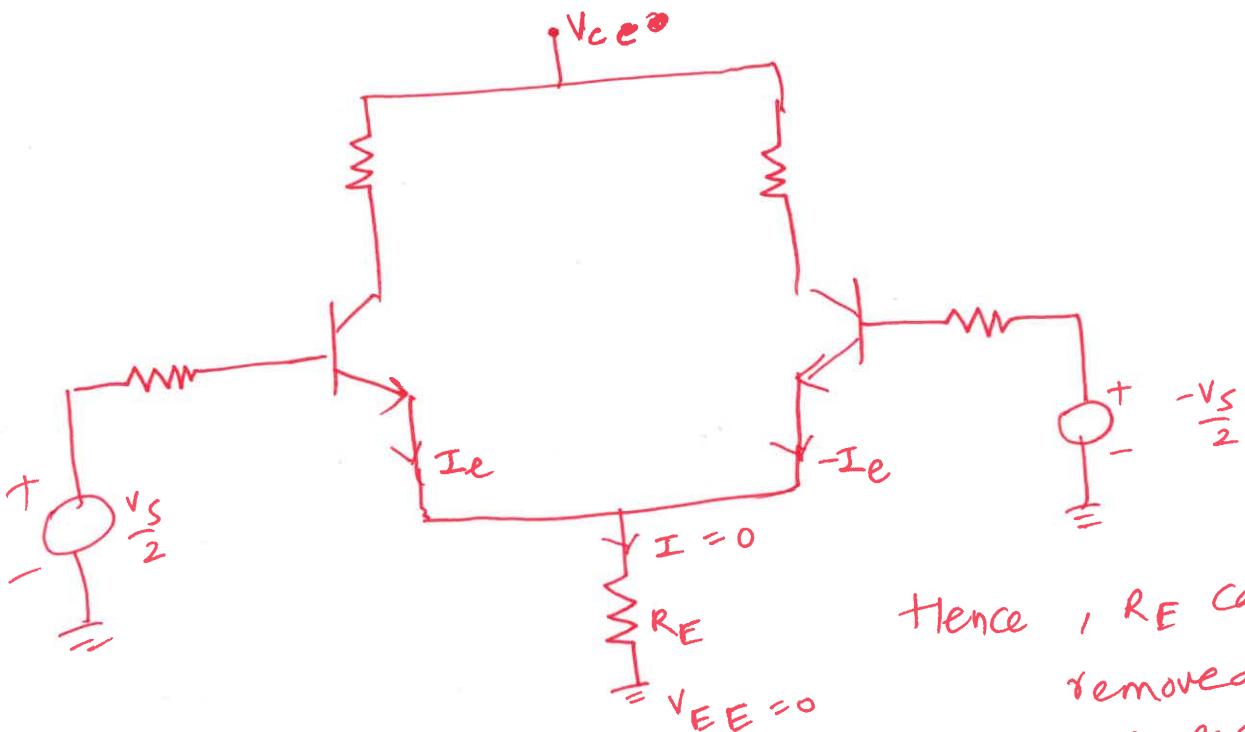
$$V_{S_1} = -V_{S_2} = \frac{V_S}{2}$$

$$\therefore V_d = V_{S_1} - (-V_{S_2})$$

$$\text{For } A_d: V_{S_2} = -\frac{V_S}{2}, V_{S_1} = \frac{V_S}{2}$$

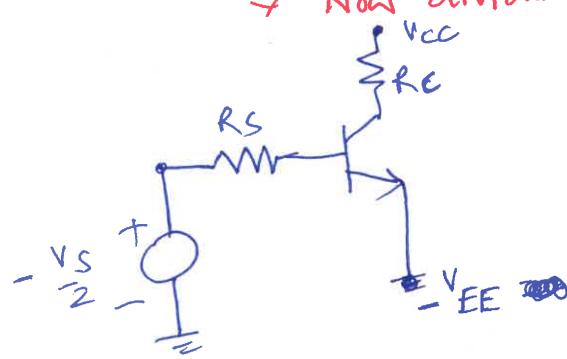
$$\therefore V_d = V_S, V_C = 0$$

$$\therefore A_d = \frac{V_o}{V_S}$$



Hence,  $R_E$  can be removed (or) short ckt.

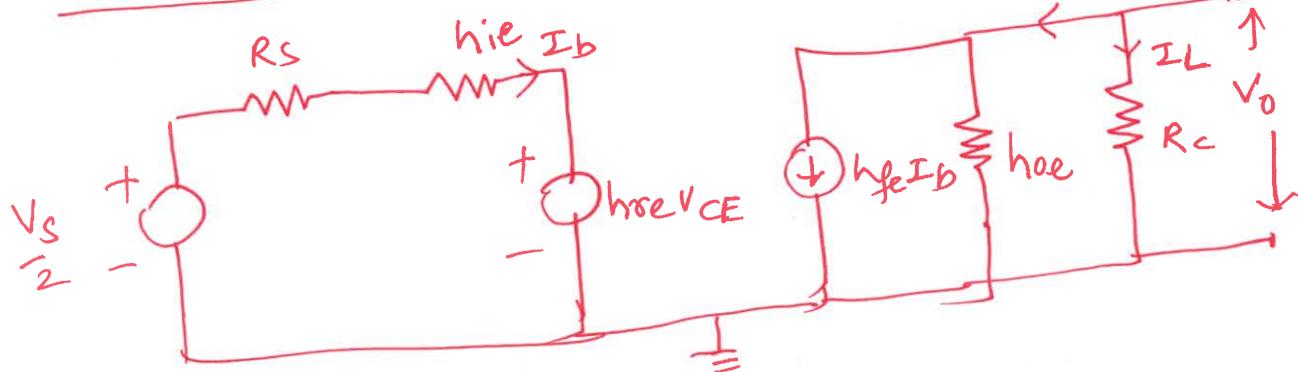
II Now dividing the CKT



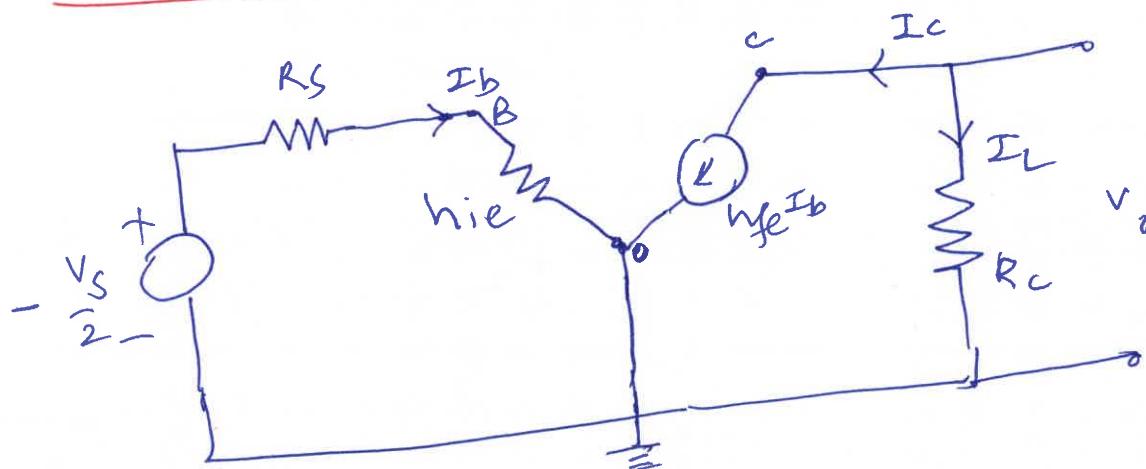
Current flowing through  $R_E$  is zero. So emitter terminals of each transistor are at ground potential.

So for AC analysis, the emitter terminals of each transistor are at ground potential.

h-parameter model:



## Simplified hybrid model



From output circuit

$$\begin{aligned} V_O &= I_L R_C \\ &= -I_C R_C \\ &= -h_{FE} I_B R_C \end{aligned}$$

From input circuit

$$-\frac{V_S}{2} = (R_S + h_{IE}) I_B$$

$$V_S = -2(R_S + h_{IE}) I_B$$

$$\begin{aligned} \therefore A_d &= \frac{V_O}{V_S} = \frac{-h_{FE} I_B R_C}{-2(R_S + h_{IE}) I_B} \\ &= \frac{h_{FE} R_C}{2(R_S + h_{IE})} \end{aligned}$$

$$\therefore CMRR = \left| \frac{A_d}{A_c} \right|$$

$A_d$  : It does not depend on  $R_E$ .

$$CMRR = \frac{\left| \frac{h_{fe} R_C}{2(R_S + h_{ie})} \right|}{\left| \frac{-h_{fe} R_C}{R_S + h_{ie} + (1+h_{fe})^2 R_E} \right|}$$

$$= \frac{R_S + h_{ie} + (1+h_{fe})^2 R_E}{2(R_S + h_{ie})}$$

If  $(1+h_{fe})^2 R_E \gg R_S + h_{ie}$ , then

$$CMRR = \frac{(1+h_{fe})^2 R_E}{2(R_S + h_{ie})}$$

$$CMRR = \frac{(1+h_{fe}) R_E}{(R_S + h_{ie})}$$

As  $R_E \rightarrow \infty$  then  $CMRR \rightarrow \infty$  (ideal value)

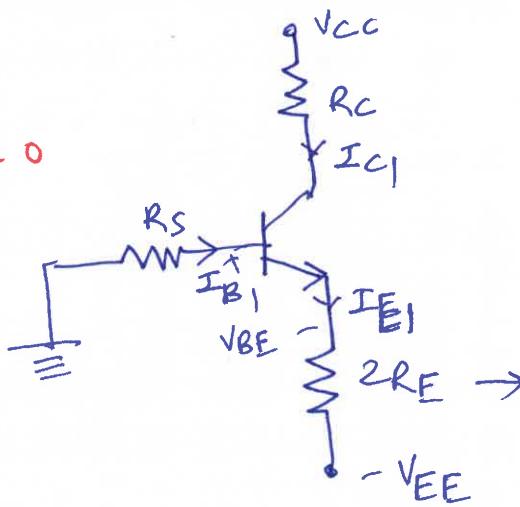
\*  $\theta_m = \frac{|I_C|}{V_T}$  as  $R_E \uparrow$ ,  $V_{EN} \uparrow$  Feedback  $\uparrow$   
 $I_B \downarrow \Rightarrow I_C \downarrow$

Effect of increasing  $R_E$ :

- 1) Negative feedback across  $R_E \uparrow$ es
- 2)  $A_C \downarrow$ ,  $CMRR \uparrow$ es,  $\theta_m \downarrow$  - gain  $\downarrow$   
 $\{ \text{gain} \propto \theta_m \}$
- 3)  $R_i \uparrow$

## DC Analysis:

$$V_{S1} = V_{S2} = 0$$



( $\beta$  or  $h_f$ )

Applying KVL:

$$I_{B1}R_S + V_{BE} + (1+\beta)I_B(2R_E) - V_{EE} = 0 \rightarrow (1)$$

(bcz of feedback)  
potential should  
be equal to  $2I_E R_E$   
but  $I_E$  cannot be  
doubled, hence  
Resistance is doubled.

$$-V_{CC} + I_{C1}R_C + V_{CE} + (1+\beta)I_B(2R_E) - V_{EE} = 0 \rightarrow (2)$$

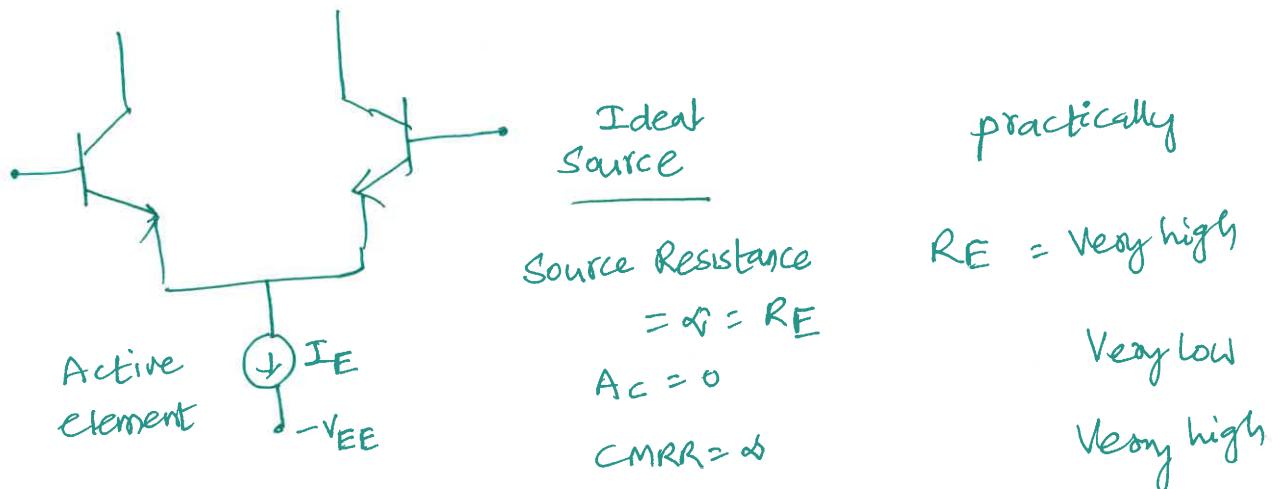
$$I_{C1} = \beta I_{B1} \rightarrow (3)$$

Now if  $V_{CE} > 0.2$ , transistor is in active region.

## Applications:

1. It is used as the first internal stage in op-amp.
2. As an instrumentation amplifier.
3. As a very good clipper.
4. As a Linear amplifier i.e. We can apply Superposition theorem.
5. It is used in designing of AVC (Automatic voltage control) or AGC (Automatic gain control).

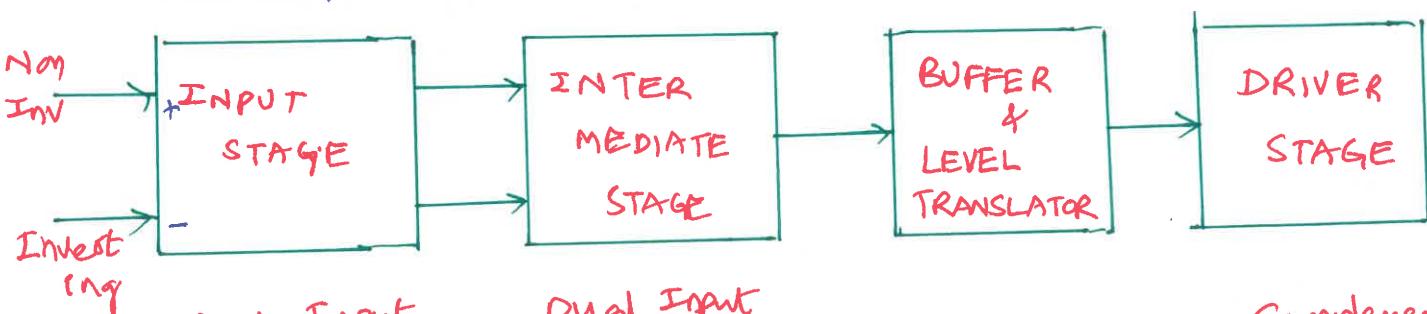
\* Any ideal differential amplifier can be designed by connecting an ideal current source in place of  $R_E$ .



\* In a practical diff. amplifier, active load is connected to get best performance. In place of passive load  $R_C$ , pnp transistor is used to get maximum peak to peak output voltage (or) maximum swing.

### OPERATIONAL AMPLIFIER INTERNAL CIRCUIT:

\* An operational amplifier is basically a very high gain, direct coupled amplifier with high input impedance and low output impedance.



Dual Input  
Balanced output  
Differential amplifier

Dual Input  
Unbalanced output Diff Amplifier

Complementary Symmetry  
push pull  
power amplifier

The first two stages are cascaded differential amplifiers used to provide high gain and high input resistance.

The third stage acts as a buffer as well as a level shifter (translator).

The Buffer is usually an emitter follower whose input impedance is very high so that it prevents loading of the high gain stage.

The Level shifter adjusts the d.c voltages so that output voltage is zero for zero inputs.

The adjustment of d.c level is required as the gain stages are direct coupled.

\* As it is not possible to fabricate large values of capacitors, all IC's are direct coupled usually.

\* The output stage is designed to provide a low output impedance [The final stage usually a complementary symmetry push pull power amplifier. The output voltage increases the output voltage swing and raises the current supply capability of the op-amp.

An output stage is also provide low output resistance.

## Differential Amplifier:

The main purpose of the difference amplifier stage is to provide high gain to the difference-mode signal and cancel the common-mode signal.

\* The relative sensitivity of an op-amp to a difference signal as compared to common-mode signal is called Common-Mode Rejection Ratio (CMRR).

→ It gives the Figure of merit of the differential amplifier.

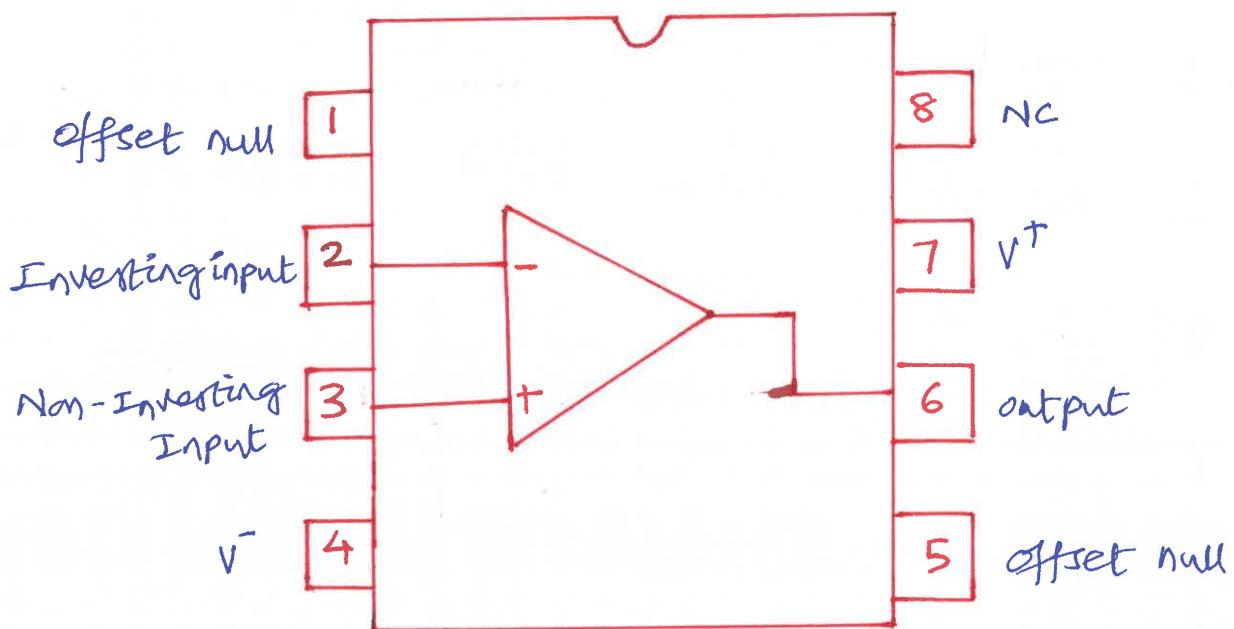
\* The higher the value of CMRR, better is the op-amp.

\* since, the input stage amplifier and the intermediate stage amplifiers are direct coupled. The dc voltage at the output of the intermediate stage tends to rise above the ground, which is not desirable.

\* To make the dc voltage down to zero, a level shifter (or level translator) is employed. This is usually is an emitter follower which also acts as a buffer, with very high input resistance & low opf resistance.

\* The output stage consists of a Complementary Symmetry class-B push pull power amplifier, which helps to increase the output voltage swing.

### PIN DIAGRAM OF 741 IC



- (2) : Inverting Input
- (3) : Non Inverting Input
- (4) : Negative Supply
- (7) : +ve supply
- (6) : output .

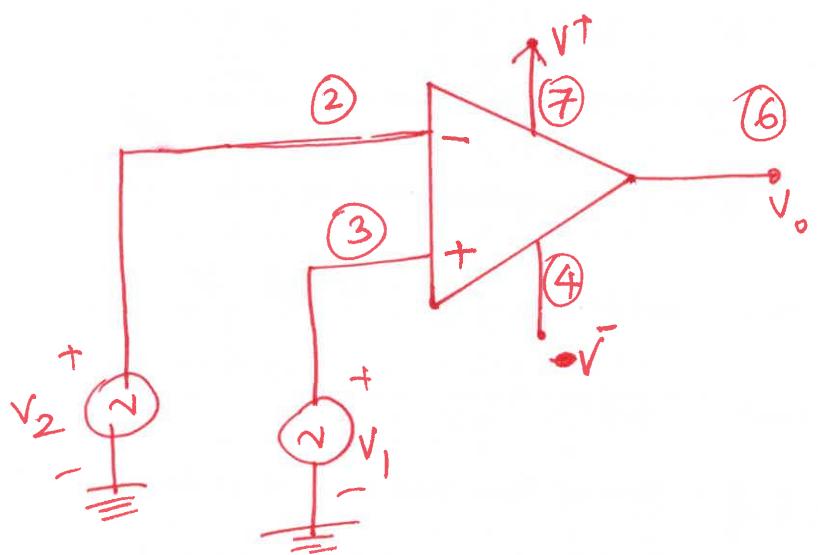
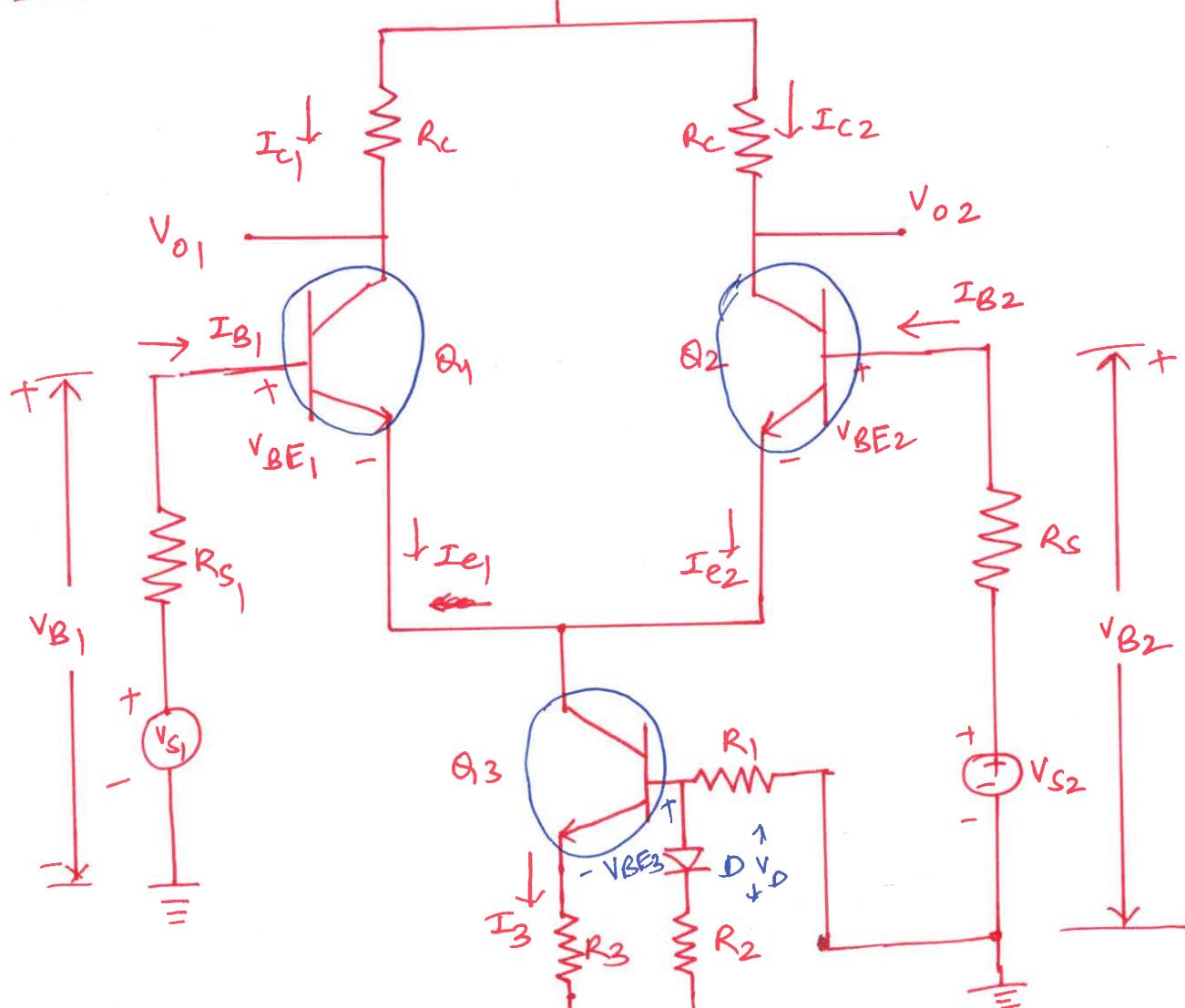


Fig: Schematic diagram of 741 IC .

## Differential Amplifier Supplied with a Constant current source:



Here  $R_E$  is replaced by a transistor circuit.

Applying KVL to the base circuit of  $Q_3$ , the transistor  $Q_3$  acts as an approximately constant current source, subject to the condition that the base current of  $Q_3$  is negligible.

Applying KVL to the base circuit of  $Q_3$ :

$$V_{BE3} + I_3 R_3 = V_D + (V_{EE} - V_D) \frac{R_2}{R_1 + R_2}$$

where  $V_D$  is the diode voltage.

Hence

$$I_3 R_3 = V_D - V_D \frac{R_2}{R_1+R_2} + V_{EE} \frac{R_2}{R_1+R_2} - V_{BE3}$$

$$= V_D \left[ \frac{R_1+R_2-R_2}{R_1+R_2} \right] + V_{EE} \frac{R_2}{R_1+R_2} - V_{BE3}$$

$$I_3 R_3 = V_D \left( \frac{R_1}{R_1+R_2} \right) + V_{EE} \frac{R_2}{R_1+R_2} - V_{BE3}$$

$$\therefore I_3 \approx I_0 = \frac{1}{R_3} \left[ V_D \left( \frac{R_1}{R_1+R_2} \right) + V_{EE} \frac{R_2}{R_1+R_2} - V_{BE3} \right]$$

If the circuit parameters are chosen so that

$$\frac{V_D R_1}{R_1+R_2} = V_{BE3}$$

then

$$I_0 = \frac{V_{EE} R_2}{R_3 (R_1+R_2)}$$

Since this current is independent of the signal

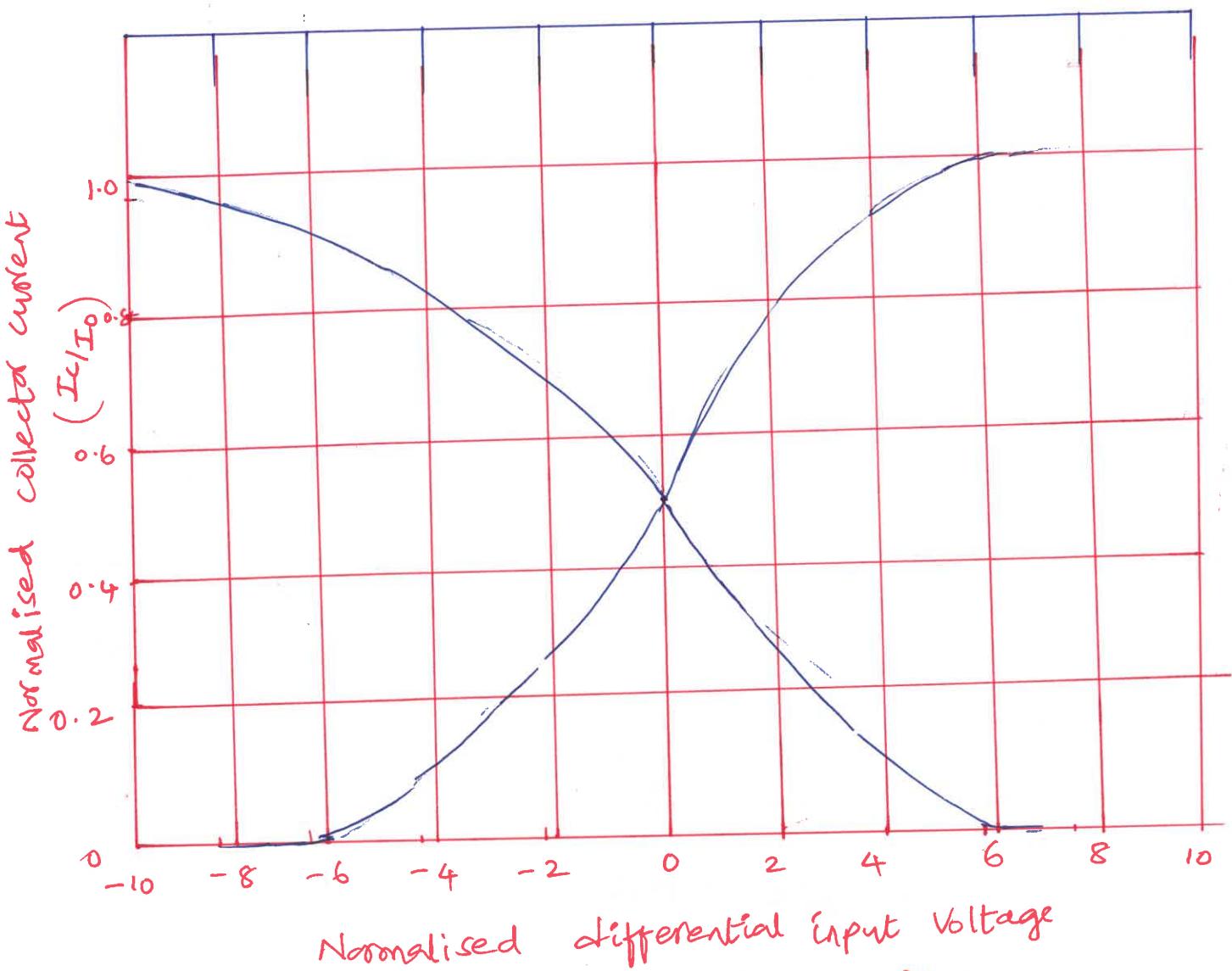
voltages  $V_{S1}$  and  $V_{S2}$ , then  $\Omega_3$  acts to supply the

DIFF AMP consisting of  $\Omega_1$  and  $\Omega_2$  with the constant

current  $I_0$ .

It acts as a constant current source.

# TRANSFER CHARACTERISTICS OF A DIFFERENTIAL AMPLIFIER:



Transfer characteristics for the normalised collector current  $I_c (I_c/I_o)$  and for the normalised differential

current  $(V_{B1} - V_{B2})/V_T$  is shown in figure.

Input  $(V_{B1} - V_{B2})/V_T$  is shown in figure.  
when  $V_{B1}$  is below the cut-off point of  $Q_1$ , all the

current  $I_o$  flows through  $Q_2$  (Assume  $V_{B2}$  is constant).

As  $V_{B1}$  carries  $Q_1$  above cut-off, the current in  $Q_1$  increases, while the current in  $Q_2$  decreases.

and the sum of the currents in the two transistors remains constant and equal to  $I_o$ .

The slope of the two curves defines the transconductance and it is clear that  $g_{md}$  starts from zero, reaches a maximum of  $\frac{I_o}{4V_T}$  when

$I_{C1} = I_{C2} = \frac{I_o}{2}$  and gain approaches to zero.

the value of  $g_{md}$  is proportional to  $I_o$ .

\* Transfer characteristics are linear in a small region around the operating point, where the input

Voltages approximately  $\pm V_T$  ( $\pm 26\text{mV}$  at room temp)

From the basic DIFF AMP.

$$I_{E1} + I_{E2} = -I_o$$

$$V_{B1} - V_{B2} = V_{BE1} - V_{BE2}$$

We know diode equation [ $I_E$  of each transistor is related to  $V_{BE}$  by the diode V-I characteristic]

$$\therefore I_E = I_s e^{\frac{V_{BE}}{V_T}}$$

$$\text{But } I_E = I_{E1} + I_{E2}$$

$$= I_{E1} + I_s e^{\frac{V_{BE2}}{V_T}}$$

$$= I_{E_1} + I_S e^{\frac{V_{BE1}}{V_T}} \times e^{-\frac{V_{BE1}}{V_T}} \times e^{\frac{V_{BE2}}{V_T}}$$

$$= I_{E_1} + I_S e^{\frac{V_{BE1}}{V_T}} \left[ e^{-\frac{[V_{BE1} - V_{BE2}]}{V_T}} \right]$$

$$I_E = I_{E_1} + I_{E_1} \left[ e^{-\frac{(V_{BE1} - V_{BE2})}{V_T}} \right]$$

$$I_E = I_{E_1} \left[ 1 + e^{-\frac{(V_{BE1} - V_{BE2})}{V_T}} \right]$$

$$\therefore I_E = -I_0 \quad \left[ \because I_{E_1} + I_{E_2} = -I_0 \right]$$

$$-I_0 = I_{E_1} \left[ 1 + e^{-\frac{(V_{BE1} - V_{BE2})}{V_T}} \right]$$

$$\therefore I_{E_1} = \frac{-I_0}{1 + e^{-\frac{(V_{BE1} - V_{BE2})}{V_T}}} \quad (\because I_C = +I_E)$$

$$\therefore I_C = \frac{-I_0}{1 + e^{-\frac{(V_{B1} - V_{B2})}{V_T}}}$$

Differentiate the above equation w.r.t  $\frac{V_{B1} - V_{B2}}{V_T}$

$$\frac{dI_C}{d(V_B - V_{B2})} = \frac{I_0}{V_T} \frac{1}{\left[ 1 + e^{-\frac{(V_{B1} - V_{B2})}{V_T}} \right]} \times e^{-\frac{(V_{B1} - V_{B2})}{V_T}}$$

If  $V_{B1} = V_{B2}$ , we get

$$\frac{dI_C}{d(V_{B1} - V_{B2})} = \frac{I_0}{4V_T} = g_{md}$$

$$\therefore g_{md} = \frac{I_0}{4V_T} \quad (\text{transconductance})$$

- \* This equation indicates that for the same value of  $I_0$ , the effective transconductance of the DIFF AMP is one-fourth that of a single transistor.

### \* Constant Current source circuits:

- \* An ideal current source provides a constant current regardless of the load connected to it.
- There are many applications in electronics for a circuit that provides a constant current with a very high impedance.

- \* Constant-current sources can be built using FET devices, BJT's and a combination of these components.

### BJT Constant Current Source:

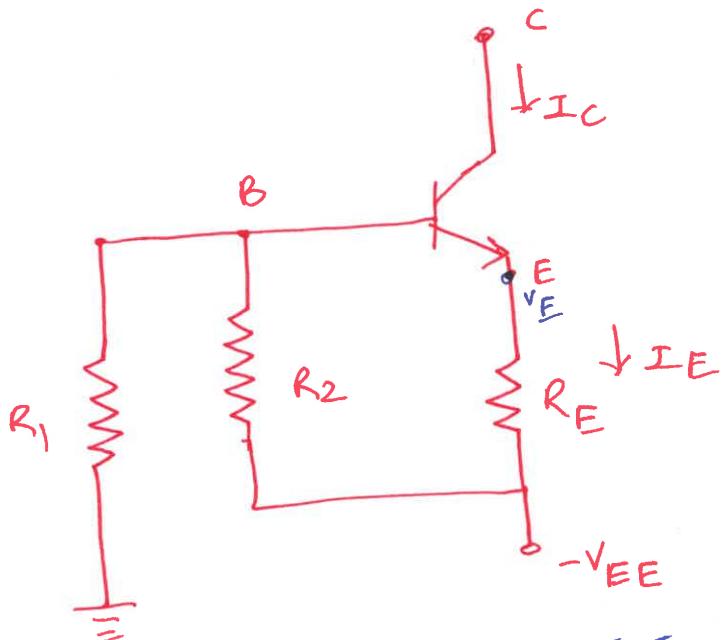


Fig:  
Discrete Constant Current source

Constant current  $I_C$  is given by the following equation.

$$I_C \approx I_E = \frac{V_E - (-V_{EE})}{R_E} = \frac{V_E + V_{EE}}{R_E}$$

We know  $V_{BE} = V_B - V_E$

$$\therefore V_E = V_B - V_{BE}$$

$$\therefore I_C = \frac{(V_B - V_{BE}) + V_{EE}}{R_E} = \frac{(V_B - 0.7 + V_{EE})}{R_E}$$

$\therefore$  Where  $V_B = \frac{R_1}{R_1 + R_2} \times (-V_{EE})$

[ Write KCL at  $V_B$

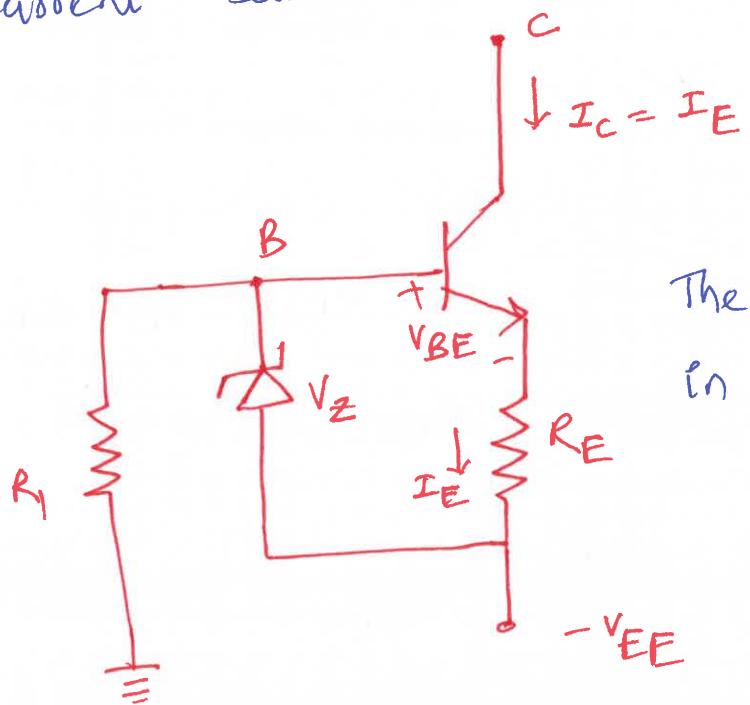
$$\frac{V_B - 0}{R_1} + \frac{V_B - (-V_{EE})}{R_2} = 0$$

$$V_B \left[ \frac{1}{R_1} + \frac{1}{R_2} \right] = -\frac{V_{EE}}{R_2}$$

$$\therefore V_B = \frac{R_1}{R_1 + R_2} \times (-V_{EE})$$

## (2) BJT / ZENER CONSTANT CURRENT SOURCE:

If Resistor  $R_2$  is replaced with a zener diode in the above Figure, an improved constant current source is obtained.



The zener diode results in a constant current  $I$ :

$$I = I_E = \frac{V_b - V_{BE}}{R_E}$$

$$I = \frac{V_z - V_{BE}}{R_E}$$

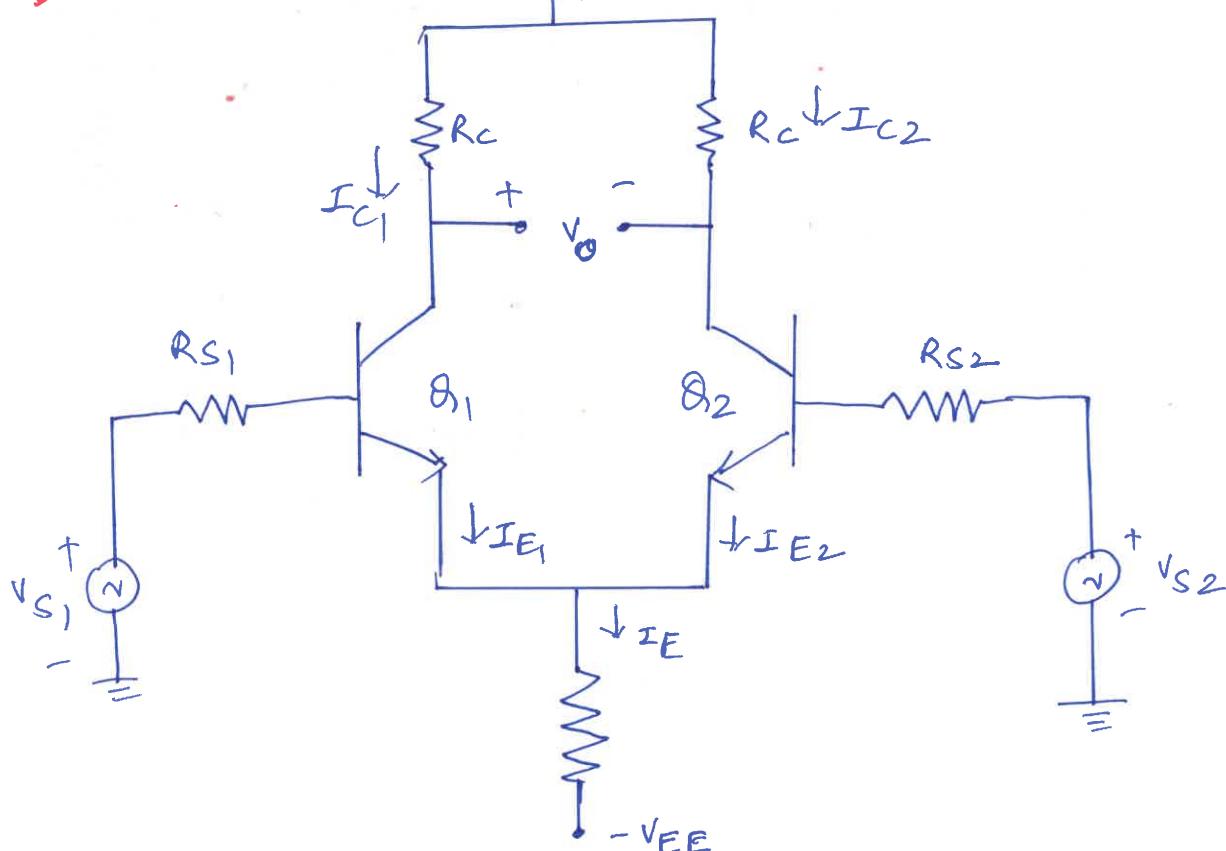
$$I = \frac{V_z - 0.7}{R_E}$$

$\therefore$  The constant current depends on zener diode Voltage, which remains quite constant and the emitter Resistor ( $R_E$ ).

$\therefore$  The Voltage Supply  $V_{EE}$  has no effect on the magnitude of current  $I$  delivered by the circuit.

## Alternate Method:

DIFF AMP Using Transistors:



$\theta_1$  and  $\theta_2$  are identical transistors. Assume  $\beta$

$\alpha$  ( $h_{fe}$ ) value of transistors are very high

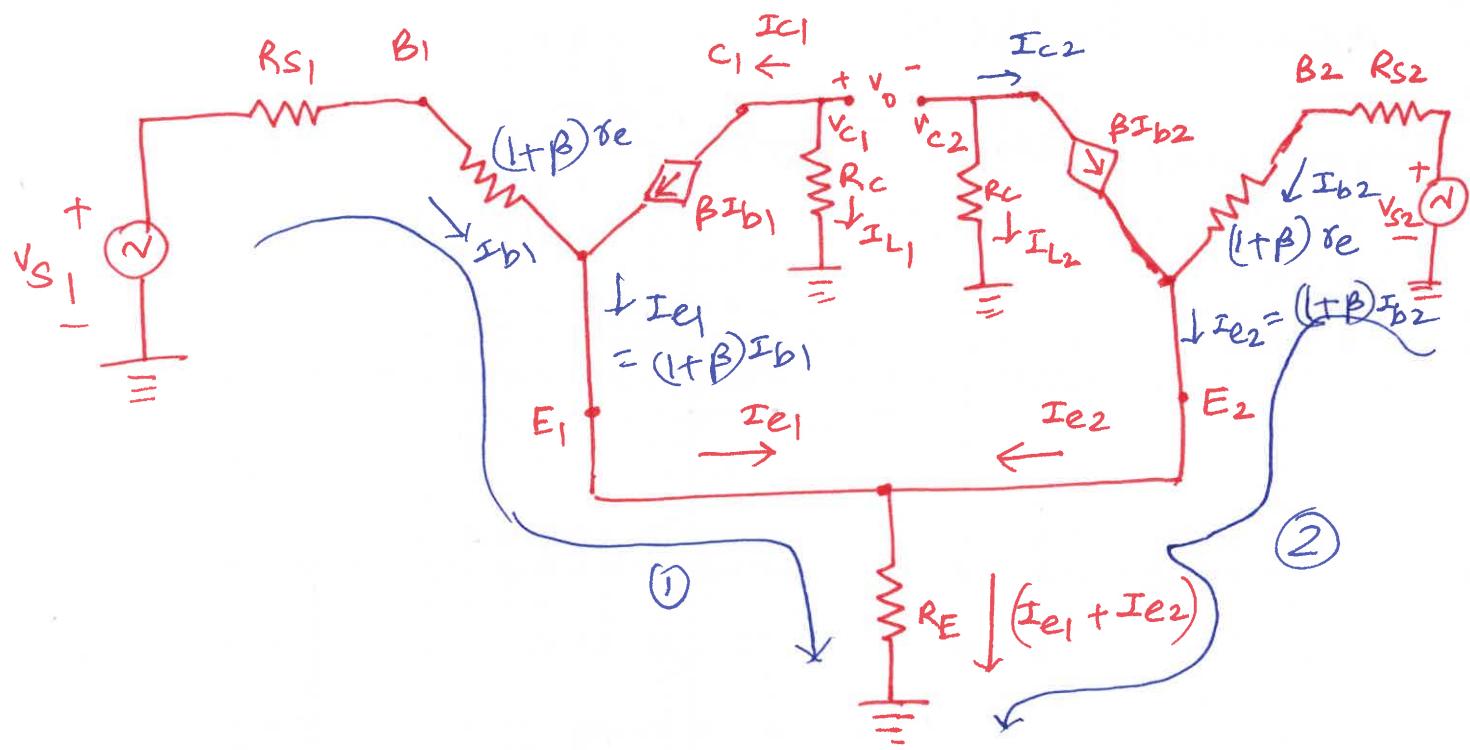
$$\therefore I_{B1} \approx I_{B2} \approx 0$$

$$I_{C1} \approx I_{C2} \approx I_{E1} \approx I_{E2}$$

$$\beta = \frac{I_C}{I_B}$$

$$I_B = \frac{I_C}{\beta}$$

$\approx 0$



$$V_O = V_{C1} - V_{C2}$$

$$= I_{L1} R_C - I_{L2} R_C$$

$$= -I_{C1} R_C + I_{C2} R_C$$

$$V_O = -R_C [ I_{C1} - I_{C2} ]$$

AS  $\beta$  is very high

$$I_{B1} \approx I_{B2} \approx 0$$

$$\therefore I_{C1} \approx I_{C2}$$

$$\& I_{E1} \approx I_{E2}$$

$$\therefore V_O \approx -R_C [ I_{E1} - I_{E2} ]$$

Apply KVL to the Loop (1)

$$-V_{S1} + I_{B1} R_S + (1 + \beta) r_e I_{B1} + (I_{E1} + I_{E2}) R_E = 0$$

$$I_{B1} R_S \approx 0$$

$$V_{S1} = I_{E1} r_e + (I_{E1} + I_{E2}) R_E$$

$$V_{S1} = I_{E1} [ r_e + R_E ] + I_{E2} R_E \rightarrow ①$$

Apply KVL to the loop (2)

$$-V_{S2} + I_{B2}R_{S2} + (1+\beta)r_e I_{B2} + (I_{e1} + I_{e2})R_E = 0$$

$$I_{B2}R_{S2} \approx 0 \quad (1+\beta)I_{B2} = I_{e2}$$

$$V_{S2} = I_{e2}r_e + (I_{e1} + I_{e2})R_E$$

$$V_{S2} = (I_{e1})R_E + I_{e2}(r_e + R_E) \rightarrow (2)$$

By solving (1) & (2)

$$(1) \times R_E \quad \text{and} \quad (2) \times (r_e + R_E)$$

$$V_{S1}R_E = I_{e1}R_E(r_e + R_E) + I_{e2}R_E^2 \rightarrow (3)$$

$$V_{S2}(r_e + R_E) = I_{e1}R_E(r_e + R_E) + I_{e2}(r_e + R_E)^2 \rightarrow (4)$$

Subtract:

$$V_{S1}R_E - V_{S2}(r_e + R_E) = I_{e2}R_E^2 - I_{e2}(r_e + R_E)^2$$

$$\therefore I_{e2} = \frac{V_{S1}R_E - V_{S2}(r_e + R_E)}{R_E^2 - (r_e + R_E)^2}$$

$$I_{e2} = \frac{V_{S2}(r_e + R_E) - V_{S1}R_E}{(r_e + R_E)^2 - R_E^2}$$

$$\textcircled{1} \times (r_e + R_E) \quad \& \quad \textcircled{2} \times R_E$$

$$V_{S_1}(r_e + R_E) = I_{e1} (r_e + R_E)^2 + I_{e2} R_E (r_e + R_E) \rightarrow (5)$$

$$\underline{V_{S_2} R_E = I_{e1} R_E^2 + I_{e2} R_E (r_e + R_E)} \rightarrow (6)$$

Subtract

$$V_{S_1}(r_e + R_E) - V_{S_2} R_E = I_{e1} (r_e + R_E)^2 - I_{e1} R_E^2$$

$$I_{e1} = \frac{V_{S_1}(r_e + R_E) - V_{S_2}(R_E)}{(r_e + R_E)^2 - R_E^2}$$

$$\therefore V_o = -R_C [I_{e1} - I_{e2}]$$

$$= -R_C \left[ \frac{V_{S_1}(r_e + R_E) - V_{S_2} R_E}{(r_e + R_E)^2 - R_E^2} - \left[ V_{S_2}(r_e + R_E) - V_{S_1} R_E \right] \right]$$

$$V_o = \frac{-R_C}{(r_e + R_E)^2 - R_E^2} \left[ \begin{array}{l} V_{S_1} r_e + V_{S_1} R_E \\ -V_{S_2} R_E - V_{S_2} r_e - V_{S_2} R_E \\ + V_{S_1} R_E \end{array} \right]$$

$$V_o = \frac{-R_C \left[ (V_{S_1} - V_{S_2})(r_e + 2R_E) \right]}{r_e^2 + R_E^2 + 2r_e R_E - R_E^2} - V_{S_2} [r_e + 2R_E]$$

$$V_o = \frac{R_C}{R_E} (V_1 - V_2) \rightarrow \text{So op voltage is amplification of differential input voltages.}$$

Differential amplifiers are of four types:

\* At the input side, we have

- \* Single input
- \* Dual input

\* At the output side, we have

- \* Balanced output
- \* Unbalanced output

Configurations:

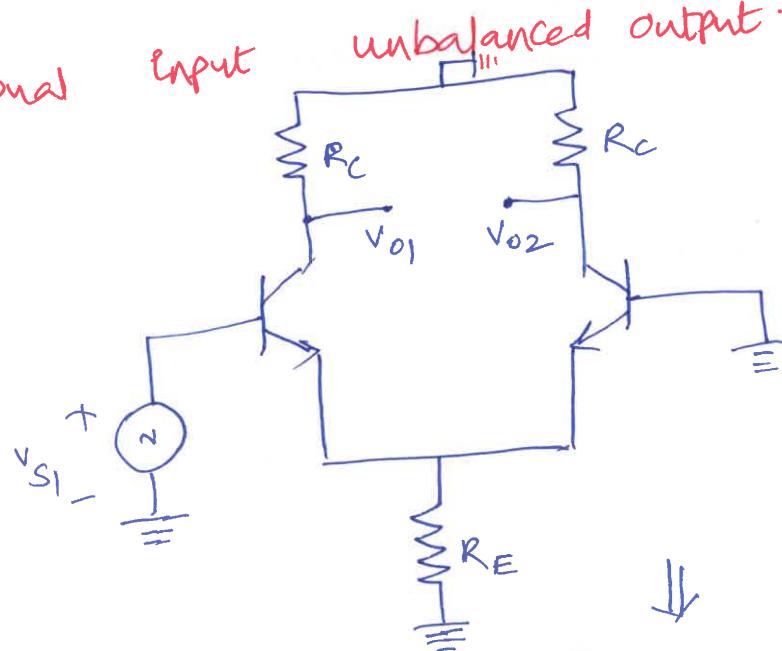
1. Single input balanced output

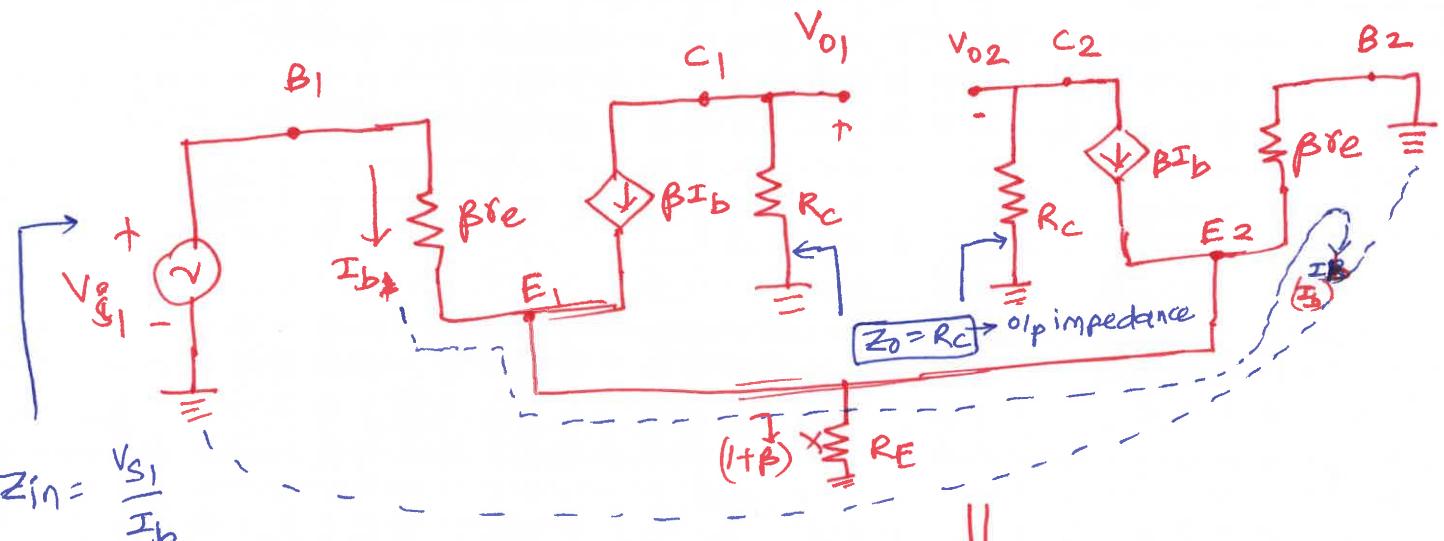
2. Single input unbalanced output

3. Dual input balanced output

4. Dual input unbalanced output.

AC Model:





$$V_{O1} = -\beta I_b R_C$$

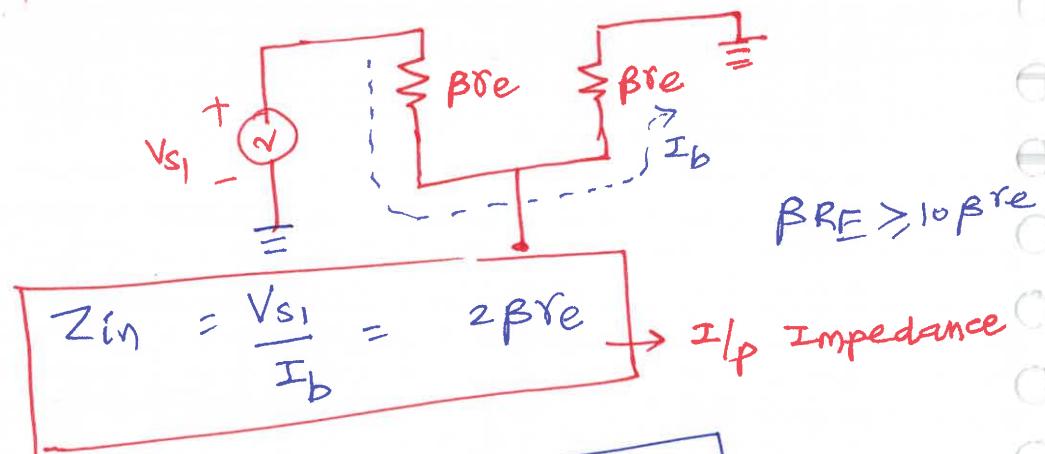
$$= -\beta \times \frac{V_{S1}}{2\beta r_e} \times R_C$$

$$A_{d1} = \frac{V_{O1}}{V_{S1}} = \frac{-R_C(\beta)}{2\beta r_e} = \frac{-R_C}{2r_e}$$

+ Unbalanced gain

$$A_{d2} = \frac{V_{O2}}{V_{S1}} = \frac{+R_C}{2r_e}$$

↓  
unbalanced gain



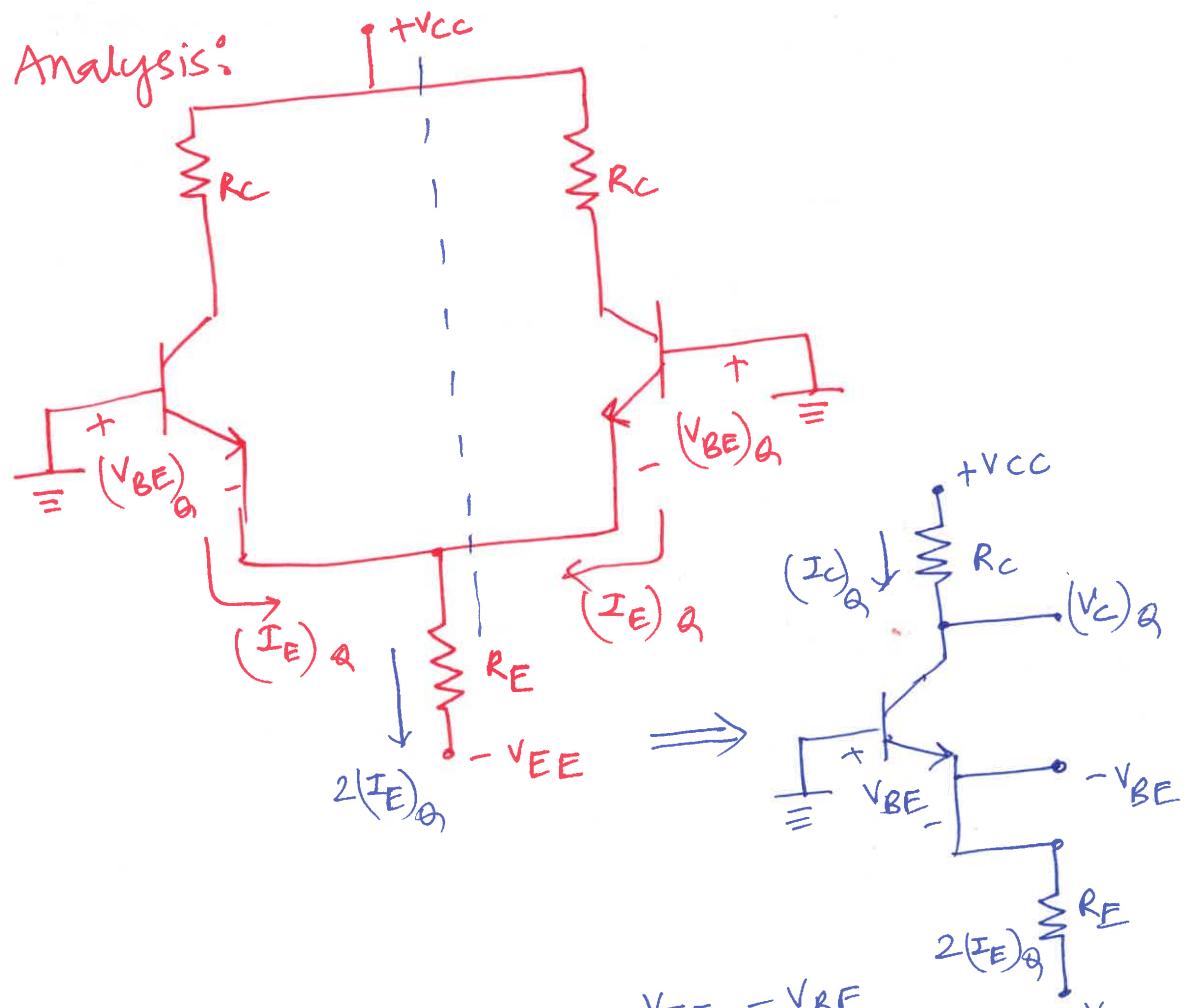
$$Z_{in} = \frac{V_{S1}}{I_b} = 2\beta r_e$$

→ I/p Impedance

$$\therefore Ad = \frac{A_{d2} - A_{d1}}{(or) A_{d1} - A_{d2}} = \pm \frac{R_C}{r_e}$$

Balanced gain.

DC Analysis:



$$(I_E)_Q = \frac{V_{EE} - V_{BE}}{2R_E}$$

$$(V_{CE})_Q = (V_C)_Q - (V_E)_Q$$

$$(V_{CE})_Q = V_{CC} - (I_C)_Q R_C + V_{BE}$$

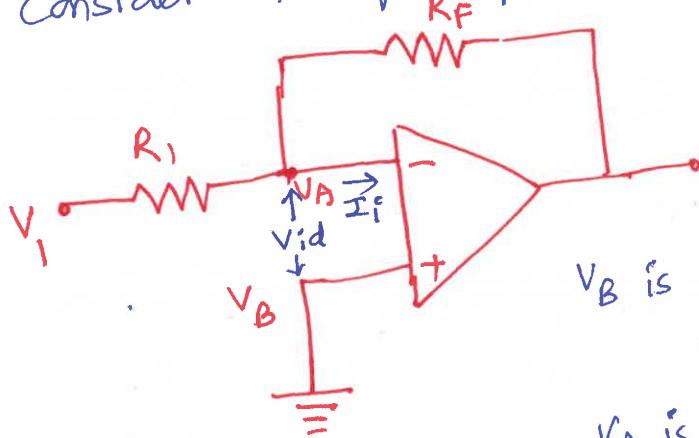
Drawbacks of Differential amp:

1. It is having unstable gain
2. It is having low input impedance.

## VIRTUAL GROUND (OR) VIRTUAL SHORT CONCEPT:

This is an important concept for an op-amp, as it plays a vital role in deriving the expressions for output voltage  $V_o$ .

Consider the op-amp circuit shown in figure.



$V_B$  is a potential at Non-inverting terminal.  
 $V_A$  is a potential at Inverting terminal.

$$V_{id} = V_B - V_A$$

According ideal characteristics of op-amp

Input resistance  $R_i$  is infinite ( $\infty$ ), therefore the current entering into op-amp  $I_i$  will be zero.

That means differential voltage  $V_{id}$  will be zero

$$\text{i.e. } 0 = V_B - V_A$$

$$\therefore \boxed{V_B = V_A}$$

$$\begin{aligned} I_i &= \frac{V_{id}}{R_i} \\ &= \frac{V_{id}}{\infty} \\ &= 0 \end{aligned}$$

The node voltage  $V_B$  at +ve terminal is same as

the node voltage  $V_A$  at -ve terminal. This concept is called as Virtual ground concept.

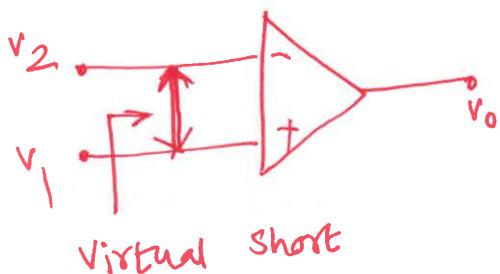
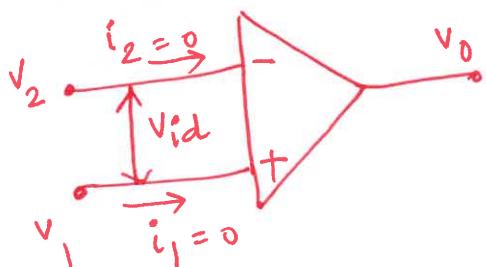
It can be seen that

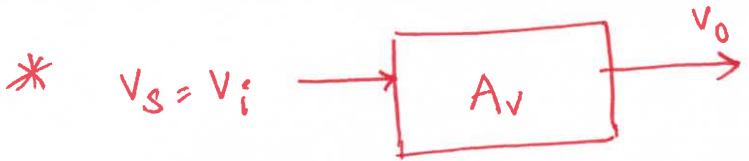
- (i) An ideal op-amp draws no current at both the input terminals i.e  $i_1 = i_2 = 0$ . Because of infinite input impedance, any signal source can drive it and there is no loading on the preceding driver stage.
- (ii) Since gain is  $\infty$  (infinite), the voltage between the inverting and non-inverting terminals i.e the differential input voltage  $V_{id} = V_1 - V_2$  is essentially zero for finite output voltage.
- (iii) The op voltage  $V_o$  is independent of the current drawn from the output as  $R_o = 0$ . The op can drive an infinite number of other devices.

Remember

\*\*

1. The current drawn by either of the input terminals (Non-inverting and Inverting) is negligible.
2. The differential input voltage ( $V_{id}$ ) between non-inverting and inverting input terminals is essentially zero.

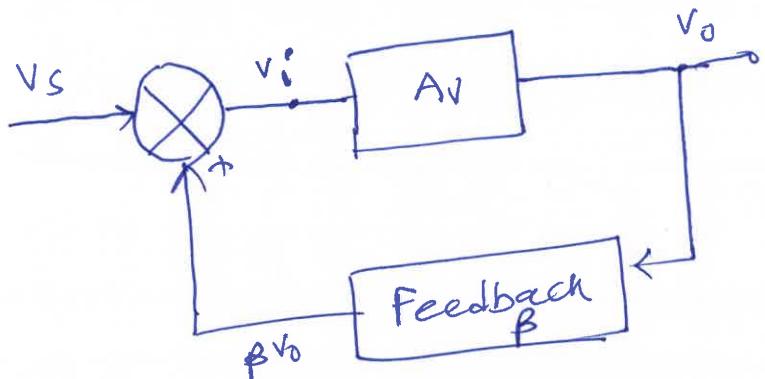




$A_{OL} = A_v$   
= open Loop gain

$$A_{OL} = A_v = \frac{V_o}{V_i} = \frac{V_o}{V_S}; V_S = V_i$$

+ve Feedback



$$V_i = V_S + \beta V_o$$

$$\begin{aligned} V_o &= A_v \times V_i \\ &= A_v [V_S + \beta V_o] \end{aligned}$$

$$V_o [1 - \beta A_v] = A_v V_S$$

$$A_{CL} = \frac{V_o}{V_S} = \frac{A_v}{1 - \beta A_v} = \frac{A_v}{1 - \beta} > A_v$$

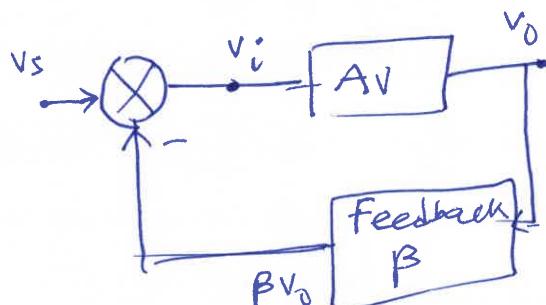
Closed Loop gain for +ve Feedback

\* +ve feedback is used in oscillators

op-amp with +ve Feedback

$$|A_{CL}| \gg |A_{OL}|$$

-ve Feedback



$$V_i = V_S - \beta V_o$$

$$V_o = A_v \times V_i$$

$$V_o = A_v [V_S - \beta V_o]$$

$$V_o [1 + A_v \beta] = A_v V_S$$

$$A_{CL} = \frac{V_o}{V_S} = \frac{A_v}{1 + A_v \beta} < A_v$$

Closed Loop gain for -ve Feedback

-ve Feedback is used  
in amplifiers

$$|A_{CL}| \ll |A_{OL}|$$

We can assume

$$A_{OL} = A_v \rightarrow \infty$$

∴ Virtual Ground

process is valid.

## Modes of operation

(i) Inverting Mode

$$\text{phase shift} = 180^\circ \quad (\phi)$$

(2) Non-Inverting mode

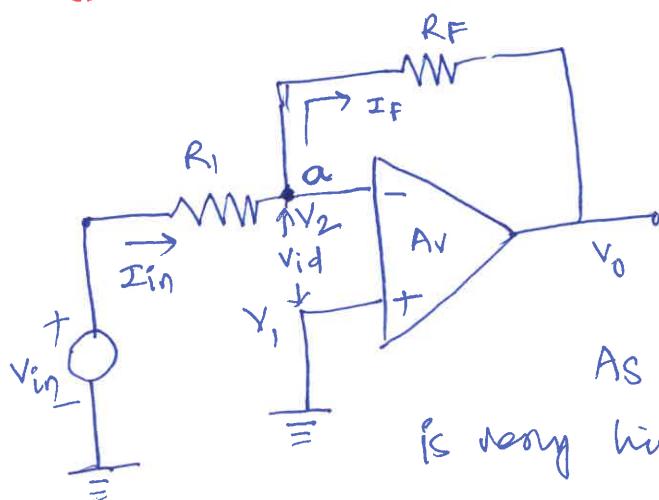
$$\text{phase shift } (\phi) = 0^\circ$$

(3) Differential Mode

$$V_o \propto (V_1 - V_2)$$

Imp\*

(1) INVERTING AMPLIFIER (OR) INVERTING OP-AMP:



As the input resistance of op-amp is very high, the current entering into the op-amp terminals is very low & neglected.

Apply KCL at node (a)

$$I_{in} = IF$$

$$\frac{V_{in} - V_2}{R_1} = \frac{V_2 - V_0}{R_F} \rightarrow (1)$$

$$\text{We know } V_{id} = V_1 - V_2 = 0$$

$$\text{Here } V_1 = 0 \therefore V_2 = 0$$

[According to  
Virtual Ground  
concept]

Substitute  $V_2$  in eq(1)

$$\frac{V_{in} - 0}{R_1} = \frac{0 - V_o}{R_F} \Rightarrow \frac{V_o}{V_{in}} = -\frac{R_F}{R_1}$$

$$\therefore V_o = -\frac{R_F}{R_1} V_{in} \Rightarrow$$

-ve sign indicates  $180^\circ$  of phase shift between  $V_o$  and  $V_{in}$ .

.. Because of this phase inversion, this configuration is commonly called as Inverting amplifier.

$$A_v = \frac{V_o}{V_{in}} = -\frac{R_F}{R_1}$$

(or) Method -(2):

Apply KCL at node  $V_2$ .

$$\frac{V_2 - V_{in}}{R_1} + \frac{V_2 - V_o}{R_F} = 0$$

According to Virtual Short (Ground) Concept  
 $V_{id} = V_1 - V_2 = 0$

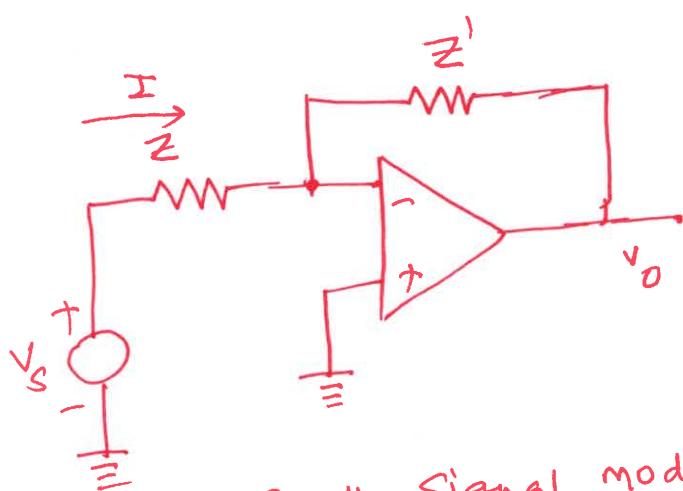
$$[V_1 = V_2] = 0$$

$$\therefore \frac{V_o}{V_{in}} = -\frac{R_F}{R_1} \Rightarrow V_o = -\frac{R_F}{R_1} V_{in}$$

$$A_v = -\frac{R_F}{R_1}$$

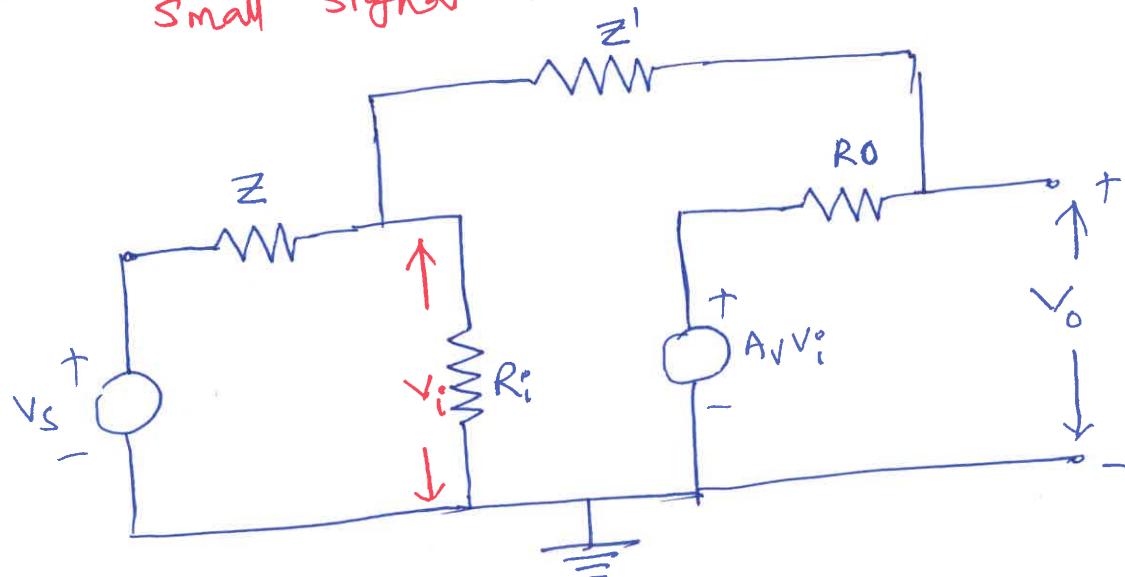
## practical Inverting Amplifier:

$A_v \neq \infty$ ,  $R_i \neq \infty$  and  $R_o \neq 0$

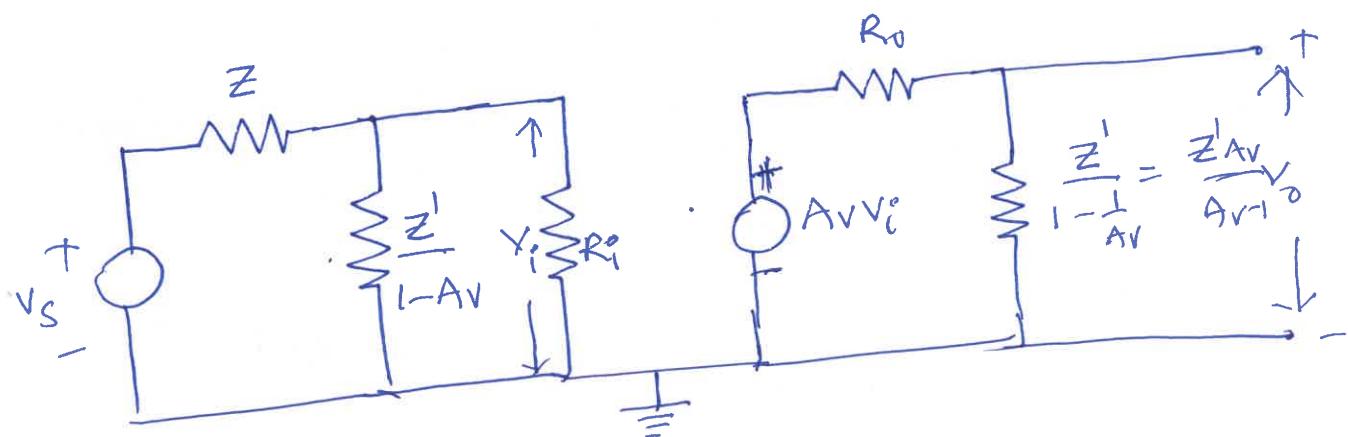


Voltage shunt  
FB amp

Small Signal model ( $\infty$ ) Low - freq model of op-amp



According to Miller's theorem



$\therefore A_{vf} = \text{Voltage gain with Feedback}$

$$A_{vf} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \times \frac{V_i}{V_s} = A_v \times \frac{V_i}{V_s}$$

According to Voltage division rule

$$V_i^o = \frac{V_s \times Y}{Y + (1-Av)Y' + Y_i} \quad Y' = \frac{1}{Z'} \quad Y_i = \frac{1}{R_i}$$

$$Y = \frac{1}{Z}$$

$$V_i^o = \frac{V_s \times Y}{-AvY' + (Y + Y' + Y_i)}$$

$$V_i^o = \frac{-V_s Y}{AvY' - [Y + Y' + Y_i]}$$

$$\frac{V_i^o}{V_s} = \frac{-Y}{AvY' - [Y + Y' + Y_i]}$$

$$Av_f = \frac{V_o}{V_s} = Av \times \frac{V_i^o}{V_s}$$

$$Av_f = \frac{Av [-Y]}{Av Y' - [Y + Y' + Y_i]}$$

$$Av_f = \frac{-Y}{Y' - \frac{1}{Av} [Y + Y' + Y_i]}$$

(OR) write KCL equation at node  $V_i^o$

$$\frac{V_i^o - V_s}{Z} + \frac{V_i^o}{R_i} + \frac{V_i^o}{\left( \frac{Z'}{1-Av} \right)} = 0$$

$$\frac{V_i - V_s}{Z} + \frac{V_i}{R_i} + \frac{V_i (1 - A_v)}{Z'} = 0$$

$$V_i \left[ \frac{1}{Z} + \frac{1}{R_i} + \frac{1}{Z'} \right] - \frac{A_v V_i}{Z'} = \frac{V_s}{Z}$$

$$V_i [Y + Y_i + Y'] - A_v \times V_i Y' = V_s Y$$

$$V_i [Y + Y_i + Y'] - A_v \times Y' = V_s Y$$

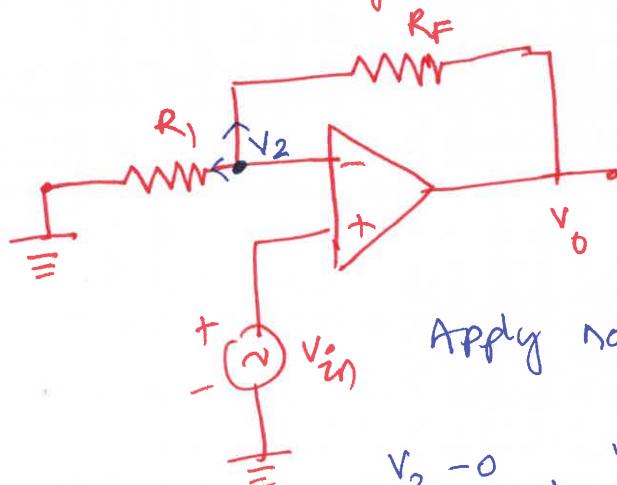
$$\begin{aligned} \frac{V_i}{V_s} &= \frac{Y}{[Y + Y' + Y_i] - A_v \times Y'} \\ &= \frac{-Y}{A_v Y' - (Y + Y' + Y_i)} \end{aligned}$$

$$\begin{aligned} A_{vF} &= A_v \times \frac{V_i}{V_s} \\ &= \frac{A_v \times (-Y)}{A_v Y' - (Y + Y' + Y_i)} \end{aligned}$$

$$A_{vF} = \frac{-Y}{Y' - \frac{1}{A_v} [Y + Y' + Y_i]}$$

If  $A_v \rightarrow \infty$   $A_{vF} = \frac{-Y}{Y'} = \frac{-\frac{1}{Z}}{\frac{1}{Z'}} = -\frac{Z}{Z'}_g$

## (2) Non-Inverting Amplifier



Apply node equation at  $V_2$

$$\frac{V_2 - 0}{R_1} + \frac{V_2 - V_o}{R_F} = 0 \rightarrow (1)$$

According to Virtual Short Concept,

Voltage at Non Inverting Terminal = Voltage at  
Investing terminal

$$V_2 = V_1 \quad V_2 = V_{in}$$

Substitute  $V_2 = V_{in}$  in eq (1)

$$\frac{V_{in}}{R_1} + \frac{V_{in} - V_o}{R_F} = 0$$

$$V_{in} \left[ \frac{1}{R_1} + \frac{1}{R_F} \right] = \frac{V_o}{R_F}$$

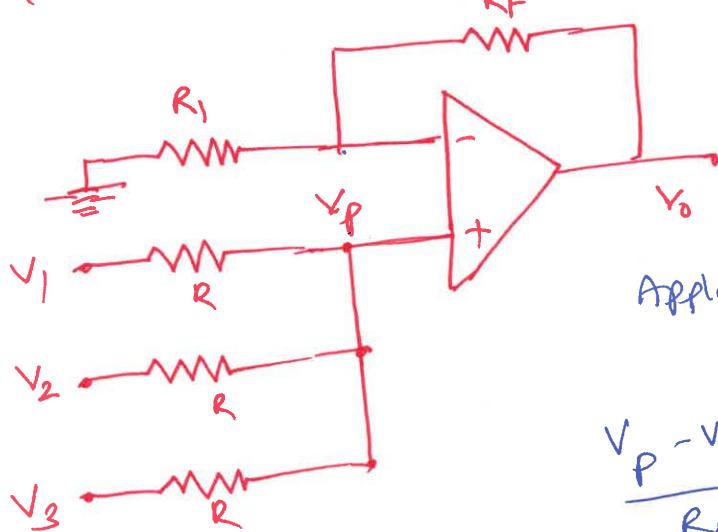
$$V_o = \left( 1 + \frac{R_F}{R_1} \right) V_{in}$$

+ve sign indicates  $0^\circ$  phase shift between  
 $V_o$  and  $V_{in}$

$$\text{Voltage Gain, } A_V = \frac{V_o}{V_{in}} = 1 + \frac{R_F}{R_1}$$

2  
(a)

## Non-Inverting Summer:



Apply KCL at Non Inverting terminal

$$\frac{v_p - v_1}{R} + \frac{v_p - v_2}{R} + \frac{v_p - v_3}{R} = 0$$

$$v_p = \frac{v_1 + v_2 + v_3}{3}$$

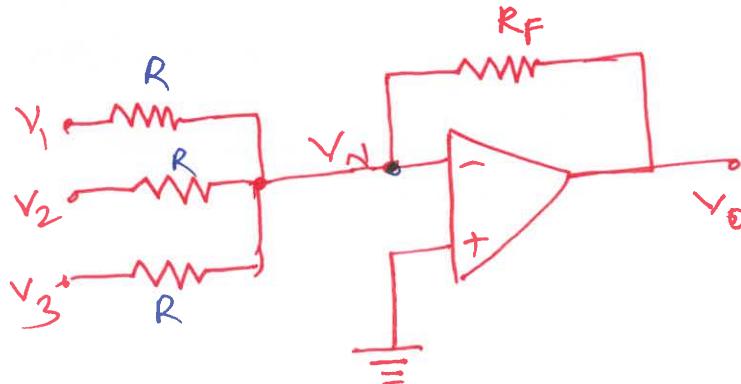
Now  $\frac{v_o}{v_p} = \left(1 + \frac{R_F}{R_1}\right)$

$$\therefore v_o = \left(1 + \frac{R_F}{R_1}\right) \left[ \frac{v_1 + v_2 + v_3}{3} \right] [\phi = 0^\circ]$$

If  $R_F = 2R_1$

$$\therefore \boxed{v_o = v_1 + v_2 + v_3}$$

### (3) Inverting summing Amplifier: (ADDER)



Apply KCL at node vN

$$\frac{v_N - v_1}{R} + \frac{v_N - v_2}{R} + \frac{v_N - v_3}{R} + \frac{v_N - v_o}{R_F} = 0$$

According to virtual short concept,  
 Voltage at Non inverting terminal = Voltage at  
 Inverting terminal

$$\therefore V_N = 0$$

$$\frac{0 - V_1}{R} + \frac{0 - V_2}{R} + \frac{0 - V_3}{R} + \frac{0 - V_o}{R} = 0$$

$$\frac{V_o}{R_F} = -\frac{1}{R} [V_1 + V_2 + V_3]$$

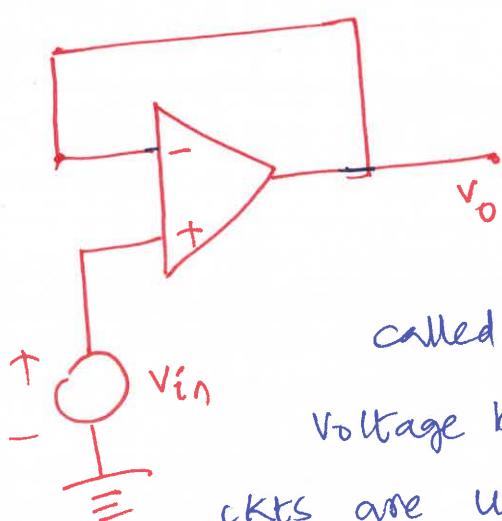
$$V_o = -\frac{R_F}{R} [V_1 + V_2 + V_3]$$

when  $R_F = R$

$$V_o = -[V_1 + V_2 + V_3]$$

-ve sign indicates  $180^\circ$  phase shift.

#### 4. Voltage Follower



As per virtual short concept:

$[V_o = V_{in}]$ , it is called voltage follower ckt (or) voltage buffer ckt. These buffer ckt's are used in impedance matching circuits.

(6R)

In Non inverting amplifier, when the Resistor  $R_F$  is set equal to zero (or)  $R_1$  is made  $\infty$  (by keeping it open circuited)

$$\therefore V_o = \left(1 + \frac{R_F}{R_1}\right) V_{in}$$

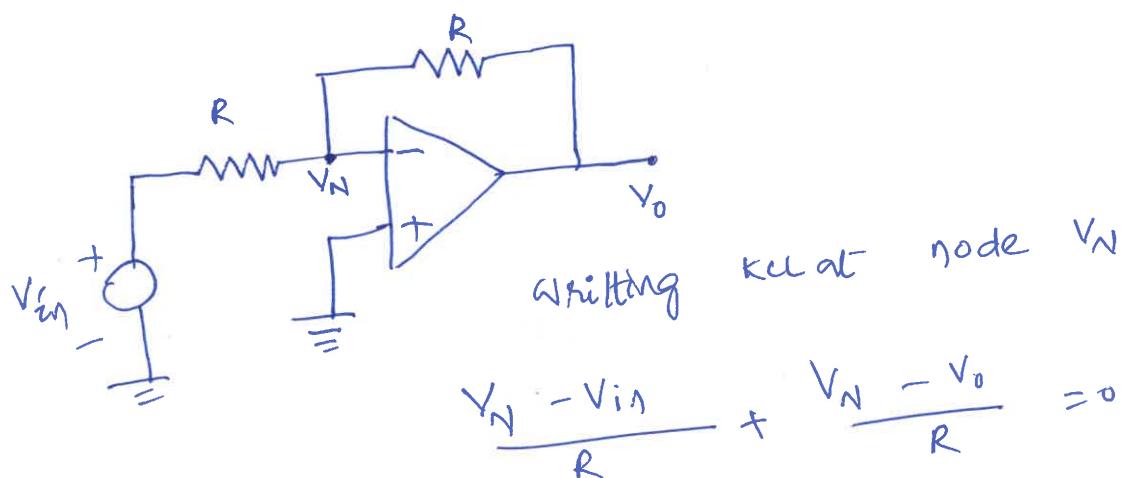
$$\begin{aligned} \frac{R_F}{R_1} &= 0 \text{ i.e.} \\ R_F &= 0 \Omega \\ R_1 &= \infty \Omega \end{aligned}$$

$$\boxed{\therefore V_o = V_{in}}$$

i.e. the output voltage of the op-amp exactly tracks the input voltage both in sign and magnitude.

### 5. phase shifter:

In an Inverting amp if  $R_1 = R_F = R$  then



According to virtual short concept

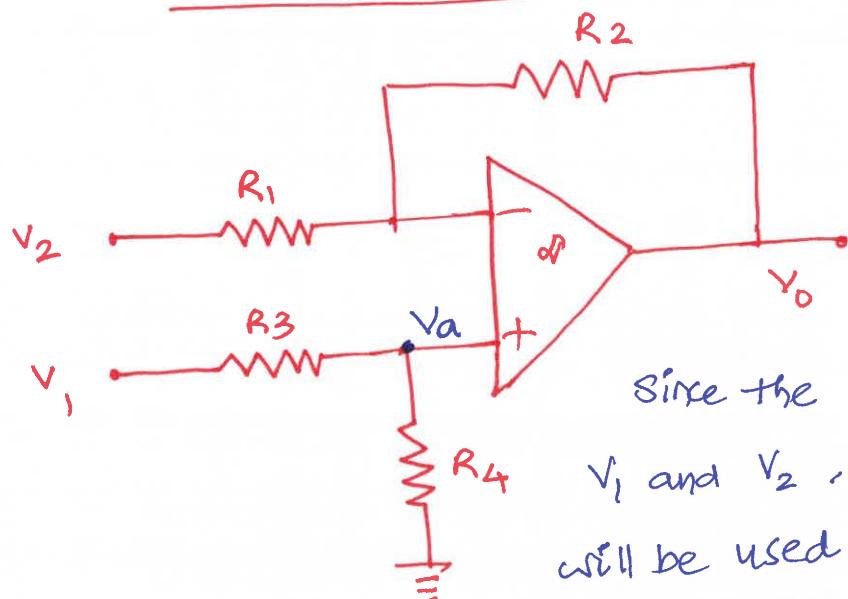
$$V_N = 0$$

$$\frac{V_o}{V_{in}} = -\frac{R}{R} = -1$$

$$\boxed{A_v = -1}$$

Negative sign indicates that the  $180^\circ$  phase shift between  $v_o$  and  $v_{in}$ , but magnitude is same

## 6. Differential DC amplifiers:



Since the circuit has two inputs  $v_1$  and  $v_2$ , Super position theorem will be used for determination of voltage gain of the amplifier.

\* Applying super position theorem.

$$v_o = v_{o1} + v_{o2} \quad [\text{bcz of two voltage sources}]$$

when  $v_1 = 0$ ; it behaves like a inverting mode.

$$\therefore v_{o1} = -\frac{R_2}{R_1} v_2 \quad \rightarrow (1)$$

when  $v_2 = 0$ ; it behaves like a Non-inverting mode.

$$v_{o2} = \left(1 + \frac{R_2}{R_1}\right) \cdot v_a$$

$$v_{o2} = \left(1 + \frac{R_2}{R_1}\right) \times \frac{R_4}{R_3 + R_4} \times v_1$$

$$v_a = \frac{R_4}{R_3 + R_4} \times v_1$$

[Voltage divider principle]

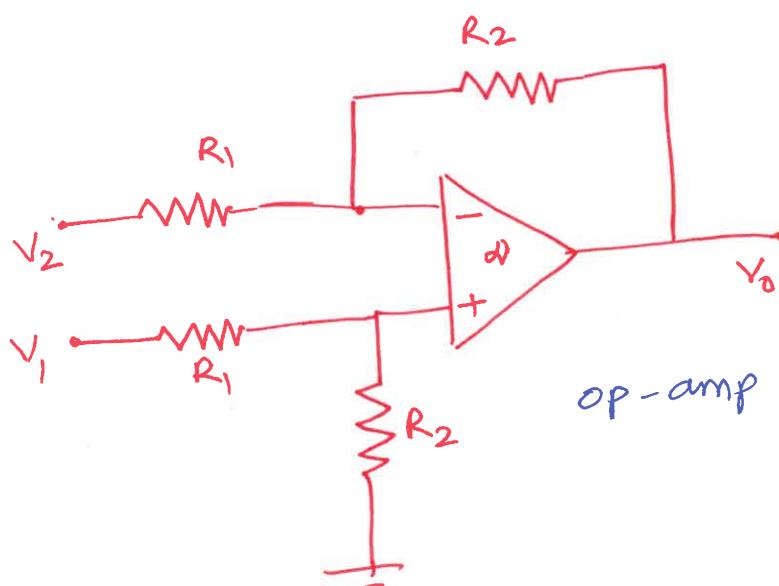
$$\therefore V_o = V_{o1} + V_{o2}$$

$$= -\frac{R_2}{R_1} V_2 + \left(1 + \frac{R_2}{R_1}\right) \times \left(\frac{R_4}{R_3 + R_4}\right) V_1$$

Case (i):

If suppose the differential amplifier with  $R_3 = R_1$

$$\text{and } R_4 = R_2 \quad \left[ \frac{R_2}{R_1} = \frac{R_4}{R_3} \right]$$



op-amp Differential Amplifier.

$$\therefore V_o = -\frac{R_2}{R_1} V_2 + \left(1 + \frac{R_2}{R_1}\right) \times \left(\frac{R_2}{R_1 + R_2}\right) V_1$$

$$= -\frac{R_2}{R_1} V_2 + \left(\frac{R_2 + R_1}{R_1}\right) \times \left(\frac{R_2}{R_1 + R_2}\right) V_1$$

$$\boxed{V_o = \frac{R_2}{R_1} [V_1 - V_2]}$$

\*

Balanced

$$\boxed{V_o = \frac{R_2}{R_1} (V_1 - V_2)}$$

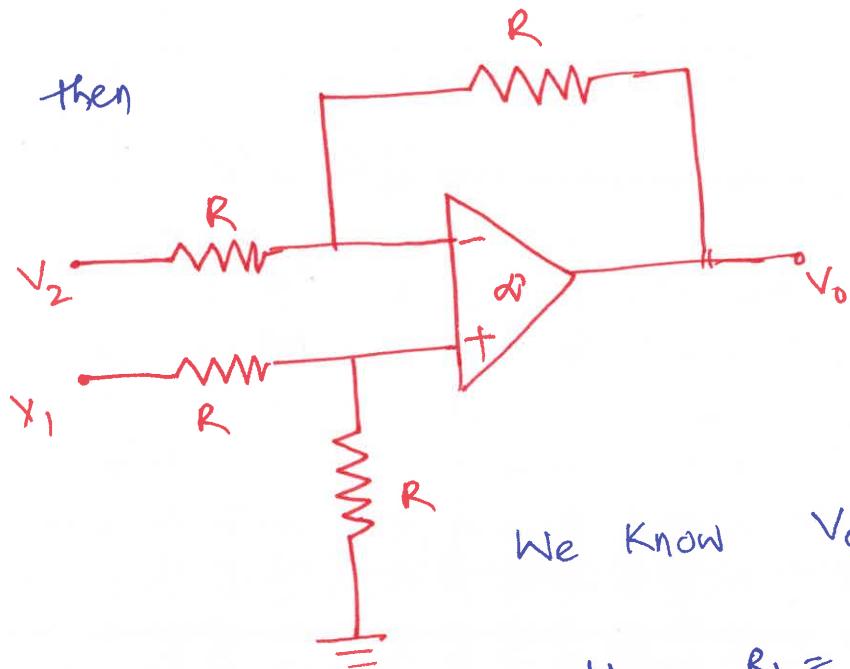
DIFF AMP

\*

case (ii):

Subtractor:

If  $R_1 = R_2 = R_3 = R_4 = R$  in op-amp DIFF AMP



We Know  $V_o = \frac{R_2}{R_1} (V_1 - V_2)$

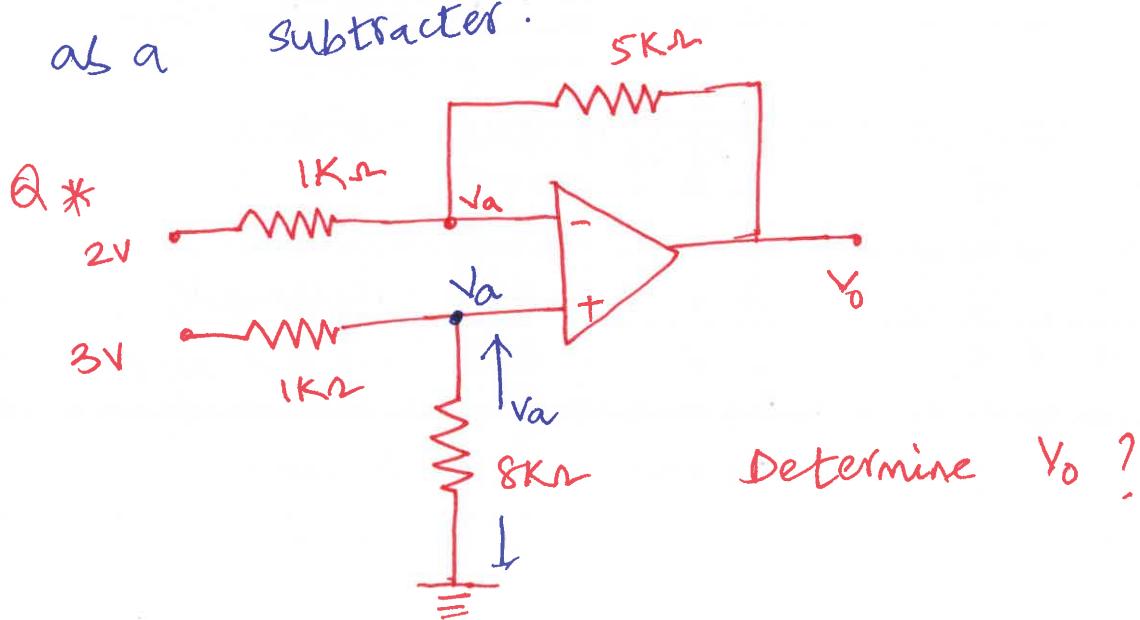
Here  $R_1 = R_2 = R$

$$V_o = \frac{R}{R} (V_1 - V_2)$$

$$V_o = V_1 - V_2$$

which is the practical application of op-amp

as a Subtractor.



### Method 1:

Based on superposition theorem  $V_o = V_{o1} + V_{o2}$

$$V_o = -\cancel{\frac{5K}{1K}} \times 2v + \left(1 + \frac{5K}{1K}\right) V_a$$

$$\text{Here } V_a = \frac{\frac{8K}{8K+1K} \times 3}{}$$

$$V_o = -\frac{5K \times 2}{1K} + \left(1 + \frac{5K}{1K}\right) \times \left(\frac{8K}{8K+1K}\right) \times 3$$

$$= -5 \times 2 + \frac{2}{\cancel{5} \times \cancel{9}} \times 3$$

$$= -10 + 16 = 16 - 10 = 6V$$

$$\boxed{V_o = 6V}$$

### Method - 2:

According virtual short concept, Voltage at non inverting terminal = Voltage at Inverting terminal

\* Apply KCL at node  $V_a$  [ inverting side]

$$\frac{V_a - 2}{1K} + \frac{V_a - V_o}{5K} = 0$$

$$V_a \left[ \frac{1}{1K} + \frac{1}{5K} \right] - \frac{2}{1K} = \frac{V_o}{5K} \quad \rightarrow (1)$$

writing KCL at node  $V_a$  (Non-inverting side)

$$\frac{V_a - 3}{1K} + \frac{V_a - 0}{8K} = 0 \quad V_a \left[ \frac{1}{1K} + \frac{1}{8K} \right] = \frac{3}{1K}$$

$$V_a = \left( \frac{8K}{8K+1K} \right) \times 3$$

$$V_a = \frac{8}{9} \times 3 = \frac{8}{3} \text{ Volts}$$

→ (2)

Substitute eq(2) in eq(1)

$$\frac{8}{3} \left[ \frac{6K}{5K \times 1K} \right] - \frac{2}{1K} = \frac{V_o}{5K}$$

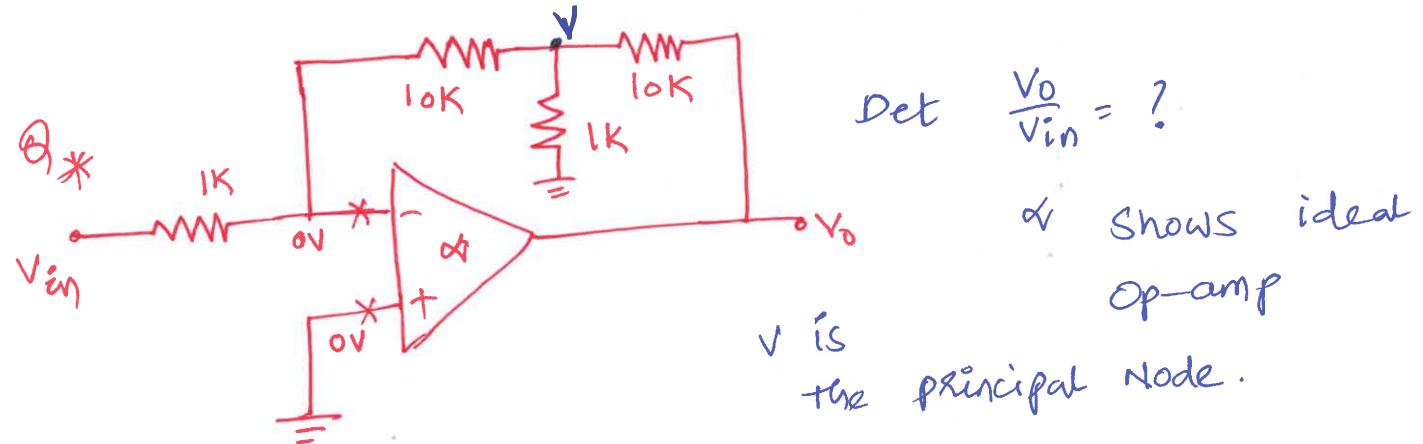
$$\frac{8}{3} \left[ \frac{6K}{5K \times 1K} \right] - \frac{2}{1K} = \frac{V_o}{5K}$$

$$\frac{48}{15K} - \frac{2}{1K} = \frac{V_o}{5K}$$



$$\frac{48 - 30}{15K_3} = \frac{V_o}{5K}$$

$$V_o = \frac{18}{3} = 6V$$



\* No current is accepted by ideal Op-amp.

Writing eq at inverting terminal

$$\frac{0 - V_{in}}{1k} + \frac{0 - V}{10k} = 0$$

$$V = -10V_{in} \rightarrow (1)$$

Write the nodal equation at Centre

$$\frac{V - 0}{10 \times 10^3} + \frac{V}{1 \times 10^3} + \frac{V - V_o}{10 \times 10^3} = 0$$

$$V + 10V + V = (V_{out}) \text{ or } V_o$$

$$V_o = 12V \rightarrow (2)$$

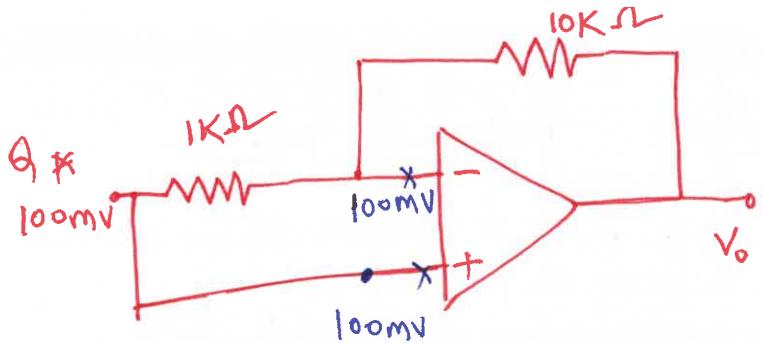
Substitute eq(1) in eq (2)

$$V_o = 12 \times -10V_{in}$$

$$= -120V_{in}$$

$$\frac{V_o}{V_{in}} = -120$$

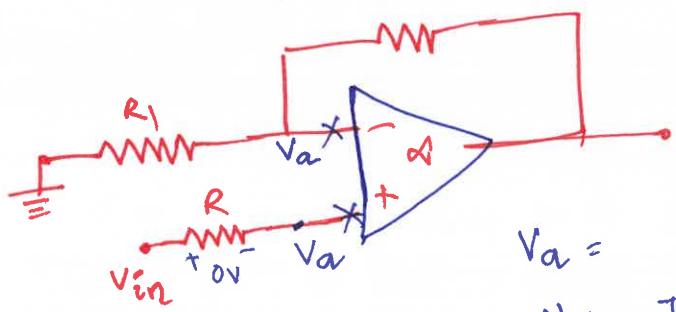
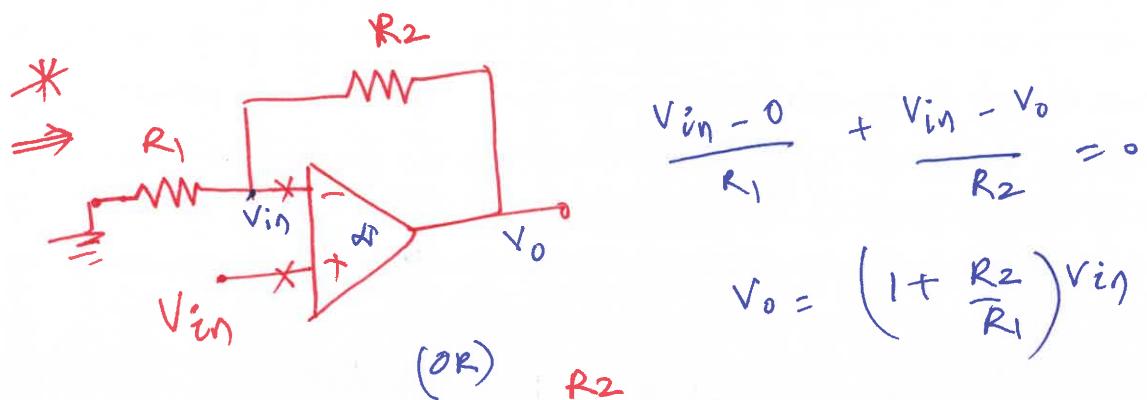
Voltage gain.



KCL equation

$$\frac{100\text{mV} - 100\text{mV}}{1\text{K}} + \frac{100\text{mV} - \cancel{100\text{mV}}}{\cancel{10}\text{K}} = 0$$

$$V_o = 100\text{mV}$$



$V_a$  = Actual voltage at the Non-Inverting terminal

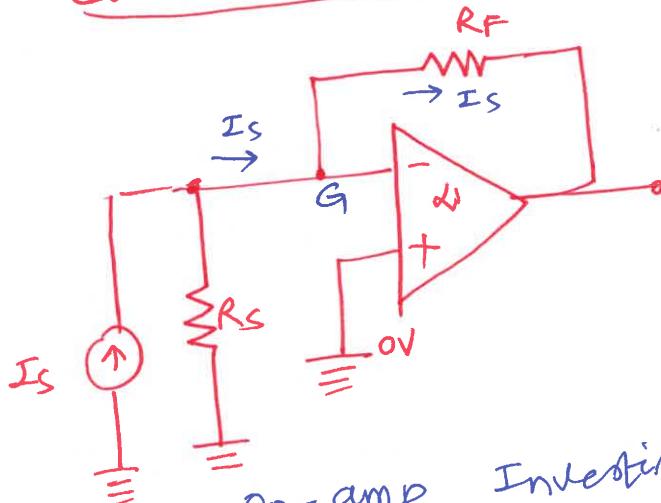
$$V_o = \left(1 + \frac{R_2}{R_1}\right) V_a$$

$$\Rightarrow V_a = V_{in} \quad (\text{Here current is not accepted})$$

$$\therefore V_o = \left(1 + \frac{R_2}{R_1}\right) V_{in}$$

## CONVERTERS:

### (i) Current to Voltage Converter:



Op-amp Inverting amp can also be used  
as current to voltage converter.

Due to virtual short (ground) at the point G,  
the current in  $R_S$  is zero. Hence the entire current  
 $I_S$  of the current source flows through the resistor  
 $R_F$  and develops the output voltage

$$\frac{0 - V_O}{R_F} = I_S$$

$$\therefore V_O = -I_S R_F \quad [V_O \text{ is independent of Load}]$$

$I_S$ : Input current

$V_O$ : Output Voltage

Hence it is  
converter]

$$V_O = -I_S R_F$$

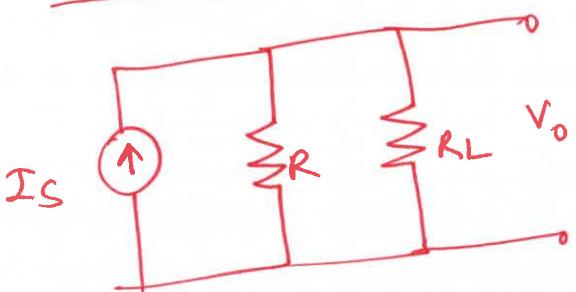
$\therefore V_O \propto (I_S)$  : the op-amp voltage is proportional to the input current. Hence an input current

is converted into an output voltage.

Eg: photo cells and photomultiplier tubes gives an output current which is independent of its load may be connected to the input of a

## Current to Voltage converter.

### (iii) Voltage to current converter

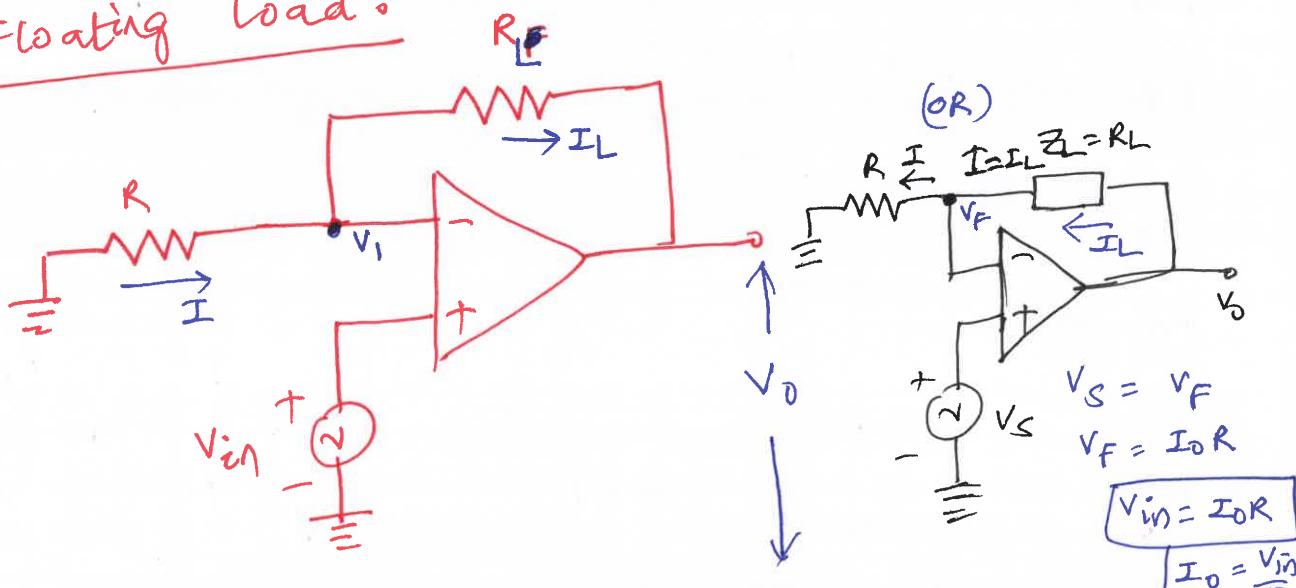


$$V_0 = I_S \times \left( \frac{R \times R_L}{R + R_L} \right) =$$

But this is not converting  $I_S$  into a voltage source because  $V_o$  is dependent on  $RL$ . Hence given ckt is not a converter.

### (ii) Voltage to Current Converter

## (a) Floating load:



It is basically a Non-inverting op-amp.

But in this  $R_F$  is replaced with  $R_L$ .

Because of  $A_V = \infty$ , the input of op-amp is virtually shorted. So  $V_{in}$  appears at  $V_1$ .

Waiting KCL at point  $V_1$ .

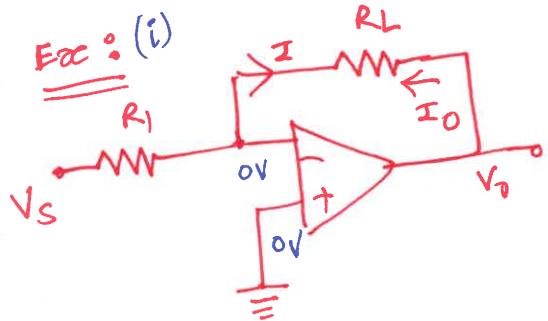
$$I = I_L \quad \text{But} \quad I = \frac{V_I}{R}$$

$$\therefore I_L = \frac{V_I}{R}$$

.. output current is proportional to the input voltage

Hence the input voltage gets converted into an output vs. current ( $I_L$ ).

### ~~(i)~~ For Grounded loads

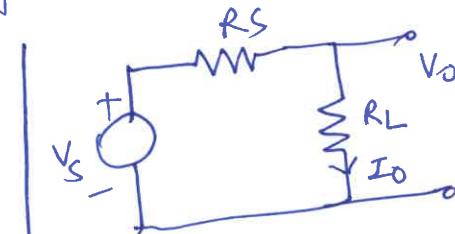


$$I = \frac{V_s - 0}{R_1} \Rightarrow I = \frac{V_s}{R_1}$$

$$I_o = -I = -\frac{V_s}{R_1}$$

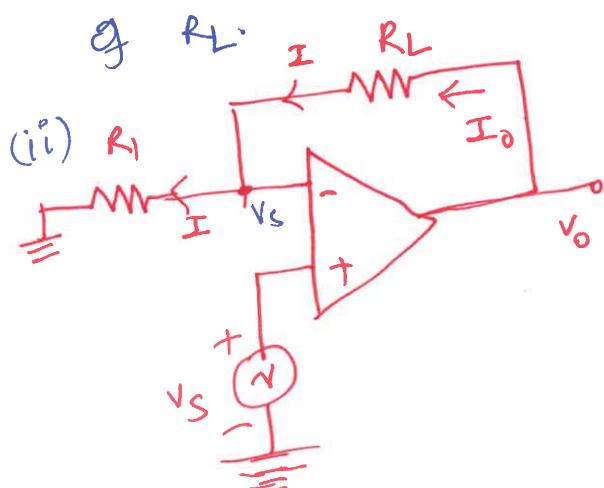
$I_o$ : output current Independent

{It is standard conversion to take load current  $I_o$  in direction away from output voltage}



$$\frac{V_o}{R_L} = I_o = \frac{V_s}{R_s + R_L}$$

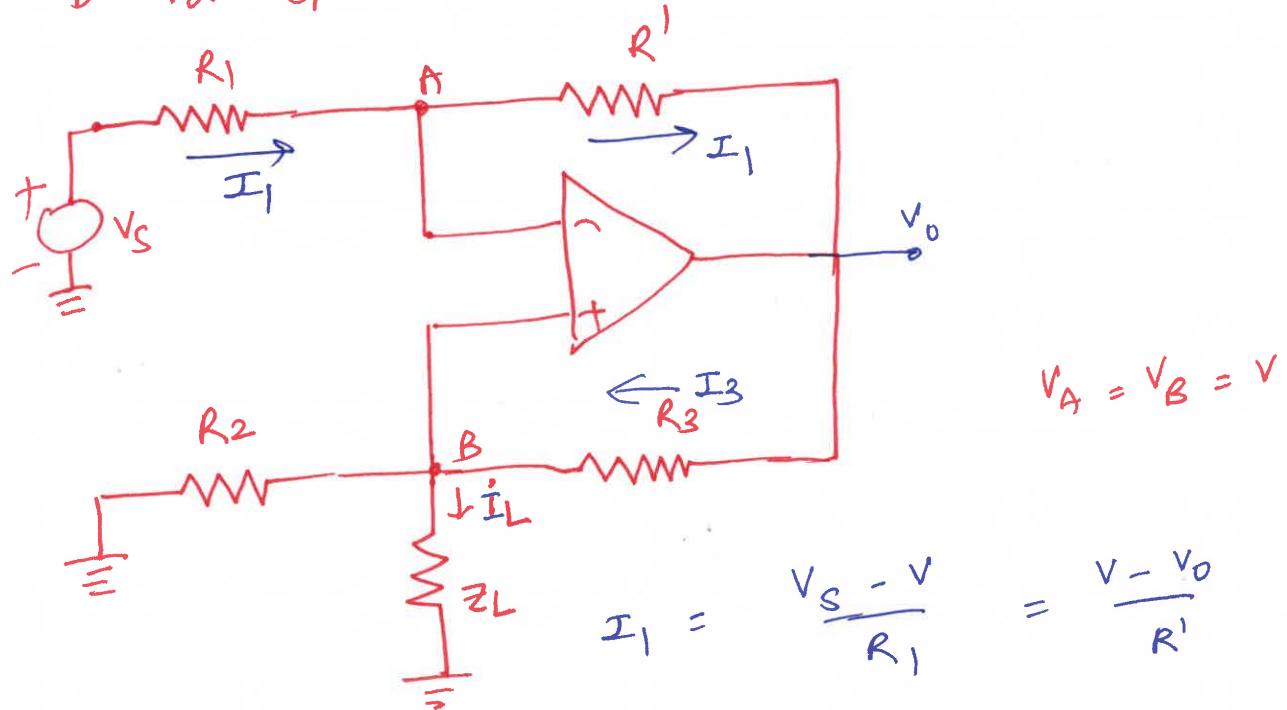
$\therefore I_o$  depends on  $R_L$ , hence not a converter



$$\frac{V_s - 0}{R_1} = I$$

$$I_o = I = \frac{V_s}{R_1}$$

(ii) For Grounded Loads



$$I_1 = \frac{V_s - V}{R_1} = \frac{V - V_0}{R'}$$

$$\begin{aligned} \frac{V_s}{R_1} + \frac{V_0}{R'} &= \frac{V}{R_1} + \frac{V}{R'} \\ &= V \left[ \frac{1}{R_1} + \frac{1}{R'} \right] \end{aligned}$$

$$V = \frac{V_s}{R_1} + \frac{V_0}{R'} / \left[ \frac{1}{R_1} + \frac{1}{R'} \right]$$

$$I_3 = \frac{V_0 - V}{R_3} = \frac{V - 0}{R_2} + I_L$$

(iii) applying KCL at node B

$$I_L = \frac{V_0 - V}{R_3} - \frac{V}{R_2}$$

$$= \frac{V_0}{R_3} - \frac{V}{R_3} - \frac{V}{R_2}$$

$$I_L = \frac{V_0}{R_3} - V \left[ \frac{1}{R_3} + \frac{1}{R_2} \right]$$

Substitute the value of  $V_o$  in  $I_L$  equation.

$$I_L = \frac{V_o}{R_3} - \left[ \frac{V_s}{R_1} + \frac{V_o}{R'} \right] \left/ \left( \frac{1}{R_1} + \frac{1}{R'} \right) \right. \left[ \frac{1}{R_3} + \frac{1}{R_2} \right]$$

$$I_L = \frac{V_o}{R_3} - \frac{\frac{V_s}{R_1} \left( \frac{1}{R_3} + \frac{1}{R_2} \right)}{\left( \frac{1}{R_1} + \frac{1}{R'} \right)} - \frac{\frac{V_o}{R'} \left[ \frac{1}{R_3} + \frac{1}{R_2} \right]}{\left( \frac{1}{R_1} + \frac{1}{R'} \right)}$$

We want the load current  $I_L$  must be

independent of  $V_o$   
So that the coefficient of  $V_o = 0$

$$\frac{1}{R_3} = \frac{1}{R'} \left[ \frac{1}{R_3} + \frac{1}{R_2} \right] \times \frac{1}{\left( \frac{1}{R_1} + \frac{1}{R'} \right)}$$

$$R' \left[ \frac{1}{R_1} + \frac{1}{R'} \right] = R_3 \left[ \frac{1}{R_3} + \frac{1}{R_2} \right]$$

$$1 + \frac{R'}{R} = 1 + \frac{R_3}{R_2}$$

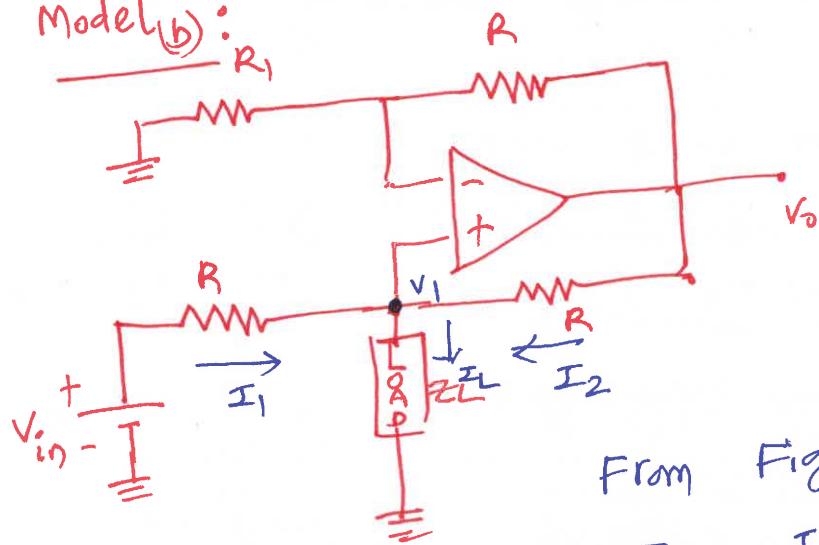
$$\therefore \frac{R'}{R} = \frac{R_3}{R_2}$$

$$\therefore I_L = -\frac{V_s}{R_1} \left[ \frac{1}{R_3} + \cancel{\frac{1}{R_2}} \right] \left/ \left( \frac{1}{R_1} + \cancel{\frac{1}{R'}} \right) \right.$$

$$I_L = -\frac{V_s}{R_1}$$

$\therefore$  the output current is proportional to input voltage  
So it is called Voltage to Current converter

Model(b):



From Figure

$$I_L = I_1 + I_2$$

$$I_1 = \frac{v_{in} - v_1}{R} \quad \text{and} \quad I_2 = \frac{v_o - v_1}{R}$$

$$\therefore I_L = \frac{v_{in} - v_1}{R} + \frac{v_o - v_1}{R}$$

$$I_L = \frac{v_{in} + v_o - 2v_1}{R}$$

$$I_L R = v_{in} + v_o - 2v_1$$

$$v_1 = \frac{v_{in} + v_o - I_L R}{2}$$

We know that the closed loop gain of  
non-inverting op-amp is given by

$$1 + \frac{R_F}{R} \quad \text{where } R_F = \frac{F/B}{\text{resistance}}$$

$$\text{But } R_F = R$$

$$\text{Overall gain} = 1 + \frac{R}{R} = 2$$

$$\text{o/p voltage } v_o = 2v_i$$

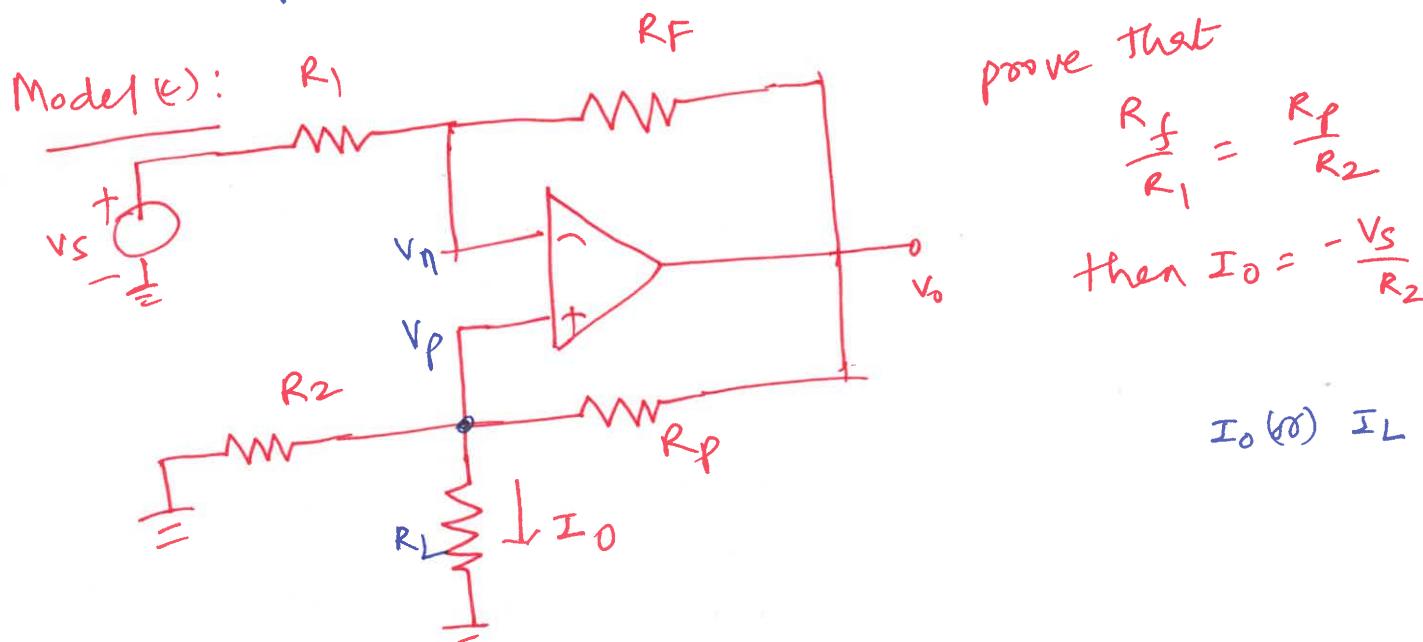
$$\text{Where } v_i = \frac{v_{in} + v_o - I_L R}{2}$$

$$\therefore v_o = v_{in} + v_o - I_L R$$

$$I_L R = v_{in}$$

$$I_L = \frac{v_{in}}{R}$$

$\frac{v_{in}}{R} \times 2$  Input voltage gets converted into  
o/p load current  $I_L$



Sol: Applying KCL at node  $v_p$

$$\frac{v_p - 0}{R_2} + \frac{v_p - v_o}{R_P} + \frac{v_p}{R_L} = 0$$

$$V_p \left[ \frac{1}{R_2} + \frac{1}{R_p} + \frac{1}{R_L} \right] = \frac{V_o}{R_p} \rightarrow (1)$$

$$I_o = \frac{V_p}{R_L} \rightarrow (2)$$

Applying KCL at node  $V_n$

$$\frac{V_n - V_s}{R_1} + \frac{V_n - V_o}{R_F} = 0$$

$$\frac{V_p - V_s}{R_1} + \frac{V_p - V_o}{R_F} = 0$$

$$V_p \left[ \frac{1}{R_1} + \frac{1}{R_F} \right] = \frac{V_s}{R_1} + \frac{V_o}{R_F}$$

putting  $V_o$  from eq(1)

$$V_p \left[ \frac{1}{R_1} + \frac{1}{R_F} \right] = \frac{V_s}{R_1} + \frac{1}{R_F} \left[ R_p V_p \left[ \frac{1}{R_2} + \frac{1}{R_L} + \frac{1}{R_p} \right] \right]$$

on Simplifying

$$V_p = \frac{-R_2 R_L R_p R_F V_s}{R_1 R_2 R_p^2 + R_L R_p [R_p R_1 - R_2 R_F]}$$

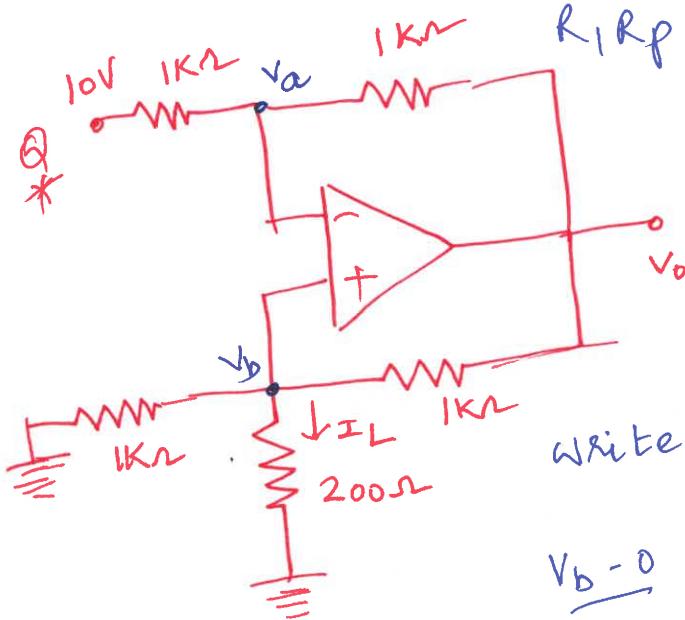
From circuit  $I_o = \frac{V_p}{R_L}$

$$I_o = \frac{-R_2 R_p R_F V_s}{R_1 R_2 R_p^2 + R_L R_p [R_p R_1 - R_2 R_F]}$$

$$\text{If } R_p R_1 = R_2 R_{RF}$$

$$(10) \quad \frac{R_{RF}}{R_1} = \frac{R_p}{R_2} \Rightarrow \frac{1}{R_2} = \frac{R_{RF}}{R_p R_1}$$

$$\therefore I_o = \frac{-V_s}{R_1 R_p} R_{RF} = \frac{-V_s}{R_2} //$$



determine  $I_L$ ?

write KCL at  $V_b$  (b)

$$\frac{V_b - 0}{200} + \frac{V_b - V_o}{1k} + \frac{V_b - 0}{1k} = 0$$

$$V_b \left[ \frac{1}{200} + \frac{1}{1k} + \frac{1}{1k} \right] = \frac{V_o}{1k}$$

$$5V_b + V_b + V_b = V_o$$

$$7V_b = V_o \rightarrow (1)$$

apply KCL at node (a)

$$\frac{V_a - V_o}{1k} + \frac{V_a - 10}{1k} = 0$$

$$2V_a = V_o + 10 \Rightarrow V_a = \frac{10 + V_o}{2} = V_b$$

Substitute this  $V_b$  value in eq (1)

$$7 \left[ \frac{10 + V_o}{2} \right] = V_o \Rightarrow 2V_o = 70 + 7V_o$$

$$-5V_o = 70$$

$$V_o = -\frac{70}{5}$$

$$\therefore V_b = \frac{V_o}{7} = -\frac{70/5}{7} = -10/5 = -2V$$

$$\therefore I_L = \frac{V_b}{200} = -\frac{2}{200} = -10mA$$

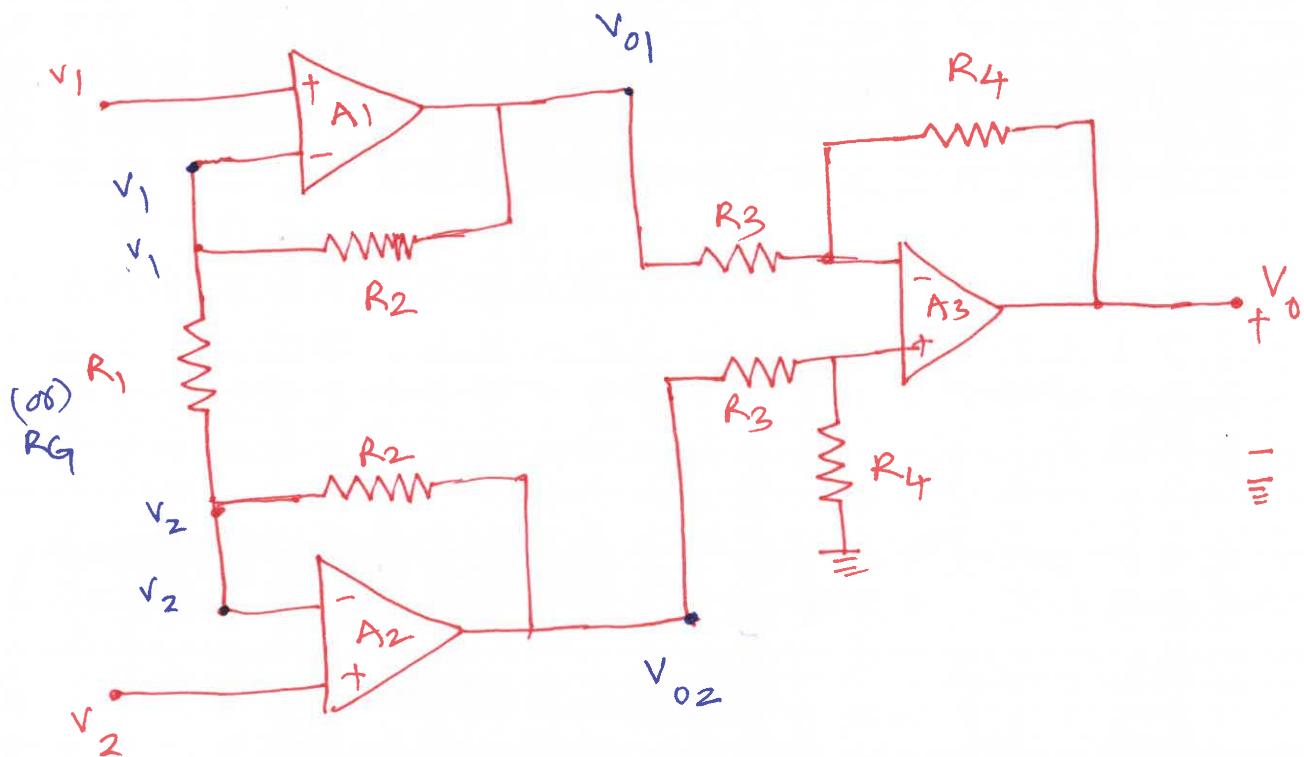
## INSTRUMENTATION AMPLIFIER:

Differential Amplifier Disadvantages:

1. Its main drawback are its low input resistance.
2. Its gain cannot be varied easily.

Block diagram of Instrumentation Amplifier:

\* It is a high gain amplifier  
IA is used to improve the input impedance and voltage gain.



Writing KCL equations.

$$\frac{v_1 - v_{01}}{R_2} + \frac{v_1 - v_2}{R_1} = 0$$

# INSTRUMENTATION AMPLIFIER

$$\frac{v_1}{R_2} + \frac{v_1}{R_1} - \frac{v_2}{R_1} = \frac{v_{o1}}{R_2} \Rightarrow \frac{v_{o1}}{R_2} = \frac{R_1 + R_2}{R_1 R_2} v_1 - \frac{v_2}{R_1}$$

$$\therefore v_{o1} = \frac{R_1 + R_2}{R_1} v_1 - \frac{R_2}{R_1} v_2$$

$$v_{o1} = \left(1 + \frac{R_2}{R_1}\right) v_1 - \frac{R_2}{R_1} v_2 \quad \longrightarrow (1)$$

Second KCL equation at node  $v_2$ .

$$\frac{v_2 - v_{o2}}{R_2} + \frac{v_2 - v_1}{R_1} = 0$$

$$\therefore \frac{v_2}{R_2} + \frac{v_2}{R_1} - \frac{v_1}{R_1} = \frac{v_{o2}}{R_2} \Rightarrow \frac{v_{o2}}{R_2} = \frac{R_1 + R_2}{R_1 R_2} v_2 - \frac{v_1}{R_1}$$

$$\therefore v_{o2} = \left(1 + \frac{R_2}{R_1}\right) v_2 - \frac{R_2}{R_1} v_1 \quad \longrightarrow (2)$$

$$v_{o1} - v_{o2} = \left(1 + \frac{R_2}{R_1}\right) v_1 - \frac{R_2}{R_1} v_2 - \left[\left(1 + \frac{R_2}{R_1}\right) v_2 - \frac{R_2}{R_1} v_1\right]$$

$$= v_1 + \frac{R_2}{R_1} v_1 - \frac{R_2}{R_1} v_2 - v_2 - \frac{R_2}{R_1} v_2 + \frac{R_2}{R_1} v_1$$

$$= v_1 + \frac{2R_2}{R_1} v_1 - \frac{2R_2}{R_1} v_2 - v_2$$

$$= v_1 \left[1 + \frac{2R_2}{R_1}\right] - \left(1 + \frac{2R_2}{R_1}\right) v_2$$

$$= \left(1 + \frac{2R_2}{R_1}\right) (v_1 - v_2)$$

$$\therefore v_o = -\frac{R_4}{R_3} [v_{o1} - v_{o2}]$$

$$V_0 = -\frac{R_4}{R_3} \left[ \left(1 + \frac{2R_2}{R_1}\right) (V_1 - V_2) \right]$$

$$= \frac{R_4}{R_3} \left[ \left(1 + \frac{2R_2}{R_1}\right) (V_2 - V_1) \right]$$

differential Voltage gain ( $A_d$ ) =  $\frac{V_0}{V_2 - V_1}$

$$= \left(1 + \frac{2R_2}{R_1}\right) \frac{R_4}{R_3} //$$

$$A_d = \frac{R_4}{R_3} \left[ 1 + \frac{2R_2}{R_1} \right]$$

**Requirements of a Good Instrumentation Amplifier**  
 The Instrumentation amplifiers are used to amplify the low level differential signals in presence of the large common mode noise and interference signals.  
 Hence a good instrumentation amplifier has to meet the following specifications.

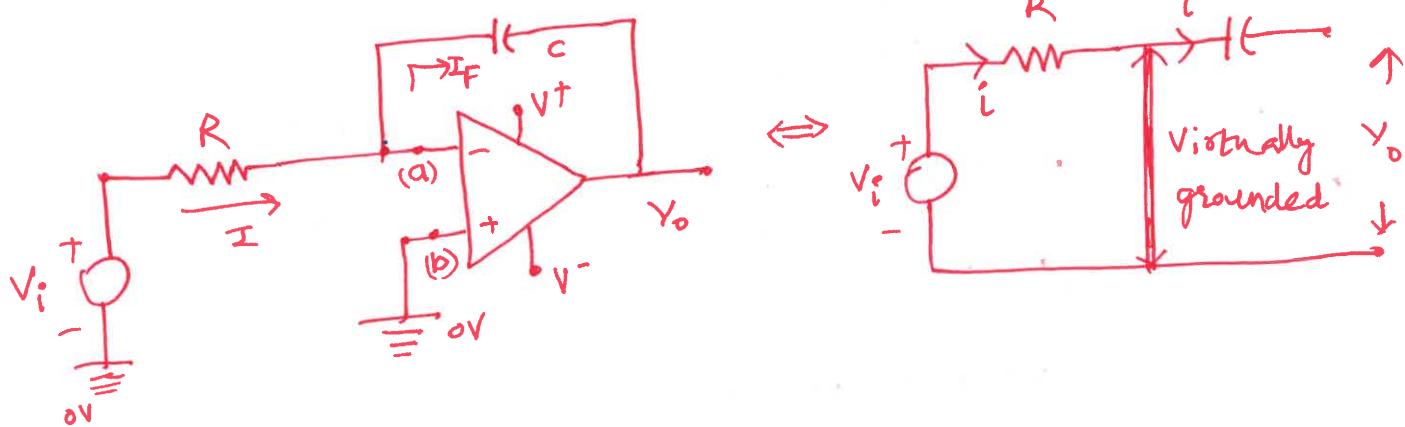
1. Finite, accurate & stable gain  
 2. Easier gain adjustment: Not only finite & stable gain is required but a variable gain over the prescribed range is also required.

3. High Input Impedance: To avoid the loading of input sources, input impedance of IA must be very high

4. Low output Impedance: Extremely low output impedance (ideally zero) to avoid the loading on the immediate stage.

5. High CMRR. 6. Low power consumption & High slew rate.

## OP-AMP INTEGRATOR:



$$V_o \propto \int V_i dt$$

since  $V_{id} \approx 0 ; V_b = V_a = 0$

Apply KCL at node (a)  
 $I = I_F$

$$\frac{V_i - V_a}{R} = C \frac{d}{dt} [V_a - V_o]$$

$$\frac{V_i}{R} = C \frac{d}{dt} (-V_o)$$

$$\frac{V_i}{R} = -C \frac{dV_o}{dt}$$

$$\Rightarrow \frac{dV_o}{dt} = -\frac{1}{RC} V_i$$

Integrating on both sides

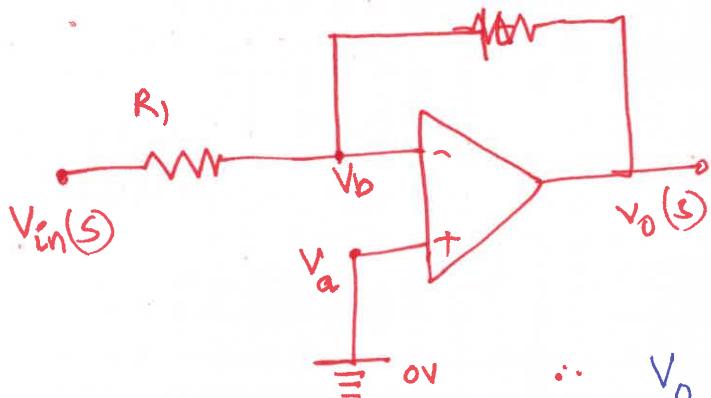
$$V_o = -\frac{1}{RC} \int V_i dt$$

$$V_o \propto \int V_i dt \rightarrow \text{Integrator}$$

Time Constant =  $RC$

$$V_o = -\frac{1}{RC} \int_0^t V_i dt + C$$

# FREQUENCY DOMAIN INTEGRATOR:



Since  $V_{id} = 0$

$$V_b = V_a = 0$$

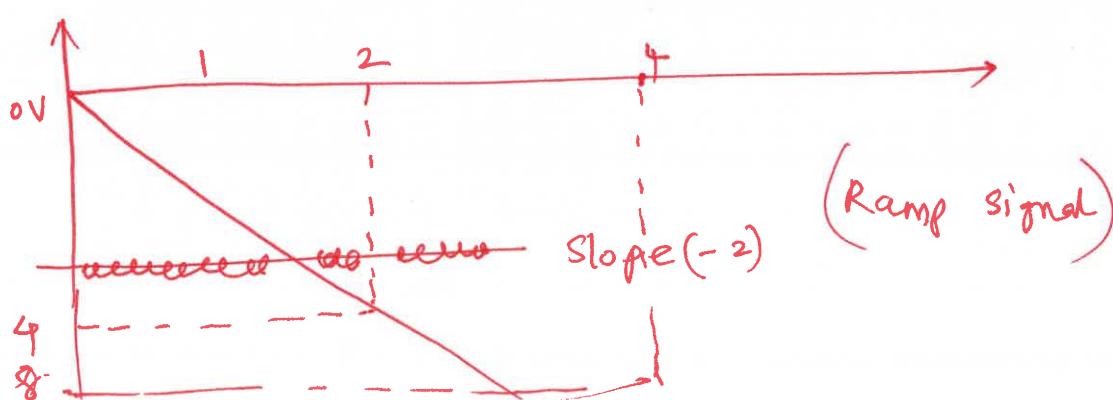
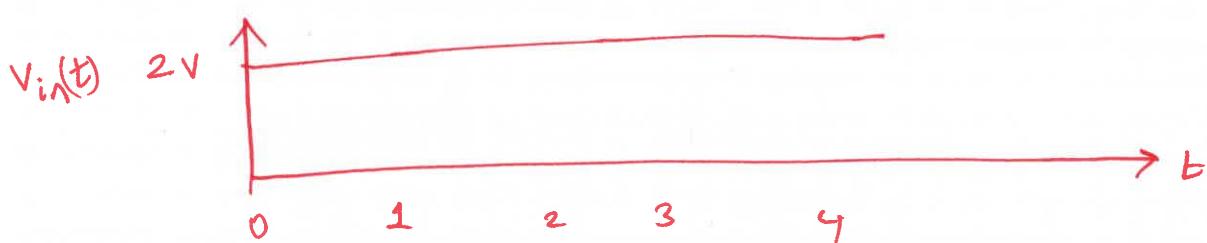
$$\frac{V_o(s)}{V_{in}(s)} = -\frac{Z_F}{Z_1} = \frac{-\frac{1}{SCF}}{\frac{1}{R_1}} = \frac{-1}{SCF R_1}$$

$$\text{put } s = j\omega$$

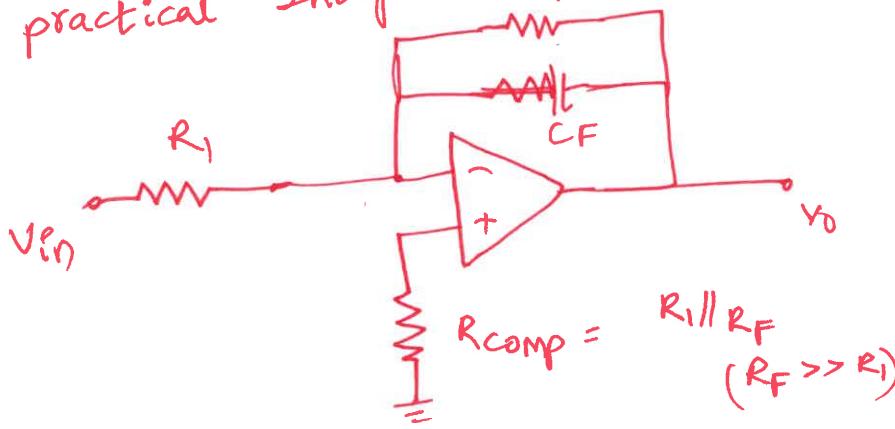
$$\frac{V_o(j\omega)}{V_{in}(j\omega)} = -\frac{1}{j\omega C F R_1}$$

Magnitude  $\left| \frac{V_o(j\omega)}{V_{in}(j\omega)} \right| = \frac{1}{\omega C F R_1} = \frac{1}{2\pi f C F R_1}$

$$V_o(j\omega) = -\frac{1}{j\omega C F R_1} V_{in}(j\omega)$$



practical Integrator: RF



The gain of an integrator at low frequency (dc) can be limited to avoid the saturation problem if the feedback capacitor is shunted by a resistance  $R_F$  as shown.

Voltage gain of practical Integrator:

$$\frac{V_o(s)}{V_{in}(s)} = \frac{-Z_F(s)}{Z_I(s)} = \frac{-\frac{RF}{RFCFs+1}}{\frac{R_1}{R_1}} = \frac{-RF}{(1 + sRFCF)R_1} = \frac{-RF}{R_1} \frac{1}{1 + sRFCF}$$

$Z_F(s) = \frac{RF \parallel \frac{1}{sCF}}{RF + \frac{1}{sCF}} = \frac{RF}{RFCFs + 1}$

$\left[ \omega_1 = \frac{1}{RFCF} \right]$

$$\frac{V_o(j\omega)}{V_{in}(j\omega)} = \frac{-\frac{RF}{R_1}}{(1 + j\omega RFCF)} = \frac{-RF}{R_1} \frac{1}{1 + j(\omega/\omega_1)}$$

$$\left| \frac{V_o(j\omega)}{V_{in}(j\omega)} \right| = \frac{\frac{R_F}{R_1}}{\sqrt{1 + (\omega R_F C_F)^2}}$$

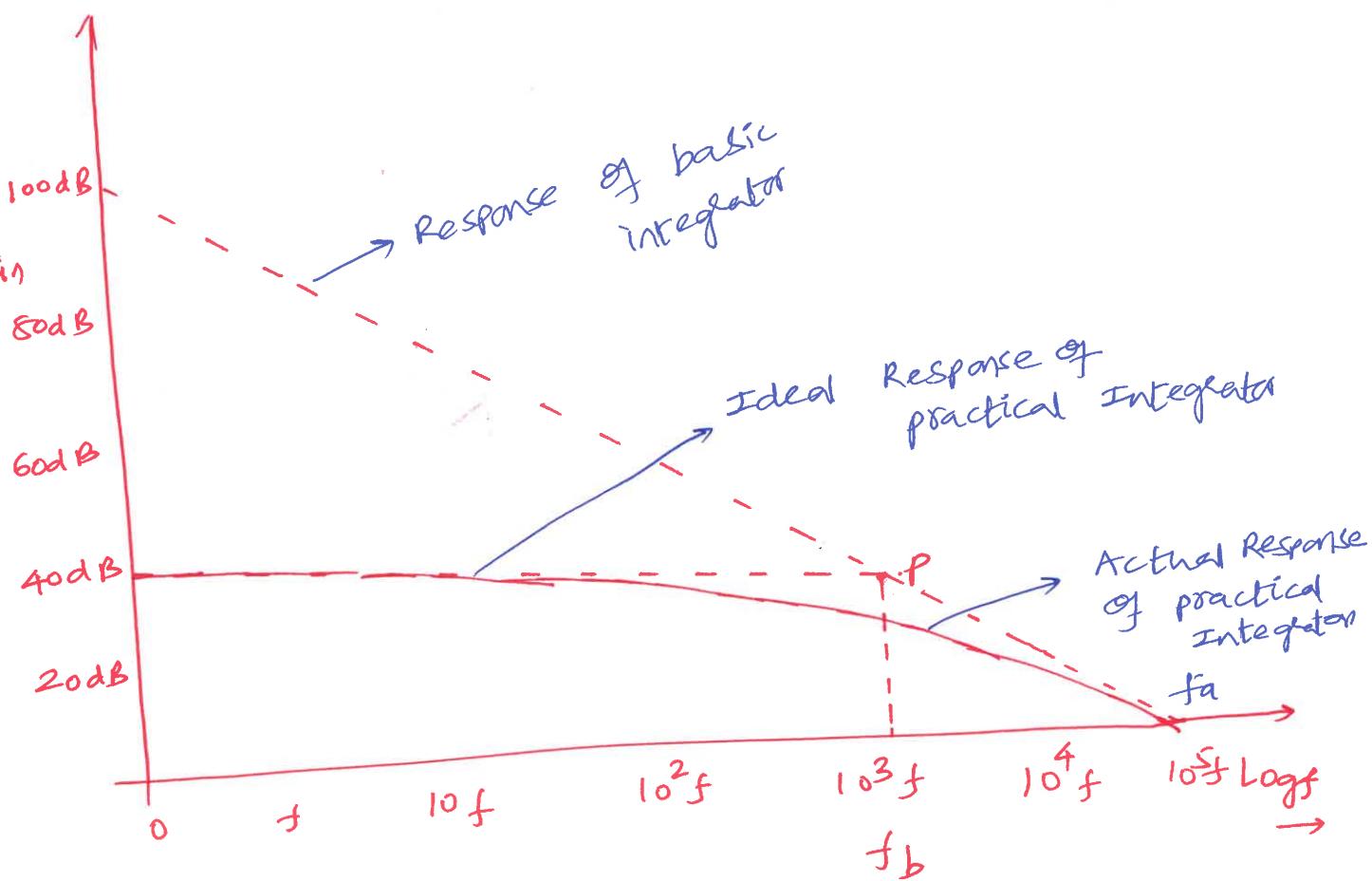
$$\therefore A_V = \frac{-\frac{R_F}{R_1}}{1 + j(\omega/\omega_1)} \quad \omega_1 = \frac{1}{R_F C_F}$$

$$= \boxed{A_V = \frac{-R_F/R_1}{1 + j(f/f_1)}} \quad A_{V_0} = -\frac{R_F}{R_1}$$

\* The feedback resistor  $R_F$  limits the gain.

The d.c gain (at  $\omega=0$ )  $A_{V_0} = -\frac{R_F}{R_1}$

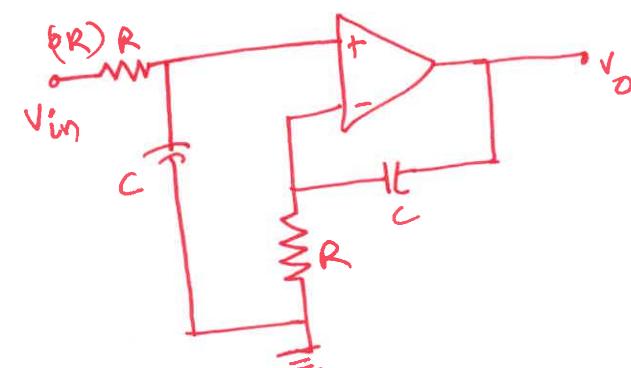
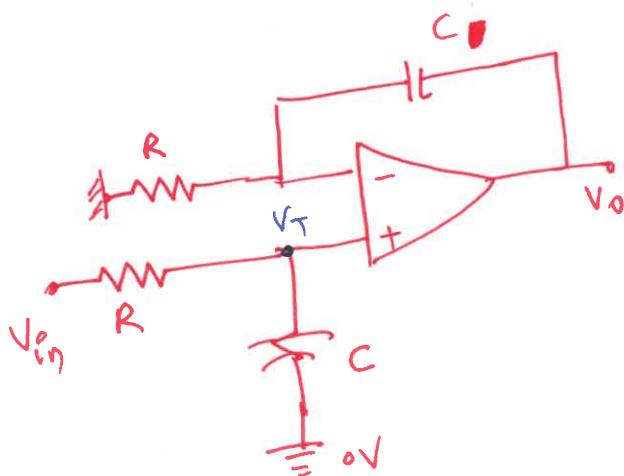
$$(A_{V_0}) = \frac{R_F}{R_1}$$



$$f_b = \frac{1}{2\pi R_F C_F}$$

$$f_a = \frac{1}{2\pi R_i C_F}$$

Non Inverting Integrator:



$$V_T(s) = V_{in}(s) \times \left( \frac{\frac{1}{sC}}{R + \frac{1}{sC}} \right)$$

$$V_T(s) = \left[ \frac{V_{in}(s)}{1 + SRC} \right]$$

$$V_o(s) = \left[ 1 + \frac{\frac{1}{sC}}{R} \right] \times V_{in}(s)$$

$$\begin{aligned} V_o(s) &= \left[ 1 + \frac{1}{SCR} \right] \frac{V_{in}(s)}{(1 + SCR)} \\ &= \frac{(1 + SCR)}{SCR} \times \frac{V_{in}(s)}{(1 + SCR)} \end{aligned}$$

$$V_o(s) = \frac{1}{SCR} V_{in}(s)$$

Apply Inverse Laplace Transform

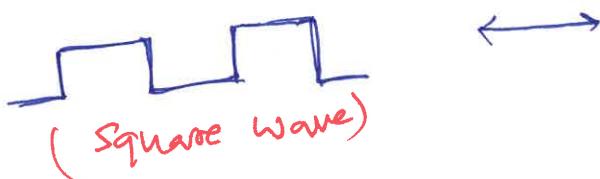
$$V_o(t) = \frac{1}{RC} \int V_{in}(t) dt$$

Imp:



- (1) If the Input voltage is a step voltage, then the output voltage will be a ramp (or) Linearly changing

Voltage

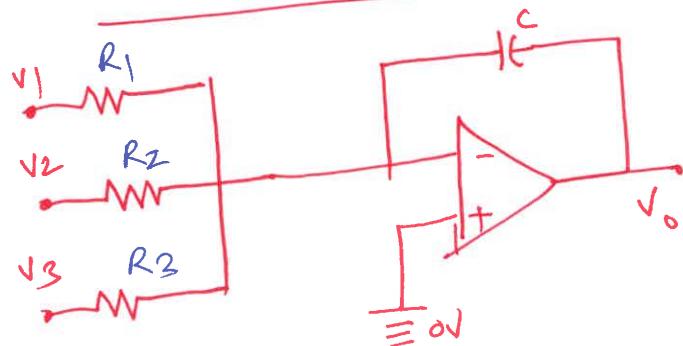


(2)

- If the input voltage is a sinusoidal signal, the o/p voltage will be Cosine wave.

Integrators are widely used in ramp or sweep generators, filters, analog computers etc.

### SUMMING INTEGRATOR:

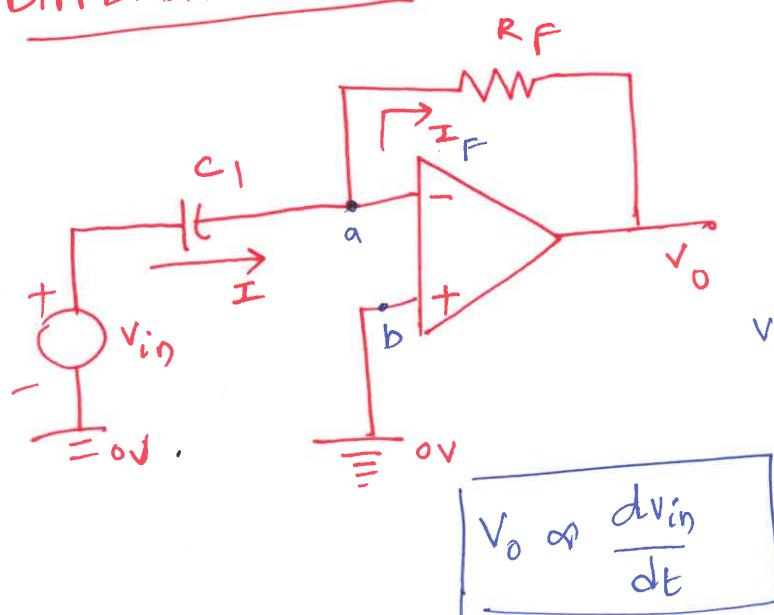


Generally, Summing Integrators are used in analog computers.

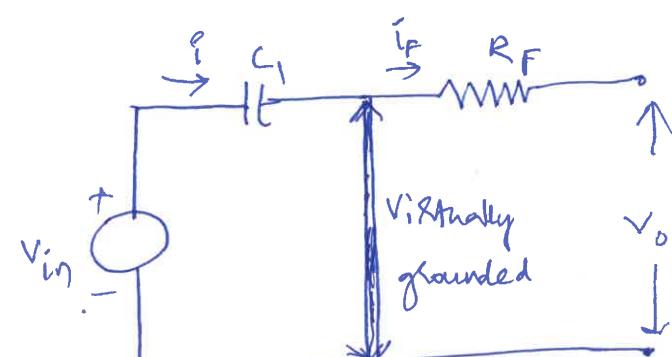
The op voltage

$$V_0 = - \left[ \frac{1}{R_1 C} \int V_1 dt + \frac{1}{R_2 C} \int V_2 dt + \frac{1}{R_3 C} \int V_3 dt \right]$$

### DIFFERENTIATOR:



### EQUIVALENT CKE:



$$\text{Since } V_{id} = 0 ; \quad V_b = V_a = 0$$

Apply KCL at node (a)

$$C \frac{d(V_{in} - V_a)}{dt} = \frac{V_a - V_0}{R_F}$$

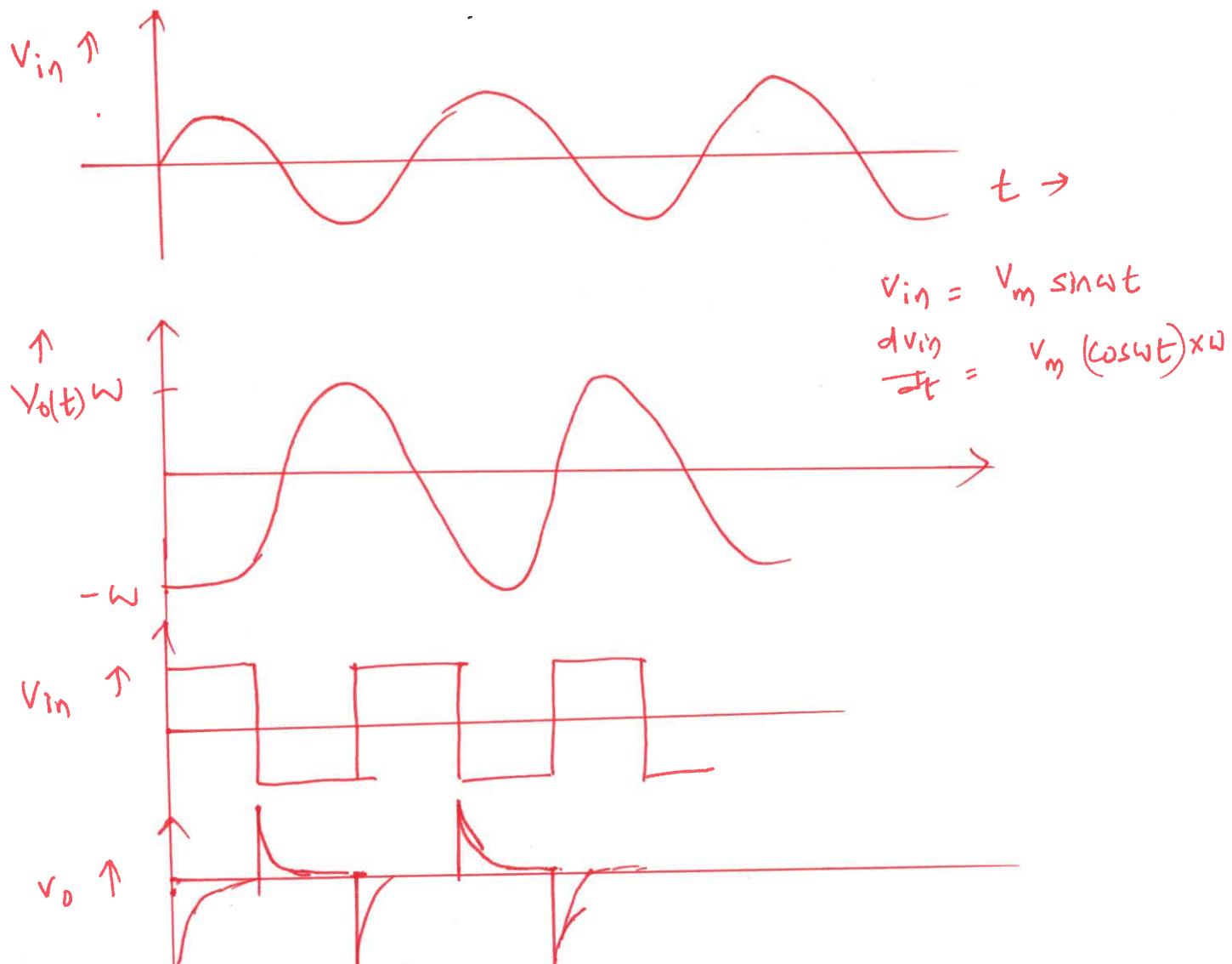
$$C_1 \frac{dV_{in}}{dt} = -\frac{V_o}{R_F}$$

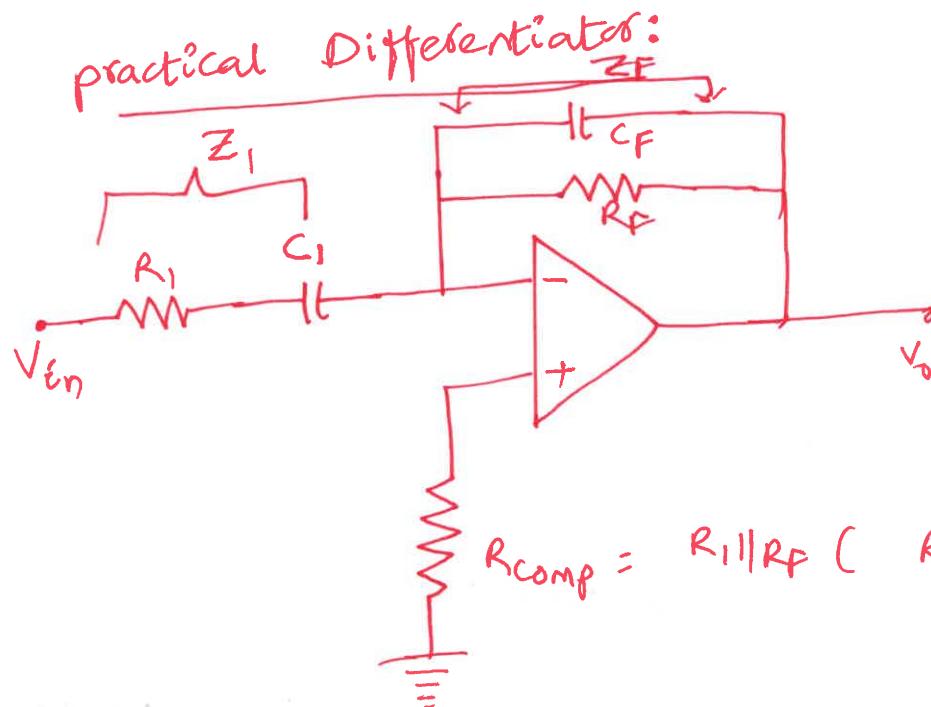
$$V_o = -R_F C_1 \frac{dV_{in}}{dt}$$

$$\text{Time Constant } (\tau) = R_F C_1$$

$\therefore$  The op voltage ( $V_o$ ) is a time constant  
 $(-R_F C_1)$  times the derivative of input voltage

$V_{in}$ .  
The -ve sign indicates  $180^\circ$  phase shift b/w  
the input and output signal.





$$R_{\text{comp}} = R_1 \parallel R_F \quad (R_F \gg R_1)$$

The transfer function

$$\frac{V_o(s)}{V_{\text{in}}(s)} = - \frac{Z_F}{Z_1}$$

$$Z_1 = R_1 + \frac{1}{sC_1} = \frac{1 + sC_1 R_1}{sC_1}$$

$$Z_F = R_F \parallel \frac{1}{sC_F} = \frac{R_F \times \frac{1}{sC_F}}{R_F + \frac{1}{sC_F}}$$

$$\frac{V_o(s)}{V_{\text{in}}(s)} = - \frac{\frac{R_F}{1 + sR_F C_F}}{\frac{(1 + sR_1 C_1)}{sC_1}}$$

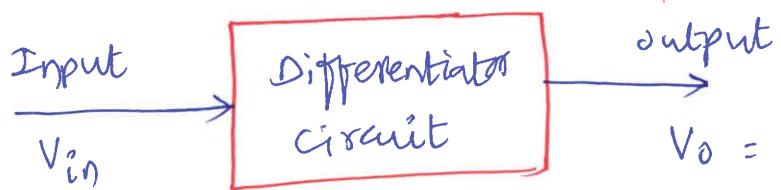
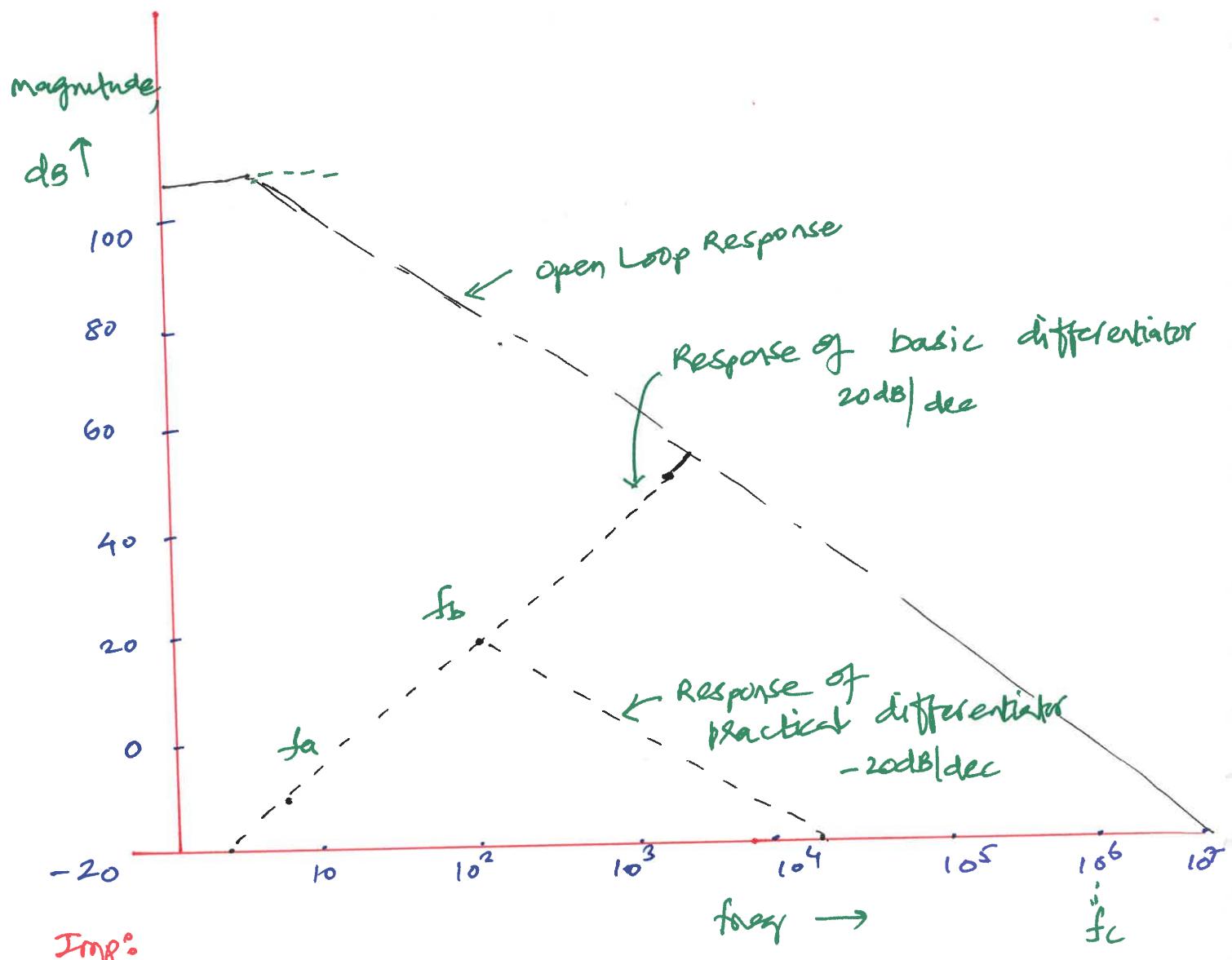
$$= - \frac{sR_F C_1}{(1 + sR_F C_F)(1 + sR_1 C_1)}$$

For  $R_F C_F = R_1 C_1$

$$\frac{V_o(s)}{V_{\text{in}}(s)} = - \frac{R_F C_1 s}{(1 + sR_F C_F)^2}$$

$$f_b = \frac{1}{2\pi R_F C_F}$$

Frequency Response:



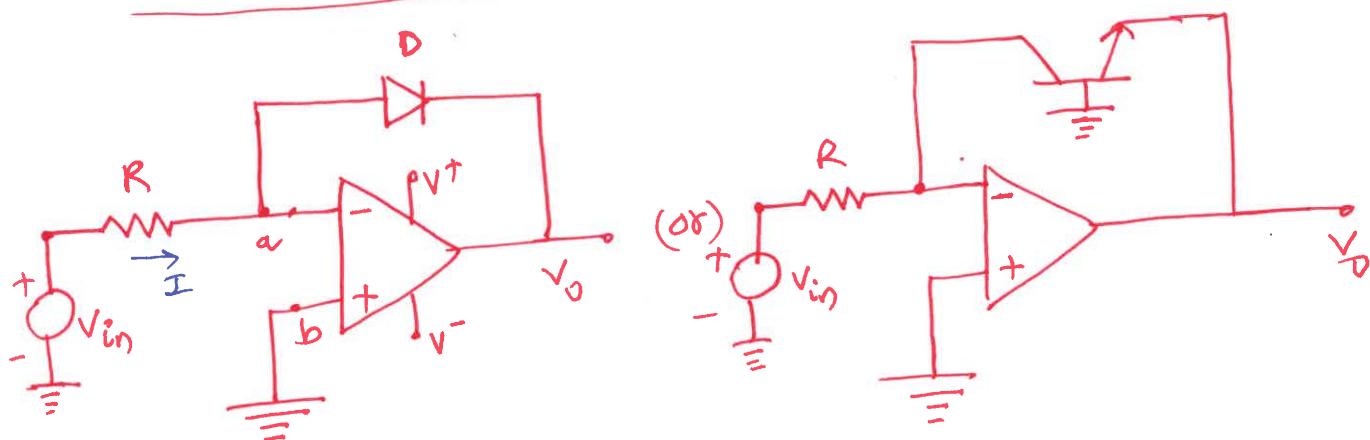
$$V_o = -RC \frac{dV_{in}}{dt} = -\gamma \frac{dV_{in}}{dt}$$

( $\gamma = \text{time const}$ )

Applications:

- op-amp differentiator is to produce very narrow spikes.
- A cosine wave input will generate a sine wave o/p.
- A triangular input will produce a square wave output.

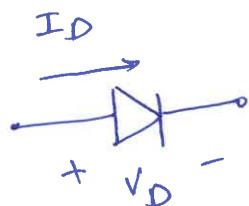
## LOGARITHMIC AMPLIFIER:



Since  $V_{id} \approx 0$

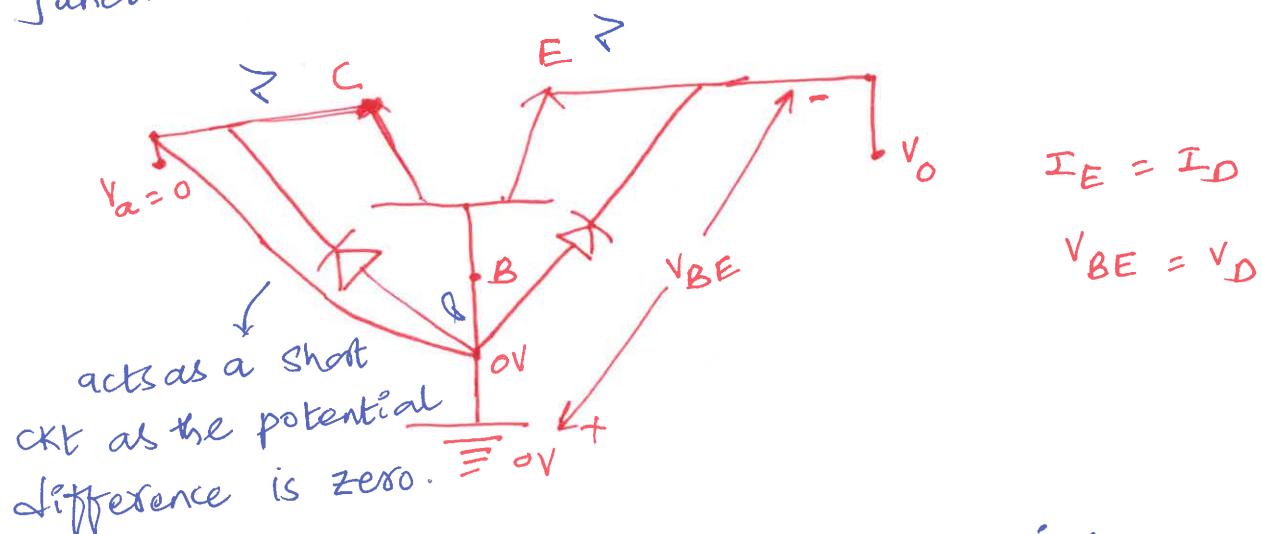
$$V_b = V_a = 0$$

node 'a': virtual ground



\* Grounded base transistor in this circuit acts as a

PN junction diode



We know the diode current equation

when the diode is in forward biased

$$I_D = I_0 \left[ e^{\frac{V_D}{\eta V_T}} - 1 \right]$$

$$I_D = I_0 e^{\frac{V_D}{\eta V_T}} - I_0$$

$$I_D + I_0 = I_{D0} e^{\frac{V_D}{\gamma V_T}}$$

$I_0$  = Reverse saturation current.

$$I_D \gg I_0$$

$$\therefore I_D + I_0 \approx I_D$$

$$\therefore I_D \approx I_{D0} e^{\frac{V_D}{\gamma V_T}}$$

Apply KCL at node (a)

$$I_D = I$$

$$I_0 = \frac{V_i^o - 0}{R} = \frac{V_i^o}{R}$$

$$I_{D0} e^{\frac{V_D}{\gamma V_T}} = \frac{V_i^o}{R}$$

$$e^{\frac{V_D}{\gamma V_T}} = \frac{V_i^o}{I_{D0} R}$$

$$\frac{V_D}{\gamma V_T} = \ln\left(\frac{V_i^o}{I_{D0} R}\right)$$

writing KVL equation

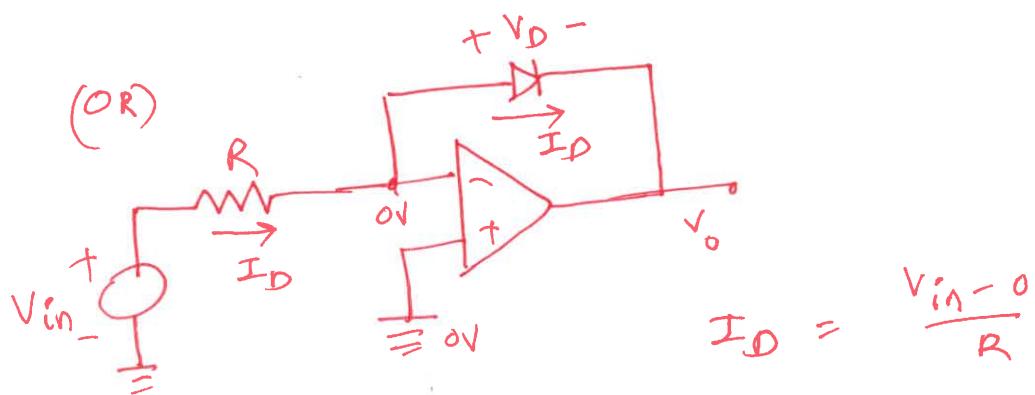
$$-V_a + V_D + V_o = 0$$

$$V_a \rightarrow 0$$

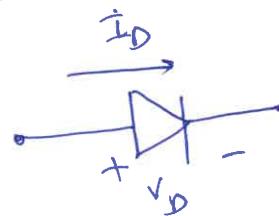
$$V_o = -V_D$$

$$V_o = -\gamma V_T \ln\left(\frac{V_i^o}{I_{D0} R}\right)$$

$V_o \propto \ln(V_i^o) \rightarrow$  Logarithmic Amplifier.



$$I_D = \frac{V_{in} - 0}{R}$$



We know

$$I_D = I_S e^{\frac{V_D}{V_T}} \quad [\gamma = 1]$$

For Ge  
diode

$$V_D = V_T \ln\left(\frac{I_D}{I_S}\right)$$

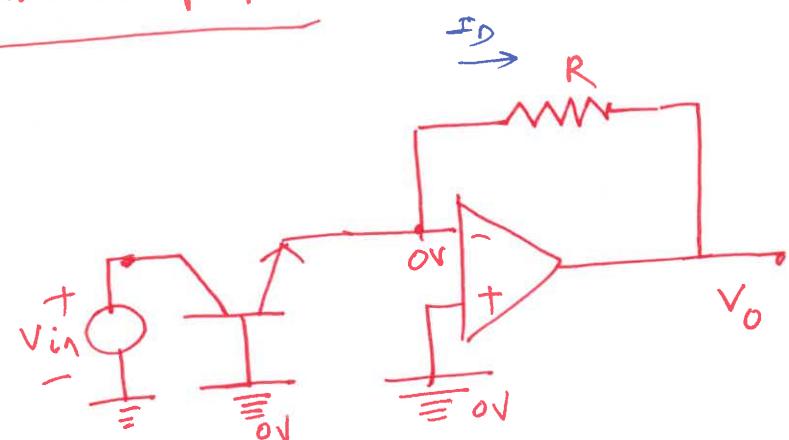
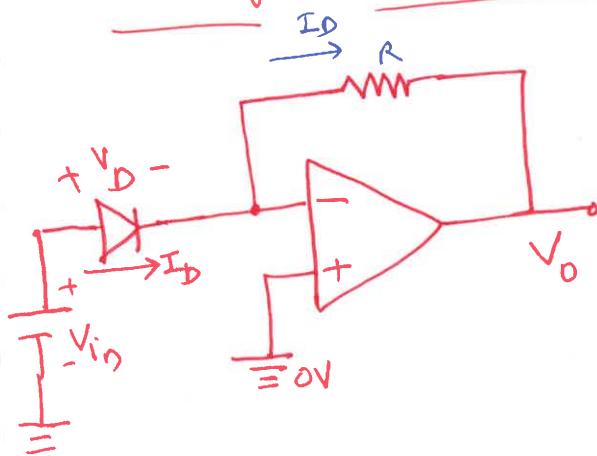
$$I_D = \frac{V_{in}}{R}$$

$$\rightarrow V_o = -V_D$$

$$= -V_T \ln\left(\frac{I_D}{I_S}\right) = -V_T \ln\left(\frac{V_{in}}{R I_S}\right)$$

\*  $V_o \propto \ln(V_{in})$

### Antilog (or) Exponential Amplifiers:



Antilog amplifiers using diode and BJT.

writing KVL equation

$$-V_{in} + V_D = 0$$

$$V_{in} = V_D$$

$$I_D = \frac{0 - V_D}{R} = -\frac{V_D}{R}$$

$$\boxed{V_o = -I_D R}$$

We know diode current equation

$$I_D = I_0(e^{\frac{V_D}{nV_T}} - 1)$$
$$= I_0 e^{\frac{V_D}{nV_T}} - I_0$$
$$\frac{V_D}{nV_T}$$

$$I_D + I_0 = I_0 e$$

$$I_D \ggg I_0$$

$$I_D + I_0 \approx I_D$$
$$\frac{V_D}{nV_T}$$

$$\therefore I_D = I_0 e$$

$$\therefore V_o = -\left[ I_0 e^{\frac{V_D}{nV_T}} \right] R$$

$$V_o = -(I_0 R) e^{\frac{V_D}{nV_T}}$$

$$\boxed{V_o = -(I_0 R) e^{\frac{V_{in}}{nV_T}}}$$

in case of  
diode

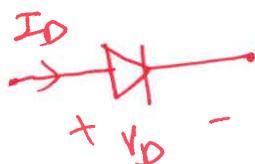
$$V_o = -I_{C0}R \left[ e^{\frac{V_o}{\eta V_T}} \right] \text{ (using BJT)}$$

$\therefore$

$V_o \propto e^{\frac{V_{in}}{\eta V_T}}$

\* Small Signal Analysis of diode:

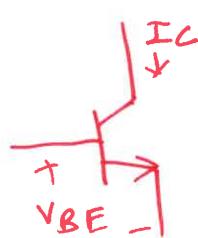
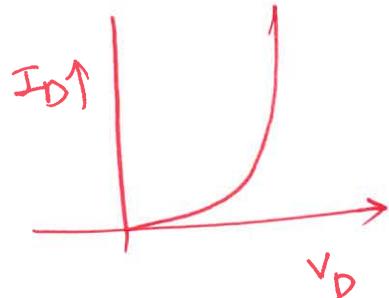
Non Linear devices:



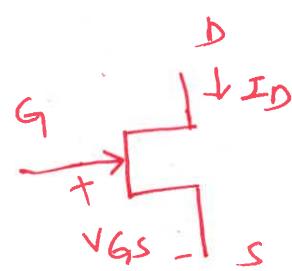
$$ID = I_S e^{\frac{VD}{VT}}$$

$$(00) \quad ID \propto e^{\frac{VD}{VT}}$$

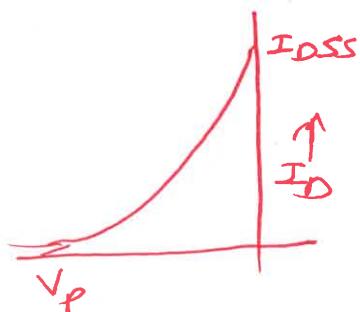
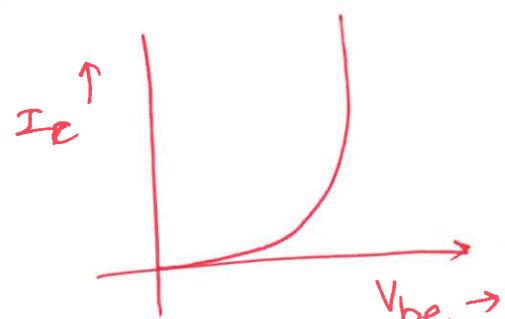
$$ID = I_0 e^{\frac{VD}{VT}}$$



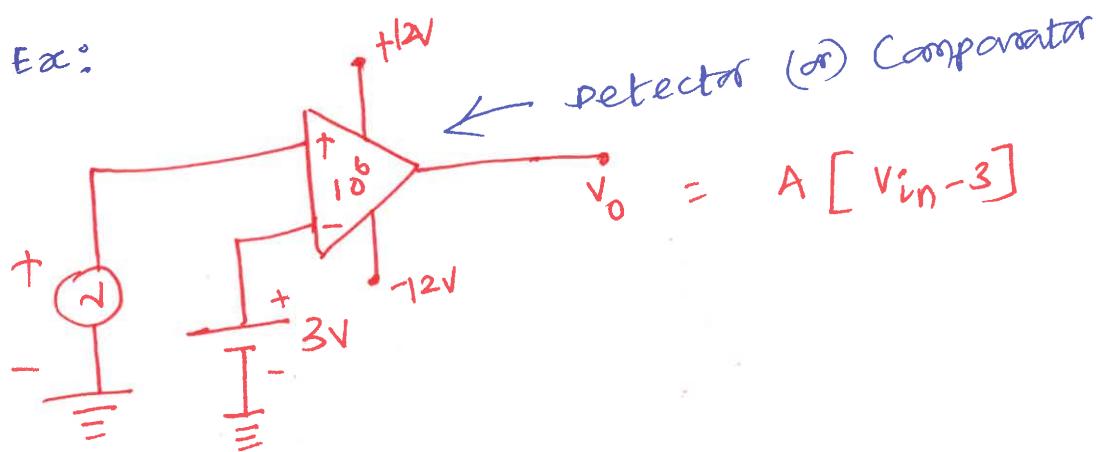
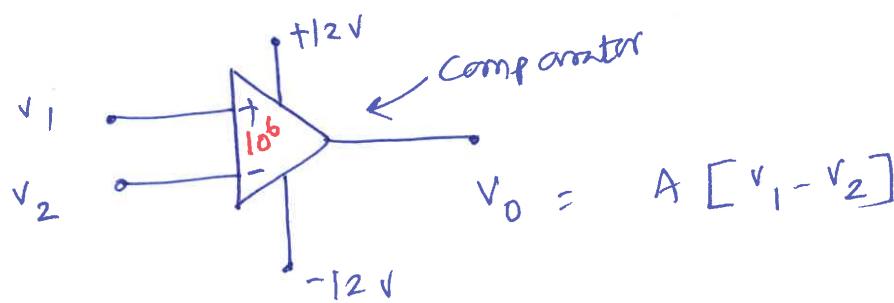
$$I_C = I_S e^{\frac{V_{BE}}{VT}}$$



$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2$$



## Op-Amp in open Loop Configuration:



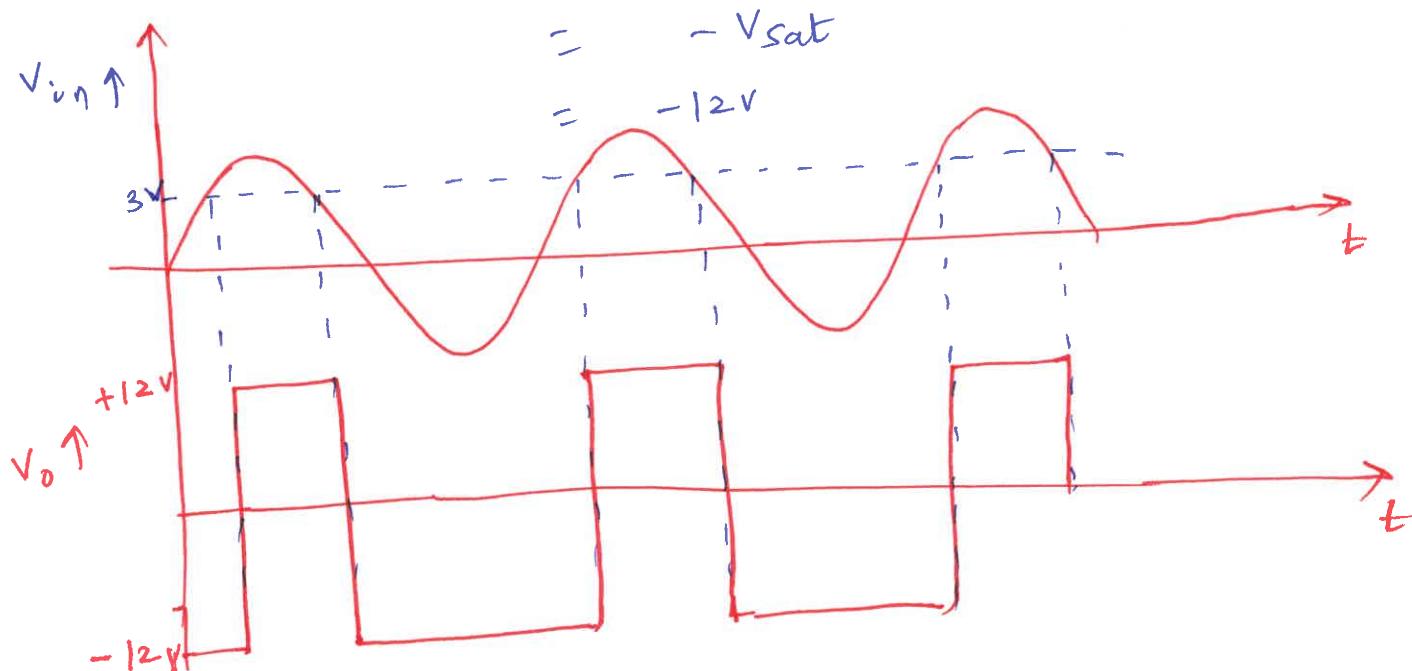
Case (1) If  $v_{in} > 3V$

$$\begin{aligned} v_o &= 10^6 [v_{in} - 3] \\ &= 10^6 [\text{positive}] = +v_{sat} \\ &= +12V \end{aligned}$$

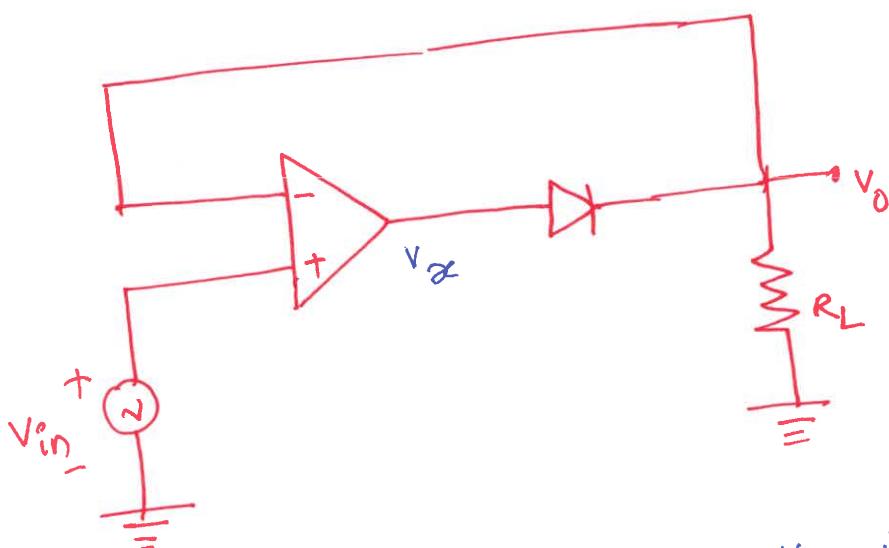
Case (2)

If  $v_{in} < 3V$

$$v_o = 10^6 [v_{in} - 3] = 10^6 [-ve] = -v_{sat}$$



Ideal Diode (OR)    PRECISION DIODE (OR)    SUPER DIODE



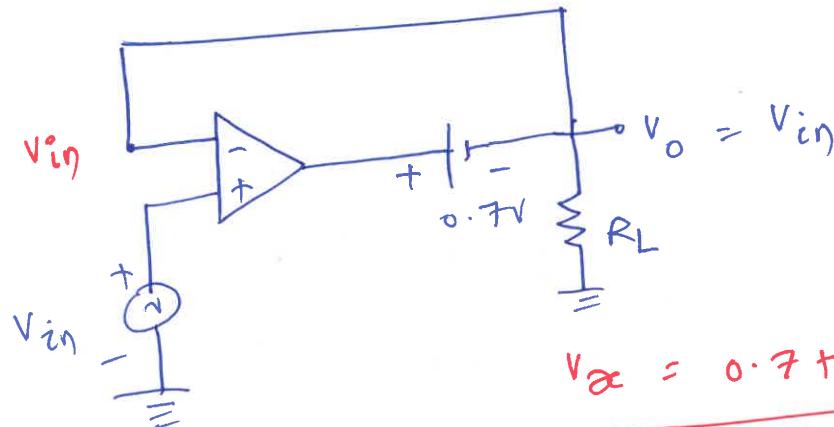
Case (i)

$V_{in} > 0V \rightarrow V_{ac}$  is positive

→ Diode is in forward biased

→ virtual ground ( $\approx$ ) short

↓



$$V_{ac} = 0.7 + V_{in}$$

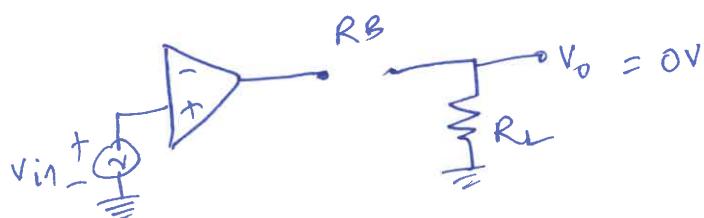
$$\boxed{V_{ac} = V_{in} + 0.7}$$

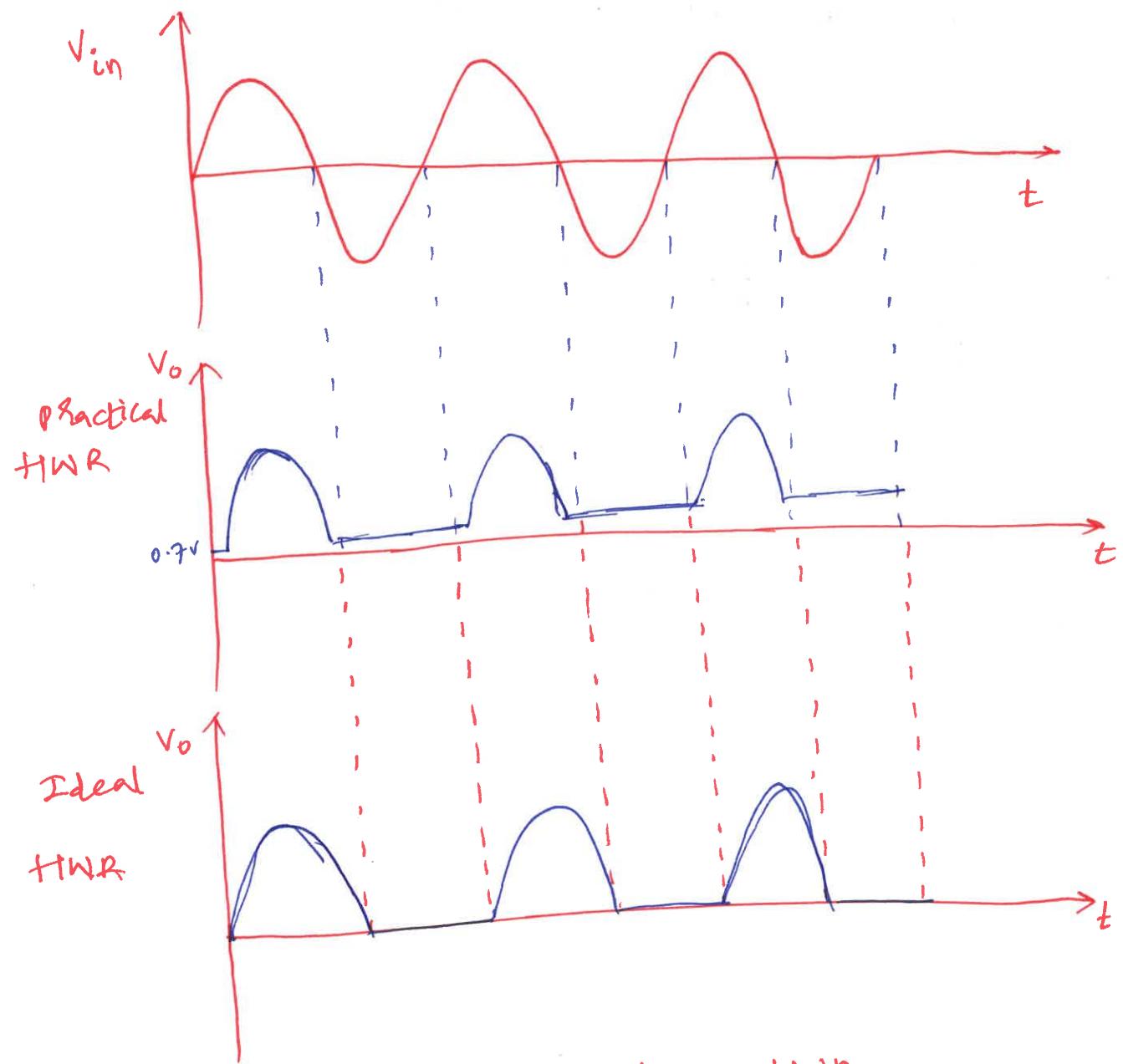
case (2)

$V_{in} < 0V \rightarrow V_{ac}$  is -ve

→ open loop

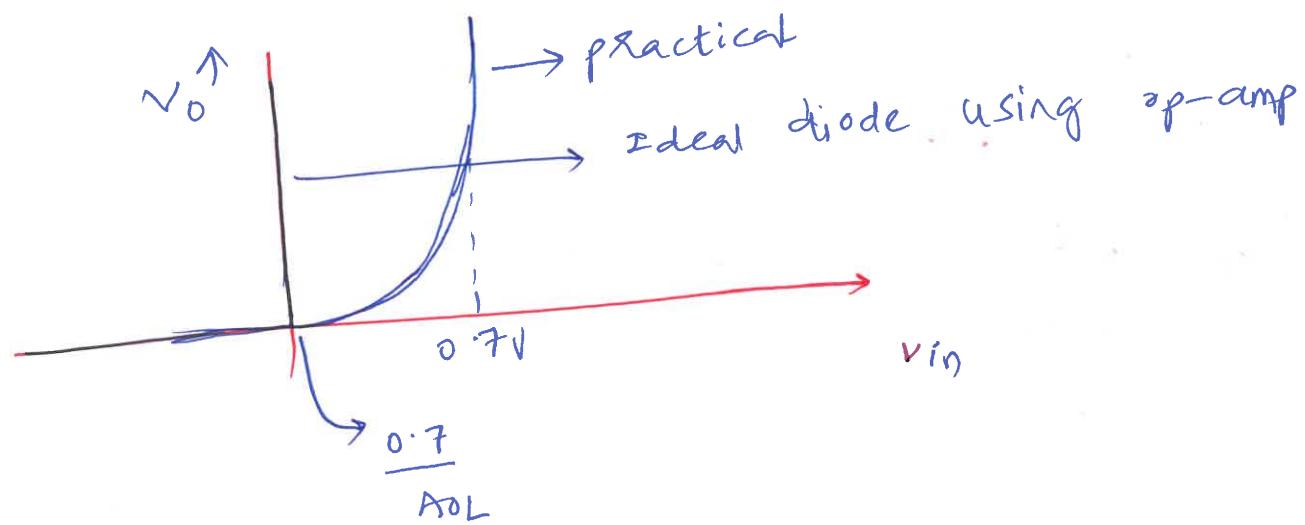
→ Diode is in R.B



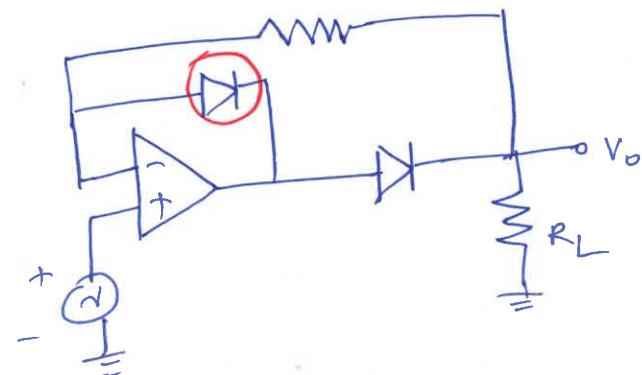


- \* CKT acts as a ideal HWR
- It does not wait for input to become  $0.7V$
- It rectifies voltages greater than  $(\frac{0.7V}{106})$

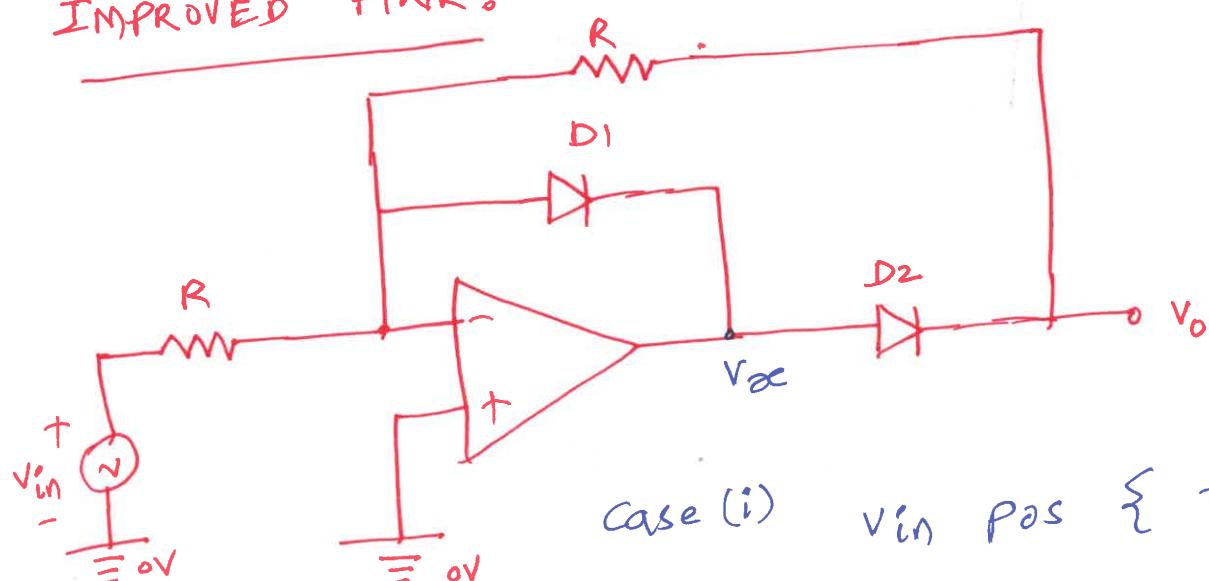
NOTE: These CKTs can rectify all voltages  $V_{in}$  slightly greater than  $(\frac{0.7}{A_{OL}})$  typically  $(1mV)$ .



Note: op-amp will continuously be in saturation and linear region due to which we get spikes at the output. To avoid this, we can connect one more diode to keep op-amp continuously in a -ve FB.



IMPROVED HWR:

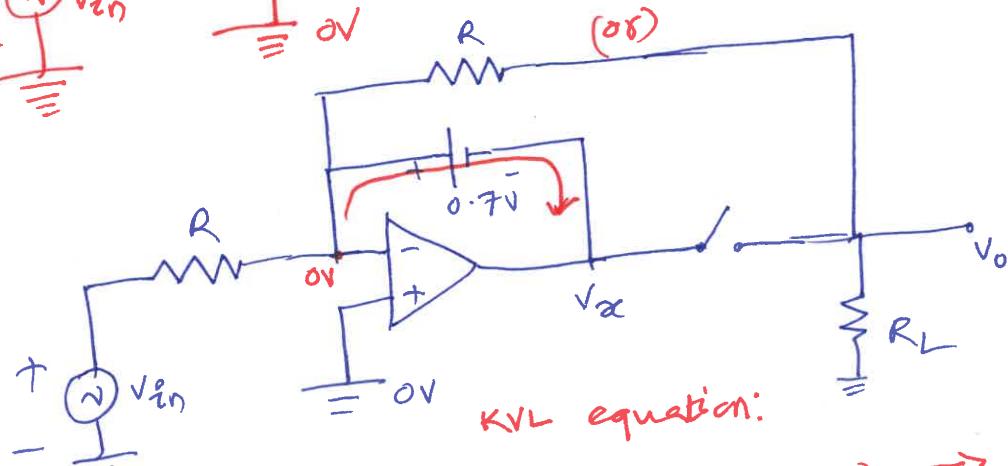
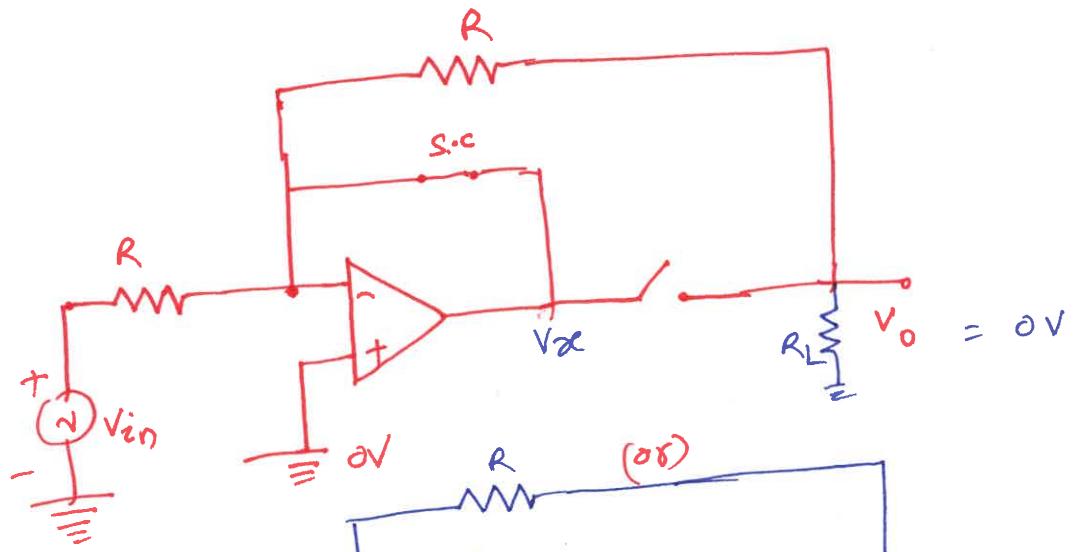


Case (i)

$V_{in}$  pos { +ve half cycle }

$V_{oe}$  negative

D<sub>1</sub> FB }  
D<sub>2</sub> R<sub>B</sub> }



KVL equation:

$$-0 + 0.7 + v_{ae} = 0 \Rightarrow v_{ae} = -0.7V$$

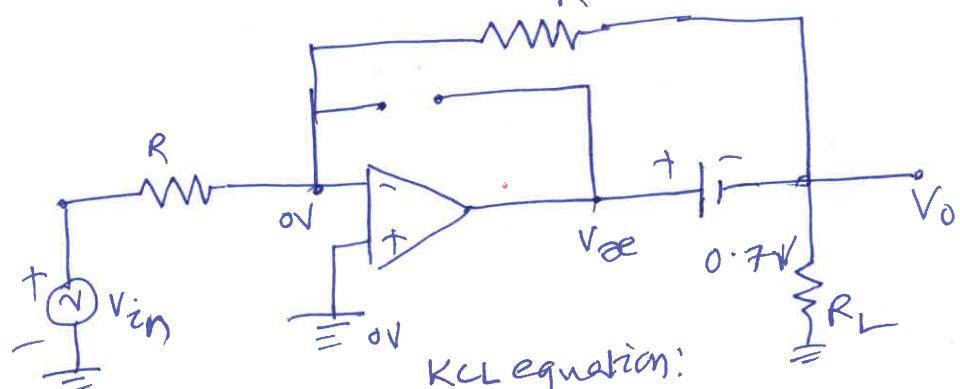
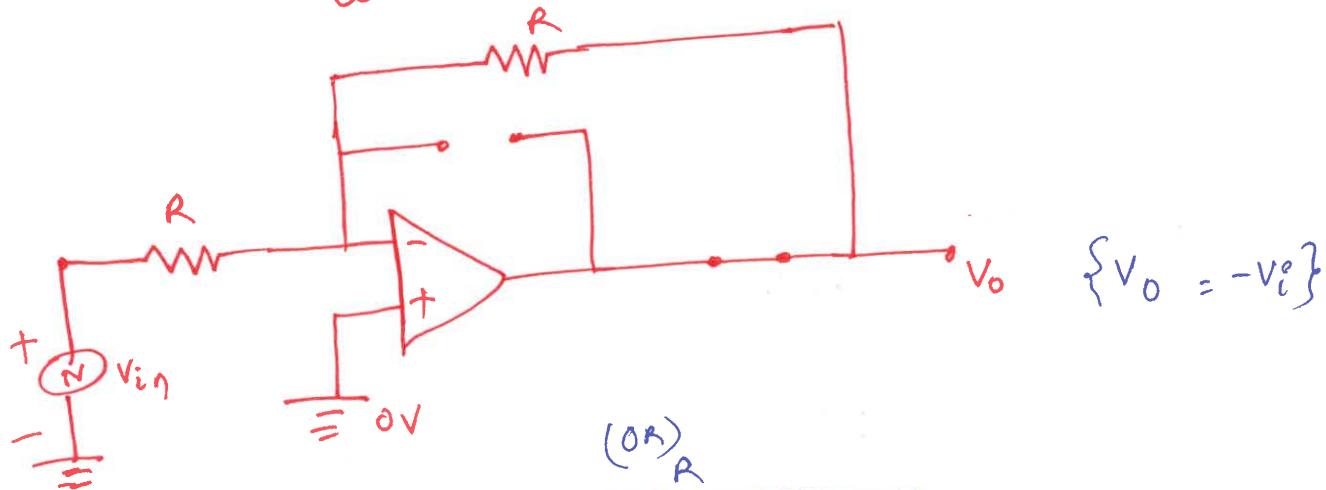
$$\boxed{v_{ae} = -0.7V}$$

case(ii)

$v_{in}$  -ve }  $v_{ae}$  +ve }

D<sub>2</sub> FB

D<sub>1</sub> RB



KCL equation:

$$\frac{0 - V_{in}}{R} + \frac{0 - V_o}{R} = 0$$

$$\therefore V_o = -V_{in} \quad (\text{phase shifted})$$

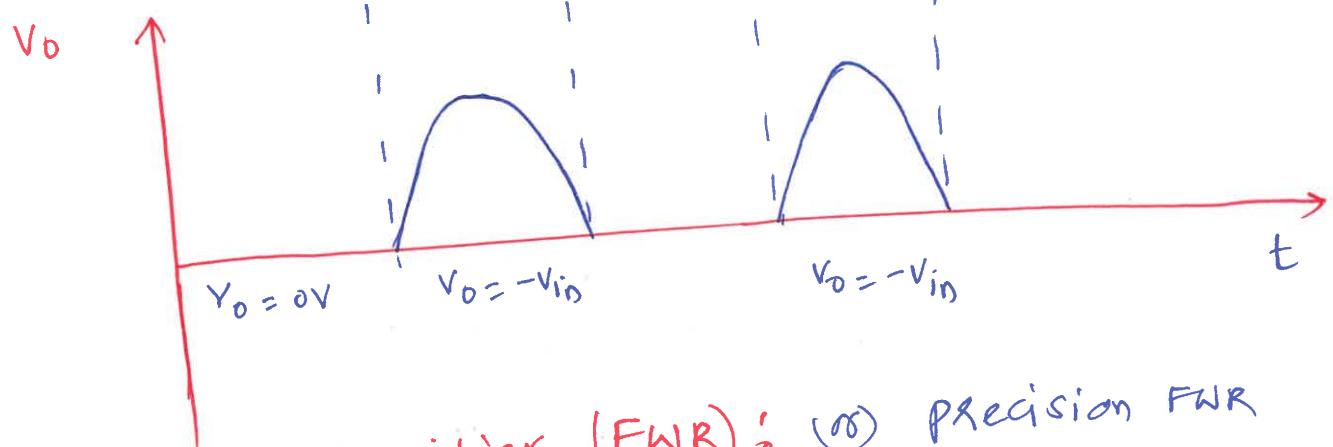
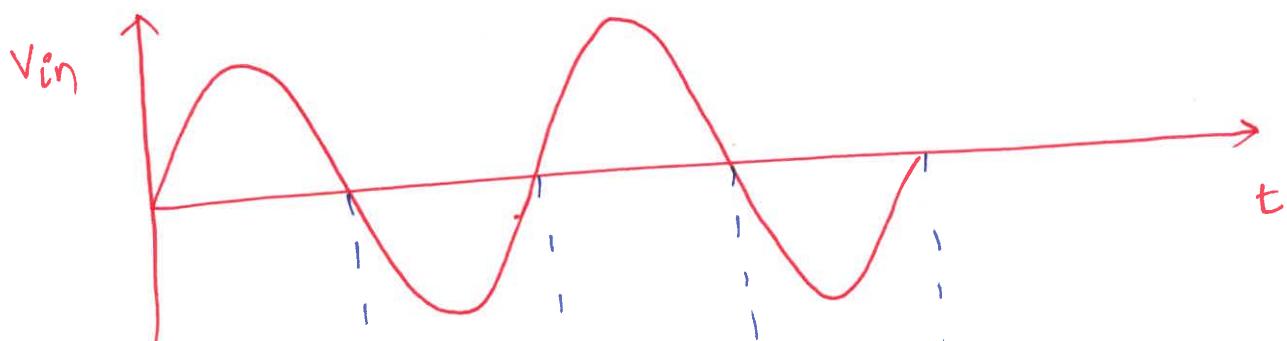
KVL equation:

$$-V_{ae} + 0 \cdot 7 + V_o = 0$$

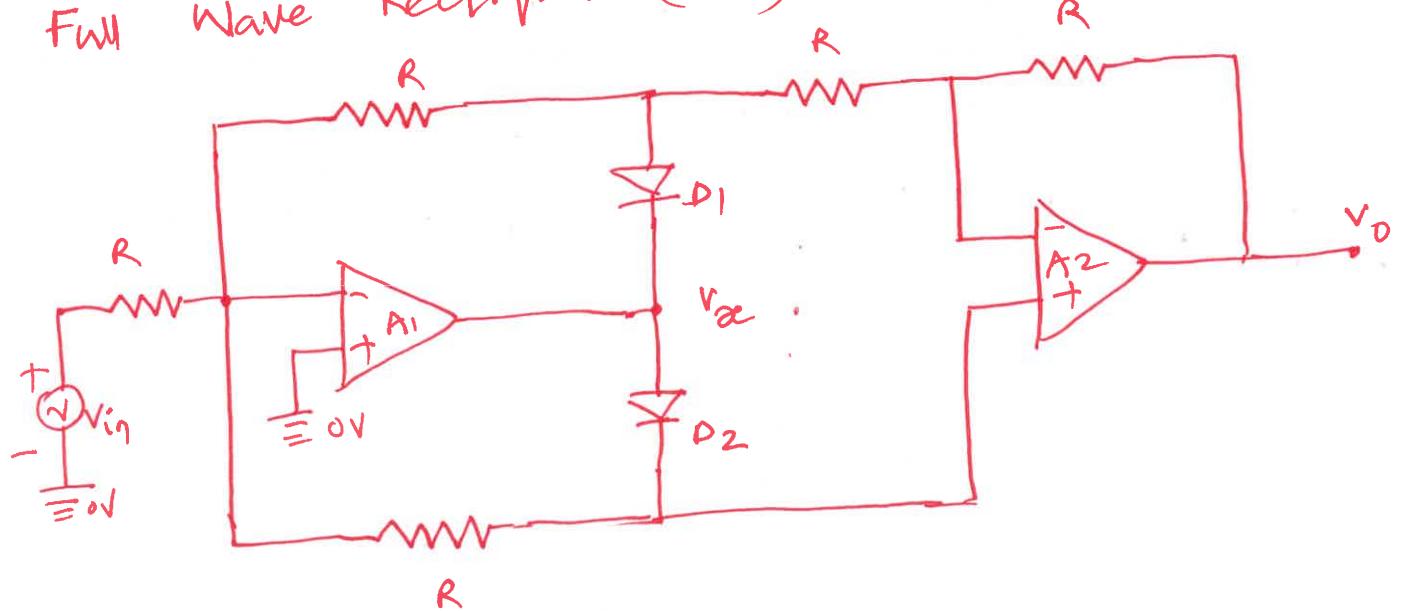
$$V_{ae} = V_o + 0 \cdot 7$$

$$= -V_{in} + 0 \cdot 7$$

$$\boxed{V_{ae} = 0 \cdot 7 - V_{in}}$$



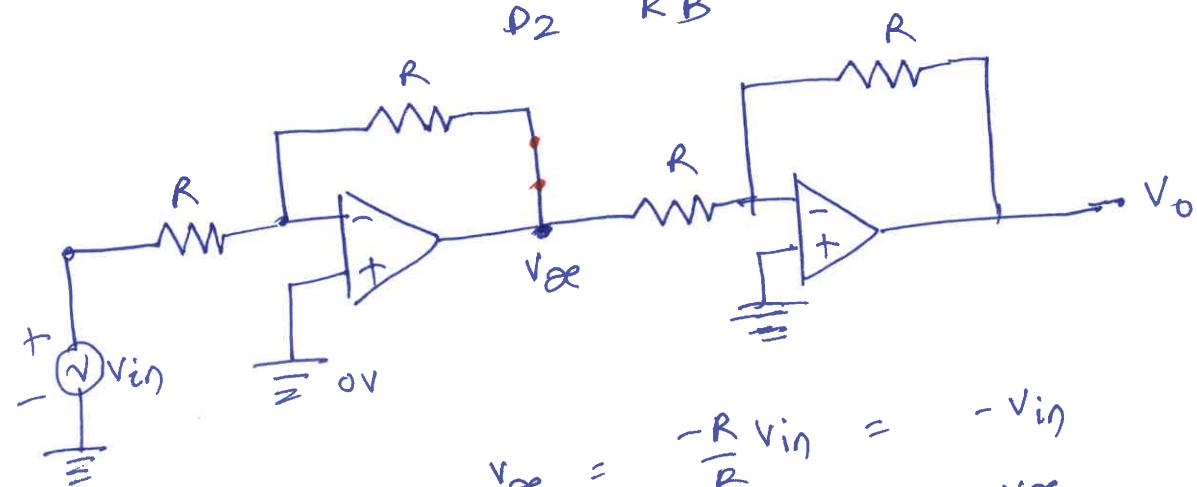
FULL Wave Rectifier (FWR) : (v) precision FWR



Case(i)  $V_{in} \rightarrow +ve$  half cycle (+ve) (as)  $V_{in} > 0V$

$$v_{oe} \rightarrow -ve$$

$\therefore D_1$  FB  
 $D_2$  RB



$$v_{oe} = -\frac{R}{R} V_{in} = -V_{in}$$

$$V_o = -\frac{R}{R} \times (-V_{in})$$

$$\boxed{V_o = V_{in}}$$

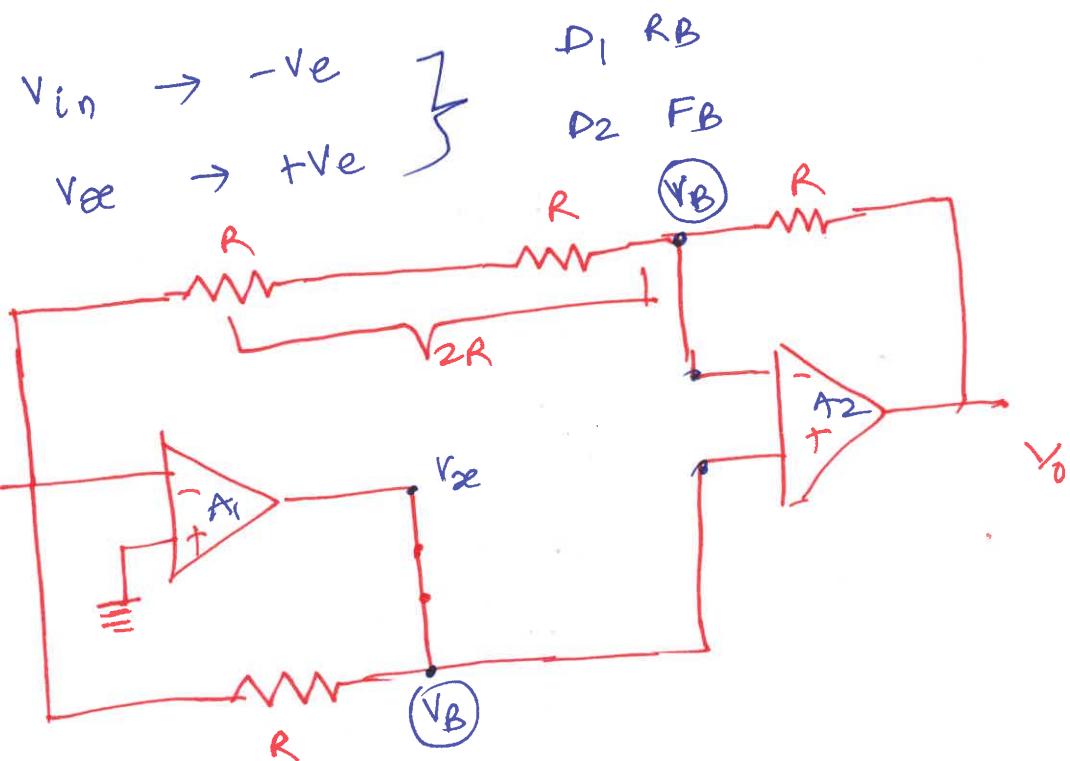
Case(ii)

$$V_{in} \rightarrow -ve$$

$$v_{oe} \rightarrow +ve$$

$D_1$  RB

$D_2$  FB



Writing KCL equation.

$$\frac{0 - V_{in}}{R} + \frac{0 - V_B}{R} + \frac{0 - V_B}{2R} = 0$$

$$-\frac{V_{in}}{R} - \frac{3V_B}{2R} = 0 \quad \frac{3V_B}{2R} = -\frac{V_{in}}{R}$$

$$\boxed{V_B = -\frac{2}{3}V_{in}}$$

Writing KCL at node  $V_B$ .

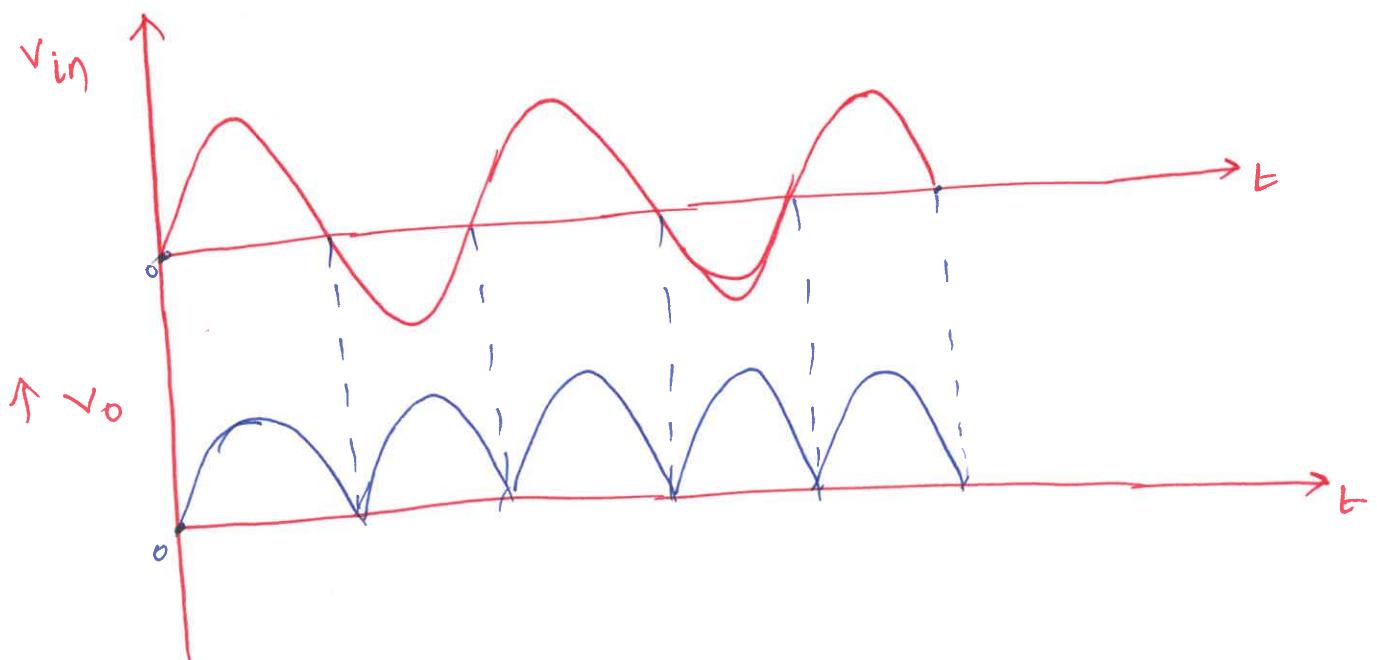
$$\frac{V_B - 0}{2R} + \frac{V_B - V_0}{R} = 0$$

$$\frac{V_B}{2R} + \frac{V_B}{R} = \frac{V_0}{R} \Rightarrow \frac{3V_B}{2R} = \frac{V_0}{R}$$

$$V_0 = \frac{3}{2}V_B$$

$$V_0 = \frac{3}{2} \times -\frac{2}{3}V_{in} = -V_{in}$$

$$V_0 = -V_{in} \text{ (phase shifter)}$$





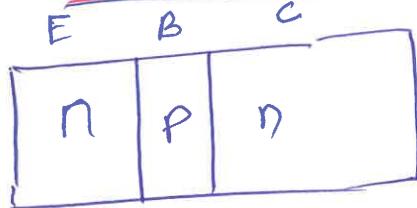
# BJT : Bipolar junction Transistor

Sudhakar Busi

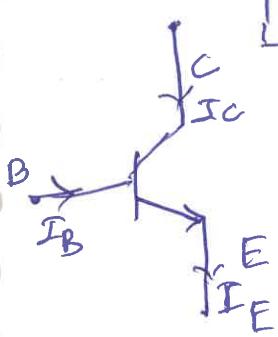
M.Tech

(Microelectronics)

0



For npn transistor



According to KCL

Sum of leaving currents

= Sum of entering currents

(or)

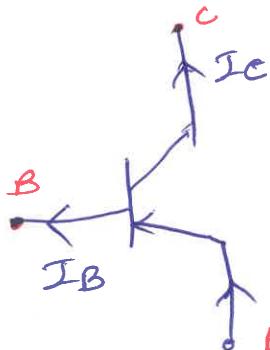
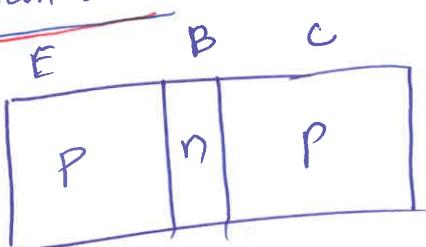
Sum of entering currents

= Sum of leaving currents.

$$I_B + I_C = I_E$$

$$I_E = I_B + \beta I_B \\ = (1 + \beta) I_B$$

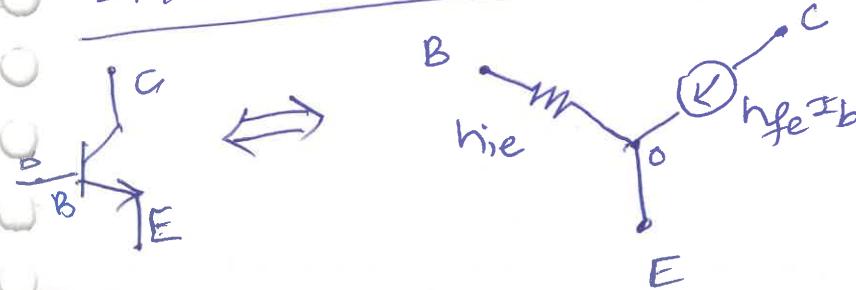
\* For PNP transistor



As per KCL

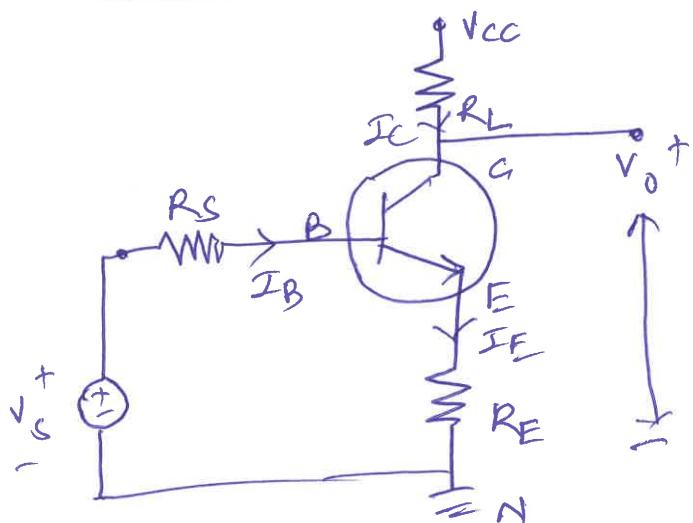
$$I_E + I_B + I_C = 0$$

Small signal model of npn BJT:

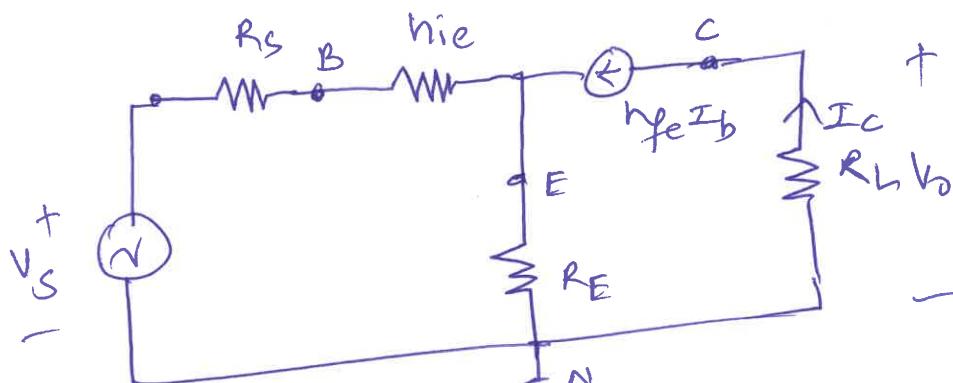


$$Th_{fe} = \beta$$

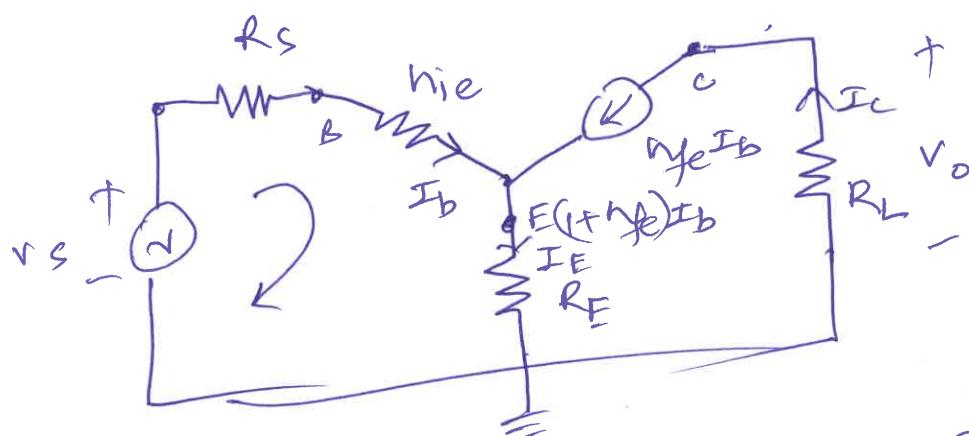
## Common Emitter with $R_E$ :



For applying small signal analysis of BJT, all D.C sources should be grounded  
(a) connected to Gnd



$$V_0 = -I_c R_L$$



$$h_{fe}(ss) + B$$

Writing KVL around loop 1

$$-V_s + R_S I_b + h_{ie} I_b + ((1+h_f) I_b) R_E = 0$$

$$V_s = (R_S + h_{ie} + (1+h_f) R_E) I_b$$

$$I_c = h_{fe} I_b$$

Total flowing Current in Emitter Resistor

$$I_b + h_{fe} I_b = I_E$$

$$(KCL)$$

$$(1+h_f) I_b$$

(2)

$$\text{Voltage gain } (A_v) = \frac{V_o}{V_s} = \frac{-I_c R_L}{V_s}$$

$$I_c = h_{fe} I_b$$

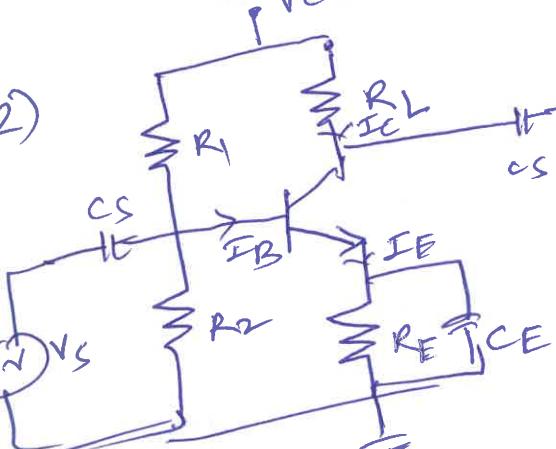
$$= \frac{-h_{fe} I_b R_L}{(R_S + r_{ie} + (1+h_{fe}) R_E) I_b}$$

$$A_v = \frac{-h_{fe} R_L}{R_S + r_{ie} + (1+h_{fe}) R_E}$$

As  $R_E \uparrow$  then  $A_v \downarrow$

$$\text{If } R_S = 0 \Rightarrow A_v = \frac{-h_{fe} R_L}{r_{ie} + (1+h_{fe}) R_E}$$

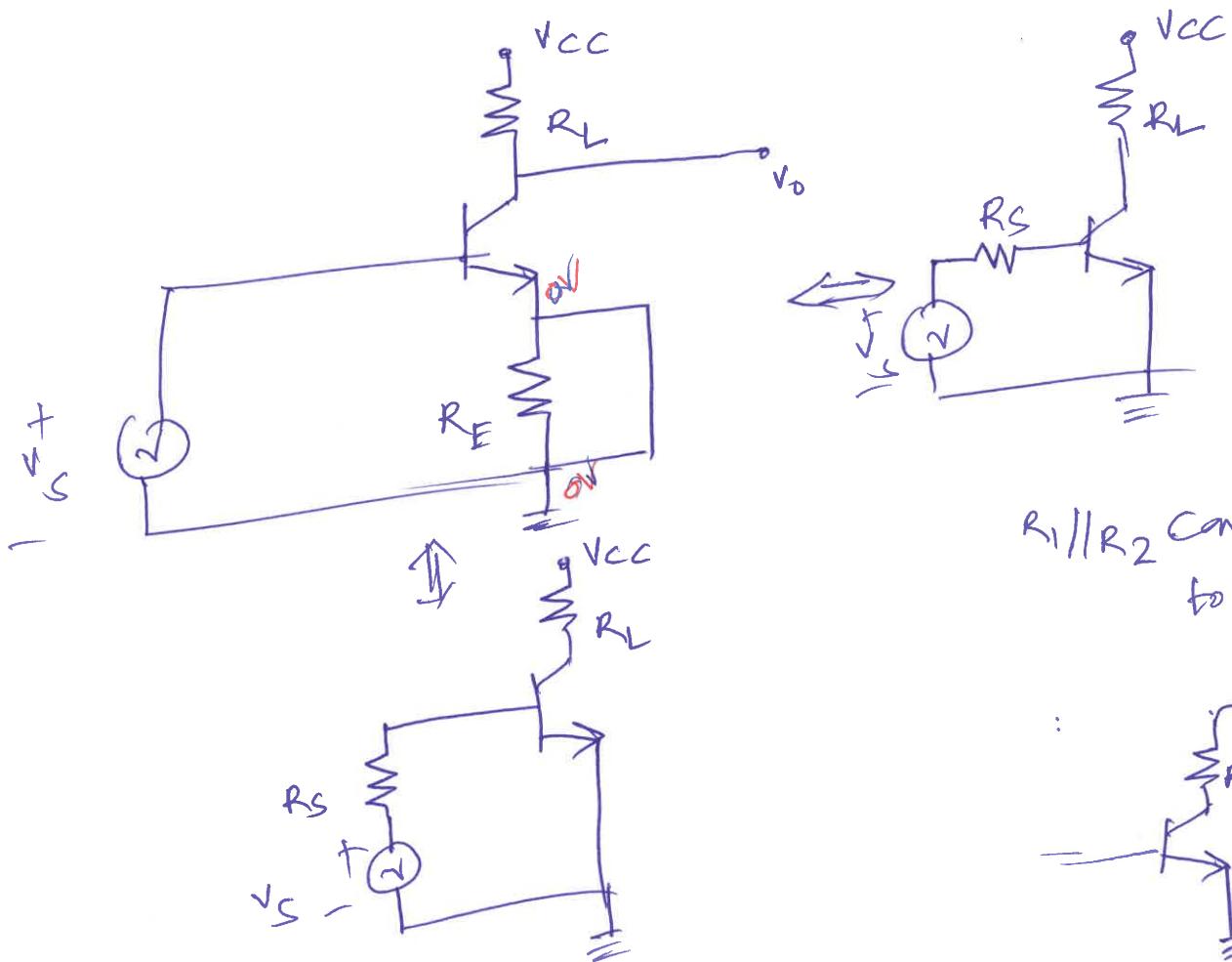
-ve sign indicates  $180^\circ$  phase shift between input and output.



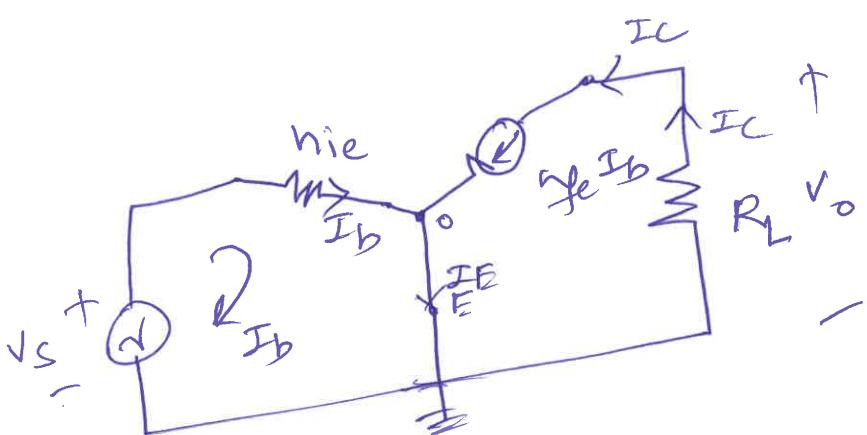
(1) what is the small signal voltage gain  $A_v = \frac{V_o}{V_s}$

(Find at high frequency)

## Small Signal analysis:



## Applying Small signal analysis :



$$I_C = h_F I_B$$

$$V_O = -I_C R_L$$

Applying KVL around loop (1)  
 $-V_S + h_{ie} I_B = 0$

$$V_S = +h_{ie} I_B$$

(3)

$$\text{Voltage gain } \left( \frac{V_o}{V_s} \right) = A_v = \frac{-I_c R_L}{h_{ie} I_b}$$

↓

$$= -\frac{h_{fe} I_b R_L}{h_{ie} I_b}$$

$$= -\frac{h_{fe} R_L}{h_{ie}}$$

$$\therefore \boxed{\frac{h_{fe}}{h_{ie}} = g_m} \quad \text{transconductance}$$

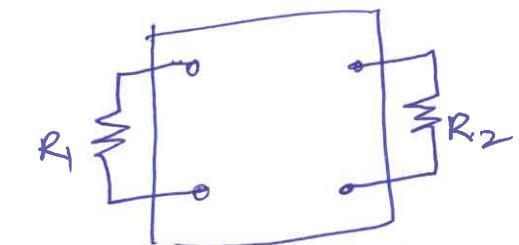
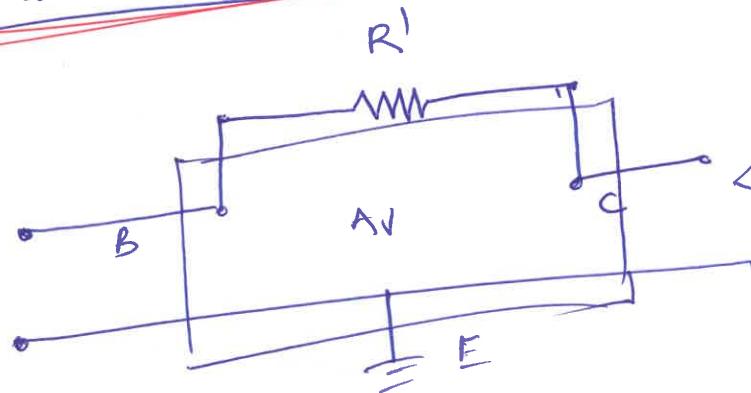
$$= -g_m R_L$$

(or)

$$g_m = \frac{I_c}{V_T}$$

\* Miller resistance:

Miller is the open



$$v_1 \xrightarrow{I_1} R' \xrightarrow{} v_2$$

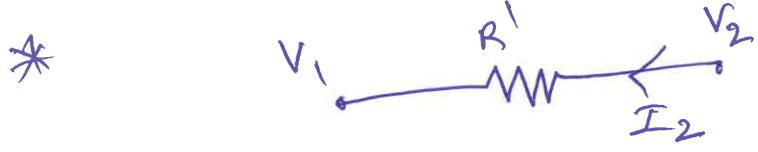
$$I_1 = \frac{v_1 - v_2}{R'} =$$

$$\frac{v_1 \left[ 1 - \frac{v_2}{v_1} \right]}{R'}$$

$$A_v = \frac{v_2}{v_1}$$

$$I_1 = \frac{v_1 \left[ 1 - A_v \right]}{R'}$$

$$*\frac{V_1}{I_1} = R_1 = \frac{R'}{1 - A_v}$$



$$I_2 = \frac{V_2 - V_1}{R'}$$

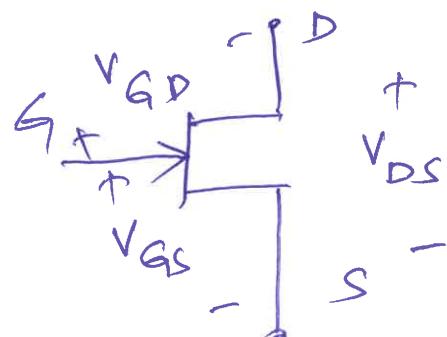
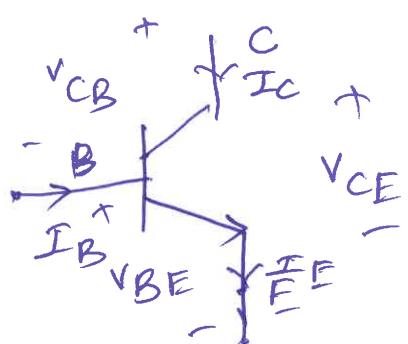
$$I_2 = \frac{V_2 \left[ 1 - \frac{V_1}{V_2} \right]}{R'}$$

$$I_2 = \frac{V_2 \left[ 1 - \frac{1}{A_v} \right]}{R'}$$

\*

$$\frac{V_2}{I_2} = R_2 = \frac{R'}{1 - \frac{1}{A_v}} = \frac{R'(A_v)}{(A_v - 1)}$$

\* Relevance of BJT and JFET:



Apply KVL:

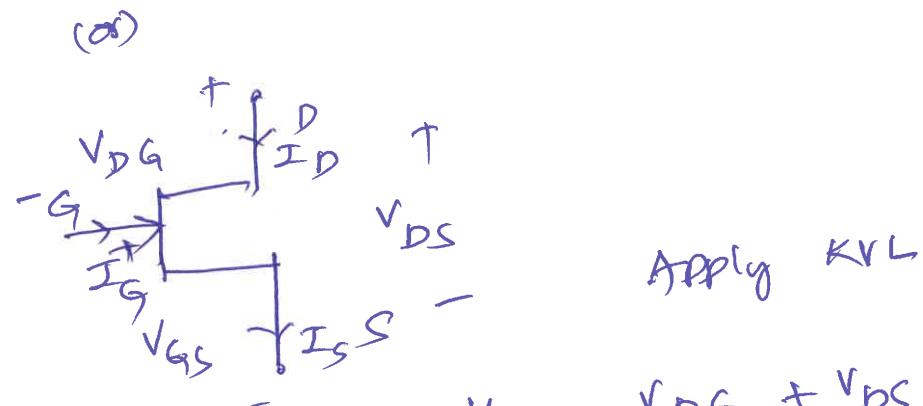
$$-V_{BE} - r_{CB} + V_{CE} = 0$$

$$V_{CE} = V_{CB} + V_{BE}$$

Apply KVL

$$-V_{GS} + V_{GD} + V_{DS} = 0$$

$$V_{DS} = V_{GS} - V_{GD}$$



Apply KVL

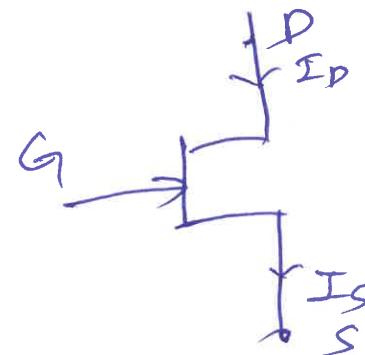
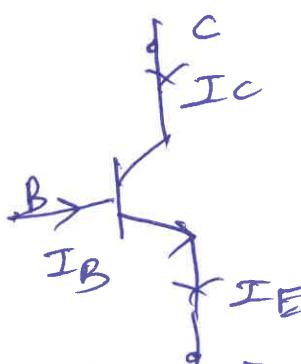
$$-V_{GS} - V_{DG} + V_{DS} = 0$$

$$V_{DS} = V_{DG} + V_{GS}$$

$V_{DS}$  means Voltage difference between Drain and Source

Drain and Source

$$V_{DS} = V_D - V_S$$



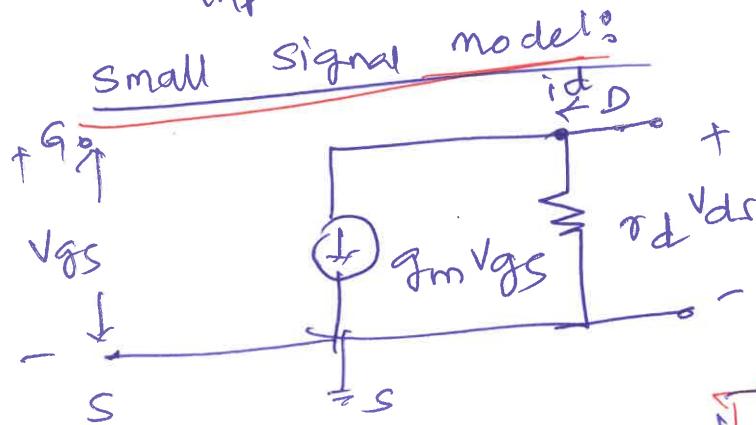
\* Base is equivalent to Gate ( $B = G$ )

\* Collector is equivalent to Drain ( $C = D$ )

\* Emitter is equivalent to Source ( $E = S$ )

## Small signal model of JFET

\* In JFET Gate junction is reverse biased means open circled and  $I_{G20}$  (and) high input resistance.



Apply KCL at outer node  
sum of entering currents  
= sum of leaving currents

$$i_d = g_m v_{gs} + \frac{v_{ds}}{r_d}$$

Resistance:

h-parameter model

$$v_{be} = h_{ie} i_b + h_{re} v_{ce}$$

$$i_c = h_{fe} i_b + h_{oe} v_{ce}$$

} CE model

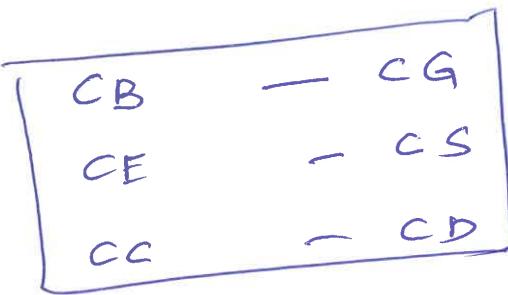
current controlled current source (CCCS)

$$\text{JFET: } i_d = g_m v_{gs} + \frac{1}{r_d} v_{ds}$$

Voltage controlled current source (VCCS)

BJT: Current controlled current source device (CCCS)

FET: Voltage controlled current source device (VCCS)



$$i_d = g_m v_{gs} + \frac{v_{ds}}{r_d}$$

$g_m$  = (transconductance) =  $\frac{i_d}{v_{gs}} \Big|_{v_{ds}=0}$

①

\*

In BJT

$$\text{h}_{fe} = \frac{i_c}{i_b}$$

voltage  
current gain

( $i_d$  is controlled by  $v_{gs}$ )

( $h_{fe(0)}$   
 $\beta$ )

$r_d$  = drain resistance =  $\frac{v_{ds}}{i_d} \Big|_{v_{gs}=0}$

②

\*

$$\mu = \text{amplification factor} = g_m r_d = \frac{v_{ds}}{v_{gs}}$$

③

\*

Junction Field Effect Transistor:

JFET:

$$i_D \uparrow$$

Active (on)  
Linear (on)  
Ohmic  
Regime

Non Linear  
(off)  
Saturation Region

Breakdown  
Region.

$$I_D = I_{DSS} \left( 1 - \frac{v_{gs}}{V_p} \right)^n$$

$$v_{DS} \rightarrow$$

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

Drain current is controlled by  $V_{GS}$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{i_d}{V_{GS}}$$

Differentiate w.r.t  $V_{GS}$

$$\frac{\partial I_D}{\partial V_{GS}} = I_{DSS}^2 \cdot 2 \left( 1 - \frac{V_{GS}}{V_P} \right) \times \left( -\frac{1}{V_P} \right)$$

$$g_m = - \frac{2 I_{DSS}}{V_P} \left( 1 - \frac{V_{GS}}{V_P} \right)$$

As  $V_{GS} \uparrow \rightarrow g_m \uparrow$

$V_P$  = pinch off voltage  
decided by manufacturer

$$\therefore g_m = g_{m0} \left( 1 - \frac{V_{GS}}{V_P} \right)$$

$$g_{m0} = \frac{-2 I_{DSS}}{V_P}$$

$$g_m = \frac{-2 I_{DSS}}{V_P} \frac{I_D}{I_{DSS}}$$

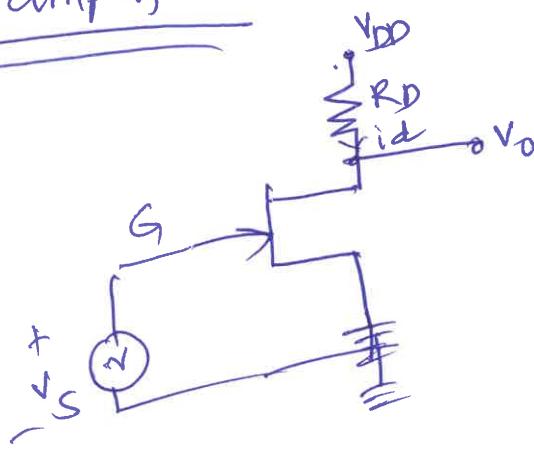
(G)

$$g_m = \frac{2}{|V_p|} \quad \boxed{I_{DS} \quad I_{DSS}}$$

$$g_m = \frac{2}{|V_p|} \quad \boxed{I_{DS} \quad I_{DSS}}$$

\* Impedance derivations

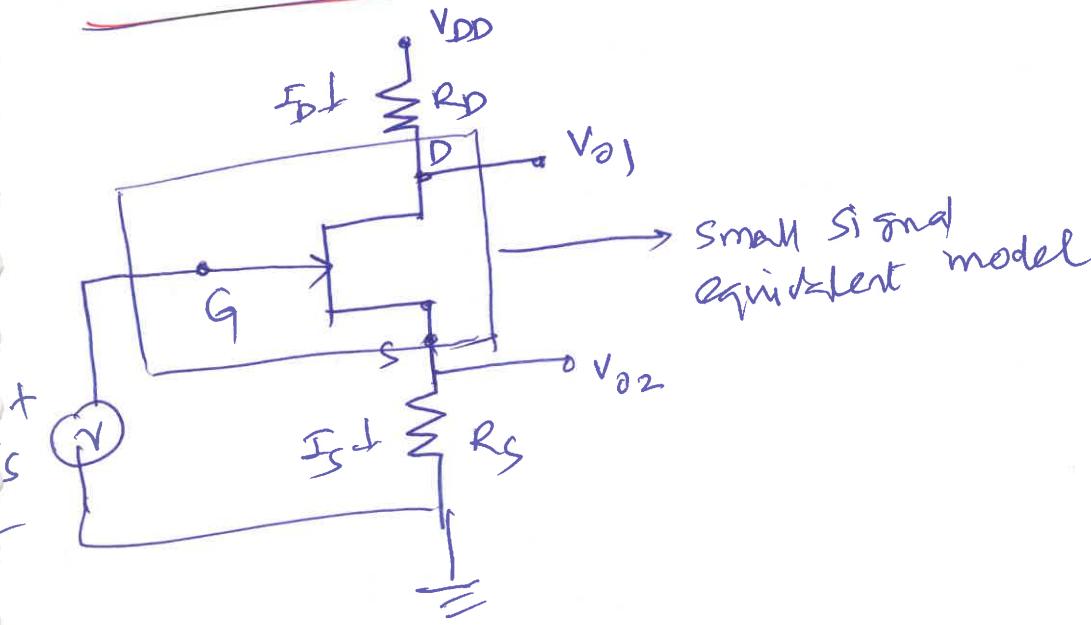
CS amplifier:

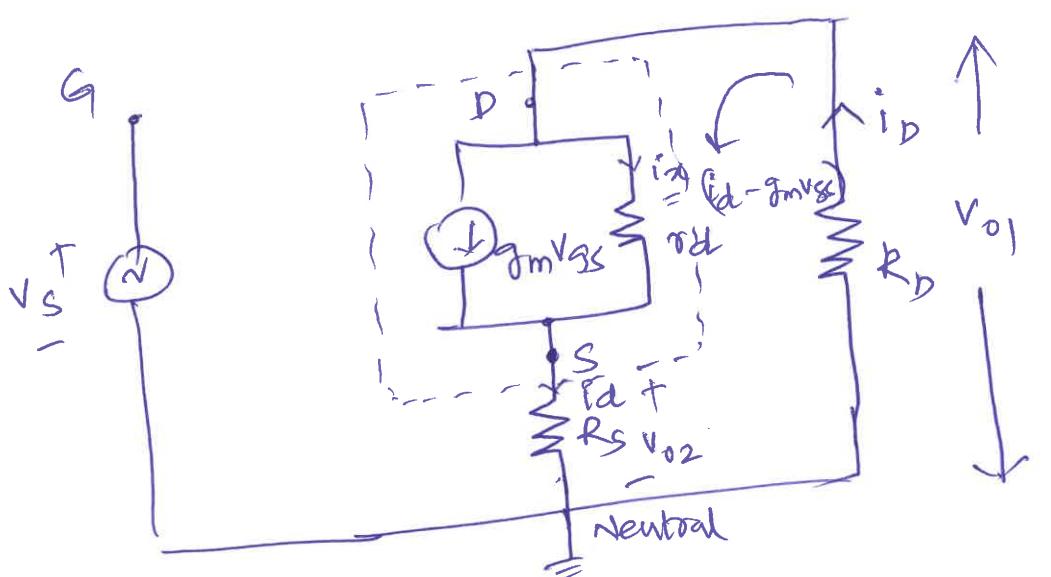


Source must be grounded

$$V_o = -i_d R_D$$

Common Source and Common Drain amplifier:





For Small Signal analysis is all DC  
Supplies are connected to ground

$$V_{O1} = -i_D R_D \rightarrow 180^\circ \text{ phase shift like CE}$$

$$V_{O2} = i_D R_S$$

Writing KVL at the output side

$$i_D R_D + (i_D - g_m V_{GS}) r_d + i_D R_S = 0$$

$$V_{GS} = \cancel{g_m V_S} = V_S - i_D R_S$$

$$\text{We know } \mu = g_m r_d$$

$$i_D R_D + [i_D - g_m (V_S - i_D R_S)] r_d + i_D R_S = 0$$

$$i_D [R_D + r_d + g_m r_d R_S + R_S] = g_m V_S r_d$$

$$i_D [R_D + r_d + \mu R_S + R_S] = g_m V_S r_d$$

$$i_D = \frac{\mu V_S}{R_D + r_d + R_S(1 + \mu)}$$

$$\begin{aligned} i_A + g_m V_{GS} &= i_D \\ (i_A = i_D - g_m V_{GS}) & \end{aligned}$$

$$i_A = i_D - g_m V_{GS}$$

$$\begin{aligned} V_{GS} &= V_S - R_S \\ (V_{GS} = V_S - V_S) & \end{aligned}$$

$$i_d = \frac{M V_s}{R_d + R_D + (\mu+1)R_S}$$

(7)

CS amp:

$$V_{O1} = -i_d R_D$$

$$= \frac{-M V_s}{R_d + R_D + (\mu+1)R_S} \times R_D$$

$$\frac{V_{O1}}{V_s} = A_{CS} = \frac{-M R_D}{R_d + R_D + (\mu+1)R_S}$$

If  $R_S = 0$ 

$$A_{CS} = \frac{V_{O1}}{V_s} = \frac{-M R_D}{r_d + R_D}$$

$$= \frac{-(g_m r_d) R_D}{R_d + R_D}$$

$$= -g_m \left( \frac{r_d R_D}{R_d + R_D} \right)$$

$$A_{CS} = -g_m R_D'$$

$$R_D' = r_d || R_D$$

In BJTCE  
⇒

$$A_{CE} = \frac{-h_{FE} R_L}{h_{IE}}$$

 $\propto \frac{h_{FE} R_L}{R_{in}}$

$$\therefore A_{CS} = -g_m R_D$$

$$\frac{h_{FE}}{h_{IE}} = g_m$$

Now CD amplifier: gain

$$V_{O2} = I_d R_S$$

$$= \frac{M V_S}{r_d + R_D + (M+1)R_S} \times R_S$$

$$\frac{V_{O2}}{V_S} = A_{CD} = \frac{M R_S}{r_d + R_D + (M+1)R_S}$$

$$A_{CD} \Big|_{R_D \approx 0} = \frac{M R_S}{r_d + (M+1)R_S}$$

$$(M+1)R_S \gg r_d$$

$$\approx \frac{M R_S}{(M+1) R_S} \quad M > > 1$$

$$A_{CD} \approx 1$$

Like CC gain  
 $A_{\text{CC}} = 1$

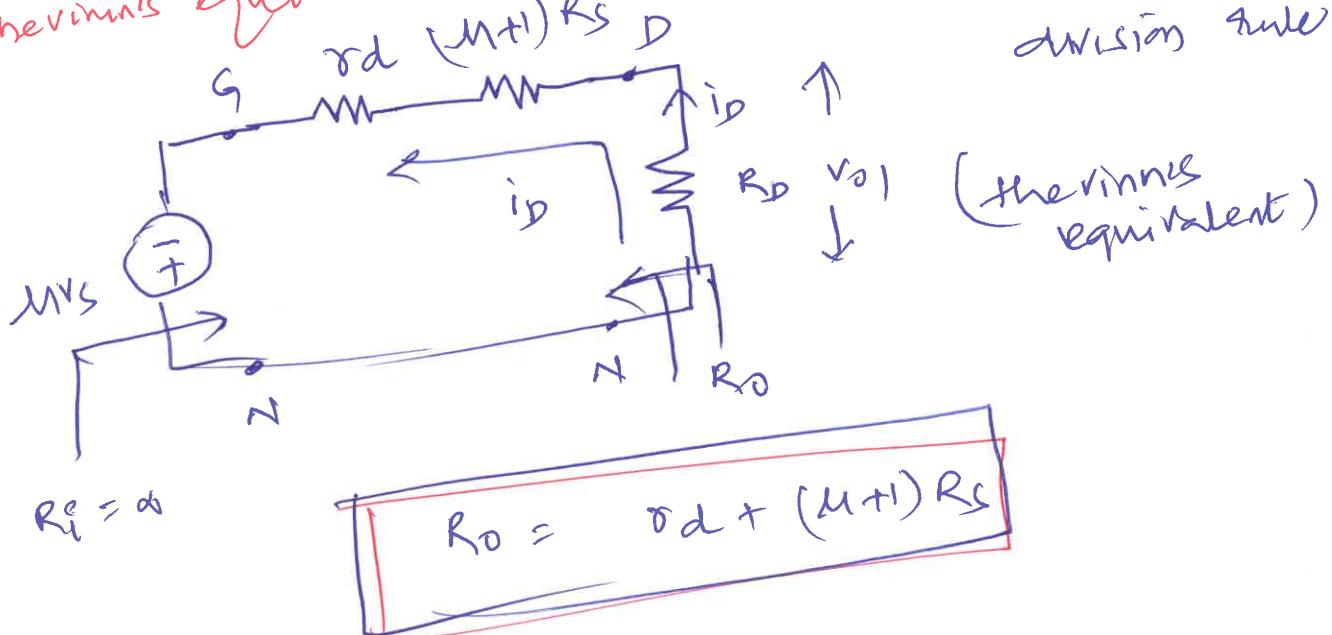
Buffer amplifier

CS amplifier: Input resistance and output resistance ( $R_i$ ) ( $R_o$ )

$[R_i = \infty]$  because Gate terminal is open & reverse biased  
 $I_G = 0$  &  $R_i = \infty$   
 $R_i = \infty$  for both CS & CD  
output resistance: ( $R_o$ )

We know  $V_{o1} = \frac{-Mv_s R_D}{r_d + R_D + (M+1)R_S}$

Thevenin's equivalent:



in CE amplifier (BJT)  
input resistance increases by  
of a factor of  $(1+h_{fe}) R_E$

In CS the op resistance increases by a factor of  $(M+1) R_S$ .

here  
 $(M = g_m r_d)$

# CD amplifier $R_i$ and $R_o$ 's

$$R_i = \infty$$

$R_o$  (output resistance)

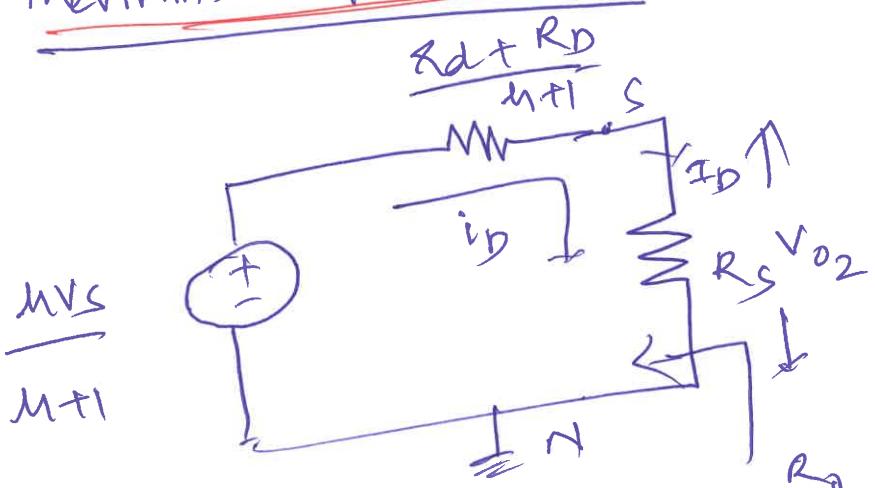
we know  $V_{o2} = i_d R_s$

$$= \frac{MvS}{r_d + R_D + (\mu + 1)R_S} R_S$$

$$= \frac{MvS}{\mu + 1} \times R_S$$

$$\frac{r_d + R_D}{\mu + 1} + R_S$$

Thevenin's equivalent:



$$\therefore R_o = \frac{r_d + R_D}{\mu + 1}$$

$R_o$ :

$$R_o (R_D = 0) = \frac{r_d}{\mu + 1} = \frac{r_d}{\mu} \quad M \gg 1$$

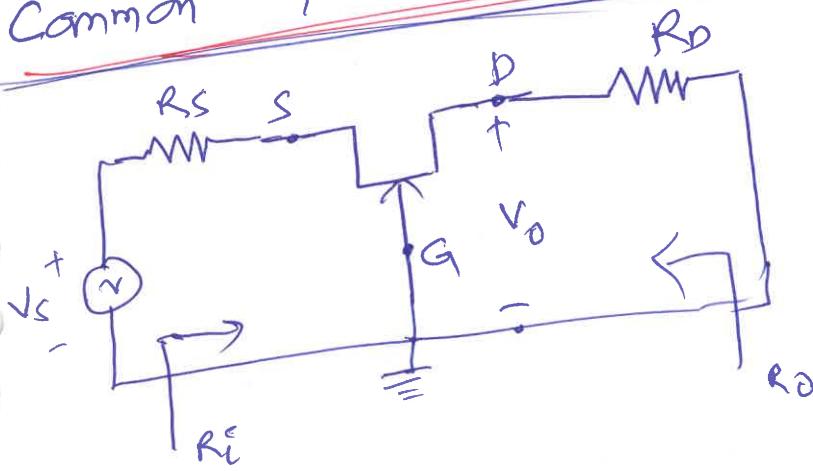
$$R_o \underset{(R_D \rightarrow 0)}{\approx} \frac{1}{g_m}$$

(9)

$$\Rightarrow * \boxed{g_o = g_m}$$

O/p Conductance of CS amplifier ( $g_o$ ) is  $= g_m$  (transconductance)

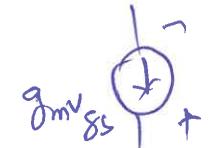
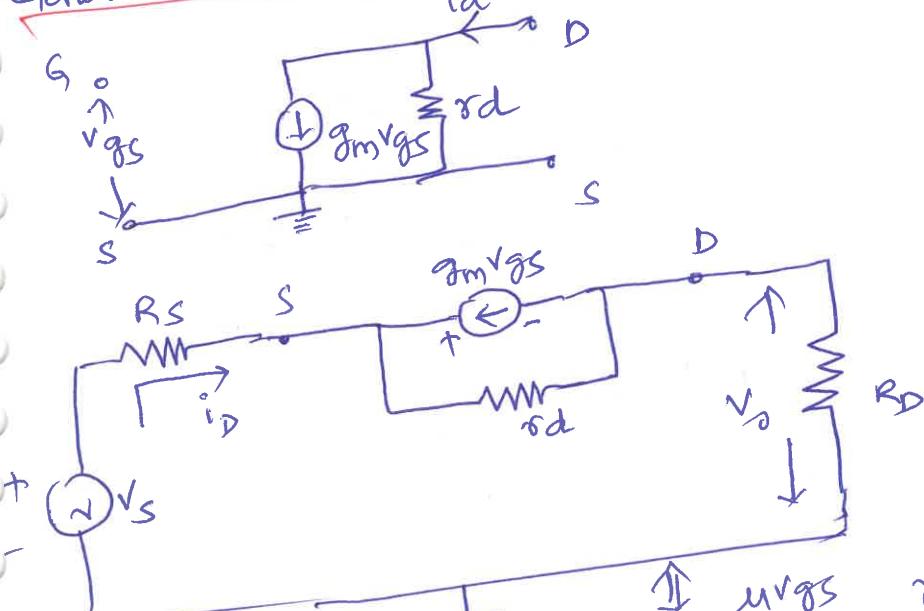
Common Gate amplifier :



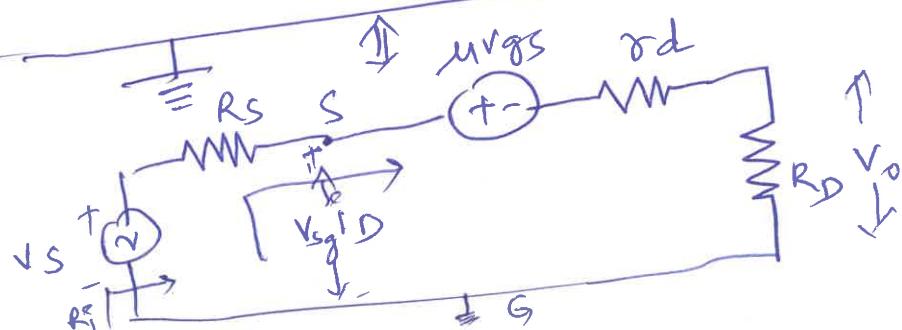
Just rotate  
we will get  
CG small signal  
model.



Generalised Small Signal model:



$$M = g_{mod}$$



$$V_o = i_D R_D$$

Writing KVL to the Loop

$$-V_S + R_S i_D + M V_{GS} + i_D \cancel{R_D} + i_D R_D = 0$$

$$V_S - M V_{GS} = i_D (R_S + r_d + R_D)$$

KVL:  $-V_S + i_D R_S + V_{SG} = 0$

$$V_{SG} = V_S - i_D R_S$$

$$V_{GS} = -[V_S - i_D R_S]$$

$$V_{GS} = -V_S + i_D R_S$$

$$\therefore V_S - M[-V_S + i_D R_S] = i_D [R_S + r_d + R_D]$$

$$V_S + M V_S - M i_D R_S = i_D [R_S + r_d + R_D]$$

$$(1+M) V_S = i_D [R_S + M R_S + r_d + R_D]$$

$$= i_D [R_S (1+M) + r_d + R_D]$$

$$i_D = \frac{(1+M) V_S}{R_S (1+M) + r_d + R_D}$$

$$\therefore V_O = i_D R_D$$

$$= \frac{(M+1)V_S}{r_d + R_D + (M+1) R_S} \times R_D$$

$$\therefore * \frac{V_o}{V_s} = A_{CG} = \frac{(M+1) R_D}{r_d + R_D + (M+1) R_S}$$

(10)

Voltage gain  
(Common gate)

$$\frac{V_o}{V_s} = A_{CG} = \frac{(1+M) R_D}{r_d + R_D + (M+1) R_S}$$

$$r_d + R_D = \frac{3.3K + 10K}{53.3K}$$

Let  
 $R_D = 10K$

$$(1+M) R_S = (1+100) 1K$$

$$= 101K$$

$$(1+M) R_S \gg r_d + R_D$$

$$\therefore \frac{V_o}{V_s} = A_{CG} \approx \frac{R_D}{R_S}$$

$(\alpha = \text{unity})$

Analogy:

$$A_{CB} = \frac{\alpha R_L}{r_e} = \frac{R_L}{r_e}$$

$r_s$  is external to FET

$r_e$  = internal to

BJT.

Common Gate  $\rightarrow$  Input Resistance  $R_{in}$

$$R_{in} = \frac{V_S}{I_D}$$

$$= \frac{(1+M)R_S + r_d + R_D}{(1+M)}$$

$$= \frac{(1+M)R_S + r_d + R_D}{(M+1)}$$

$$R_{in} = R_S + \frac{r_d + R_D}{M+1}$$

$$R_{in} \quad \text{at } R_S = 0 = \frac{r_d + R_D}{M+1}$$

$$V_{sg} = V_S$$

$$\boxed{R_{in} \quad \text{at } R_S = 0 = \frac{V_{sg}}{I_D} = \frac{r_d + R_D}{M+1}}$$

also  
CD  
output-resistance  
( $R_o$ )

Output Resistance ( $R_o$ ):

We know

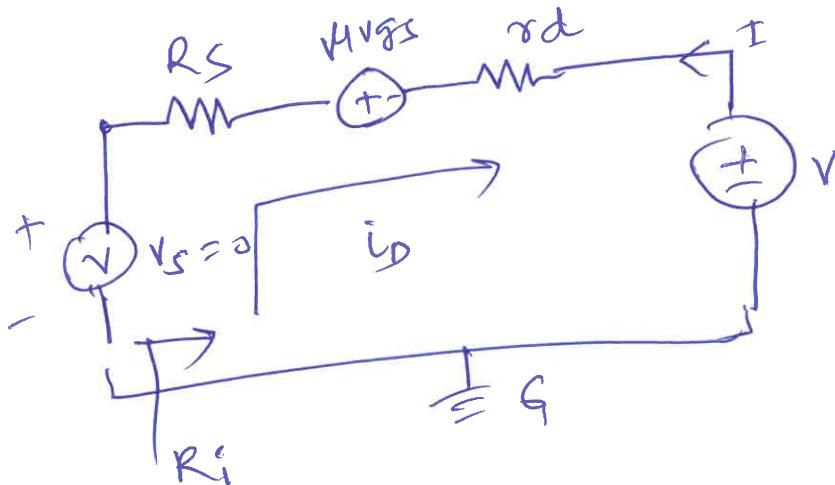
$$V_o = \frac{V_S(M+1)R_D}{(1+M)R_S + r_d + R_D}$$

Apply ' $\nabla$ ' by taking  $R_D = \infty$  (O.C.).

calc the 'I' when  $V_S = 0$

$$R_O = \frac{V}{I}$$

No load  
Test source  
(V)  
and current  
(I)



$$V + \mu V_{GS} = i(C(R_s + r_d))$$

(or)

write KVL

$$R_s i_D + \mu V_{GS} + r_d i_D + V = 0$$

$$V + \mu V_{GS} = i(C(R_s + r_d))$$

We know  $V_{GS} = -V_S + i_D R_s$

$$\begin{aligned} V_{GS} &= \epsilon_D R_s \\ &= -I R_s \end{aligned}$$

Since  
 $V_S = 0$

$$i_D = -I$$

$$V + \mu(-I R_s) = I(R_s + r_d)$$

$$\boxed{\frac{V}{I} = R_O = r_d + (\mu + 1) R_s}$$

also  
CS O/P  
resistance

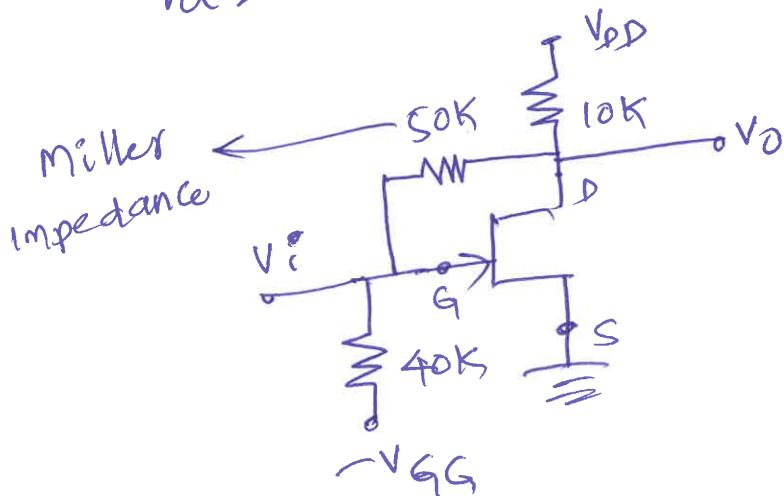
CD: Voltage Series F/B amp      C Collected

CS: current series       $\rightarrow$  Common Emitter.

Imp\* If the input signal  $V_i$  is impressed between Gate and ground. Find the amplification

$\frac{V_o}{V_i}$ ,  $A_v = \frac{V_o}{V_i}$ . parameters are  $\mu = 30$ ,

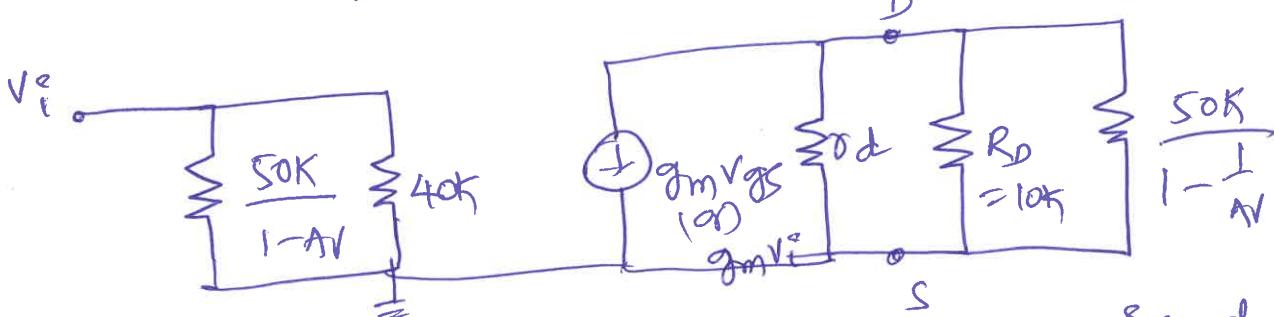
$r_d = 5k\Omega$ , neglect the capacitance



a.c signal  
 $V_i = V_{GS}$

$V_G = V_{GS}$

This is Common  
Source amp



$V_{GG}$  is also DC source - So connected to ground.

$$c.s \text{ amp} \quad A_v = -gmR_D'$$

$$= -\frac{\mu}{r_d} \left[ r_d \parallel R_D \parallel \frac{50k}{1 - \frac{1}{A_v}} \right]$$

$$gm = \frac{\mu}{8a}$$

$$A_V = \frac{-30}{5K} \left[ SK \parallel 10K \parallel \frac{50K}{1 - \frac{1}{A_V}} \right] \quad (12)$$

$$= \frac{-30}{5K} \left[ SK \parallel 10K \parallel 50K \right]$$

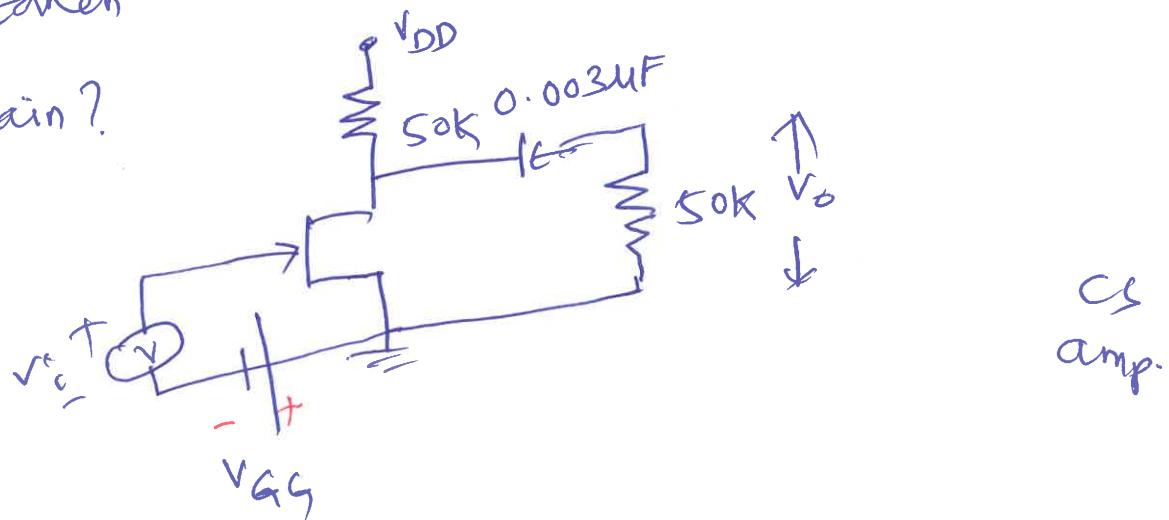
$$A_V = -18.7 \parallel$$

Imp  
 $\Omega_L$  \* Cal the voltage gain  $\frac{V_o}{V_i}$  at 1KHz for  
the CKT shown

The FET parameters are  $g_m = 2 \text{ mA/V}$

and  $r_d = 10K\Omega$

(2) If the capacitance 0.003 MF is taken into consideration . Find the voltage gain?



(1)

For small signal analysis  $V_{DD}$   
is connected to ground (all D.C sources)

CS<sup>o</sup>

$$AV = -g_m R_D'$$

$$= -g_m [$$

$$R_D' = r_d \parallel 50k \parallel 50k$$

$$= 10k \parallel 50k \parallel 50k$$

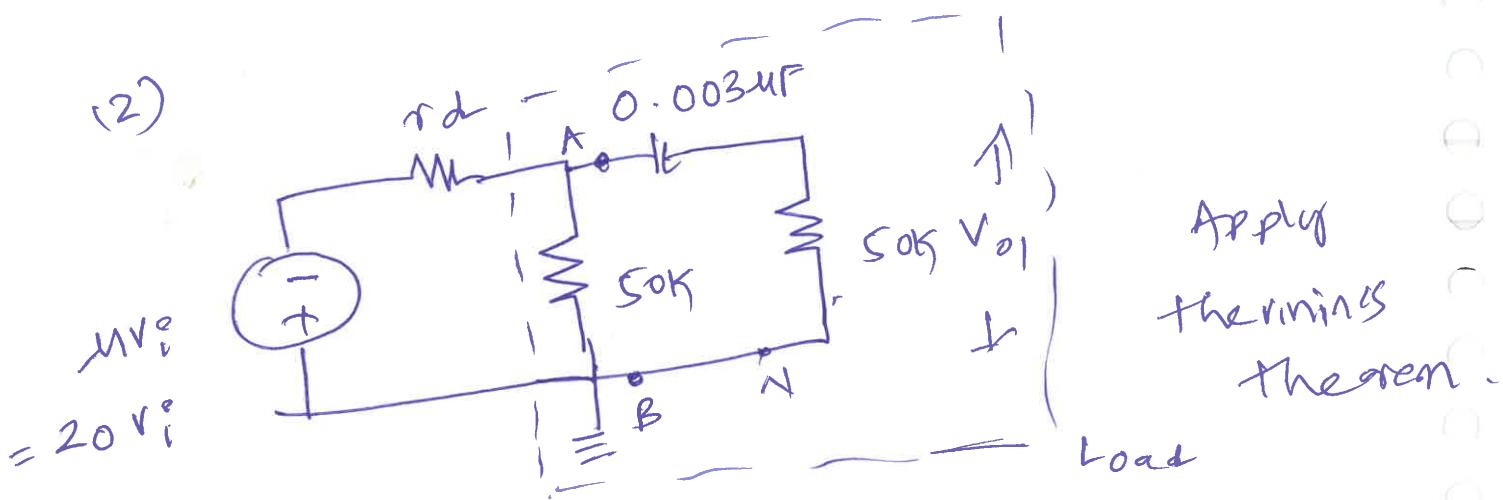
with out  
capacitor)

(CS short  
circuited)

$$AV = -2 \times 10^{-3} [10k \parallel 25k]$$

$$AV = -14.28$$

(2)

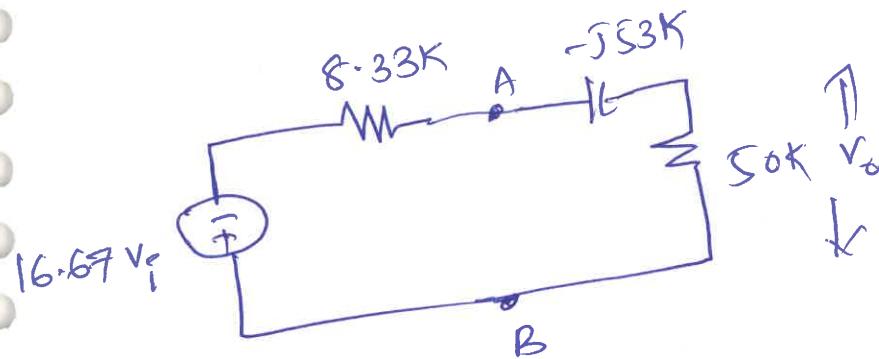


$$\text{Net } \frac{g_m}{r_d} = \frac{2 \times 10^{-3} \times 10k}{20} \quad V_{TH} = +20V_i \times \frac{50k}{50k + 10k}$$

$$M = g_m r_d = \frac{2 \times 10^{-3} \times 10k}{20} \quad = +16.67V_i$$

$$R_{TH} = 50k \parallel 10k = 8.33k$$

(13)

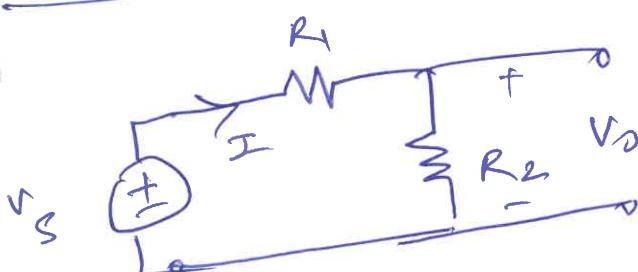


$$Z_C = \frac{1}{j\omega C} = \frac{1}{j2\pi f C}$$

$$V_o = -16.67 V_i \times \frac{50k}{50k + 8.33k - 553k}$$

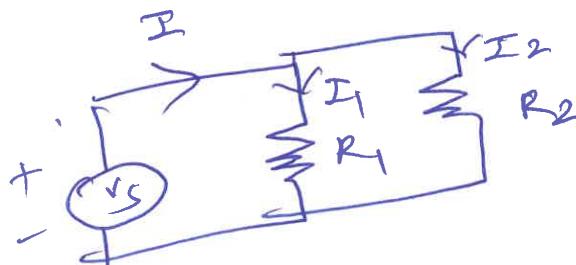
$A_v = \frac{V_o}{V_i} = 10^{-6} \angle -137.7^\circ \text{ } \text{II}$

Voltage division rule's



$$V_o = \frac{R_2}{R_1 + R_2} \times V_s$$

current  
division  
rule:



$$I_1 = I \times \frac{R_2}{R_1 + R_2}$$

$$I_2 = I \times \frac{R_1}{R_1 + R_2} \text{ } \text{II}$$

Imp



## MOSFET Summary:

$i_D$   
(drain current)

Const current Source

Saturation  
region

Linear

Ohmic  
region

$V_{DS}$

(Drain to Source  
Voltage)

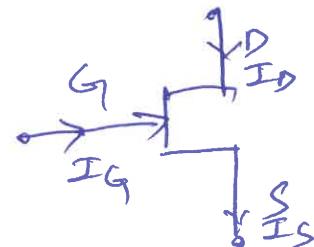
$$V_{DS} = V_{GS} - V_{th}$$

$$V_{DS} < V_{GS} - V_{th} \text{ (Linear)}$$

$$V_{DS} \geq V_{GS} - V_{th} \text{ (Saturation)}$$

$V_{th}$ : Threshold voltage

\* minimum voltage at which the transistor  
becomes ON. (make it on)



When

Conditions:

$$\textcircled{1}. \quad V_{GS} < V_{th} \quad \text{then} \quad I_D = 0$$

\textcircled{2} Linear region (a) Ohmic region (b) Non Sat region.

$$I_D = K_n \frac{W}{L} \left[ (V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$V_{DS} < V_{GS} - V_{th}$$

$$K_n = \mu_n C_{ox}$$

### (3) Saturation region

$$I_D = K_n' \frac{W}{L} \left( \frac{V_{GS} - V_{Th}}{2} \right)^2 \quad \text{when } V_{DS} \geq V_{GS} - V_{Th}$$

$$K_n' = \mu_n C_{ox}$$

$\mu_n$  = mobility of electrons

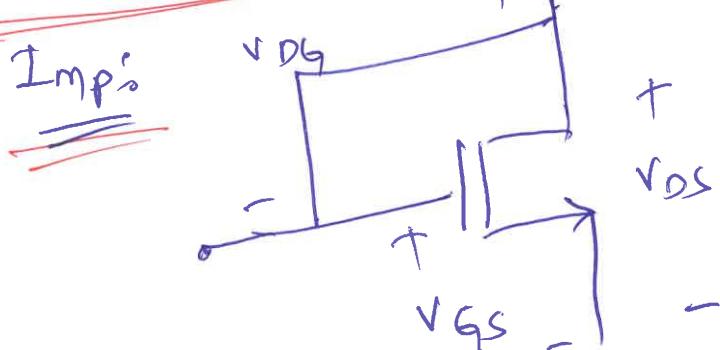
$C_{ox}$  = Gate oxide capacitance

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$W$  = width of S.C

$L$  = length of S.C

Diode Connected:



Here Drain and Gate are short circuited

$$V_{DG} = 0$$

$$K_n L$$

$$-V_{GS} - V_{DG} + V_{DS} = 0$$

$$V_{DG} = V_{DS} - V_{GS}$$

$$0 = V_{DS} - V_{GS}$$

$$V_{DS} = V_{GS}$$

It is in saturation region.

$V_{DG} = 0$  means

$$V_D - V_G = 0$$

$$V_D = V_G$$

$$i_d = g_m v_{gs} + \frac{v_{ds}}{r_d}$$

$$g_m > \frac{i_d}{v_{gs}} \quad | \quad v_{ds} > 0$$

figure of merit

$$r_d = \frac{v_{ds}}{i_d} \quad | \quad v_{gs} > 0$$

$M = g_m r_d$

Amplification factor

Transconductance ( $g_m$ ) (a) Figure of merit

$$g_m = \left. \frac{\partial i_d}{\partial v_{gs}} \right|_{v_{ds}=\text{const}}$$

$$= \left. \frac{\partial}{\partial v_{gs}} \left[ k_n' \frac{W}{L} \frac{(v_{gs} - v_{th})^2}{2} \right] \right|_{v_{ds}=\text{const}}$$

$$g_m = k_n' \frac{W}{L} \frac{2(v_{gs} - v_{th})}{2}$$

$g_m = k_n' \frac{W}{L} (v_{gs} - v_{th})$

$g_m = M_n C_o x \frac{W}{L} (v_{gs} - v_{th})$

→ (1)

$$g_m = \frac{1}{R_{on}}$$

$R_{on}$  is the drain-to-source resistance in the triode region.

$$g_m = 2m_n C_o x \frac{W}{L} (V_{GS} - V_{Th})$$

$$g_m = m_n C_o x \frac{W}{L} \left[ \frac{2I_D}{m_n C_o x \frac{W}{L}} \right]$$

$$I_D = m_n C_o x \frac{W}{L} (V_{GS} - V_{Th})$$

$$V_{GS} - V_{Th} = \sqrt{\frac{2I_D}{m_n C_o x \frac{W}{L}}}$$

$$g_m = 2 \left( m_n C_o x \frac{W}{L} \right) I_D \quad (2)$$

$$* I_D = \frac{1}{2} m_n C_o x \frac{W}{L} (V_{GS} - V_{Th})^2$$

$$\frac{2I_D}{(V_{GS} - V_{Th})^2} = m_n C_o x \frac{W}{L}$$

$$g_m = \sqrt{2 \left[ \frac{2I_D}{(V_{GS} - V_{Th})^2} \times I_D \right]}$$

$$g_m = \frac{2I_D}{V_{GS} - V_{Th}} \quad (3)$$

Basics:

We know

$$v_o = A_1 v_1 + A_2 v_2$$

(a) Superposition principle.

$$A_1 = \frac{v_o}{v_1} \Big|_{v_2=0}$$

$$A_2 = \frac{v_o}{v_2} \Big|_{v_1=0}$$

 $A_1$  &  $A_2$  are gains

For op-amp:  $v_d = v_1 - v_2$  — (1)  $v_c = \frac{v_1 + v_2}{2}$  — (2)

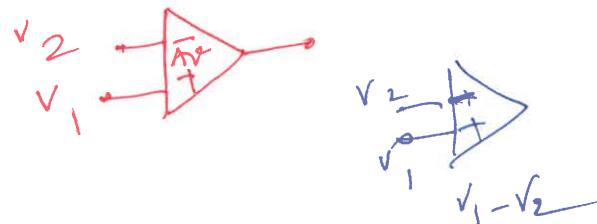
Solve (1) &amp; (2)

$$v_1 - v_2 = v_d$$

$$v_1 + v_2 = 2v_c$$

$$(+) \quad \underline{\quad 2v_1 = v_d + 2v_c}$$

$$v_1 = \frac{v_d + 2v_c}{2} = v_c + \frac{1}{2}v_d \quad \text{--- (3)}$$



$$v_2 = v_c - \frac{1}{2}v_d \quad \text{--- (4)}$$

Substituting (3) &amp; (4) in Eq (a)

$$v_o = A_1 \left[ v_c + \frac{1}{2}v_d \right] + A_2 \left[ v_c - \frac{1}{2}v_d \right]$$

$$v_o = (A_1 + A_2)v_c + \left( \frac{A_1 - A_2}{2} \right) v_d$$

∴  $\boxed{v_o = A_d v_d + A_c v_c}$

## Comparing

$$A_d = \frac{A_1 - A_2}{2} \quad A_c = A_1 + A_2$$

$V_c$  is Common mode voltage

$V_d$  is differential mode voltage.

$A_c$  is common mode gain

$A_d$  is differential mode gain

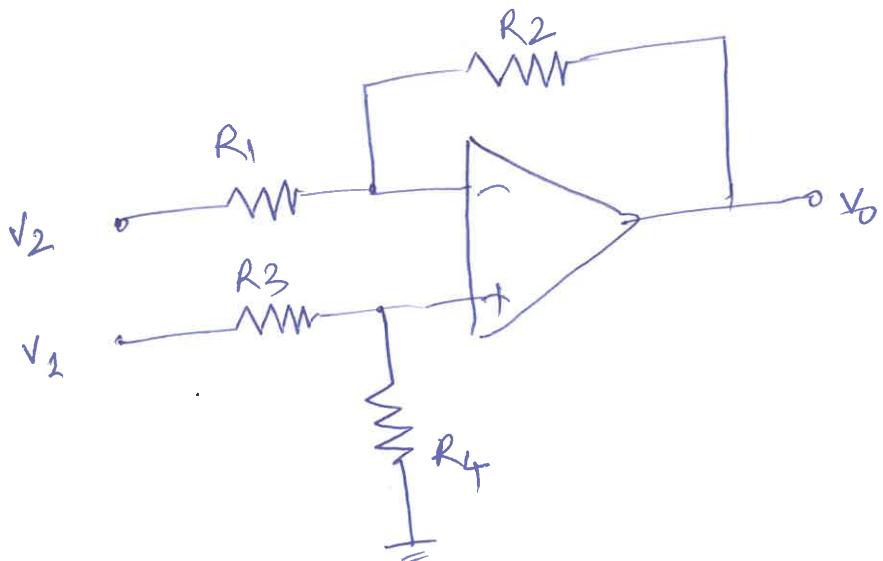
$$CMRR = \frac{|A_d|}{|A_c|}$$

$$CMR =$$

$$\left( \frac{|A_d|}{|A_c|} \right)$$

CMRR: Common Mode Rejection Ratio

1. Common mode gain ( $A_c$ ) and Differential mode gain.  
 (Ad) for a difference amplifier: ①



Assumptions:

1. The current drawn by non-inverting & inverting terminal is zero.

2. The differential input voltage ( $V_d$ ) between non-inverting and inverting input is zero.

$V_d = V_1 - V_2 = 0 \Rightarrow V_1 = V_2$

so Voltage at inverting terminal = Voltage at non-inverting terminal.

By Using Superposition principle

$$V_o = -\frac{R_2}{R_1} V_2 + \left(1 + \frac{R_2}{R_1}\right) \times \left(\frac{R_4}{R_3 + R_4}\right) V_2$$

(2)

$$v_o = -\frac{R_2}{R_1} v_2 + \left( \frac{R_1+R_2}{R_1} \right) \times \left( \frac{R_4}{R_3+R_4} \right) v_1 \quad \text{--- (a)}$$

We know  $v_d = v_1 - v_2$  &  $v_c = \frac{v_1 + v_2}{2}$

$\therefore v_1 = v_c + \frac{1}{2} v_d \quad \text{--- (1)} \quad \& \quad v_2 = v_c - \frac{1}{2} v_d \quad \text{--- (2)}$

Substitute (1) & (2) in eq (a)

$$v_o = -\frac{R_2}{R_1} \left( v_c - \frac{1}{2} v_d \right) + \left( \frac{R_1+R_2}{R_1} \right) \times \left( \frac{R_4}{R_3+R_4} \right) \left( v_c + \frac{1}{2} v_d \right)$$

$$\Rightarrow v_o = -\frac{R_2}{R_1} v_c + \frac{(R_1+R_2)(R_4)}{(R_3+R_4) R_1} v_c \\ + \frac{R_2}{R_1} \times \frac{v_d}{2} + \frac{(R_1+R_2) R_4}{(R_3+R_4) R_1} \frac{1}{2} v_d$$

$$v_o = \left( \frac{R_2}{2 R_1} + \frac{(R_1+R_2) R_4}{2 (R_3+R_4) R_1} \right) v_d \\ + \left( \frac{(R_1+R_2) R_4}{(R_3+R_4) R_1} - \frac{R_2}{R_1} \right) v_c$$

$\therefore \boxed{v_o = A_d v_d + A_c v_c}$

Comparing.

(3)

$$Ad = \frac{R_2}{2R_1} + \frac{(R_1+R_2)R_4}{2(R_3+R_4)R_1}$$

$$\therefore Ad = \frac{1}{2} \left[ \frac{R_2}{R_1} + \frac{(R_1+R_2)R_4}{(R_3+R_4)R_1} \right]$$

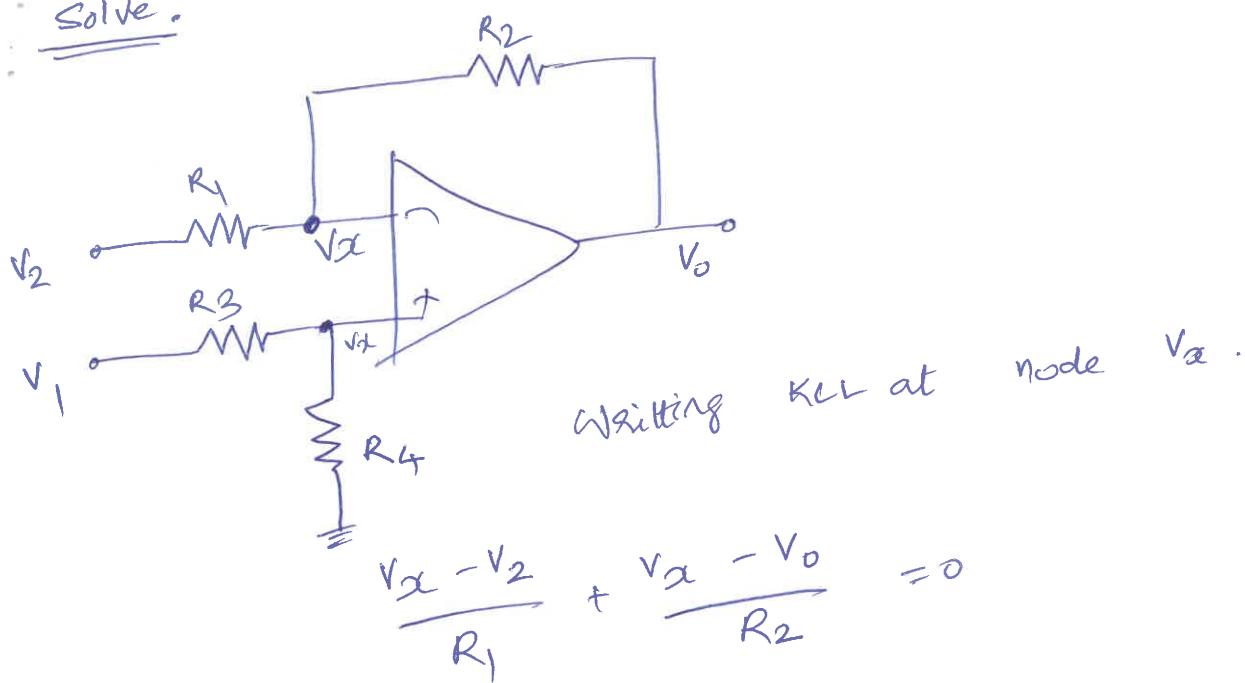
$$Ac = \frac{(R_1+R_2)R_4}{(R_3+R_4)R_1} - \frac{R_2}{R_1}$$

$$= \frac{1}{R_1} \left[ \frac{(R_1+R_2)R_4 - R_2R_1(R_3+R_4)}{(R_3+R_4)} \right]$$

$$= \frac{1}{R_1} \left[ \frac{R_1R_4 + R_2R_4 - R_2R_1R_3 - R_2R_1R_4}{(R_3+R_4)} \right]$$

$$\therefore Ac = \frac{(R_1+R_2)R_4 - R_1R_2(R_3+R_4)}{R_1(R_3+R_4)}$$

2)

(OR) (Q) 1<sup>st</sup> questionSolve:

$$V_x \left[ \frac{1}{R_1} + \frac{1}{R_2} \right] - \frac{V_2}{R_1} = \frac{V_0}{R_2}$$

$$V_0 = \left( \frac{R_2}{R_1} + \frac{R_2}{R_2} \right) V_x - \frac{R_2}{R_1} V_2$$

$$V_0 = \left( 1 + \frac{R_2}{R_1} \right) V_x - \frac{R_2}{R_1} V_2$$

As per virtual short concept

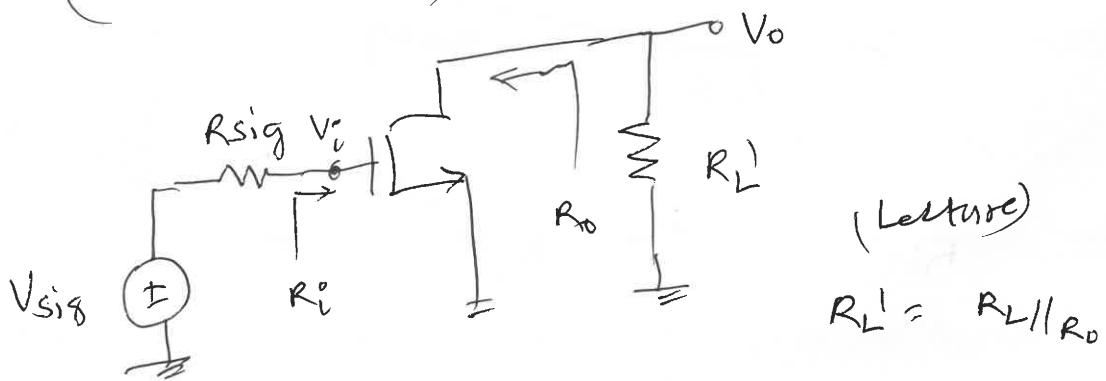
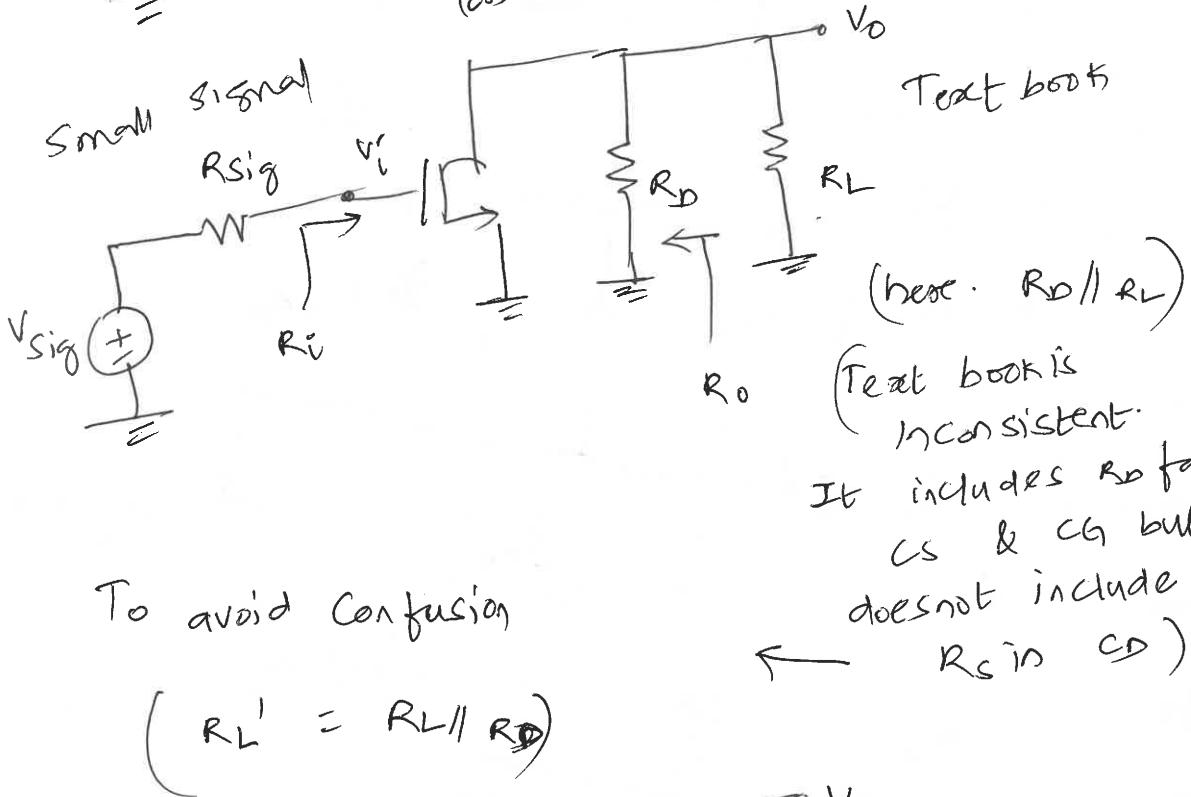
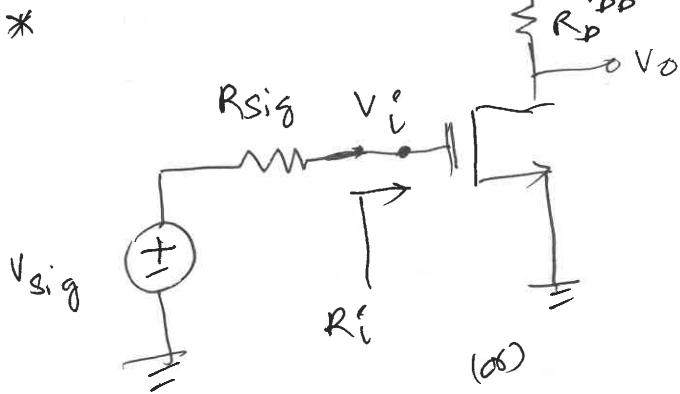
Voltage at inverting terminal = Voltage at  
non-inverting terminal.

$$\therefore V_x = \frac{R_4}{R_3 + R_4} V_1 \quad (\text{Voltage divider principle})$$

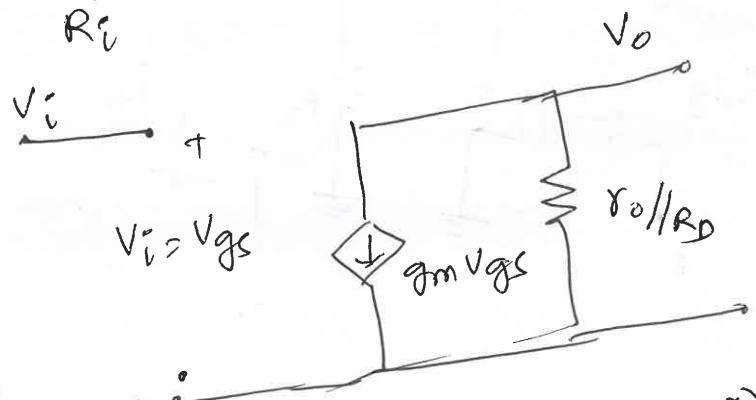
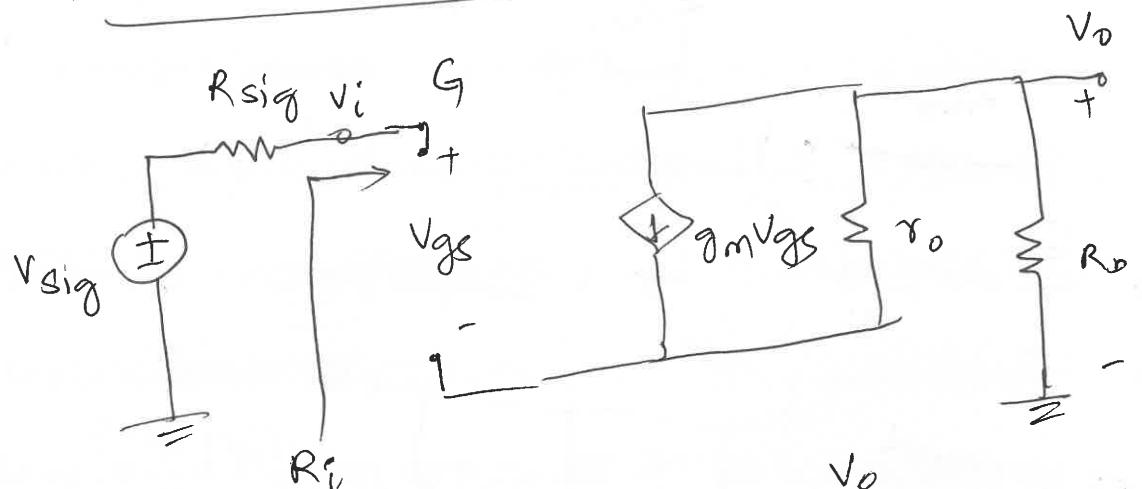
$$\therefore V_0 = \left( 1 + \frac{R_2}{R_1} \right) \frac{R_4}{R_3 + R_4} V_1 - \frac{R_2}{R_1} V_2 //$$

(~~scribbled~~) from Sedra & Smith

Sudhakar Busi



small signal model:



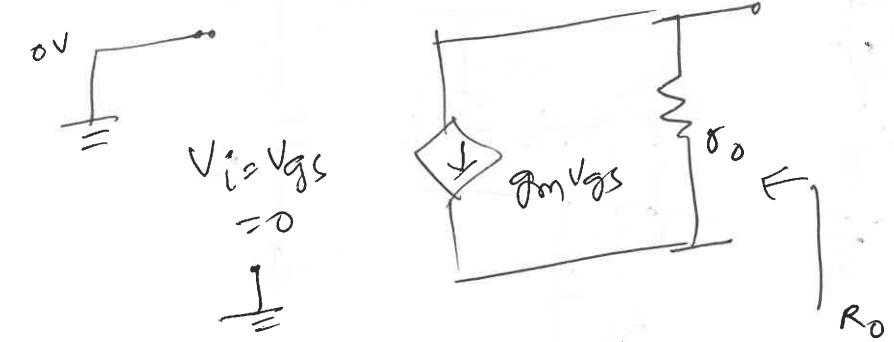
$$V_o = -gmV_{gs} \left( r_o \parallel R_o \right) \quad \text{and} \quad \overset{\infty}{-gmV_{gs}} \left( r_o \parallel R_o \right)$$

$$A_v = \frac{V_o}{V_i} = -gm \left( r_o \parallel R_o \right)$$

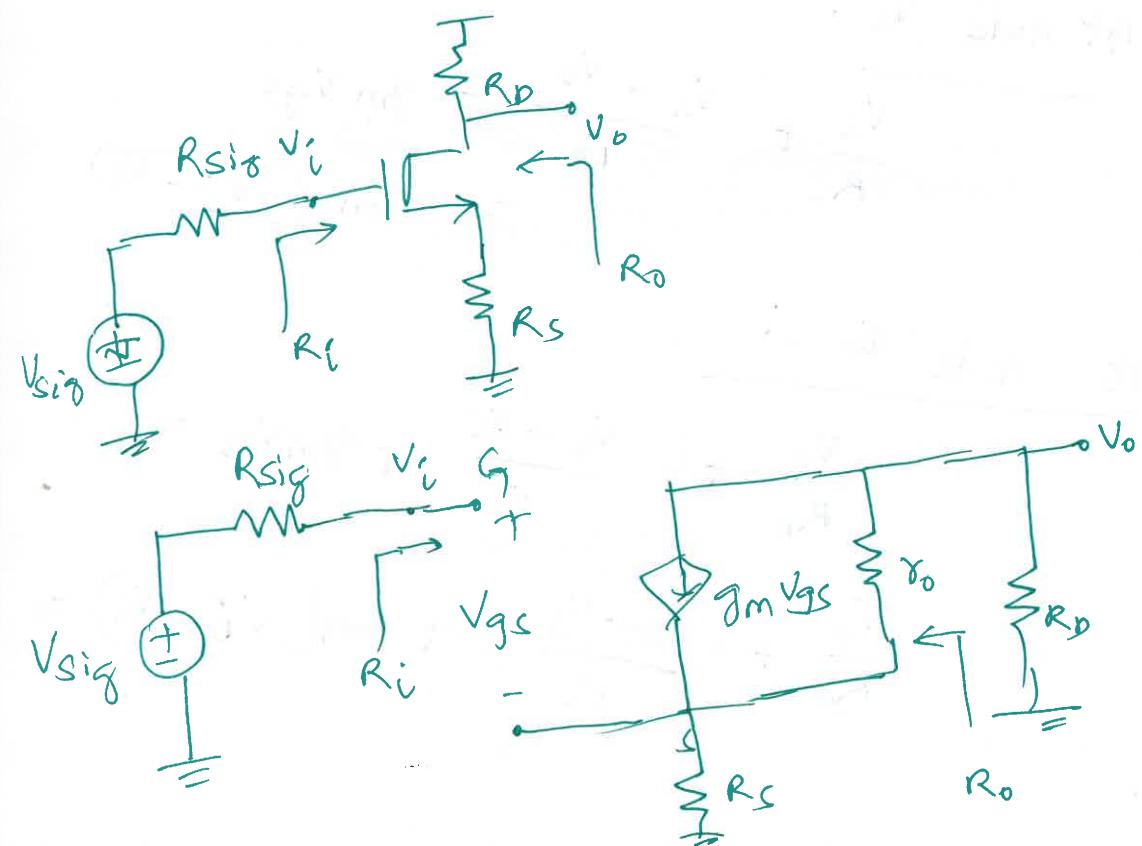
$$\boxed{A_{v0} = -gm r_o}$$

$$R_i : I_i = 0 \quad \text{and} \quad R_i = \frac{V_i}{I_i} = \infty$$

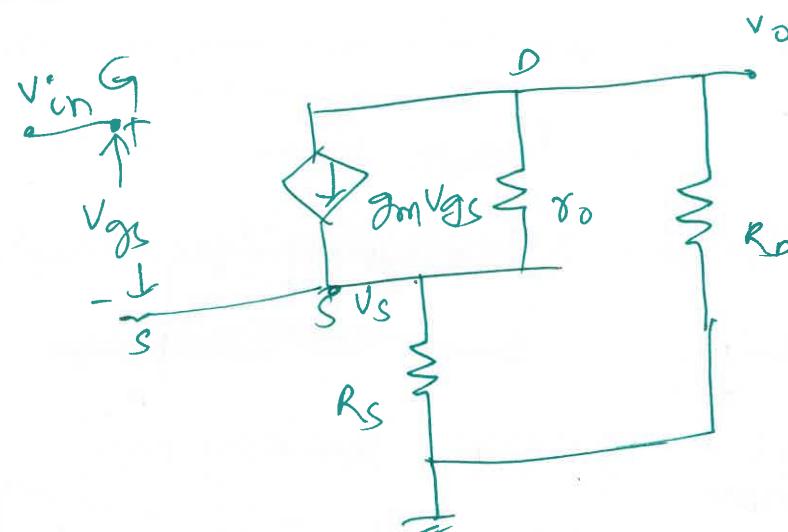
R<sub>o</sub>: R<sub>o</sub> calculation (Set V<sub>o</sub> = 0)



here Current Source becomes  $\frac{0 \cdot C}{\therefore R_o = r_o}$   
Common Source with Source Resistance! (R<sub>s</sub>)



### Gain Calculation:



Node Voltages:

$$V_{gs} = V_{in} - V_S$$

At node  $V_S$ :

$$\frac{V_S}{R_s} + \frac{V_S - V_o}{R_D} = g_m V_{gs}$$

$$= g_m (V_i - V_S)$$

At node  $V_o$ :

$$\frac{V_o}{R_D} + \frac{V_o - V_S}{R_o} + g_m V_{gs} = 0$$

$$\frac{V_o}{R_D} + \frac{V_o - V_S}{R_o} + g_m (V_i - V_S) = 0$$

$$-V_{in} + V_{gs} + V_o = 0$$

$$V_{gs} = V_{id} - V_S$$

$$V_{gs} = V_{in} - I_D R_S$$

After Solving:

$$AV = \frac{V_o}{V_{in}} =$$

$$\frac{-g_m r_o R_D}{r_o + R_D + (1 + g_m r_o) R_L}$$

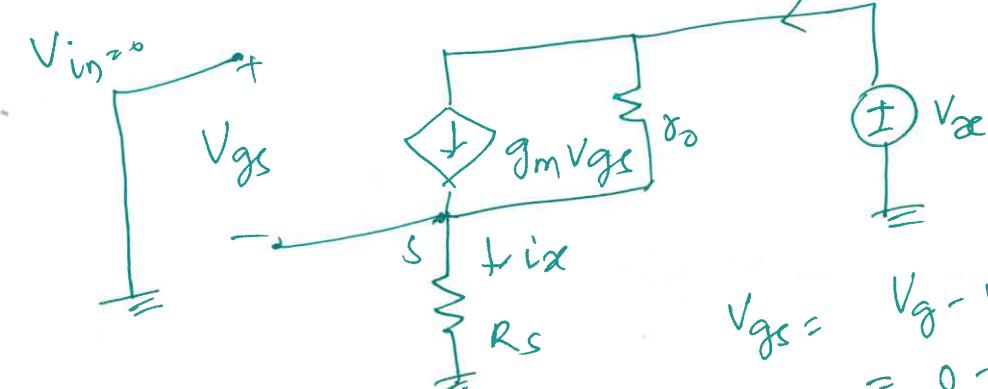
$$AV = \frac{-M R_D}{r_d + R_D + (1 + M) R_L}$$

$$\boxed{AV_o = -g_m r_o}$$

$R_o$ :

- ① Set  $V_{in} = 0$
- ② Attach  $V_\alpha$  and Compute  $i_\alpha$
- ③

$$R_o = \frac{V_\alpha}{i_\alpha}$$



$$V_{gs} = V_g - V_S$$

$$= 0 - V_S$$

At node  $V_S$

$$\frac{V_S}{R_S} + \frac{V_S - V_\alpha}{r_o} = g_m V_{GS}$$

$$\frac{V_S}{R_S} + \frac{V_S - V_\alpha}{r_o} = -g_m V_S$$

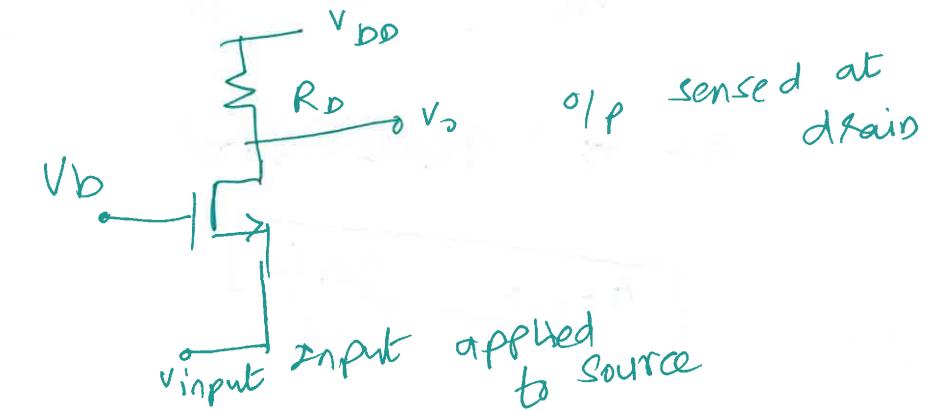
$$\frac{V_S}{R_S} = \frac{V_\alpha}{r_o + (1 + g_m r_o) R_S}$$

$$i_{de} = \frac{V_S}{R_S} = \frac{V_\alpha}{r_o + (1 + g_m r_o) R_S}$$

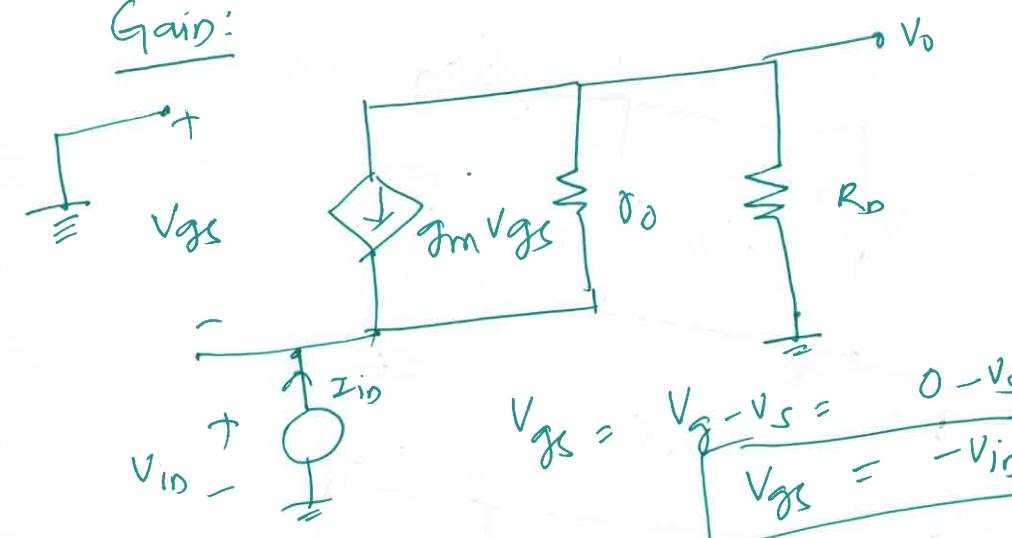
$$\frac{1}{R_o} = \frac{i_{de}}{V_\alpha} = \frac{1}{r_o + (1 + g_m r_o) R_S}$$

$$\therefore R_o = r_o + (1 + g_m r_o) R_S$$

Common Gate Configuration:



Gain:



$$\text{at Node } V_o: \frac{V_o}{R_D} + \frac{V_o - v_{in}}{r_o} + g_m V_{GS} = 0$$

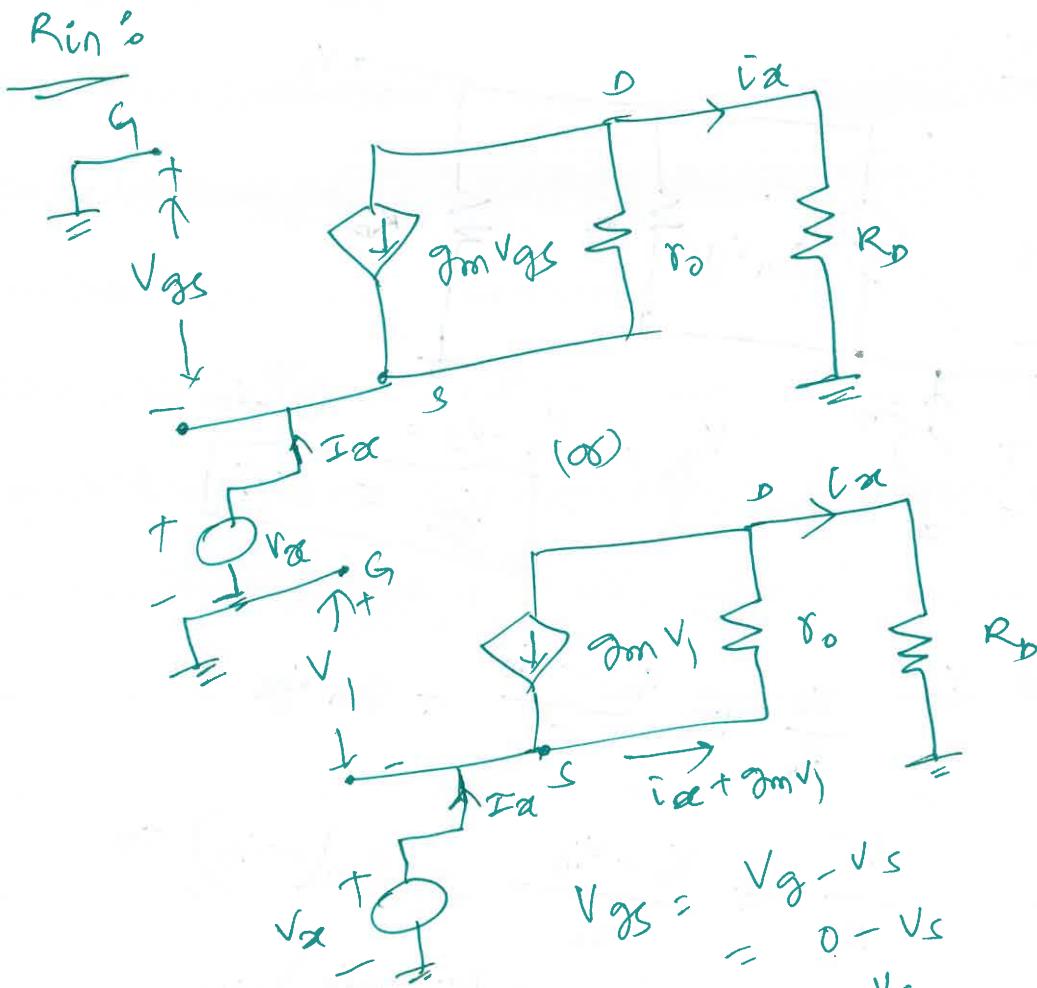
$$\frac{V_o}{R_D} + \frac{V_o - v_{in}}{r_o} + g_m(-v_{in}) = 0$$

$$\frac{V_o}{(R_D || r_o)} = \left( \frac{1 + g_m r_o}{r_o} \right) v_{in}$$

$$A_f = \frac{V_o}{V_{IN}} = \left( \frac{1 + g_m r_o}{r_o} \right) (r_o / R_D)$$

$$A_f \approx g_m (r_o / R_D)$$

$$A_f \approx g_m r_o$$



$$V_{GS} = V_g - V_s \\ = 0 - V_s \\ = -V_s$$

$$V_s = V_a \\ V_{GS} = -V_s \\ V_I = -V_a$$

KVL equation:

$$-V_a + (i_a + g_m V_I) r_o + i_a R_D = 0$$

5

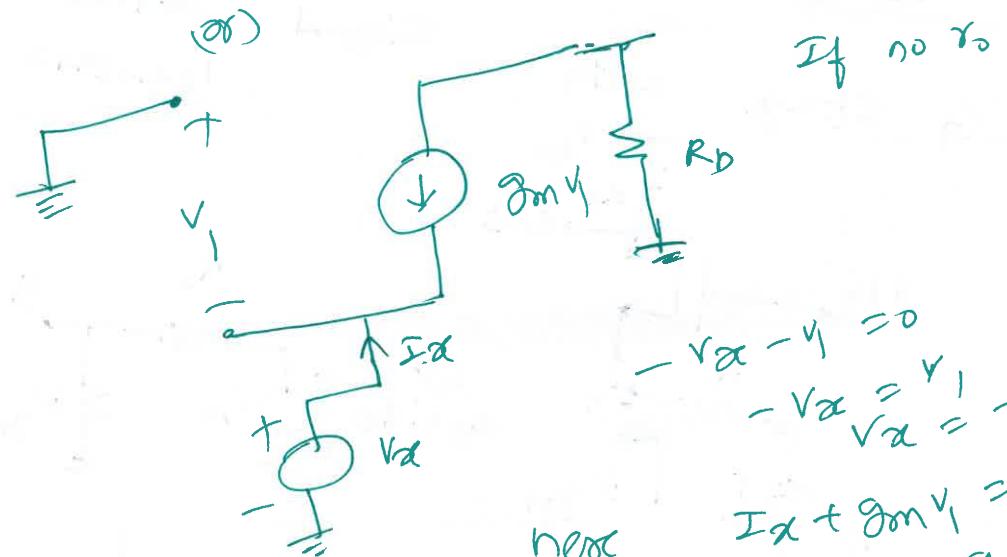
$$V_a = (i_a + g_m V_I) r_o + i_a R_D$$

$$V_a = [i_a + g_m (-V_a)] r_o + i_a R_D$$

$$V_a [1 + g_m r_o] = i_a [r_o + R_D]$$

$$\frac{V_a}{i_a} = R_{in} = \frac{r_o + R_D}{1 + g_m r_o}$$

$$R_{in} \approx \frac{1}{g_m} + \frac{R_D}{g_m r_o}$$



$$-r_a - V_I = 0 \\ -V_a = V_I \\ V_a = -V_I$$

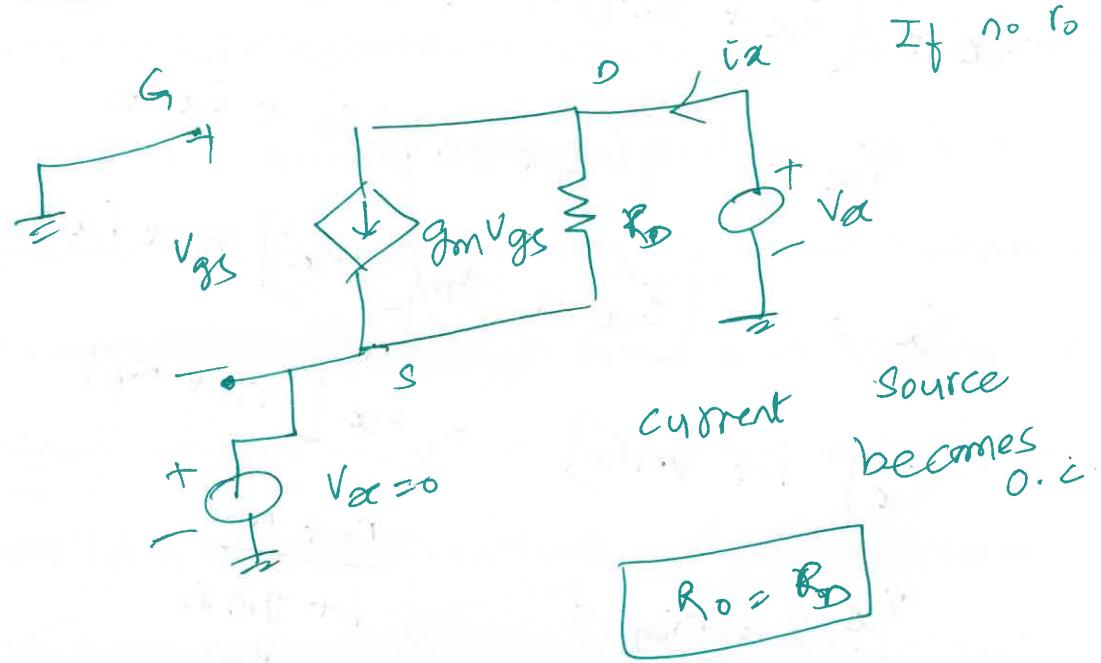
$$I_a + g_m V_I = 0 \\ I_a = -g_m V_I$$

$$I_a = -g_m (-V_a)$$

$$\frac{V_a}{I_a} = R_{in} = \frac{1}{g_m}$$

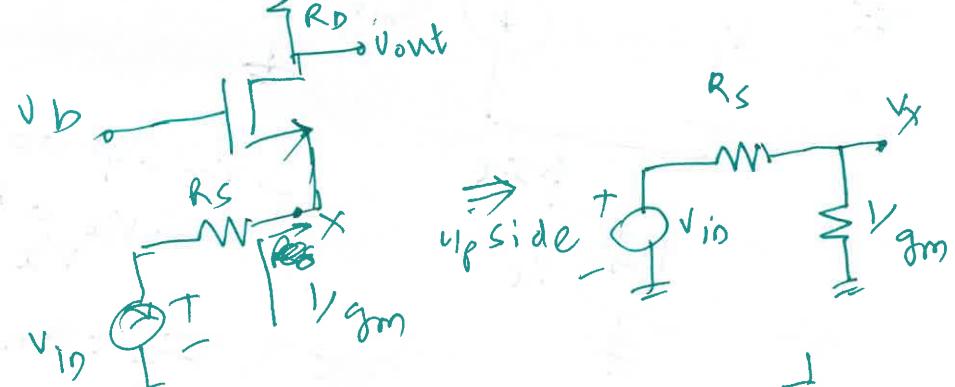
$R_0$ :

Set  $V_{in} = 0$



# Common Point Configuration

Common Source resistance ( $R_s$ ):  
CG stage with  $T_{V_{DD}}$  Signal



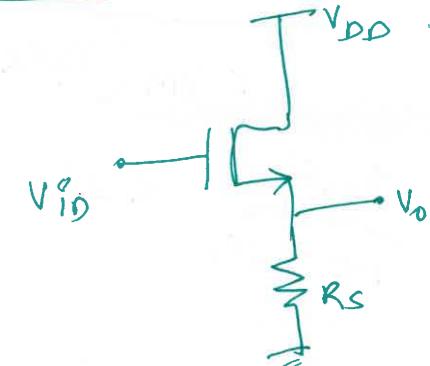
$$V_x = V_{ID} \times \frac{\frac{1}{gm}}{\frac{1}{gm} + R_S}$$

$$V_x = \frac{i}{1 + g_m R_S} V_{in}$$

$$\therefore \frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_x} \cdot \frac{V_x}{V_{in}} = \frac{g_m R_D x}{1 + g_m R_S}$$

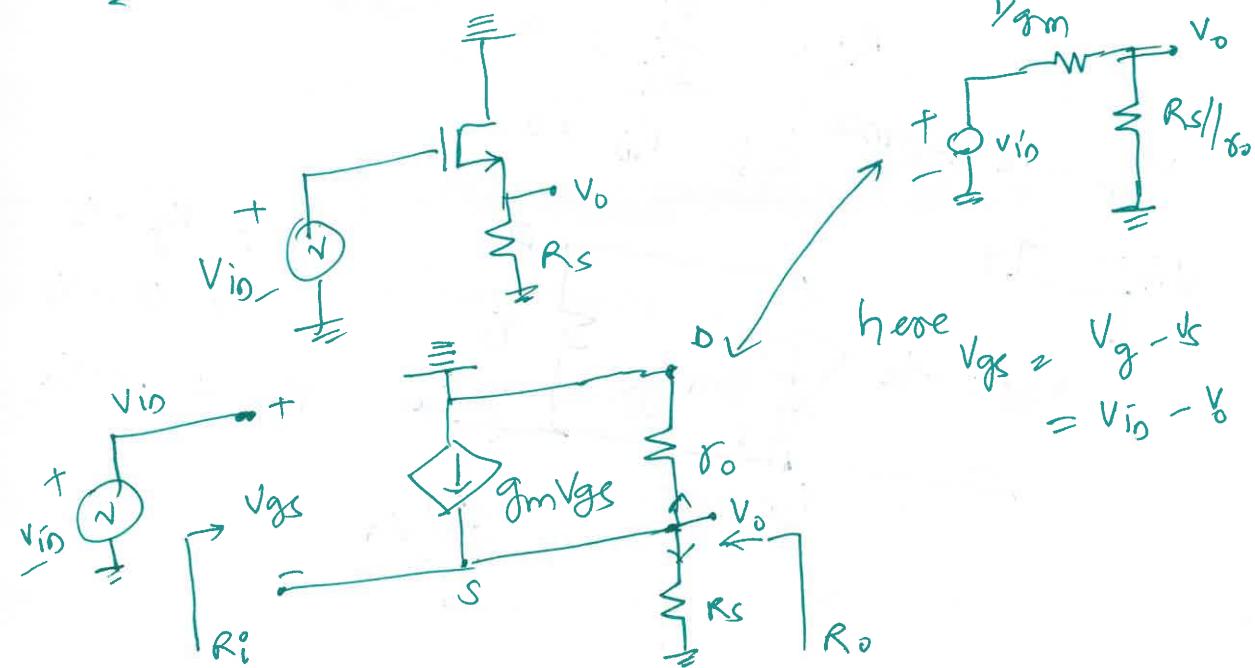
$$\frac{V_{out}}{V_{in}} = \frac{R_D}{\frac{1}{g_m} + R_S} \quad //$$

## CD Configuration:



## CD gain Calculation:

- small signal equivalent





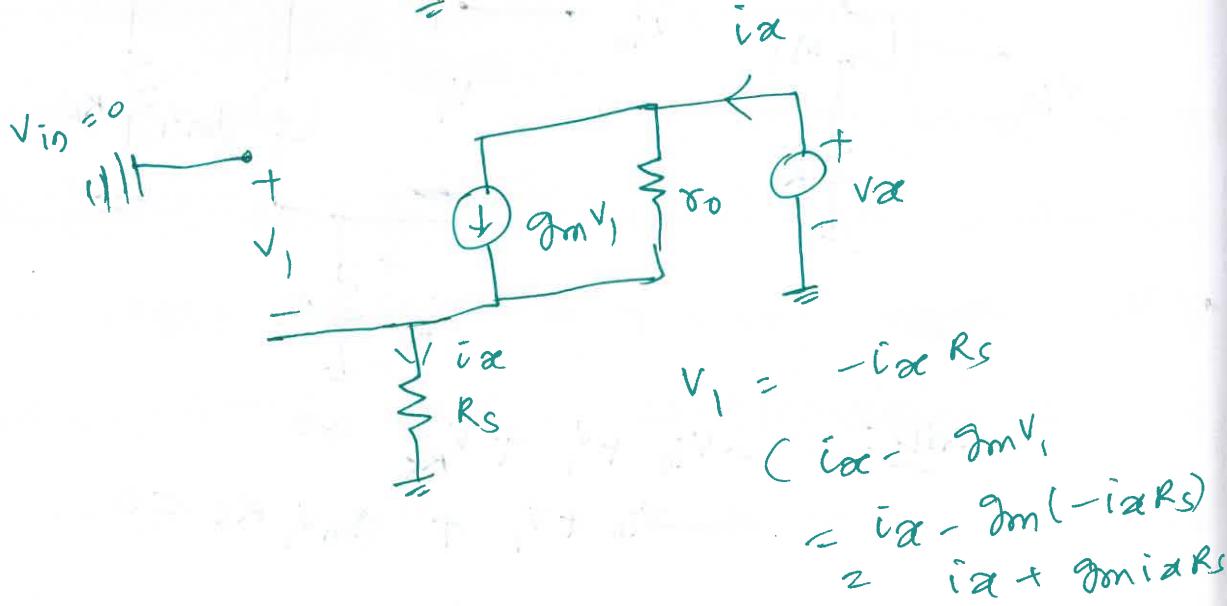
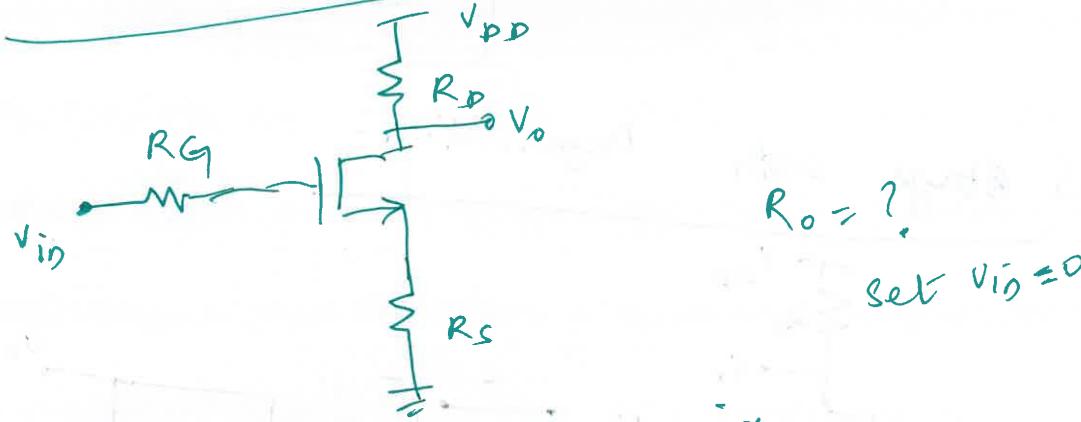
$$v_{id} = v_i [1 + g_m R_s]$$

$$v_i = \frac{v_{in}}{1 + g_m R_s}$$

and  $v_o = -g_m v_i R_D$

$$\frac{v_o}{v_{id}} = \frac{-g_m R_D}{1 + g_m R_s} = \frac{-R_D}{\frac{1}{g_m} + R_s}$$

CS Stage with Gate Resistance:



KVL:

$$-v_{id} + r_0 (i_a - g_m v_i) + i_a R_s = 0$$

$$-v_{id} + r_0 (i_a + g_m i_a R_s) + i_a R_s = 0$$

$$\frac{v_x}{i_a} = \frac{r_0 (1 + g_m R_s) + R_s}{r_0 (1 + g_m R_s) + R_s} i_a = 0$$

$$\frac{v_x}{i_a} = r_0 (1 + g_m R_s) + R_s$$

$$\approx r_0 + g_m R_s \approx r_0 + R_s$$

$$\approx r_0 + (g_m r_0 + 1) R_s$$

$$\approx r_0 + (1 + g_m r_0) R_s + R_s$$

$$\approx g_m r_0 R_s + r_0 // R_s$$

# KNOW?

hit only 6 sixes!

In his entire Test career, Sir Donald Bradman



Dragonflies were around long before the dinosaurs. Back then, they had wingspans of two and a half feet!

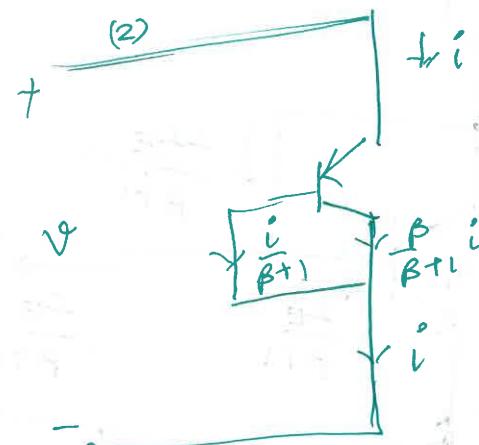
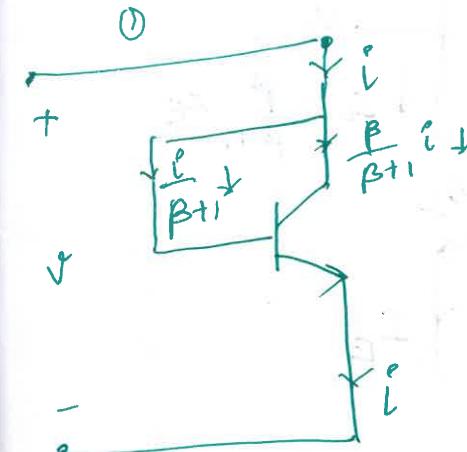
In a year, million tons of dust get carried by the wind from the Sahara Desert to the Amazon!

18/12/2023

classmate

GKT0621528 B

Diode Connected BJTs:



Sudhakar Busi 9

here

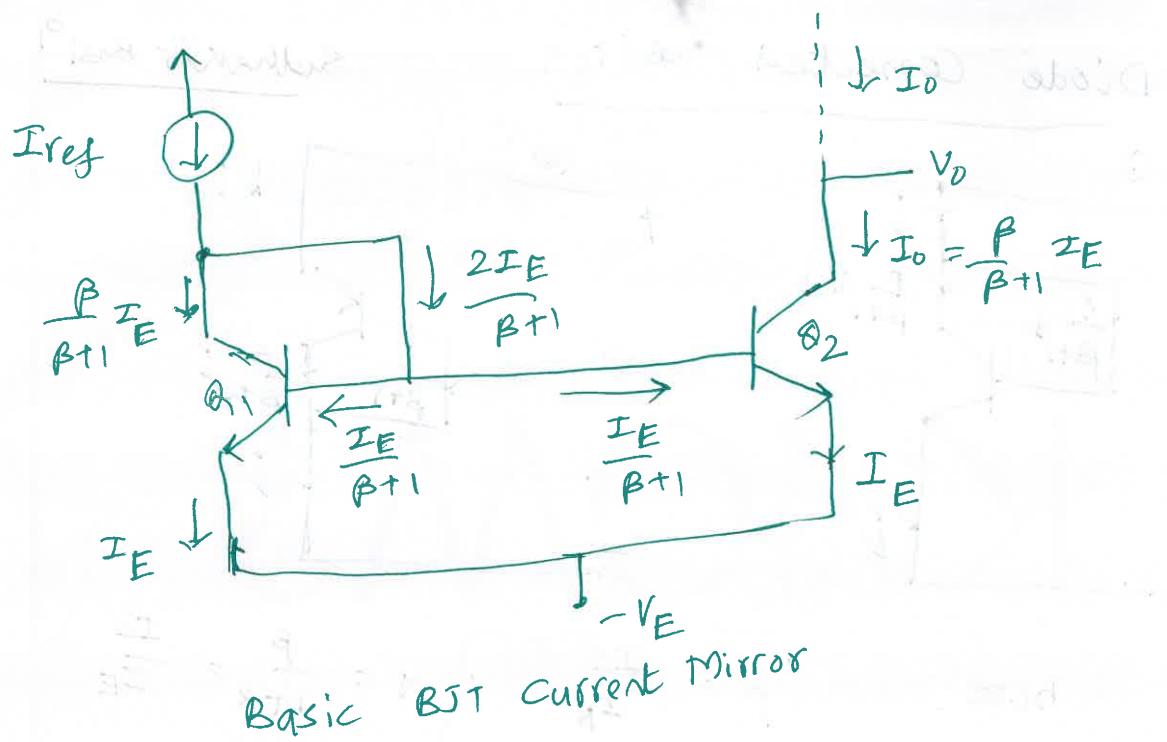
$$\beta = \frac{I_C}{I_B} ; \alpha = \frac{\beta}{1+\beta} = \frac{I_C}{I_E}$$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{I_C}{I_B}$$

$$\Gamma = \frac{I_E}{I_B} = 1 + \beta \Rightarrow I_B = \frac{I_E}{1 + \beta}$$

current mirror (BJT): It consists of two matched transistors  $\alpha_1$  and  $\alpha_2$  with their bases are connected together and having

same  $V_{BE}$ .



Basic BJT Current Mirror

$$\text{Here } I_0 = \frac{\beta}{\beta+1} I_E$$

$$I_{\text{ref}} = \frac{\beta}{\beta+1} I_E + \frac{2IE}{\beta+1}$$

$$I_{\text{ref}} = \frac{\beta+2}{\beta+1} I_E$$

Current gain of the current mirror

$$\frac{I_0}{I_{\text{ref}}} = \frac{\frac{\beta}{\beta+1} I_E}{\frac{\beta+2}{\beta+1} I_E} = \frac{\beta}{\beta+2} I_E$$

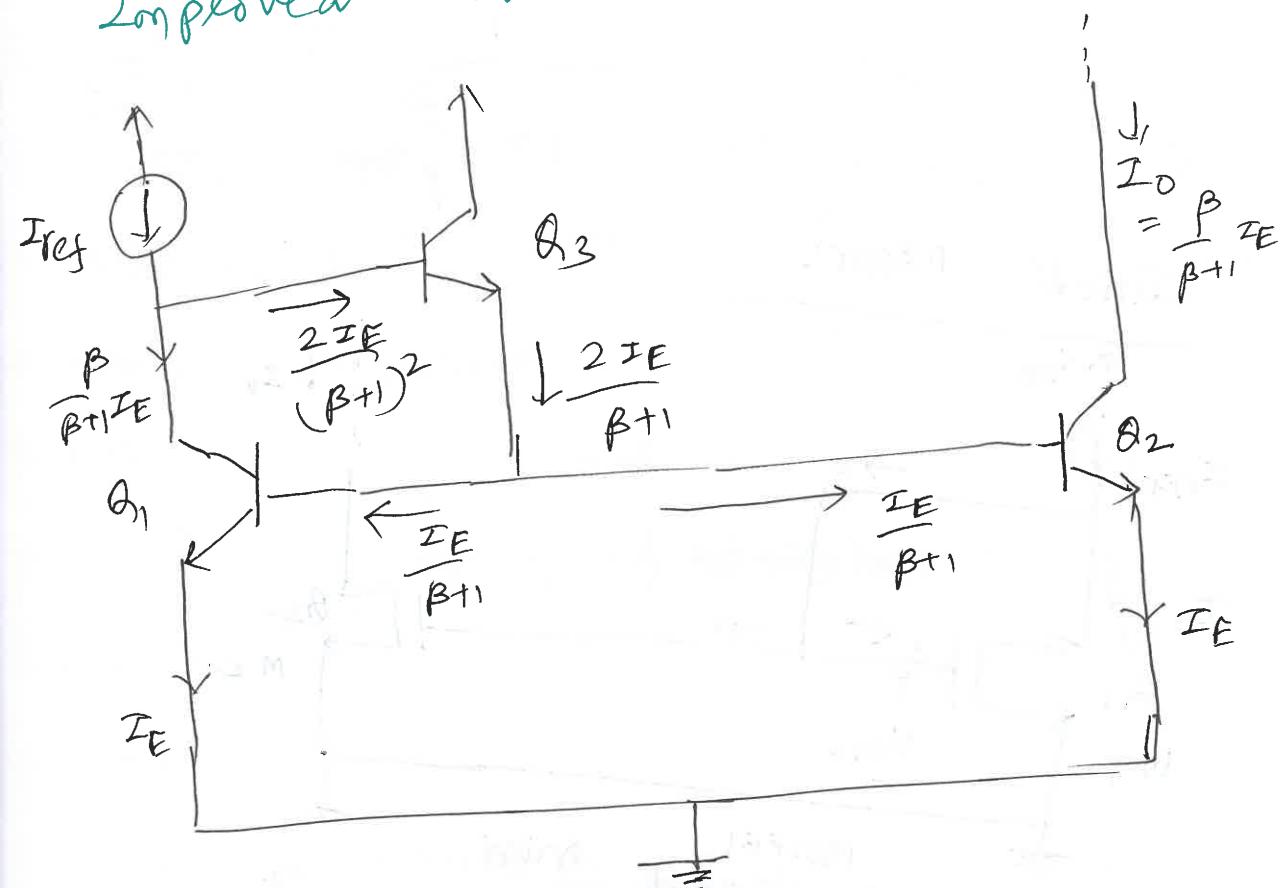
$$\frac{I_0}{I_{\text{ref}}} = \frac{1}{1 + \frac{2}{\beta}}$$

$\beta \gg 1$

approaches to unity when  $\beta \gg 1$

The MOS mirror does not suffer from the finite  $\beta$  effect. (10)

Improved Current Source Circuits



$$\text{Here } I_{\text{ref}} = \frac{\beta}{\beta+1} I_E + \frac{2IE}{(\beta+1)^2}$$

$$= \left[ \frac{\beta}{\beta+1} + \frac{2}{(\beta+1)^2} \right] I_E$$

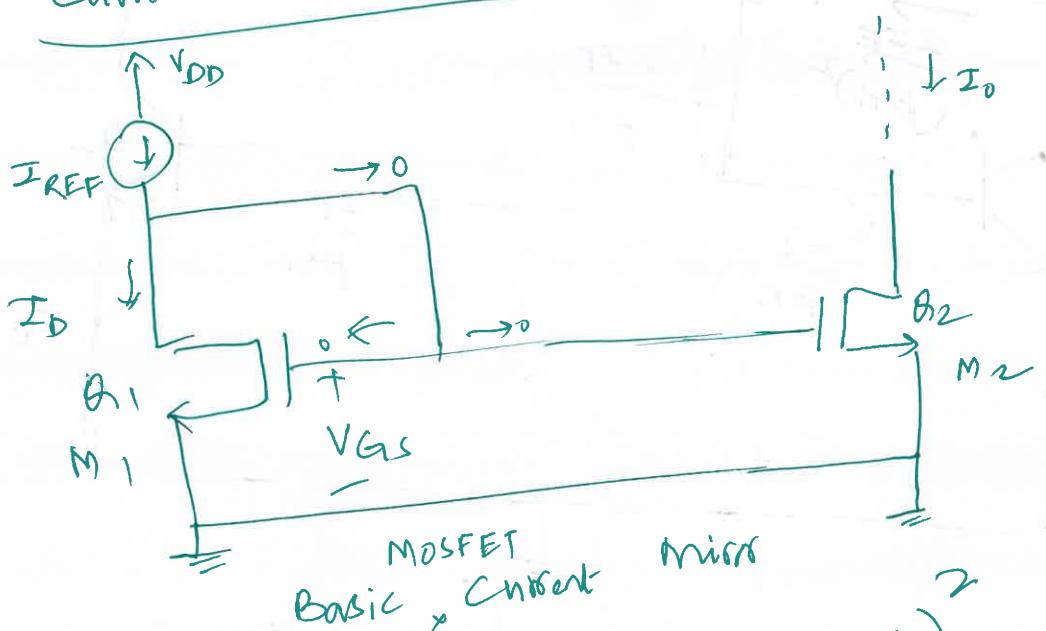
$$I_0 = \frac{\beta}{\beta+1} I_E$$

Current gain of the mirror is

$$\frac{I_0}{I_{REF}} = \frac{\beta}{\frac{\beta}{\beta+1} + \frac{2}{(\beta+1)^2}}$$

$$= \frac{1}{1 + \frac{2}{\beta^2 + \beta}} \approx \frac{1}{1 + \frac{2}{\beta^2}}$$

Current Mirror:



$$I_{D2} = \frac{1}{2} k_n' \left( \frac{W}{L} \right)_2 (V_{GS} - V_T)^2$$

The heart of the circuit is transistor Q<sub>1</sub>, whose drain is shorted to its gate and thus operating in saturation region.

$$V_{DG} = 0$$

$$V_{G0} = 0$$

means  $V_{GD} = V_{GS} - V_{DS}$

Transistor Q<sub>2</sub>:

$$I_0 = I_{D2} = \frac{1}{2} k_n' \left( \frac{W}{L} \right)_2 (V_{GS} - V_T)^2$$

It has same voltage V<sub>GS</sub> as Q<sub>1</sub>

If we assume it is operating in saturation

its drain current

$$I_0 = I_{D2} = \frac{1}{2} k_n' \left( \frac{W}{L} \right)_2 (V_{GS} - V_T)^2$$

neglect channel-length modulation

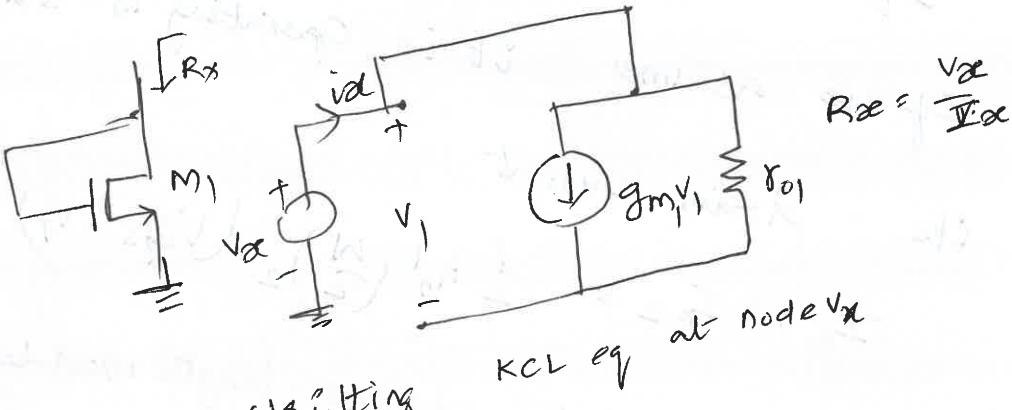
$$\frac{I_0}{I_{REF}} = \frac{\frac{1}{2} k_n' \left( \frac{W}{L} \right)_2 (V_{GS} - V_T)^2}{\frac{1}{2} k_n' \left( \frac{W}{L} \right)_1 (V_{GS} - V_T)^2}$$

$$= \frac{\left( \frac{W}{L} \right)_2^2}{\left( \frac{W}{L} \right)_1} = \text{Aspect ratio of the transis}$$

The Relationship between  $I_o$  and  $I_{REF}$  Solely determined by the geometry of the transistors.

\* In Special Case: Identical Transistors:  
 $I_o = I_{REF}$ .

Diode Connected NMOS device:



KCL eq at node  $V_x$

$$I_{xe} = \frac{v_{xe}}{R_{02}} + g_{m1} V_1$$

$$\text{But } v_{xe} = V_1$$

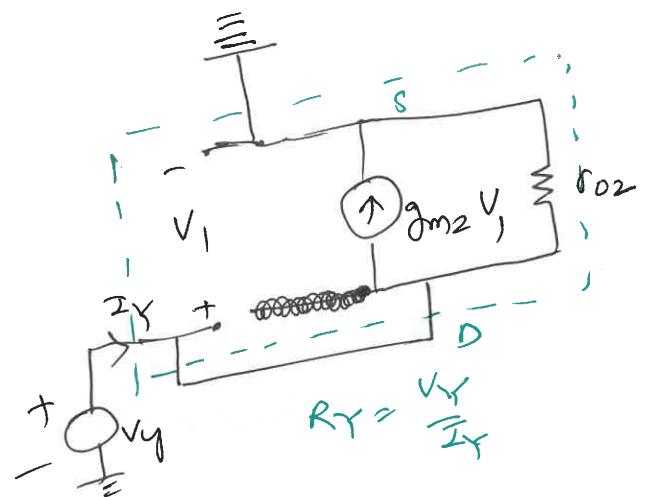
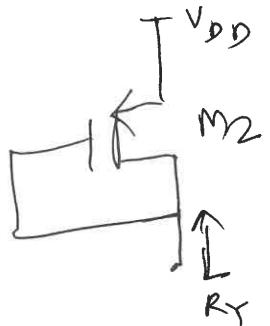
$$I_{xe} = \frac{V_1}{R_{02}} + g_{m1} V_1$$

$$I_{xe} = V_1 \left[ \frac{1}{R_{01}} + g_{m1} \right]$$

$$\frac{v_{xe}}{I_{xe}} = \frac{1}{\left[ g_{m1} + \frac{1}{R_{01}} \right]}$$

$$r_{xe} = \frac{v_{xe}}{I_{xe}} = \frac{1}{g_{m1} \parallel R_{01}}$$

Diode Connected pmos device  $\frac{1}{\alpha_e + y} \text{ means } \frac{1}{\alpha_e} \parallel \frac{1}{y}$  (12)



$$\text{KCL eq: } I_{Y} = \frac{V_Y}{R_{02}} + g_{m2} V_1$$

$$I_Y = \frac{V_Y}{R_{02}}$$

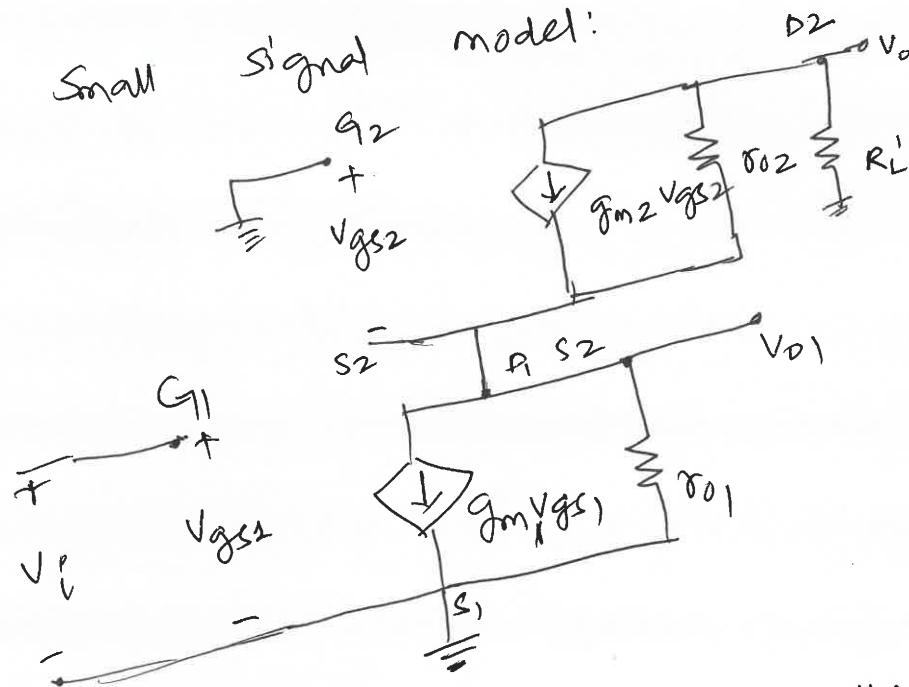
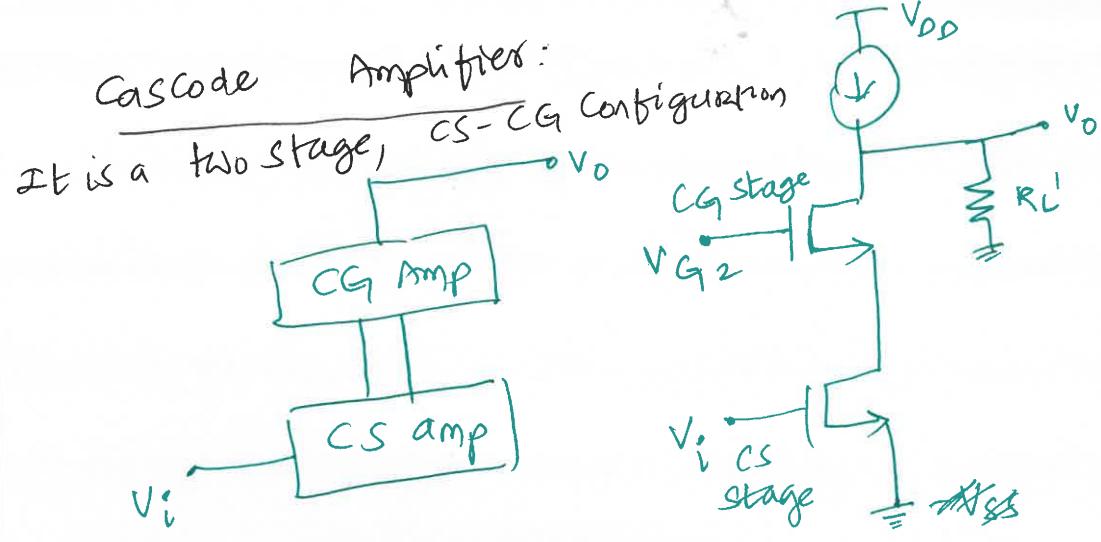
$$\text{But } V_Y = V_1$$

$$I_Y = g_{m2} V_1 + \frac{V_Y}{R_{02}}$$

$$I_Y = \left( g_{m2} + \frac{1}{R_{02}} \right) V_Y$$

$$\frac{V_Y}{I_Y} = \frac{1}{\left( g_{m2} + \frac{1}{R_{02}} \right)} = \frac{1}{g_{m2} \parallel R_{02}}$$

$$R_Y = \frac{V_Y}{I_Y} = \frac{1}{g_{m2} \parallel R_{02}}$$



V01: writing KCL at node V01

$$\frac{V_{01} - 0}{r_{01}} + g_{m1} v_{gs1} = 0 \quad (1)$$

$$V_{01} = -g_{m1} r_{01} v_{gs1}$$

$$V_{01} = -g_{m1} r_{01} v_i$$

KCL at node V0

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$$\frac{V_0 - V_{01}}{r_{02}} + g_{m2} v_{gs2} = 0$$

$$\text{here } v_{gs2} = v_{g2} - v_{s2} = 0 - V_{01}$$

$$\frac{V_0}{r_{02}} = \frac{V_{01}}{r_{02}} - g_{m2} v_{gs2}$$

$$= \frac{V_{01}}{r_{02}} + g_{m2} V_{01}$$

$$\frac{V_0}{r_{02}} = V_{01} \left[ \frac{1}{r_{02}} + g_{m2} \right]$$

$$V_0 = V_{01} + g_{m2} r_{02} V_{01}$$

$$V_0 = V_{01} \left[ 1 + g_{m2} r_{02} \right]$$

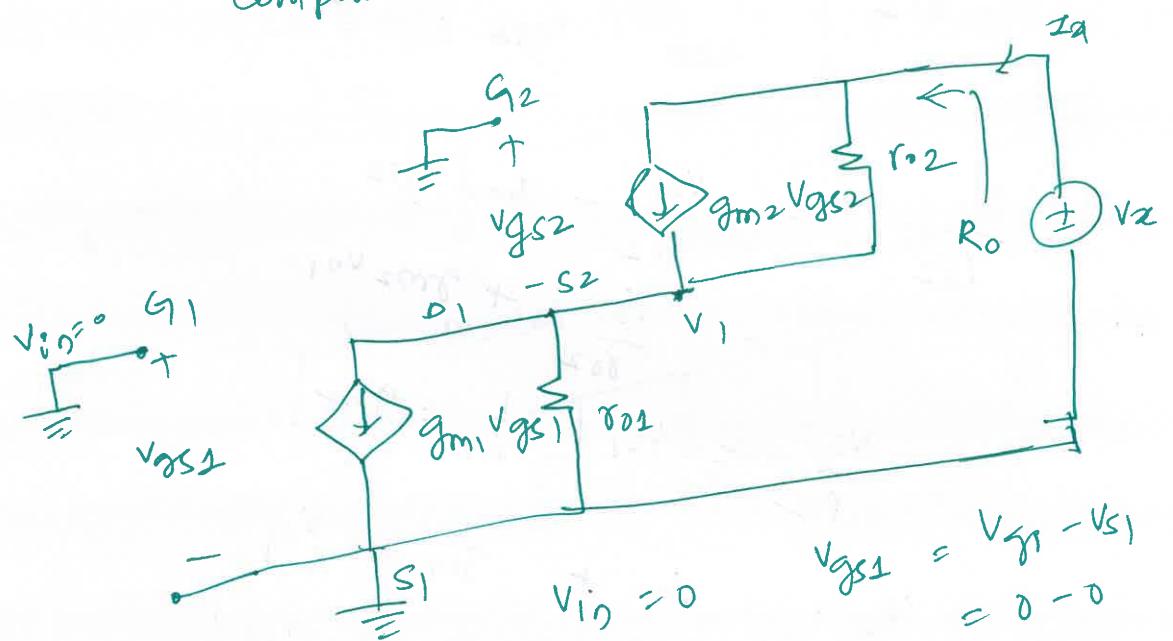
$$V_0 = -(g_{m1} r_{01} V_{01}) (1 + g_{m2} r_{02})$$

$$= -(g_{m1} r_{01}) V_i (1 + g_{m2} r_{02})$$

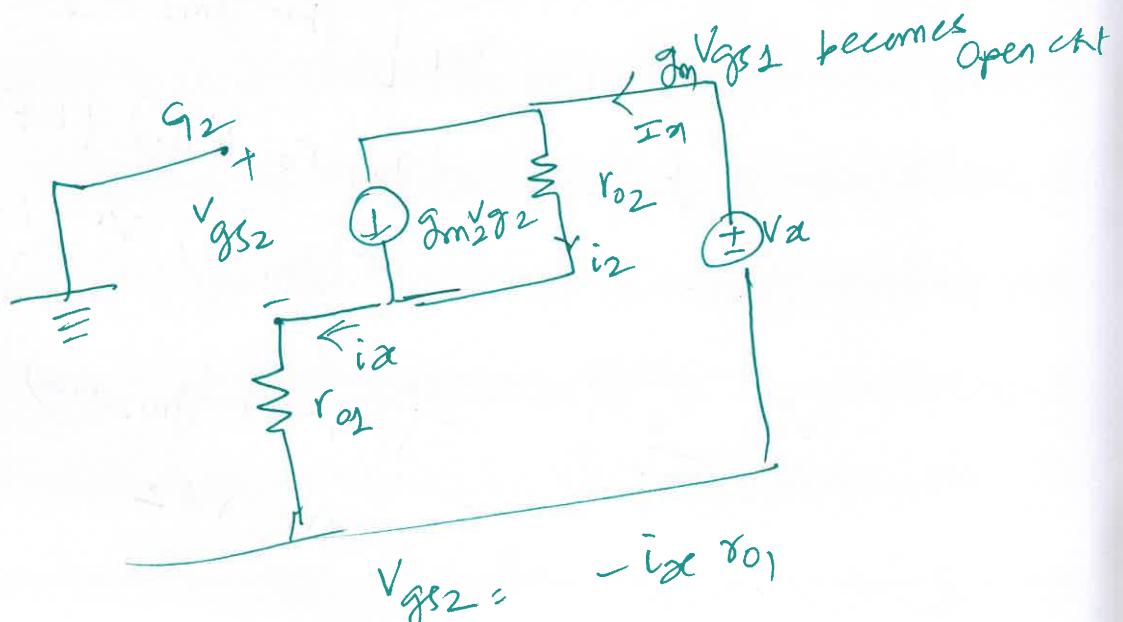
$$\text{so } \frac{V_0}{V_i} = - (g_{m1} r_{01}) (g_{m2} r_{02})$$

$$A_1 \times A_2$$

Cascode amplifier o/p resistance  
Set  $V_i = 0$  and attach a voltage source  $V_{\alpha}$ .  
Compute  $i_{\alpha}$ ,  $R_o = \frac{V_{\alpha}}{i_{\alpha}}$



$$V_{gs1} = V_{g1} - V_S \\ = 0 - 0$$



$$\text{here } i_2 = i_{\alpha} - g_m2 V_{gs2} \\ = i_{\alpha} - g_m2 (-i_{\alpha} r_o1) \\ = i_{\alpha} + g_m2 i_{\alpha} r_o1$$

$$i_2 = i_{\alpha} [1 + g_m2 r_o1] \quad \text{--- (1)}$$

$$-V_{\alpha} + i_2 r_o2 + i_{\alpha} r_o1 = 0 \quad \text{KVL eqn:}$$

$$V_{\alpha} = i_{\alpha} (1 + g_m2 r_o1) r_o2 + i_{\alpha} r_o1$$

$$R_o = \frac{V_{\alpha}}{i_{\alpha}} = r_o1 + r_o2 (1 + g_m2 r_o1) \\ = r_o1 + r_o2 + g_m2 r_o1 r_o2.$$

\* Cascode amplifier needs a large load to get a high gain

### Cascode amp Benefits:

1. Much better high frequency response  
(high gain bandwidth)
2. Simpler biasing

### Drawbacks:

1. Low voltage headroom ( $V_{DD}$  across 4 MOS)

\* Solve this problem by folded cascode.