

## dc model parameters

$$\text{Linear: } I_{DS} = \beta_N \left\{ (V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right\} \quad \beta_N = kP_N \cdot \frac{W}{L}$$

$$\text{Saturation: } I_{DS} = \frac{\beta_N}{2} (V_{GS} - V_{THN})^2 [1 + \lambda_n V_{DS}] \quad \lambda_N$$

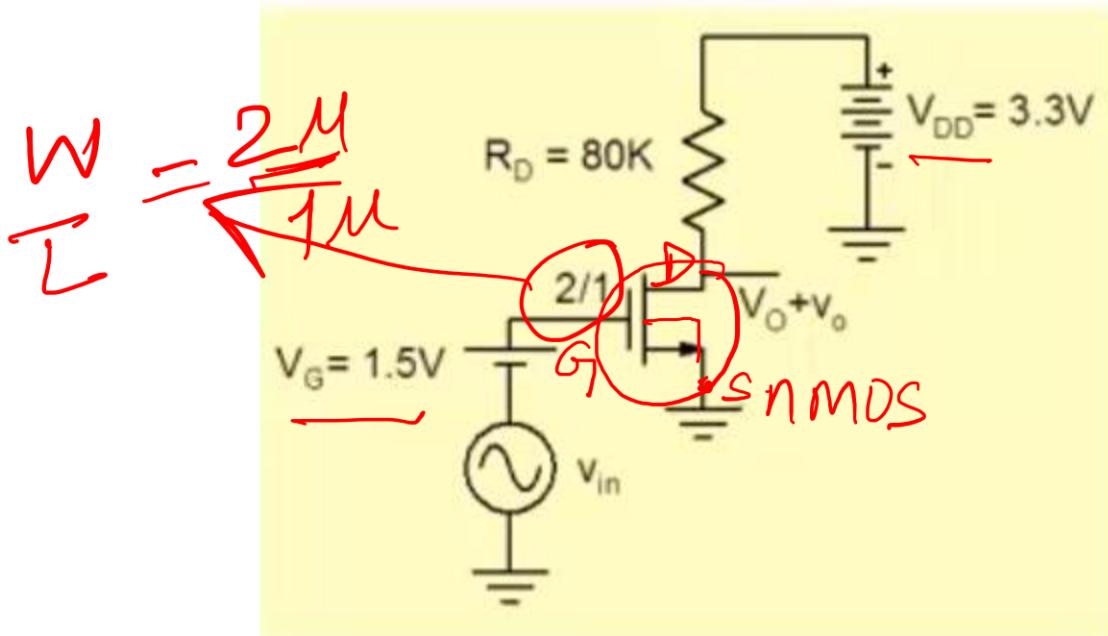
$$V_{THN} = V_{THN0} + \gamma (\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$$

$$V_{THN0} = 1V; \gamma = 0.7 V^{1/2}; 2\phi_F = 0.7V;$$

$$KP_N = 100 \mu A/V^2; L = 1 \mu m; \lambda = 0.01 V^{-1}$$

## Common Source Amplifier with Resistive load

Calculate  
Bias point → ac sources are shorted



✓ dc analysis

Assume : MOS is in saturation

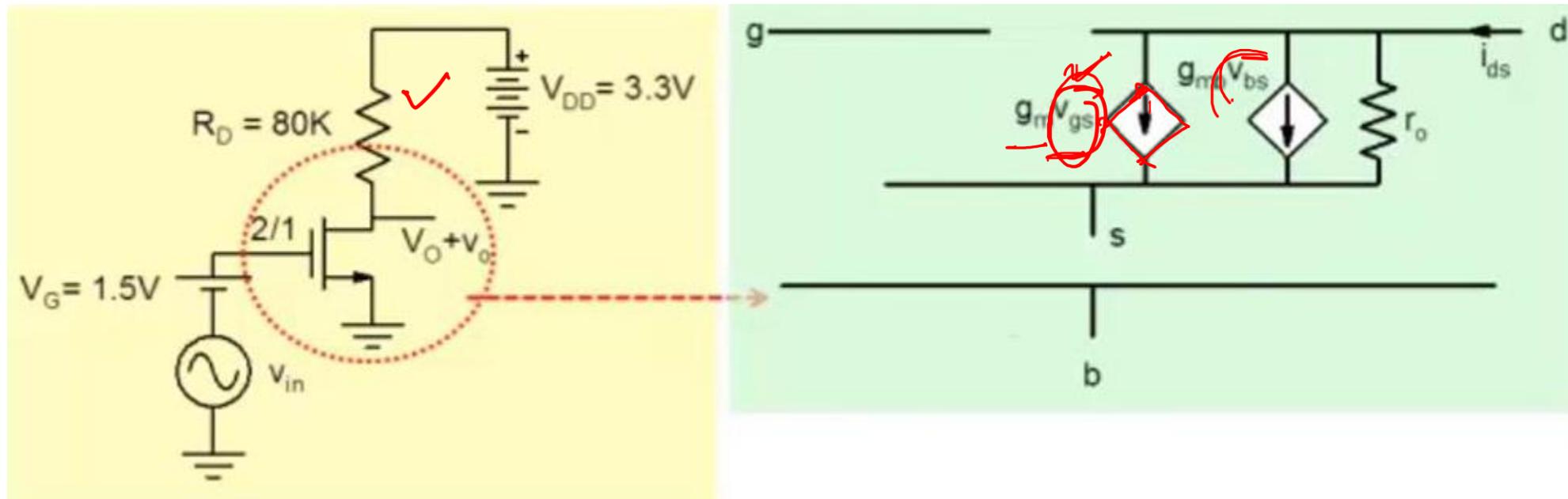
$$I_{DSQ} = \frac{\beta_n}{2} (V_{GS} - V_{TN})^2 = 25\mu A$$

$$V_{DSQ} = V_{DD} - I_{DSQ} \times R_D = 1.3V$$

$$3.3V - 25\mu A \times 80K = 1.3V$$

Bias point  $\Rightarrow \{ I_{DSQ}, V_{DSQ} \}$  ✓

Small Signal Model  $\rightarrow$  DC sources are shorted



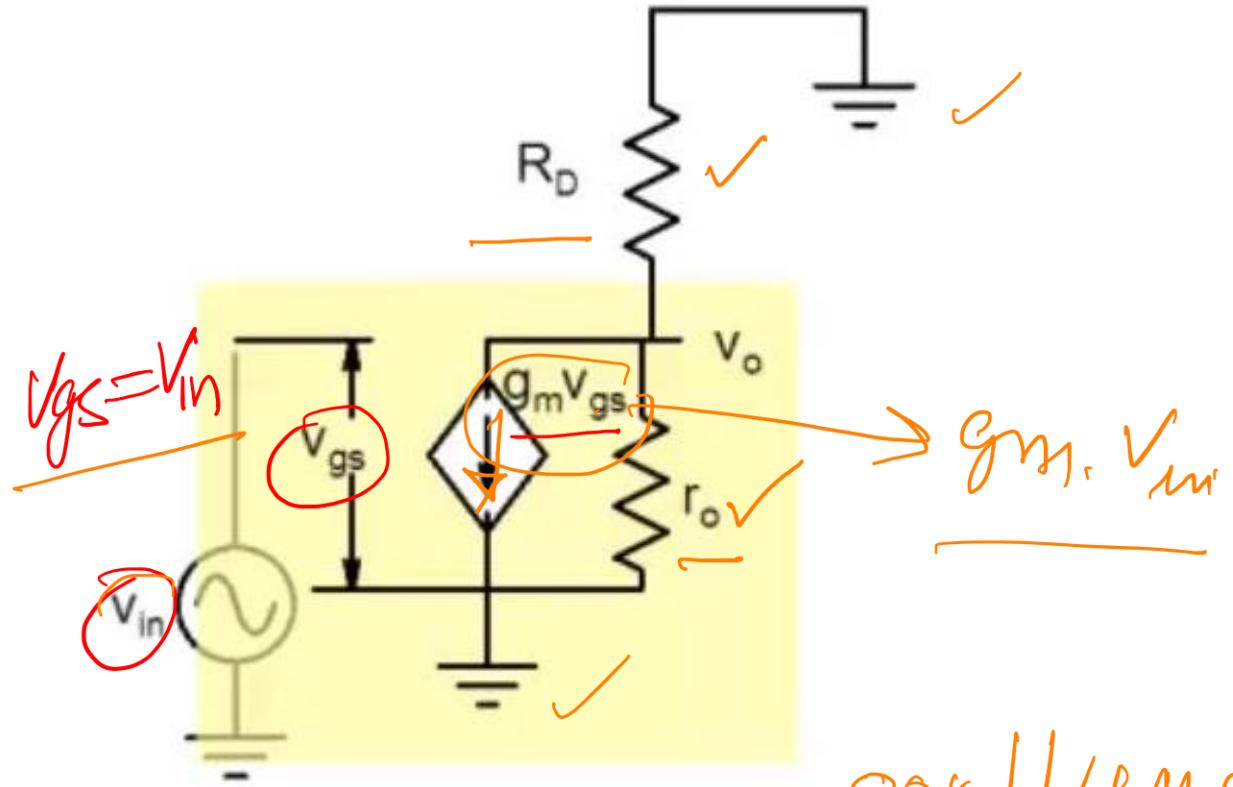
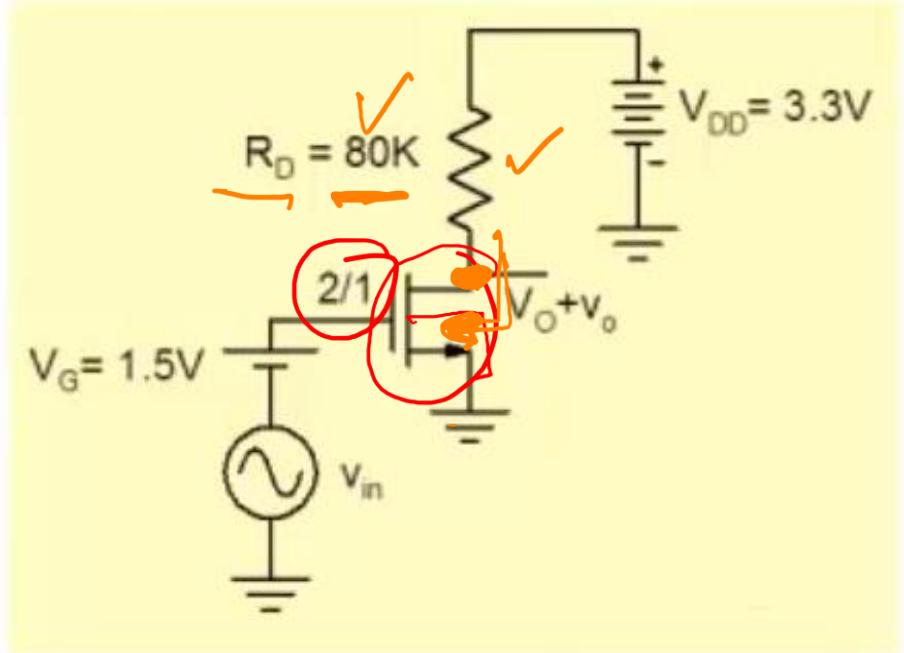
$$g_m = \frac{2I_{DSQ}}{V_{GSQ} - V_{THN}} = \sqrt{2I_{DSQ}\beta} = \underline{100\mu A/V}$$

$$r_o = \frac{1}{\lambda_n I_{DSQ}} = \underline{4M\Omega}$$

$$g_{mb} = g_m \cdot \eta = \underline{41.83\mu A/V}$$

$\rightarrow$  Now, we have small-signal terms) values

## ✓ 1. Voltage Gain ✓



$$80K \parallel 4M\Omega \approx 80K$$

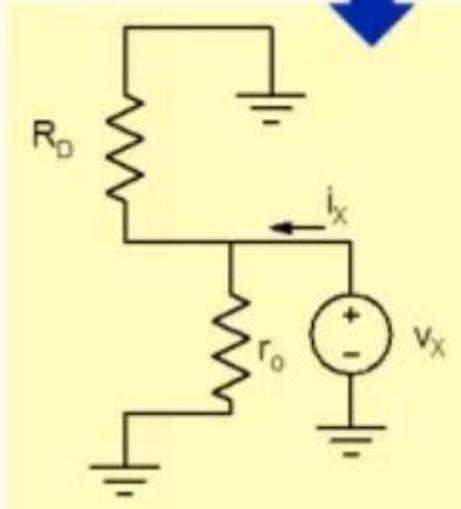
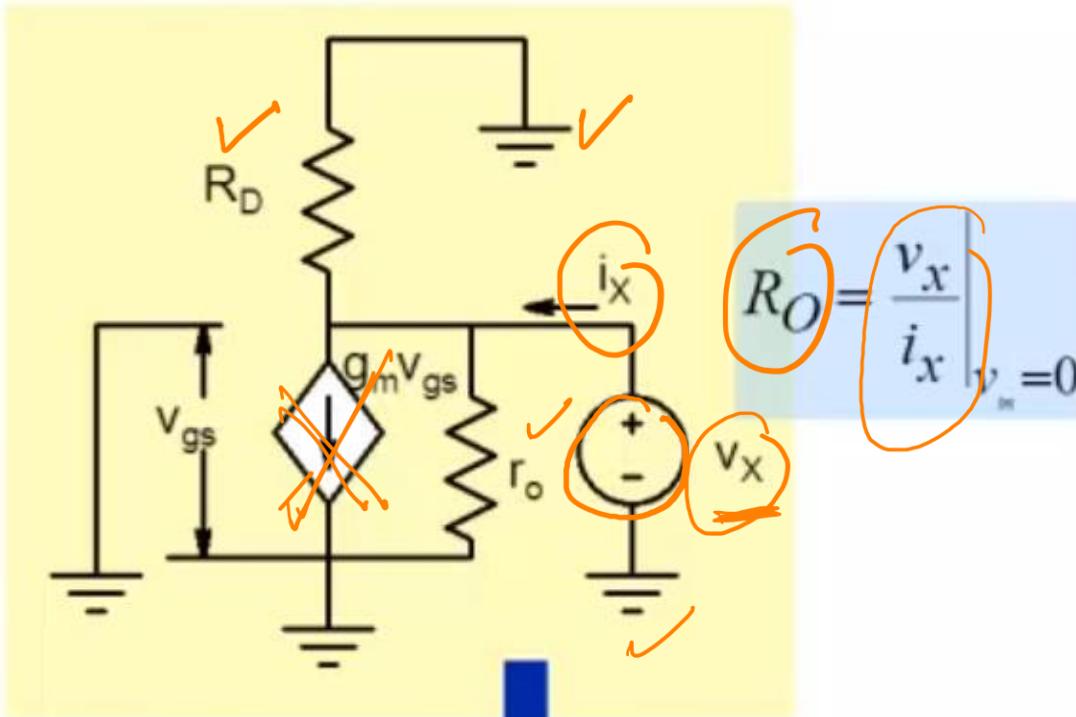
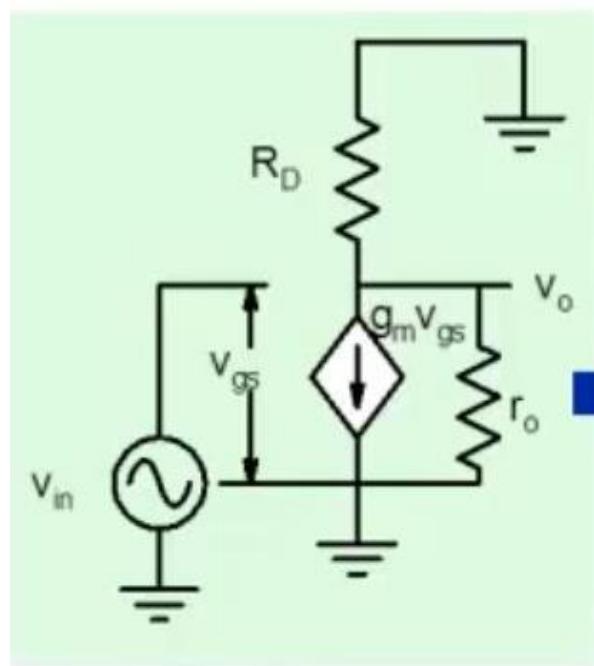
$$v_o = -g_m v_{in} \times R_D \parallel r_o$$

$$A_V = \frac{v_o}{v_{in}} = -g_m \times R_D \parallel r_o \approx -g_m R_D = -8$$

$$R_D \parallel r_o \approx R_D$$

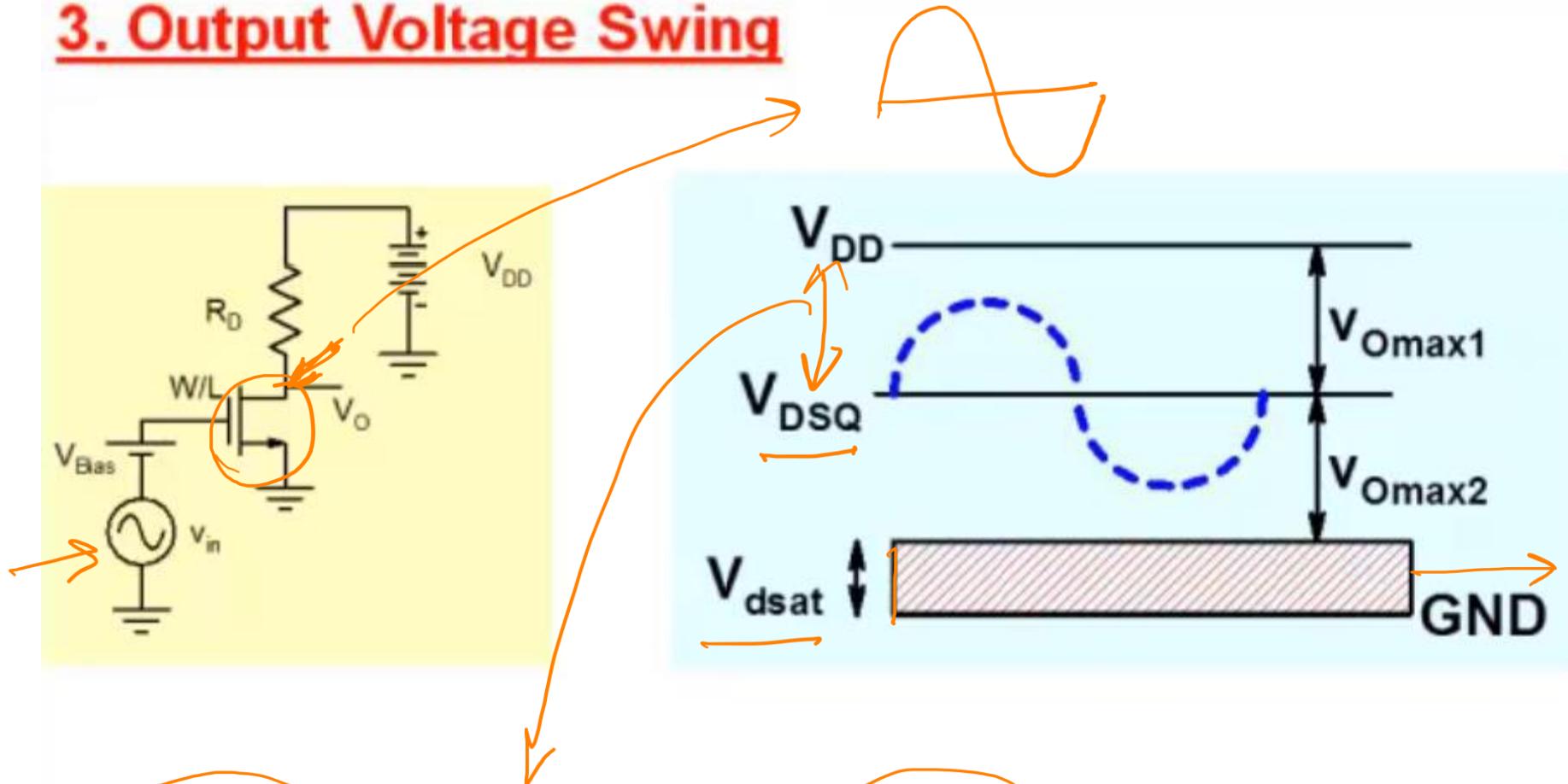
## 2. Output Resistance

To calculate o/p resistance  $\rightarrow$  Remove i/p source  
 $v_{gs} = 0$   $\downarrow$   
 $I = 0$



$$R_O = R_D \parallel r_o \approx R_D = 80K$$

### 3. Output Voltage Swing



$$v_{o\max 1} = V_{DD} - V_{DSQ}$$

$$v_{o\max 2} = V_{DSQ} - V_{dsat}$$

$$v_{o\max} = \text{Min}\{v_{o\max 1}; v_{o\max 2}\}$$

[However, this will not match with actual results/values]



## Voltage swing limited by harmonic distortion

- Harmonic distortion in CS amplifier occurs because the relationship between drain current and gate voltage is nonlinear.

$$I_{DSQ} + i_{ds} = \frac{\beta}{2} \times (V_{GSQ} + v_{gs} - V_T)^2$$

$$i_{ds} = g_m v_{gs} + \left( \frac{0.5}{V_{GSQ} - V_T} \right) \times g_m v_{gs}^2$$

Let's take

$$v_{gs} = a_o \sin(2\pi f_o t)$$

$$i_{ds} = g_m a_o \sin(2\pi f_o t)$$

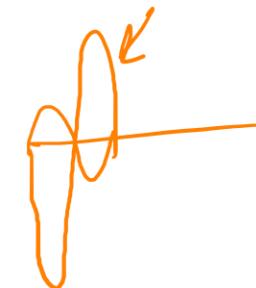
$$+ \left( \frac{a_o^2 g_m}{4(V_{GSQ} - V_T)} \right)$$

$$- \left( \frac{a_o^2 g_m}{4(V_{GSQ} - V_T)} \right) \cos(2\pi 2f_o t)$$

Re-arrangement

amplitude

wanted



$$HD_2 (\%) =$$

$$HD_2 (\%) = \frac{a_o / 4}{V_{GSQ} - V_T} \times 100$$

Amplitude distortion

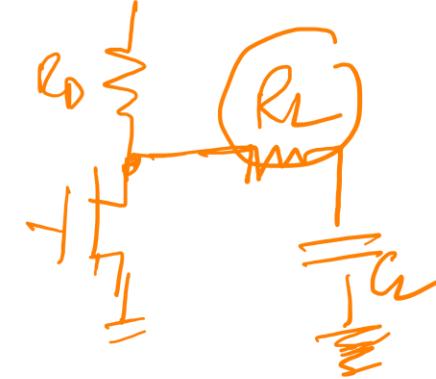
$$\frac{a_o^2}{4(V_{GSQ} - V_T)} \times 100$$

Cont  
(DC) elimination by C<sub>gs</sub>

## Output Voltage Swing

$$v_{in} = a_o \sin(2\pi f_o t)$$

$$HD_2 (\%) = \frac{a_o / 4}{V_{GSQ} - V_T} \times 100 = \frac{v_{in}}{V_{dsat}} \times 25$$



$$\checkmark v_{in} = \frac{HD_2}{25} \times V_{dsat}$$

put for the sake of completeness

Now,

$$A_V = \frac{v_o}{v_{in}} \approx g_m R_D \parallel R_L \times v_{in}$$

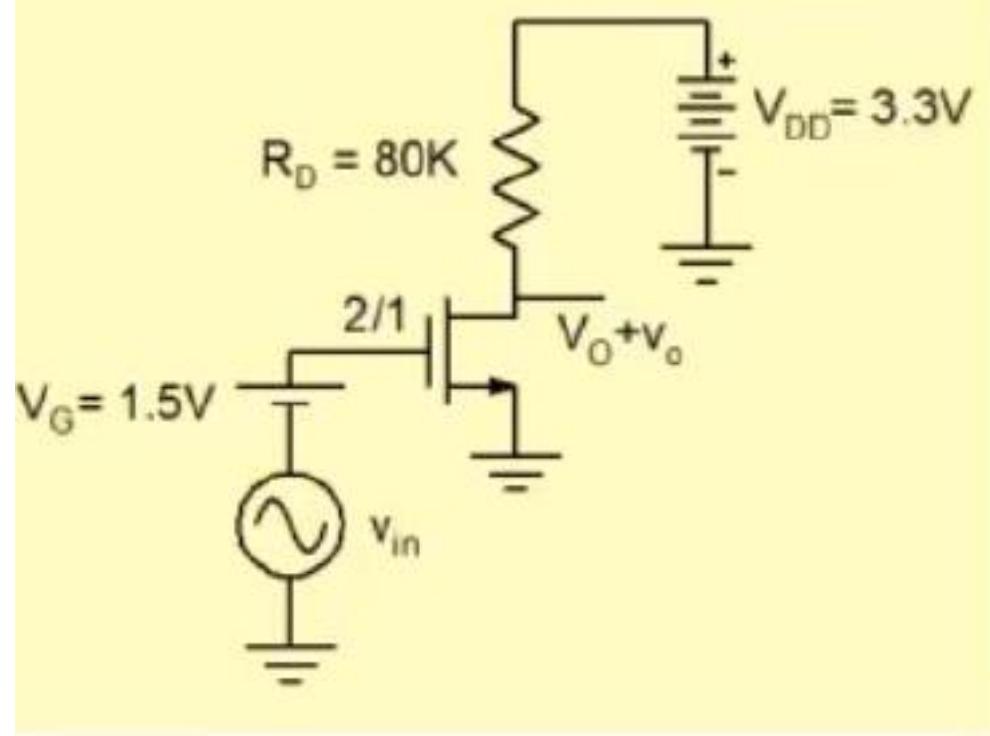
$$v_{o\max 3} \cong I_{DSQ} R_D \parallel R_L \times \frac{HD_2}{12.5}$$

$$g_m = \frac{2I_{DSQ}}{V_{GSQ} - V_T}$$

( This is the swing determined by the distortion)

$$v_{o\max 1} = V_{DD} - V_{DSQ} = I_{DSQ} R_D$$

$$v_{o\max 3} < v_{o\max 1}$$



$$V_{DSQ} = \underline{1.3V}; V_{sat} = \underline{0.5V}$$

$$v_{o \max} \leq V_{DSQ} - V_{sat} = 0.8V$$

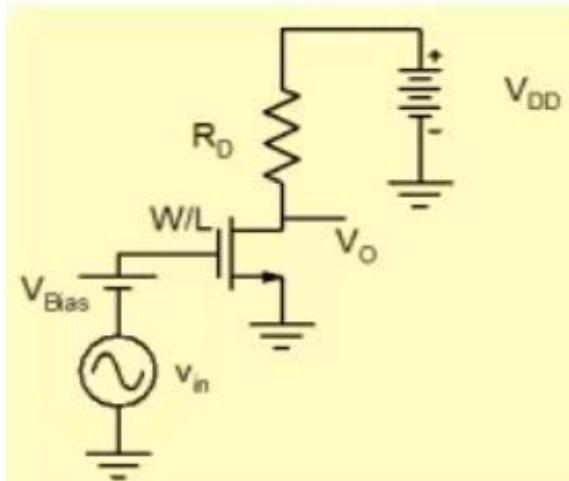
$$\underline{v_{omax}} \cong I_{DSQ} R_D \| R_L \times \frac{H D_2}{12.5}$$

$= 0.8V$  for  $H D_2 = 5\%$

$$\frac{25\text{mA} \cdot 80\text{k} \cdot \frac{5}{12.5}}{25 \times 10^3 \cdot \frac{80 \times 10^3}{12.5}} = 0.8\text{V}$$

# Design Problem

How to get the maximum swing (at given  $V_{DD}$ )



$$v_o \approx I_{DSQ} R_D \| R_L \times \frac{HD_2}{12.5} \quad \checkmark$$

( $v_{o\max}$ )

$$v_o \leq V_{DSQ} - V_{sat}$$

( $v_{o\max 2}$ )

**Optimum drain-source bias**

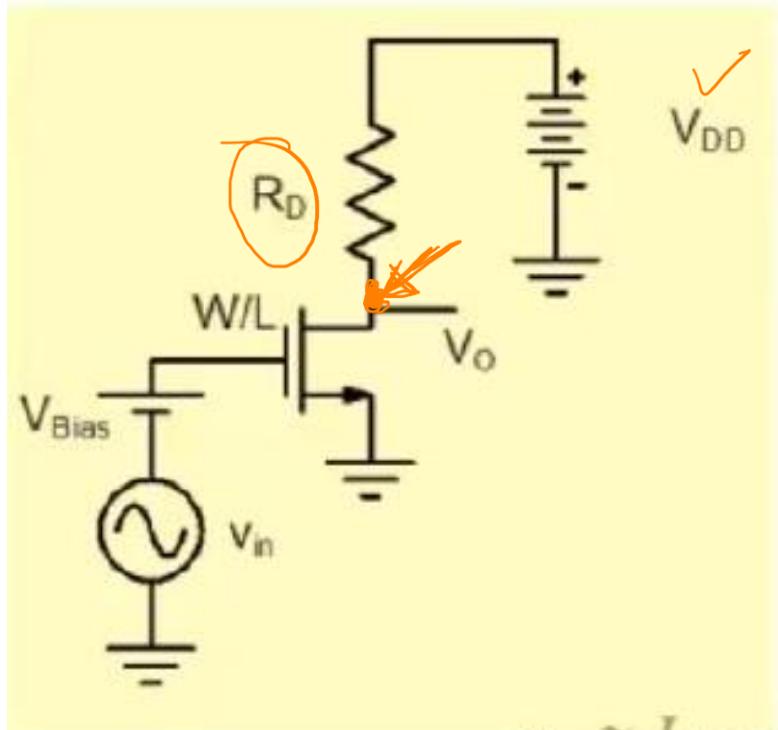
$$I_{DSQ} R_D \times \frac{HD_2}{12.5} \times \frac{1}{1 + R_D/R_L} = V_{DSQ} - V_{sat}$$

$$V_{DSQ} = \frac{V_{DD} \times \frac{HD_2}{12.5} + V_{sat}}{1 + \frac{HD_2}{\chi}}$$

$$v_{o\max} = \frac{V_{DD} - V_{sat}}{1 + \frac{\chi}{HD_2}}$$

$$\chi = 12.5 \times (1 + R_D/R_L)$$

## Voltage Gain (including voltage swing)



$v_o \approx I_{DSQ} R_D \| R_L \times \frac{HD_2}{12.5}$

one limit

Trade off  
Gain - voltage swing

$$A_V = -g_m R_D$$

$g_m = \sqrt{2I_{DSQ}\beta}$

$$R_D = \frac{V_{DD} - V_{DSQ}}{I_{DSQ}}$$

$A_v = \sqrt{\frac{2\beta}{I_{DSQ}}} \times (V_{DD} - V_{DSQ})$

Max CO ×  $\frac{W}{L}$

$$v_o \leq V_{DSQ} - V_{sat}$$

second limit

$$V_{DSQ} > V_{sat}$$

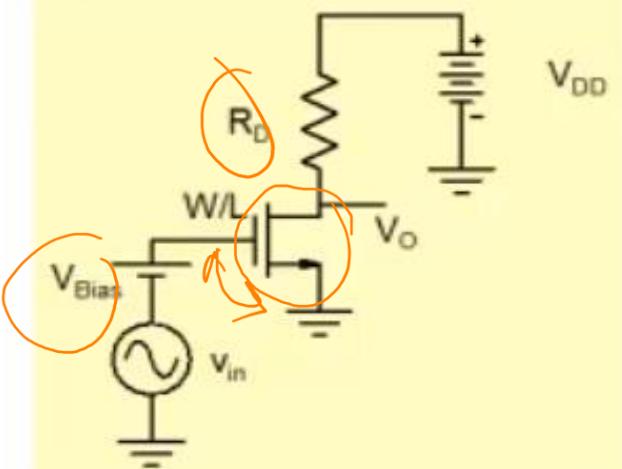
$$A_v \leq \sqrt{\frac{2\beta}{I_{DSQ}}} \times (V_{DD} - v_{om}) + \sqrt{\frac{2I_{DSQ}}{\beta}}$$

max voltage swing

$$I_{DSQ} = \frac{\beta}{2} (V_{GS} - V_T)$$

$$\sqrt{2I_{DSQ}} = (V_{GS} - V_{sat})$$

How to improve gain (for example)



fix

$$I_{DS} = 25 \mu A \text{ and } v_{om} = 0.1V, \\ R_D = 108k$$

High width  
Cap  
B.W.

W ( $\mu m$ )	A <sub>V</sub>	V <sub>GS</sub> (V)
2	10.8	1.5
5	18.24	1.316
10	26.6	1.22
20	38.47	1.158
50	62	1.1
100	88.5	1.07

$$A_V \leq \frac{2\beta}{\sqrt{I_{DSQ}}} \times (V_{DD} - v_{om}) - \sqrt{\frac{2I_{DSQ}}{\beta}}$$

1 fix  $W=2\mu m$  and  $v_{om} = 0.1V$  → low swing

for example  
May be we want to use this opamp in first stage

I <sub>DS</sub> ( $\mu A$ )	A <sub>V</sub>	R <sub>D</sub> (M $\Omega$ )	V <sub>GS</sub> (V)
100	4.4	0.022	2
50	7.05	0.05	1.707
25	10.8	0.108	1.5
10	18.2	0.29	1.316
5	26.6	0.59	1.224
2	43.2	1.53	1.14
1	62	3.1	1.1

Low current or large size is needed to obtain large gain.

→ High R

Gain saturates as transistor gets closer to threshold voltage

Not good for fabrication  
↓ Sub-VT

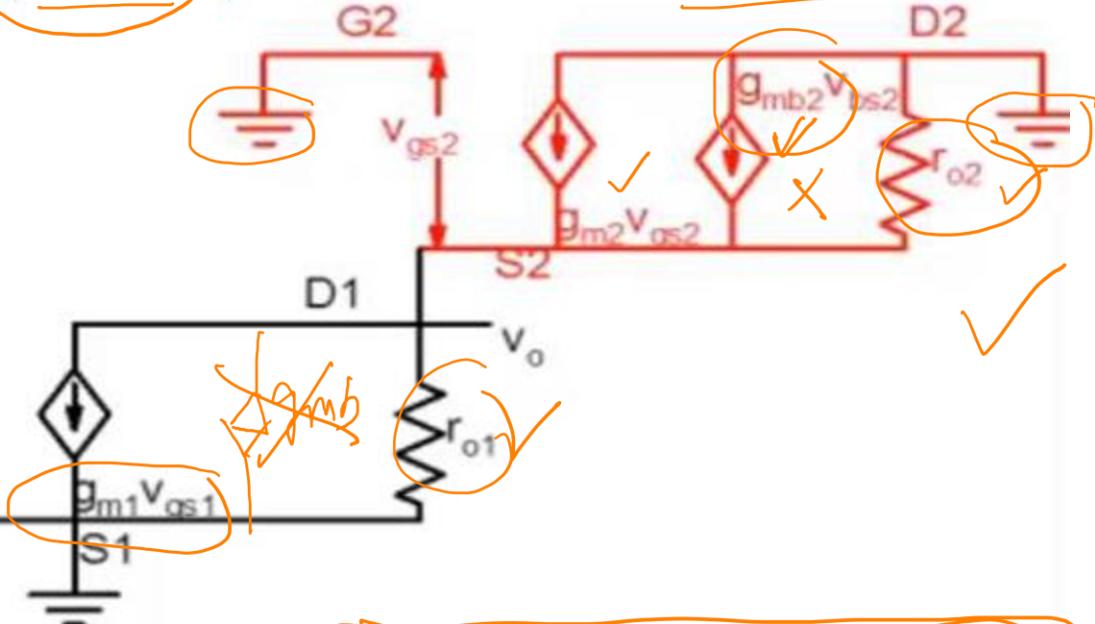
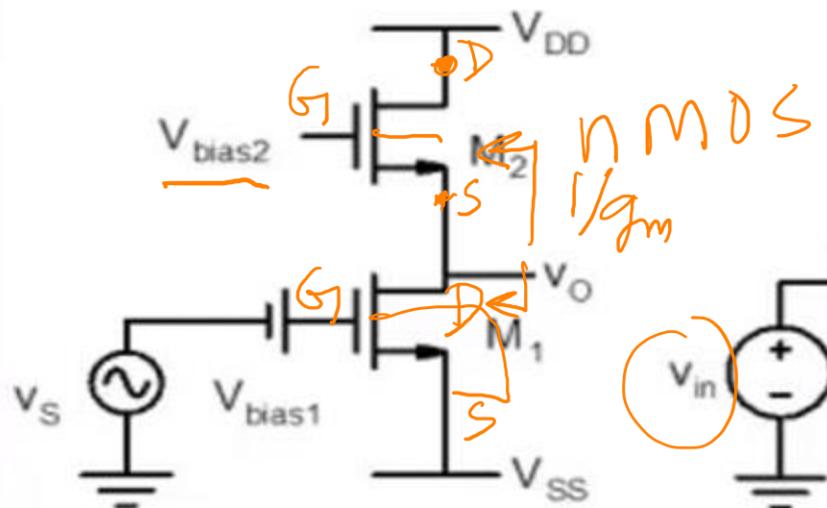
$$V_{TH} = IV$$

so V<sub>TH</sub> decrease

↓ Sub-VT

**CS amplifier with Active Load**

## CS Amplifier with Active Load (NMOS)



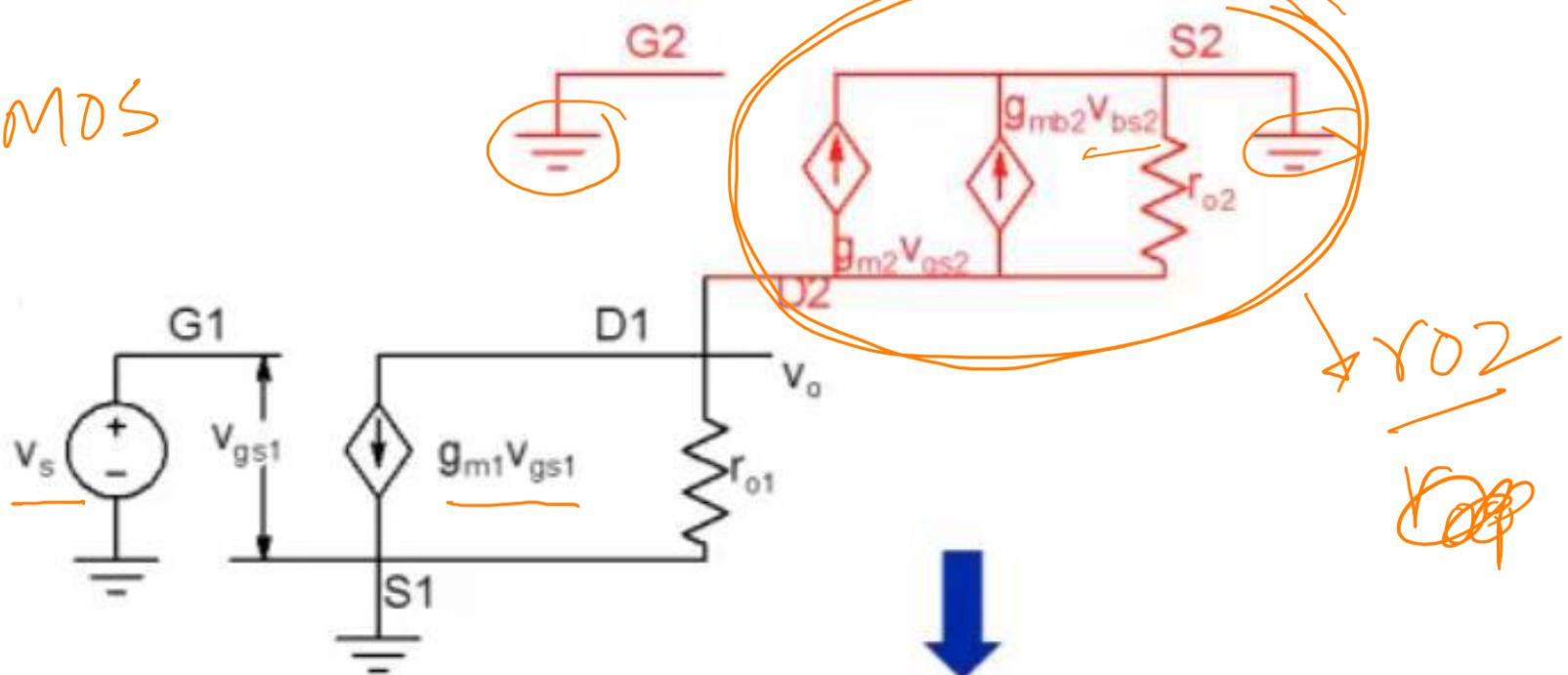
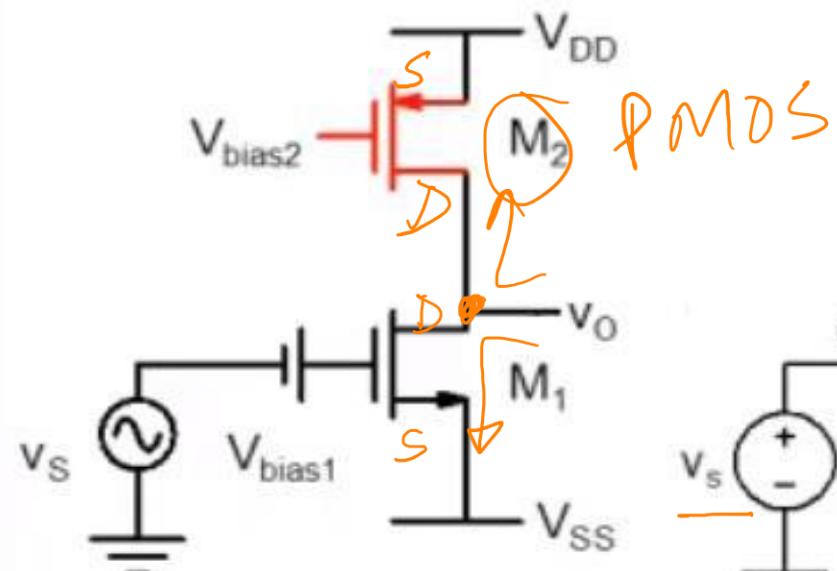
$$v_o = -g_{m1} v_{in} \times \left\{ r_{o1} \parallel r_{o2} \parallel \frac{1}{g_{m2}(1+\eta)} \right\}$$

$$A_V \cong - \frac{g_{m1}}{g_{m2}(1+\eta)}$$

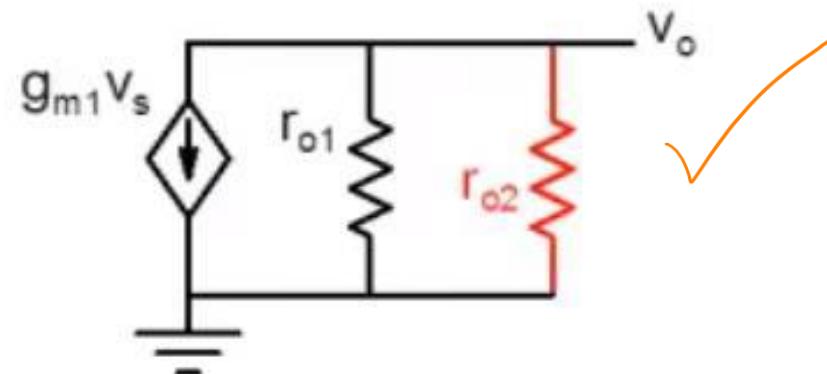
$$= \frac{\sqrt{2KP \times (W/L)_1 \times I_{DSQ1}}}{\sqrt{2KP \times (W/L)_2 \times I_{DSQ1}}} \times \frac{1}{1+\eta}$$

$$= \frac{\sqrt{(W/L)_1}}{\sqrt{(W/L)_2}} \times \frac{1}{1+\eta} = \frac{1}{10/2.5} \times \frac{1}{1+1.5} \times \frac{L}{10/2.5} \times g_{m2}(1+\eta)$$

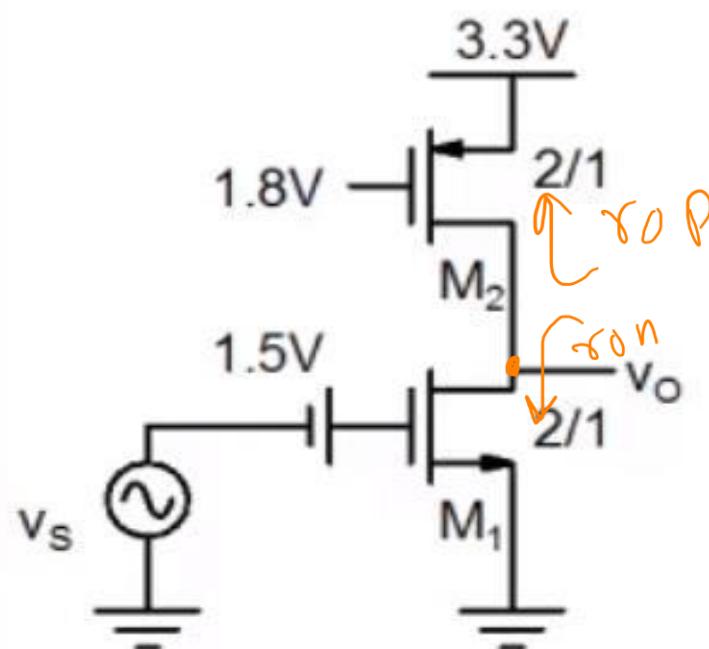
## CS Amplifier with PMOS active load



$$A_V = -g_{m1} \times r_{o1} \parallel r_{o2}$$



## Example



$$I_{DSQ} = 25 \mu A; V_{DSQ} = 1.65(?)$$

$$g_{mn} = g_{mp} = 100 \mu A/V; r_{on} = r_{op} = 4 M\Omega$$

$$|A_V| = g_{mn} \times r_{on} \parallel r_{op}$$

$$= -200$$

$$R_o = r_{on} \parallel r_{op} = 2 M\Omega$$

Large gain is easily obtained without requiring large resistors which are difficult to fabricate