ANALOG ELECTRONIC CIRCUITS

LAB REPORT-5

BJT Amplifiers

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Components Used

- **Power Supply**
- **Digital Storage Oscilloscope (DSO)**
- **Resistors:** 5.6 kΩ, 1 kΩ, RC, RE
- **Capacitors:** 10 µF, 440 pF
- **BJT Transistor**
- **Function Generator**

1) DC Analysis :

To find the values of RC and RE for the given conditions

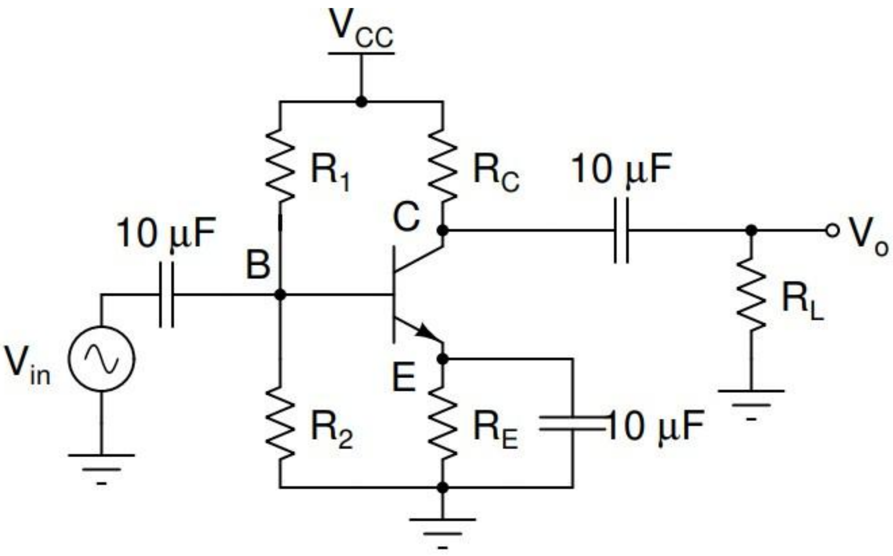


Figure 1: Single stage common emitter voltage amplifier

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$V_E = V_B - V_{BE}$$

$$V_C = V_{CC} - I_C R_C$$

$$I_E = \frac{V_E}{R_E}$$

$$I_C = \frac{\beta}{\beta + 1} I_E$$

$$I_B = \frac{I_E}{\beta + 1}$$

R1=5.6 k ohm and R2= 1k ohm [Given] ;

Collector- current(Ic)=1.5m A ;

RL = 1 kΩ and VCC = 12 V

Mid-band voltage gain(Vout/Vin) = 5

Beta = 150

VBE = 0.7V

1. **Base Voltage (VB):**
   VB = (R2 / (R1 + R2)) * VCC
   Given R1 = 5.6 kΩ, R2 = 1 kΩ, and VCC = 12 V:
   VB = (1 kΩ / (5.6 kΩ + 1 kΩ)) * 12 V = 1.82 V

2. **Emitter Voltage (VE):**
   VE = VB - VBE
   Assuming VBE = 0.7 V:
   VE = 1.82 V - 0.7 V = 1.12 V

3. **Emitter Current (IE):**
   IE = VE / RE
   Given IC ≈ IE = 1.5 mA:
   RE = VE / IE = 1.12 V / 1.5 mA = 745.45

R_C and R_E calculations

$$R_E = \frac{V_E}{I_E}$$

$$I_E = \frac{I_C \beta}{\beta+1}$$ $\beta = 150$

$I_C = 1.5mA$ collector current

$$= (1.5 \times 10^{-3})\left(\frac{151}{150}\right)$$

$$V_E = V_B - V_{BE}$$

$$= \left(\frac{R_2}{R_1+R_2}\right) V_{CC} - V_{BE}$$

$$= \frac{5.6k}{1+5.6k} \cdot 12 - 0.7$$

$$\Rightarrow R_E = \frac{V_E}{I_E} = 745.454\Omega$$

R_C:-

$A_V = g_m R_O$

$g_m = \frac{I_C}{V_T}$

$R_O = R_C \parallel R_L$

$R_O = \frac{A_V \cdot V_T}{I_C}$ $\left[\begin{array}{l} V_T = 26mV \\ A_V = 5 \quad I_C = 1.5mA \\ \text{(voltage gain)} \end{array} \right]$

$$\frac{1}{R_O} = \frac{1}{R_C} + \frac{1}{R_L}$$

$$\frac{1}{R_O} = \frac{I_C}{A_V V_T} = \frac{1}{R_C} + \frac{1}{R_L}$$

$$R_C = 90\Omega$$

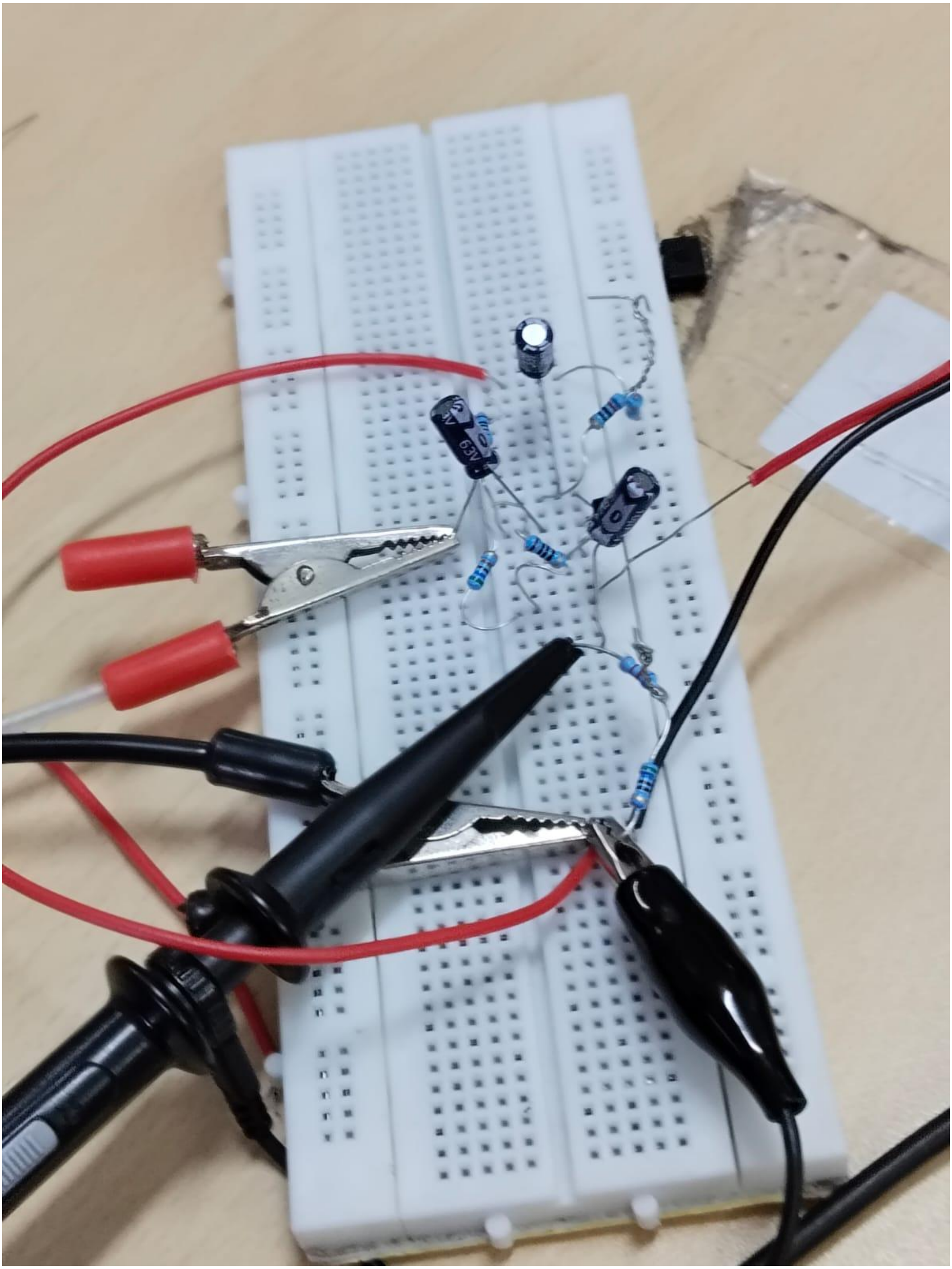
From the DC Analysis we got values of R_E and Rc R_E =745.45 ohm

Rc = 96.1514 ohm

2) Transient Response and Total Harmonic Distortion:

Objective: To find the total harmonic distortion at different input voltages

After connecting the circuit as shown in the fig



(1A) From the above calculations we can ~~take~~ Say (3)

$R_C = 94\Omega$

$R_E = 730\Omega$

By taking Vin with amplitude 25 mV

Vo: (165 mV) (peak to peak)

$\Rightarrow gain = \frac{165}{50} = 3.3$

(2)

b)

Input:

Vin= Sine wave of amplitude 25 mV

Freq=1 kHz

RL =1 k ohm

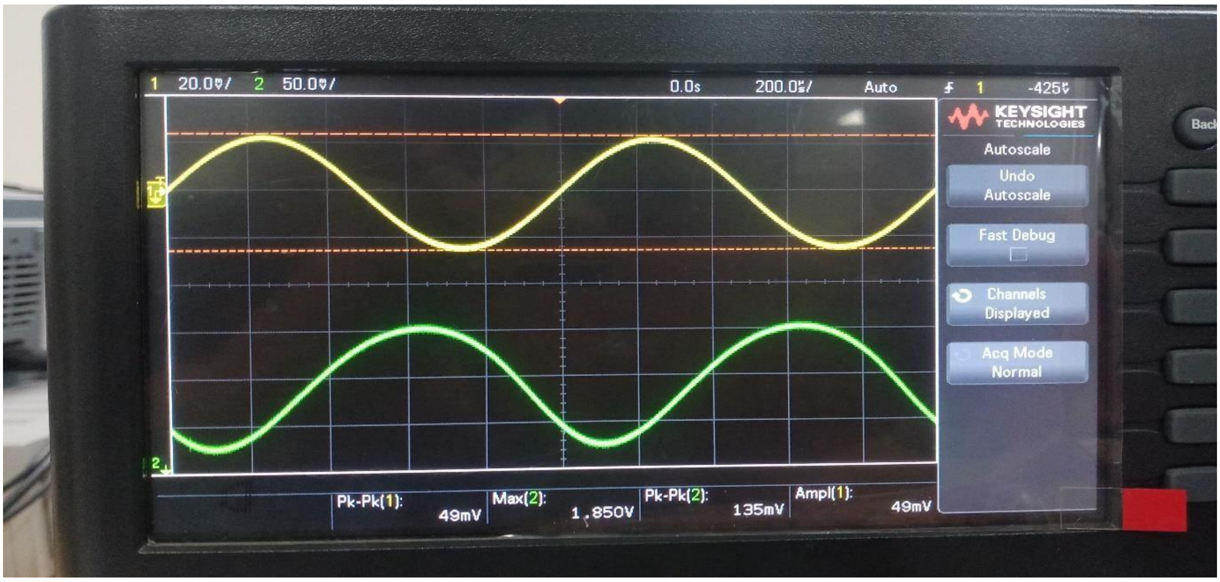
c)

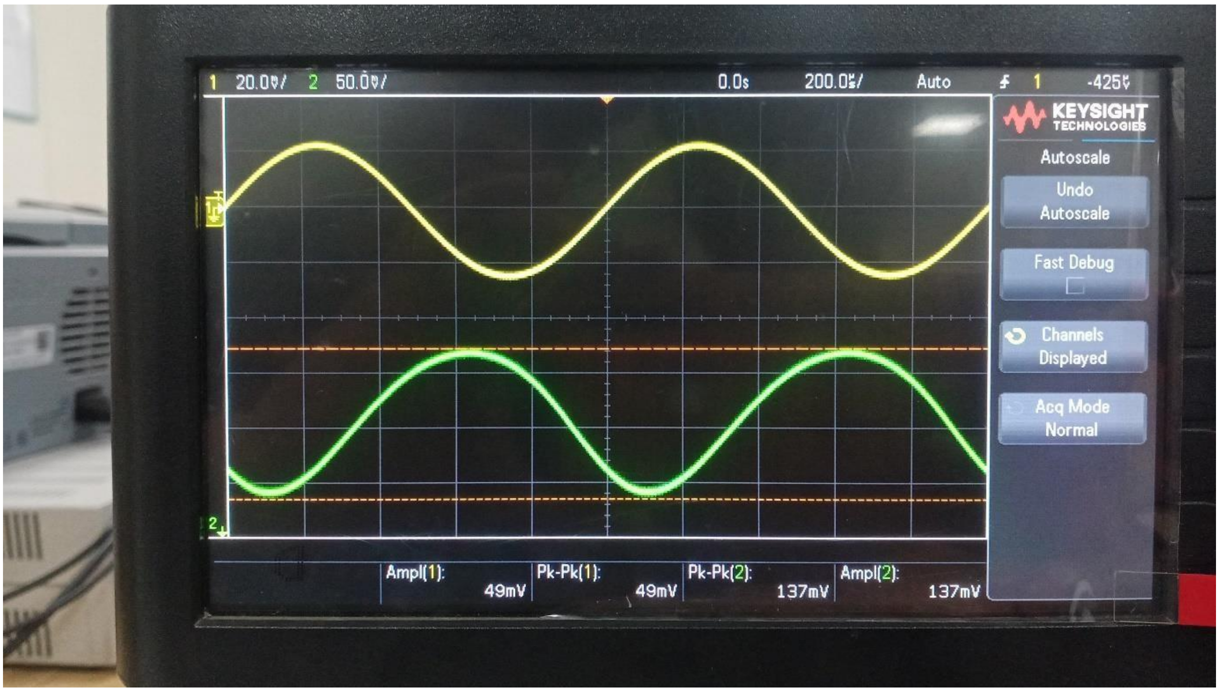
Now measure the amplitude of the output voltage (Vo) produced by the amplifier. Then, calculate the voltage gain (Av) of the amplifier by dividing the output voltage amplitude by the input voltage amplitude.

gain=gm * Ro =$I_C/V_T(R_C||R_L)$

=1.5/25 * (980* 100)/1080=5.44

Theoretical gain=5.44.





From above Aanlysis:

Vo=137mV

Vin=49mV

Therefore gain =V0/Vin =>165/50 3.3

Hence gain= 3.3

d)

Now record the amplitudes of the fundamental component (V1) and the 2nd to 5th harmonics for various amplitudes (Vin) of the input signal.

The suggested values for Vin are 2 mV, 10 mV, 20 mV, 50 mV, 100 mV, 500 mV, and 1 V.

Then use FFT analysis to measure the harmonics.

Calculate THD

THD= sqrt((V2²)+(V3²)+(V4²)+(V5²)/V1²)

Vin	V_1	Harmonic 2	H3	H4	H5	THD
40mV	130mV	48	67.5	83.3	89.2	1.13
50mV	160mV	45	62	81.2	85.2	0.87
60mV	200mV	42	59.3	77.8	84.5	0.67

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}$$

if $V_1 = 130mV$ [Vin = 40mV]

~~THD~~ = THD = 1.13

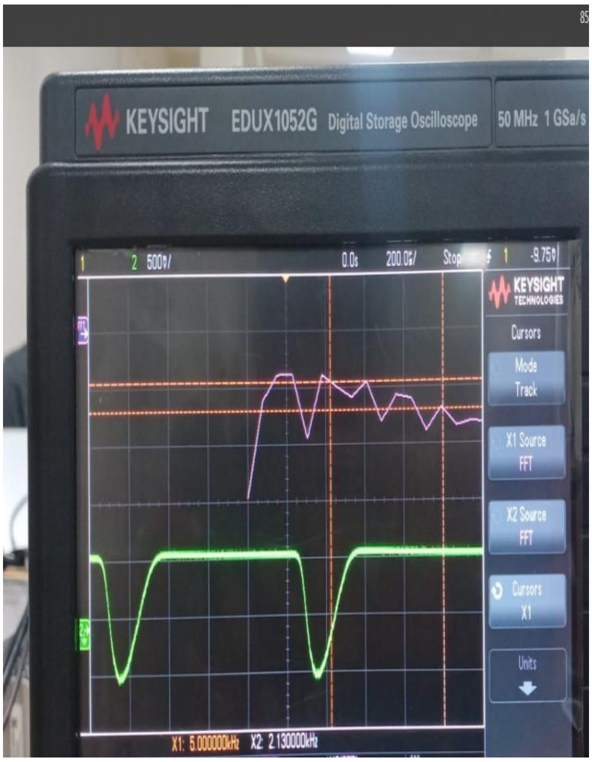
if $V_1 = 160mV$ [Vin = 50mV]

THD = 0.87

if $V_1 = 200mV$ [Vin = 60mV]

THD = 0.67


0.0s
Stop
KEYSIGHT TECHNOLOGIES
Cursors
Mode
Track
X1 Source
FFT
X2 Source
FFT
Cursors
X1
Units
X1: 1.000000kHz X2: 2.130000kHz


KEYSIGHT EDUX1052G Digital Storage Oscilloscope
50 MHz 1 GSa/s
0.0s
200.0
Stop
-9.75
KEYSIGHT TECHNOLOGIES
Cursors
Mode
Track
X1 Source
FFT
X2 Source
FFT
Cursors
X1
Units
X1: 5.000000kHz X2: 2.130000kHz


1.00V/
0.0s
200.0
Stop
-29.8
KEYSIGHT TECHNOLOGIES
Cursors
Mode
Track
X1 Source
FFT
X2 Source
FFT
Cursors
X1
Units
X1: 1.000000kHz X2: 2.130000kHz


KEYSIGHT EDUX1052G Digital Storage Oscilloscope
50 MHz 1 GSa
1.00V/
0.0s
200.0
-29.8
KEYSIGHT TECHNOLOGIES
Cursors
Mode
Track
X1 Source
FFT
X2 Source
FFT
Cursors
X1
Units

3)Frequency Response:

a)

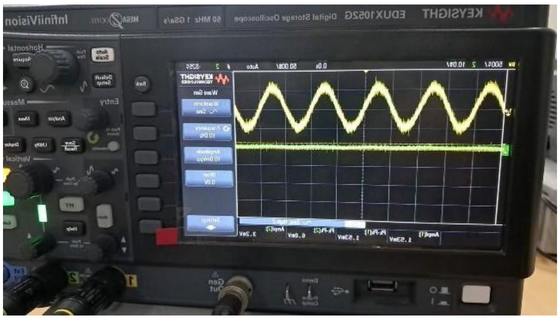
Input :

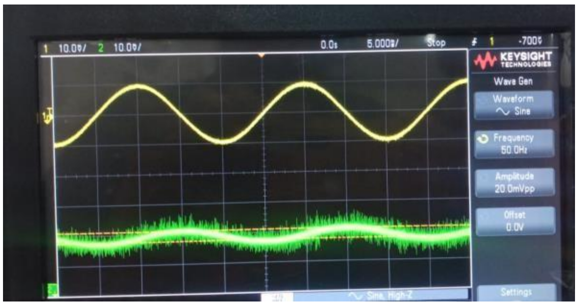
R(Load)=1 k ohm

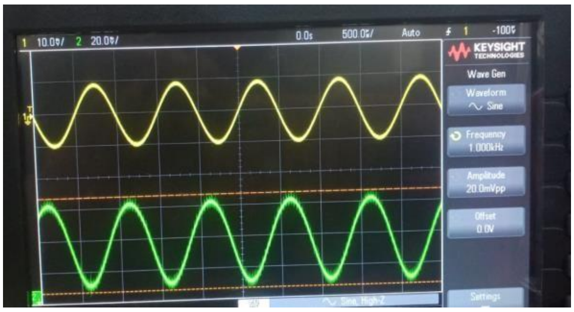
Vin=10 mV

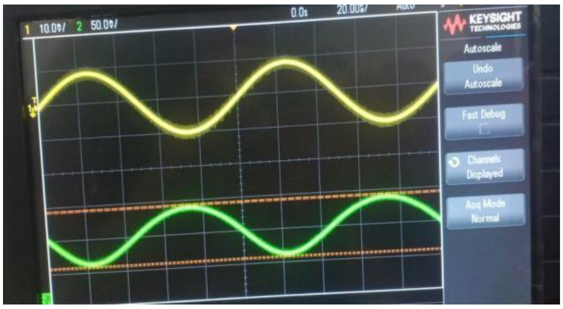
To find the voltage gain at different frequencies with a 10 microfarad capacitor and 440 picofarad capacitor and calculate the fL and fH

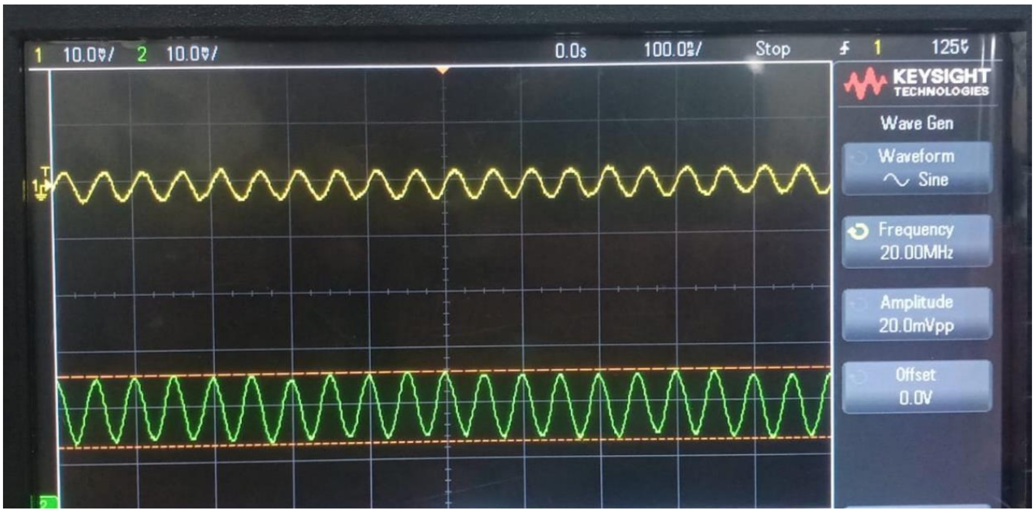
Vary Fin from 10 Hz to 20 MHz











We cannot find FH

Max dB = 14.89 dB

f_L is frequency at 11.89 dB

= 500Hz (501.2Hz)

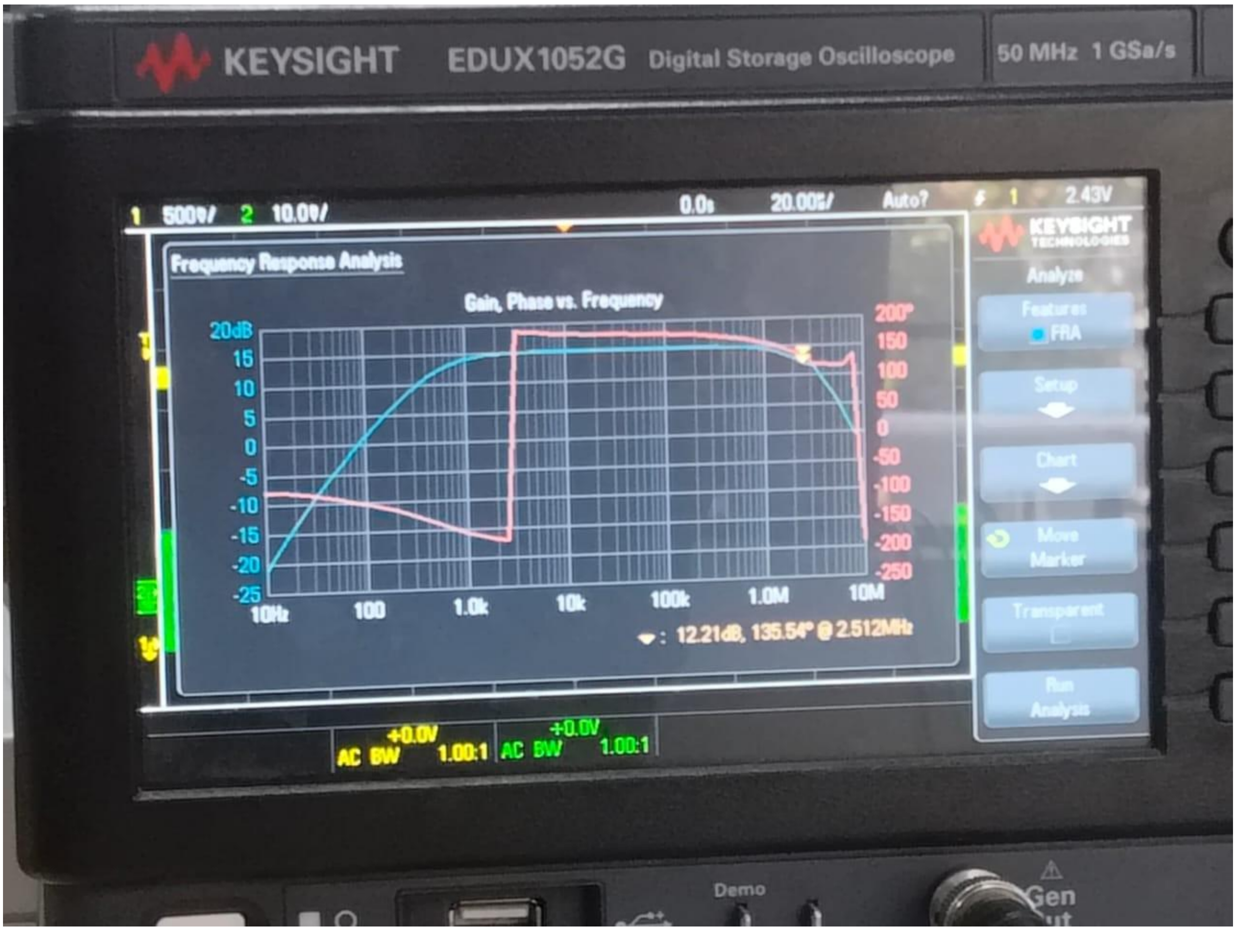
f_H cannot be found because it is above 20MHz

The readings are noted under the table below.

f_{in}	V_{in}	V_o	$A_v = \frac{V_{in}}{V_o}$
10Hz	20mV	1mV	-24 dB
50Hz	20mV	10mV	-5.25 dB
100Hz	20mV	22mV	0.96 dB
500Hz	20mV	77mV	11.82 dB
1KHz	20mV	98mV	13.84 dB
10KHz	20mV	111mV	14.89 dB
100KHz	20mV	108mV	14.68 dB
1MHz	20mV	108mV	14.71 dB
10MHz	20mV	89mV	13.03 dB
20MHz	20mV	86mV	12.70 dB

b)

F_L= 156.8 (approx)


KEYSIGHT
EDUX1052G Digital Storage Oscilloscope
50 MHz 1 GSa/s
Frequency Response Analysis
Gain, Phase vs. Frequency
20dB
15
10
5
0
-5
-10
-15
-20
-25
200°
150
100
50
0
-50
-100
-150
-200
-250
10Hz
100
1.0k
10k
100k
1.0M
10M
: 12.21dB, 135.54° @ 2.512MHz
Analyze
Features
FRA
Setup
Chart
Move Marker
Transparent
Run Analysis
AC BW 1.00:1
AC BW 1.00:1

f_{in}	V_{in}	V_o	A_v
10Hz	20mV	0.0018 (2mV)	-20.8 dB
50Hz	20mV	11.9mV	-4.5 dB
100Hz	20mV	28mV	1.5 dB
500Hz	20mV	79mV	12 dB
1KHz	20mV	99mV	13.9 dB
10KHz	20mV	107mV	14.64dB
100KHz	20mV	1.06	14.5dB
1MHz	20mV	99mV	13.9 dB
~~5MHz~~			
10MHz	20mV	18mV	-0.8dB
20MHz	20mV	4mV	-13.8dB

We can find f_L and f_H because the Highest frequency is at 14.64 dB and f_H is at 11.64 and it is between 1MHz and 10MHz

The graph does not show the -3dB cutoff frequency at higher frequencies because the parasitic capacitance in the circuit is typically very low.

This low capacitance value results in a high cutoff frequency that exceeds the maximum frequency range supported by the Digital storage oscilloscope (DSO) in use.

F=1/2*pi*RC

As a result, the high-frequency cutoff region of the graph, where the voltage gain begins to decrease, is not visible in DSO. The equipment's limitations prevent us from observing the circuit's entire frequency response, especially at higher frequencies due to the high cutoff frequency caused by the low parasitic capacitance.

With using 440p Farad Capacitor:-

fin	Vin	Vo	Av
10HZ	20mV	0.0018 (2mV)	-20.8 dB
50HZ	20mV	11.9mV	-4.5 dB
100HZ	20mV	28mV	1.5 dB
500HZ	20mV	79mV	12 dB
1KHZ	20mV	99mV	13.9 dB
10KHZ	20mV	107mV	14.64dB
100KHZ	20mV	1.06	14.5dB
1MHZ	20mV	99mV	13.9 dB
~~5MHZ~~			
10MHZ	20mV	18mV	-0.8dB
20MHZ	20mV	4mV	-13.8 dB

We can find f_L and f_H because the ~~Highest frequency~~ Highest frequency is at 14.64 dB and f_H is at 11.64 and it is between 1MHZ and 10MHZ

In this case, we are able to observe the cutoff frequency because of the presence of the capacitor at the load (CL). This capacitor, due to its configuration, acts as a low-pass filter, allowing only lower frequencies to pass through while attenuating higher frequencies.

The capacitor limits the circuit's bandwidth by reducing the amplitude of higher frequencies.

The frequency response graph shows how high-frequency components are cut off. The capacitor at the load affects the cutoff frequency and overall frequency response of the circuit.