LAB 8 REPORT: OPERATIONAL AMPLIFIERS

Course: Analog Electronic Circuits Lab (EC2.103, Spring 2025)
Instructor: Prof. Zia Abbas
Team Members:

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2. S V Santhosh Yadav (2024102054)

Components Used

- CD4007BE , UA747 IC's
- Capacitors, Resistors
- DC power supply
- Digital Storage Oscilloscope (DSO) and Function Generator

Experiment 1: CMOS Inverter with Feedback

Objective

To analyse the voltage transfer characteristics (VTC) of a CMOS inverter with feedback and determine its valid input-output region for amplification.

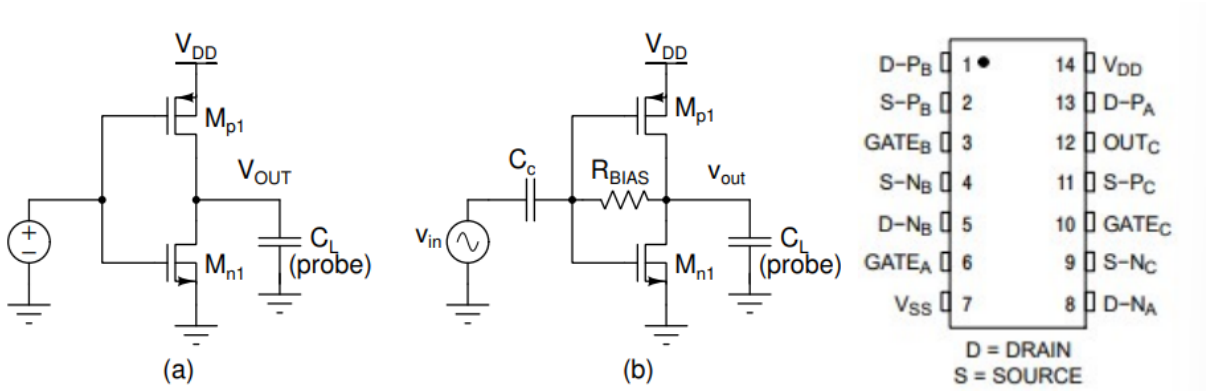
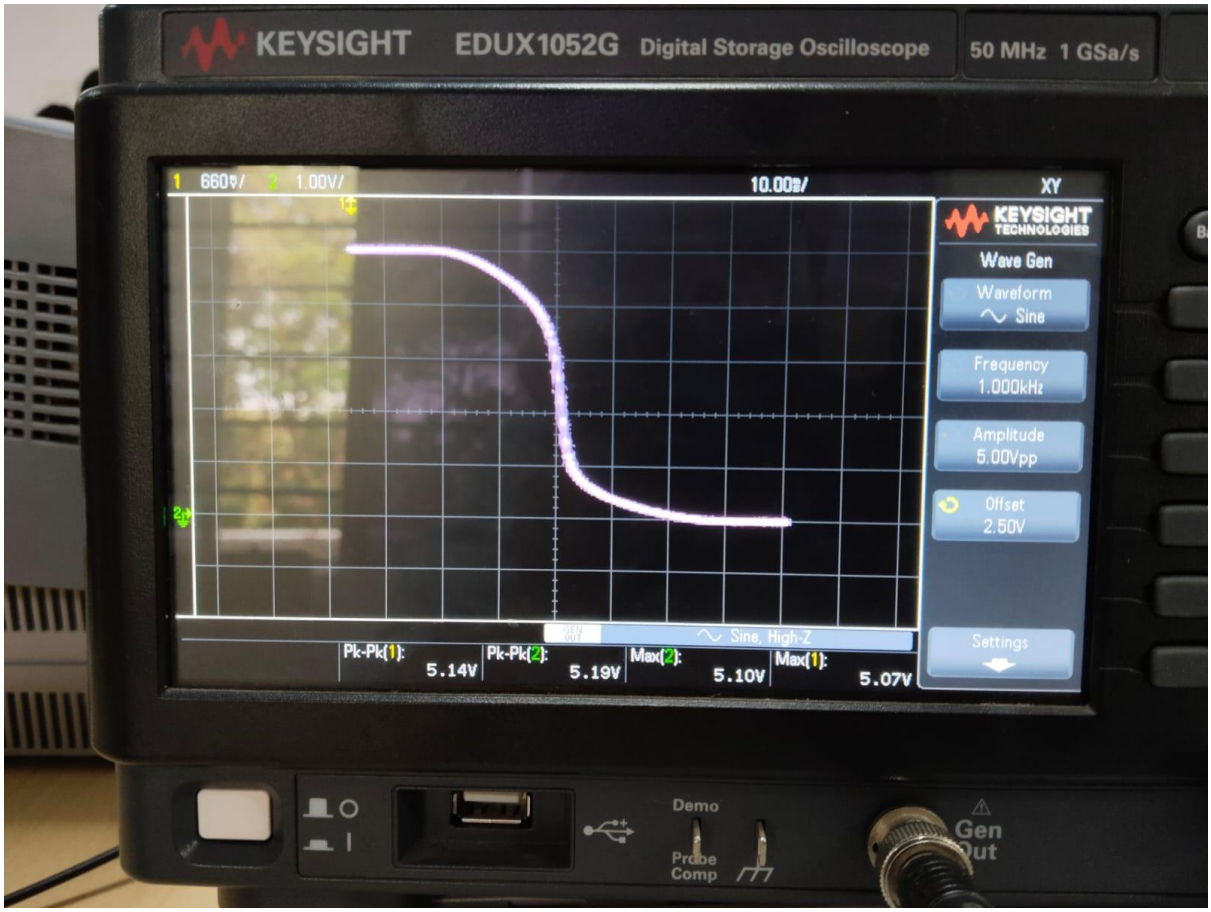


Figure 23: (a) VTC (b) voltage amplifier

Procedure

- Connected the gates of both MOSFETs to the waveform generator.
- Connected the drains of both MOSFETs to the DSO probe.
- Connected the PMOS source to +5 V and the NMOS source to ground.

- Applied a sinusoidal input signal (5 V amplitude) and plotted VOUT vs VIN using the DSO.
- Identified the valid input region for amplification (where slope |dVOUT/dVIN| > 1)
- Added a coupling capacitor (10 µF) and bias resistor (1 MΩ) between the gates and drains.
- Measured DC values at the drain (2.4 V) and gate (2.5 V).
- Applied a sinusoidal input (100 mVpp, 1 kHz) and observed the output waveform.
- Varied input amplitude (200 mVpp to 600 mVpp) and recorded output voltage and gain.
- Observed clipping at higher input amplitudes due to output swing limitations.



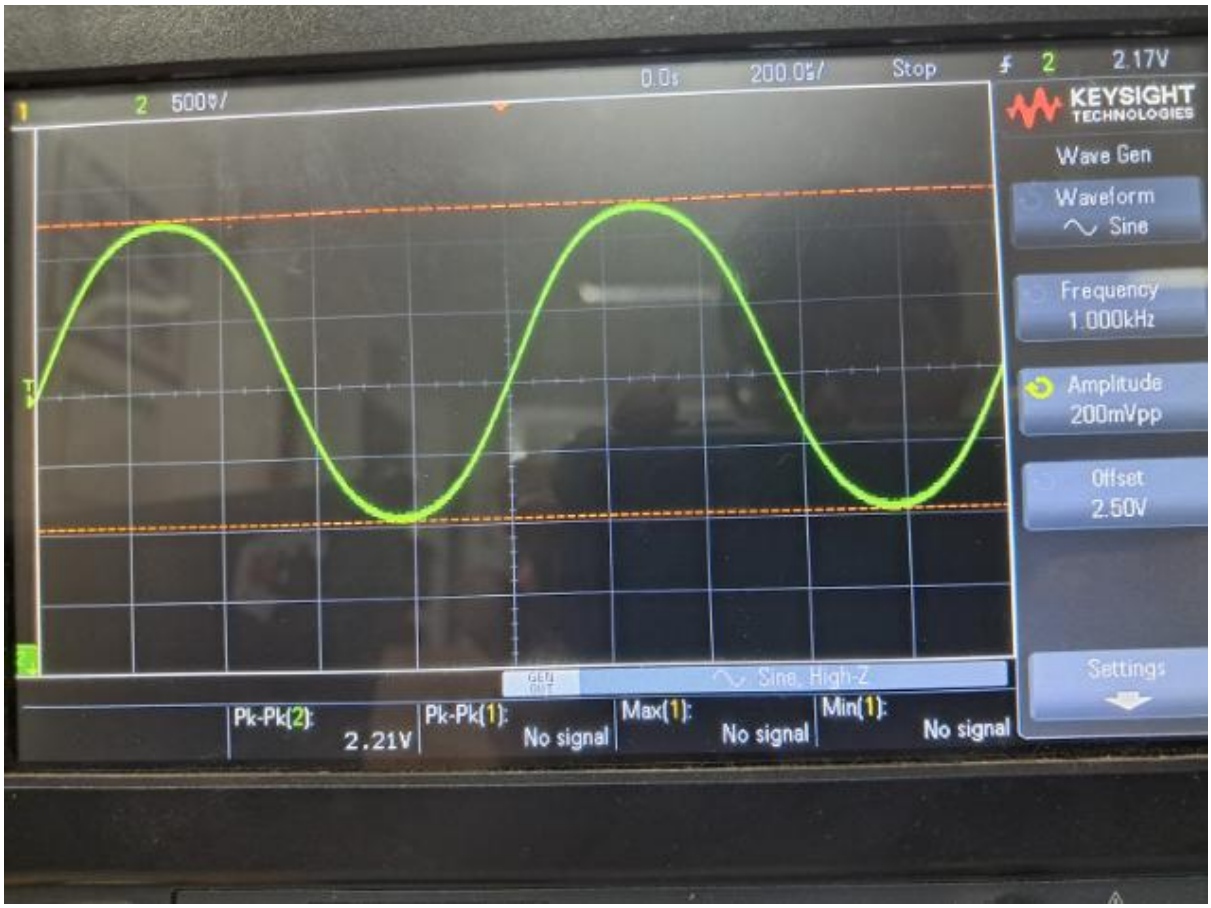
Plot of input and output voltages of the circuit

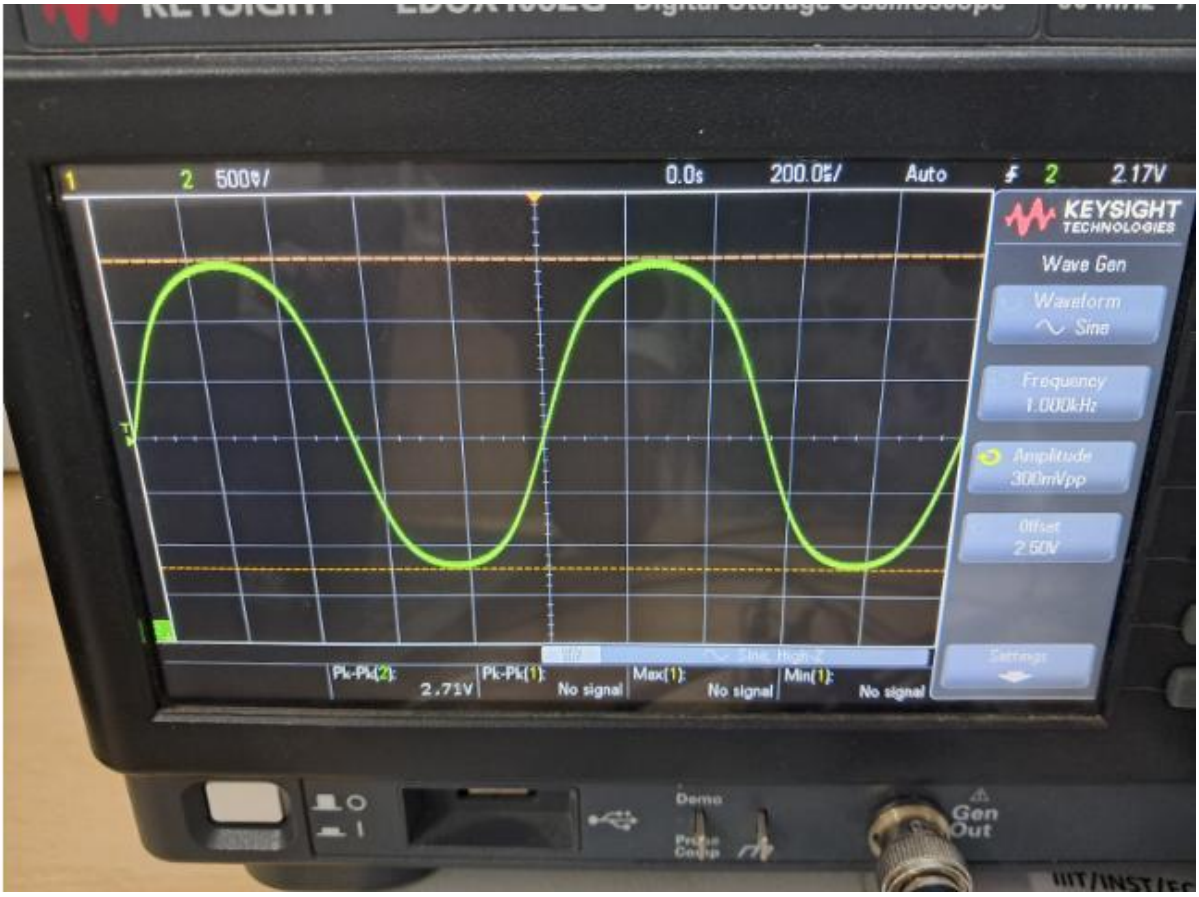
Results

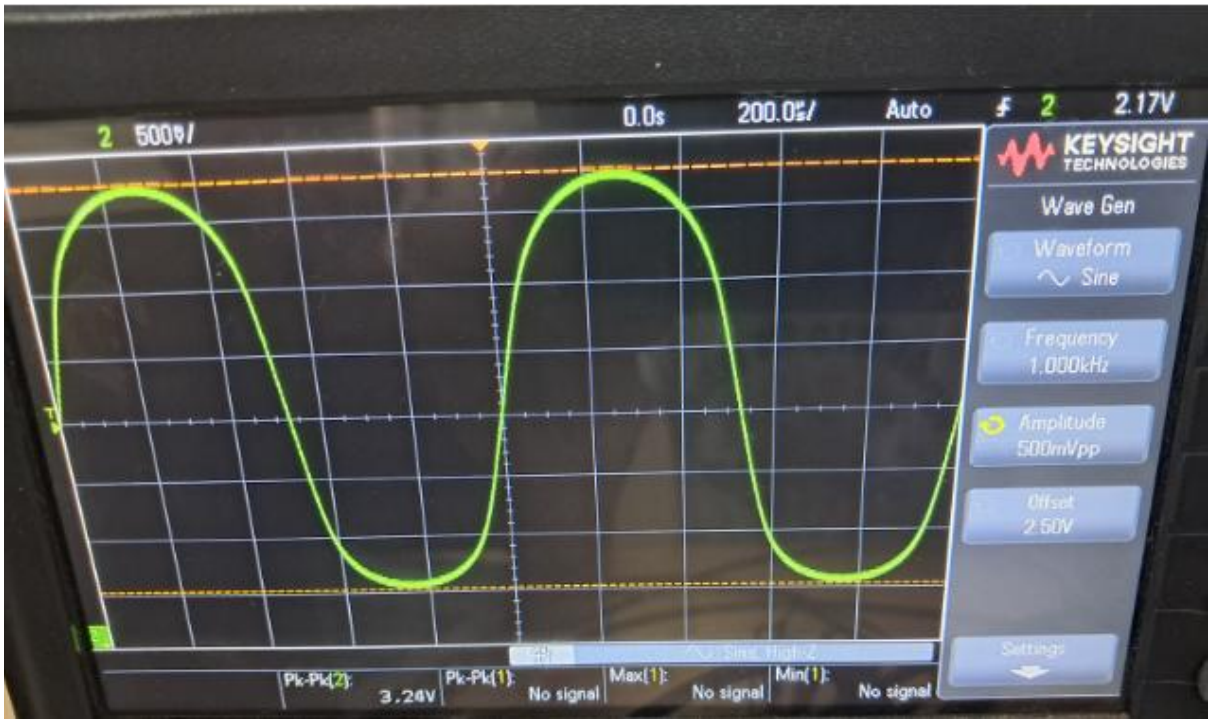
Vin (mVpp)	Vout (mVpp)	Gain (Vout/Vin)
400	1310	3.3
500	2210	4.45
600	2710	4.51
700	3000	4.28
800	3200	4.0
900	3400	3.7

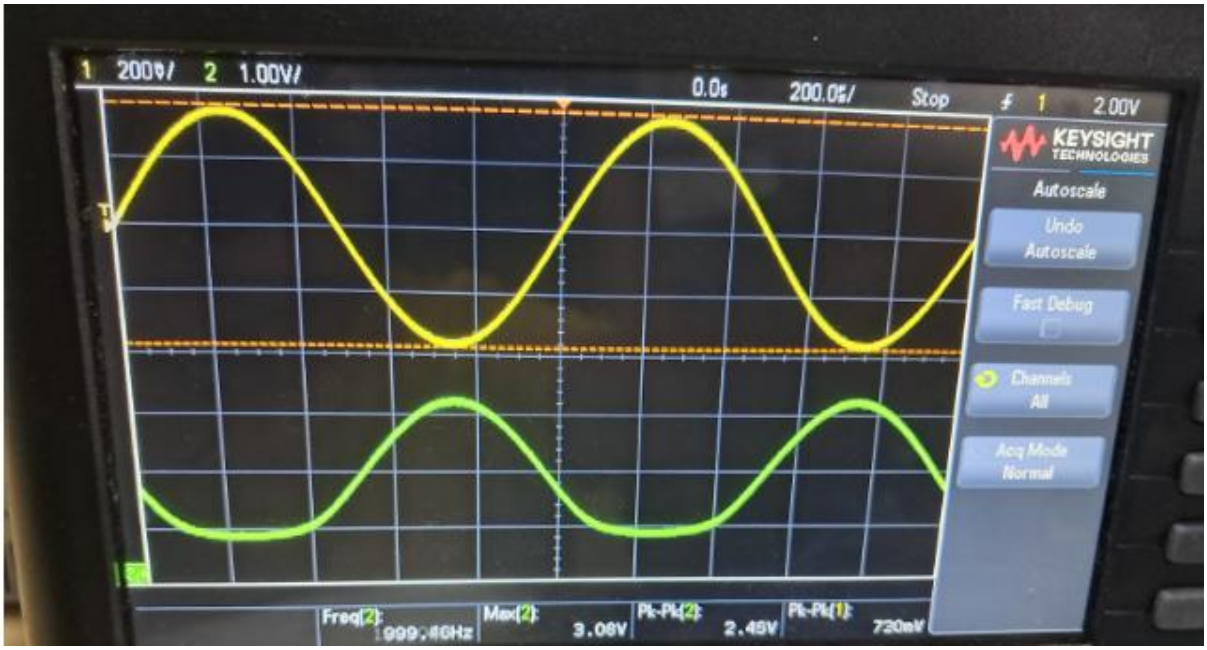
Observations

- The valid input region for amplification was around **VDD/2 = 2.5 V**, where both MOSFETs operate in saturation.
- As input amplitude increased beyond 600 mVpp, the output clipped due to saturation at VDD (5 V).
- Gain decreased at higher inputs due to clipping.




2 500mV/
0.0s
200.0ns/
Auto
2 2.17V
KEYSIGHT TECHNOLOGIES
Wave Gen
Waveform
Sine
Frequency
1.000kHz
Amplitude
300mVpp
Offset
2.50V
Settings
Pk-Pk(2):
2.71V
Pk-Pk(1):
No signal
Max(1):
No signal
Min(1):
No signal
Demo
Gen Out


2 500mV/
0.0s
200.0ns/
Auto
2 2.17V
KEYSIGHT TECHNOLOGIES
Wave Gen
Waveform
Sine
Frequency
1.000kHz
Amplitude
500mVpp
Offset
2.50V
Settings
Pk-Pk(2):
3.24V
Pk-Pk(1):
No signal
Max(1):
No signal
Min(1):
No signal



Conclusion

The CMOS inverter with feedback acts as an amplifier within a specific input range. Clipping occurs when the output approaches supply limits, reducing gain.

Experiment 2: Characterization of an Operational Amplifier

Objective

To study the open-loop characteristics of an op-amp and measure its DC offset voltage.

Procedure

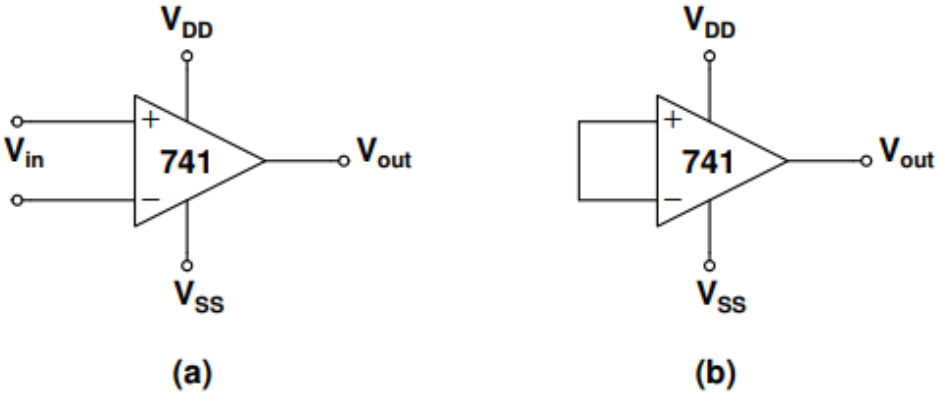
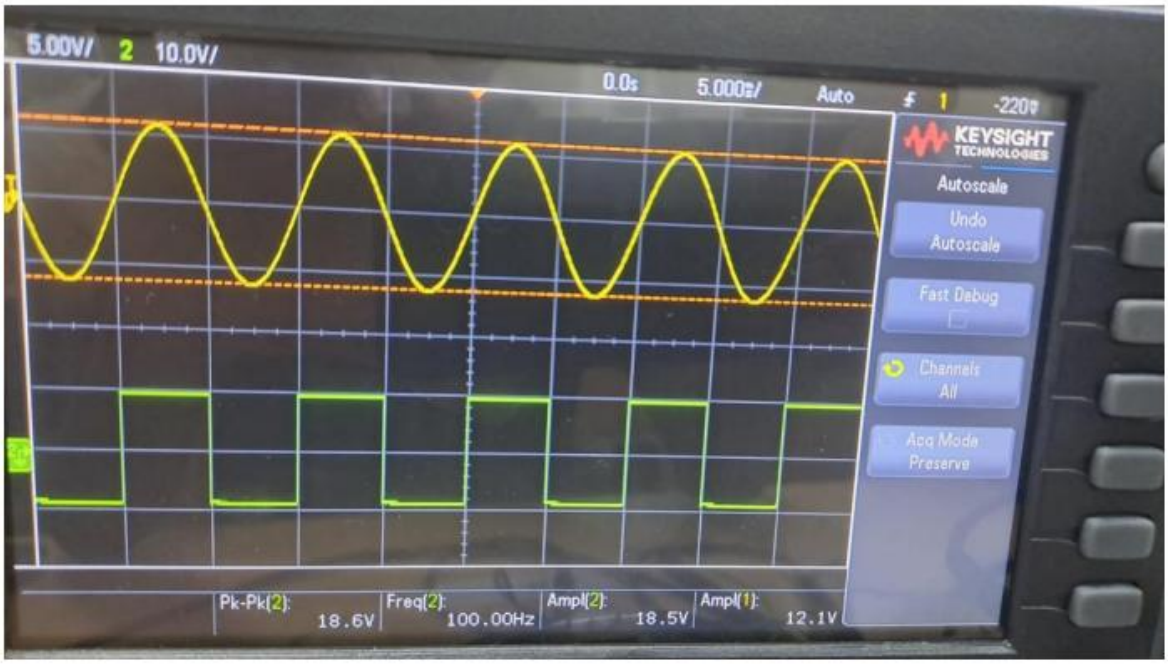
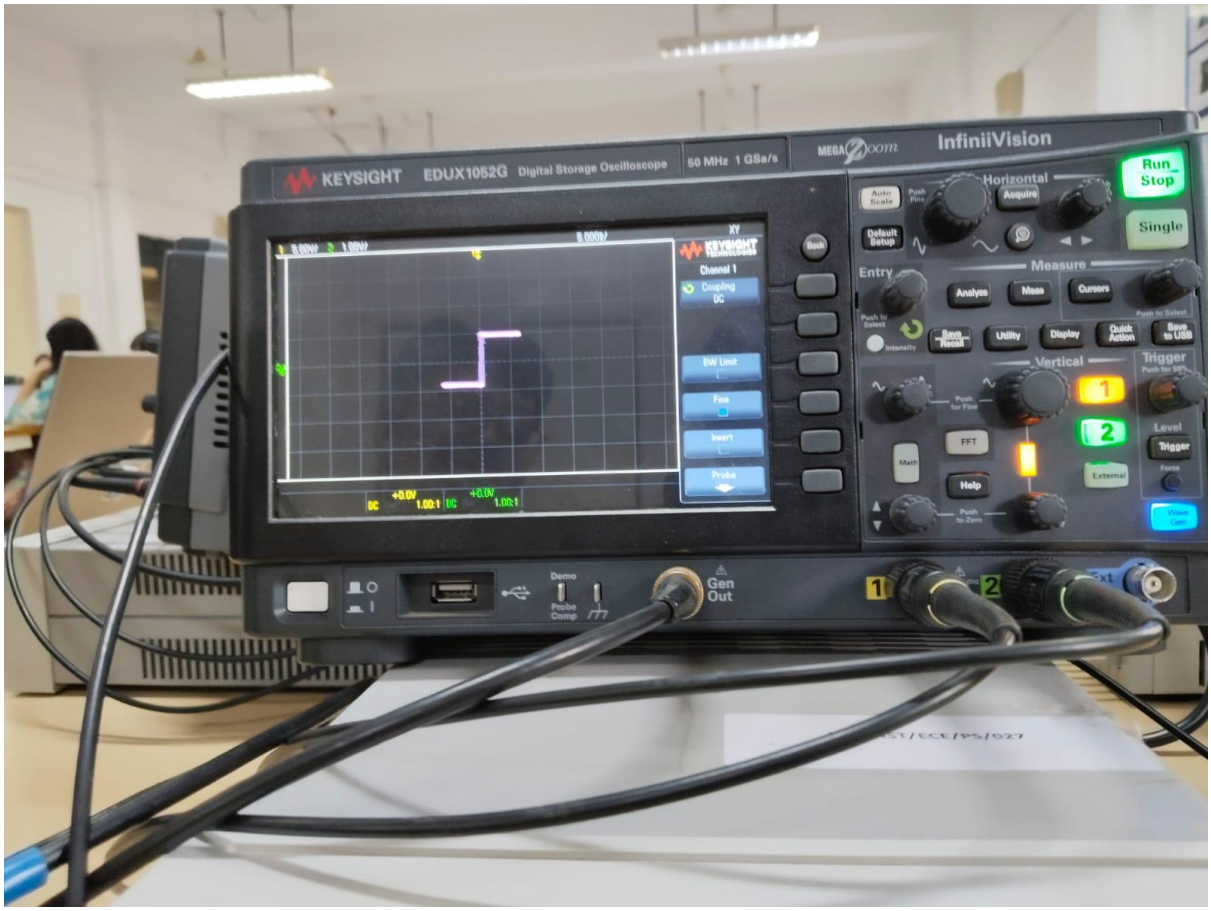
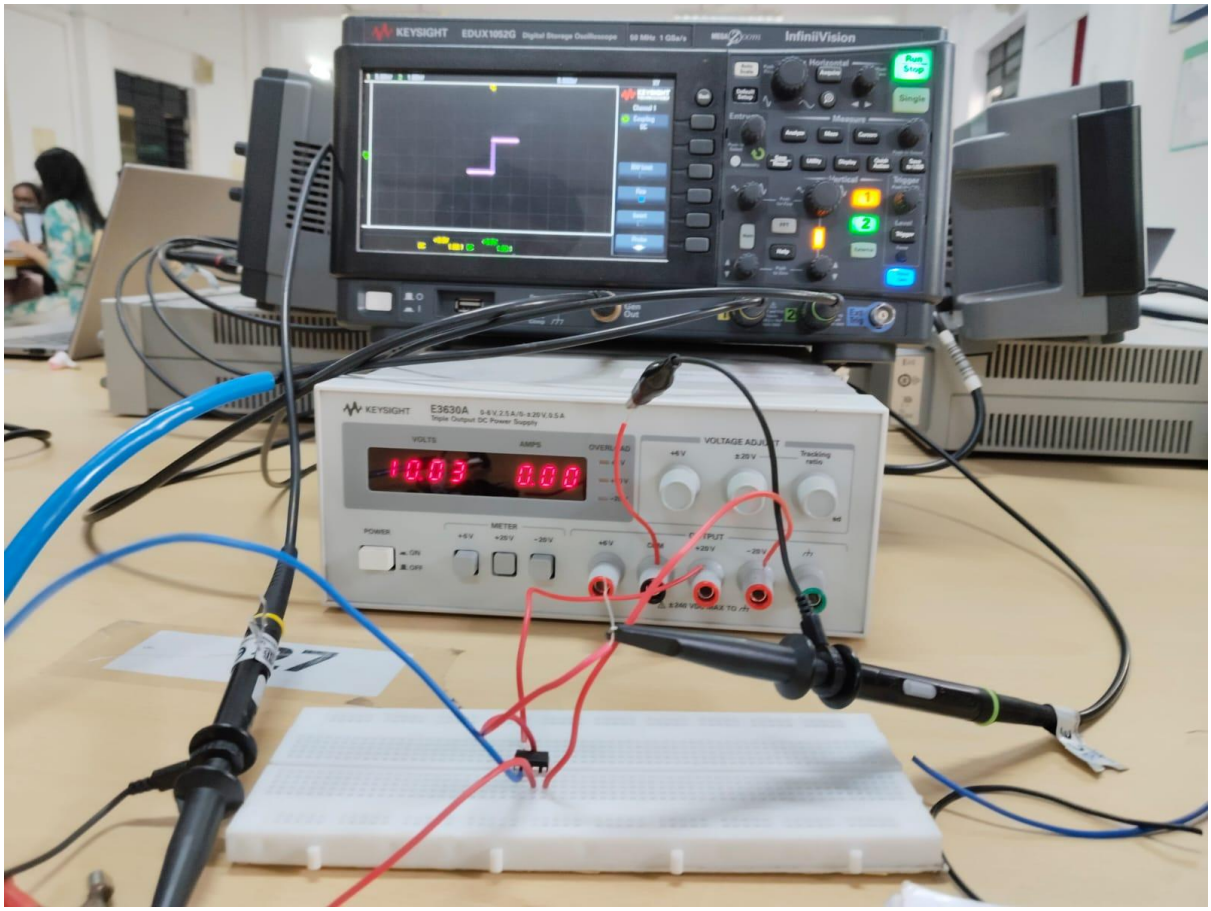


Figure 24: Opamp open loop characteristics (b) offset measurement

1. **Open-Loop Configuration:**
    - Connected the op-amp to ±10 V supplies Vdd and Vss to +10 and -10 respectively .
    - It amplifies the difference between the Non-inverting and inverting side signals
    - Output as A((V+)-(V-))
    - Input as (V+)-Non-inverting input, (V-)-inverting input
    - Practically this gain is not possible, practically the input resistances are very high and the output resistance are really small(few ohms), the gain is also of the order 10^6
    - Applied a sinusoidal input (12 Vpp, 100 Hz) to the non-inverting terminal and grounded the inverting terminal.
    - We observe that the output gets clipped and produces a square wave kind of output signal, this is due to the high gain of the OpAmp, as the input is 12Vpp the output should be 12(10^6)Vpp, but the supply to the OpAmp itself is between 10V and -10V, due to which we see clipping of the output
    - Observed output clipping (square wave) due to high open-loop gain.
    - **Output Saturation:** around ±9.3 V (due to supply limits).
    - for small inputs voltages there is proper amplification, but any more increase leads to cut off in the output signal, this we can infer from the graph


5.00V/ 2 10.0V/
0.0s 5.000s/ Auto 1 -220
KEYSIGHT TECHNOLOGIES
Autoscale
Undo Autoscale
Fast Debug
Channels All
Acq Mode Preserve
Pk-Pk(2): 18.6V
Freq(2): 100.00Hz
Ampl(2): 18.5V
Ampl(1): 12.1V


KEYSIGHT EDUX1052G Digital Storage Oscilloscope
50 MHz 1 GSa/s
MEGAZoom InfiniiVision
Run Stop
Single
Horizontal
Measure
Vertical
Trigger
Gen Out



2. **DC Offset Measurement:**
    - Connected both input terminals together (no differential input).
    - Ideally when the difference is zero the output should also should zero
    - Bu practically there can be a DC offset that we can see at the output now
    - Measured a DC offset of approx **1 V(950mV)** at the output.

- 

- Adjusted the non-inverting input to approx (-0.48)-0.5 V to nullify the offset.

DC Offset: 1 V (reduced by input adjustment).

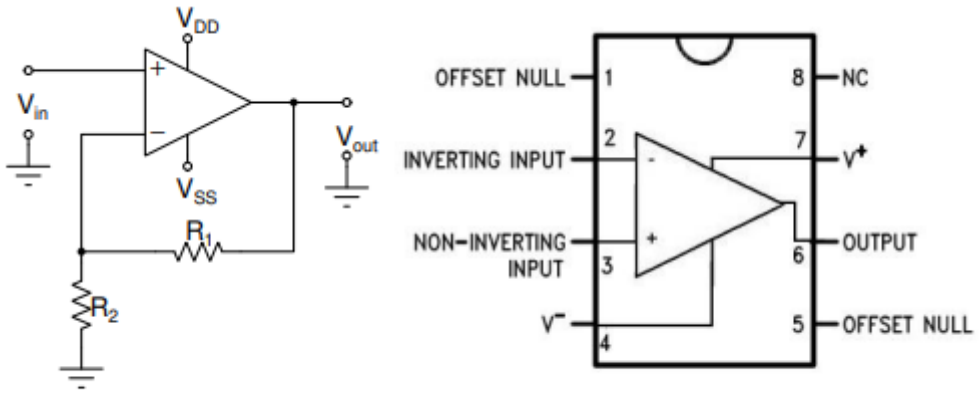
Conclusion

The op-amp exhibits high gain, causing output saturation. DC offset is present due to imperfections and also Opamp is not deal to get null.

Experiment 3: Non-Inverting Amplifier

Objective

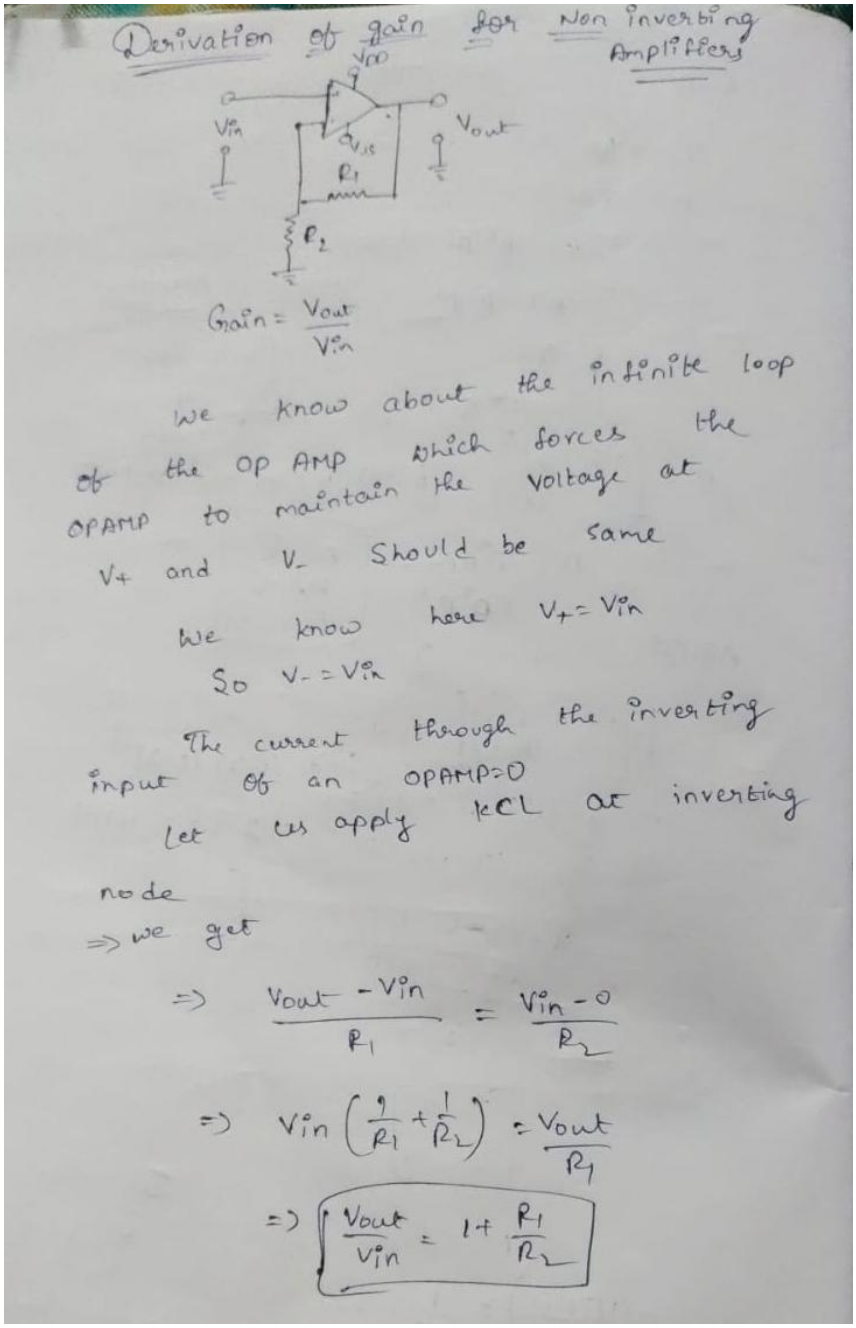
To design a non-inverting amplifier and verify its gain.



((a)) ((b))

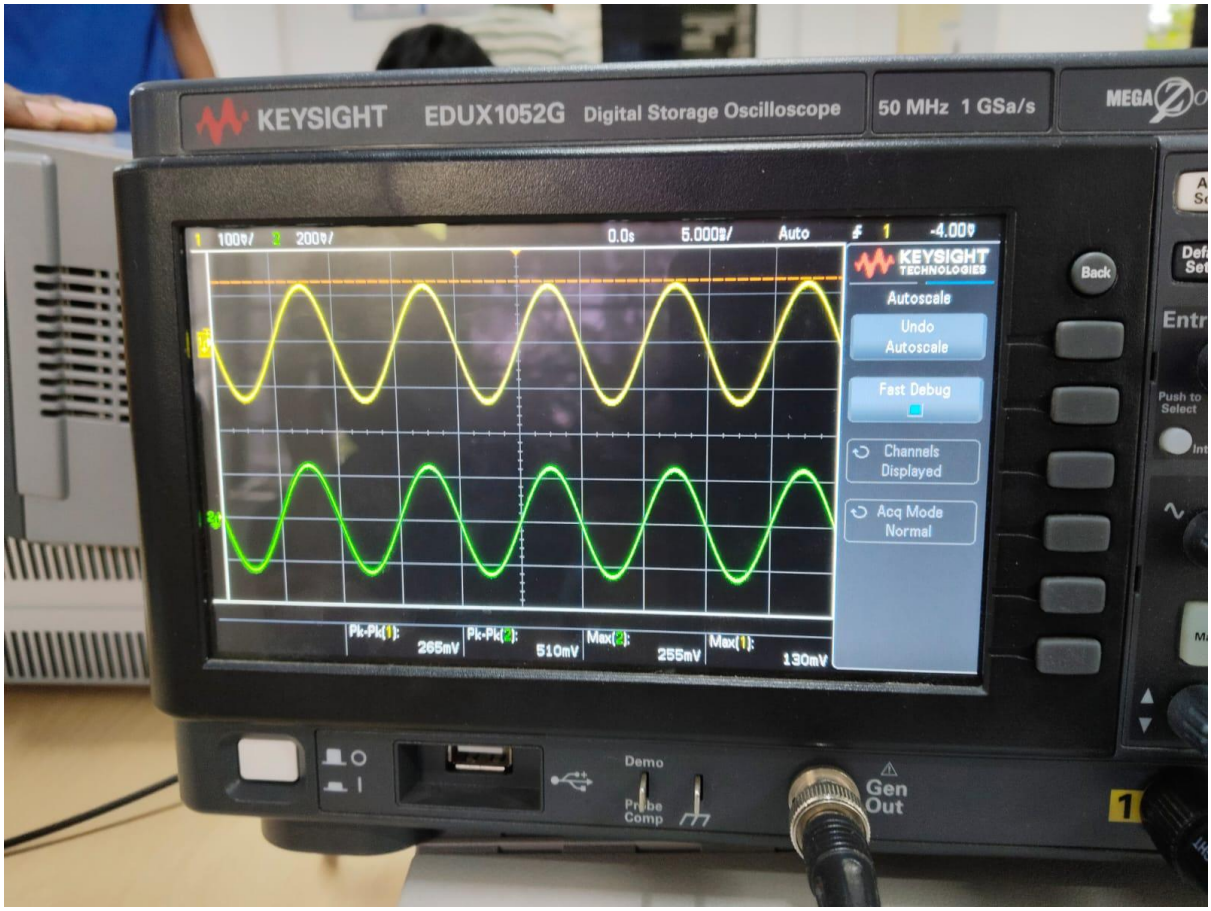
Procedure

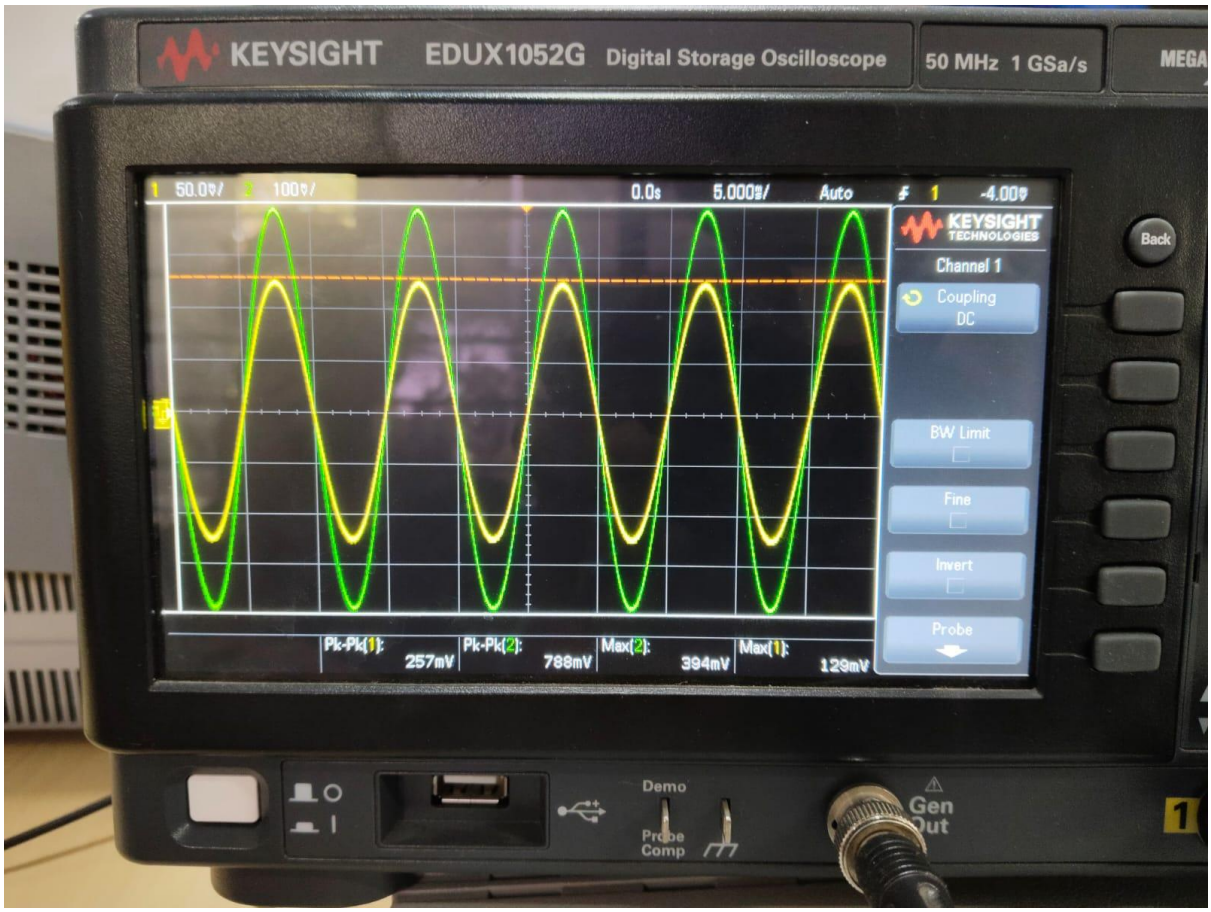
- Connected input (250 mVpp, 5 kHz) to the non-inverting terminal.
- Used negative feedback with resistors R1 and R2.



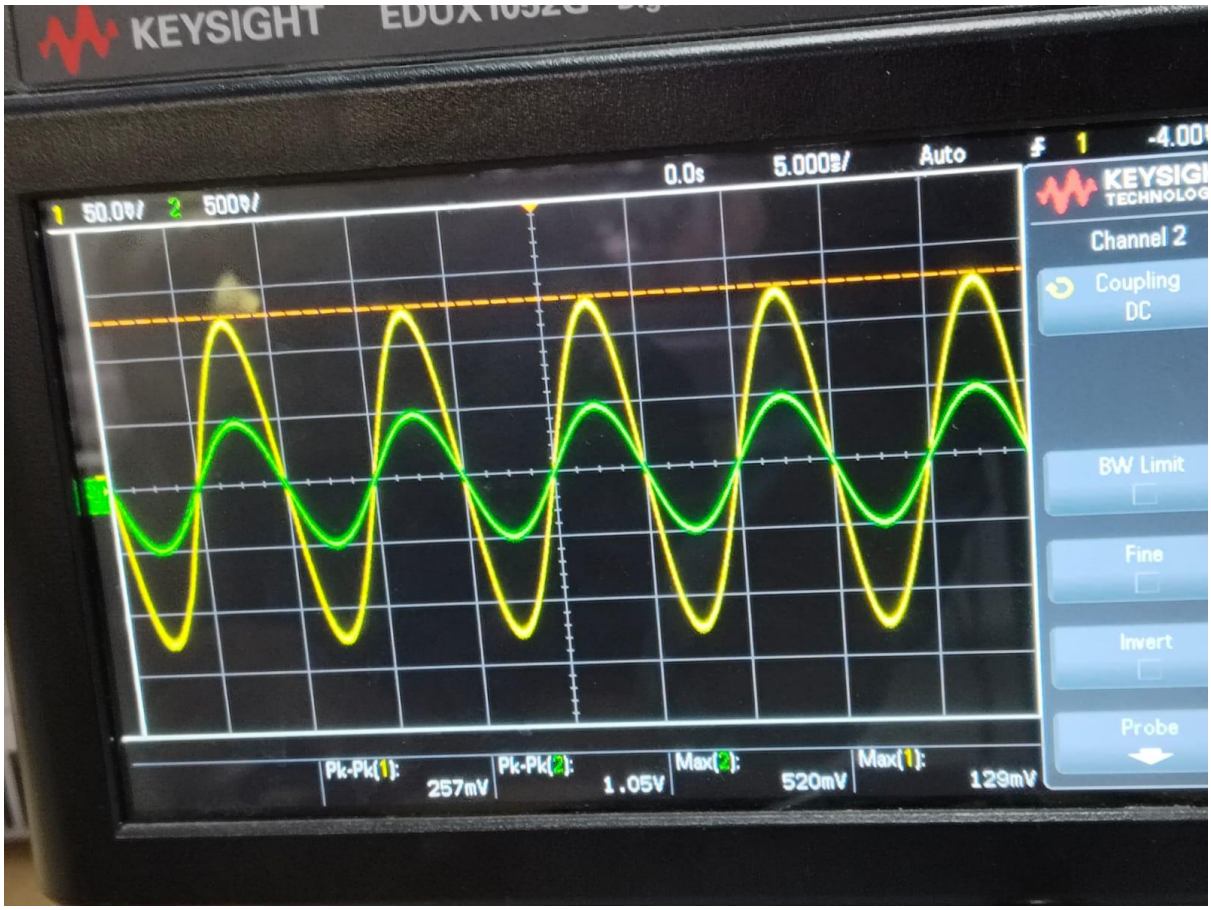
- Theoretical gain: **1 + (R1/R2)**.
- (C) Measured gain for different resistor combinations.
- For obtaining gain as 4,5
- 1+R2/R1=4 → R2=3*R1 (gain 4)
- 1+R2/R1=5 → R2=4*R1 (gain 5)

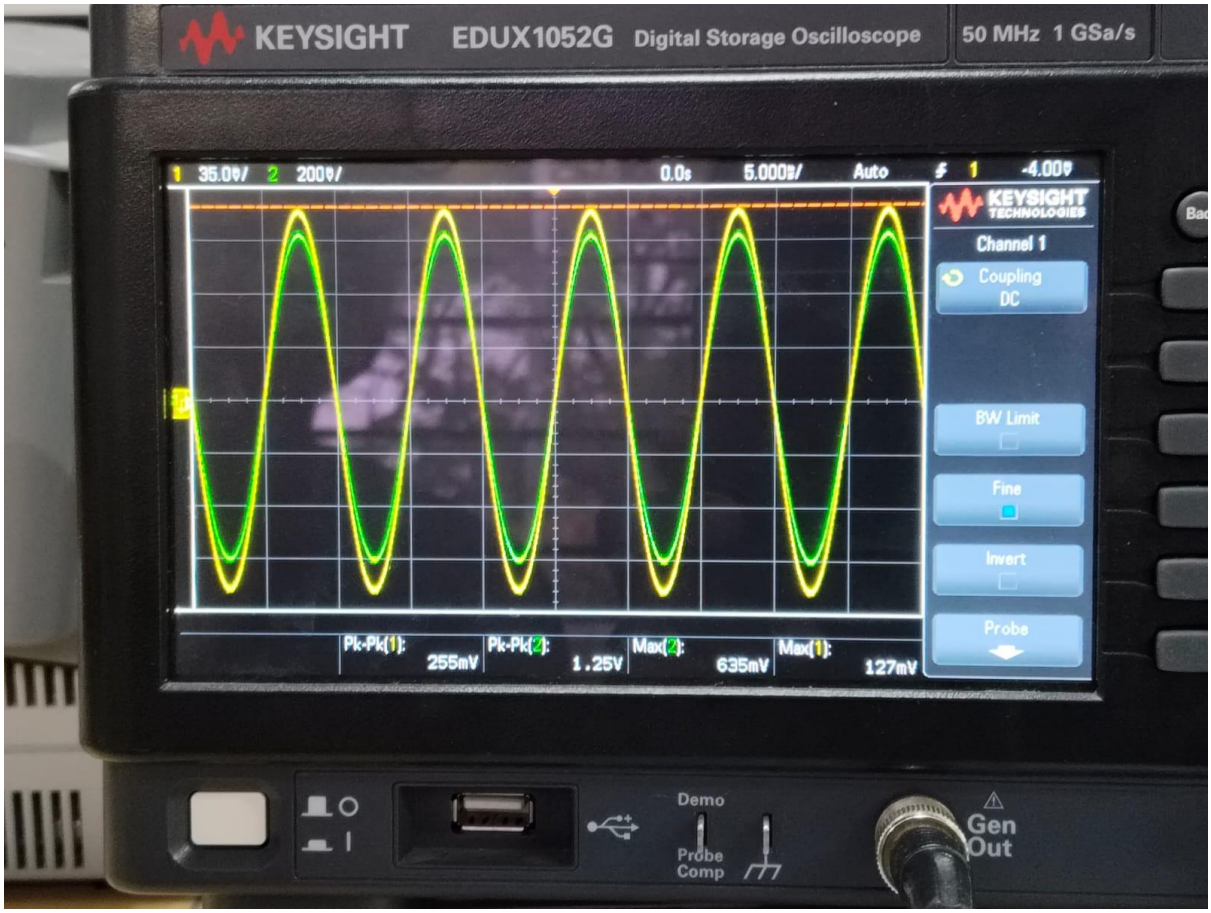
Results


KEYSIGHT EDUX1052G Digital Storage Oscilloscope
50 MHz 1 GSa/s
Autoscale
Undo Autoscale
Fast Debug
Channels Displayed
Acq Mode Normal
Back
Pk-Pk(1): 265mV
Pk-Pk(2): 510mV
Max(2): 255mV
Max(1): 130mV
Demo
Probe Comp
Gen Out


KEYSIGHT EDUX1052G Digital Storage Oscilloscope
50 MHz 1 GSa/s
Channel 1
Coupling DC
BW Limit
Fine
Invert
Probe
Back
Pk-Pk(1): 257mV
Pk-Pk(2): 788mV
Max(2): 394mV
Max(1): 129mV
Demo
Probe Comp
Gen Out

R1 (kΩ)	R2 (kΩ)	Vout (mVpp)	Calculated Gain	Observed Gain
10	10	510	2	1.924
10	4.7	750	3.127	2.72





Expected Gain	R1 (kΩ)	R2 (kΩ)	Vout (mVpp)	Observed Gain
4	60	180	1050	4.08
5	60	240	1250	5

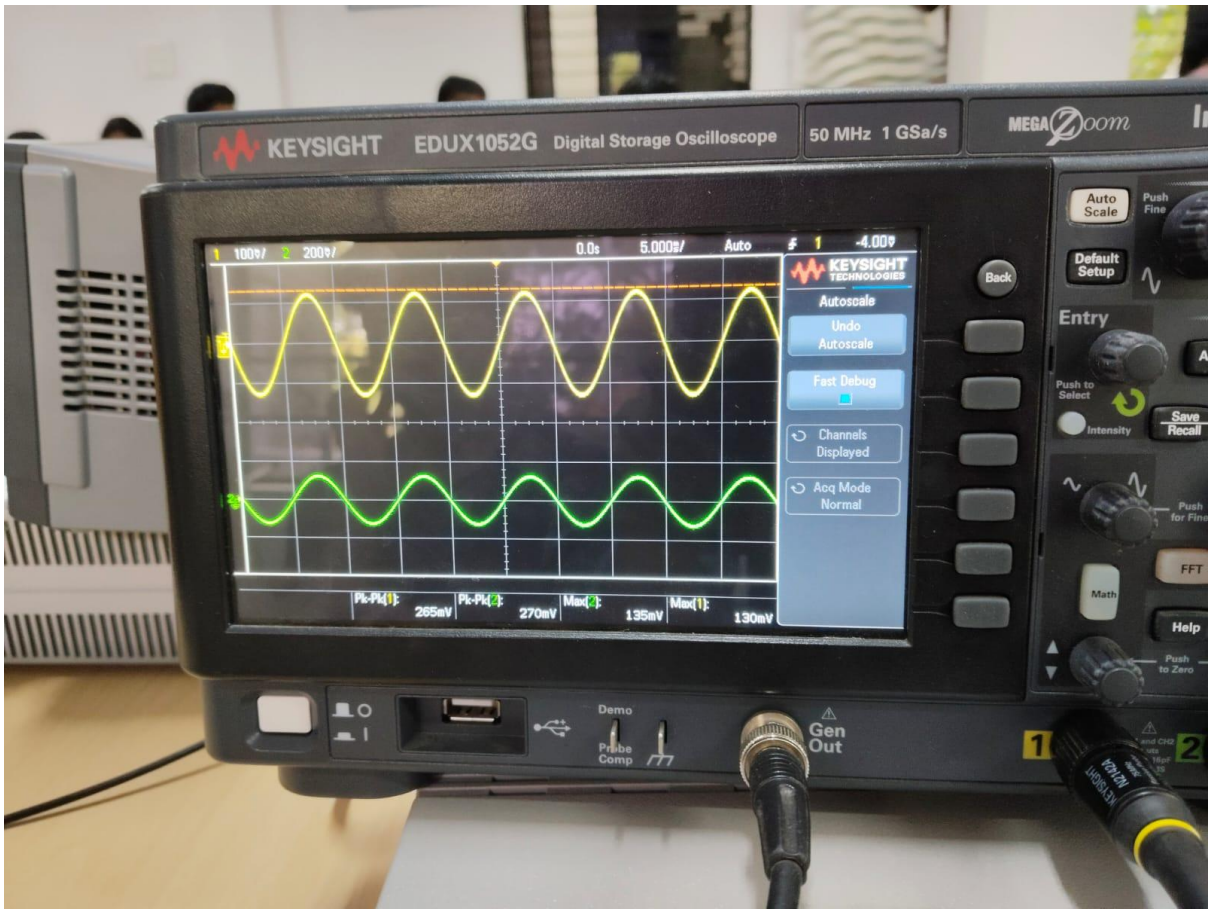
(d) if we remove both the resistors R1,R2 and then connected then gain is 1 by formula

So vout = vin

This circuit is known as a BUFFER circuit.

The buffer circuit exhibits a high input impedance, meaning it draws minimal current, resulting in minimal disturbance to the connected circuitry at its input terminals. It can function as an impedance matcher, matching the impedance between different parts of a circuit to ensure efficient signal transfer. It can also act as a signal isolator, providing electrical isolation between different sections of a circuit to prevent interference. Additionally, the buffer circuit can serve as a voltage level shifter, adjusting the voltage level of the input signal to match the requirements of the downstream circuitry. Finally, it can function as an active filter

stage within a larger filter circuit, actively manipulating the signal to achieve desired filtering characteristics



Conclusion

The non-inverting amplifier gain matches theoretical values. Direct feedback (R1 = 0) results in unity gain, useful for buffer applications.

Uses:

Voltage Follower (Input = Output)

→ Used to buffer a signal without changing its voltage, ideal for impedance matching.

Sensor Amplifier

→ Amplifies weak signals from sensors like thermistors without inverting them.

Audio Pre-Amplifier

→ Boosts microphone signals to a usable level while preserving signal polarity.

Experiment 4: Inverting Amplifier

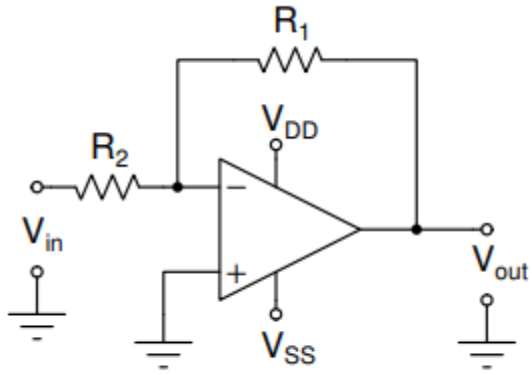


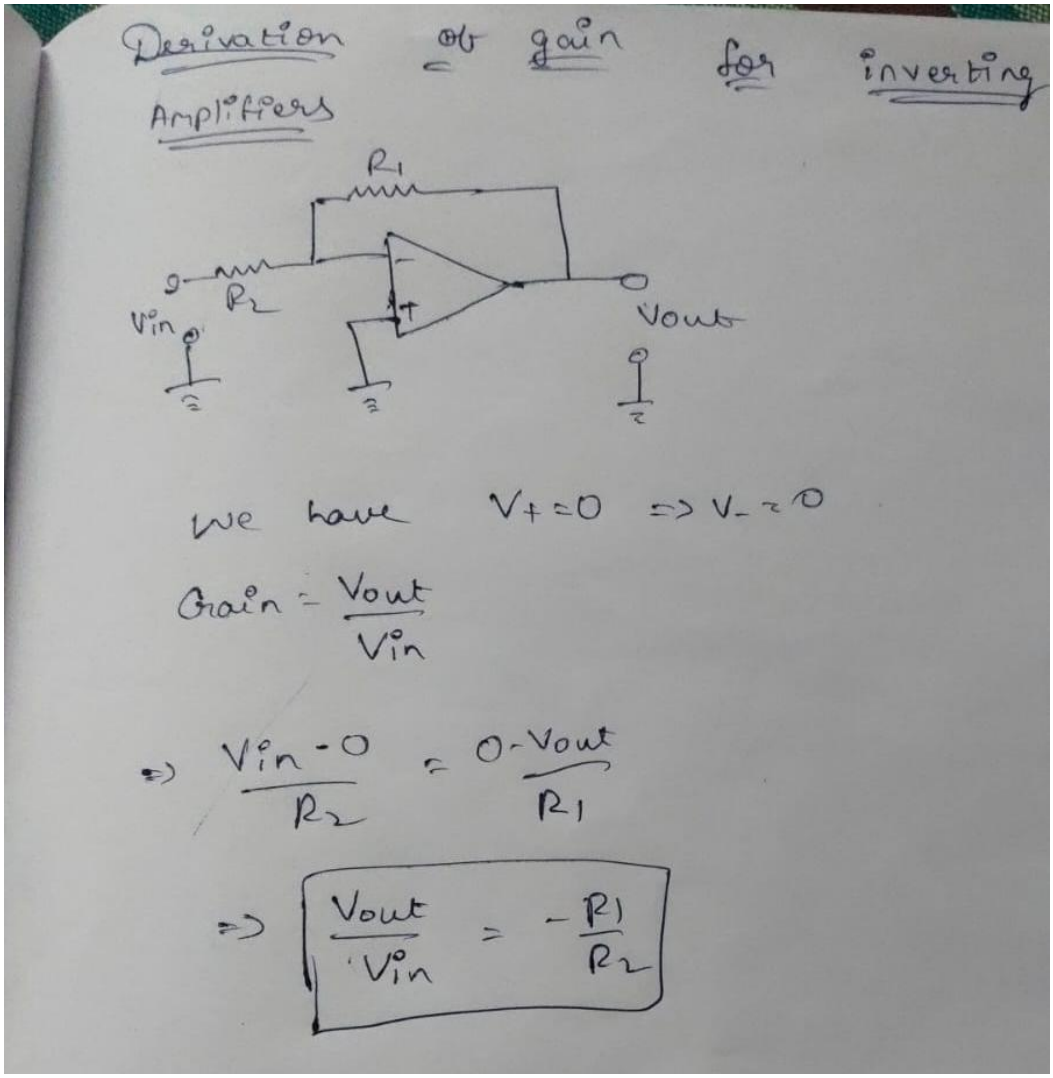
Figure 26: Inverting amplifier

Objective

To design an inverting amplifier and verify its gain.

Procedure

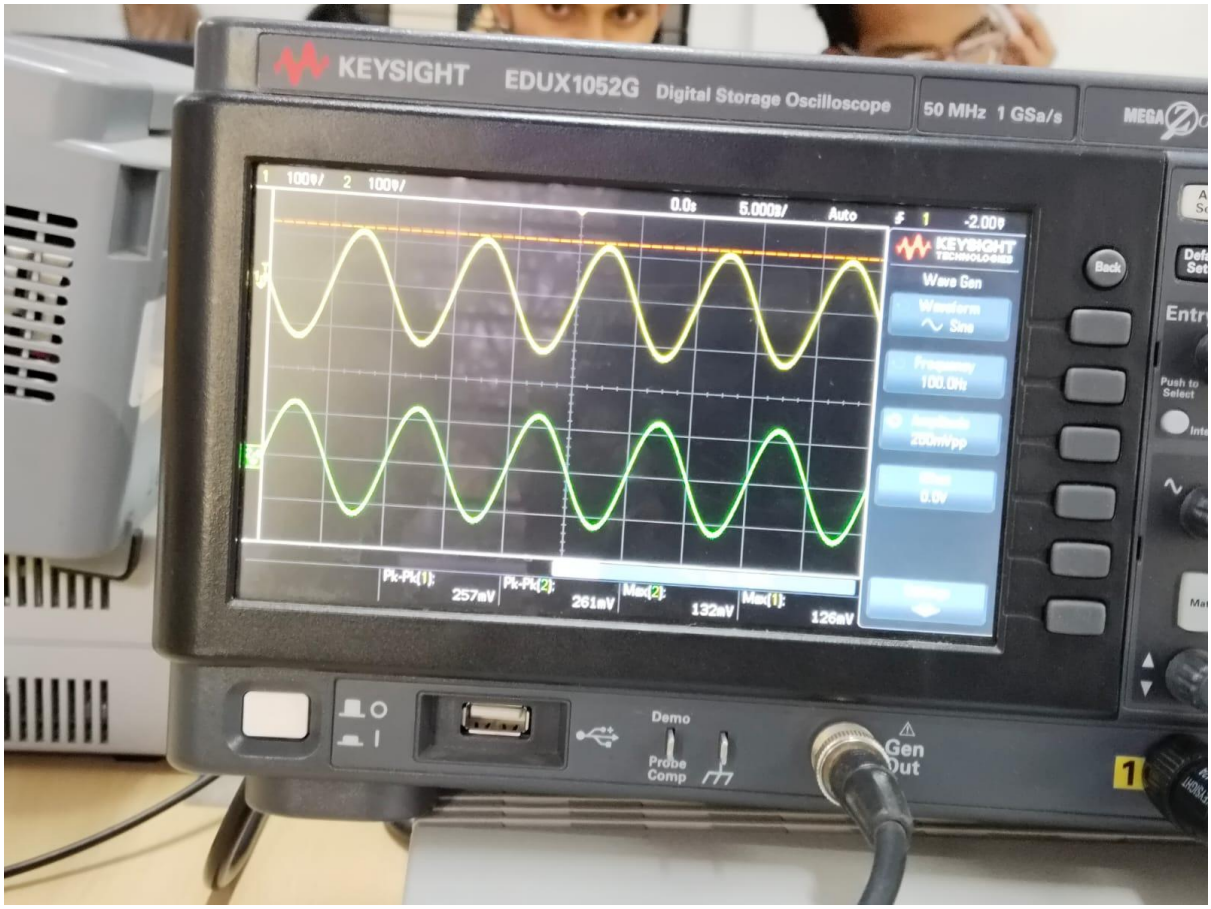
1. **Circuit Setup:**

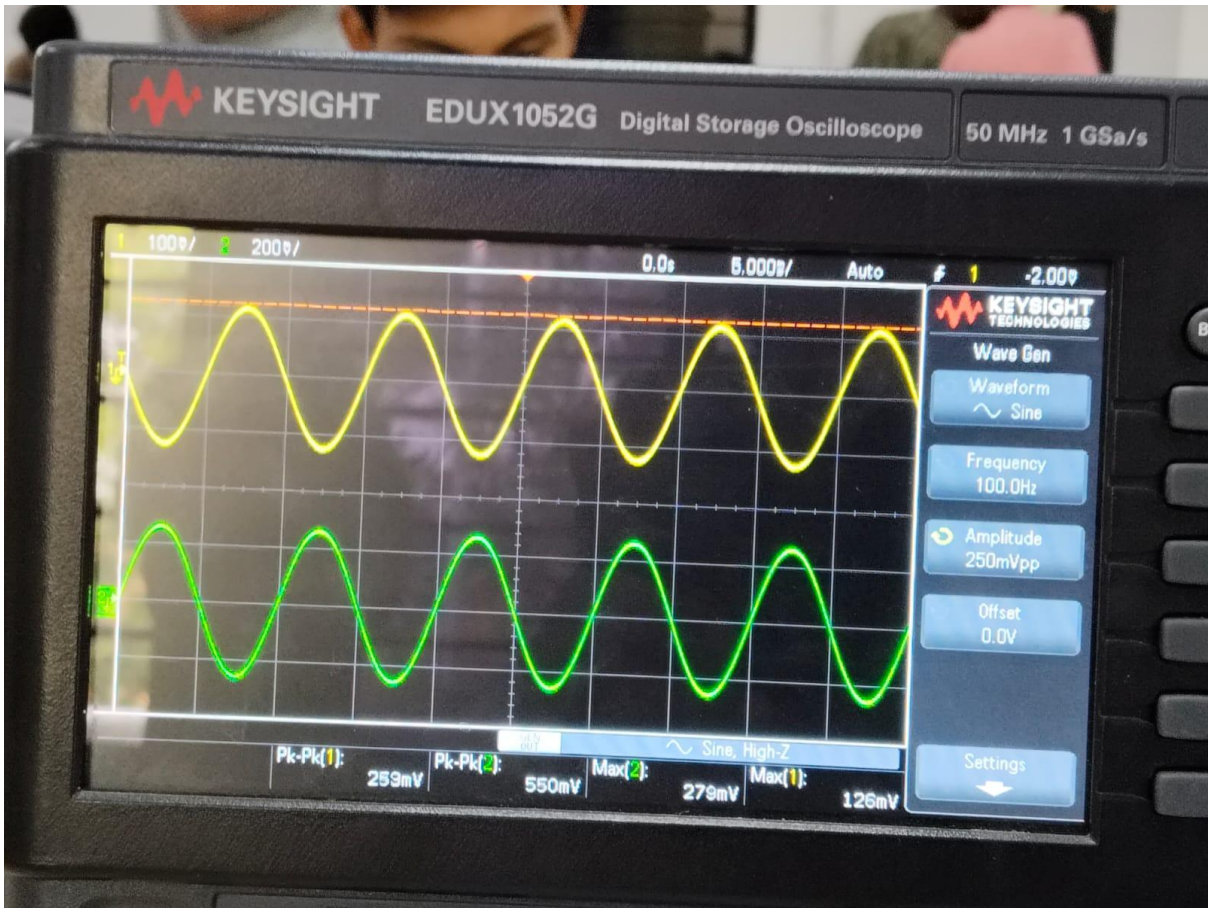


- Connected input (250 mVpp, 5 kHz) to the inverting terminal via R2.
- Used negative feedback with R1.

2. **Gain Calculation:**
   - Theoretical gain: **-(R1/R2)**.
   - Measured gain for different resistor combinations.

Results


KEYSIGHT
EDUX1052G
Digital Storage Oscilloscope
50 MHz 1 GSa/s
Wave Gen
Waveform
Sine
Frequency
100.0Hz
Amplitude
250mVpp
Offset
0.0V
Settings
Pk-Pk(1):
257mV
Pk-Pk(2):
261mV
Max(2):
132mV
Max(1):
126mV
Demo
Probe Comp
Gen Out


KEYSIGHT
EDUX1052G
Digital Storage Oscilloscope
50 MHz 1 GSa/s
KEYSIGHT TECHNOLOGIES
Wave Gen
Waveform
Sine
Frequency
100.0Hz
Amplitude
250mVpp
Offset
0.0V
Settings
Sine, High-Z
Pk-Pk(1):
259mV
Pk-Pk(2):
550mV
Max(2):
279mV
Max(1):
126mV

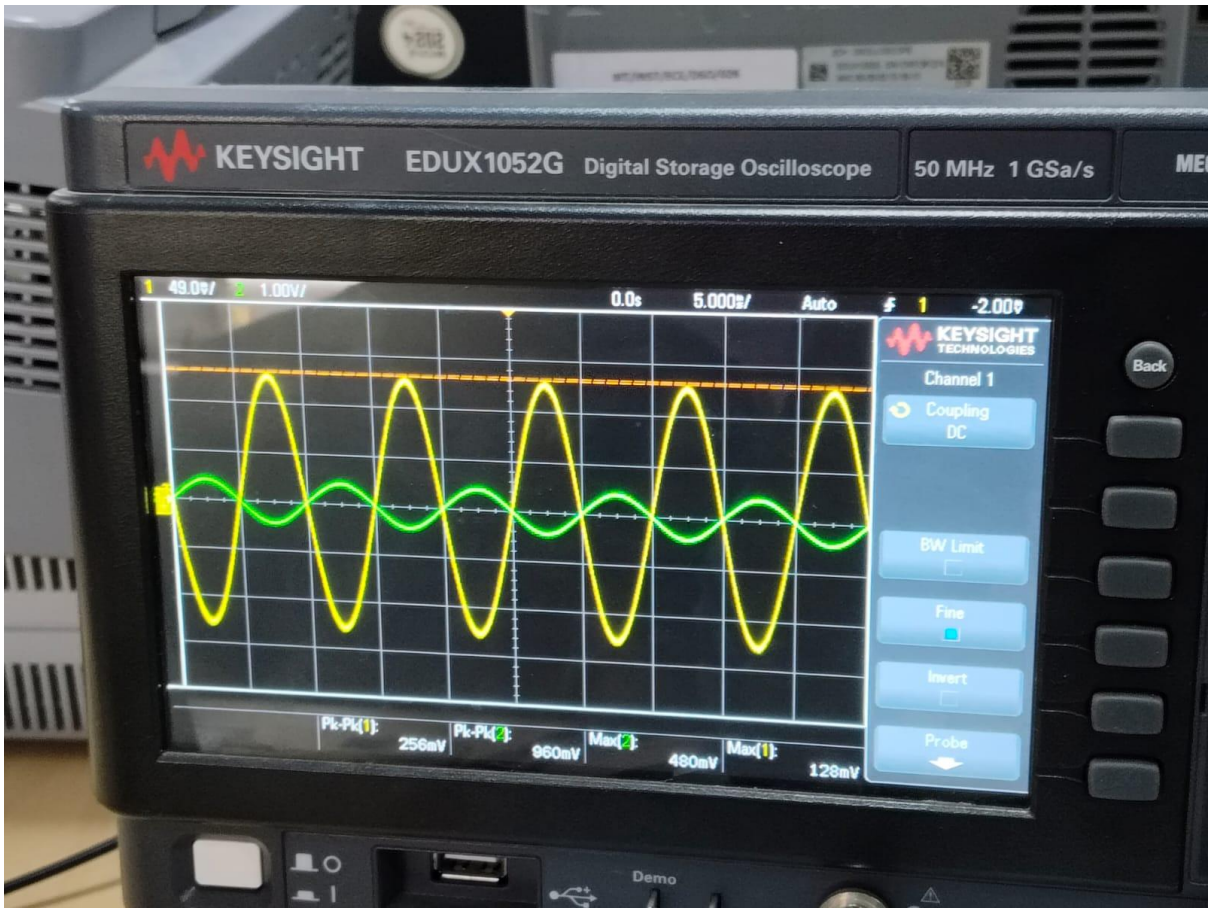
R1 (kΩ)	R2 (kΩ)	Vout (mVpp)	Calculated Gain	Observed Gain
10	10	261	-1	-1.01
10	4.7	550	-2.127	-2.17

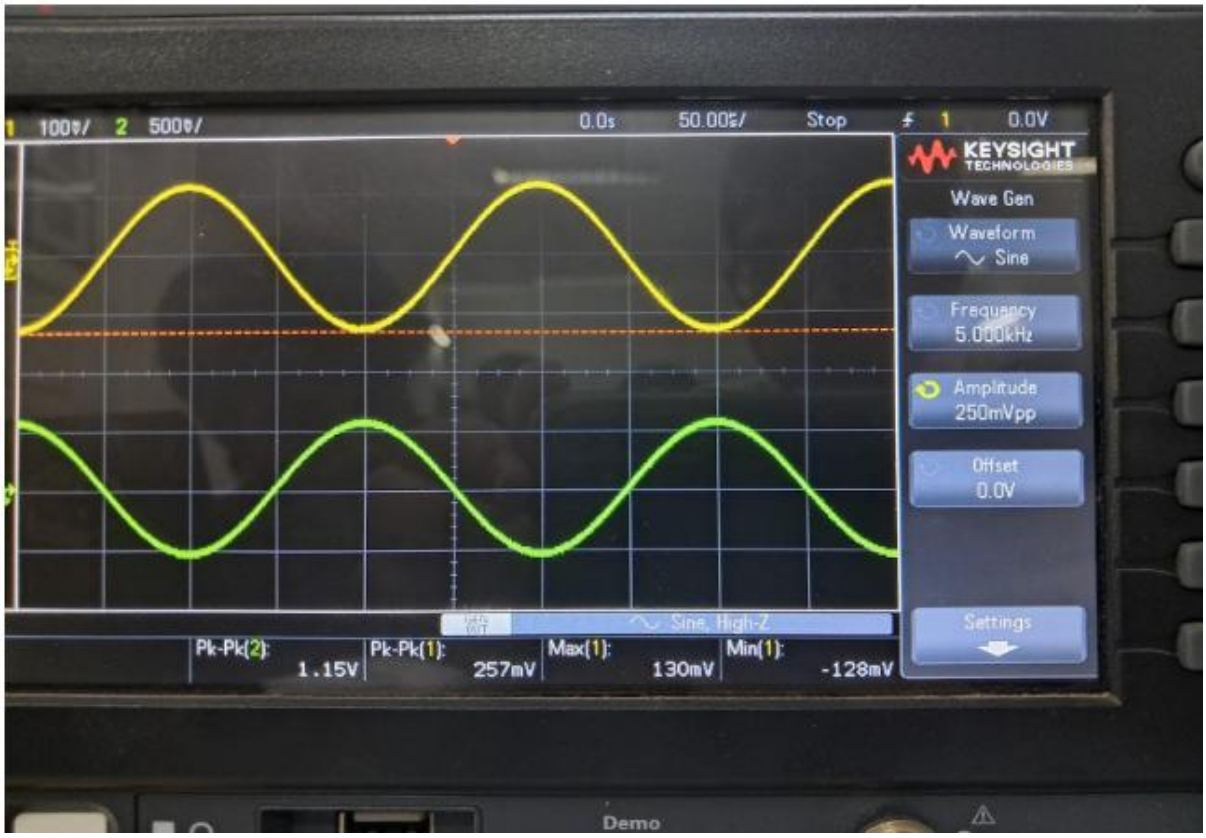
Second part

Choosing resistances for obtaining custom gain from inverting amplifier

calculation of R1 and R2 for obtaining a gain of 4 and 5

by taking r1 as 60kohm and r2 as 240(-4gain) and 300(-5gain) by formula r1/r2 = gain = -- vout/vin;





Expected Gain	R1 (kΩ)	R2 (kΩ)	Vout (mVpp)	Observed Gain
-4	60	240	960	-3.735
-5	60	300	1150	-4.4

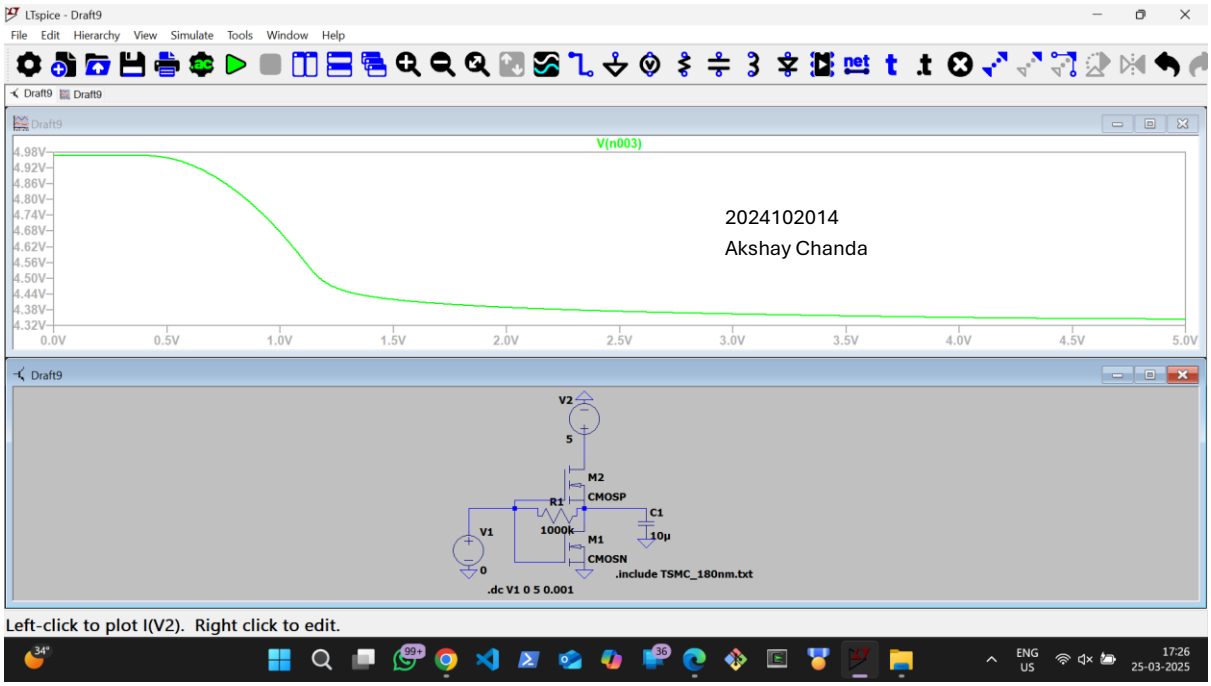
Conclusion

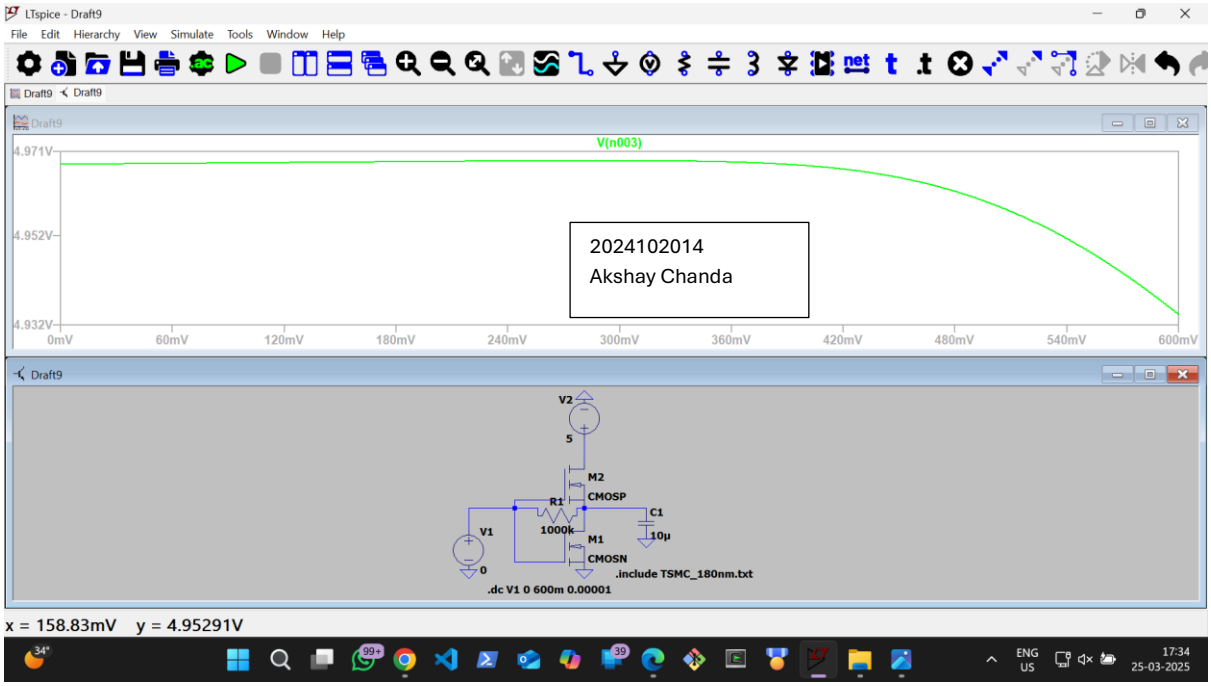
The inverting amplifier gain closely matches theoretical values. Output is inverted as expected.

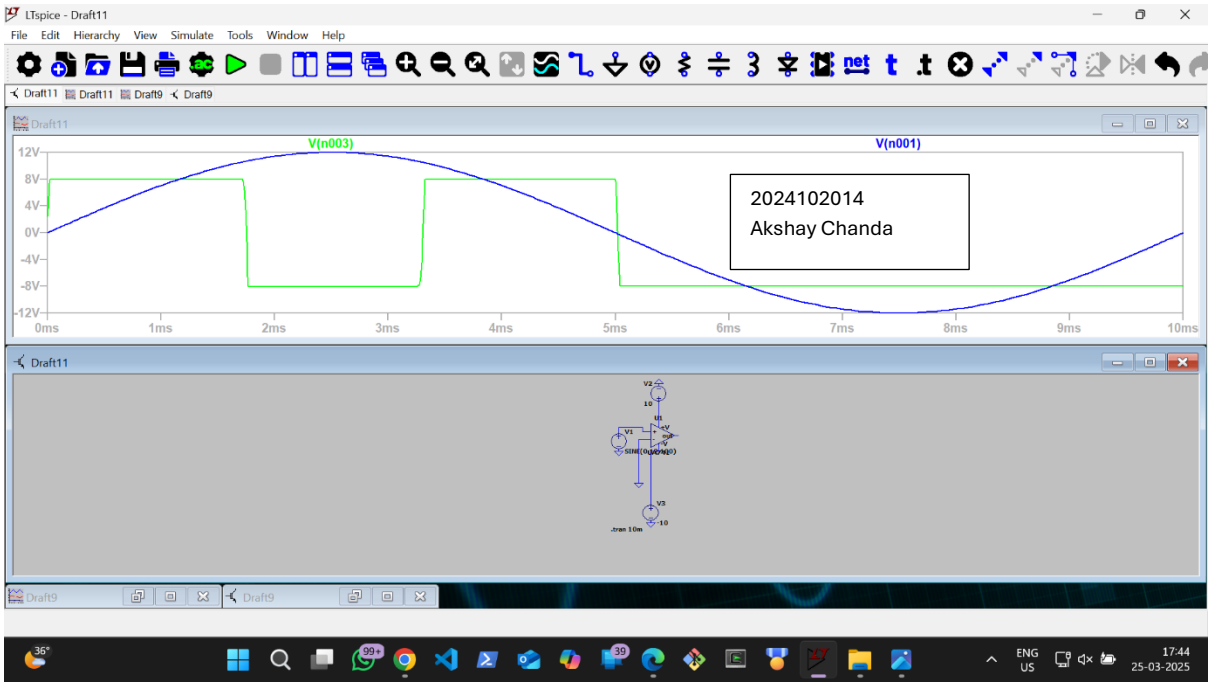
Overall Conclusion

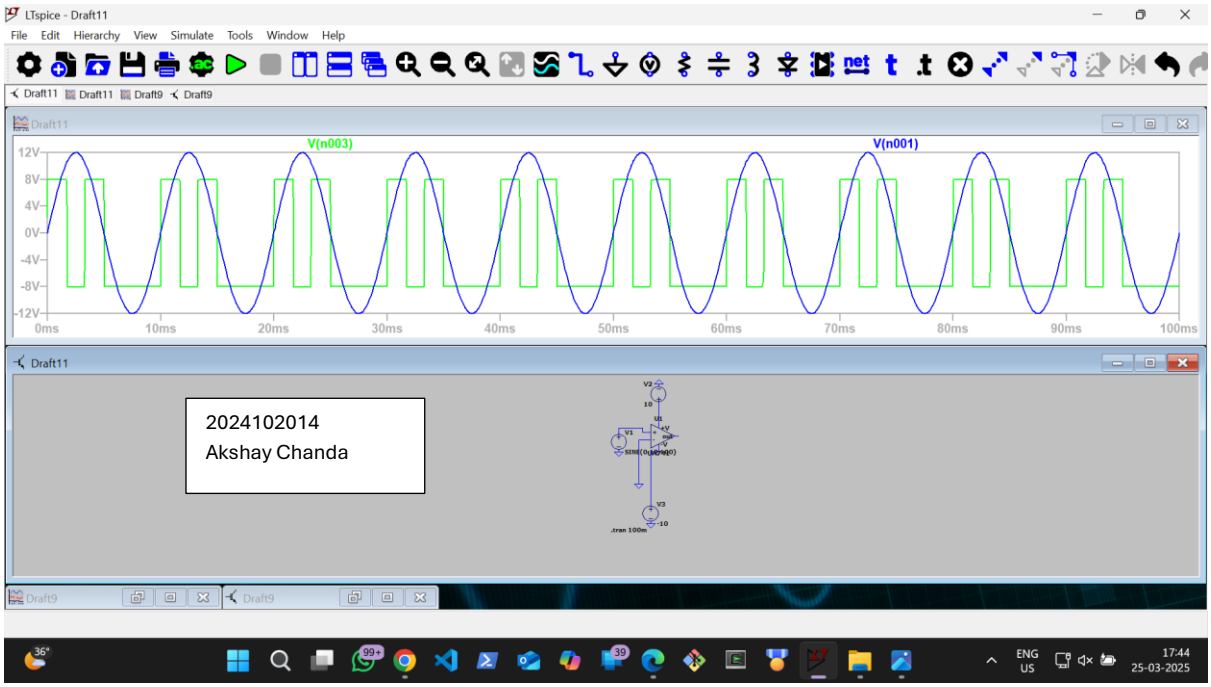
- **CMOS Inverter:** Works as an amplifier in a limited input range.
- **Op-Amp Characterization:** Shows high gain and DC offset.
- **Non-Inverting Amplifier:** Gain follows **1 + (R1/R2)**.
- **Inverting Amplifier:** Gain follows **-(R1/R2)**.

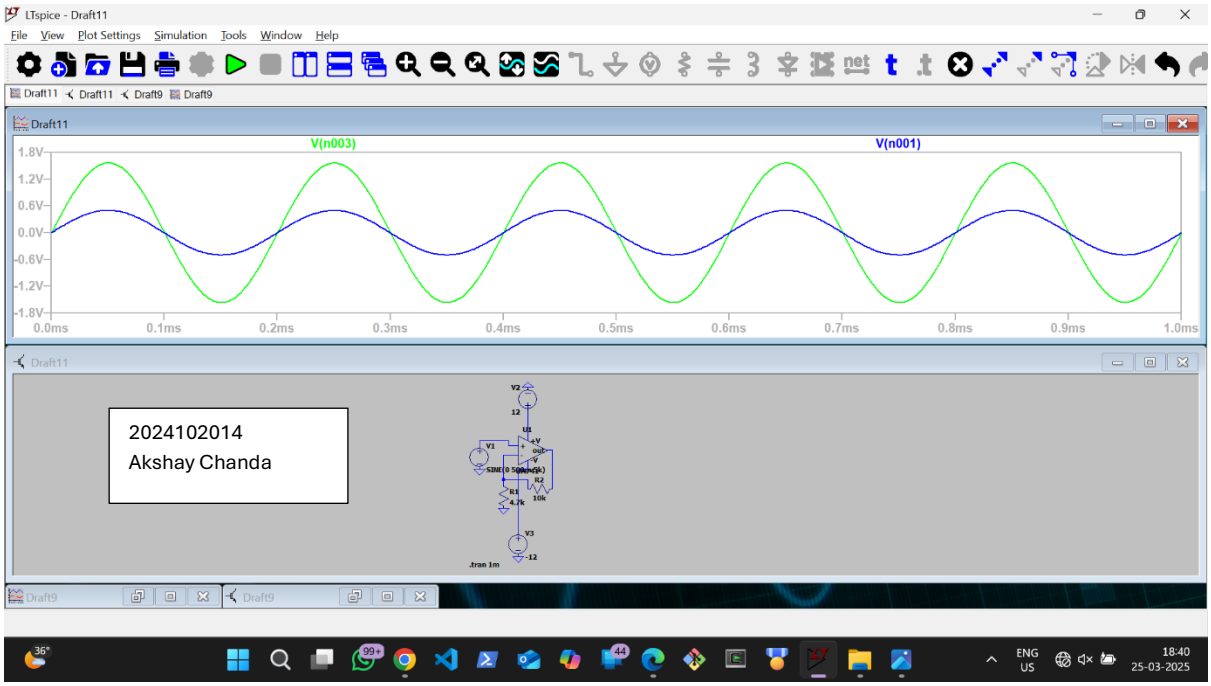
LTSPICE

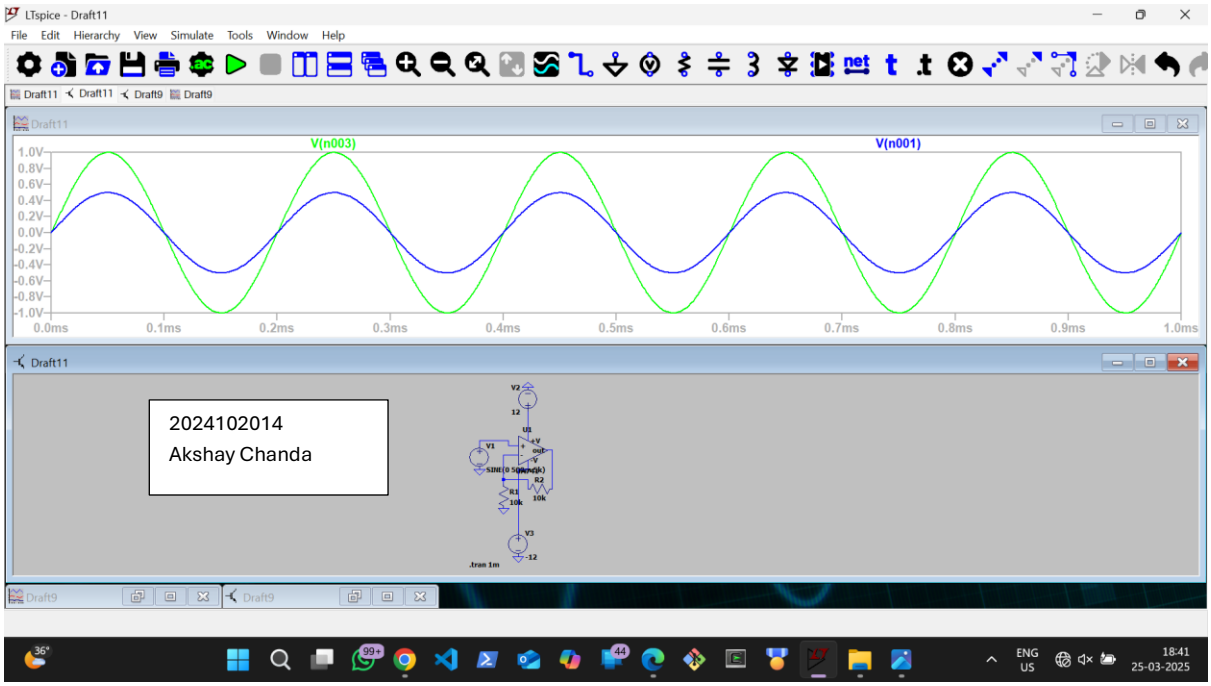

LTspice - Draft9
File Edit Hierarchy View Simulate Tools Window Help
Draft9
V(n003)
4.98V
4.92V
4.86V
4.80V
4.74V
4.68V
4.62V
4.56V
4.50V
4.44V
4.38V
4.32V
0.0V
0.5V
1.0V
1.5V
2.0V
2.5V
3.0V
3.5V
4.0V
4.5V
5.0V
2024102014
Akshay Chanda
V2
5
M2
CMOSP
R1
1000k
C1
10µ
V1
M1
CMOSN
0
.include TSMC_180nm.txt
.dc V1 0 5 0.001
Left-click to plot I(V2). Right click to edit.
ENG
US
17:26
25-03-2025

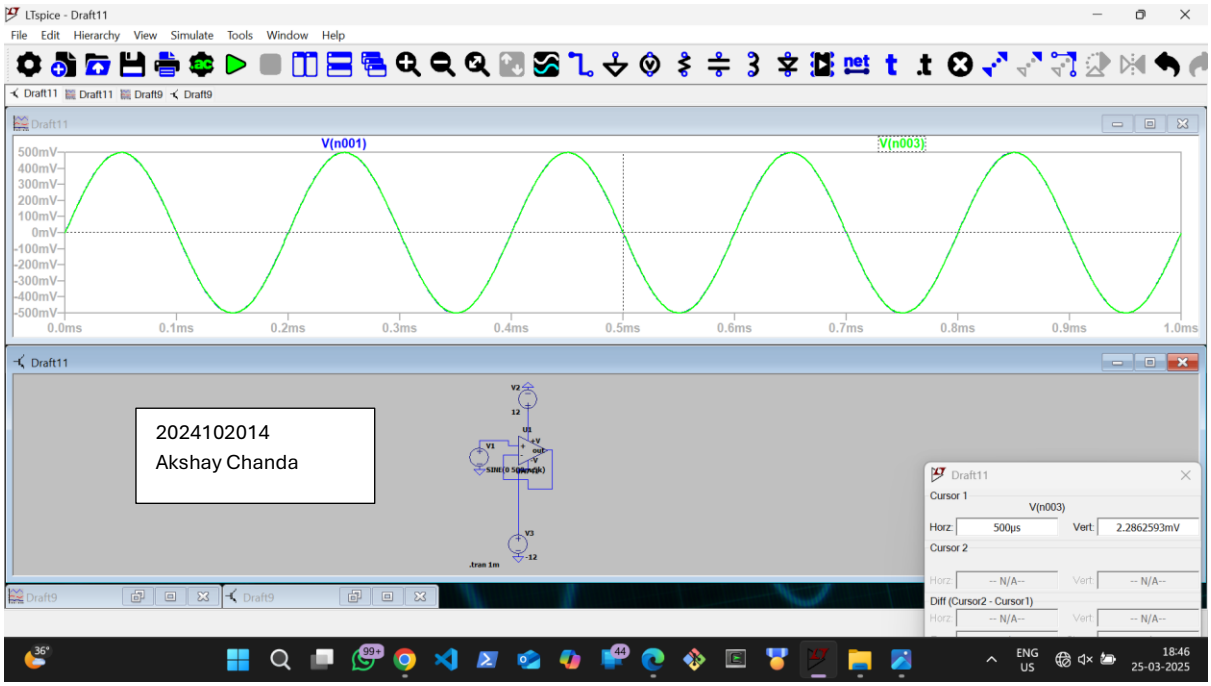

LTspice - Draft9
File Edit Hierarchy View Simulate Tools Window Help
Draft9
V(n003)
4.971V
4.952V
4.932V
0mV
60mV
120mV
180mV
240mV
300mV
360mV
420mV
480mV
540mV
600mV
2024102014
Akshay Chanda
V2
5
M2
CMOSP
R1
1000k
C1
10µ
V1
M1
CMOSN
0
.include TSMC_180nm.txt
.dc V1 0 600m 0.00001
x = 158.83mV y = 4.95291V
ENG
US
17:34
25-03-2025

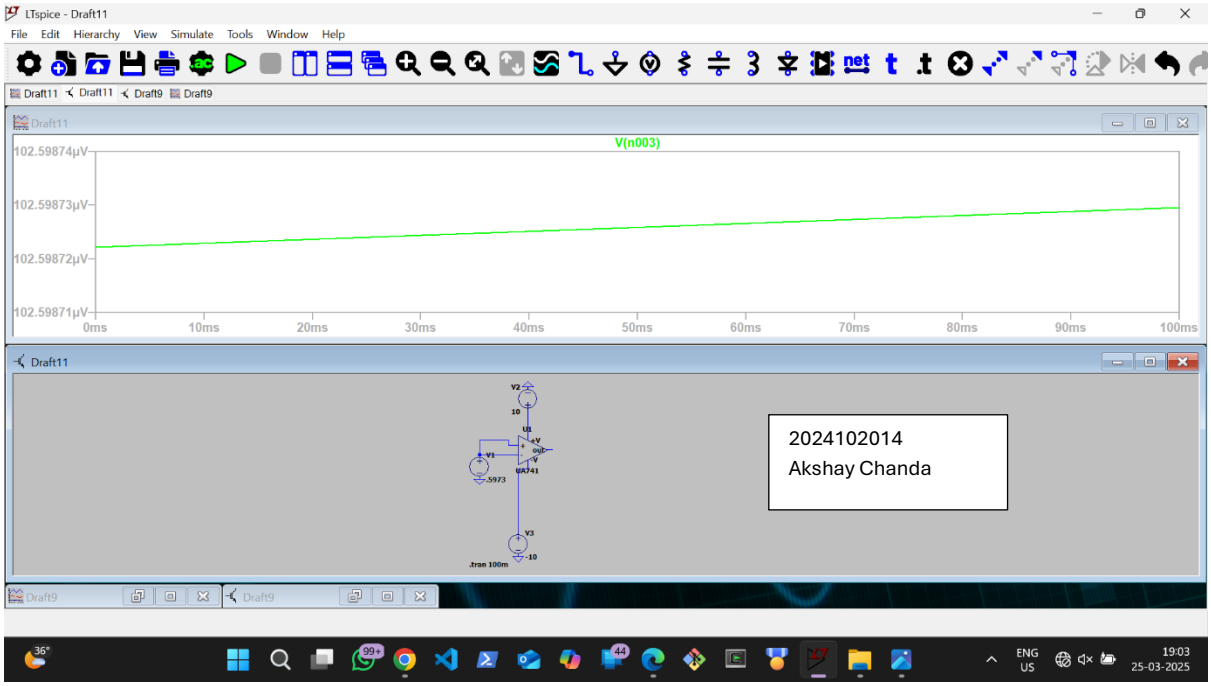

LTspice - Draft11
File Edit Hierarchy View Simulate Tools Window Help
V(n003)
V(n001)
12V
8V
4V
0V
-4V
-8V
-12V
0ms 1ms 2ms 3ms 4ms 5ms 6ms 7ms 8ms 9ms 10ms
2024102014
Akshay Chanda
Draft11
.tran 10m

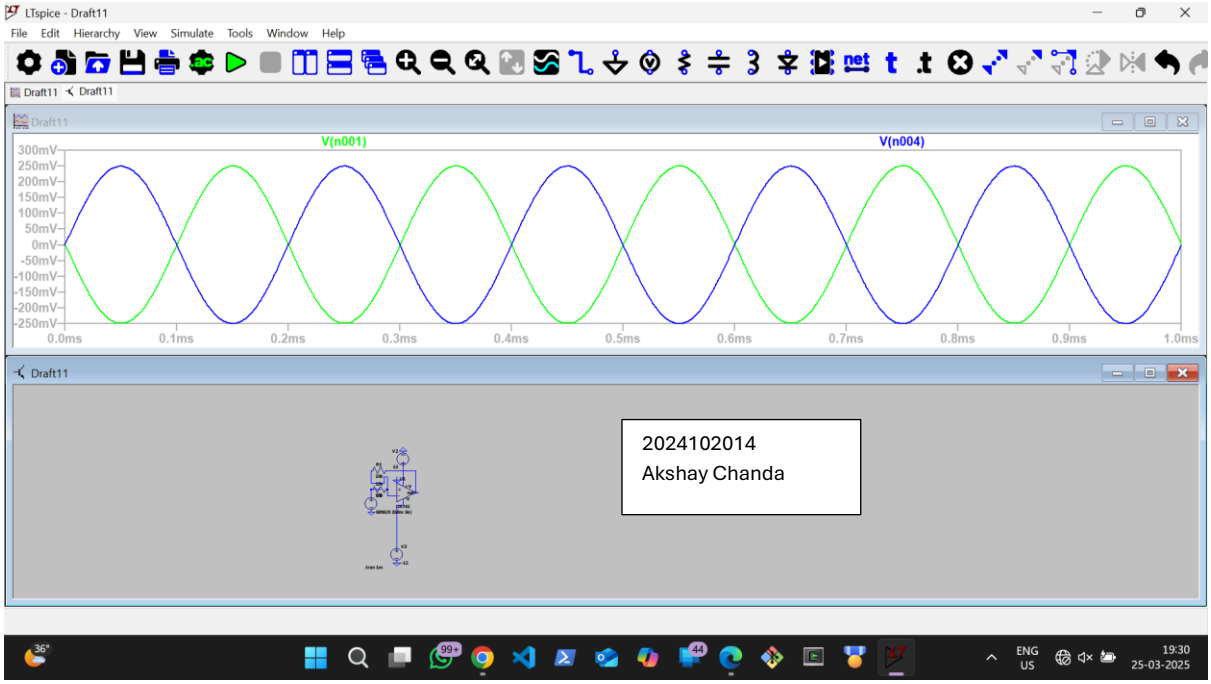

LTspice - Draft11
File Edit Hierarchy View Simulate Tools Window Help
V(n003)
V(n001)
12V
8V
4V
0V
-4V
-8V
-12V
0ms 10ms 20ms 30ms 40ms 50ms 60ms 70ms 80ms 90ms 100ms
2024102014
Akshay Chanda
Draft11
.tran 100m

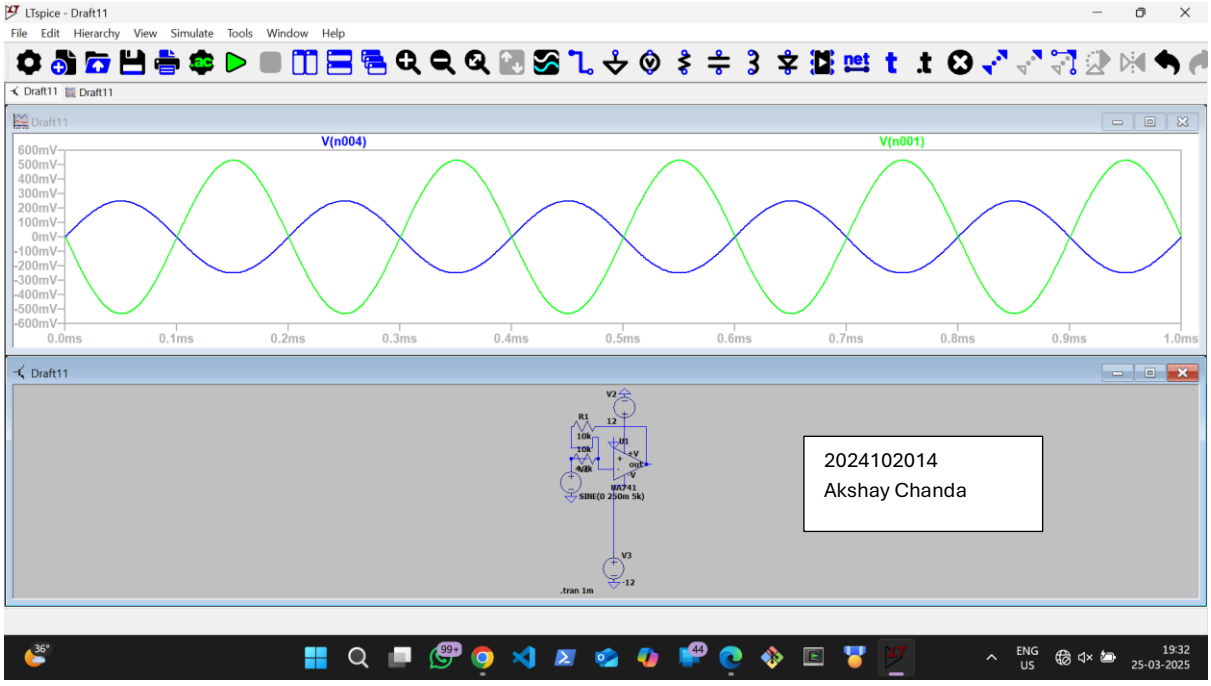

LTspice - Draft11
File View Plot Settings Simulation Tools Window Help
Draft11
V(n003)
V(n001)
1.8V
1.2V
0.6V
0.0V
-0.6V
-1.2V
-1.8V
0.0ms 0.1ms 0.2ms 0.3ms 0.4ms 0.5ms 0.6ms 0.7ms 0.8ms 0.9ms 1.0ms
2024102014
Akshay Chanda
V2
12
U1
V1
SINE(0 500mV 1k)
R1
4.7k
R2
10k
V3
-12
.tran 1m
18:40
25-03-2025


LTspice - Draft11
File Edit Hierarchy View Simulate Tools Window Help
Draft11
V(n003)
V(n001)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
-0.4V
-0.6V
-0.8V
-1.0V
0.0ms 0.1ms 0.2ms 0.3ms 0.4ms 0.5ms 0.6ms 0.7ms 0.8ms 0.9ms 1.0ms
2024102014
Akshay Chanda
V2
12
U1
V1
SINE(0 500mV 1k)
R1
10k
R2
10k
V3
-12
.tran 1m
18:41
25-03-2025


LTspice - Draft11
File Edit Hierarchy View Simulate Tools Window Help
V(n001)
V(n003)
2024102014
Akshay Chanda
Cursor 1
V(n003)
Horz: 500µs
Vert: 2.2862593mV
Cursor 2
Diff (Cursor2 - Cursor1)
ENG US
18:46
25-03-2025


LTspice - Draft11
File Edit Hierarchy View Simulate Tools Window Help
V(n003)
102.59874µV
102.59873µV
102.59872µV
102.59871µV
2024102014
Akshay Chanda
ENG US
19:03
25-03-2025


LTspice - Draft11
File Edit Hierarchy View Simulate Tools Window Help
Draft11
V(n001)
V(n004)
300mV
250mV
200mV
150mV
100mV
50mV
0mV
-50mV
-100mV
-150mV
-200mV
-250mV
0.0ms
0.1ms
0.2ms
0.3ms
0.4ms
0.5ms
0.6ms
0.7ms
0.8ms
0.9ms
1.0ms
2024102014
Akshay Chanda
ENG
US
19:30
25-03-2025


LTspice - Draft11
File Edit Hierarchy View Simulate Tools Window Help
Draft11
V(n004)
V(n001)
600mV
500mV
400mV
300mV
200mV
100mV
0mV
-100mV
-200mV
-300mV
-400mV
-500mV
-600mV
0.0ms
0.1ms
0.2ms
0.3ms
0.4ms
0.5ms
0.6ms
0.7ms
0.8ms
0.9ms
1.0ms
V2
12
R1
10k
10k
U1
-V
+
out
V
uA741
SINE(0 250m 5k)
V3
-12
.tran 1m
2024102014
Akshay Chanda
ENG
US
19:32
25-03-2025