DSM Tutorial Quiz Questions (Post Midsems)

October 16th

Q1

You have an 8-bit bidirectional shift register with the initial value 11001100. The register can shift both left and right, and it has an additional control input (C) that determines the direction:
C = 0 shifts the register to the left.
C = 1 shifts the register to the right.
Each shift operation also takes in an external input bit (D_in) that is inserted into the register from the direction of the shift. The external input bits provided are: 1, 0, 1, 1 (used in the order of each shift operation).
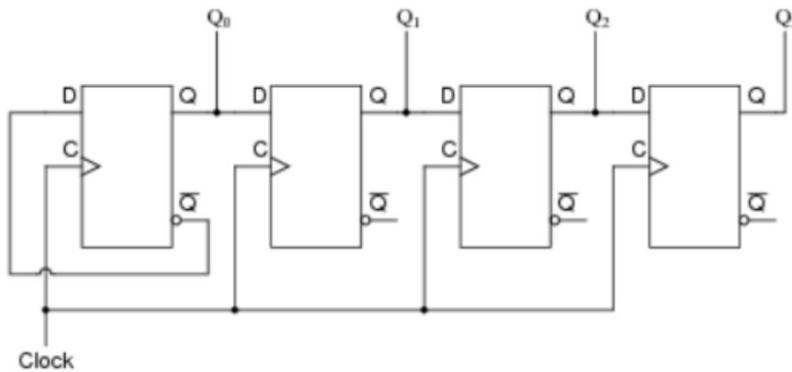The sequence of operations is as follows:

1. Shift left (C = 0) with D_in = 1

2. Shift right (C = 1) with D_in = 0

3. Shift left (C = 0) with D_in = 1
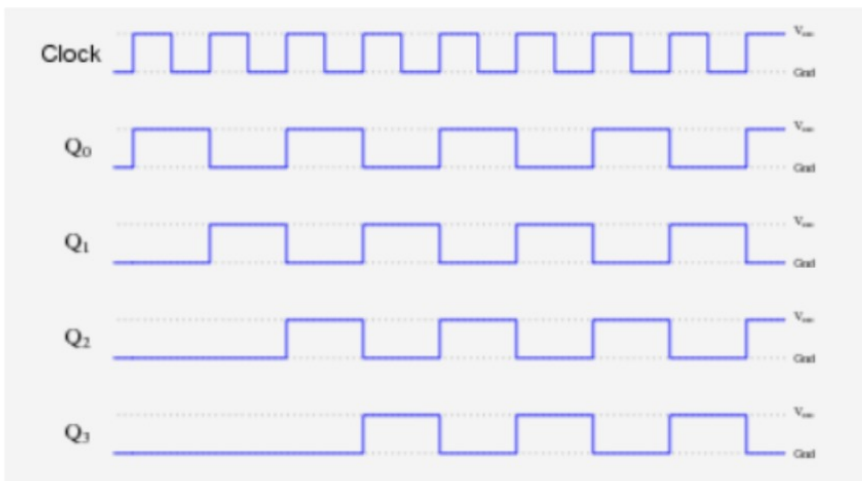
4. Shift left (C = 0) with D_in = 1
   What will be the final value in the shift register after these 4 operations?

Answer : 00110011

2. Complete the timing diagram for this circuit, assuming all Q outputs begin in the low state:

A.

The input to each consecutive flip-flop keeps alternating at their first clock pulse. If k is the output at flip-flop 1, k will be the input for flip-flop 2 and k' will be the input for flip-flop 1. If we keep on repeating this, we get k as the input for flip-flop i whenever i is even and k' as the input whenever i is odd.
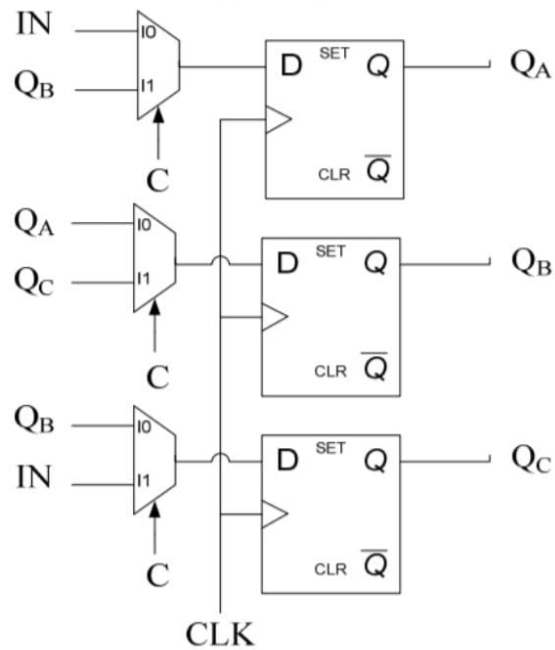
October 15th

Q1

Design a 3-bit shift register using 2:1 Mux and D Flip Flops which shifts right if the control input, C = 0 and shifts left if C = 1?

Ans

If C = 0, the circuit shifts from IN → Q_A → Q_B → Q_C and
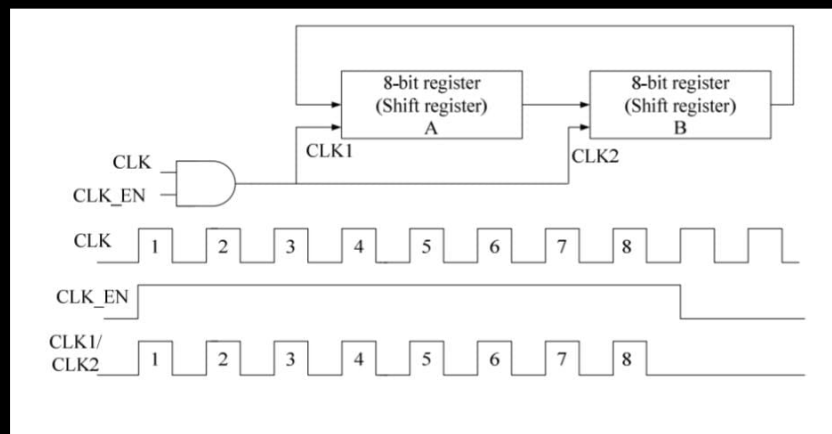If C = 1, the circuit shifts from IN → Q_C → Q_B → Q_A

Q2

How to swap the contents of two 8-bit registers without using a third register.

Ans

The complete design using shift registers is shown in the following figure. The main clock is gated with the clock enable so that A and B will be shifted just 8 clocks. After 8 clocks A and B will have their contents swapped.

October 11th

Q1

State Reduction: A sequential circuit has the following state table:

Curr State	Next State (I = 0)	Next State (I = 1)	Output (I = 0)	Output (I = 1)
A	A	C	1	0
B	A	D	1	0
C	D	A	0	1
D	D	A	0	1

Perform state reduction to find the minimum equivalent state table.

Solution:

- The state reduction process involves finding equivalent states. In this case, states C and D can be combined because they have the same behavior for all inputs. The reduced state table is:

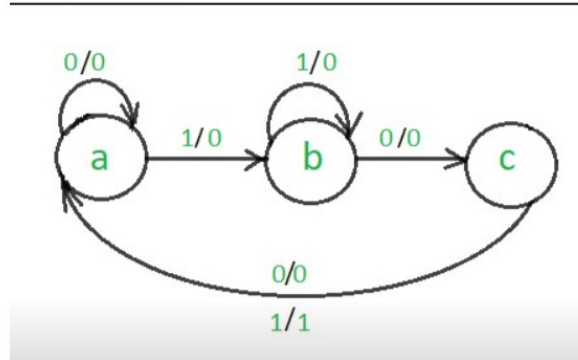| Curr State	Next State (I = 0)	Next State (I = 1)	Output (I = 0)	Output (I = 1)
A	A	C(=D)	1	0
B	A	D	1	0
D	D	A	0	1

- Similarly, since C and D are equivalent, states A and B can be combined because they have the same behavior for all inputs.

Curr State	Next State (I = 0)	Next State (I = 1)	Output (I = 0)	Output (I = 1)
A	A	D	1	0
D	D	A	0	1

Q2

2. Develop a "101" sequence detector using D flip flops
A. This is the state diagram:

Consider state a to be 00, state b to be 10, state c to be 01

Using D flip flops, this will be the final truth table:

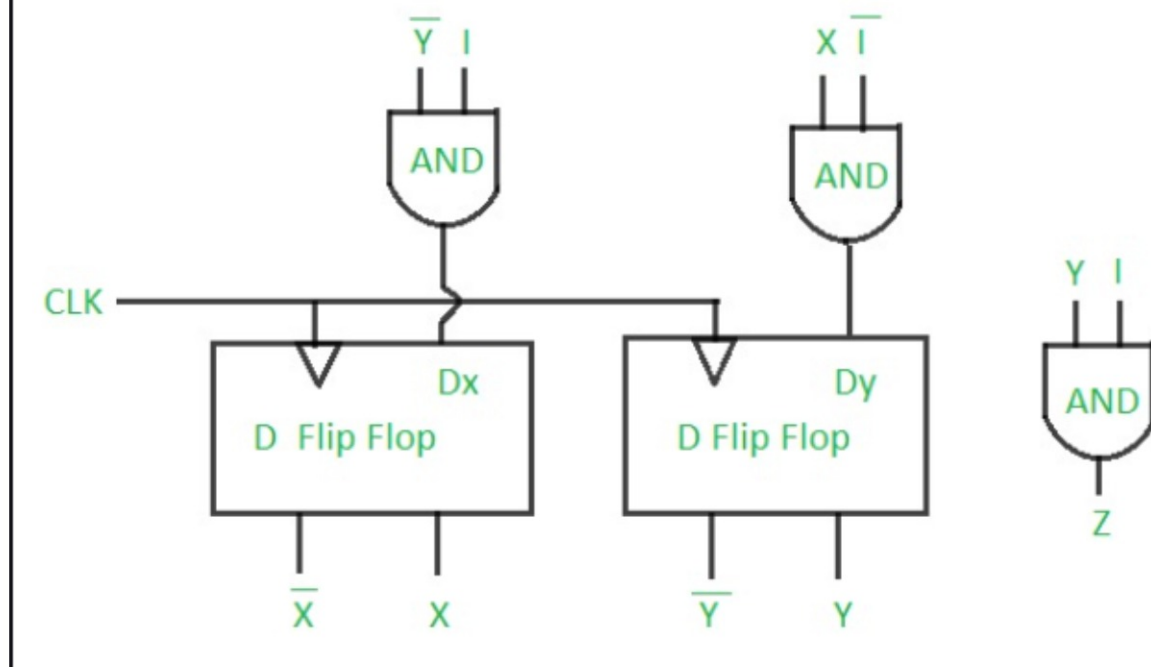| Present X state (X)	Present Y state (Y)	Input (I)	Next X state (X')	Next X state (Y')	Dx	Dy	Output (Z)
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	0	0
0	1	1	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	1	1	0	1	0	0
1	1	0	X	X	X	X	X
1	1	1	X	X	X	X	X

Using K-maps, we get
Dx = Y'.I
Dy = X.I'
Z = Y.I

Circuit diagram:

October 10th

Q1

1. Implement D flip-flop using JK flipflop

D	Qn	Qn+1	J	K
0	0	0	0	x
0	1	0	x	1
1	0	1	1	x
1	1	1	x	0

The first 3 columns show all the cases for D flipflop.

For the transition Qn = 0 and Qn+1 = 0, we just need J to be 0 as the state won't change when K=0 and Q will remain 0 when K=1.
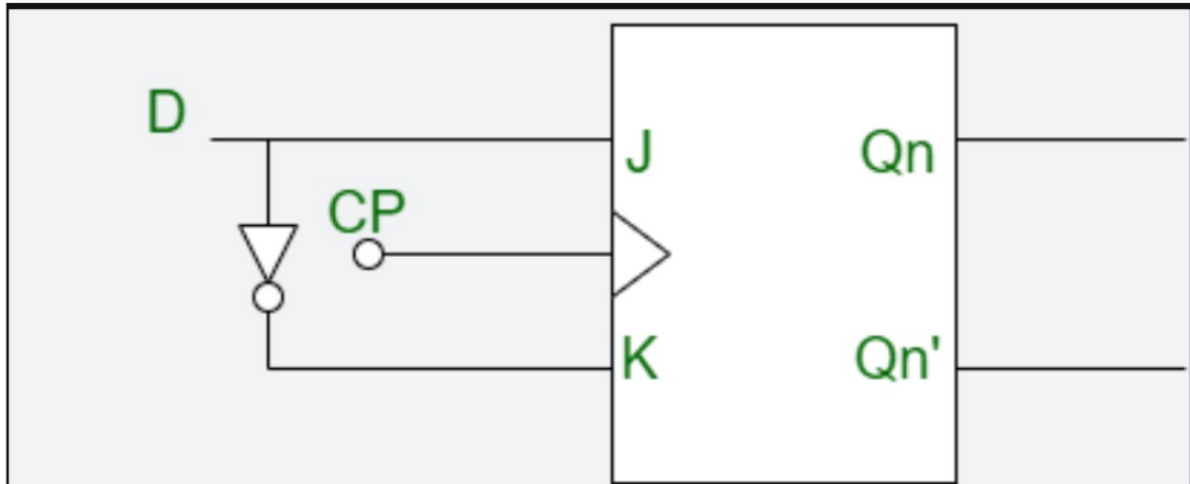For the transition Qn = 0 and Qn+1 = 1, we need J to be 1 as the state toggles when K=1 and Q will change to 1 when K=0.
For the transition Qn = 1 and Qn+1 = 0,we need K to be 1 as the state toggles when J=1 and Q changes to 0 when J=0.
For the transition Qn = 1 and Qn+1 = 1,we need K to be 0 as the state remains the same when J=0 and Q remains 1 when J=1.

For D and Qn as inputs and J as output, we apply a K-map and we'll get the equation
J=D

For D and Qn as inputs and K as output, we apply a K-map and we'll get the equation K=D'.
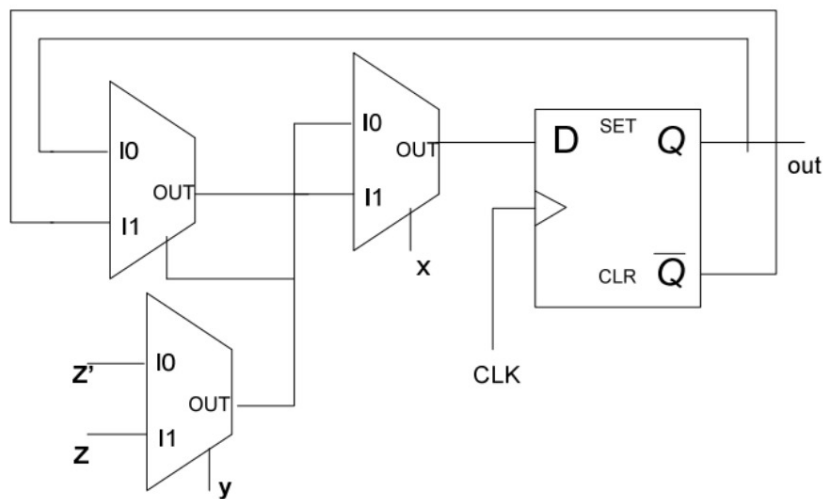
So, our final circuit will be:

Q2

Using DFFs and minimum no. of 2×1 Mux, implement the following XYZ flip-flop. (Assume you have the inverse f the variables also)

X	Y	Z	Q(t+1)
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	Q(t)
1	0	1	Q(t)`
1	1	0	Q(t)`
1	1	1	Q(t)

Ans

It is clear that if X=0, Q(t+1) = Y XNOR Z. If X =1 and if (Y XNOR Z), Q(t+1) = Q(t), else Q(t)'. So we need one 2:1 mux to generate Y XNOR Z. One to select Q(t) and Q(t)' and one more to select between X=0 case and X=1 case. Total we need 3 2:1 mux.
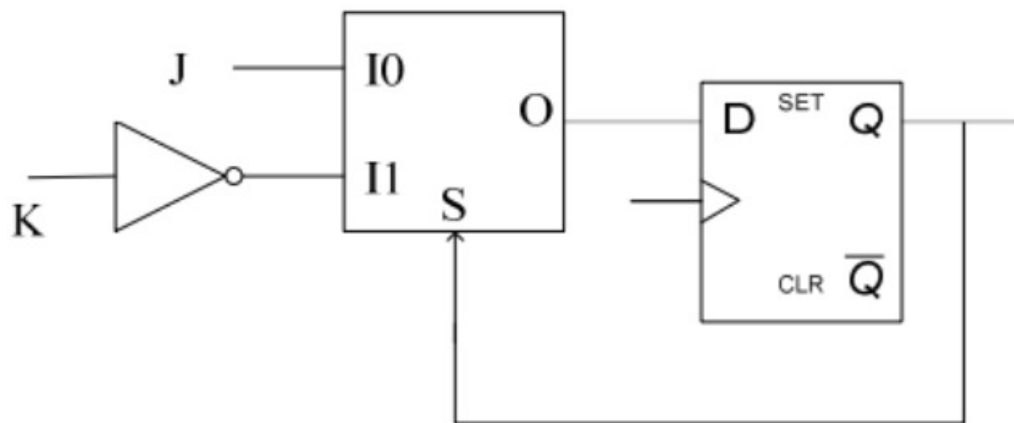
October 9th

Q1

Construct a J-K flip flop using a DFF, 2:1 Mux and an-inverter

Ans

The catch here is to use Q as select line. You can observe the cofactors of Q(t+1) with respect to J,K and Q(t). Using J or K as the select line with 2:1 mux will not do.

Q2

2. A sequential circuit with two D flip-flops A and B, inputs x and y, and output z is specified by the following next-state and output equations:

$$A(t+1) = x'y + xB$$

$$B(t+1) = xA + yB$$

$$z = A'$$

Construct the state table for this circuit.

2. • The resultant state table would be:

Present State		Input		Next State		Output
A	B	x	y	A(t+1)	B(t+1)	z
0	0	0	0	0	0	1
0	0	0	1	1	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	0	1
0	1	0	1	1	1	1
0	1	1	0	1	0	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	1	0
1	1	0	0	0	0	0
1	1	0	1	1	1	0
1	1	1	0	1	1	0
1	1	1	1	1	1	0