

# DSM Midsem Grading Scheme

October 7, 2024

## TA Distribution

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## Answer 1

In all circuit diagrams, marks will not be cut for assuming the complement of the variables as direct inputs.

### Subpart(a)

Simplify below Boolean function and implement using minimum NOR gates.  $F = \prod(1,3,6,9,11,12,14)$  (4)

Can simplify to one of the below 2 methods:

#### POS form

To get a POS form in  $y$ , obtain the SOP form in  $y'$ .

Consider the kmap and truth table for  $y'$ :

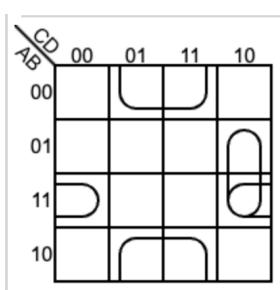


Figure 1: K-Map

	A	B	C	D	Y
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	1
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	0
14	1	1	1	0	1
15	1	1	1	1	0

Figure 2: Truth Table

$$\bar{y} = \overline{B} \cdot D + B \cdot C \cdot \overline{D} + A \cdot B \cdot \overline{D}$$

$$\bar{y} = \overline{\overline{B} \cdot D + B \cdot C \cdot \overline{D} + A \cdot B \cdot \overline{D}}$$

$$y = (B + \overline{D}) \cdot (\overline{B} + \overline{C} + D) \cdot (\overline{A} + \overline{B} + D)$$

So simplified y in POS form:

$$y = (B + \overline{D}) \cdot (\overline{B} + \overline{C} + D) \cdot (\overline{A} + \overline{B} + D)$$

To implement circuit using nor gate:

$$\bar{y} = \overline{(B + \overline{D}) \cdot (\overline{B} + \overline{C} + D) \cdot (\overline{A} + \overline{B} + D)}$$

$$\bar{y} = \overline{(B + \overline{D})} + \overline{(\overline{B} + \overline{C} + D)} + \overline{(\overline{A} + \overline{B} + D)}$$

$$y = \bar{y} = \overline{((B + \overline{D}) + (\overline{B} + \overline{C} + D) + (\overline{A} + \overline{B} + D))}$$

Circuit Diagram:

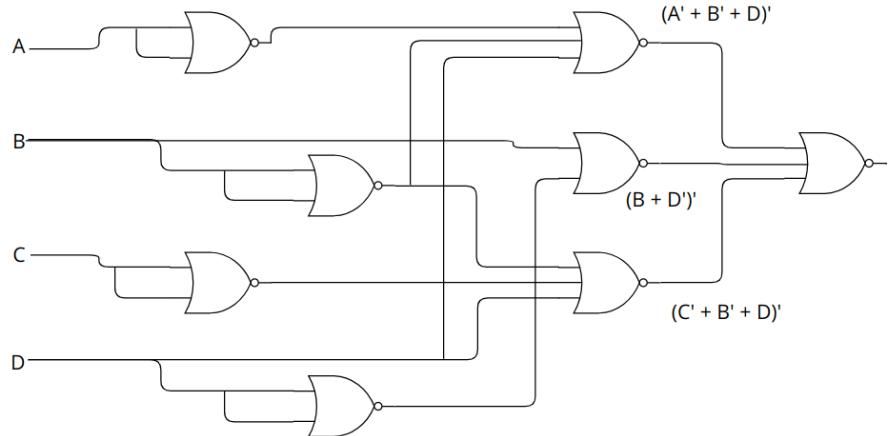


Figure 3: Circuit Diagram

### SOP form

Use a K-Map to get f in SOP form:

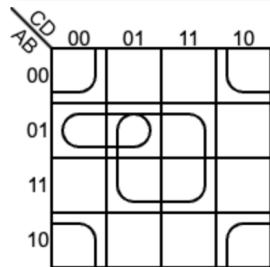


Figure 4: K-Map

Truth Table					
	A	B	C	D	Y
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	1
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	0
15	1	1	1	1	1

Figure 5: Truth Table

y in SOP form:

$$y = B \cdot D + \overline{B} \cdot \overline{D} + \overline{A} \cdot B \cdot \overline{C}$$

To use NOR gates:

$$\bar{y} = \overline{(B \cdot D + \overline{B} \cdot \overline{D} + \overline{A} \cdot B \cdot \overline{C})}$$

$$\bar{y} = \overline{(B \cdot D)} \cdot \overline{(\overline{B} \cdot \overline{D})} \cdot \overline{(\overline{A} \cdot B \cdot \overline{C})}$$

$$\bar{y} = (\overline{B} + \overline{D}) \cdot (B + D) \cdot (A + \overline{B} + C)$$

$$y = \bar{y} = \overline{((\overline{B} + \overline{D}) \cdot (B + D) \cdot (A + \overline{B} + C))}$$

$$y = \overline{(\overline{B} + \overline{D})} + \overline{(B + D)} + \overline{(A + \overline{B} + C)}$$

$$y = (y')' = \overline{\overline{\overline{(\overline{B} + \overline{D})}} + \overline{(B + D)} + \overline{(A + \overline{B} + C)}}$$

Circuit:

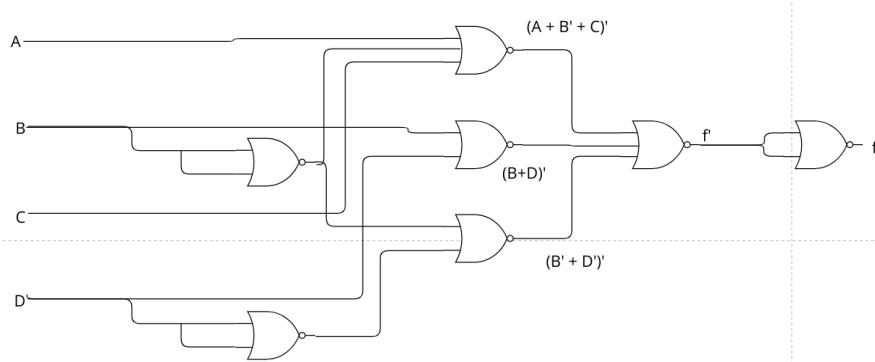


Figure 6: NOR Gate Circuit Diagram

Marking scheme:

- (Step 1) Simplification into POS or SOP form - **(1 Mark)**

Partial marks of 0.5 if the POS or SOP form is very close. Otherwise no partial marks will be given. 0.5 given if at least 2 terms match with the correct POS or SOP form.

- (Step 2) Conversion to a format plausible by NOR gates and Any NOR circuit implementation with the correct output - **(3 Marks)**

1. If (Step 1) goes wrong, and (Step 2) is in accordance with (Step 1) then 1.5 mark will be given.

2. **Special case:** In SOP method many have taken both the terms  $A'BC'$  and  $A'C'D'$ . only 1 of the 2 are required to cover m4 cell. if you have taken both, then 0.5 mark awarded in step 1 and 2 marks awarded in step 2.

3. If (Step 1) is correct, and (Step 2) is in accordance with (Step 1) then full marks (3) will be given.

4. If (Step 1) is correct, and (Step 2) went wrong then marks between 1 and 2 will be awarded based on effort. Few cases:

5. **Common case:** In SOP method many have forgot to put a nor gate at the end of the circuit diagram. if you don't put a nor gate, you get  $F'$ . In such a case, if step 1 is correct 2 marks given in step 2, if step 1 is incorrect 1 mark is given in step 2

- **Note:** If anyone has not even attempted to simplify the function, and has directly used al minterms, then given 0 marks in step 1 and 1.5 mark in step 2 if the diagram is correct.
- **Note:** Implementing using POS form with AND/OR gates and then writing their NOR equivalents will be awarded **full marks**. Any other simplification other than using POS and SOP will be awarded partial marks 1-3 based on the effort.

### Subpart(b)

Implement above Boolean function using multiplexer. (3)

The connections to the select line can be inferred by comparing the values of D and the output Y in the truth table(5).

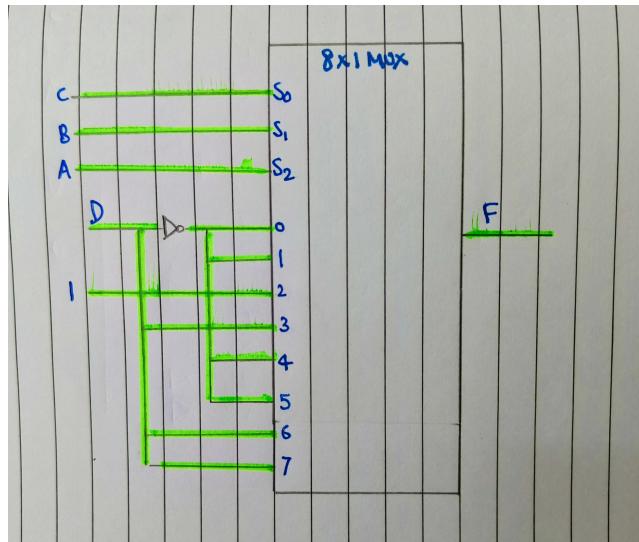


Figure 7: Circuit using MUX

### Marking Scheme

- **3 Marks:** A completely correct circuit diagram using a single 4:1 or 8:1 MUX.
- **Common Mistake:** Drawing the circuit diagram for  $F'$  (complement of  $F$ ) instead of  $F$ .
- **Partial Marks:** Awarded in all other cases where the circuit diagram is incorrect, based on:
  - Correctness of the truth table.
  - Explanation of the relation between the input variable  $D$  and the output variable.
  - Any other relevant explanation or partial work.

## Answer 2

A binary-coded-decimal (BCD) message appears in four input lines of a digital circuit. Design an NAND gate network with minimum possible gates that produces an output value 1 whenever the input combination is 0, 1, 3, 5, or 8. (4)

In all circuit diagrams, marks will not be cut for assuming the complement of the variables as direct inputs.

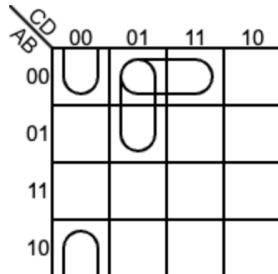


Figure 8: K-Map (1 Mark)

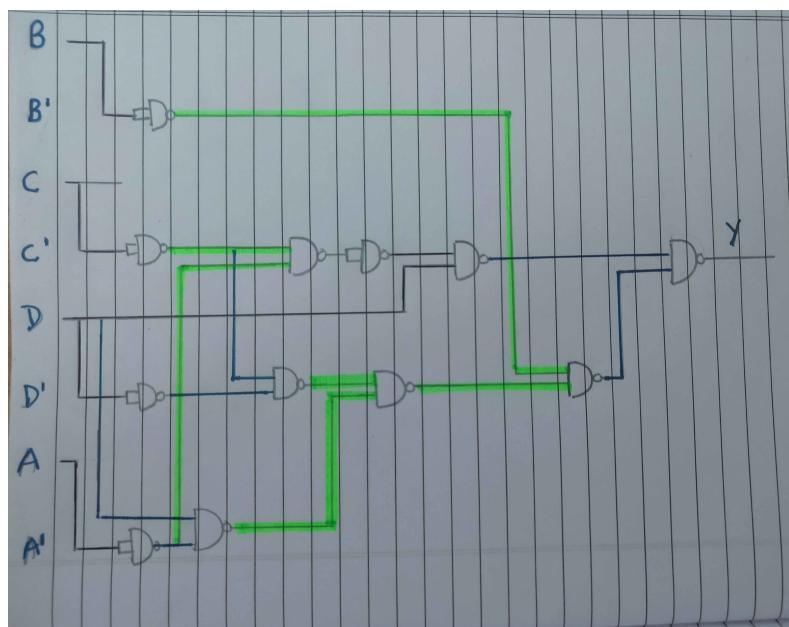


Figure 9: Circuit Diagram (3 Marks)

### Marking Scheme

**Total Marks: 4 (1.5 for Expression, 2.5 for Circuit)**

- **1.5 Marks for Expression:**

- **1.5 Marks:** Correct expression with the minimum number of terms.
- **1 Mark:** Correct expression, but not using the minimum number of terms.
- **0.5 or 0 Marks:** In all other cases, depending on the level of simplification.

- **2.5 Marks for Circuit:**

- **2.5 Marks:** Correct circuit that uses the minimum number of NAND gates.

- **General Note:** If the expression obtained in the initial part is wrong, maximum of 2 marks are given for the question.

- **Common Mistakes:**

- The simplified expression should have at most 3 terms. If it has more than 3 terms, a maximum of **3 to 3.5 Marks** is given even if the rest of the solution is correct.

## Answer 3

### Subpart(a)

Design one digit octal numbers comparator with minimum possible number of gates. (3)

Since it is a one digit octal comparator, we need only 3 bits.

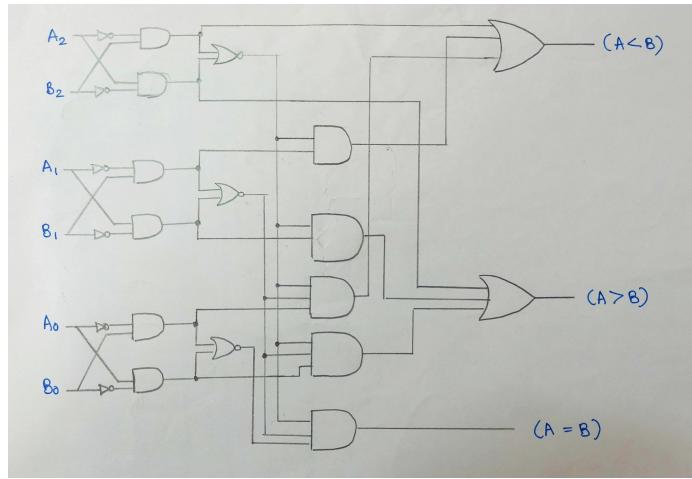


Figure 10: Circuit Diagram

**Marking Scheme:** Full marks awarded if the complete circuit is implemented correctly with minimum number of gates. Partial marks in all other cases.

### Subpart(b)

What is the need for priority encoder? (2)

In a standard encoder, if multiple inputs are equal to 1 at the same time, it can lead to ambiguity since the encoder will not know which input to prioritize. A priority encoder solves this by assigning priority to inputs based on their significance which is decided beforehand, ensuring that only the highest-priority input equal to 1 is encoded.

**Marking Scheme:** Full marks awarded if all the necessary points are covered . Partial marks in all other cases

### Subpart(c)

Perform  $(546)_8 - (342)_8$  using 8's complement. (2)

Since the subtraction is of the form  $M - N$  and  $M > N$ ,

Find the 8's complement of  $(342)_8 = 436$

Add the 8's complement of  $N$  to  $M \Rightarrow 546 + 436 = (1204)_8$

Discard the end carry:  $(204)_8$

**Final answer is  $(204)_8$**

**Marking Scheme:**

- **Case 1:** Fully correct solution, accurately applying the 8's complement method – **2 Marks**
- **Case 2:** Mostly correct solution with a minor error, but the 8's complement method was applied correctly – **1.5 Marks**
- **Case 3:** Correct answer achieved through an incorrect method, without using the 8's complement – **1 Mark**
- **Case 4:** Incorrect solution using an incorrect method, without applying the 8's complement – **0.5 Marks**
- **Case 5:** No logical approach or irrelevant attempt – **0 Marks**

**Subpart(d)**

Compare usage of encoder and multiplexer. **(2)**

Encoders convert  $2^n$  (or fewer) input lines to  $n$  output lines.

Multiplexers select one of  $2^n$  signals based on  $n$  selection lines, whose bit combinations determine which input is selected and routed to the single output.

**Marking Scheme:**

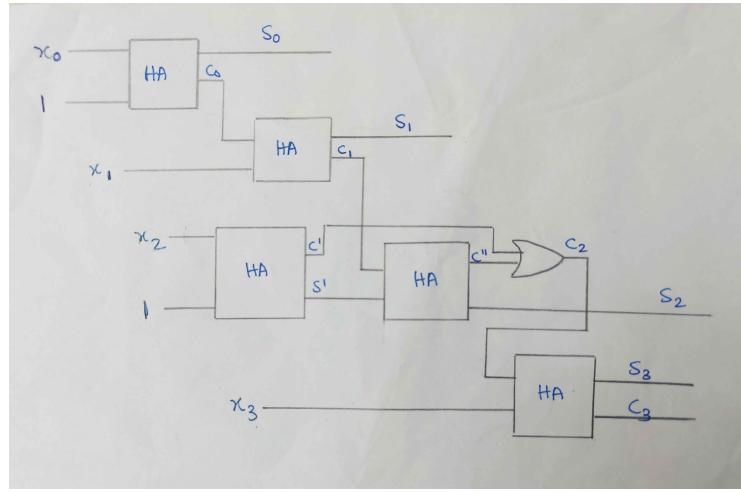
- **Case 1:** Clear and accurate differentiation between the architecture of multiplexers and encoders, with proper quantitative details – **2 Marks**
- **Case 2:** Mostly correct differentiation, with minor mistakes or incomplete quantitative details – **1.5 Marks**
- **Case 3:** Partial explanation of both multiplexers and encoders, but lacking depth or clarity – **1 Mark**
- **Case 4:** Partial explanation of only one of the devices, or explanation without quantification – **0.5 Marks**
- **Case 5:** No logical approach or incorrect explanation – **0 Marks**

**Answer 4**

You are incharge of a spaceship and need to send messages to other ships (buddy-ship) in your team without letting the enemy knowing your plans. Write a simple excess 5 code for numbers if you can only use 4 bits at a time.

**Subpart(a)**

Implement using half adders. **(4)**



$C_3$  can be discarded as we are guaranteed that the maximum encoded value cannot be greater than  $(2^4 - 1) \Rightarrow 15$

**A diagram which has only used Half Adders will also receive full marks.**

The input is of the form  $x_3x_2x_1x_0$ .  
The encoded output is in the form  $S_3S_2S_1S_0$ .

#### Marking Scheme

- **Full Marks:** Given to students who correctly solve the problem using half adders, or those who use OR gates in their solution alongside a clear explanation.
- **1 Mark:** Awarded if a full adder is directly used without explaining how to construct it using half adders, or if a half adder is incorrectly used with 3 inputs.
- **0 Marks:** Given if no circuit implementation is provided.
- **Partial Marks:** Granted based on the correctness and completeness of the provided solution.

#### Subpart(b)

Draw a parity generator schematic if you plan to use odd parity. (5)

Take the output of half adders which should be 3 bit(+1 parity which make total of 4 bits) or 4 bits. In this case let us take 4 bit:  $abcd$  (this should be the output of half adders), then the parity bit generated is  $Y$  which is 1 when  $abcd$  have odd number of ones else 0.

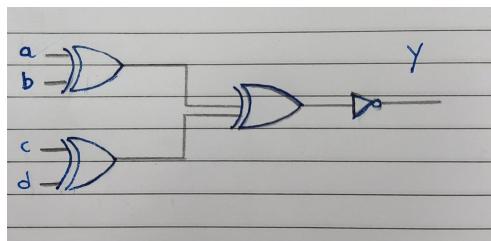


Figure 11: Parity Generator Circuit

**Marking Scheme** Explanation +/ Truth Table :- 1-2 marks  
Diagram + Formula :- 3-4 marks  
Partial marks given based on how close is your solution.

Alternative approach - using kmaps or half adders is also accepted but simplified expression/diagram is expected.

### **Subpart(c)**

How can your buddy-ship check if there has been any message interruption/corruption.  
**(1)**

Given the message, the buddy-ship can use a 5 bit-odd parity checker to detect whether the parity is odd or even. Depending on the output of the parity checker, we can know whether the message has been corrupted.

#### **Marking Scheme**

- **Full Marks:** Awarded if the term "parity checker" or its equivalent explanation (checking parity using XOR gates) is mentioned in the solution.
- **Partial Marks:** Given if "parity checker" or its equivalent explanation is not mentioned, based on the correctness and completeness of the rest of the solution.