

# MOS Operating Regions

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graph TD; A[MOS Operating Regions] --> B[Above Threshold<br/>(V<sub>GS</sub> > V<sub>TN</sub>)]; A --> C[Subthreshold<br/>(V<sub>GS</sub> < V<sub>TN</sub>)]; B --> D[Saturation<br/>(V<sub>DS</sub> > V<sub>DSAT</sub>)]; B --> E[Triode<br/>(V<sub>DS</sub> < V<sub>DSAT</sub>)];
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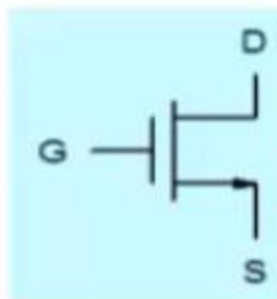
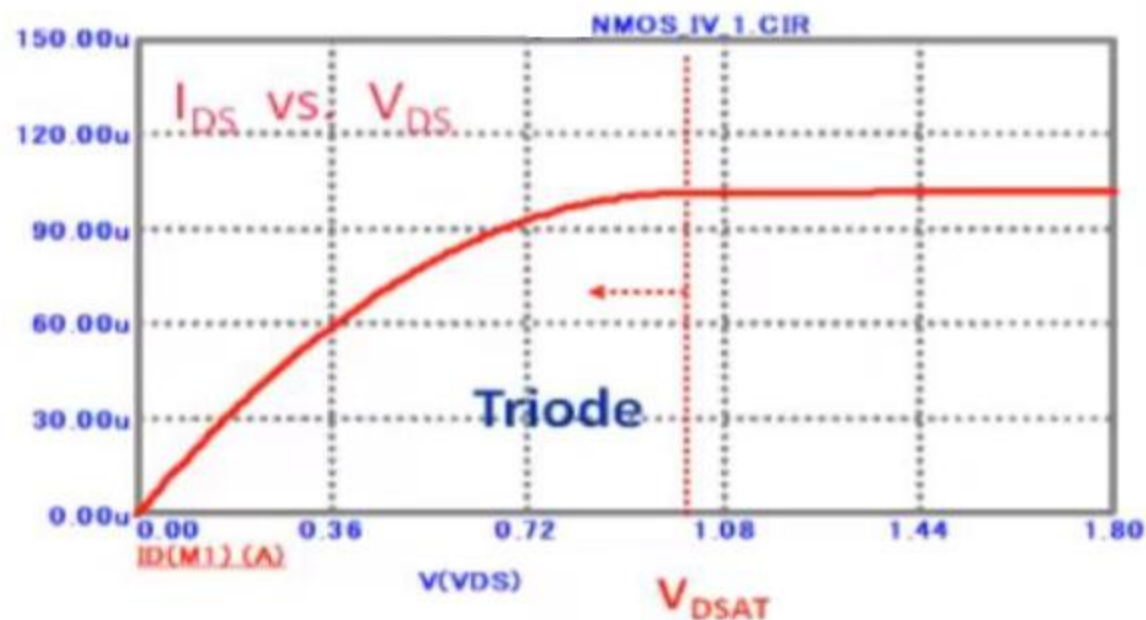
**Above Threshold**  
 $(V_{GS} > V_{TN})$

**Subthreshold**  
 $(V_{GS} < V_{TN})$

**Saturation**  
 $(V_{DS} > V_{DSAT})$

**Triode**  
 $(V_{DS} < V_{DSAT})$

## dc Model: Triode (or Linear)



$$V_{GS} > V_{TN}$$

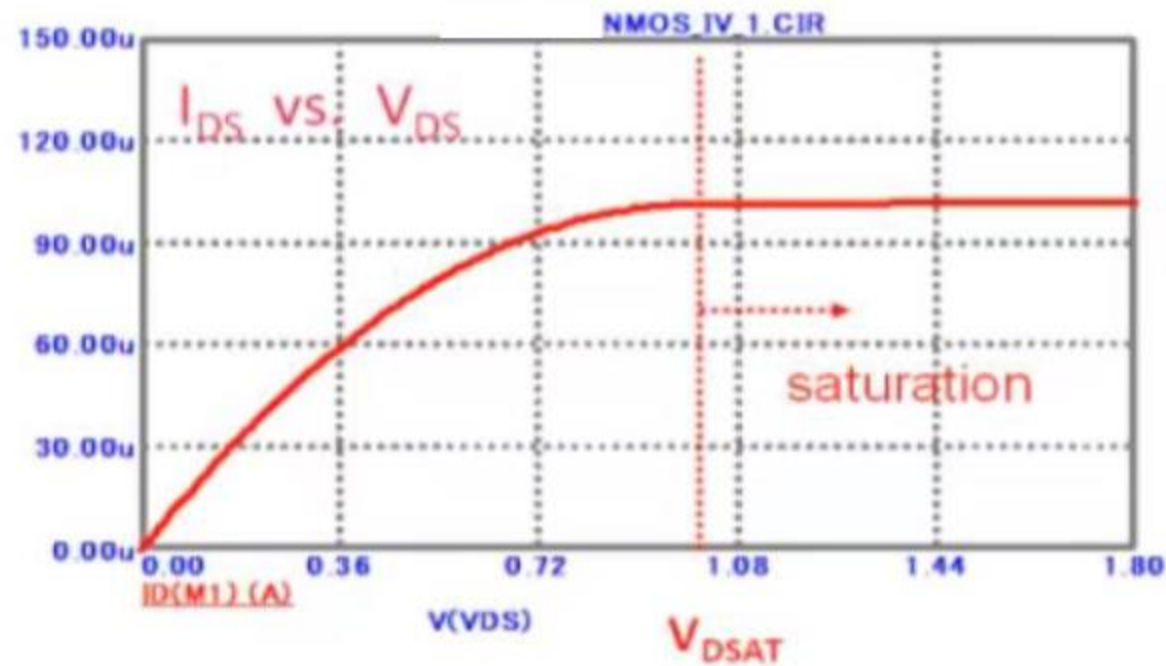
$$V_{DS} < V_{Dsat} = V_{GS} - V_{TN}$$

$$I_{DS} = \beta_N \left\{ (V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right\}$$

$$\beta_N = kP_N \cdot \frac{W}{L}$$

$$kP_N = \mu_n C_{ox'} : (\text{TransConductance parameter } \frac{\mu A}{V^2})$$

## DC Model: Saturation Region



$$V_{GS} > V_{THN}$$

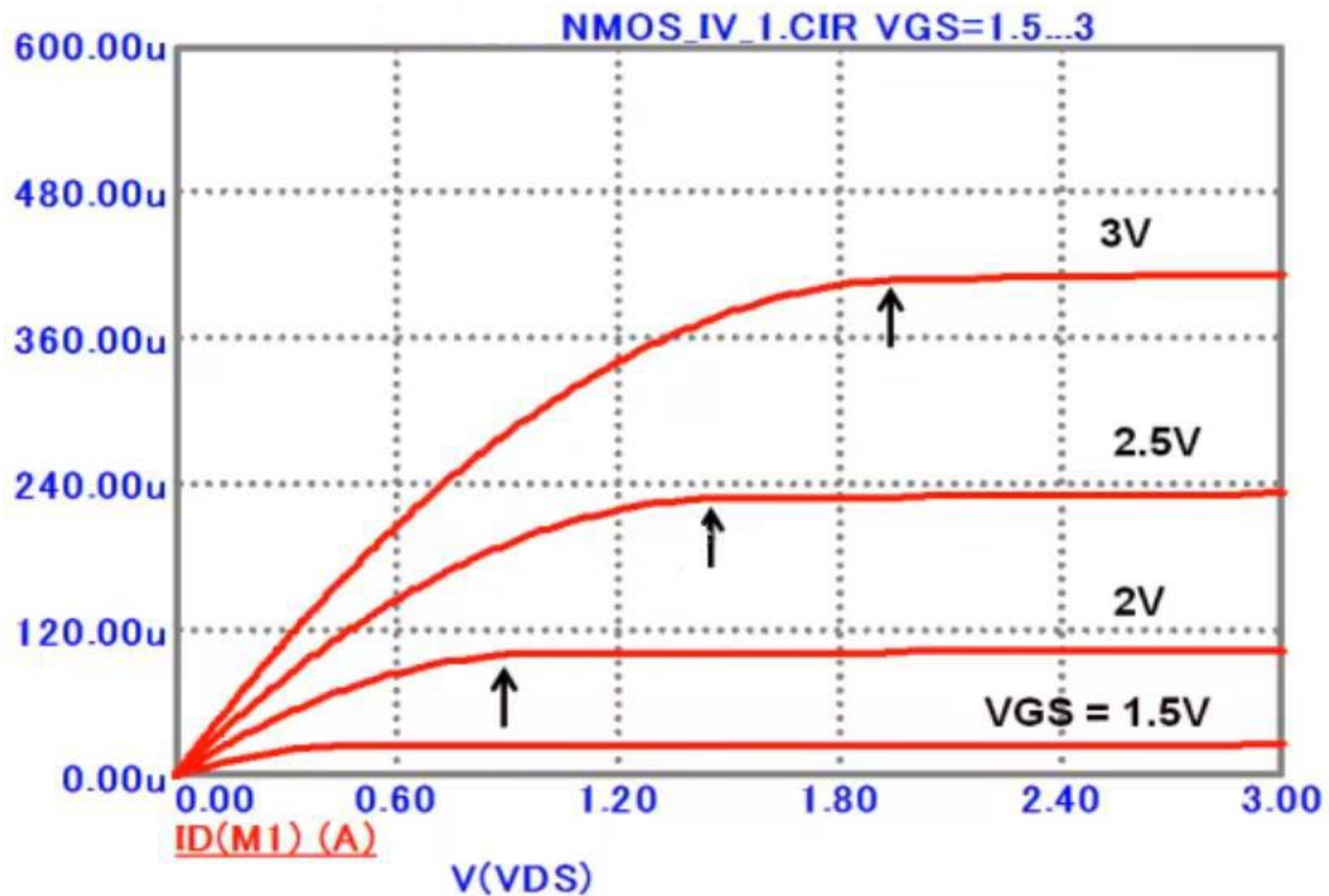
$$V_{DS} \geq V_{GS} - V_{THN}$$

$$I_{DS} = \frac{\beta_N}{2} (V_{GS} - V_{THN})^2 [1 + \lambda_n V_{DS}]$$

$\lambda_N$  is the channel length modulation parameter

Note that unlike BJT,  $V_{DSAT}$  is not only larger but also dependent on applied gate-source voltage

# Output Characteristics of MOSFET



## dc model parameters

$$\text{Linear : } I_{DS} = \beta_N \left\{ (V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right\} \quad \beta_N = kP_N \cdot \frac{W}{L}$$

$$\text{Saturation : } I_{DS} = \frac{\beta_N}{2} (V_{GS} - V_{THN})^2 [1 + \lambda_n V_{DS}] \quad \lambda_N$$

$$V_{THN} = V_{THN0} + \gamma (\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$$

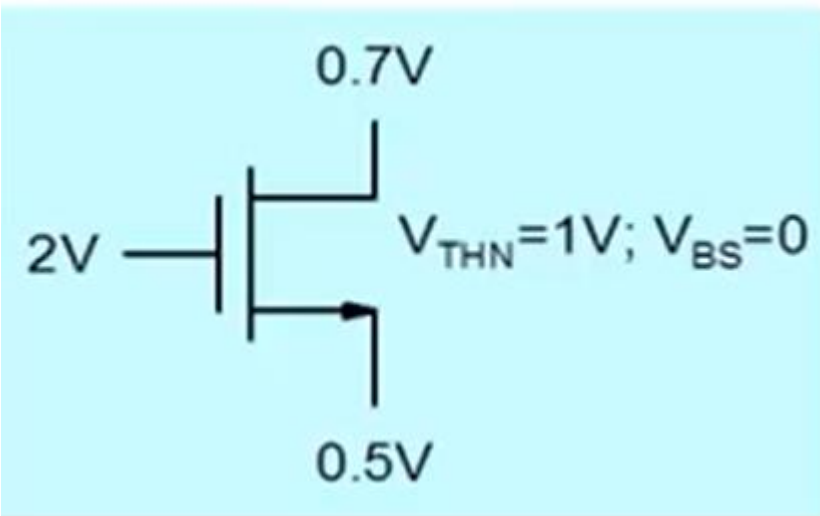
$$V_{THN0} = 1V; \gamma = 0.7 V^{1/2}; 2\phi_F = 0.7V;$$

$$KP_N = 100 \mu A / V^2; L = 1 \mu m; \lambda = 0.01 V^{-1}$$

L is usually fixed, W is determined by designer



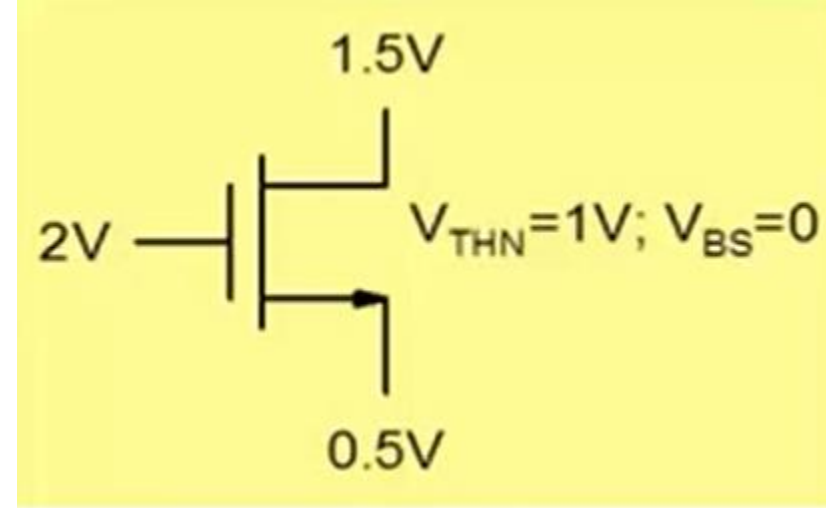
Which mode is the transistor operating in ?



$$V_{GS} = 1.5 ; V_{DS} = 0.2$$

$$V_{DSAT} = V_{GS} - V_{THN} = 0.5$$

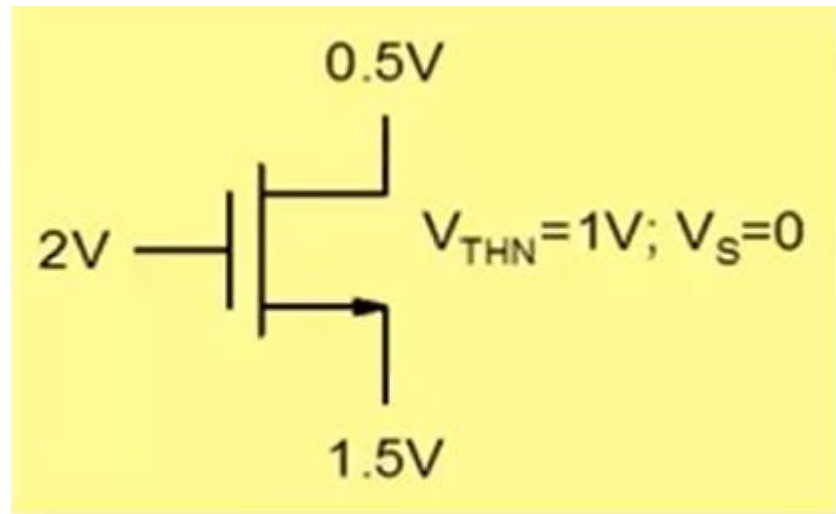
$$V_{DS} < V_{DSAT} \Rightarrow \text{Linear}$$



$$V_{DSAT} = 0.5 ; V_{DS} = 1V$$

Saturation

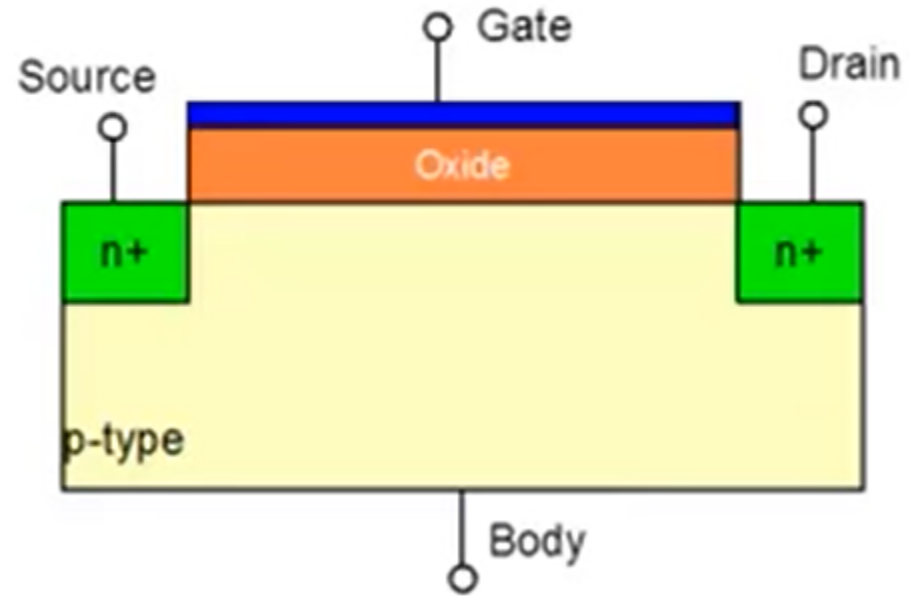
Which mode is the transistor operating in ?



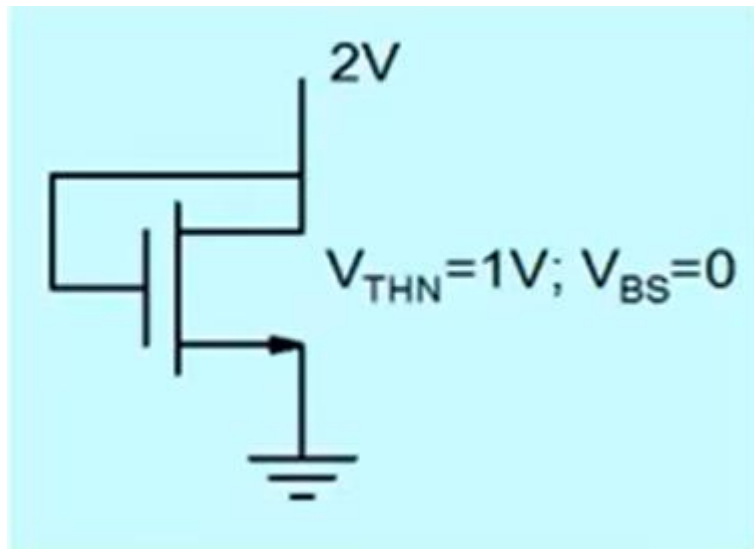
$$V_{GS} = 0.5 ; V_{DS} = -1V$$

$$V_{DSAT} = V_{GS} - V_{THN} = 0.5$$

$$V_{DS} > V_{DSAT} \Rightarrow \text{saturation}$$



$$V_{GS} = 1.5 ; V_{DS} = 1V$$



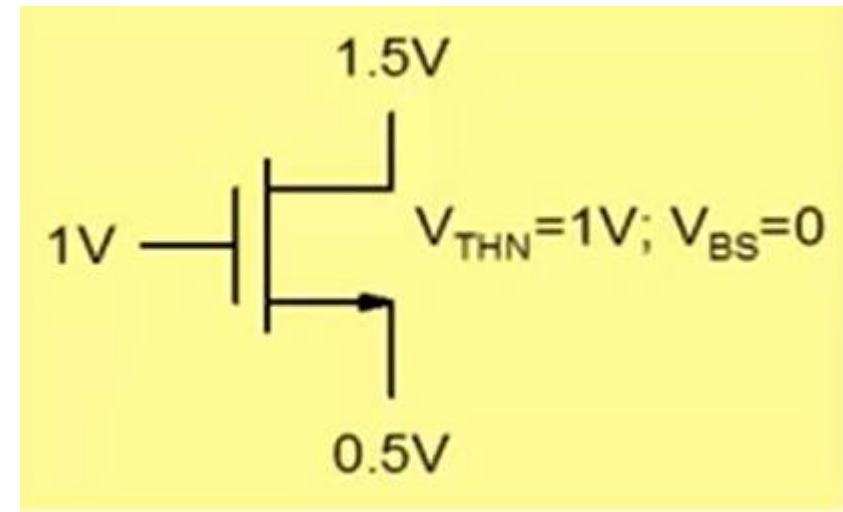
$$V_{GS} = 2; V_{DS} = 2$$

Saturation

$$I_{DS} = \frac{\beta_N}{2} (V_{GS} - V_{THN})^2 [1 + \lambda_n V_{DS}]$$

$$I_X \cong \frac{\beta_N}{2} (V_X - V_{THN})^2$$

Diode with a turn-on voltage of  $V_{THN}$



$$V_{GS} = 0.5V < V_{THN}$$

Transistor is in sub-threshold mode of operation

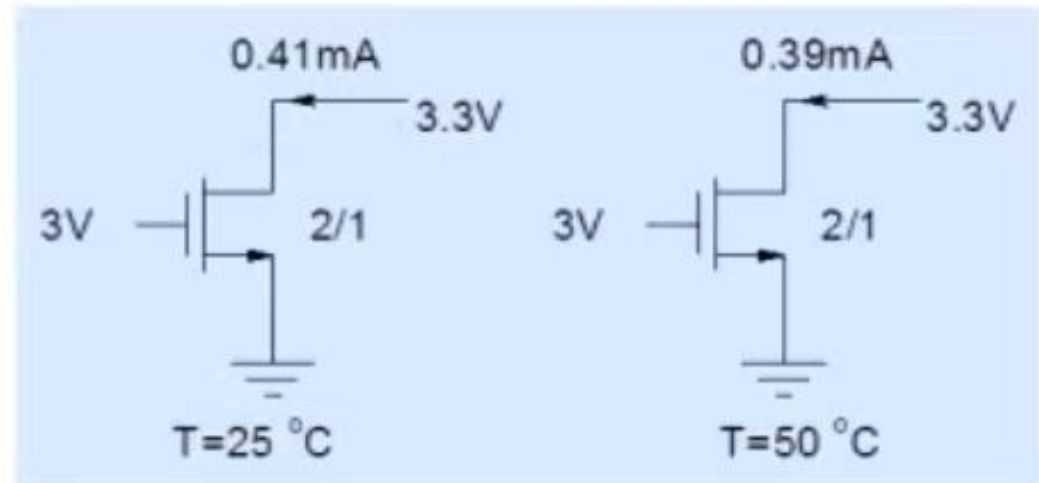
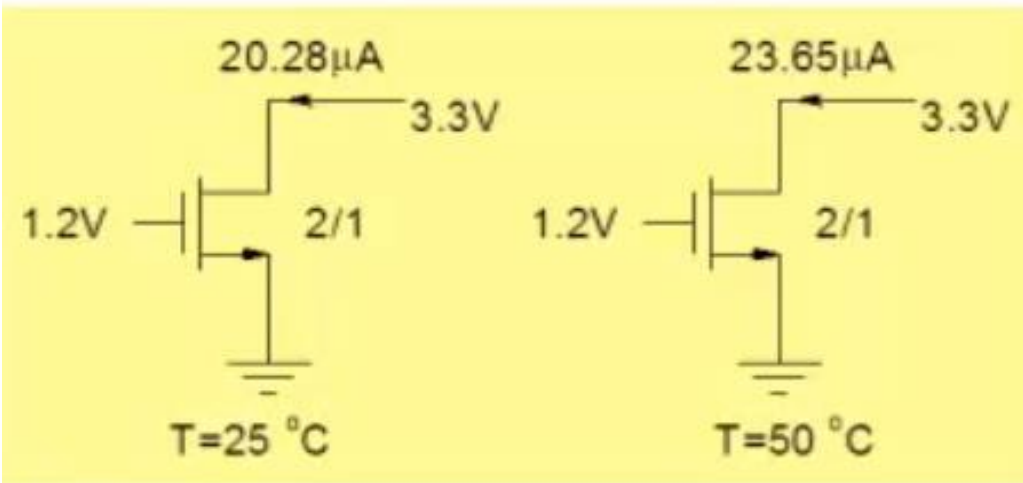


## Temperature dependence

$$I_{DS} = \frac{KP_N}{2} \times \frac{W}{L} \times (V_{GS} - V_{THN})^2$$

Increase in temperature causes both transconductance parameter  $KP_N$  and threshold voltage  $V_{THN}$  to decrease

Although both  $K_{PN}$  and  $V_{THN}$  decrease with temperature, the former causes a decrease in current while the latter causes an increase in current.



# MOS Operating Regions

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graph TD; A[MOS Operating Regions] --> B[Above Threshold  
(VGS > VTN)]; A --> C[Subthreshold  
(VGS < VTN)]; B --> D[Saturation  
(VDS > VDSAT)]; B --> E[Triode  
(VDS < VDSAT)];
```

**Above Threshold**  
( $V_{GS} > V_{TN}$ )

**Subthreshold**  
( $V_{GS} < V_{TN}$ )

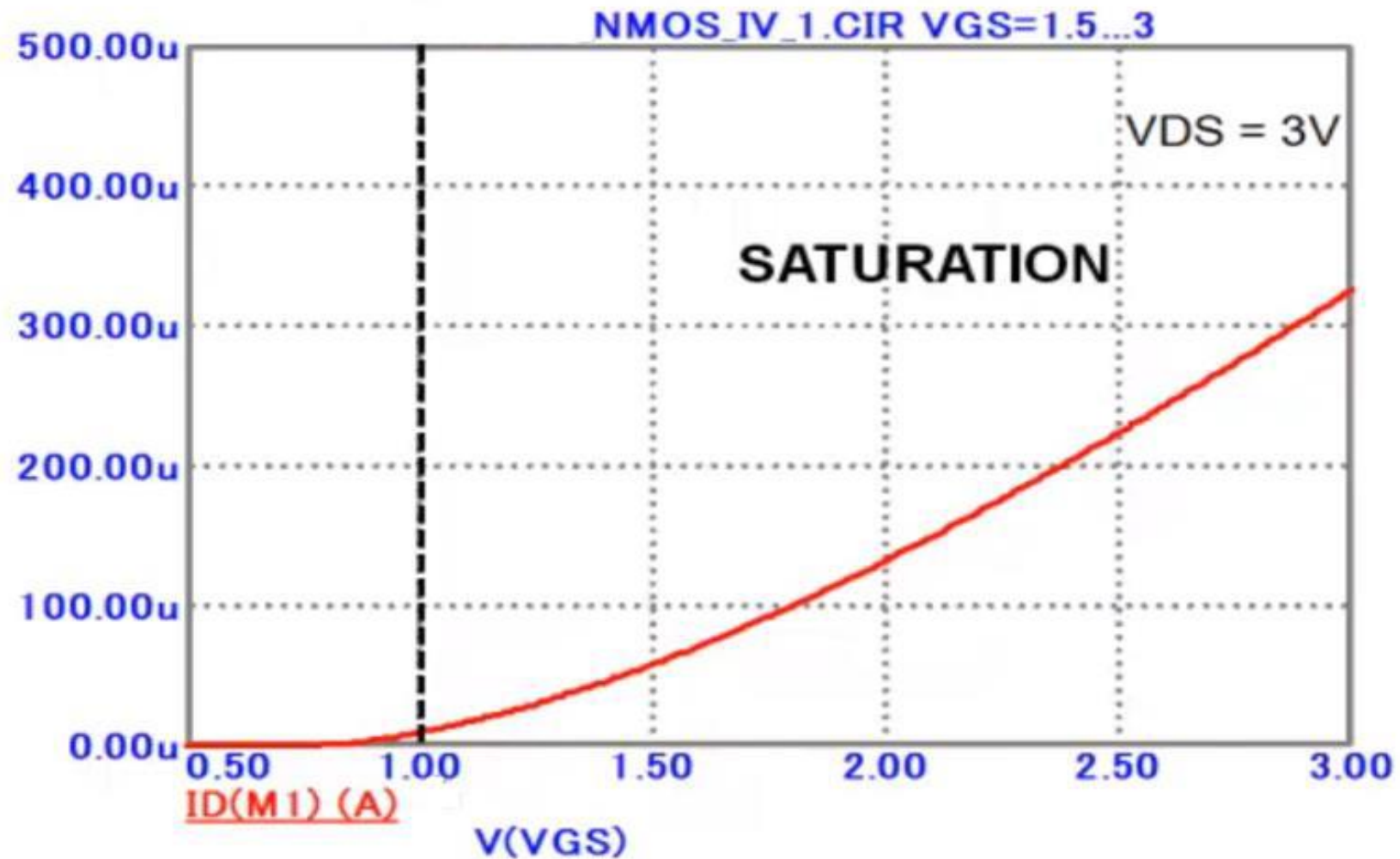
**Saturation**

( $V_{DS} > V_{DSAT}$ )

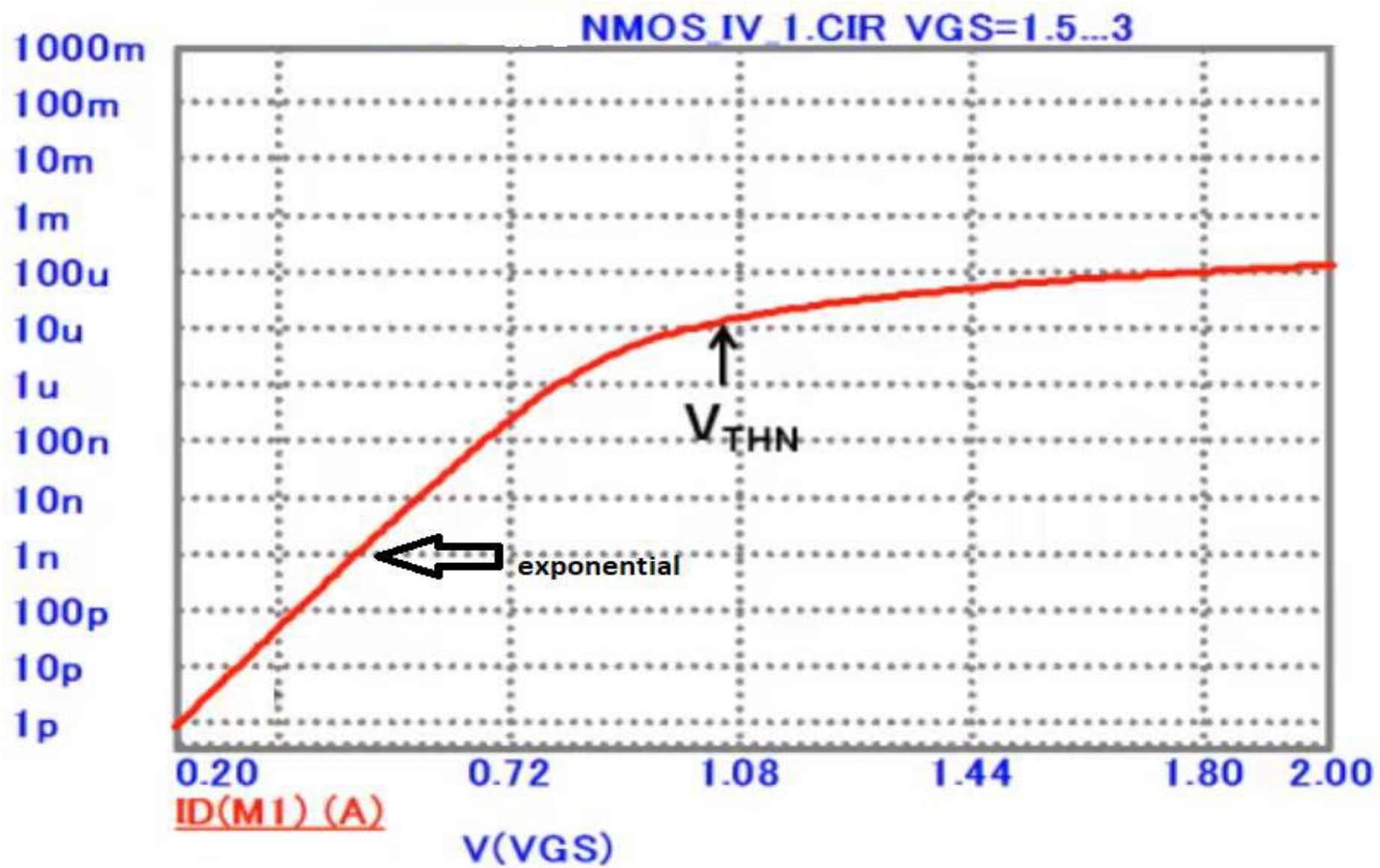
**Triode**

( $V_{DS} < V_{DSAT}$ )

## Transfer characteristics of NMOS



Current is very small until gate-source voltage **exceeds threshold voltage**  
 $V_{THN}$



- Logscale
- Ignoring leakages



$$I_D \propto e^{\frac{qV_{GS}}{N'kT}} \qquad g_m = \frac{\partial I_{DS}}{\partial V_{gs}} = \frac{I_{DS}}{nV_T}$$

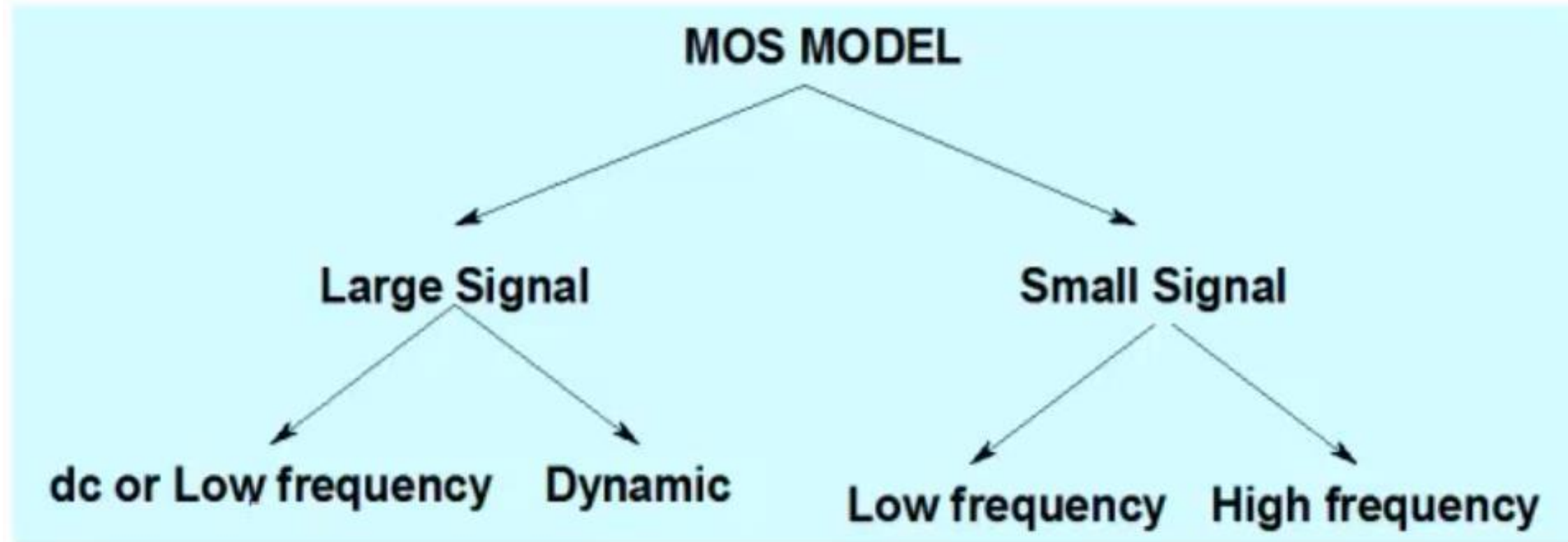
- In subthreshold region, MOS acts like a BJT

$$BJT: \qquad I_C = I_S e^{V_{BE}/V_T}$$

$$MOS: \quad I_{DS} = I_{S_1} e^{V_{GS}/\eta V_T}$$

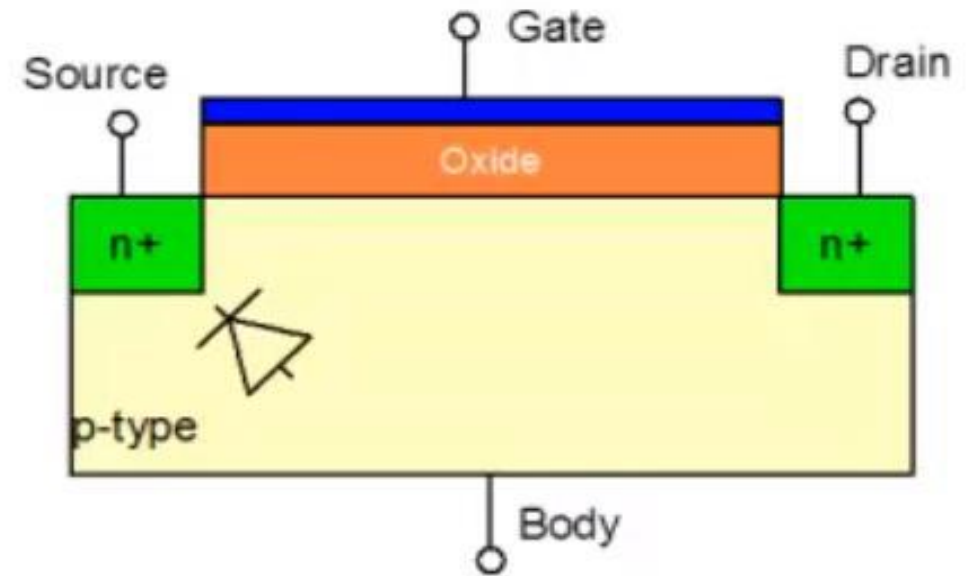
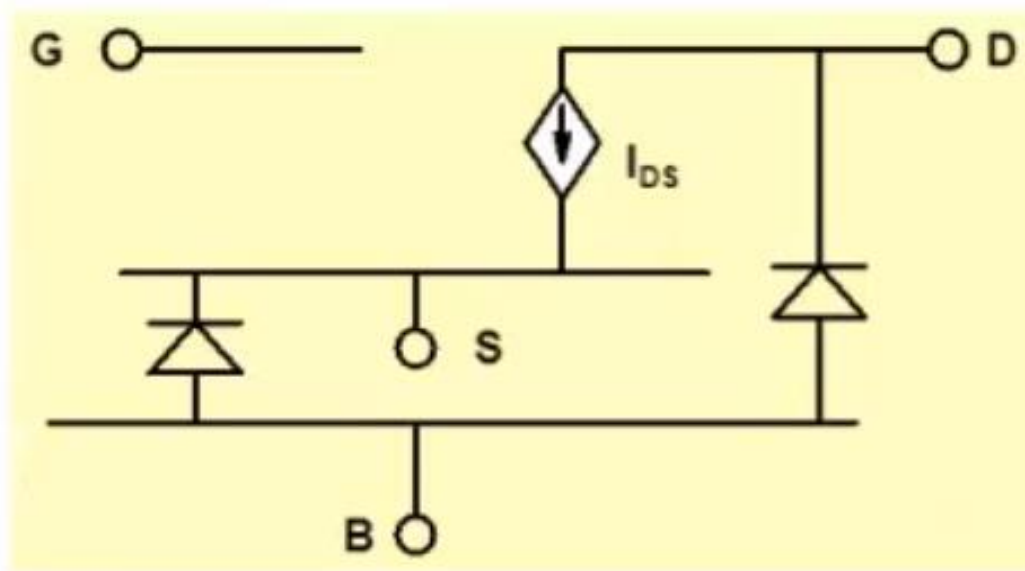
- The advantage of MOS is that it offers almost infinite input impedance. Its disadvantage is that current levels are low.

**MOS models :** The classification of models can be done on the basis of magnitude and frequency of applied voltages



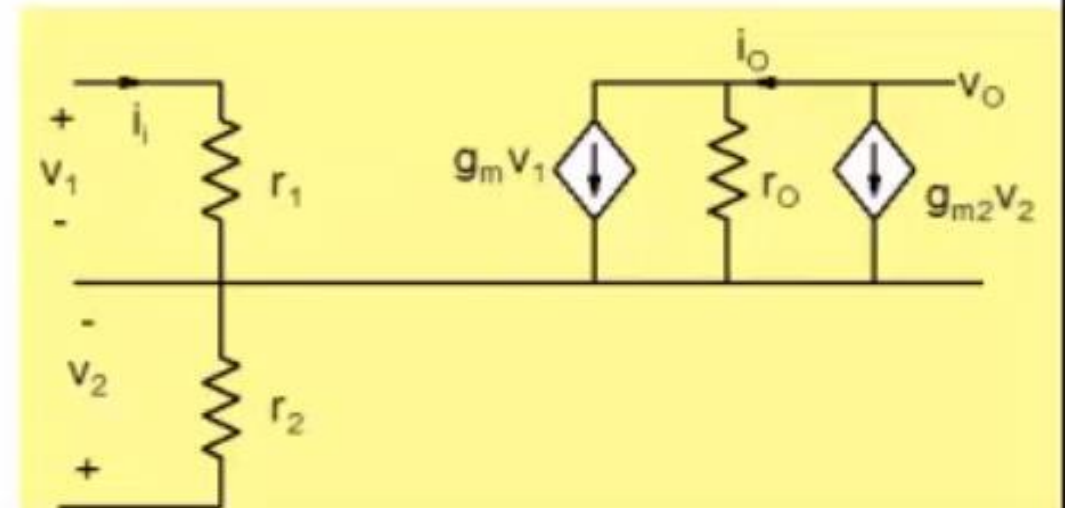
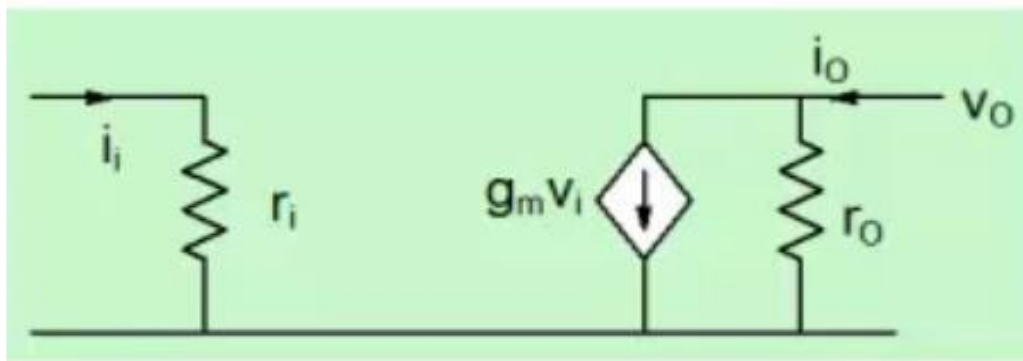
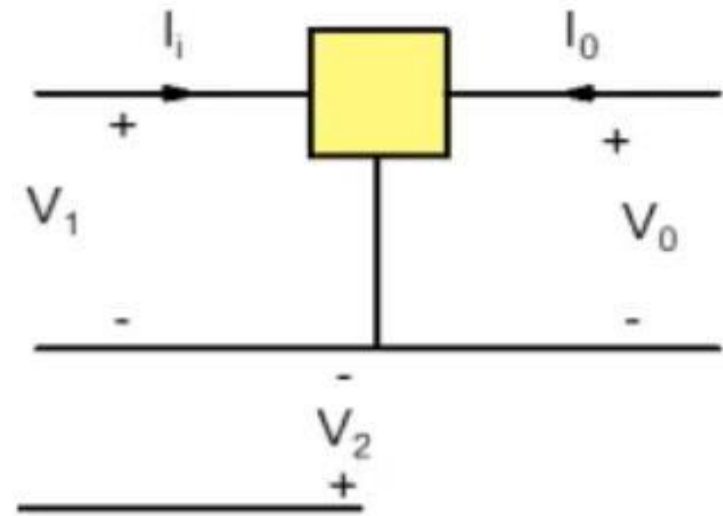
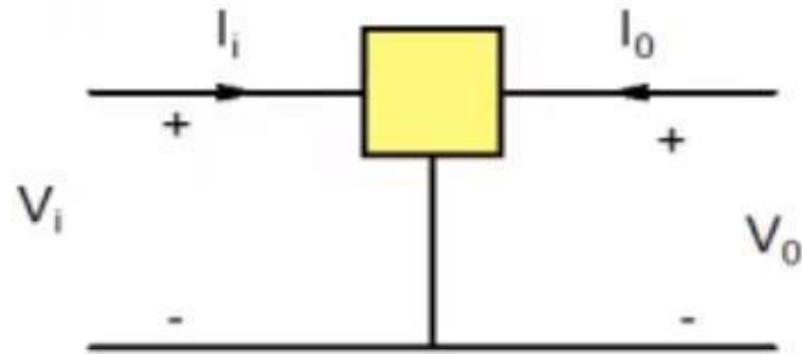


The dc model of the transistor in triode and saturation region can be represented in the form of an equivalent circuit:

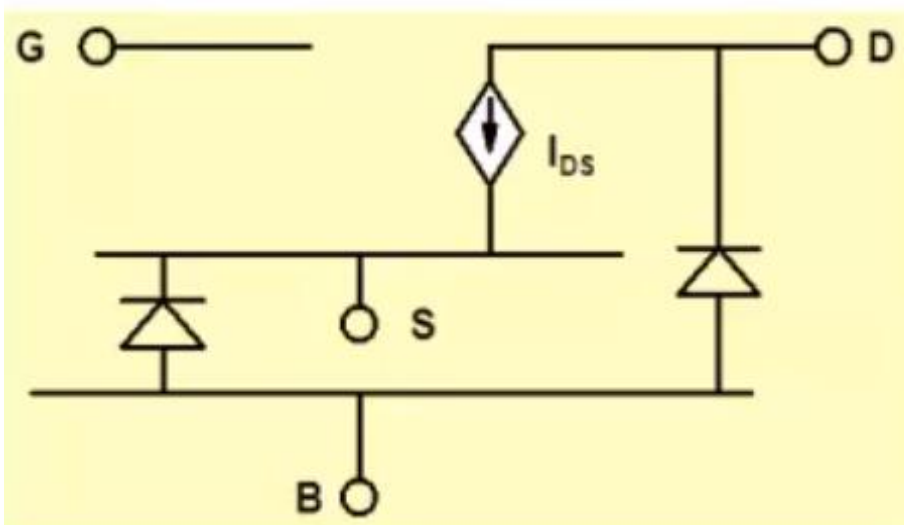


Series resistance associated with gate, source, drain and body terminals is not shown but can play an important role.

Complete **small signal model** (dc) for a 3-terminal unilateral device.



## Small Signal Model (dc/low frequency)



$$I_{ds} = \frac{\beta_N}{2} (V_{gs} - V_{THN})^2 (1 + \lambda_n V_{ds})$$

$$V_{gs} = V_{GSQ} + v_{gs}$$

$$V_{ds} = V_{DSQ} + v_{ds}$$

$$V_{sb} = V_{SBQ} + v_{sb}$$

$$I_{ds} = I_{DSQ} + i_{ds}$$

$$I_{DSQ} + i_{ds} = \frac{\beta_N}{2} \left[ V_{GSQ} + v_{gs} - V_{THN} (V_{BSQ} + v_{bs}) \right]^2 (1 + \lambda_n V_{DSQ} + \lambda_n v_{ds})$$

↑ not really multiplication, but function

$$i_{ds} \cong I_{DSQ} \left\{ \left( \lambda_n v_{ds} + \frac{2v_{gs}}{V_{GSQ} - V_{THN}} + \frac{\gamma \times v_{bs}}{(V_{GSQ} - V_{THN}) \times \sqrt{2\phi_F - V_{BSQ}}} \right) \right\}$$

$$i_{ds} = \frac{v_{ds}}{r_o} + g_m v_{gs} + g_{mb} v_{bs}$$

$$r_o = \frac{1}{\lambda_n I_{DSQ}}$$

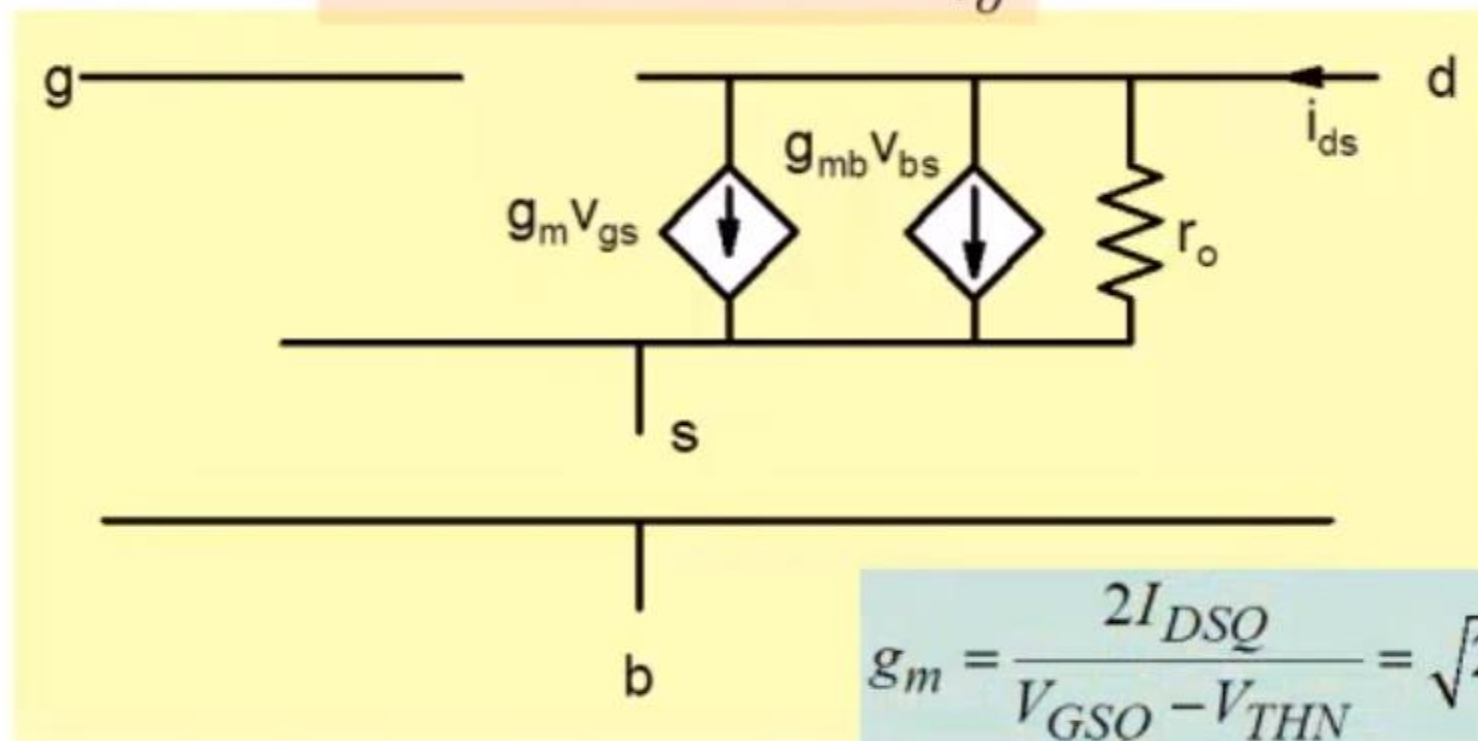
$$g_m = \frac{2I_{DSQ}}{V_{GSQ} - V_{THN}} = \sqrt{2I_{DSQ}\beta}$$

$$g_{mb} = g_m \cdot \eta$$

$$\eta = \frac{\gamma}{2\sqrt{2\phi_F + V_{SBQ}}}$$

## Low frequency Small Signal model

$$i_{ds} = g_m v_{gs} + g_{mb} v_{bs} + \frac{v_{ds}}{r_o}$$



$$g_m = \frac{2I_{DSQ}}{V_{GSQ} - V_{THN}} = \sqrt{2I_{DSQ}\beta}$$

$$r_o = \frac{1}{\lambda_n I_{DSQ}}$$

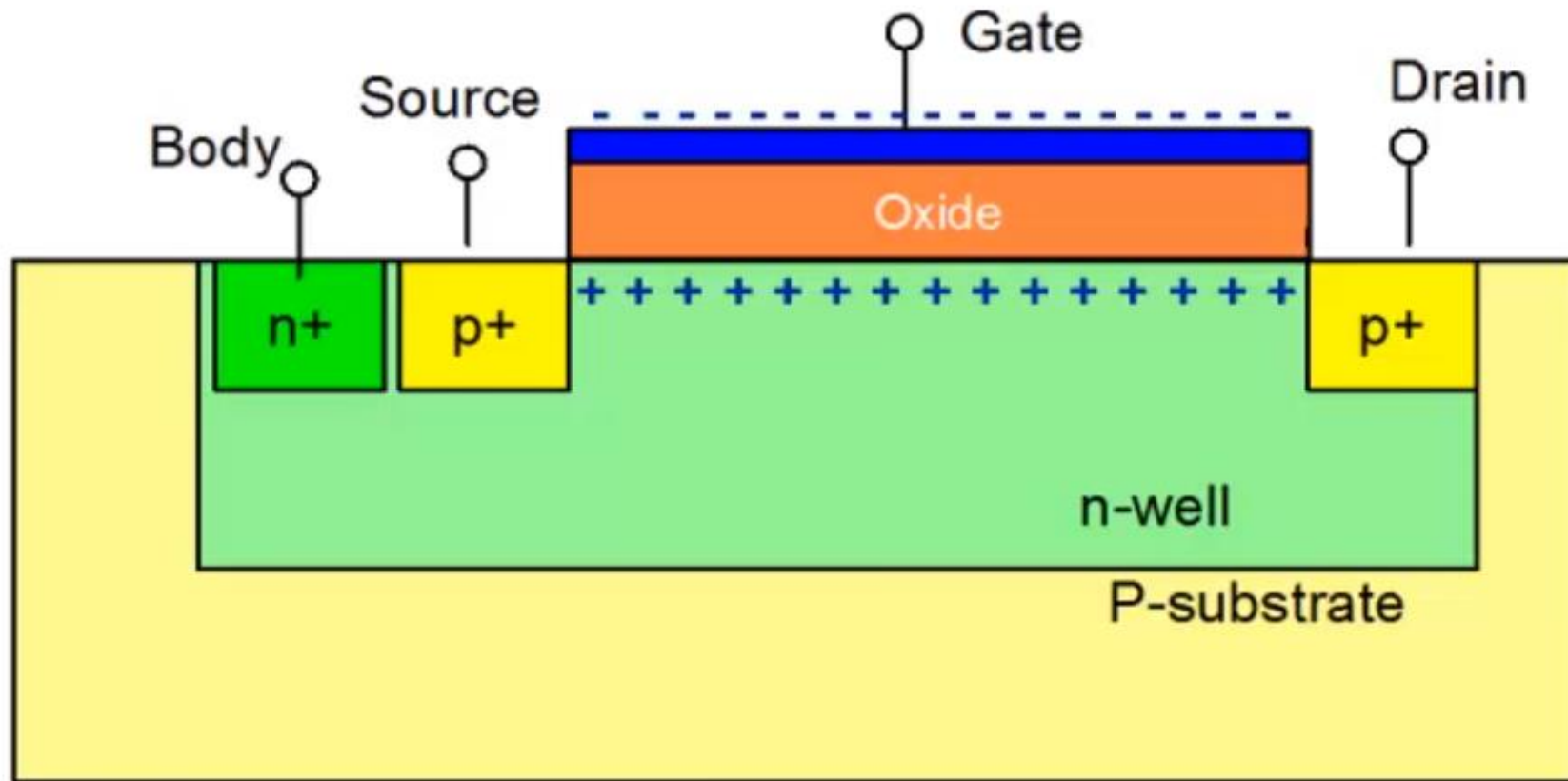
$$g_{mb} = g_m \cdot \eta$$

$$\eta = \frac{\gamma}{2\sqrt{2\Phi_F + V_{SBQ}}}$$

The small signal approximation  $i_{ds} = g_m v_{gs}$  is accurate when  $v_{gs} \ll 2(V_{GS} - V_{THN})$

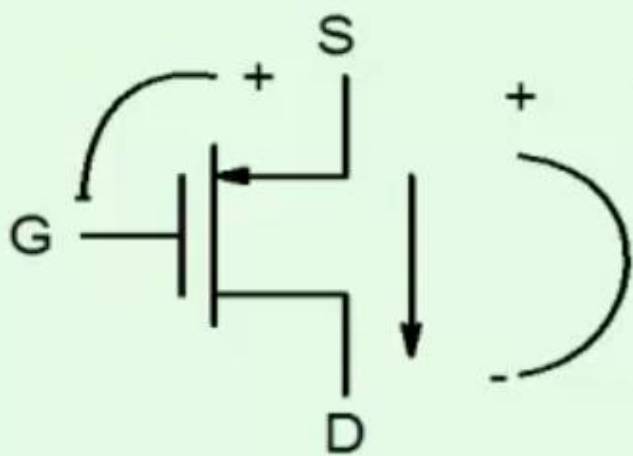
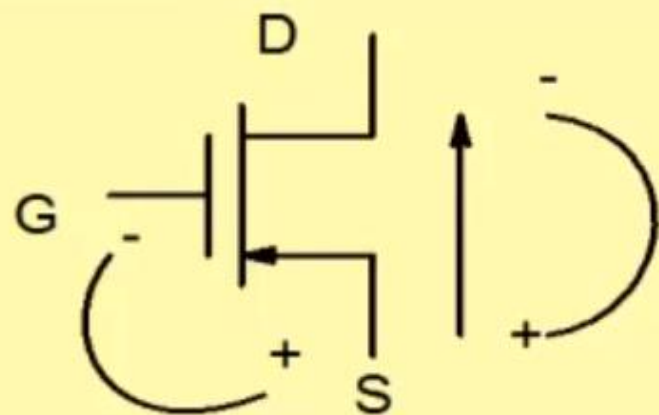
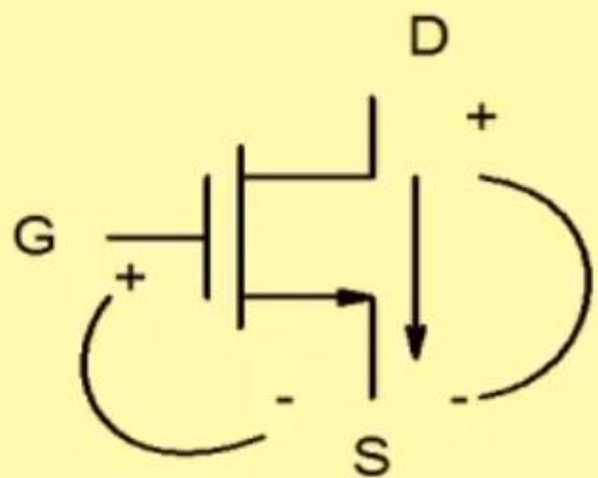


# PMOS



$V_{GS}$  is negative ; Threshold voltage  $V_{TP}$  is negative

$V_{DS}$  is negative ;  $I_{DS}$  is negative



$$V_{GSN} \rightarrow V_{SGP}$$

$$I_{DSN} \rightarrow I_{SDP}$$

$$V_{DSN} \rightarrow V_{SDP}$$

## Transformations

$$V_{GSN} \rightarrow V_{SGP}$$

$$V_{DSN} \rightarrow V_{SDP}$$

$$V_{BSN} \rightarrow V_{SBP}$$

$$V_{THN} \rightarrow -V_{THP}$$

$$I_{DSN} \rightarrow I_{SDP}$$

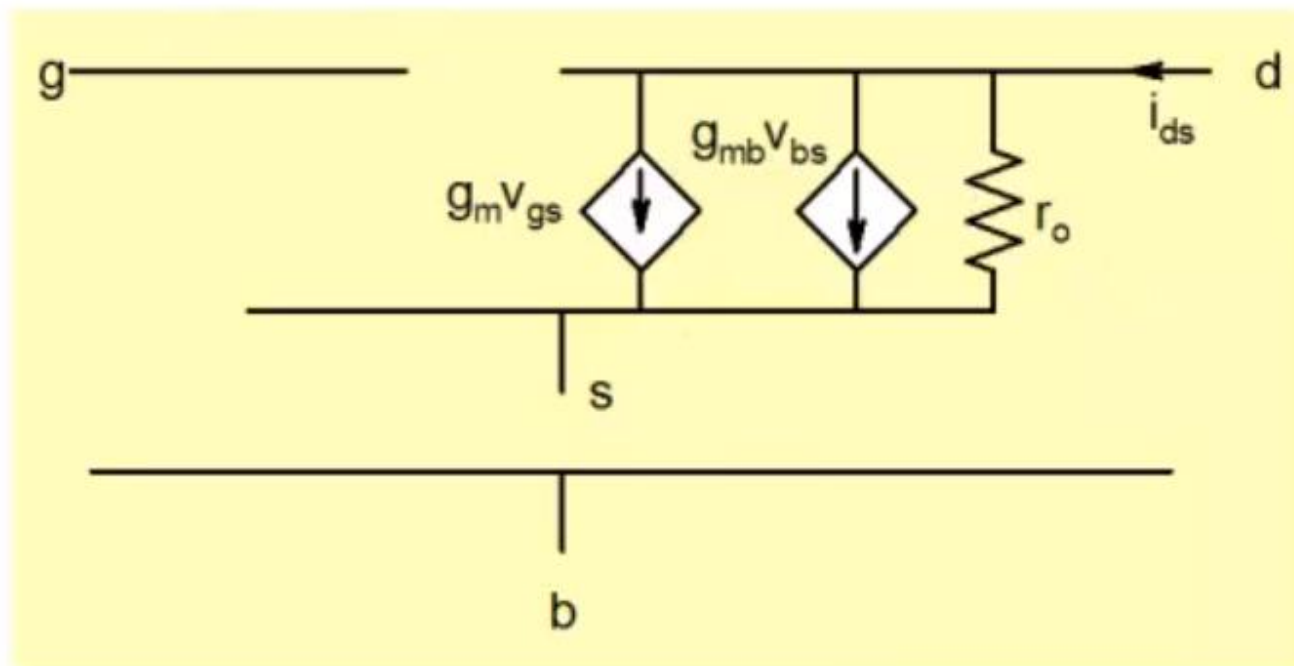
$$I_{DS} = \frac{\beta_N}{2} (V_{GS} - V_{THN})^2 [1 + \lambda_n V_{DS}] \rightarrow$$

$$I_{SD} = \frac{\beta_P}{2} (V_{SG} + V_{THP})^2 [1 + \lambda_p V_{SD}]$$

$$i_{sd} = g_m v_{sg} + g_{mb} v_{sb} + \frac{v_{sd}}{r_o}$$

$$i_{ds} = g_m v_{gs} + g_{mb} v_{bs} + \frac{v_{ds}}{r_o} \text{ same as NMOS}$$

## Small Signal Model



$$g_m = \frac{2I_{SDQ}}{V_{SGQ} + V_{THP}}$$

$$r_o = \frac{1}{\lambda_p I_{SDQ}}$$