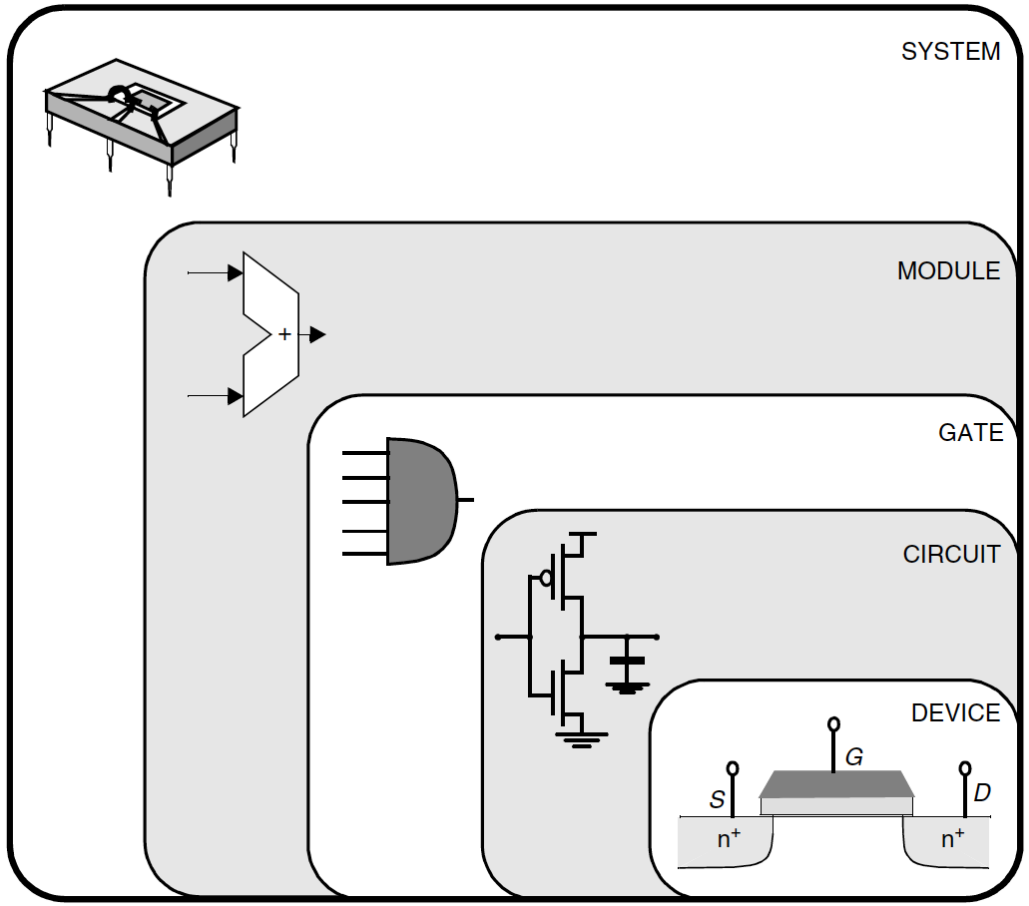
Fundamentals of Electronics

ECE 101

System Level Electronics

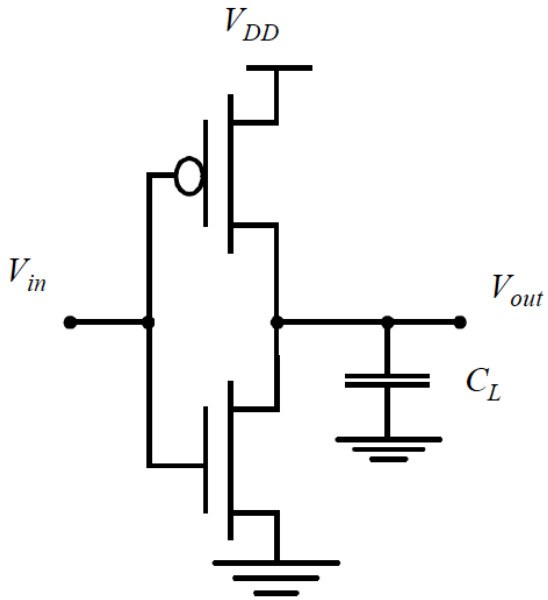
Abstraction

Design abstraction in digital electronics

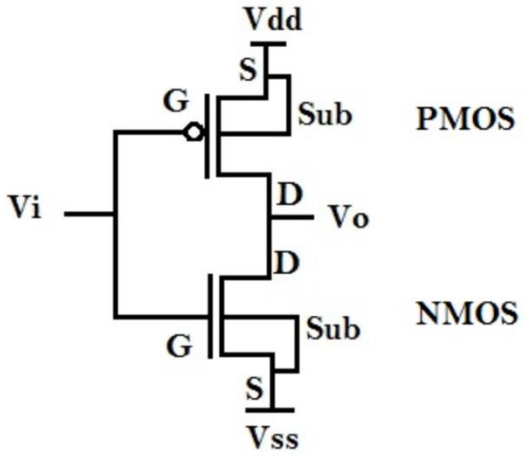


Digital Integrated Circuits by Rabaey et. al.

Logic gate implementation – CMOS Inverter

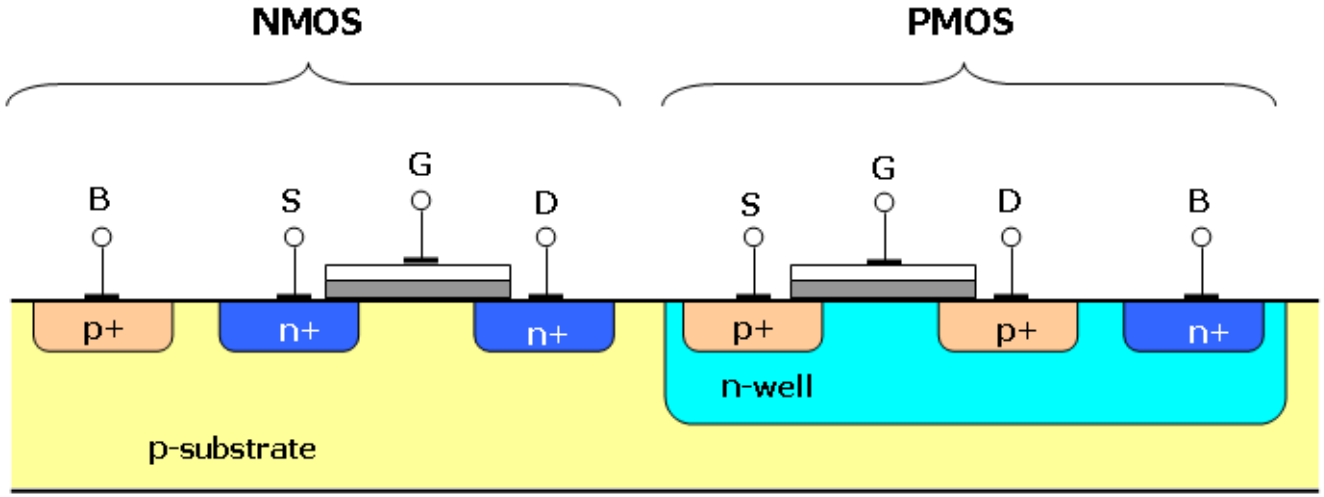


CMOS Inverter



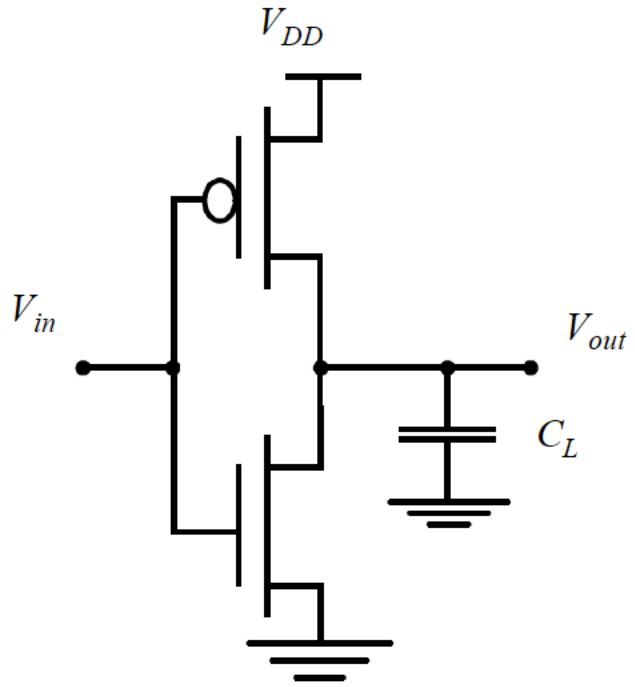
G = Gate Terminal
S = Source Terminal
D = Drain Terminal
Sub = Substrate Terminal

CMOS Technology



Input	Output
1	0
0	1

CMOS Inverter



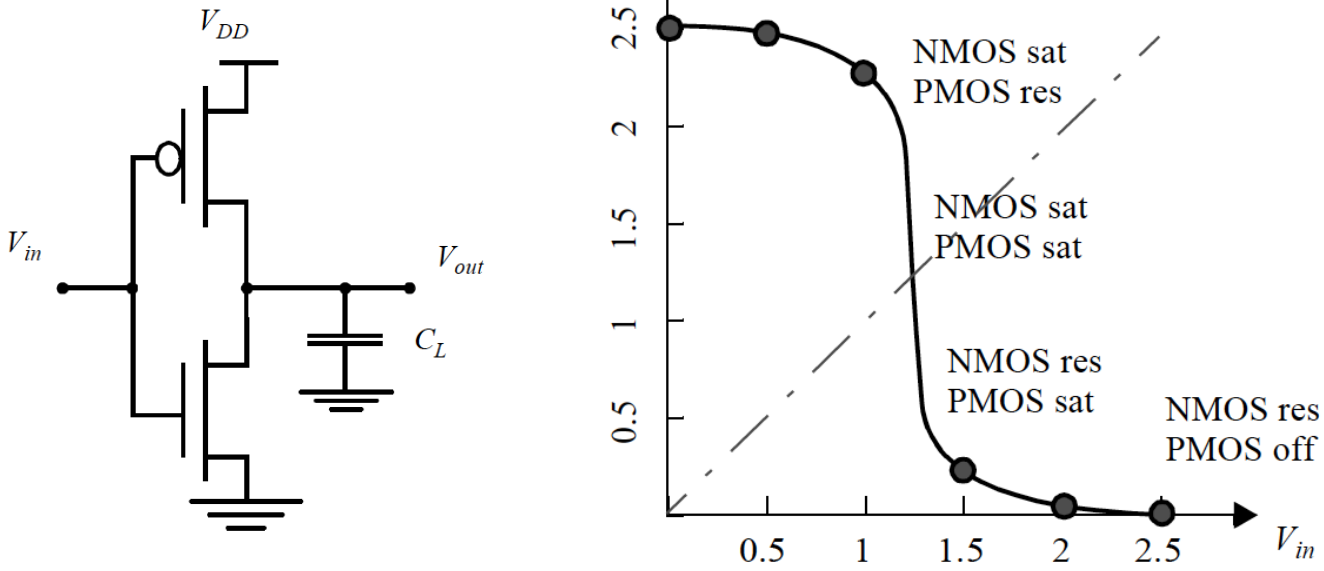
CMOS Inverter

Pull Up

Pull Down

- Cost
- Static behavior
- Dynamic behavior/performance
- Energy efficiency

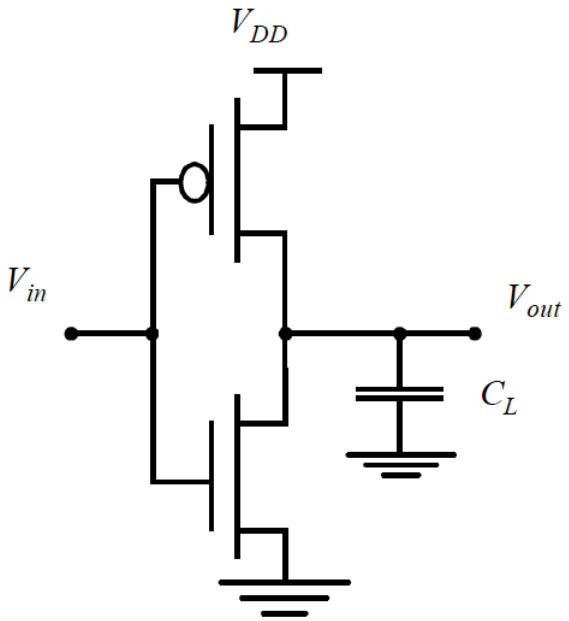
CMOS Inverter – Static behavior

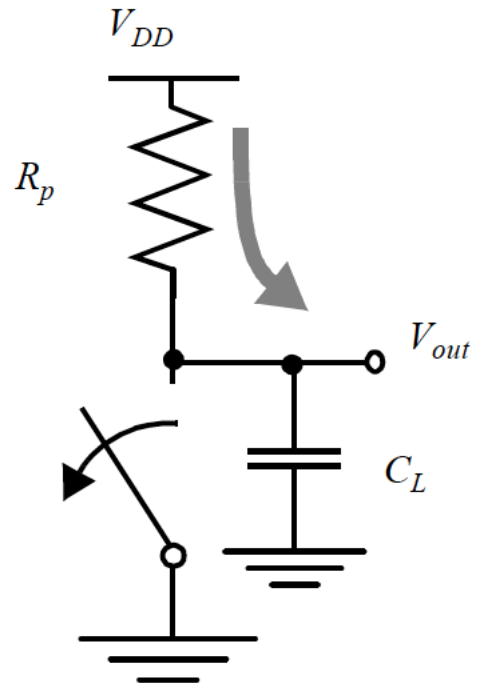


CMOS Inverter

- The high and low output levels equal VDD and GND, respectively; in other words, the voltage swing is equal to the supply voltage. This results in high noise margins.
- In steady state, there always exists a path with finite resistance between the output and either VDD or GND.
- A well-designed CMOS inverter, therefore, has a low output impedance, which makes it less sensitive to noise and disturbances. Typical values of the output resistance are in k-ohm range.
- The input resistance of the CMOS inverter is extremely high, as the gate of an MOS transistor is a virtually perfect insulator and draws no dc input current
- No direct path exists between the supply and ground rails under steady-state operating conditions (this is, when the input and outputs remain constant). The absence of current flow (ignoring leakage currents) means that the gate does not consume any static power.

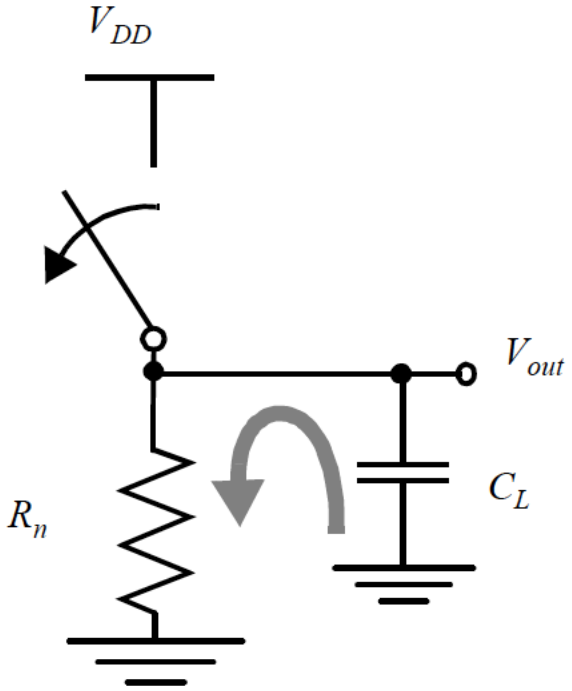
CMOS Inverter – Switching behavior





$V_{in} = 0$

(a) Low-to-high

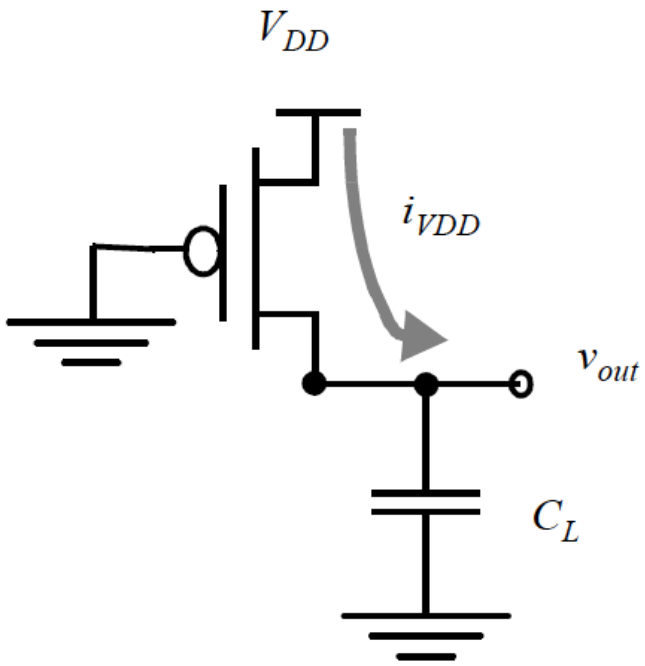


$V_{in} = V_{DD}$

(b) High-to-low

Getting C_L as small as possible is important for realizing fast switches

CMOS Inverter – Power Consumption



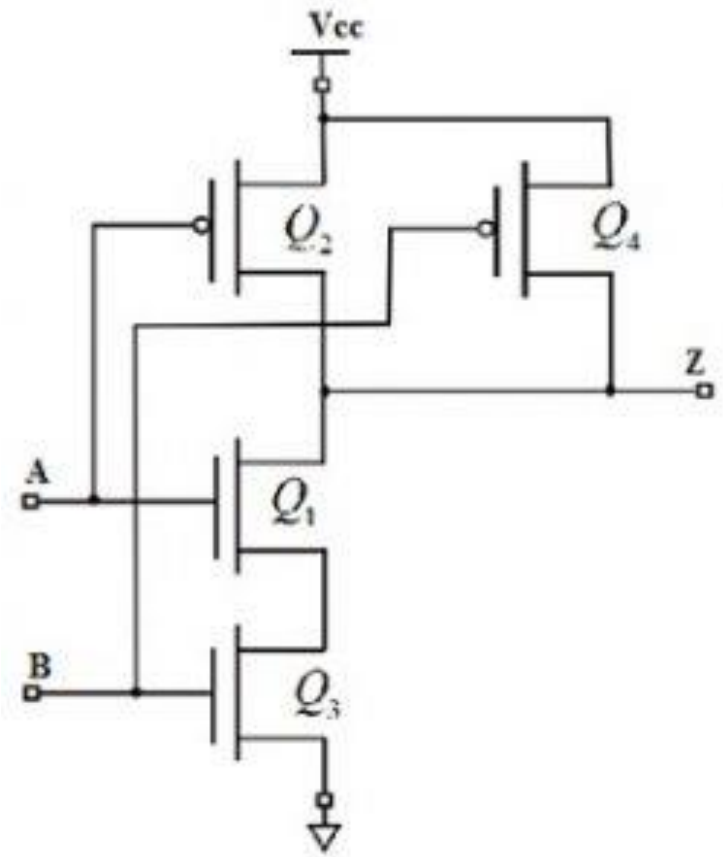
Equivalent circuit during the low-to-high transition.

- Each time the capacitor CL gets charged through the PMOS transistor, its voltage rises from 0 to VDD, and a certain amount of energy is drawn from the power supply.
- Part of this energy is dissipated in the PMOS device, while the remainder is stored on the load capacitor.
- During the high-to-low transition, this capacitor is discharged, and the stored energy is dissipated in the NMOS transistor
- The values of the energy EVDD, taken from the supply during the transition, as well as the energy EC, stored on the capacitor at the end of the transition,

$$E_{VDD} = \int_0^\infty i_{VDD}(t) V_{DD} dt = V_{DD} \int_0^\infty C_L \frac{dv_{out}}{dt} dt = C_L V_{DD} \int_0^{V_{DD}} dv_{out} = C_L V_{DD}^2$$

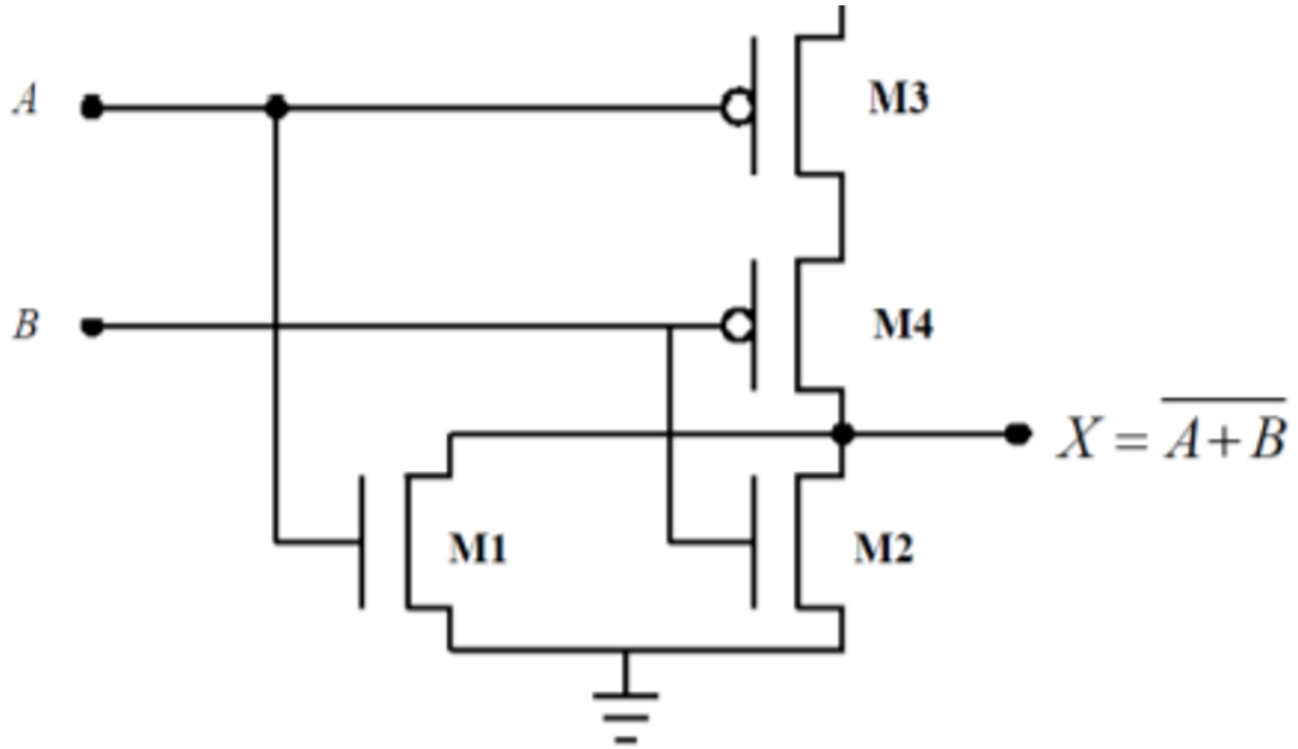
$$E_C = \int_0^\infty i_{VDD}(t) v_{out} dt = \int_0^\infty C_L \frac{dv_{out}}{dt} v_{out} dt = C_L \int_0^{V_{DD}} v_{out} dv_{out} = \frac{C_L V_{DD}^2}{2}$$

CMOS based NAND Gate



Input		Output
A	B	Y= $\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

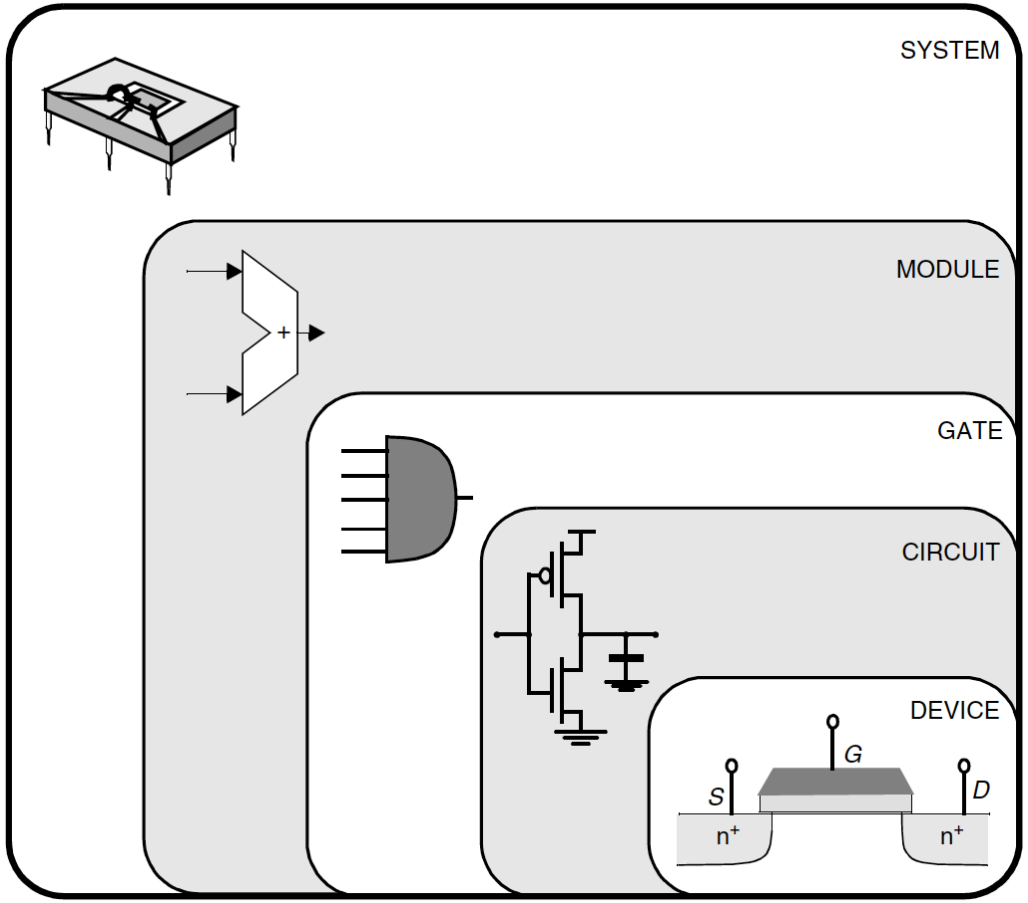
CMOS based NOR Gate



Input		Output
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

System Level Electronics

Abstraction



Digital Integrated Circuits by Rabaey et al

Operational Amplifier

- An Operational Amplifier (Op-Amp) is an integrated circuit that uses external voltage to amplify the input with a very high gain.

- The term “operational” was used as a descriptor early-on because this form of amplifier can perform operations of
  - Adding signals
  - Subtracting signals
  - Integrating signals

- The applications of Op-Amps have grown beyond those listed above.

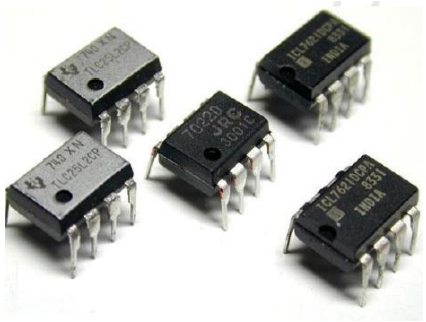
- Therefore, Op-Amp is an active circuit element designated to perform mathematical operations of addition, subtraction, multiplication, division, differentiation and integration.

- Examples:
  - LM 111
  - LM 324
  - LM 741

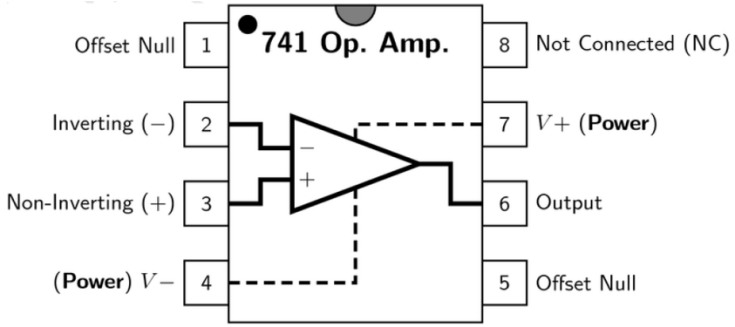
LM stands for linear monolithic.

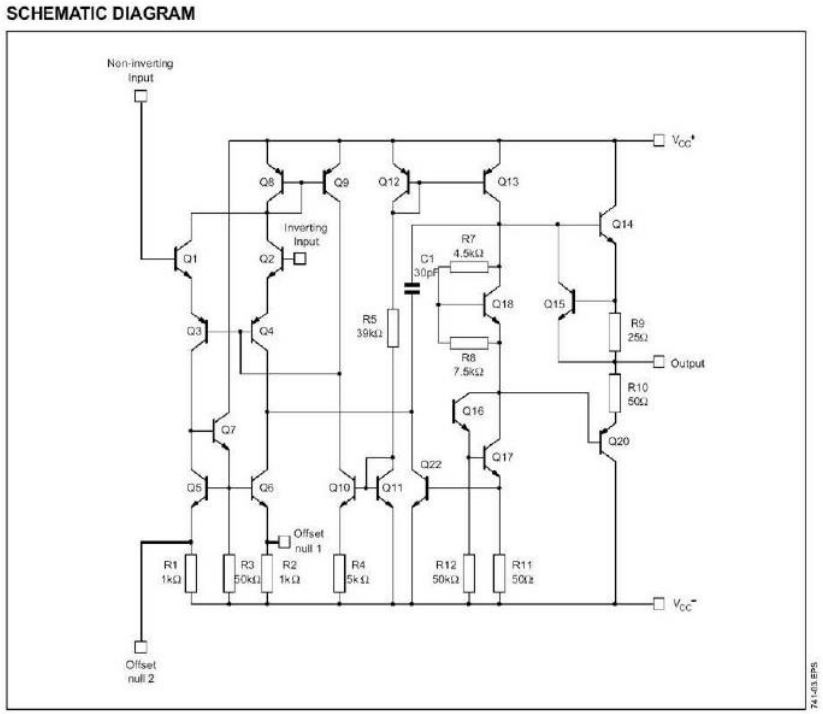
LM 741

- One of the most commonly used Op-Amp.



- Packaged device look like:

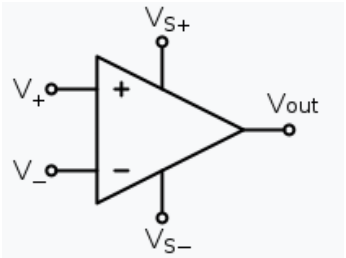


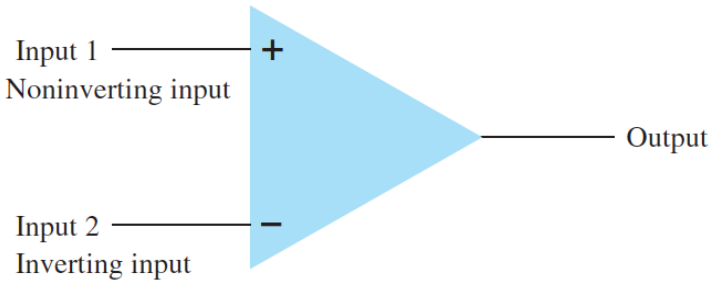


Offset null is a calibration feature of an operational amplifier (op amp) that allows the output voltage to be adjusted to zero when the input is zero. This helps to eliminate signal noise and interference.

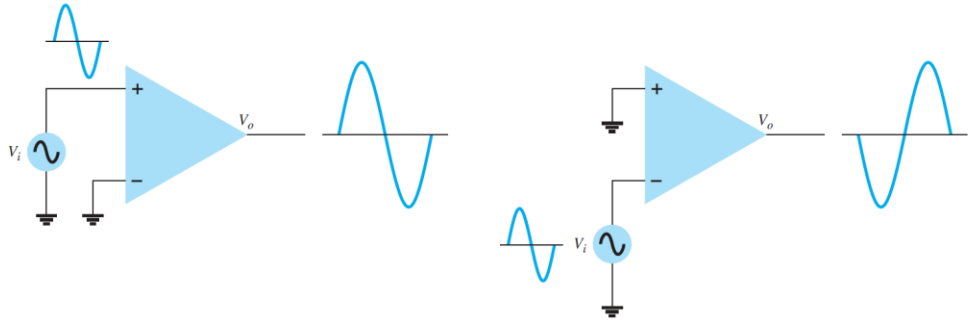
- An Op-Amp contains several transistors, resistors, and a few capacitors and diodes.

- More simply, an Op-Amp is depicted as:

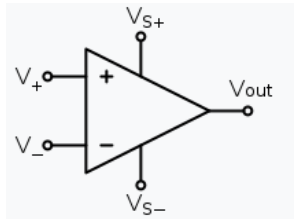


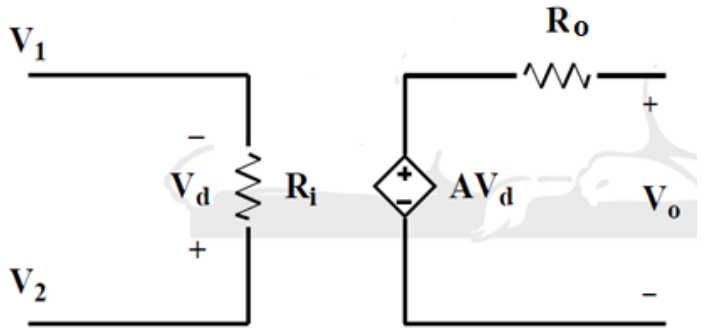


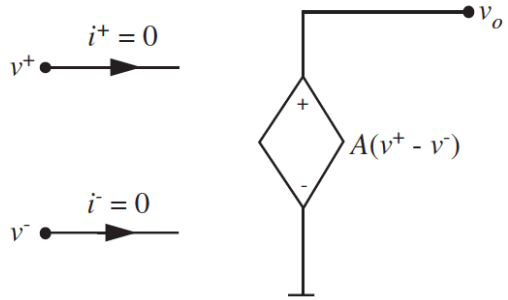
$$V_{out} = A_{OL}(V_+ - V_-)$$



Parameter	Variable	Ideal Values	Typical Ranges
Open-Loop Voltage Gain	A	∞	10^5 to 10^8
Input Resistance	Ri	$\infty\ \Omega$	10^5 to $10^{13}\ \Omega$
Output Resistance	Ro	0 Ω	10 to 100 Ω
Supply Voltage	Vcc/V+ -Vcc/V-	N/A N/A	5 to 30 V -30V to 0V



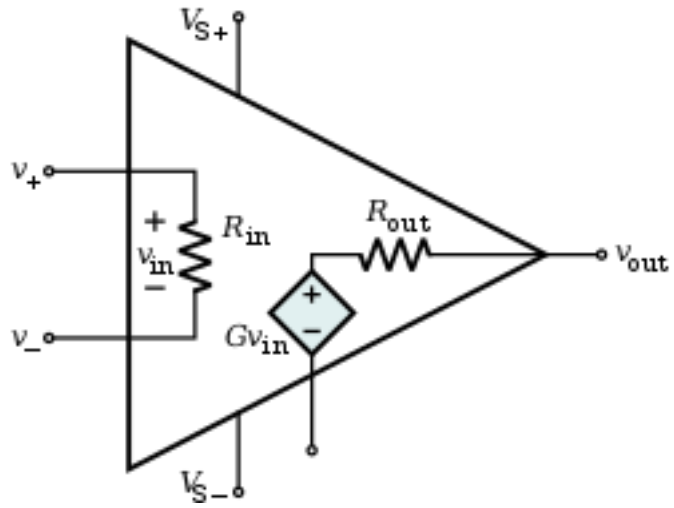




Ideal Op-Amp Summary

An ideal op amp has the following characteristics

- Infinite open-loop gain **G = V_{out} / V_{in}**
- Infinite input impedance Rin, and so zero input current
- Zero input offset voltage
- Infinite output voltage range
- Zero output impedance R_{out}, and so infinite output current range
- Zero noise
- Infinite bandwidth with zero phase shift and infinite slew rate
- Infinite common-mode rejection ratio (CMRR)
- Infinite power supply rejection ratio



These can be summarized by the two rules

- In a closed loop (negative feedback) the output does whatever is necessary to make the voltage difference between the inputs zero
- The inputs draw zero current

Op-Amp Terminology: Explained

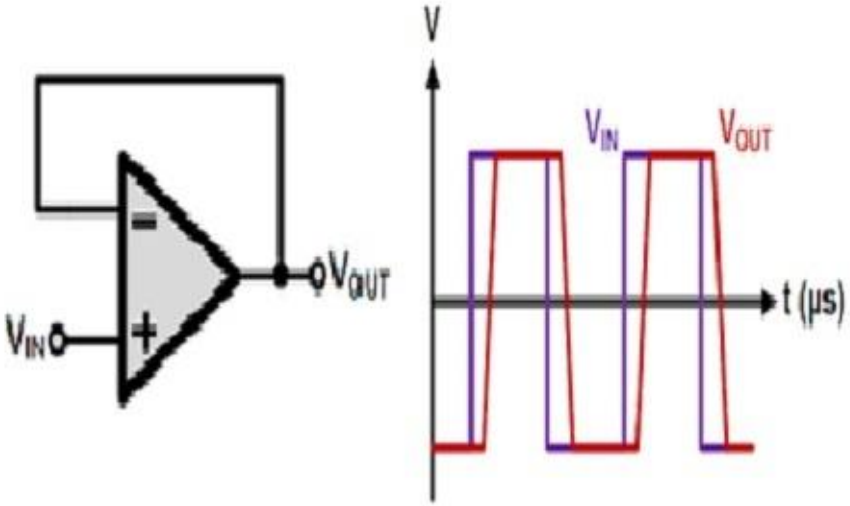
Slew Rate: Slew rate is defined as the maximum rate of change of an op amps output voltage, and is given in units of volts per microsecond.

Slew rate is measured by applying a large signal step, such as one volt, to the input of the op amp, and measuring the rate of change from 10% to 90% of the output signal's amplitude.

CMRR: If a signal is applied equally to both inputs of an op amp, so that the differential input voltage is unaffected, the output should not be affected.

In practice, changes in common mode voltage will produce changes in output. The op amp common-mode rejection ratio (CMRR) is the ratio of the common-mode gain to differential-mode gain.

For example: if a differential input change of Y volts produces a change of 1 V at the output, and a common-mode change of X volts produces a similar change of 1 V, then the CMRR is X/Y.



Op-Amp Terminology

The power supply rejection ratio is defined as the changes in input offset voltage per unit changes in the DC supply voltage. The power supply is also calculated in the format of dB. The mathematical equation of the power supply rejection ratio is given below.

$$\mathrm{PSRR[dB]} = 10\log_{10}\left(\frac{{\Delta V_{\mathrm{supply}}}^2 {A_v}^2}{{\Delta V_{\mathrm{out}}}^2}\right)\mathrm{dB}$$

Thank you