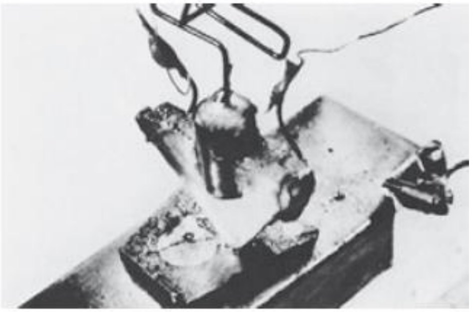
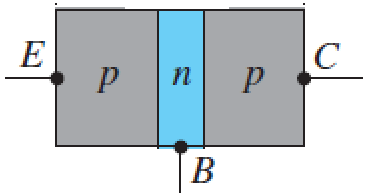
Fundamentals of Electronics

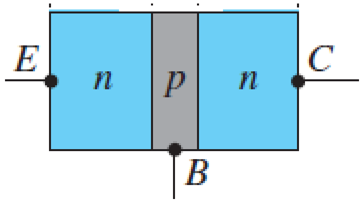
ECE 101

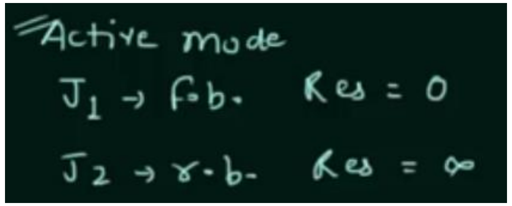
Bipolar Junction Transistor (BJT)



The first transistor

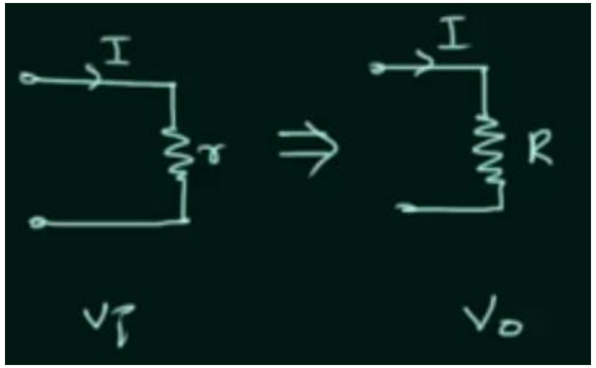


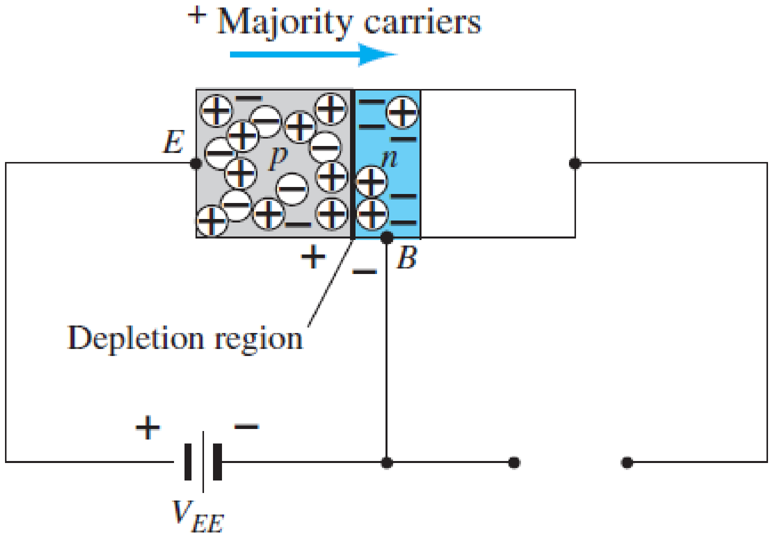


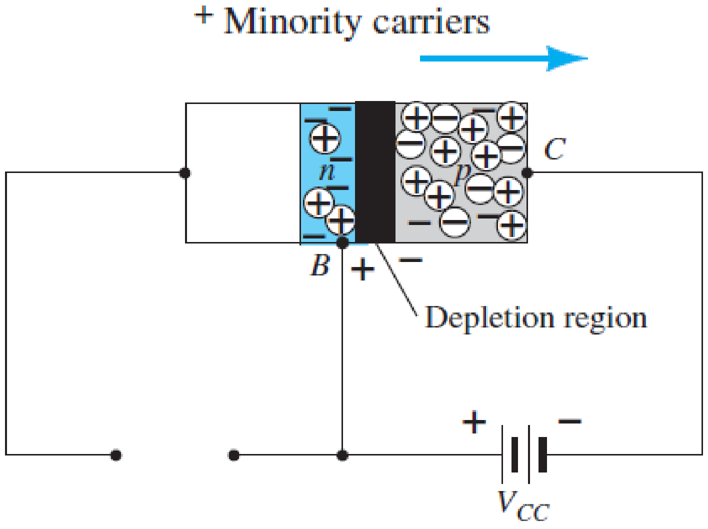


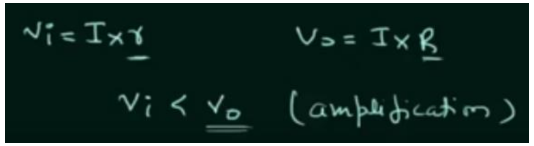
Basic mechanism

One p-n junction is forward biased,
the other one is reverse biased.

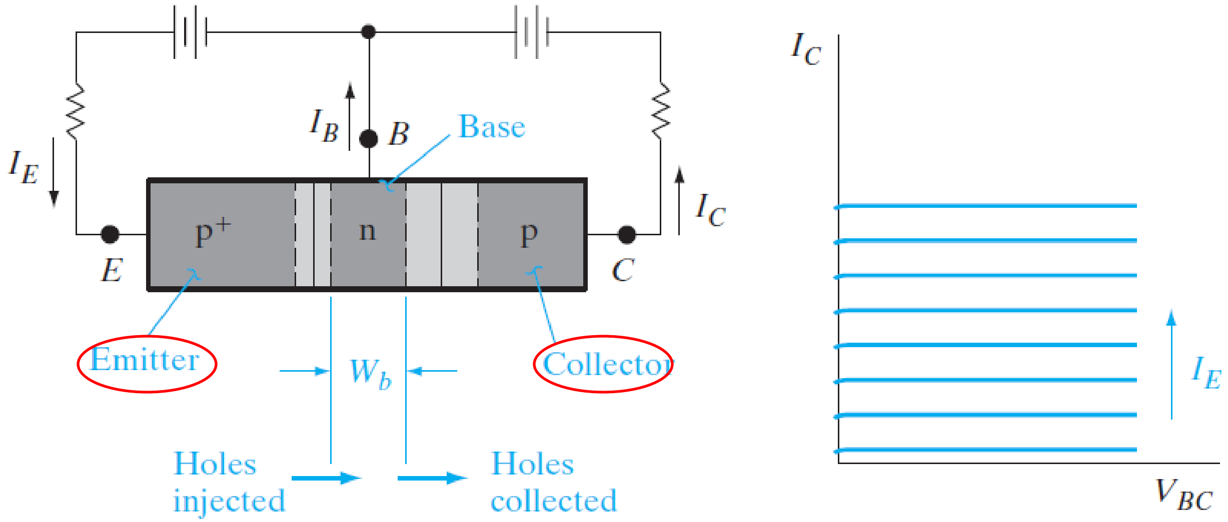






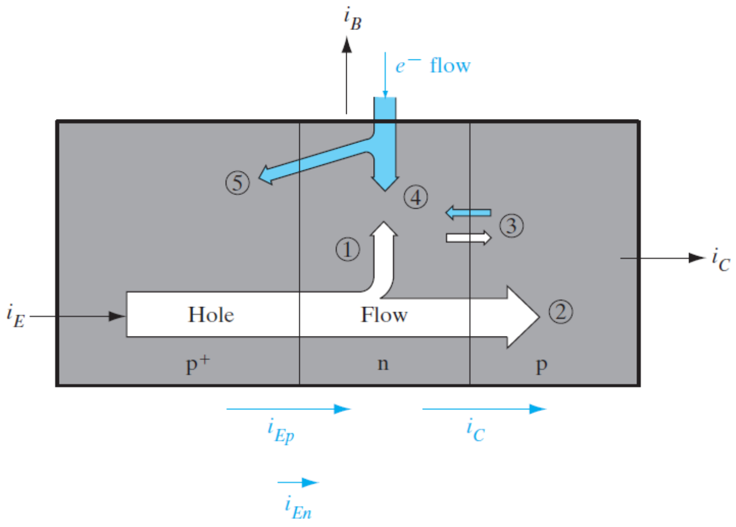


Understanding BJT IV characteristics…



- To have a good p-n-p transistor, we would prefer that almost all the holes injected by the emitter into the base be collected.
- Thus, the n-type base region should be narrow, and the hole lifetime t_p should be long. This requirement is summed up by specifying $W_b \ll L_p$.
- A second requirement is that the current I_E crossing the emitter junction should be composed almost entirely of holes injected into the base
  - Rather than electrons crossing from base to emitter.
  - This requirement is satisfied by doping the base region lightly compared with the emitter

Current components in BJT



Components of the base current

- Recombination of injected holes with electrons in the base, even with Wb < Lp. The electrons lost to recombination must be resupplied through the base contact.
- Some electrons will be injected from n to p in the forward-biased emitter junction, even if the emitter is heavily doped compared with the base.
- Some electrons are swept into the base at the reverse-biased collector junction due to thermal generation in the collector.

Amplification with BJTs

$$i_C = Bi_{Ep}$$

- B is the fraction of injected holes which make it across the base to the collector. it is called the **base transport factor**.
- The total emitter current consists of hole component and electron component (injected from the base). The **emitter injection efficiency** is defined as:

$$\gamma = \frac{i_{Ep}}{i_{En} + i_{Ep}}$$

- **For an ideal transistor, we would like B and γ to be unity.**
- The relation between collector and emitter currents is:

$$\frac{i_C}{i_E} = \frac{Bi_{Ep}}{i_{En} + i_{Ep}} = B\gamma \equiv \alpha$$

The product Bγ is defined as the factor α, called the current transfer ratio.

Amplification with BJTs contd…

- There is no real amplification between emitter and collector currents, since α is smaller than unity.
- On the other hand, the relation between base current and collector current is more promising.
- The base current consists of mainly two parts: **electrons recombining with holes in the base**, **electrons injected across the forward bias junction**:

$$i_B = i_{En} + (1-B)i_{Ep}$$

- The relation between collector and base current is: $$\frac{i_C}{i_B} = \frac{B i_{Ep}}{i_{En} + (1 - B)i_{Ep}} = \frac{B[i_{Ep}/(i_{En} + i_{Ep})]}{1 - B[i_{Ep}/(i_{En} + i_{Ep})]}$$

$$\frac{i_C}{i_B} = \frac{B\gamma}{1 - B\gamma} = \frac{\alpha}{1 - \alpha} \equiv \beta$$

- The factor β relating the collector current to the base current is the *base-to-collector current amplification factor.*
- Since α is near unity, it is clear that β can be large for a good transistor, and the collector current is large compared with the base current.

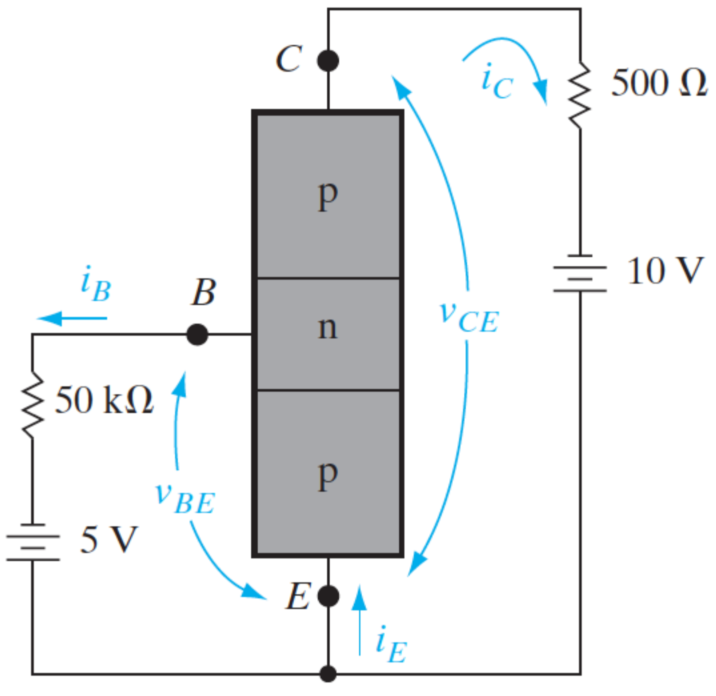
But, how can the collector current $\boldsymbol{i_C}$ can be controlled by variations in the small current $\boldsymbol{i_B}$?

- It can be shown from space charge neutrality arguments that $\boldsymbol{i_B}$ can indeed be used to determine the magnitude of $\boldsymbol{i_C}$.

- Since the n-type base region is electrostatically neutral between the two transition regions, the presence of excess holes in transit from emitter to collector calls for compensating excess electrons from the base contact.

- There is an important difference in the times that electrons and holes spend in the base.
- The average excess hole spends a time τ_t, defined as the transit time from the emitter to collector.
- Since the base width W_b is made small compared with L_p, this transit time is much less than the average hole lifetime τ_p in the base.

- On the other hand, an average excess electron supplied from the base contact spends τ_p seconds in the base, ensuring space charge neutrality during the lifetime of an average excess hole.
- While the average electron waits τ_p seconds for recombination, many individual holes can enter and leave the base region, each with an average transit time τ_t.
- In particular, for each electron entering from the base contact, τ_p / τ_t holes can pass from the emitter to collector while maintaining space charge neutrality.
-
- Thus the ratio of collector current to base current is simply: $\frac{i_C}{i_B} = \beta = \frac{\tau_p}{\tau_t}$



$$\tau_p = 10\ \mu\text{s}$$

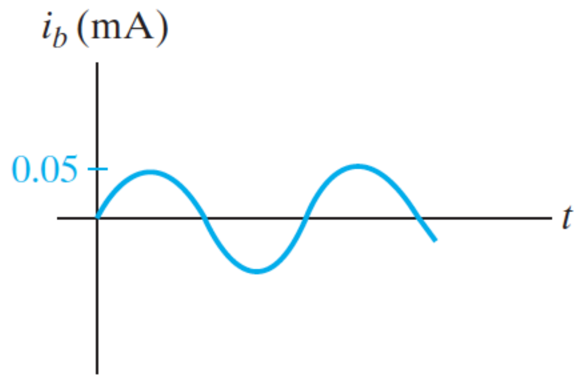
$$\tau_t = 0.1\ \mu\text{s}$$

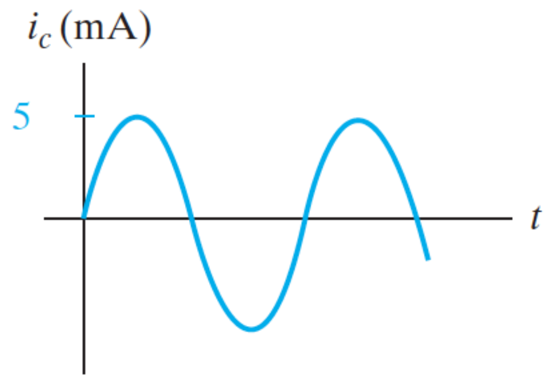
$$\frac{i_C}{i_B} = \beta = \frac{\tau_p}{\tau_t} = 100$$

Neglecting v_{BE}

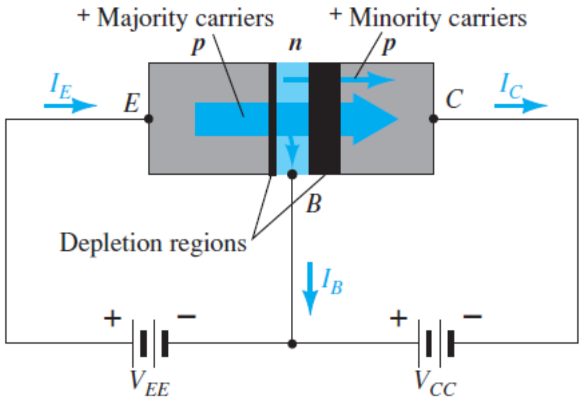
$$I_B = \frac{5\text{ V}}{50\text{ k}\Omega} = 0.1\text{ mA}$$

$$I_C = \beta I_B = 10\text{ mA}$$

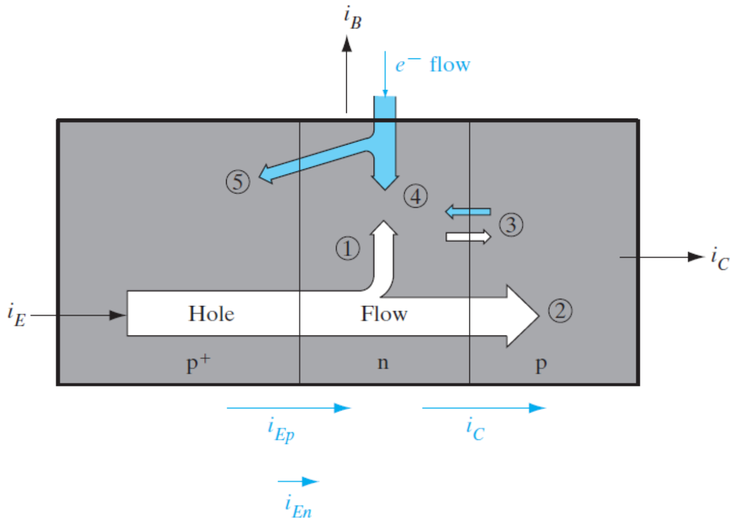


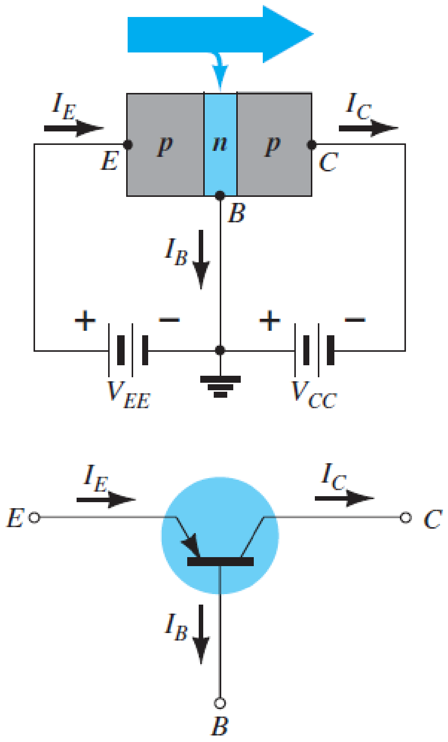


Bipolar Junction Transistor (BJT)

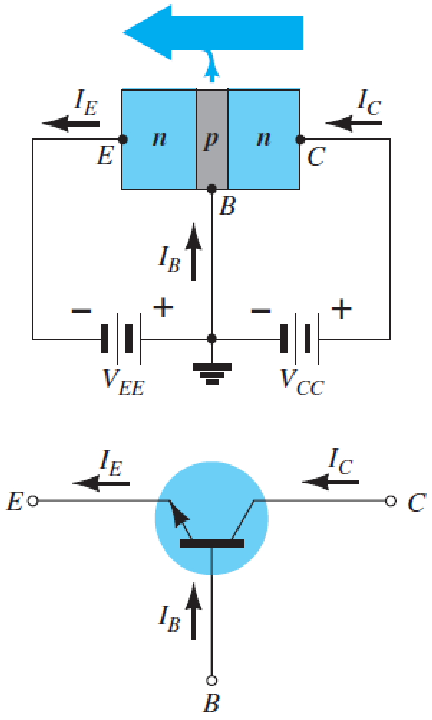


Current components in BJT





pnp transistor



npn transistor

Different regimes of operation of BJT

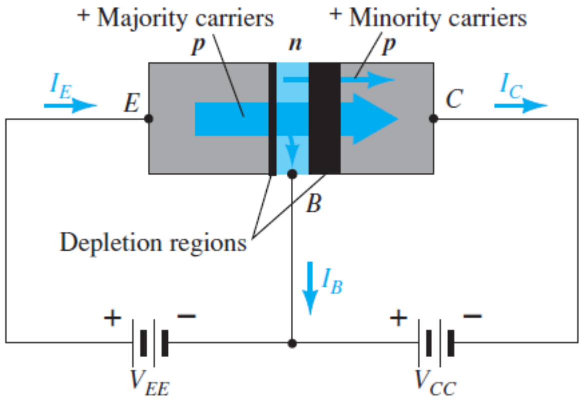
Inverse active regime

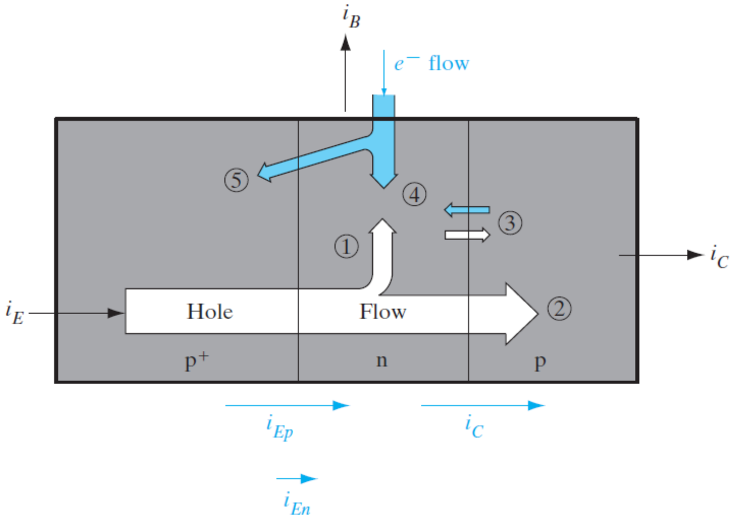
Active regime

Cut-off regime

Saturation regime

BJT Currents: Review

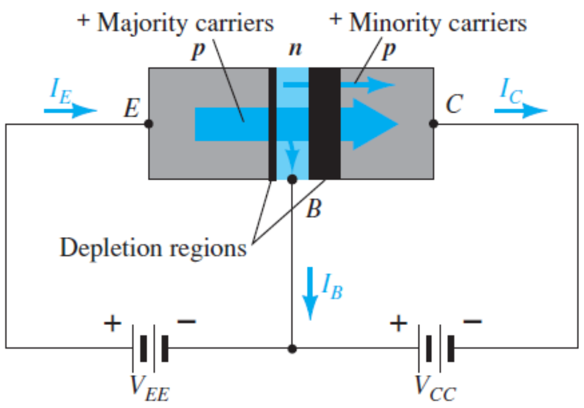




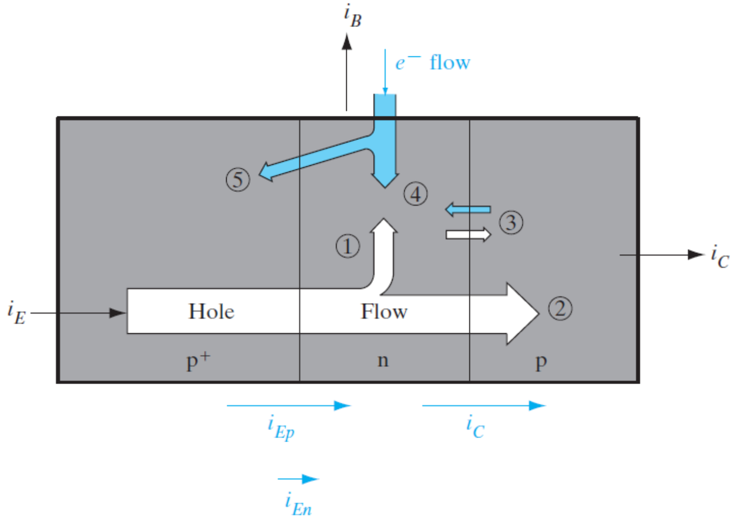
$$\frac{i_C}{i_E} = \frac{Bi_{Ep}}{i_{En} + i_{Ep}} = B\gamma \equiv \alpha$$

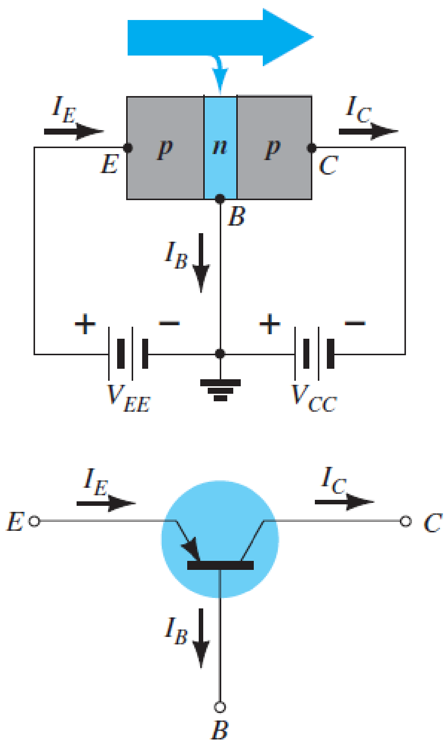
$$\frac{i_C}{i_B} = \frac{B\gamma}{1 - B\gamma} = \frac{\alpha}{1 - \alpha} \equiv \beta$$

Bipolar Junction Transistor (BJT)

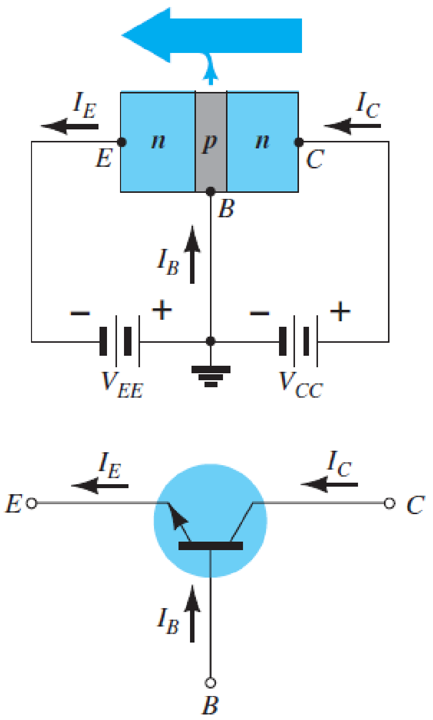


Current components in BJT





pnp transistor



npn transistor

Different regimes of operation of BJT

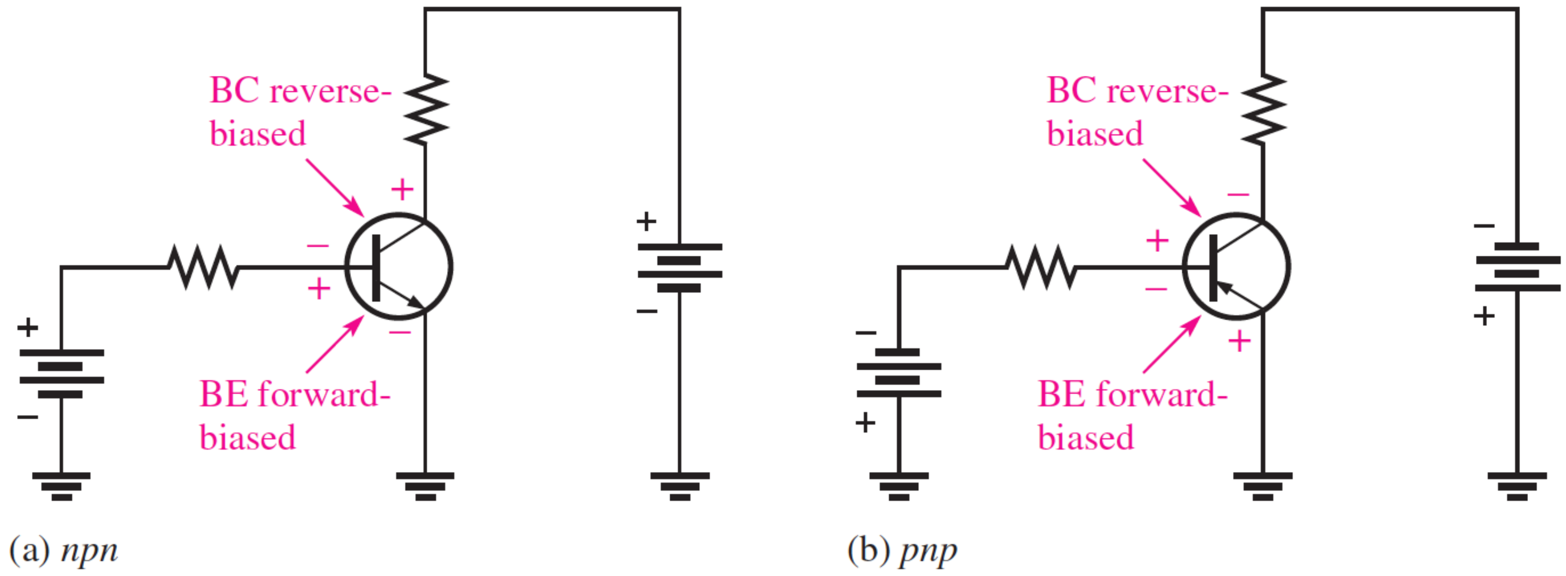
Active regime

Cut-off regime

Saturation regime

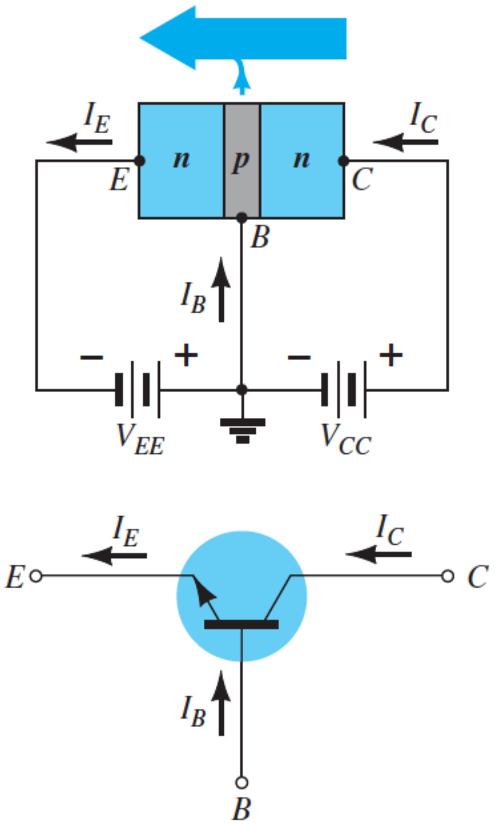
Inverse active regime

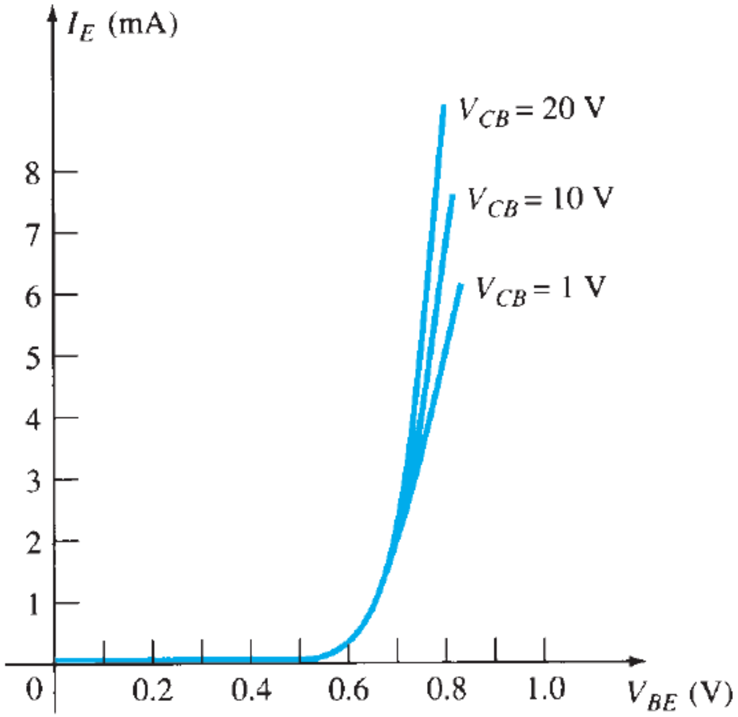
BJT Biasing

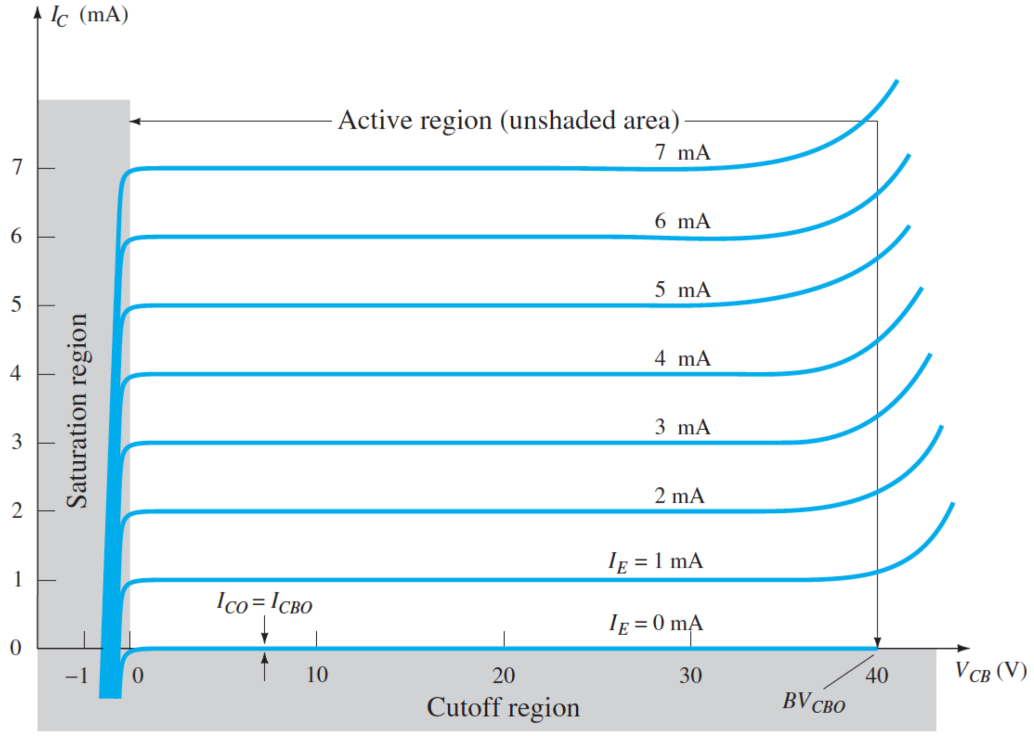


Forward-reverse bias of a BJT

Bipolar Junction Transistor (BJT): Input and Output Characteristics

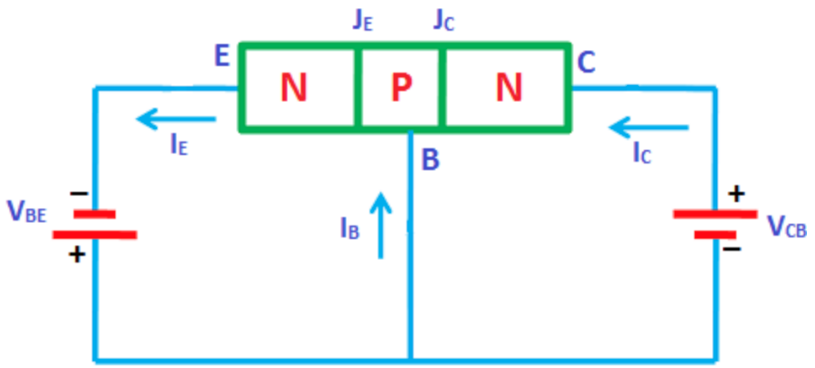


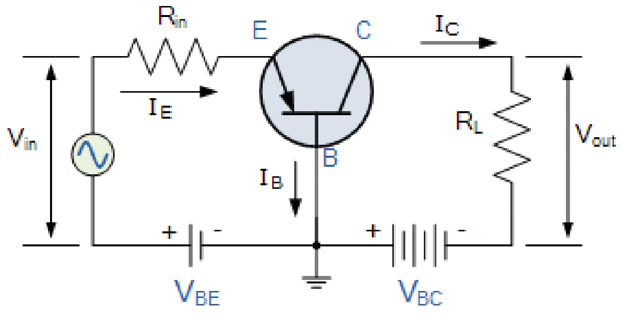




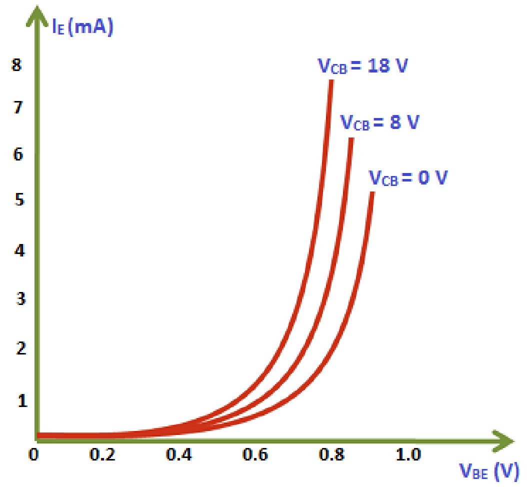
BJT Configurations

Common Base (CB) Configuration





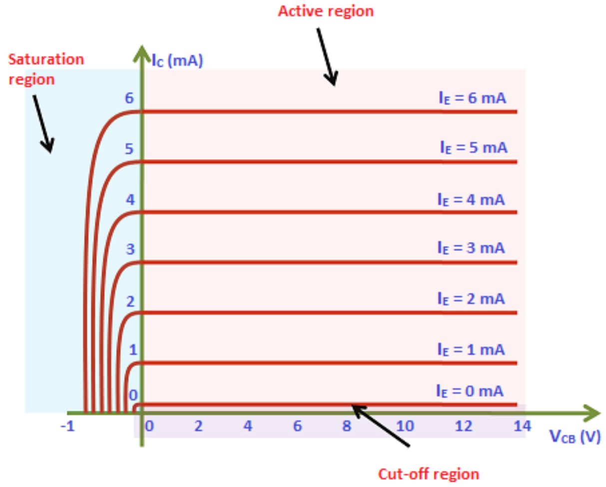
Input characteristics



I/p characteristics CB configuration

I_E vs. V_{BE}

Output characteristics



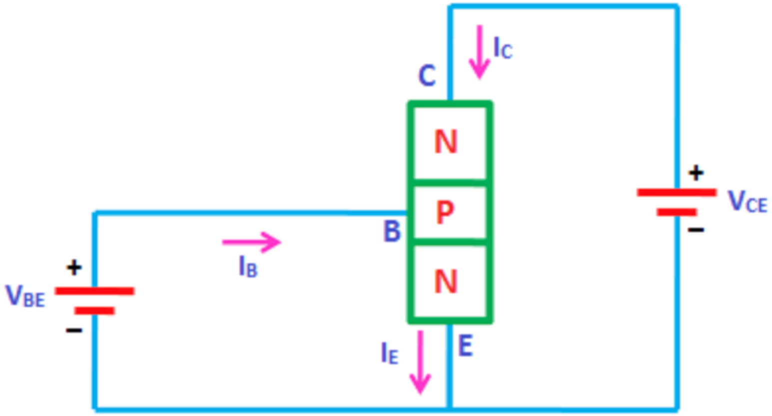
O/P characteristics CB configuration

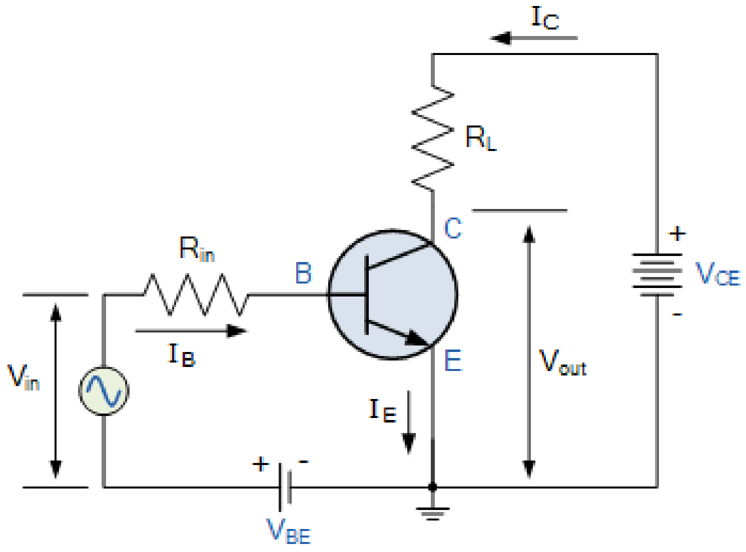
I_C vs. V_{CB}

no current gain but voltage gain

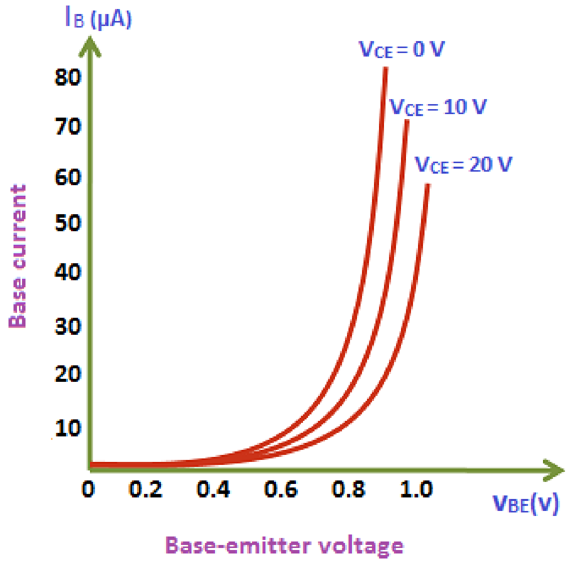
BJT Configurations

Common Emitter (CE) Configuration



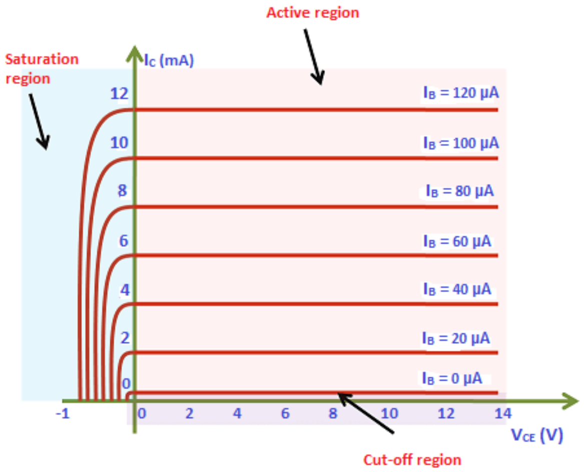


Input characteristics



I/P characteristics CE configuration

I_B vs. V_{EB}



O/P Characteristics CE Configuration

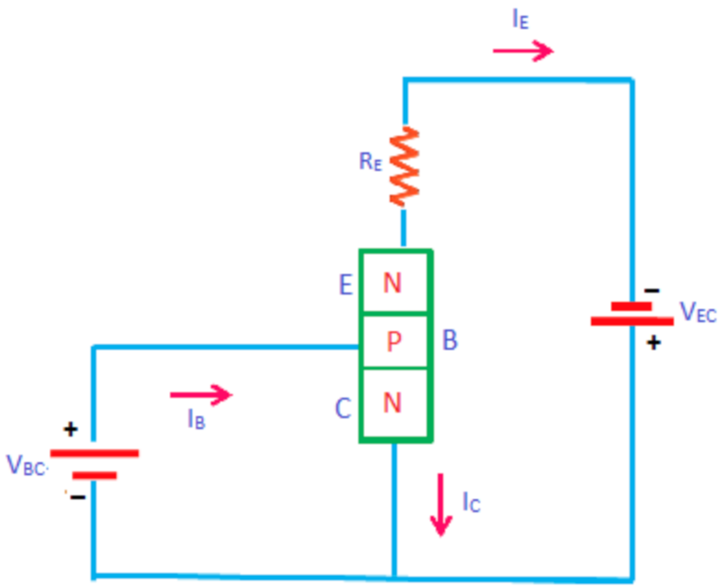
I_E vs. V_{EC}

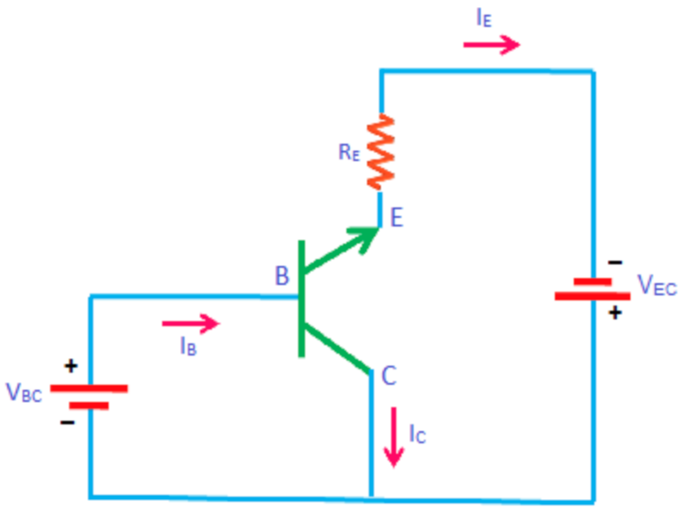
Output characteristics

current gain and voltage gain

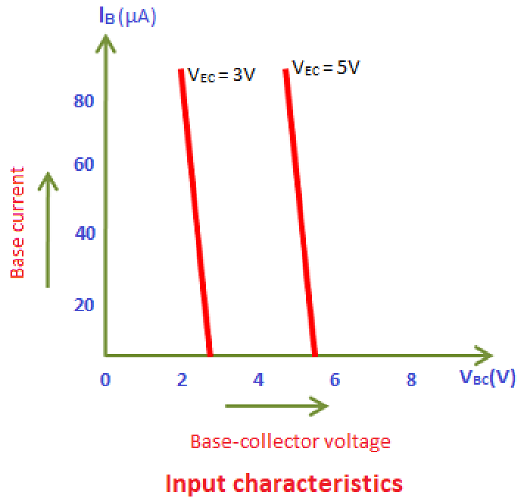
BJT Configurations

Common Collector (CC) Configuration



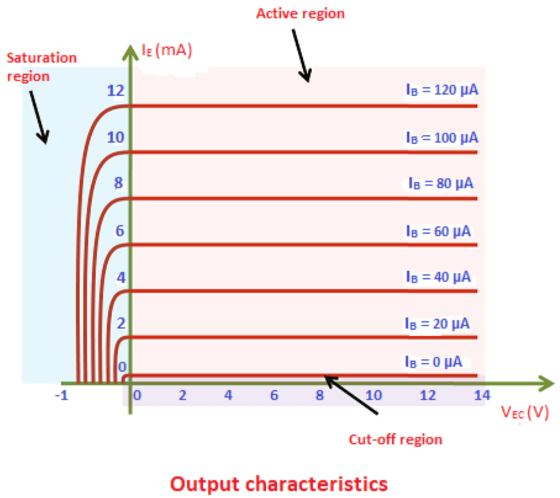


Input characteristics



I_B vs. V_{CB}

Output characteristics

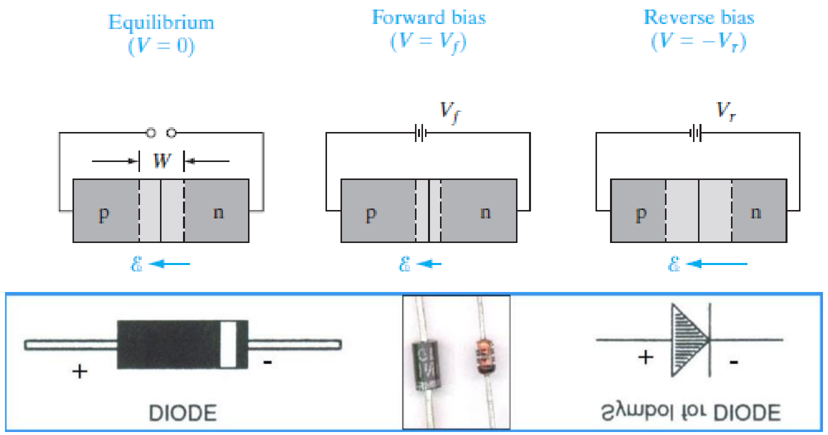


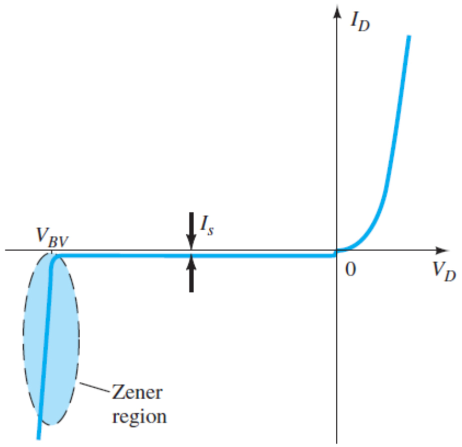
I_E vs. V_{CE}

current gain but no voltage gain

Summary of electronic devices

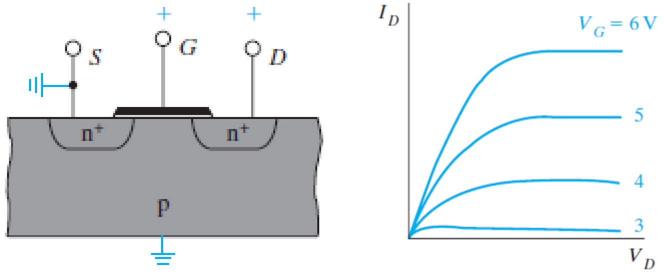
Diodes

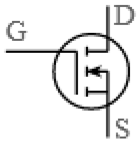




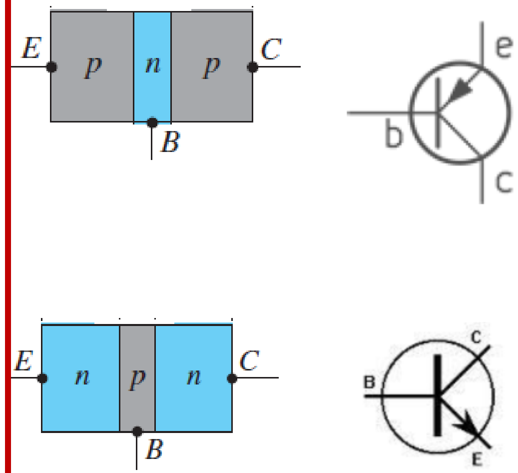
$$I_D = I_s(e^{V_D/nV_T} - 1)$$

MOSFETs





BJTs



BJT Configurations

- CB
- CC
- CE

Integration

- Integration is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip.

SSI - Small Scale integration

less than 100 components (about 10 gates)

MSI - Medium Scale integration

less than 500 components (more than 10 but less than 100 gates)

LSI - Large Scale integration

components b/w 500 and 300000 (more than 100 gates)

VLSI - Very Large Scale integration

it contains more than 300000 components per chip

Nowadays, more than a billion transistor on a chip.

Very large-scale integration (VLSI) is the process of integrating or embedding hundreds of thousands of transistors on a single silicon semiconductor microchip.

A microprocessor is an example of VLSI circuit.

Why VLSI?

- Physically smaller size
- Integration improves the design
- Lower parasitic = higher speed
- Lower power consumption
- Integration reduces manufacturing cost - (almost) no manual assembly

A Few VLSI companies in India

1 | Texas Instruments
Corporate office – Dallas, United State | **Establishment** –1951 |

2 | Analog Device Inc.
Corporate office – Norwood, USA | **Establishment** – 1965 |

3 | Cypress Semiconductor Corporation
Corporate office – San Jose, USA | **Establishment** – 1982 |

4 | Broadcom Corporation
Corporate office – Irvine, USA | **Establishment** – 1991 |

5 | Cisco Systems
Corporate office – San Jose, USA | **Establishment** – 1984 |

6 | Bit Mapper Integration Technologies Private Limited
Corporate office – Pune, Maharashtra | **Establishment** – 1985 |

7 | Horizon Semiconductors
Corporate office – Bangalore, Karnataka | **Establishment** – 1815|

8 | Einfochips limited
Corporate office – Ahmadabad, Gujarat | **Establishment** – 1994 |

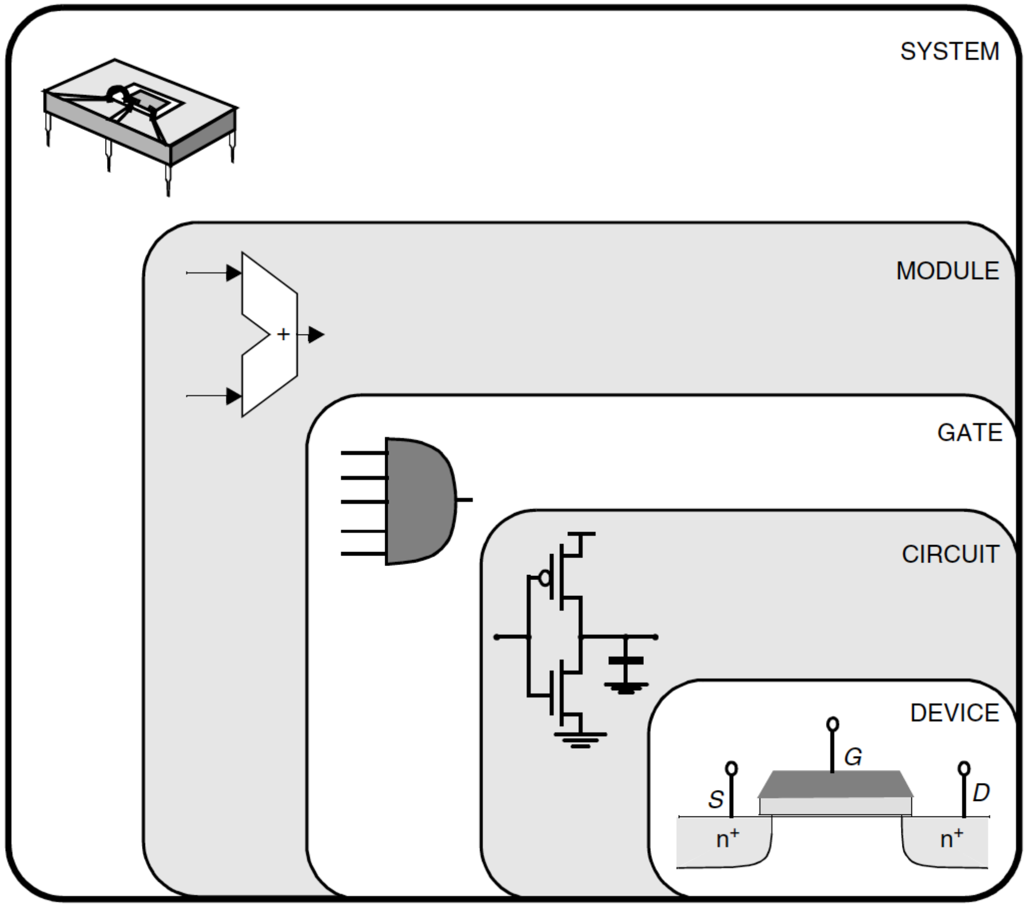
9 | Trident Tech Labs
Corporate office – New Delhi, India | **Establishment** – 2000 |

10 | HCL technologies
Corporate office – Noida, Uttar Pradesh | **Establishment** – 1991 |

System Level Electronics

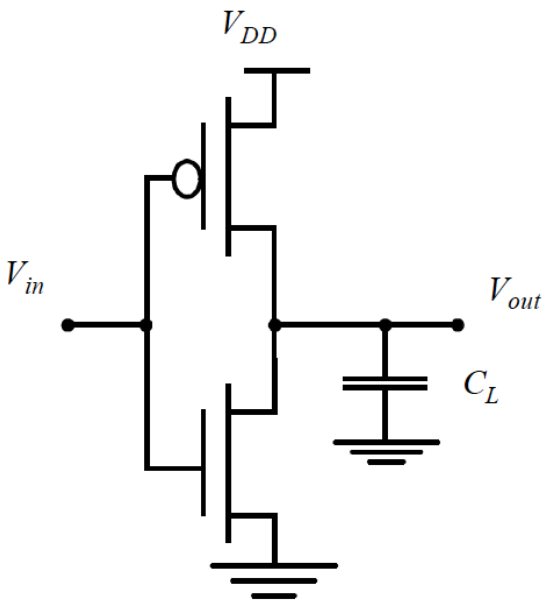
Abstraction

Design abstraction in digital electronics

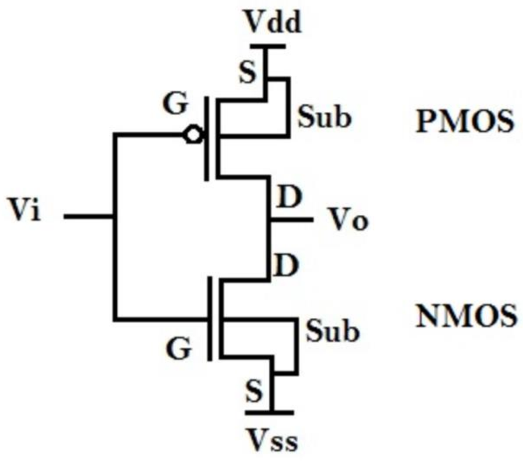


Digital Integrated Circuits by Rabaey et al

Logic gate implementation – CMOS Inverter

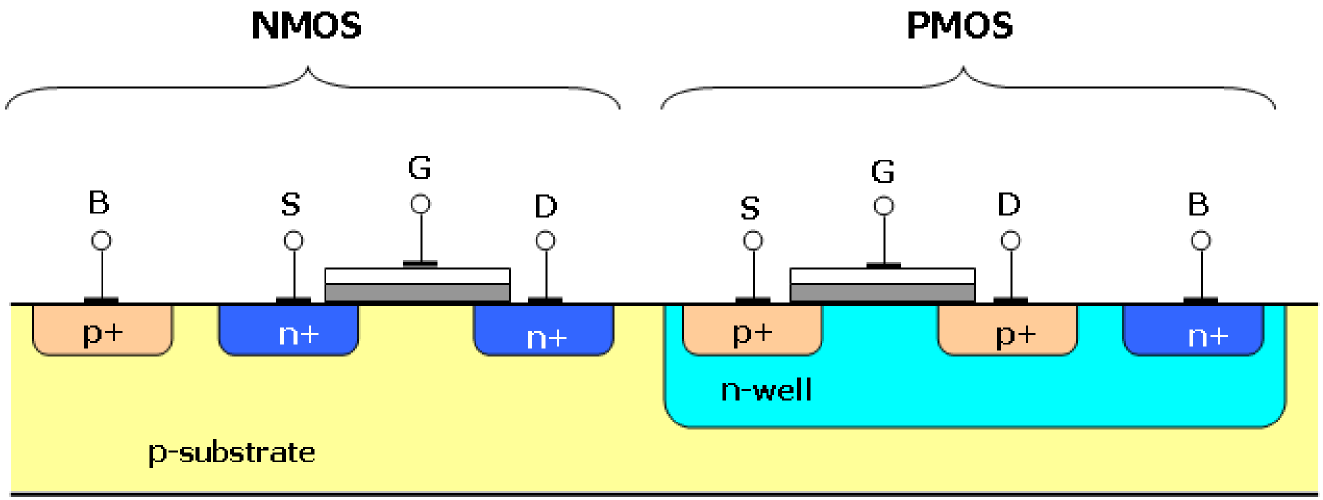


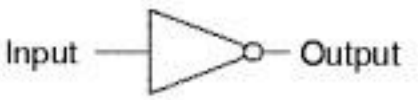
CMOS Inverter



G = Gate Terminal
S = Source Terminal
D = Drain Terminal
Sub = Substrate Terminal

CMOS Technology



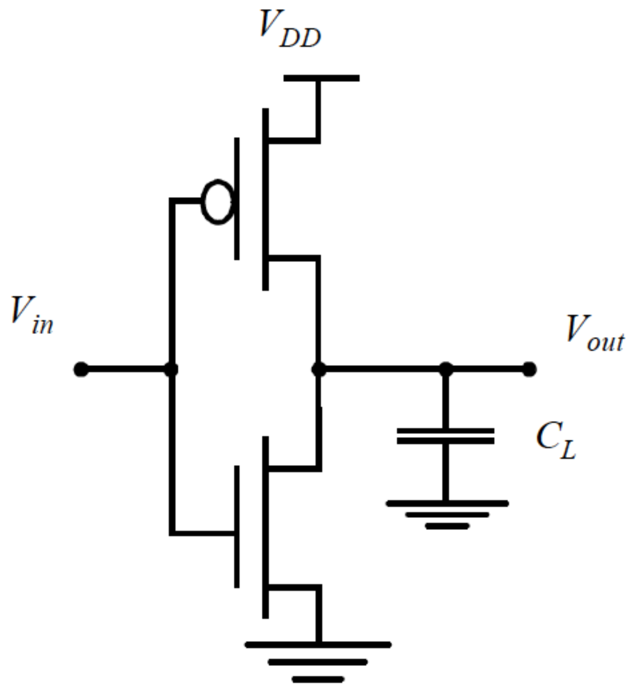


Input	Output
1	0
0	1

CMOS Inverter

Pull Up

Pull Down



CMOS Inverter

- Cost
- Static behavior
- Dynamic behavior/performance
- Energy efficiency

Thank you