Lab Report-5

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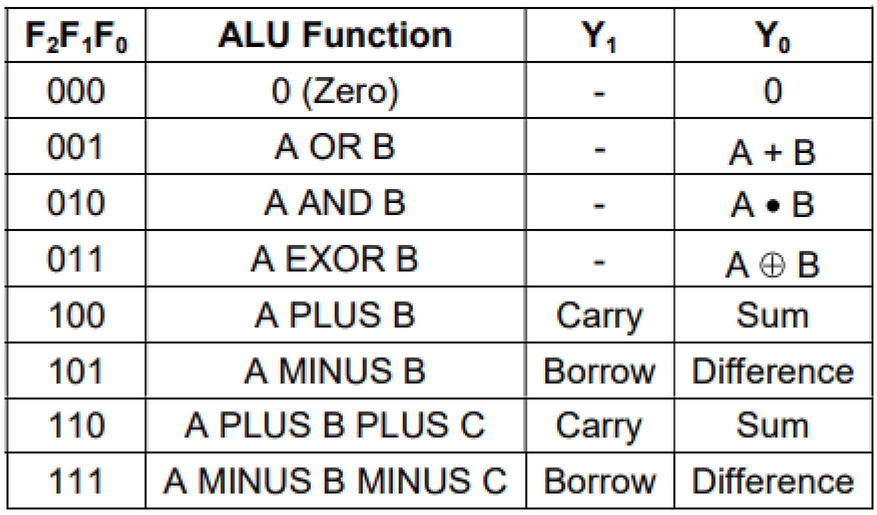
Group number: 7 (Teams-9)

Objective:

Using 1-bit operands, this experiment uses an ALU to accomplish 4 logical operations and 4 arithmetic operations. The circuit will consist of two 8-input multiplexers (74LS151), one quad 2-input multiplexer (74LS157) and one quad 2-input XOR gate (74LS86). The ALU can perform the all below given operations.

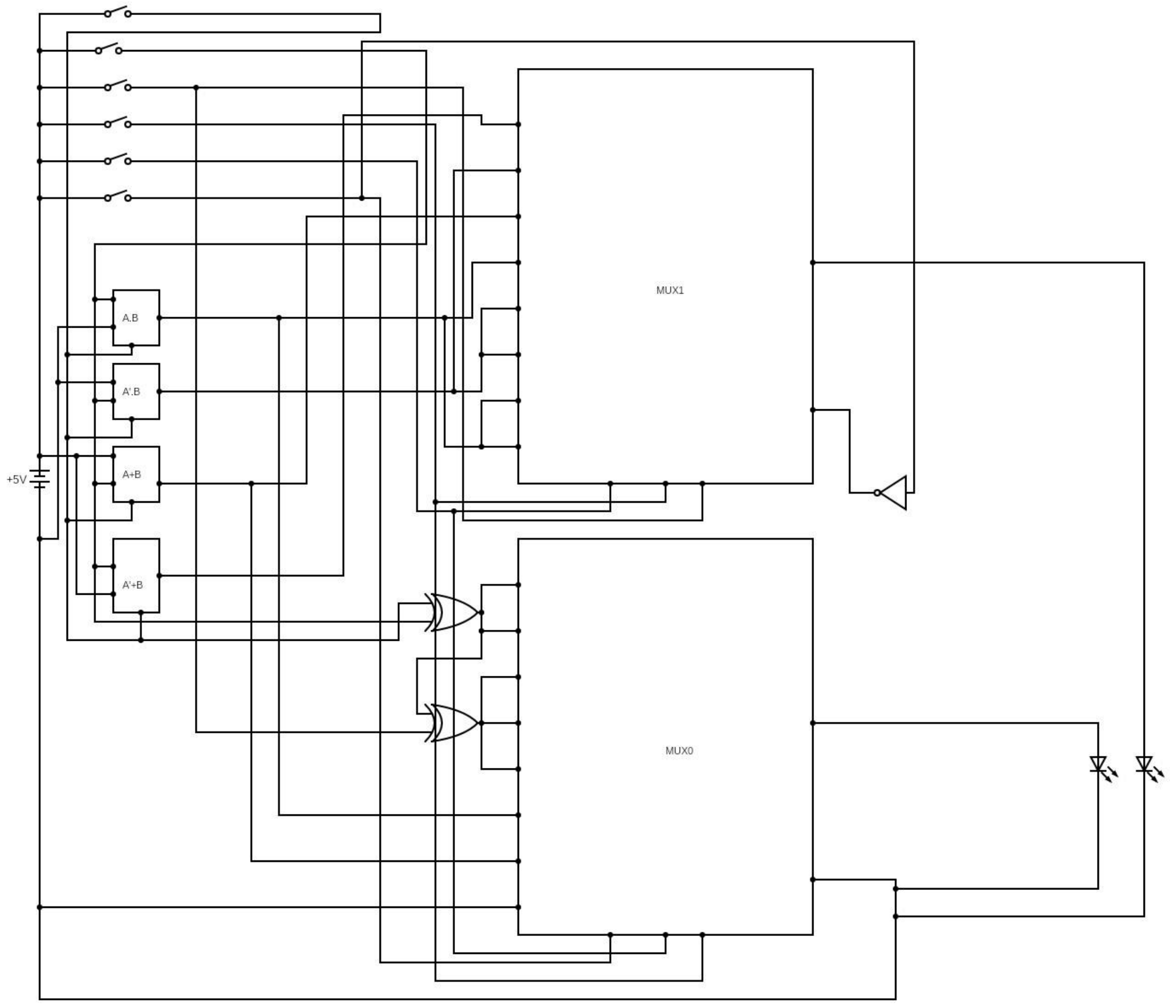


$F_2F_1F_0$	ALU Function	Y_1	Y_0
000	0 (Zero)	-	0
001	A OR B	-	$A + B$
010	A AND B	-	$A \bullet B$
011	A EXOR B	-	$A \oplus B$
100	A PLUS B	Carry	Sum
101	A MINUS B	Borrow	Difference
110	A PLUS B PLUS C	Carry	Sum
111	A MINUS B MINUS C	Borrow	Difference

Electronic components used:

1. Two 8-input multiplexers (74LS151)
2. One XOR Gate (IC - 7486)
3. 1 Quad 2-input multiplexer (74LS157)

The reference circuit:



Procedure:

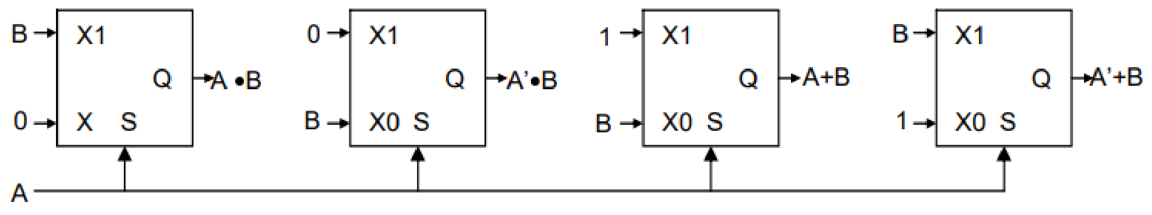
1. To execute various operations using the Arithmetic Logic Unit (ALU), we have the option of selecting from eight functions using three control lines: F2, F1, and F0. These control lines determine the specific operation that the ALU will perform. These functions encompass Zero, A OR B, A AND B, A XOR B, A PLUS B, A MINUS B, A PLUS B PLUS C, and A MINUS B MINUS C, each represented by unique binary codes ranging from 000 to 111.

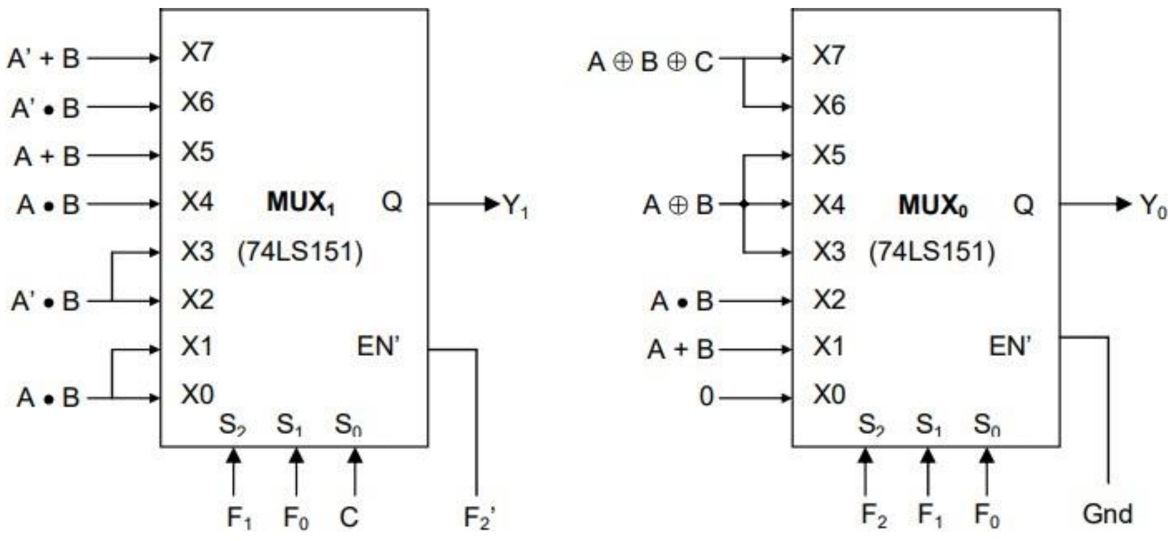
2. We configure the input values A, B, and C to match the requirements of the operation we intend to carry out. These input values serve as the operands for the chosen ALU function.

3. We complete the circuit by incorporating two 74LS151 chips, which are referred to as MUX0 and MUX1. These multiplexers are essential for selecting and executing the designated ALU function. We connect all the necessary inputs of MUX0 and MUX1 based on the chosen function.

4. To generate the Enable input for MUX1, we utilize a single gate from the XOR chip (74LS86). This is accomplished by taking the complement of the F2 input, essentially performing F2 XOR 1.

5. We then systematically apply all possible combinations of the Function select inputs (F2, F1, F0) one by one and record the resulting outputs Y0 and Y1 for a wide range of input values for A, B, and C. This step enables us to verify that the observed outcomes align with the expected behavior of the ALU. Given a circuit containing two 8:1 multiplexer (MUX), we design the ALU in accordance with the provided circuit diagram.



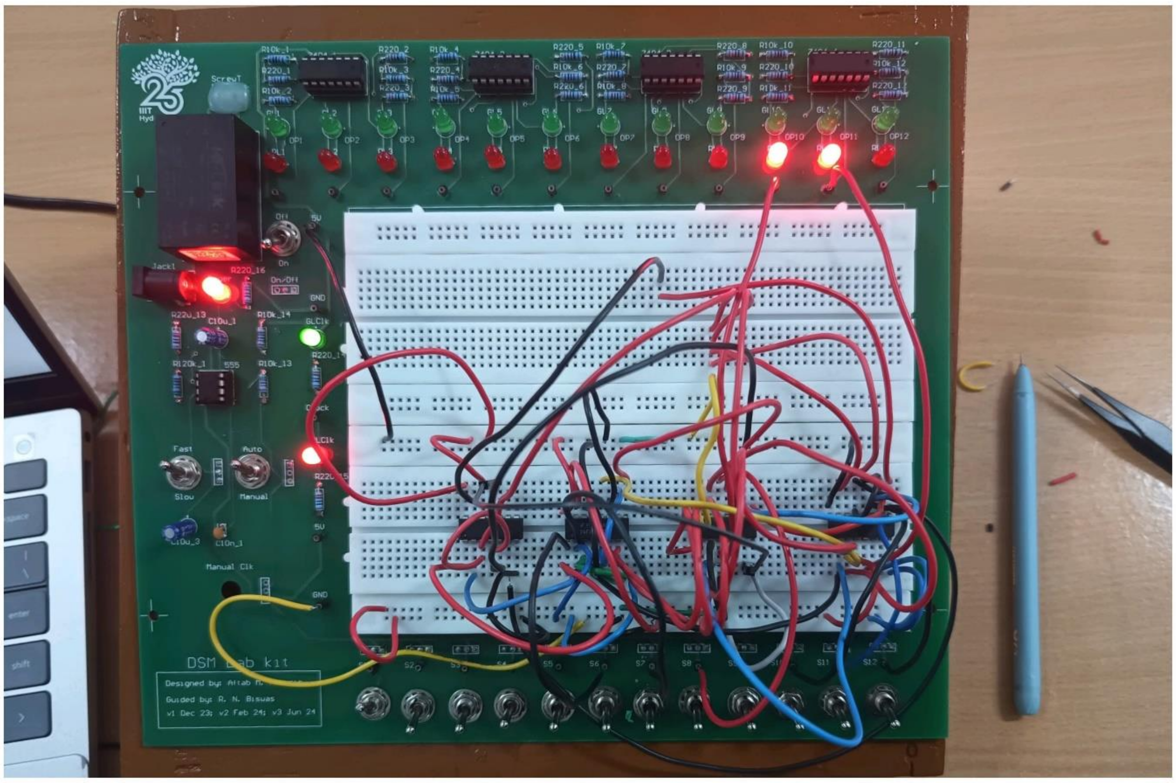


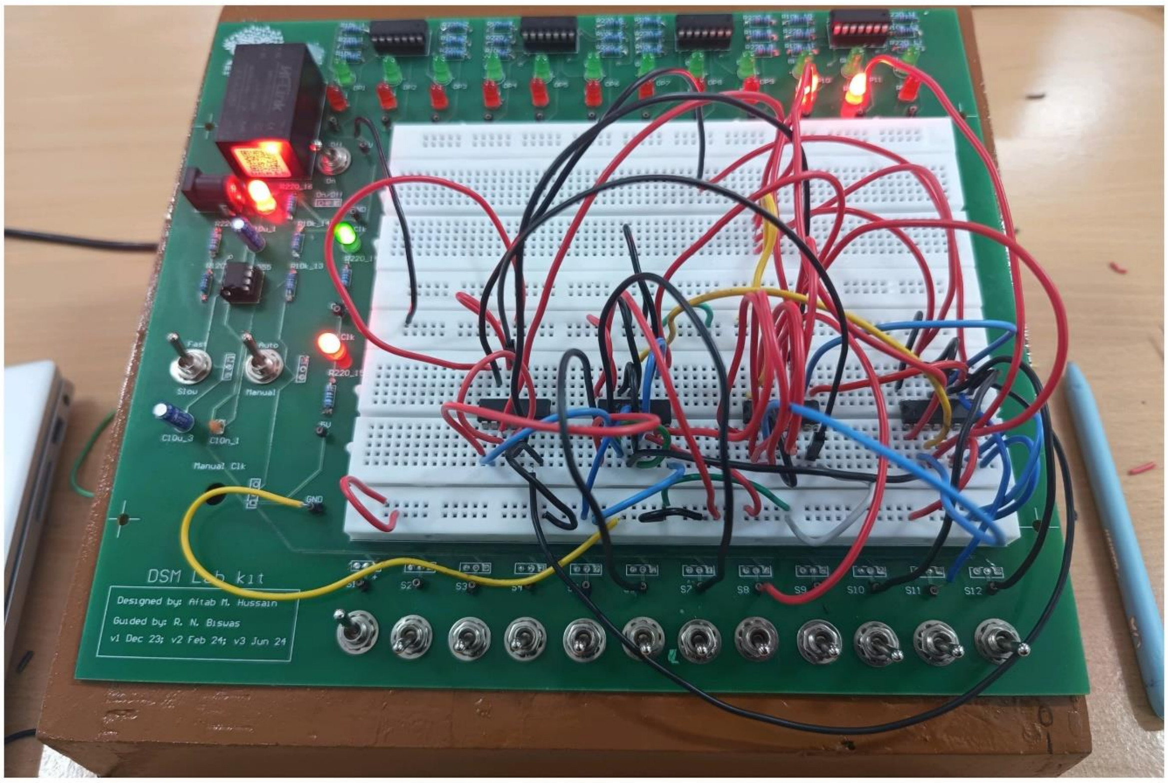
Conclusion:

Truth table

F2	F1	F0	A	B	C	ALU Function	Y1	Y0
0	0	0	-	-	-	0	-	0
0	0	0	0	0	0 or 1	A+B	0	0
0	0	0	0	1	0 or 1	A+B	0	1
0	0	0	1	0	0 or 1	A+B	0	1
0	0	1	1	1	0 or 1	A+B	0	1
0	1	1	0	0	0 or 1	A.B	0	0
0	1	1	0	1	0 or 1	A.B	0	0
0	1	1	1	0	0 or 1	A.B	0	0
0	1	0	1	1	0 or 1	A.B	0	1
0	1	0	0	0	0 or 1	$A\oplus B$	0	0
0	1	0	0	1	0 or 1	$A\oplus B$	0	1
0	1	0	1	0	0 or 1	$A\oplus B$	0	1
0	1	1	1	1	0 or 1	$A\oplus B$	0	0
1	0	1	0	0	0 or 1	A(plus)B	0	0
1	0	1	0	1	0 or 1	A(plus)B	0	1
1	0	1	1	0	0 or 1	A(plus)B	0	1
1	0	0	1	1	0 or 1	A(plus)B	1	0
1	0	0	0	0	0 or 1	A(minus)B	0	0
1	0	0	0	1	0 or 1	A(minus)B	0	0
1	0	0	1	0	0 or 1	A(minus)B	1	1
1	0	1	1	1	0 or 1	A(minus)B	0	0
1	1	1	0	0	0	A(plus)B(plus)C	0	0
1	1	1	0	1	1	A(plus)B(plus)C	1	1
1	1	1	1	0	0	A(plus)B(plus)C	1	1
1	1	0	1	1	0	A(plus)B(plus)C	1	1
1	0	0	0	0	1	A(plus)B(plus)C	0	0
1	0	0	0	1	1	A(plus)B(plus)C	0	0
1	0	0	1	0	0	A(plus)B(plus)C	0	0
1	0	1	1	1	1	A(plus)B(plus)C	1	1
1	0	1	0	0	0	A(minus)B(minus)C	0	0
1	0	1	0	1	1	A(minus)B(minus)C	0	0
1	0	1	1	0	0	A(minus)B(minus)C	1	1
1	0	0	1	1	0	A(minus)B(minus)C	1	1

1	1	0	0	0	1	A(minus)B(minus)C	0	0
1	1	0	0	1	1	A(minus)B(minus)C	0	0
1	1	0	1	0	0	A(minus)B(minus)C	0	0
1	1	1	1	1	1	A(minus)B(minus)C	1	1


DSM Lab kit
Designed by: Aftab M. Hussain
Guided by: R. N. Biswas
v1 Dec 23; v2 Feb 24; v3 Jun 24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In this experiment, we successfully designed and tested an 8-function ALU using 74LS151 multiplexers and 74LS86 XOR gates. The ALU performed 4 logic operations (1-bit output) and 4 arithmetic operations (2-bit output) as specified. After testing individual chips, the complete circuit was assembled, and its functionality was verified for all input combinations, confirming that it correctly performed the operations listed in the ALU function table.

Link for the Tinkercad simulation: