International Institute of Information Technology, Hyderabad

(Deemed to be University)

EC2.101 – Digital Systems and Microcontrollers

End Semester Examination

Max. Time: 3 Hr **Max. Marks: 70**

CALCULATORS ARE NOT ALLOWED

Numbers in square brackets [x] after a statement show the marks for that question.
Numbers in curly brackets {x} are for administrative use. Please ignore.

Q1. A leading-one detector (LOD) is an electronic circuit commonly found in central processing units and especially their arithmetic logic units (ALUs). It is used to detect at which position the leading bit in a computer word is 1. Given a 4-bit word (say $A_3A_2A_1A_0$), we are tasked with designing a LOD circuit, i.e., for a given input, the output should provide the bit position (either 3, 2, 1 or 0) of the first "1" encountered in the word, starting from the MSB side. If there are no "1"s in the word, a separate "zero" output should be activated and other outputs should be deactivated.

[15 marks]{CO-2}

Q2. Design a four-bit counter circuit using D flip-flops that jumps through only the 4-bit prime numbers sequentially. The counter goes back to 2 after 13. Assume that the circuit resets to 0010 by default.

[15 marks]{CO-3}

Q3. Let's say we plan to use the single correct, double detect Hamming code for a memory we are designing. The information word length is n-bit, and the address line width is k-bit. We plan to read the sensitive information stored after 1 year. Now, at the time of reading, we are informed that because of some cosmic forces, our memory will experience a bit-flip at a completely random place, with a probability of p. Find out the probability that our information cannot be fully retrieved [10]. Estimate the order of magnitude of the probability of failure in case $p = 10^{-6}$ (i.e., 1 in a million), $n = 32$ and $k = 32$ [5].

[10+5 = 15 marks]{CO-1}

Q4. We can design the 2's complement circuit using adder circuits. But is that the most optimum way? Design an optimal logic circuit for obtaining the 2's complement of a 4-bit binary number (ABCD) [10]. Count the number of transistors used and compare the number with the adder implementation [5].

[10+5 = 15 marks]{CO-2}

Q5. Perform the following conversions:

$(93.25)_{10} = (?)_8$
$(1011)_{10} = (?)_{16}$
$(CAD.004)_{16} = (?)_8$
$(123)_4 = (?)_{16}$
$(3.3)_{10} = (?)_2$

[2x5 = 10 marks]{CO-1}