ANALOG ELECTRONIC CIRCUITS

LAB REPORT-9

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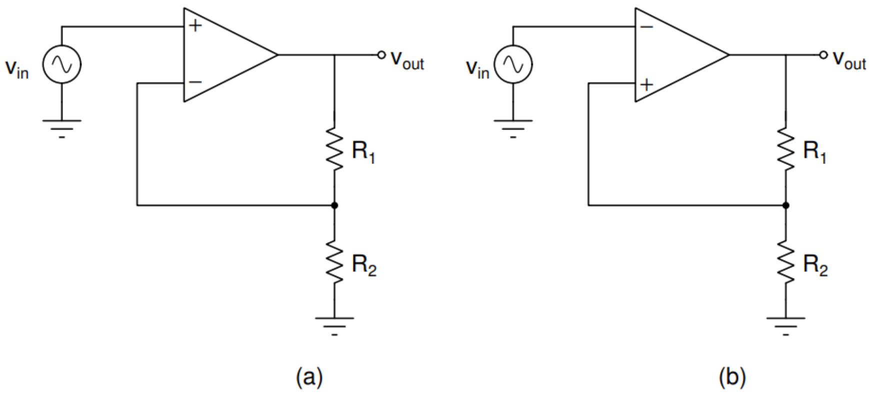
Operational Amplifier Circuits

1) Voltage Transfer characteristics in Negative and Positive feedback configurations :



a)

The Operational Amplifier in **figure (a) is operating in a Negative feedback** configuration because the output is linked to the inverting input and every time some fraction of Vout is subtracted to the differential input.

On the other hand, in **figure (b), the Operational Amplifier is in a positive feedback** configuration since the output is directed back to the noninverting input terminal and every time some fraction of Vout is adding to the differential input.

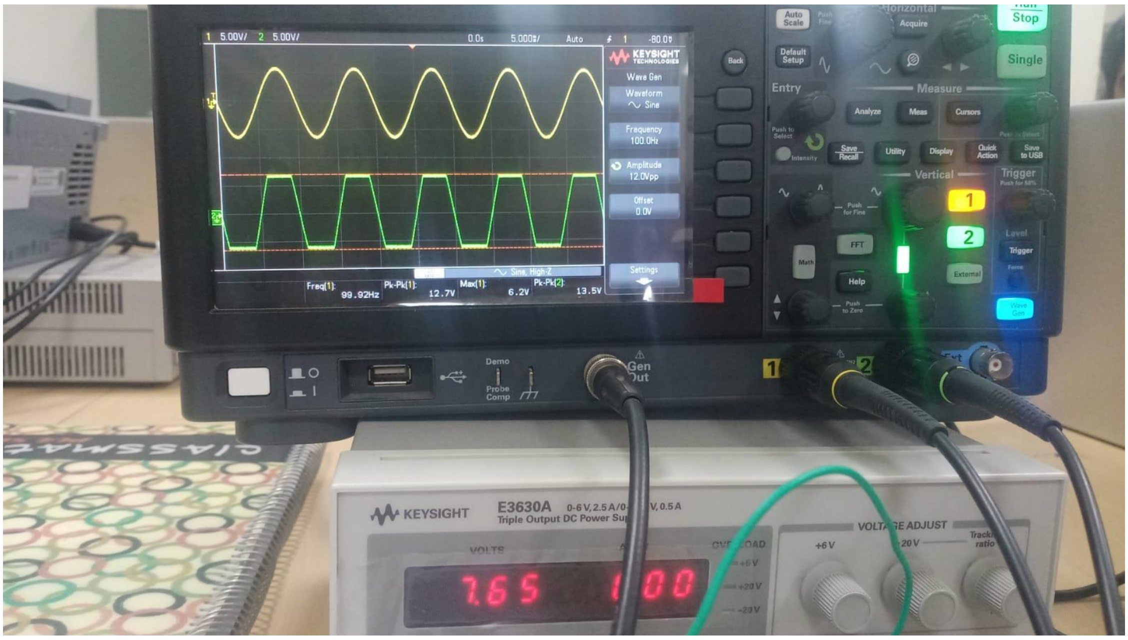
b)

We have plotted voltage transfer characteristics (Vout vs Vin) for the circuits shown in figures(a) and (b). We have varied Vin from -VDD to +VDD (a sine wave with amplitude VDD, low frequency say 100 Hz).

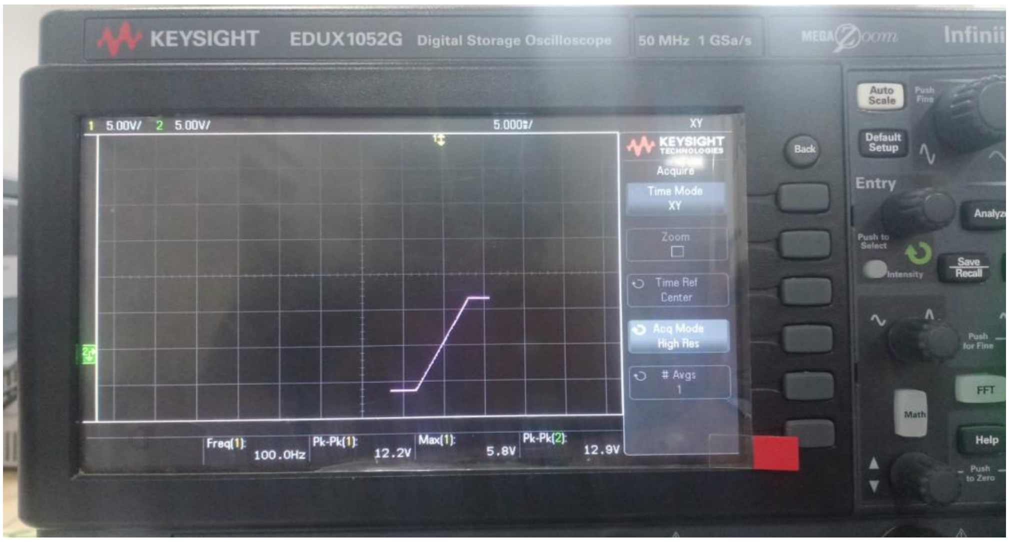
Applying Vin to inverting teminal(-ve terminal)
Vin =+-12Vpp (peak to peak)
Supply voltages=+-8V
R1=R2=10k ohm

For Figure 1 (Negative Feedback):

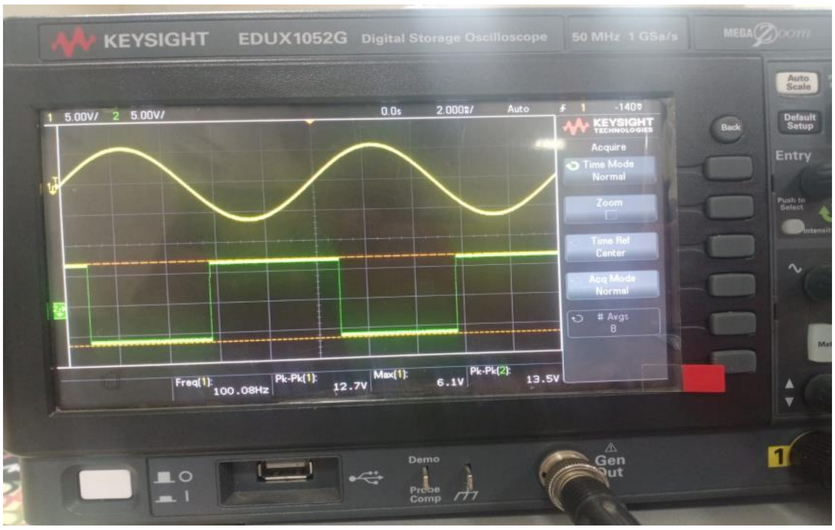
Vin and Vout:



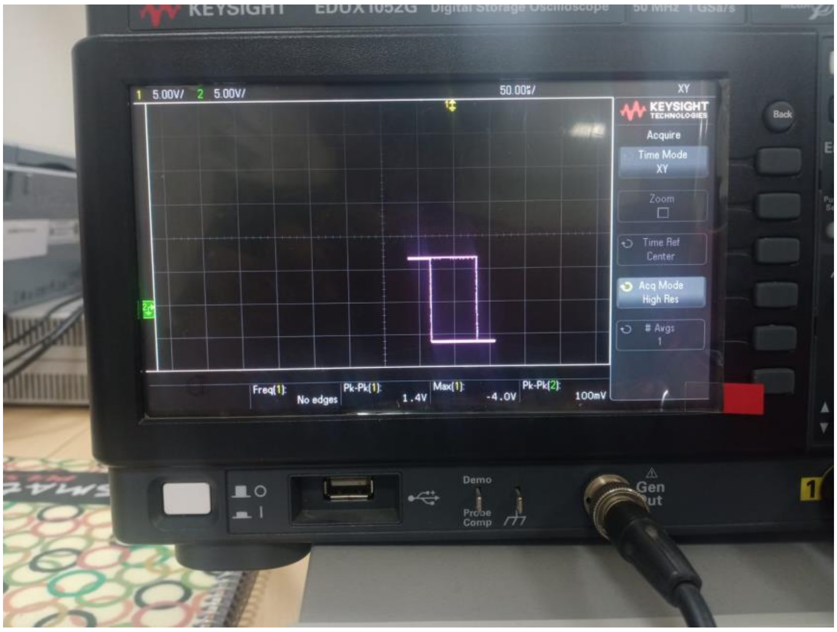
Vout v/s Vin:(VTC)



For Figure 2 (Positive Feedback):



Vout v/s Vin:(VTC)



c)

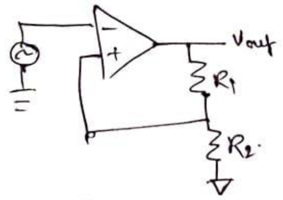
Positive feedback configuration provides regeneration/hysteresis,

where the output reinforces the input signal, leading to amplified and sustained extremes and used as oscillators. Negative feedback, on the other hand, improves stability and performance by subtracting the output from the input and can be used in building amplifiers.

Initially, **let the op-amp output is at one extreme, such as the positive supply voltage VDD. As the input voltage crosses the upper threshold, the positive feedback causes a rapid switch in the output to the opposite extreme, such as the negative supply voltage -VDD. With the output now at the opposite extreme, the input voltage must drop below the lower threshold for the output to switch back to the original extreme.** This hysteresis characteristic enables the Op-amp positive feedback circuit to provide stable and noise-tolerant switching behaviour.

The positive feedback reinforces the input signal, resulting in the output regenerating and transitioning to a new state once the input voltage crosses the thresholds.

(c)



$R_1 = R_2$

V_{in} from $-V_{DD}$ to V_{DD}

from $-V_{DD}$ to $V_{DD}/2$

the V_{out} will be V_{DD} because the difference in $V_+ - V_-$ will be greater than zero.

therefore it will saturate to $V_{DD} = V_{out}$

if $V_{in} = V_{DD}/2$ then at that instant $V_+ = V_-$

if $V_{in} > V_{DD}/2$ then it will saturate to $-V_{DD}$ as $V_+ - V_-$ is negative

Similarly if V_{in} from V_{DD} to $-V_{DD}$

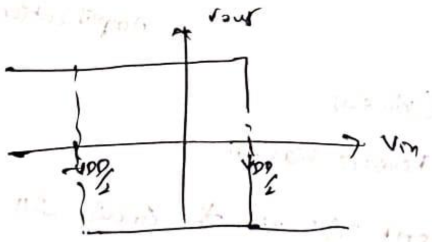
V_{DD} to $-V_{DD}/2$ $\rightarrow$ the saturated to $-V_{DD}$

then at $-V_{DD}/2$ the $V_+ - V_- = 0$

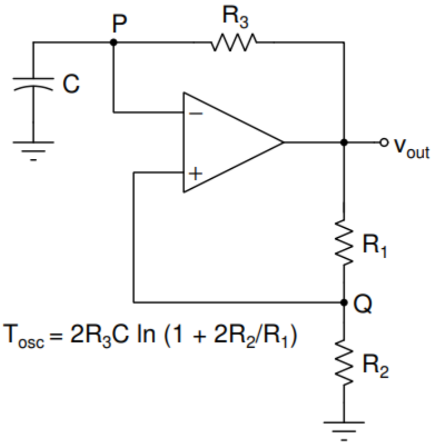
$\therefore$ it will become sudden dur

if $V_{in} < -V_{DD}/2$ then it will saturate to V_{DD}

$\therefore$ curve:

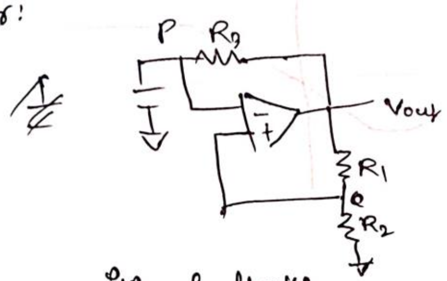


2) RC Oscillator (+ve feedback) :



Why positive feedback ?

RC oscillator:



Why it is a positive feedback?

→ Here if vout changes suddenly v_p also change suddenly and which is connected to Non-inverting terminal and some fracⁿ is adding.

But v_p is ~~charging and charging~~ changing as capacitor is charging & discharging.

∴ some fracⁿ is adding to differential input of op-Amp.

∴ It is +ve feedback.

a)**Freq Calculation:**

(a) $T = 2R_3 C \cdot \ln\left(1 + \frac{2R_2}{R_1}\right)$

$= 2\cdot(1K)(10^{-6}) \cdot \ln\left(1 + \frac{2(10K)}{(10K)}\right)$

$= 2(1K)(10^{-6}) \cdot \ln(3)$

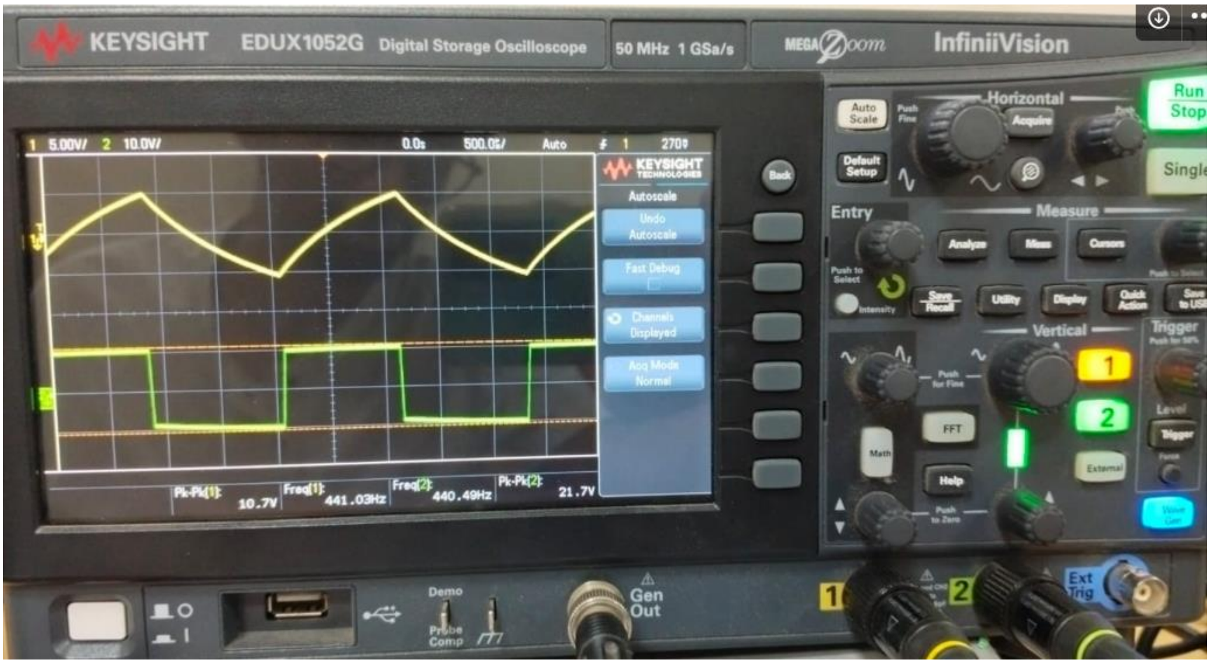
$T = 0.002197224$ sec

$f = \frac{1}{T} = \frac{1}{0.002197224}$

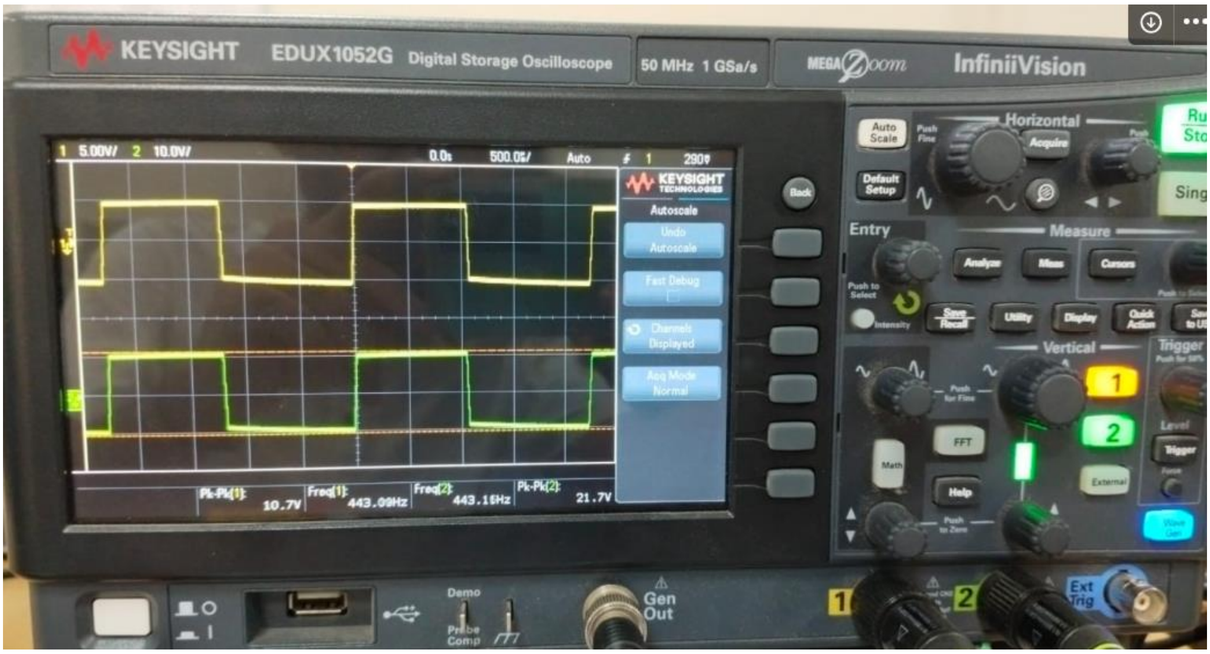
$f = 455.1199$

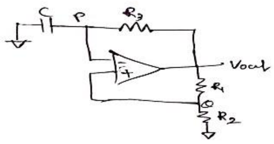
b)

Vp and Vout:

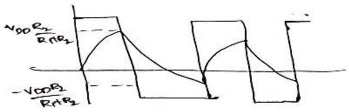


Vq and Vout:





$T_{osc} = 2R_3C\,\ln(1 + 2R_2/R_1)$



$i_C = i_{R_3}$

$C\frac{dV_P}{dt} = \frac{V_{out} - V_P}{R_3}$

→ for +ve cycle,

$\int \frac{dt}{R_3C} = \int \frac{dV_P}{V_{out} - V_P}$ $\quad V_{out} = V_{DD}$

$\frac{t}{R_3C} = \int_{-\frac{V_{DD}R_2}{R_1+R_2}}^{\frac{V_{DD}R_2}{R_1+R_2}} \frac{dV_P}{V_{out} - V_P}$

$= \ln(V_{out} - V_P)\Big|_{-\frac{V_{DD}R_2}{R_1+R_2}}^{\frac{V_{DD}R_2}{R_1+R_2}}$

$= \ln\left(\frac{R_1}{R_1 + 2R_2}\right)$

$T = R_3C\,\ln\left(1 + 2\frac{R_2}{R_1}\right)$

→ for +ve & -ve cycle (one period)

$T = 2R_3C\,\ln\left(1 + \frac{2R_2}{R_1}\right)$

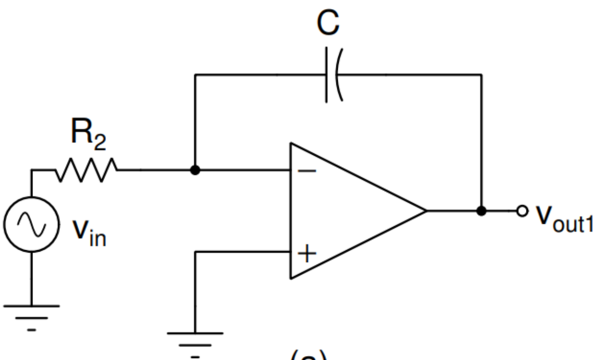
observed frequency=441.03hz.

Theoretical fosc=455.1196Hz which is nearly equal to the observes value of frequency.

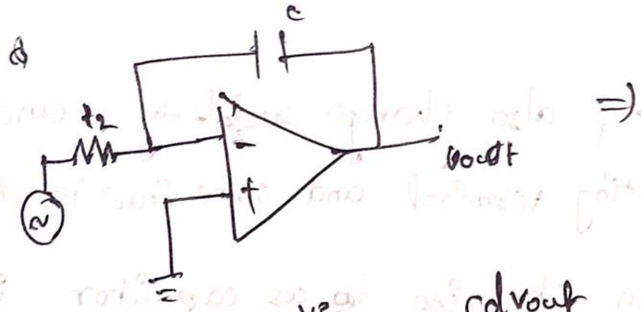
3) Integrator (-ve feedback) :

a)

We have connected the circuit as shown in the below figure. R1 = 10 kΩ, R2 = 1 kΩ, Vin = 0 V (DC) C = 10 nF.



(a)



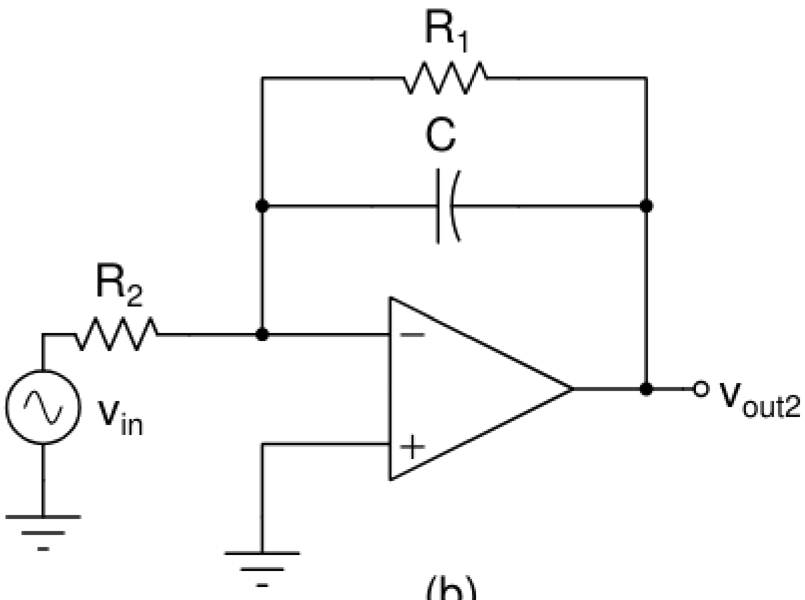
$$\frac{V_{in}}{R_2} = -\frac{C\,dV_{out}}{dt}$$

$$V_{out} = \frac{-1}{R_2 C}\int v_{in}\,dt$$

In this part of the experiment, the input voltage vin is kept at a constant 0V. However, due to the inherent DC offset of the Op Amp, the output voltage will continuously increase until the Op Amp reaches saturation.

Due to DC-Offset the output becomes saturated to VDD.

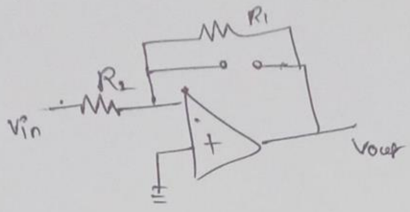
b)



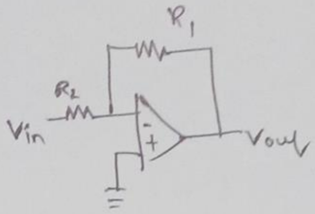
(b)

2(b)

(a) after capacitor becomes short circuit the circuit will be like -ve feedback circuit



$\Rightarrow$



$$A\left(0 - V_{in} + (V_{out} - V_{in})\frac{R_2}{R_1+R_2}\right) = V_{out}$$

$$\therefore\ AV_{in} + A(V_{out} - V_{in})\frac{R_2}{R_1+R_2} = V_{out}$$

$$AV_{in} - AV_{in}\frac{R_2}{R_1+R_2} = V_{out} - AV_{out}\left(\frac{R_2}{R_1+R_2}\right)$$

$$V_{in}\left(A - \frac{AR_2}{R_1+R_2}\right) = V_{out}\left(1 - \frac{AR_2}{R_1+R_2}\right)$$

$$\frac{V_{out}}{V_{in}} = \frac{A - \frac{AR_2}{R_1+R_2}}{1 - \frac{AR_2}{R_1+R_2}}$$

$A\left(\frac{R_2}{R_1+R_2}\right) \approx 10^{-6}$ $\longrightarrow$ Neglect

$$\approx \frac{\cancel{A}\left(\frac{R_1+R_2}{R_1}\right)}{\cancel{A}\left(1 - \cancel{A}\frac{R_2}{(R_1+R_2)}\right)}$$

$$= \frac{R_1+R_2}{R_2}$$

$$\boxed{\text{Gain} = 1 + \frac{R_1}{R_2}}$$

3(b) To prevent the op-Amp from saturating, a resistor R'_1 (with $10k\Omega$) is connected accross the capacitor in circuit.

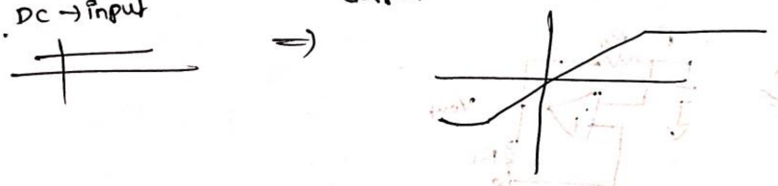
→ The resistor avoid excessive voltage build-up & ensure the op-amp operates within its linear range.

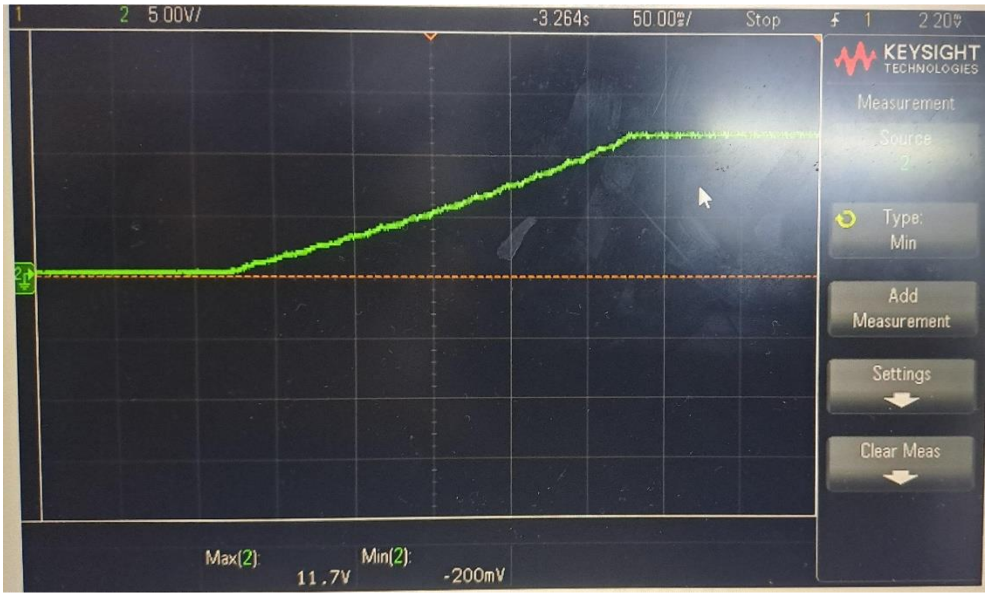
From the above plot, it is evident that op-Amp has not reduced saturation.
This is due to presence of resistor R_1, which maintains the negative feedback loop even after capacitor is fully charged.

~~DC offset in~~

DC → input ⟹ output

output





We have connected the circuit as shown in the below figure and measured voltage at Vout2 using the oscilloscope. In this configuration, when we give an input DC voltage, it acts as an integrator and produces a signal which varies linearly with time. But the capacitor gets saturated after some time. So, we add a resistor in parallel to the capacitor. After the capacitor gets fully charged, resistor makes the circuit to act as an Inverting amplifier in closed loop configuration. Therefore we won’t get much gain. Also, the output would be saturated.

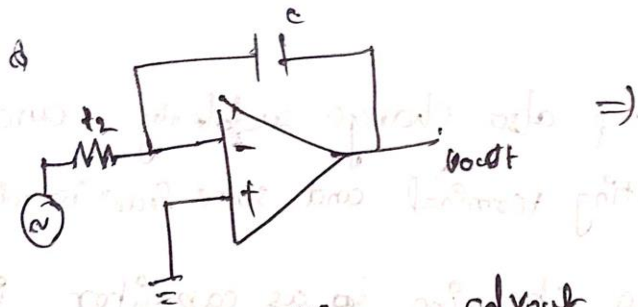
The dc voltage got integrated and output as shown in fig.

Checking of integrator:

Given sine wave:

We got the output as cos wave which is integration of sin signal in checking.

c)



$$\frac{V_{in}}{R_2} = -\frac{C\,dV_{out}}{dt}$$

$$V_{out} = \frac{-1}{R_2 C}\int v_{in}\,dt$$

for square Wave :

$$V_{out} = \frac{-1}{R_2 C} \int \frac{A}{2} dt \quad \Big\} \text{ for +ve half cycle.}$$

$$= \left(\frac{-A}{2 R_2 C}\right) t \quad \Big\}$$

$= 500m\,(T/2) + 0$

DC offset

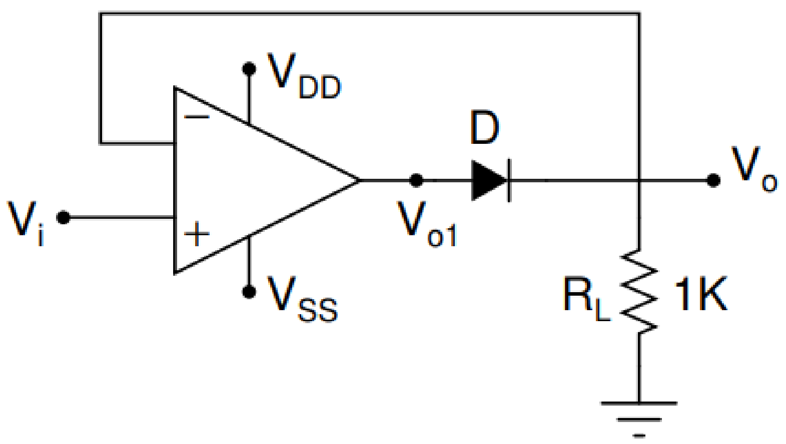
Triangular wave

we got Integrator

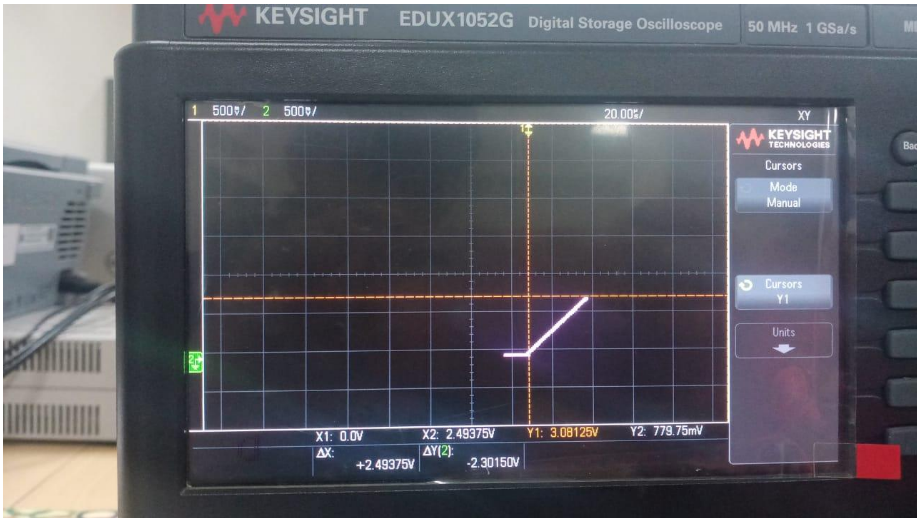
$$V_{out} = \frac{-1}{R_2 C} \int \frac{-A}{2} dt \quad \Big\} \text{-ve cycle}$$

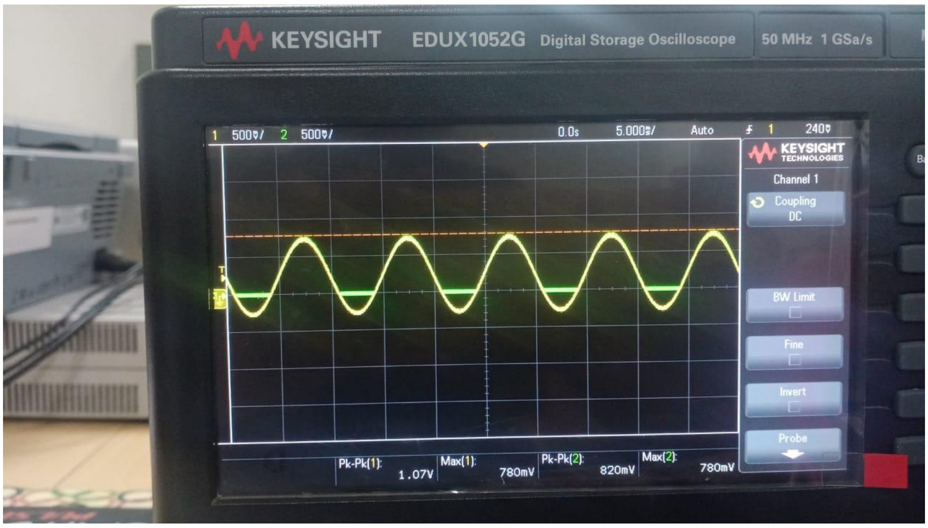
$$= \frac{A}{2 R_2 C} t \quad \text{Triangular waves.}$$

4) Precision half-wave Rectifier:



a)

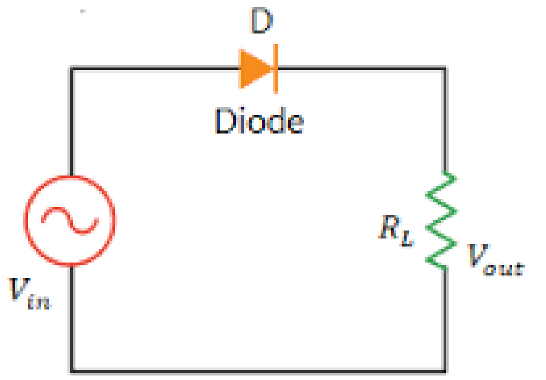

KEYSIGHT EDUX1052G Digital Storage Oscilloscope 50 MHz 1 GSa/s
X1: 0.0V
X2: 2.49375V
Y1: 3.08125V
Y2: 779.75mV
ΔX: +2.49375V
ΔY(2): -2.30150V
Cursors
Mode Manual
Cursors Y1
Units


KEYSIGHT EDUX1052G Digital Storage Oscilloscope 50 MHz 1 GSa/s
Channel 1
Coupling DC
BW Limit
Fine
Invert
Probe
Pk-Pk(1): 1.07V
Max(1): 780mV
Pk-Pk(2): 820mV
Max(2): 780mV


KEYSIGHT EDUX1052G Digital Storage Oscilloscope 50 MHz 1 GSa/s
Channel 2
Coupling DC
BW Limit
Fine
Invert
Probe
Pk-Pk(1): 1.05V
Max(1): 760mV
Pk-Pk(2): 800mV
Max(2): 780mV

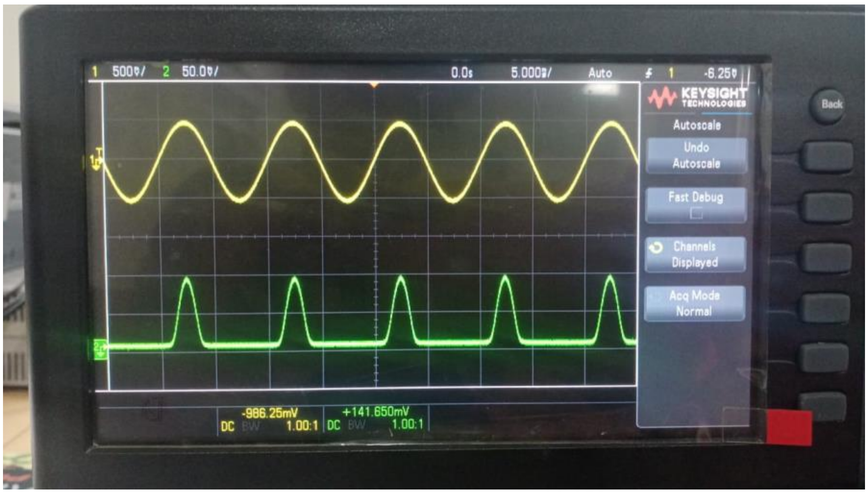
b)

when we use normal rectifier:

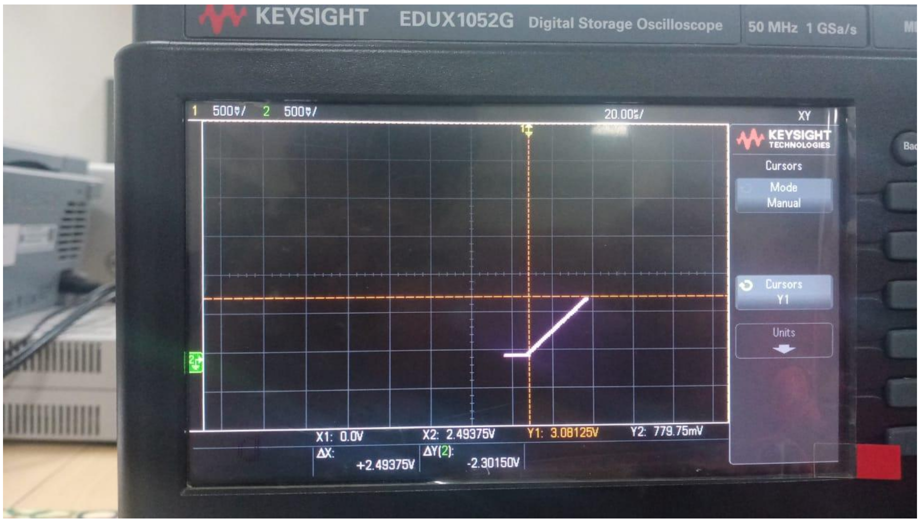


Simple Half Wave Rectifier circuit diagram

How2Electronics



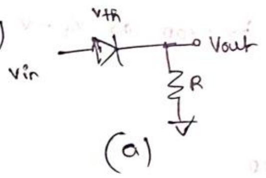
With op-Amp circuit:

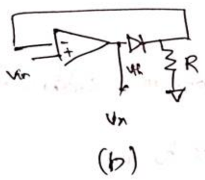


REASON:-

(4)

(b)





virtual short

in +ve cycle (vin > 0)

↳ The diode will always remain in forward bias even if vin < Vth due to

∴ Amplification at voltage vx.

in -ve cycle (vin < 0)

always in Reverse bias.

∴ ~~Vth doesn't~~ Till vth the circuit will be off in circuit (a)

But in circuit (b) it will not.

∴ It is a precise-rectifier.

These op-amp based rectifiers are better than diode and resistor based rectifiers. Op-amp-based rectifiers are better in terms of accuracy, precision, speed, input impedance, temperature stability, and linearity. Conventional diode-based rectifiers have a voltage drop across the diode, typically around 0.7 volts for silicon diodes. In these rectifiers, the output waveform has a lower amplitude due to the cut in voltage of the diode.

Op-amp rectifiers, on the other hand, can achieve nearly zero voltage drop during rectification. The diode acts as a DC voltage source with reversed polarities, resulting in a decreased output sinusoid amplitude. In contrast, the Op Amp-based rectifier circuit behaves differently. When the input sinusoid is positive, the Op Amp amplifies it, causing the diode to be forward biased and act as a short circuit.

As a result, the output voltage equals the input voltage due to the virtual short between the Op Amp's input terminals. Conversely, when the input sinusoid is negative, the diode is reverse biased and acts as an open circuit.