

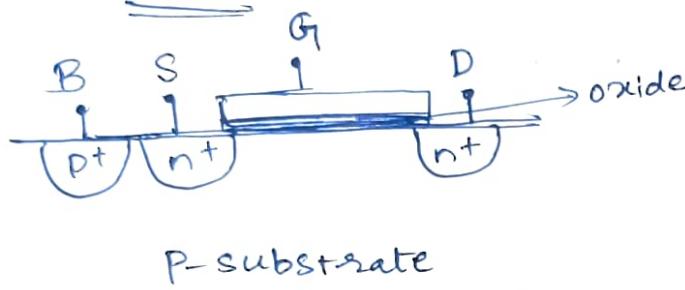
# AEC - Assignment-3

## 1. Region of operation

The different regions of operations of NMOS and PMOS are:

- (I) cut-off
- (II) saturation
- (III) sub threshold
- (IV) triode region

For NMOS:



(I) cut-off region:

$$V_{GS} < V_{TH} \quad \& \quad V_{DS} > 0,$$

When voltage of Gate w.r.t Source less than  $V_{TH}$  voltage of threshold mosfet is in off-state because there no much free  $e^-$  to conduct current and no sufficient electric field to create charge carriers and high resistance in channel.

(III) Sub-threshold region:

$$V_{GS} \approx V_{TH} \quad \& \quad V_{DS} > 0$$

In this region the no. of  $e^-$  b/w source & drain increases it is very close to form inversion layer. In this region mosfet acts as diode

$$I_D \approx I_{SD} \left( \frac{V_{GS} - V_{TH}}{nV_T} \right)$$

(II) Saturation region:-

$$V_{GS} > V_{TH}$$

$$V_{DS} > V_{GS} - V_{TH}$$

(IV) Triode region:-

$$V_{GS} > V_{TH}$$

$$V_{GS} - V_{TH} > V_{DS}$$

$I_{DS}$  → current flowing from drain to source  
Source to drain

$V_{DS}$  → Voltage of Drain w.r.t Source

$V_{GS}$  → Gate Voltage w.r.t Source

$V_{TH}$  → (V<sub>th</sub>)<sup>voltage</sup> threshold is +ve

PMOS:

$V_{th}$  is -ve

$V_{SG}$  → Source Voltage w.r.t. gate

$V_{SD}$  → Source Voltage w.r.t Drain

$V_{GS}, V_{DS}$  is -ve

$I_{SD}$  → current flowing from ~~source~~ source to Drain

(I) Cut off:  $|V_{SG}| < |V_{th}|$ ,  $I_D \approx 0$

(II) Saturation:  $|V_{SG}| > |V_{th}|$ ,  $V_{SG} + V_{th} < V_{SD}$

(III) Subthreshold:

→  $V_{GS} \approx V_{TH}$  but significant holes are attracted

→ Acts as diode

(IV) Triode region:-

$|V_{SG}| > |V_{th}|$ ,  $V_{SG} + V_{th} > V_{SD}$

Drain current equations:

PMOS:

$$\text{cutoff} \Rightarrow I_{SD} = I_0 e^{\left(\frac{V_{SG} + V_{th}}{nV_T}\right)} \approx 0$$

Saturation  $\Rightarrow$

$$I_{SD} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{SG} + V_{th})^2 (1 + \lambda_p V_{SD})$$

$\downarrow$   
Channel length modulation

triode:

$$I_{SD} = \mu_n C_{ox} \frac{W}{L} \left( (V_{SG} + V_{th}) V_{SD} - \frac{V_{SD}^2}{2} \right)$$

NMOS

$$\text{cutoff: } I_{DS} = I_0 e^{\left(\frac{V_{GS} + V_{th}}{nV_T}\right)} \approx 0$$

Saturation:

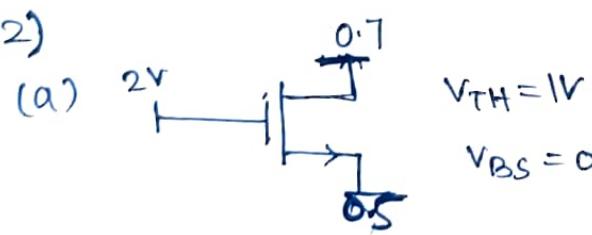
$$I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda_n V_{DS})$$

$\downarrow$   
Channel length modulation

triode  $\Rightarrow$

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left( (V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

1.2)



$$\therefore V_{DS} < V_{GS} - V_{TH}$$

$$V_{GS} = 2 - 0.5 = 1.5V$$

$$V_{GS} - V_{TH} = 1.5V - 1V$$

$$V_{GS} - V_{TH} = 0.5V$$

$$V_{DS} = 0.2V$$

$\therefore$  MOSFET is in Triode region.

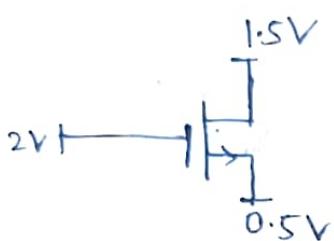
$$I_D = \frac{1}{2} \ln \left( \cos \frac{W}{L} \right) \left[ (V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$I_D = 300 \times 10^6 \times \frac{2}{10} \left[ 0.5 \times 0.2 - \frac{0.04}{2} \right]$$

$$I_D = 6 \times 10^4 [0.1 - 0.02]$$

$$I_D = 48 \text{ mA}$$

(b)



$$V_{TH} = 1V, V_{BS} = 0$$

$$V_{TH_0} = 1V$$

$$V_{GS} = 1.5V$$

$$V_{DS} = 1V$$

$$V_{GS} - V_{TH} = 0.5V$$

$$V_{DS} > V_{GS} - V_{TH}$$

$$> 0.5$$

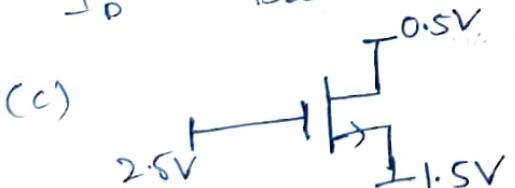
Mosfet is in saturation.

$$I_D = \frac{1}{2} \ln \left( \cos \frac{W}{L} \right) \left( (V_{GS} - V_{TH})^2 \right) V_{DS}$$

$$I_D = \frac{1}{2} \times 300 \times 10^6 \times \frac{2}{10} (0.5)^2 \times \frac{1}{10}$$

$$I_D = 3 \times 10^4 \times 25 \times 10^{-2}$$

$$I_D = 75 \text{ mA}$$



$$V_{TH} = 1V, V_{BS} = 0$$

$$V_{TH_0} = 1V$$

$$V_{DS} = -1V$$

w.r.t. Drain & Source are symmetric in Mosfet

$$-V_{DS} = 1V \text{ (after Interchange)} \quad V_{SD} = -V_{DS}$$

$$V_{GDS} = 2 - 0.5 = 1.5$$

$$V_{GDS} - V_{TH} = 1.5 - 1 = 0.5V$$

$$\therefore V_{DS} > V_{GDS} - V_{TH}$$

Saturation region

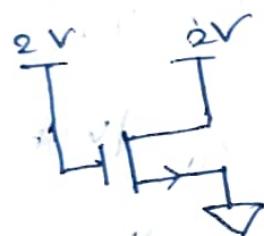
$$I_D = \frac{1}{2} \ln(C_{ox} \frac{W}{L}) (V_{GDS} - V_{TH})^2$$

$$I_D = \frac{1}{2} \times 3 \times 10^2 \times 10^{-6} \times \frac{2 \mu}{1 \mu} (0.5)^2$$

$$I_D = 750 \mu A$$

(d)

given,



$$V_{THN} = V_{THNO} = 1V$$

$$V_{GDS} - V_{TH} = 2 - 1 = 1V$$

$$V_{GDS} = 2 - 0 = 2V$$

$$V_{DS} = 2 - 0 = 2V$$

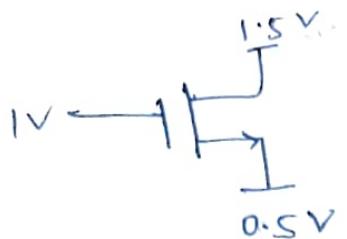
Mosfet is saturation

$$I_D = \frac{1}{2} \times 3 \times 10^2 \times 10^{-6} \times \frac{2 \mu}{1 \mu} (1)^2$$

$$I_D = \frac{3}{2} \times 10^{-4} \times (1)^2 = 1.5 \mu A$$

$$I_D = 300 \mu A$$

e)



$$V_{THN} = 1V = V_{THN_0}, V_{BS} = 0$$

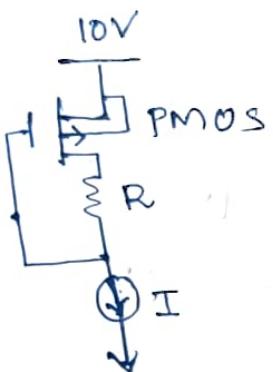
$$V_{GDS} = 1 - 0.5 \\ = 0.5V$$

$V_{GDS} < V_{TH}$   $\therefore$  MOSFET is in cutoff region

$$I_D \approx 0$$

\* Not exactly zero current very small current which is exponentially dependent on  $V_{GDS}$

1.3 (a)



$$V_D - V = IR$$

$$V_G = V$$

For PMOS to be in saturation

$$V_{SD} \geq V_{SG} - |V_{THP}|$$

$$V_S - V_P \geq V_S - V_{G1} - |V_{THP}|$$

$$V_D \leq V_{G1} + |V_{THP}|$$

$$|V_{THP}| \geq V_D - V_G$$

$$\geq IR + V_D - V$$

$$|V_{THP}| \geq IR$$

(b) (i)  $R = 0\Omega$ 

$$|V_{THP}| = 1V \quad k_p = 0.2mA/V^2 \quad I_d = 0.1mA$$

PMOS is in saturation

$$I_D = \frac{1}{2} k_p C_{ox} \frac{W}{L} (V_{SG} - V_{TH})^2$$

$$10^{-4} = \frac{1}{2} \times 0.2 \times 10^{-4} (V_{SG} - 1)^2$$

$$V_{SG1} - 1 = 1$$

$$V_{SG1} = 2V$$

Since  $R=0$   $V_D - V = IR \Rightarrow V_D = V = V_G$

$$V_{SG1} = V_{SD} = 2V$$

(ii) For  $R = 10k\Omega$

$$|V_{TH}| = 1V$$

$$J = 0.1m \quad R = 10k\Omega$$

$$I \times R = 1 = |V_{THP}|$$

For Mosfet Saturation

$$|V_{THP}| \geq 1 \Rightarrow \text{saturation}$$

$$I_D = \frac{1}{2} k_f (V_{SG1} - |V_{TH}|)^2$$

$$10^{-4} = \frac{1}{2} \times 2 \times 10^{-4} (V_{SG1} - |V_{THP}|)^2$$

$$(V_{SG1} - 1)^2 = 1 \Rightarrow V_{SG1} = 2V$$

$$V_S - V_G = 2V$$

$$V_S - V = 2V$$

$$V = 10 - 2 = 8V$$

$$V_D = IR + V$$

$$V_D = 10^{-4} \times 10^4 + 8 = 9V$$

$$V_{SD} = V_S - V_D = 10 - 9 = 1V$$

$$V_{SD} = 1V$$

(iii)  $R = 100k\Omega$   $I_d = 0.1 \times 10^{-3} A$   
current is not negligible so  $q_1 + q_2$  is not in cut off region.

$$|V_{THN}| = 1V < V_{DG1} = (10^4)(10^5)$$

$$V_{DG1} = 10V \Rightarrow V_D = V_G + 10$$

$I < 10$

Mosfet is in triode region

$$I_d = 10^{-4} = 0.2 \times 10^{-3} \left[ (V_{SG} - |V_{TH}|) V_{SD} - \frac{V_{SD}^2}{2} \right]$$

$$\frac{2}{2} = V_{SD} \left[ 2(V_{SG} - |V_{TH}|) - V_{SD} \right]$$

$$= V_{SD} [2(V_{SG} - V_{SD}) - 2|V_{TH}| + V_{SD}]$$

$$= V_{SD} [2V_{DG} + V_{SD} - 2|V_{TH}|]$$

$$\frac{2}{2} = V_{SD} [V_{SD} + 18]$$

$$\Rightarrow V_{SD} + 18V_{SD} - 1 = 0$$

$$V_{SD} = \frac{-18 + \sqrt{328}}{2}$$

$$\text{as } V_{SD} > 0$$

$$V_{SG} = V_S - (V_D - 10)$$

$$= 2V_S - V_D$$

$$= 10 + V_{SD}$$

$$V_{SG} = 20 + \frac{\sqrt{328} - 18}{2}$$

$$-V_{G1} = \frac{18 \pm \sqrt{328}}{2}$$

(.4) a) Region of operation

let's assume it is in saturation.

$$V_{in} = 0.8, V_s = 0$$

$$V_D = 1.8 - I_d(3k)$$

$$I_d = \frac{10 \text{ Cm}^2}{2L} [V_{GS} - V_{TH}]^2$$

$$= \frac{10^{-4}}{2} \times 10 [0.3]^2$$

$$= \frac{90}{2} \times 10^{-6} = 4.5 \text{ mA}$$

$$V_D = 1.8 - (4.5 \times 10^{-3})(s)$$

$$V_D = 1.8 - 0.135 \Rightarrow V_D = 1.665$$

$$V_{DS} > V_{G_S} - V_{TH}$$

$\Rightarrow$  The mosfet is in saturation

$\Rightarrow$  Our assumption is true

(b) Biasing current  $= I_d = 45 \text{ mA}$

$$g_m = \frac{2 I_d}{V_{G_S} - V_{TH}} = \frac{2 \times 45}{0.3} = \frac{90}{3} \times 10^{-5}$$

$$g_m = 3 \times 10^{-4} \text{ Simons}$$

(c) Since MOSFET is in saturation then, w.r.t,

$$V_{G_S} > V_{TH} \quad V_{G_S} > 0.5V$$

$$V_{DS} > V_{G_S} - V_{TH}$$

$$V_{G_S} < V_{DS} + V_{TH}$$

$$V_{G_S} - V_{TH} < V_{DD} - I_D R$$

$$\rightarrow V_{G_S} - V_{TH} < 1.8 - \frac{R}{2} \ln(\text{Con}_L \frac{W}{L}) (V_{G_S} - V_{TH})^2$$

$$\rightarrow (V_{G_S} - V_{TH}) + \frac{R}{2} \ln(\text{Con}_L \frac{W}{L}) (V_{G_S} - V_{TH})^2 - 1.8 < 0$$

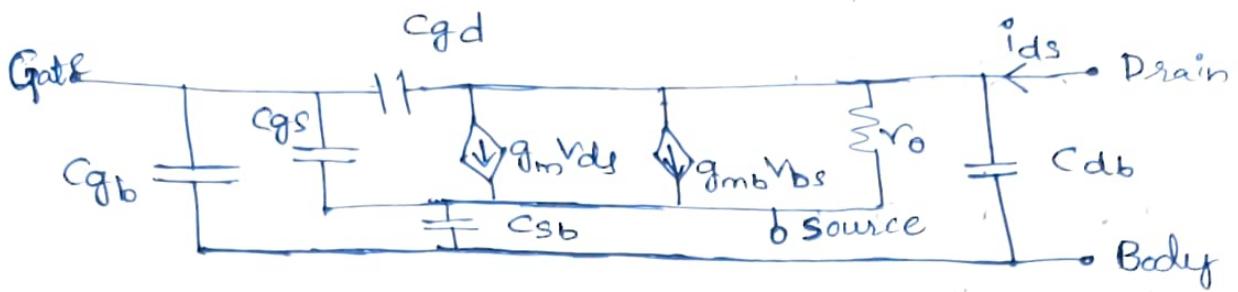
$$\rightarrow V_{G_S} < V_{TH} + \left( \frac{\sqrt{1 + 4 \times 1.8 \times R \ln(\text{Con}_L \frac{W}{L})}}{2 \times R \ln(\text{Con}_L \frac{W}{L})} \right) < 0.5 + 0.825$$

$$\rightarrow V_{G_S} < 1.325$$

$$\rightarrow \boxed{0.5 < V_{G_S} < 1.325}$$

II

(2.1)

Complete Small-Signal model of <sup>(W)</sup> NMOS :-In saturation

$$C_{GS} \approx \frac{2}{3} C_{oN} W \cdot L + C_{GSO} \cdot W$$

$\underbrace{\hspace{2cm}}$  Channel Part       $\underbrace{\hspace{2cm}}$  Overlapping Part

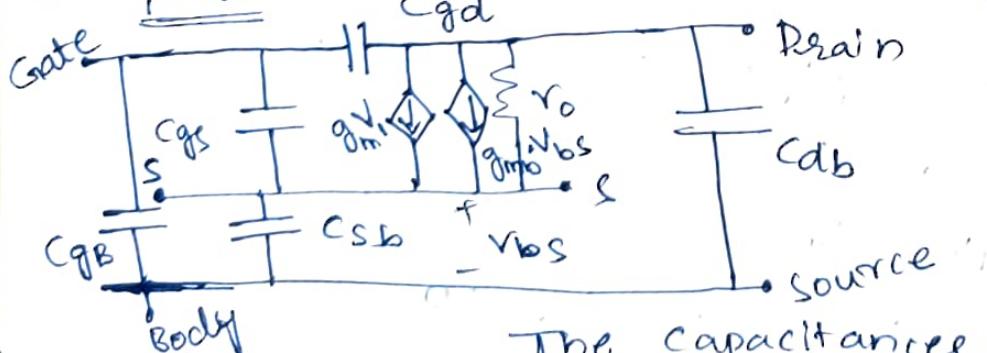
$$C_{GD} \approx C_{GDO} \cdot W$$

$$C_{GB} \approx C_{GBO} \cdot L \approx \text{negligible}$$

$$C_{BS} = \frac{C_j \cdot A_j}{\left(1 + \frac{V_{SB}}{P_B}\right)^{M_j}} + \frac{C_{JSW} \cdot P_s}{\left(1 + \frac{V_{SB}}{P_{BSW}}\right)^{M_{JSW}}} \quad \begin{cases} A_j = W \cdot L_s \\ P_s = 2L_s + W \end{cases}$$

$$C_{DB} = \frac{C_j A_j}{\left(1 + \frac{V_{DB}}{P_B}\right)^{M_j}} + \frac{C_{JS} W \cdot P_D}{\left(1 + \frac{V_{DB}}{P_{BSW}}\right)^{M_{JSW}}}$$

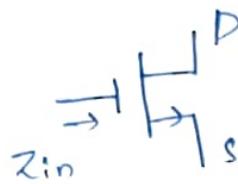
due to Area      due to Perimeter  
Parallel plate      due to fingers.

(ii) PMOS

The capacitances are same as above

(2.2)

(i)

WKT,  $I_{Gate} \approx 0$ 

$$Z_{in} = \frac{V_{G1}}{I_G} \approx \infty$$

considering  $V_{BS}=0$ 

Now let us ground the gate and source and place a voltage source at Drain

Small Signal

by KVL

$$Z_{in} = \frac{V}{I_D}$$

$$= r_0$$

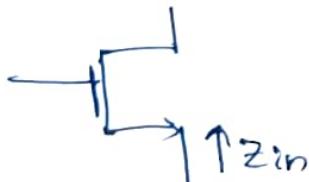
$$0 - V_i + 0 = 0$$

$$V_i = 0$$

The complete current goes into  $V_o$  as the current through it  
Source will have zero current through it

$$V_{GS} = 0$$

(iii)



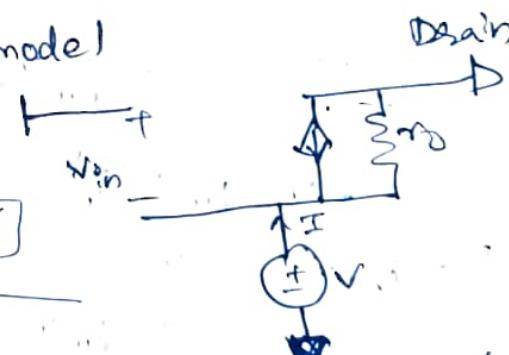
small signal model

By loop law,  $V_{in} + V = 0$ 

$$V_{in} = -V$$

$$Z_{in} = \frac{V}{I} \Rightarrow \text{we get}$$

$$\frac{V}{r_0} = I - g_m V$$



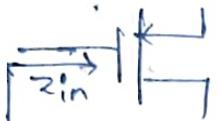
I splits into 2 terminals

$$I - g_m V = \frac{V}{r_0} \Rightarrow V(g_m + \frac{1}{r_0}) = I$$

$$g_m t + \frac{1}{r_o} = \frac{I}{V}$$

$$\boxed{\frac{V}{I} = \frac{r_o}{1 + g_m r_o} = Z_{in}}$$

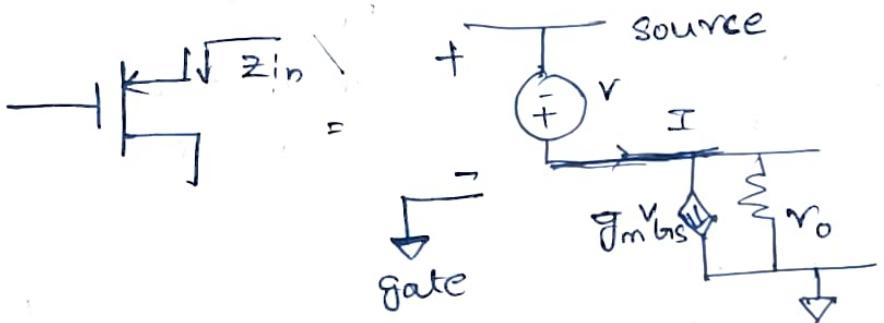
(iv) Now let us replace PMOS by its  
small signal model



as the current through gate is always zero

$$\boxed{Z_{in} = \frac{V}{0} = \infty}$$

(v)



$$V_{SG} = V, \Rightarrow Z_{in} = \frac{V}{I}$$

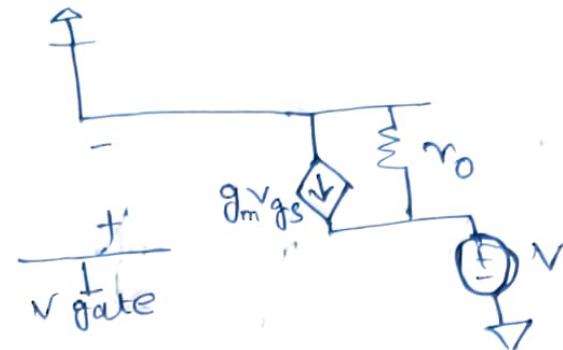
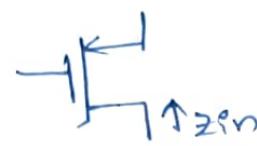
$$\text{wkt, } V_{SD} = V$$

$$\frac{V}{r_o} = I - g_m V_{GS}$$

$$V(g_m t + \frac{1}{r_o}) = I$$

$$\boxed{Z_{in} = \frac{r_o}{1 + g_m r_o}}$$

(V<sub>g</sub>)



$$V_g = 0 = V_s$$

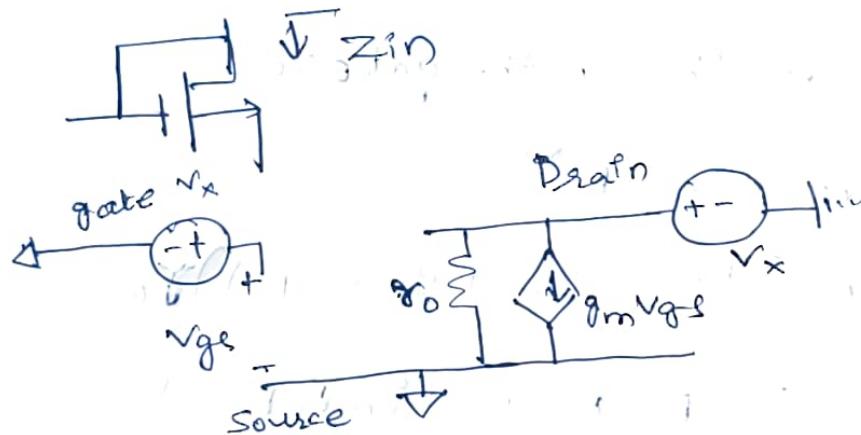
$$V_{gs} = 0$$

$$g_m \cdot V_{gs} = 0$$

The complete current  $I_o$  flows through the  $V_o$

$$\boxed{Z_{in} = \frac{V}{I} = r_o}$$

(V<sub>x</sub>)



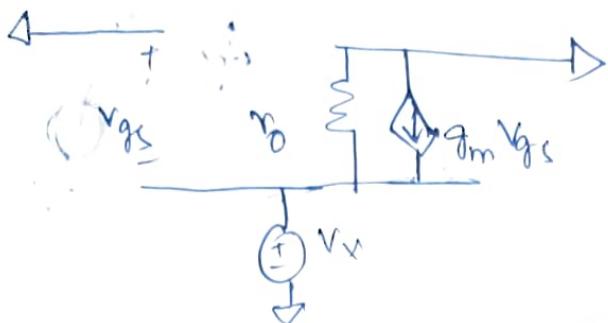
$$I = g_m V_x + \frac{V_x}{r_o}$$

$$V_x (g_m + \frac{1}{r_o}) = I$$

$$\frac{V_x}{I} = \frac{r_o}{1 + g_m r_o}$$

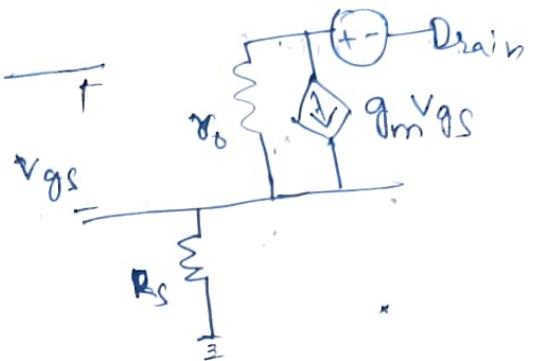
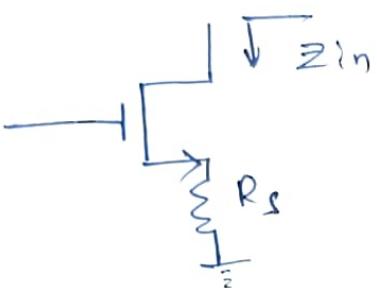
$$\boxed{Z_{in} = \frac{r_o}{1 + g_m r_o}}$$

(N999)



$$I - g_m V_{gs} = \frac{V_x}{R_o} \Rightarrow \boxed{Z_{in} = \frac{R_o}{1 + g_m V_o}} \quad N_x$$

(ix)



The current through the gate  $Z_o$ :

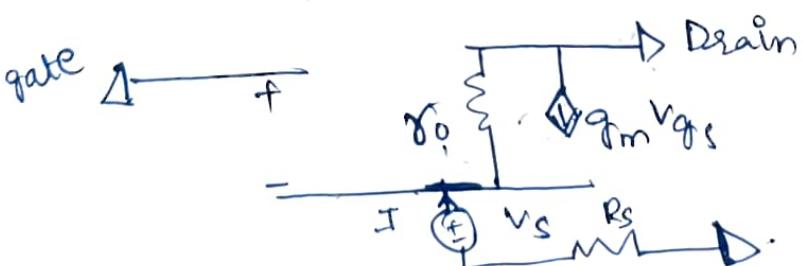
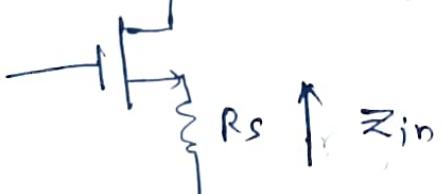
$$V_{gs} = (I)(R_s)$$

$$V_x - IR_s = (I + g_m (IR_s))R_o$$

$$I(R_s + R_o) + I g_m R_o R_s = V_x$$

$$\boxed{\frac{V_x}{I} = R_o (1 + g_m R_s) + R_s}$$

(x)



$$V_x = V_s - I_x R_S$$

$$I_x g_m(V_x) = \frac{V_x}{\tau_0}$$

$$I_x - g_m V_s + I_x g_m R_S = \frac{V_x}{\tau_0}$$

$$I_x (1 + g_m R_S) \cdot g_m V_s = \frac{V_s - I_x R_S}{\tau_0}$$

$$I_x \left( 1 + g_m R_S + \frac{R_S}{\tau_0} \right) = \frac{V_s}{\tau_0} + g_m V_s$$

$$\frac{V_s}{I_x} = \frac{\tau_0 + g_m V_o R_S + R_S}{1 + g_m V_o}$$

$$Z_{in} = \frac{V_s}{I_x} = \frac{\tau_0}{1 + g_m \tau_0} + R_S$$

3.2)

(a)  $V_{DS} = 50 \times 10^3 \text{ V}$

$$V_{TH} = 0.389 \text{ V}$$

$$I_d = 139.6 \times 10^{-6} \text{ A}$$

$$V_{GS} = 0.67 \text{ V}$$
$$1.4 \times 10^{-4} = \frac{IL \cos \omega}{L} \left[ (0.67 - 0.389) 5 \times 10^2 - \frac{25 \times 10^{-4}}{4} \right]$$

$$\approx \frac{IL \cos \omega}{L} (1.425) \times 10^{-2} = 1.4 \times 10^{-4}$$

$$\frac{IL \cos \omega}{L} = \frac{1.4}{1.425} \times 10^{-2} = 1.73 \times 10^{-3}$$

$$IL \cos \omega = 1.73 \times 10^{-3}$$

(b)

- The threshold voltage decreases when the  $V_{DS}$  increases due to Drain induced Barrier lowering
- when drain voltage increases drain depletion region is more increased which Increases the  $\vec{E}$  electric field such that pushes  $e^-$ , resistance decreases
- Thus,  $V_{TH}$  decreases
- higher drain voltage reduces the potential barrier at the source channel junction.
- allowing more  $e^-$  to flow even at lower / same gate voltage

3.3  $V_{TH} = V_{TH_0} + \sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}$

~~if~~

If  $V_{BS} = 0$

$$V_{TH} = V_{TH_0}$$

If  $2V_{BS} = 900mV$ ,  $V_{SB} = -900mV$ .

$$V_{THN} < V_{THN_0}$$

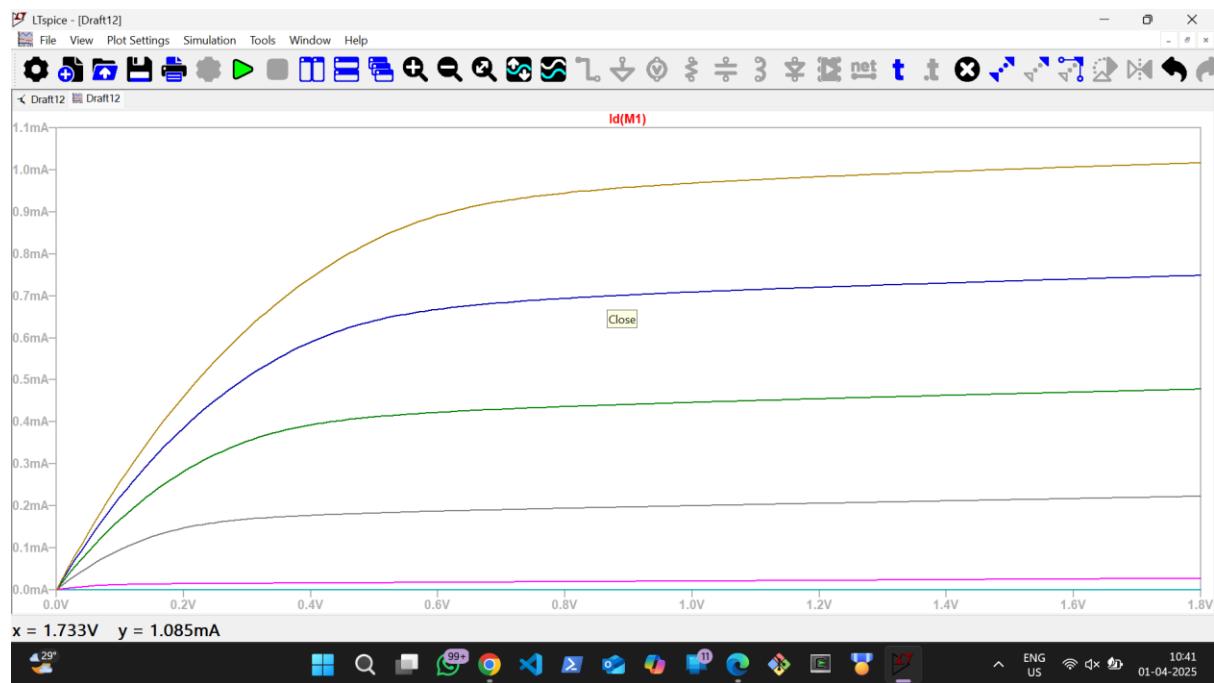
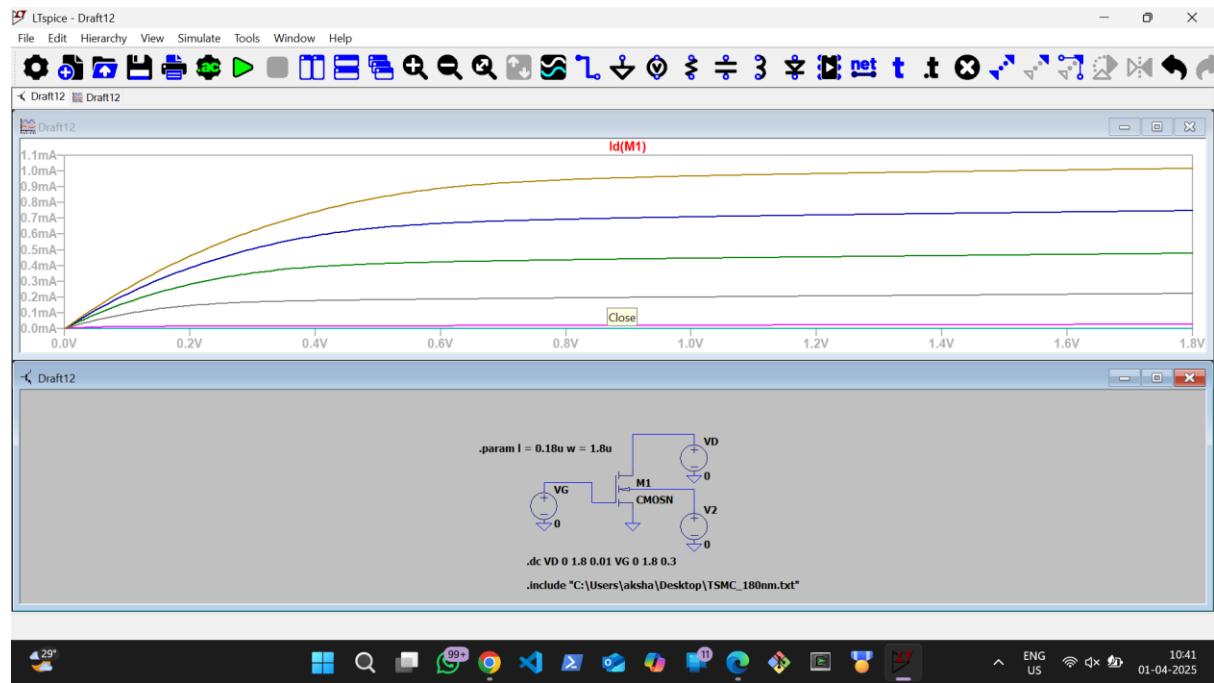
$\therefore$  threshold decreases

If  $V_{BS} = -900mV$

$$V_{THN} > V_{THN_0}$$

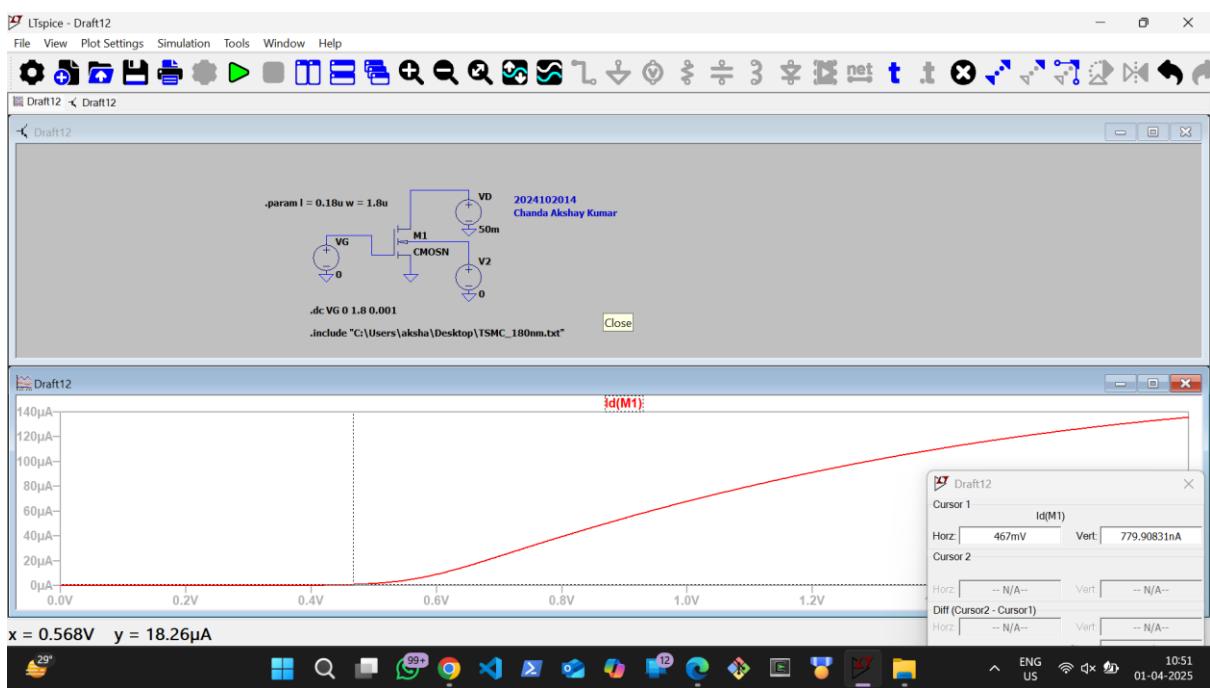
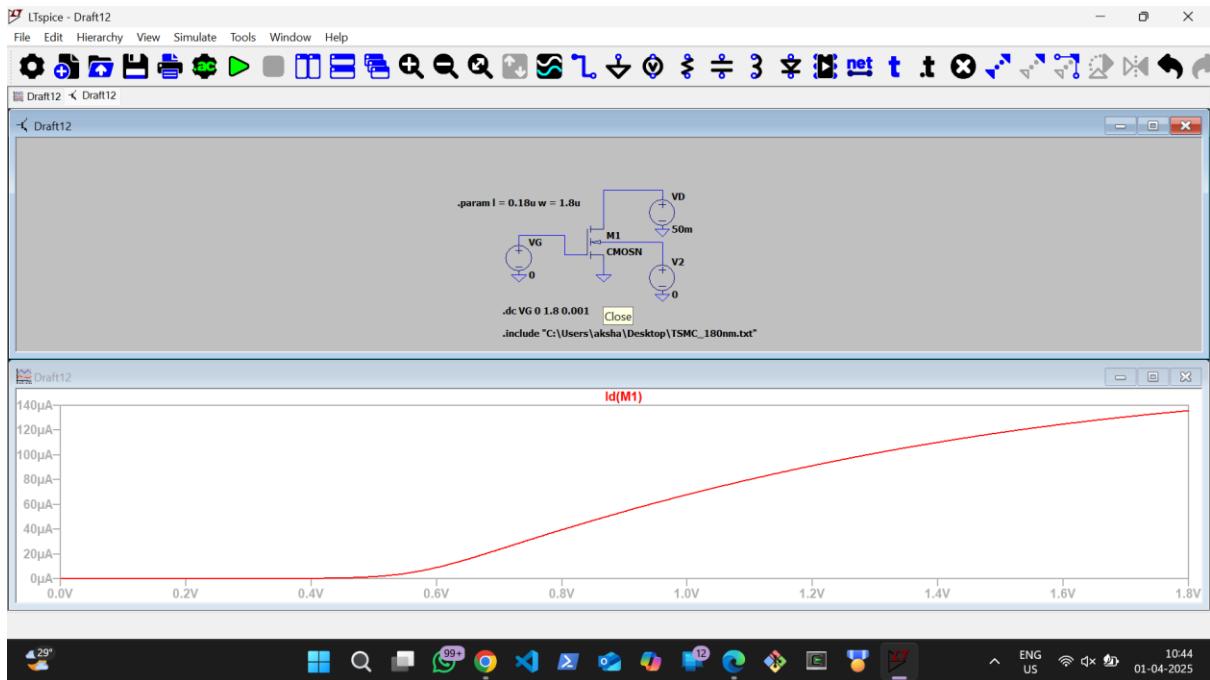
$\therefore$  threshold increases

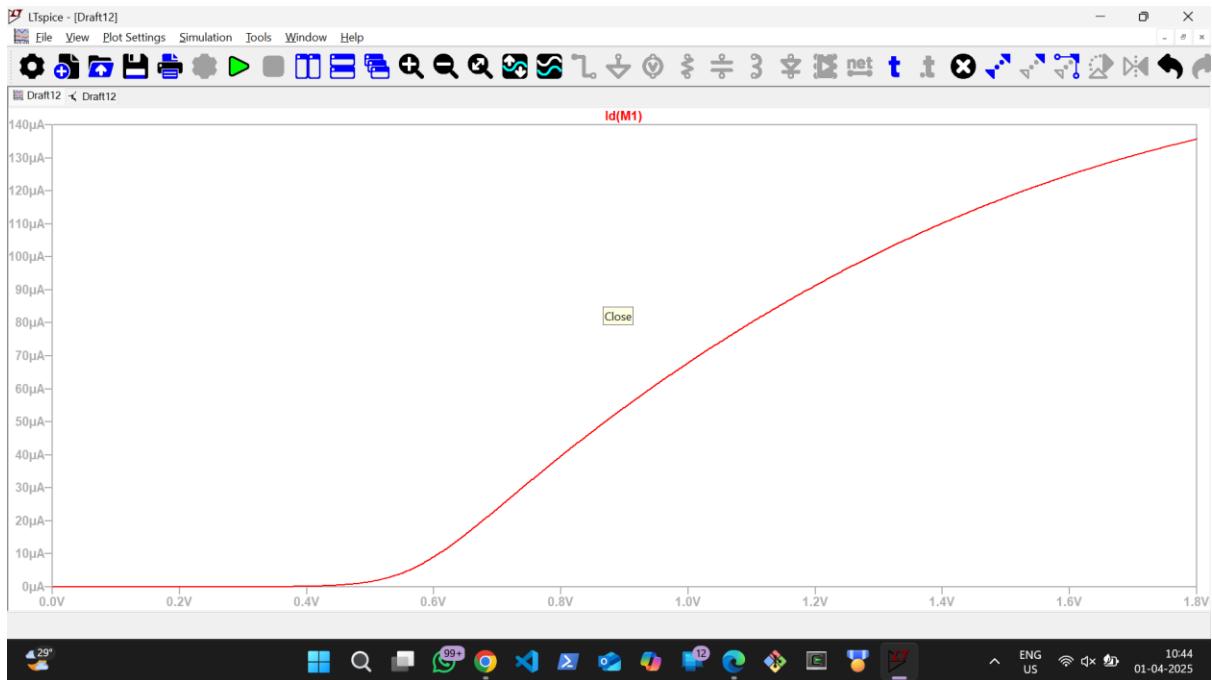
3.1---



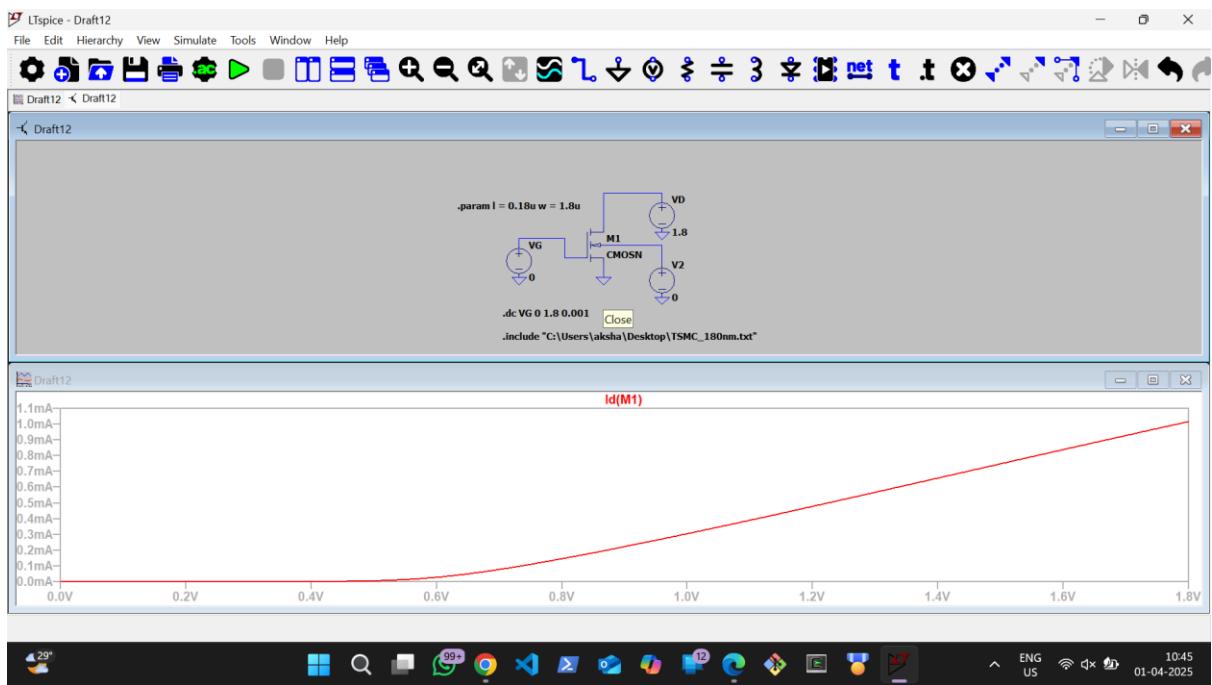
3.2---

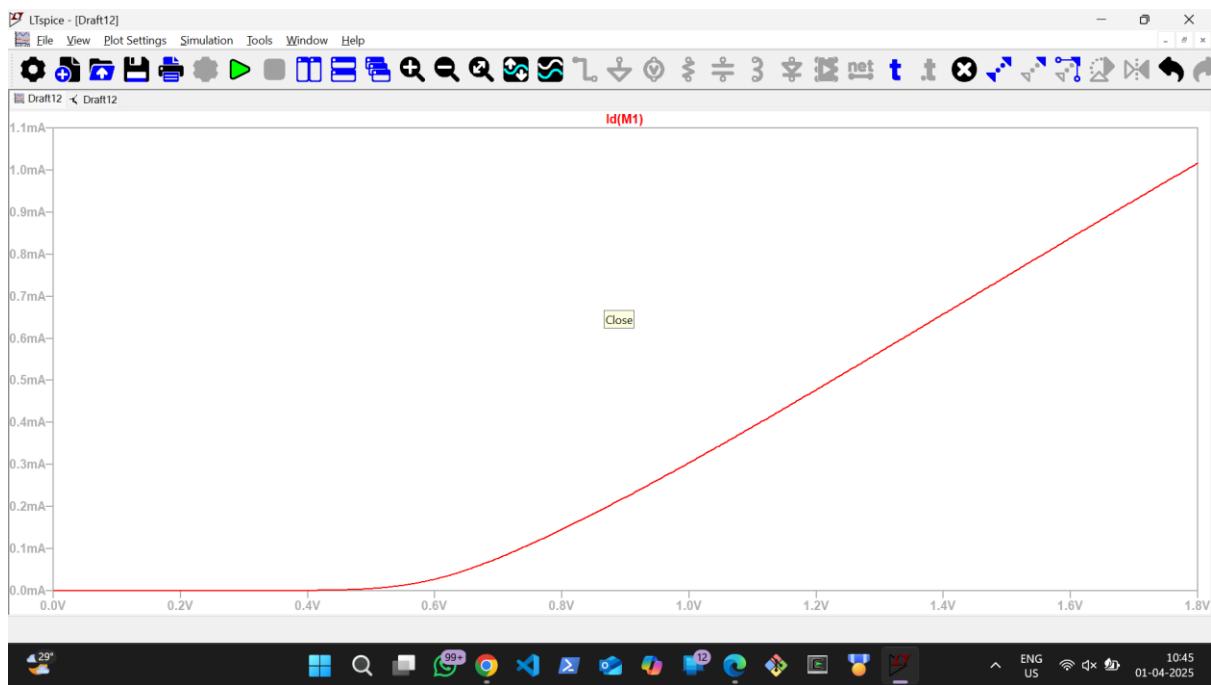
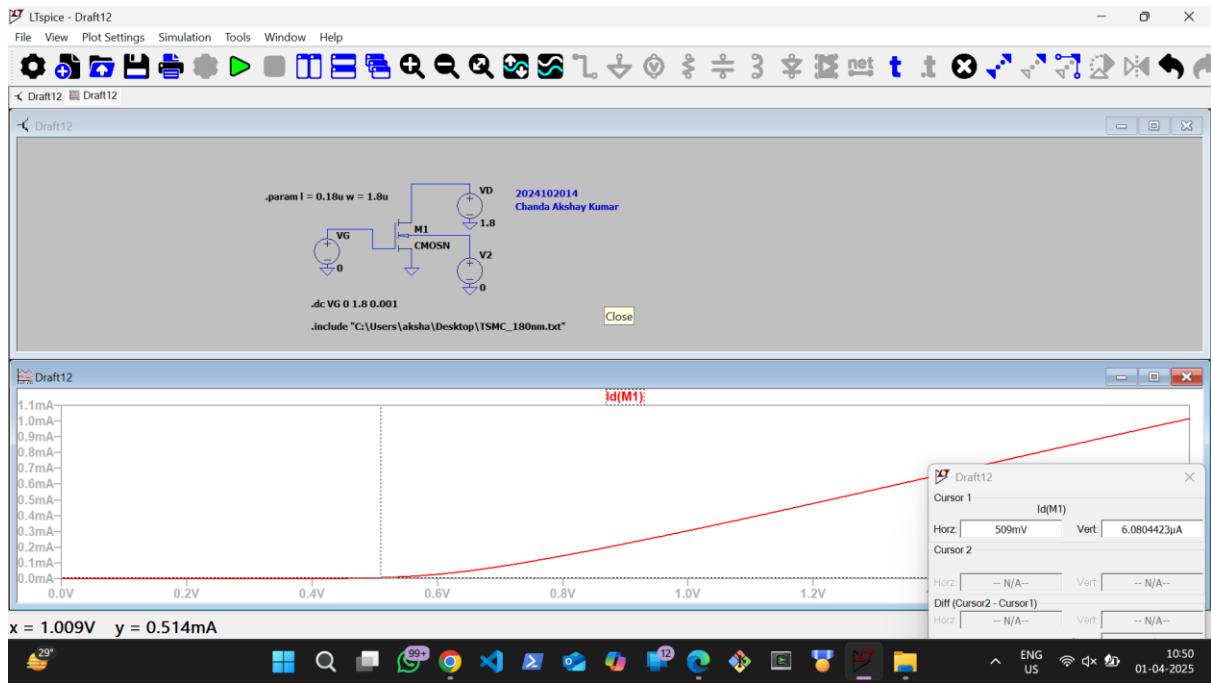
VDS = 50 mV





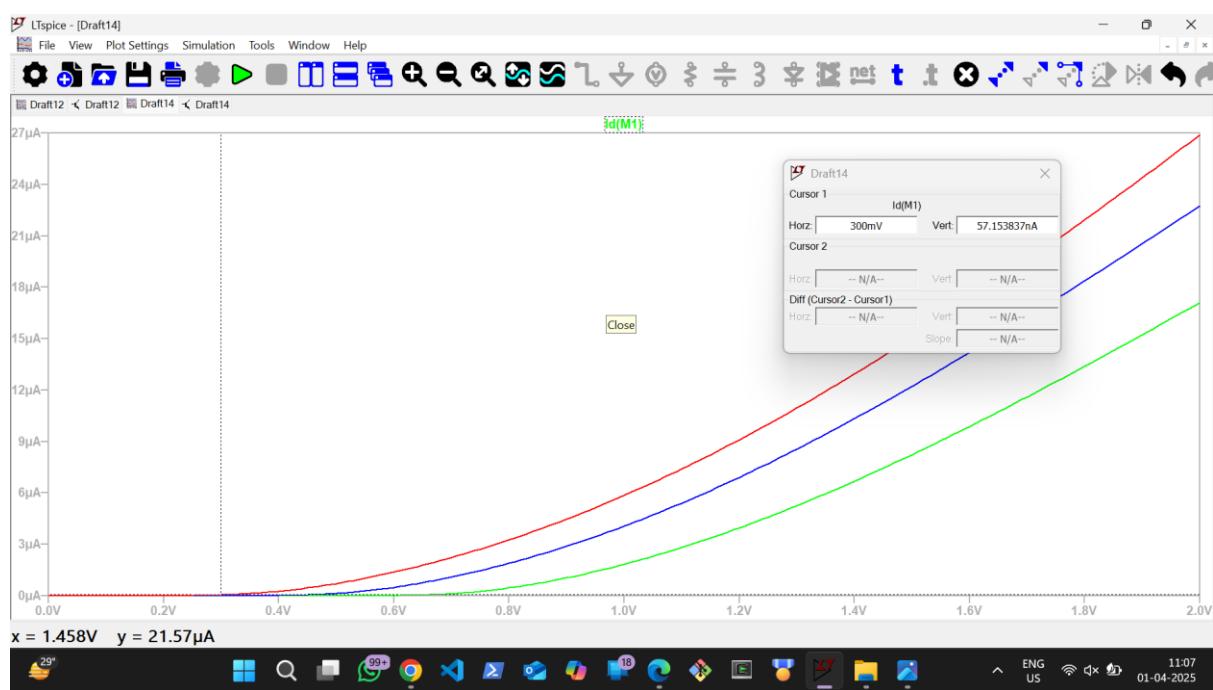
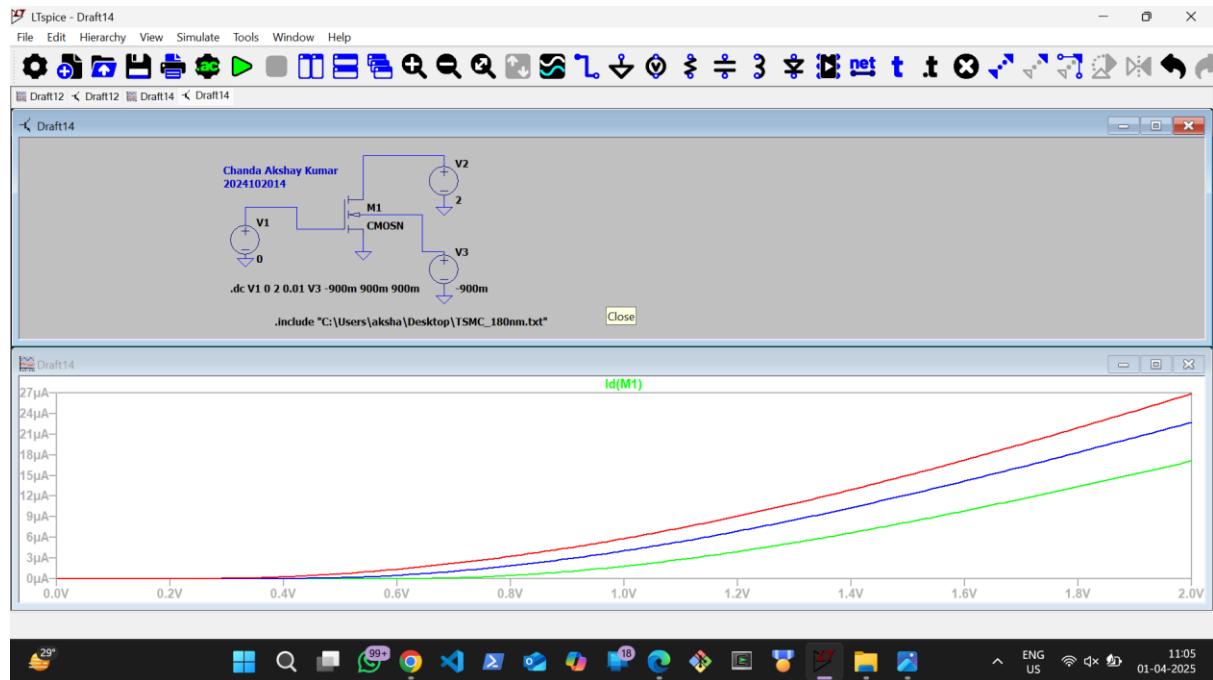
V<sub>DS</sub> = 1.8 V

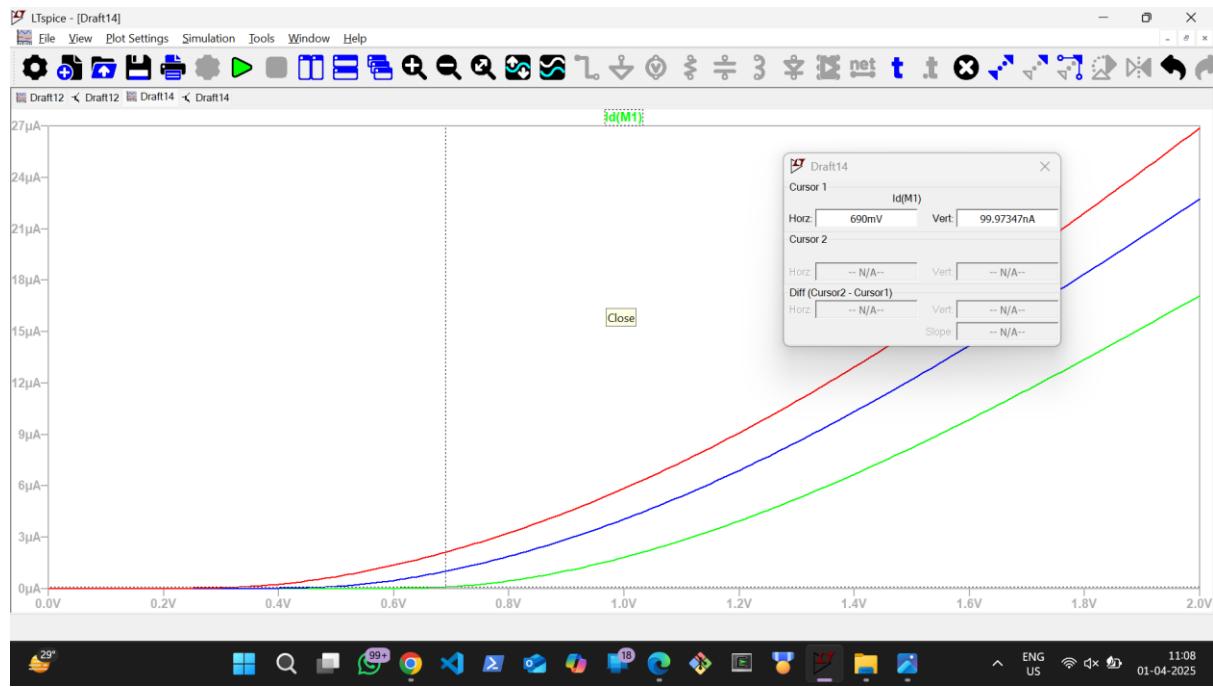
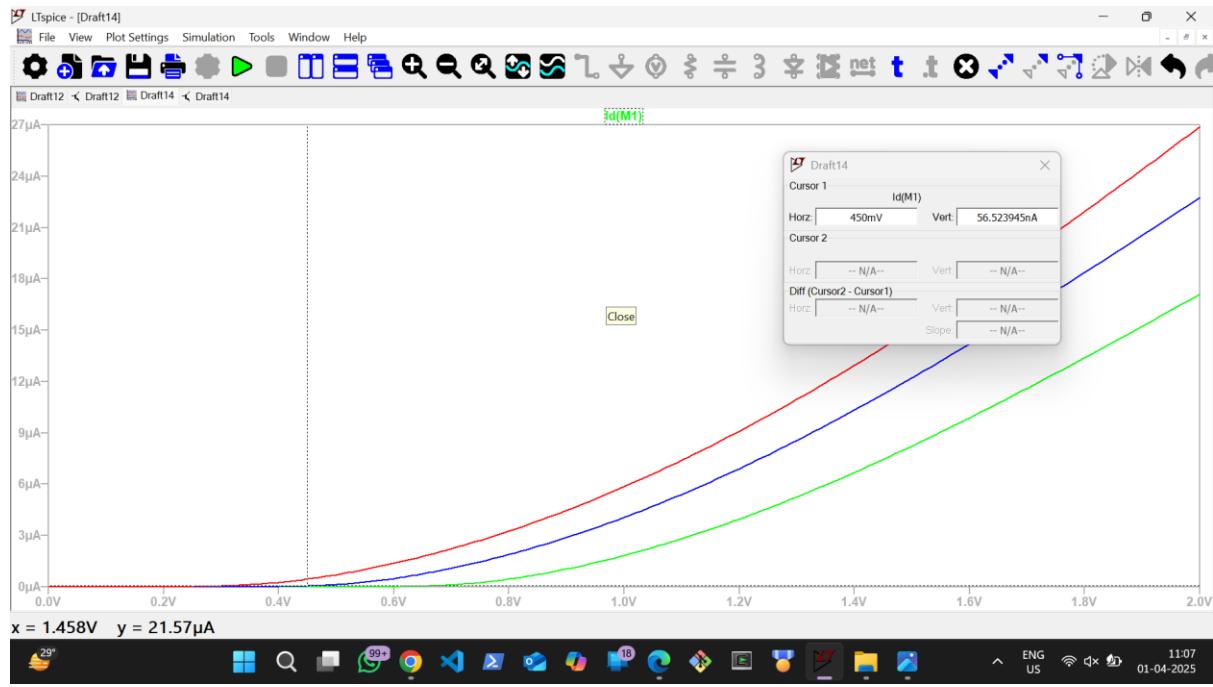




3.3---

NMOS;





PMOS;

