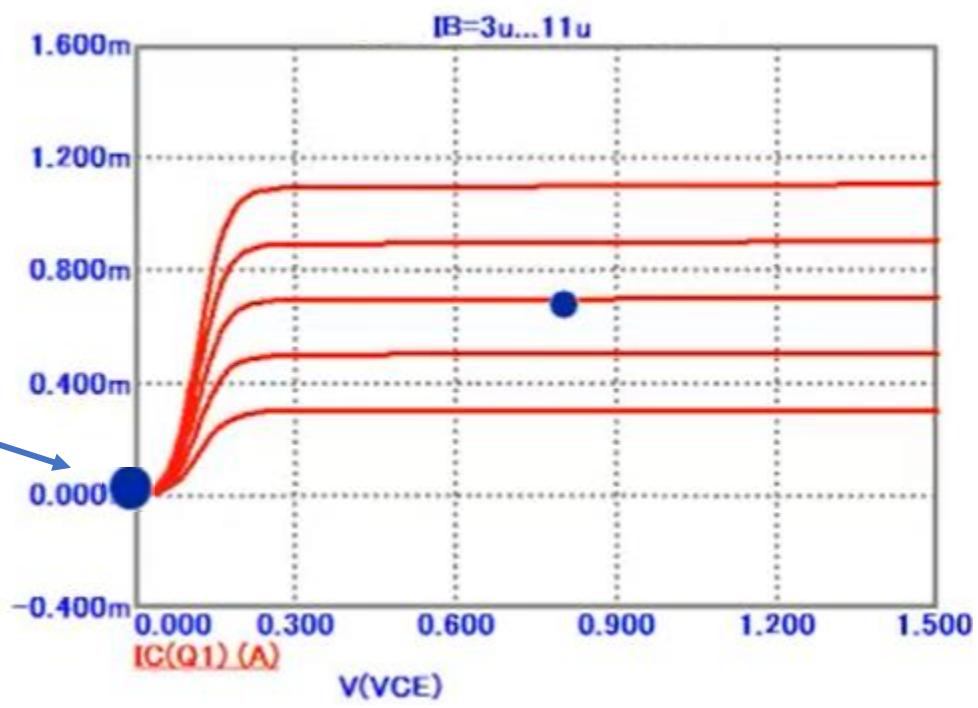
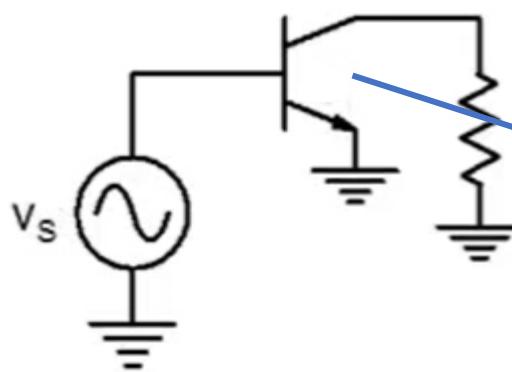
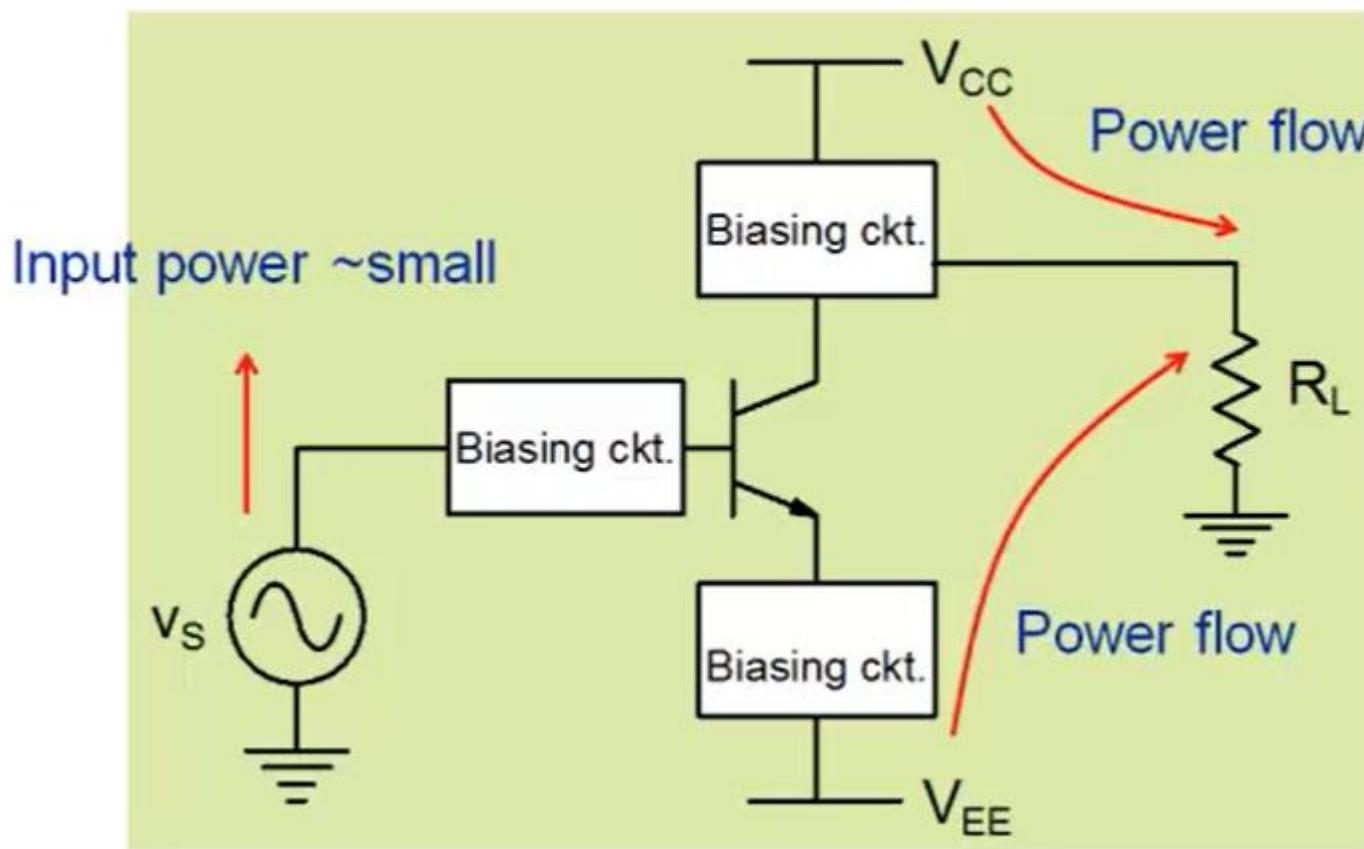


BJT Amplifier Biasing

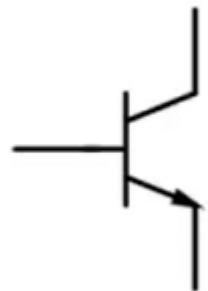
Biasing





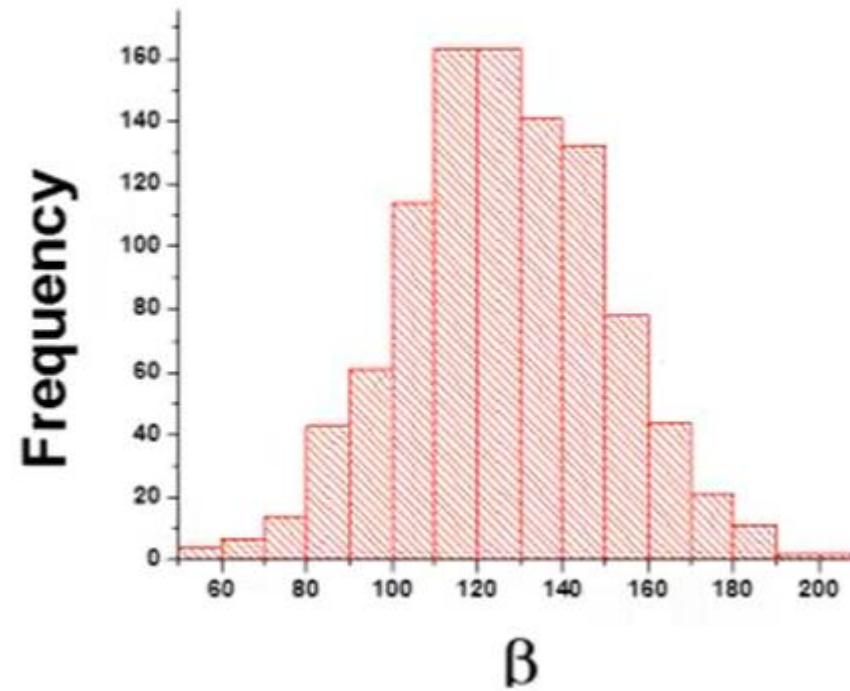
Good Biasing circuit: Bias point is stable against variations in temperature, current gain β , supply voltage etc, power efficient, low cost

Variations to watch out for

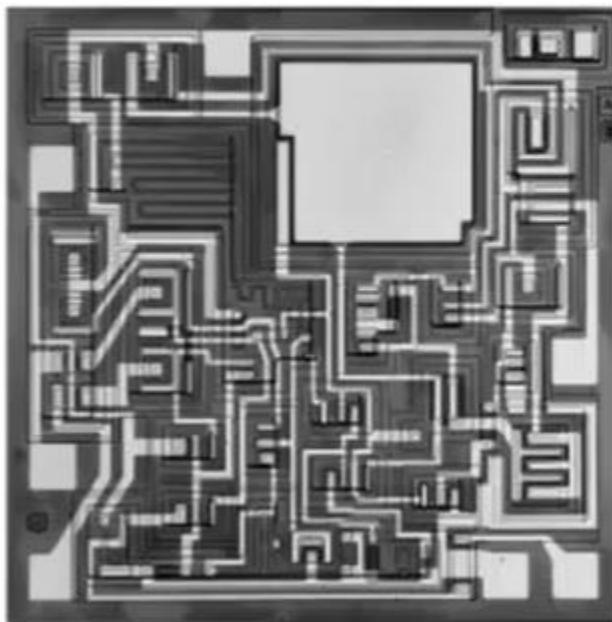
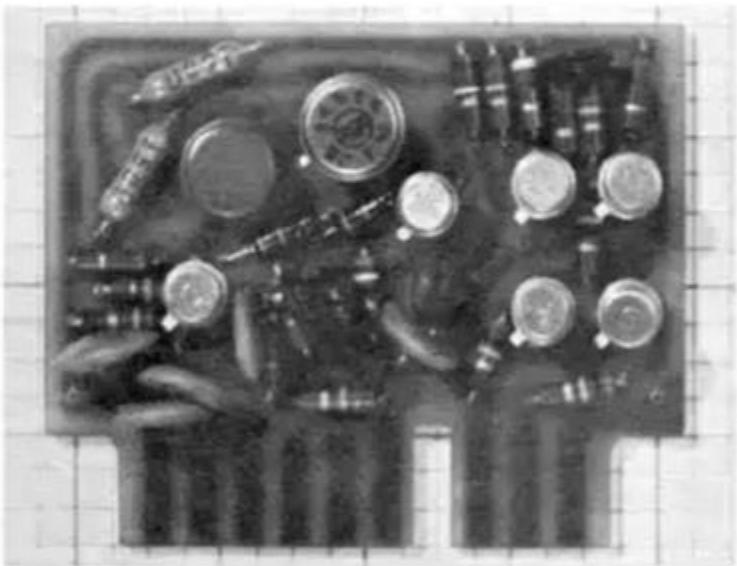


$$(1) \quad \frac{dV_{BE}}{dT} \cong -2mV /^{\circ} C$$

(2)



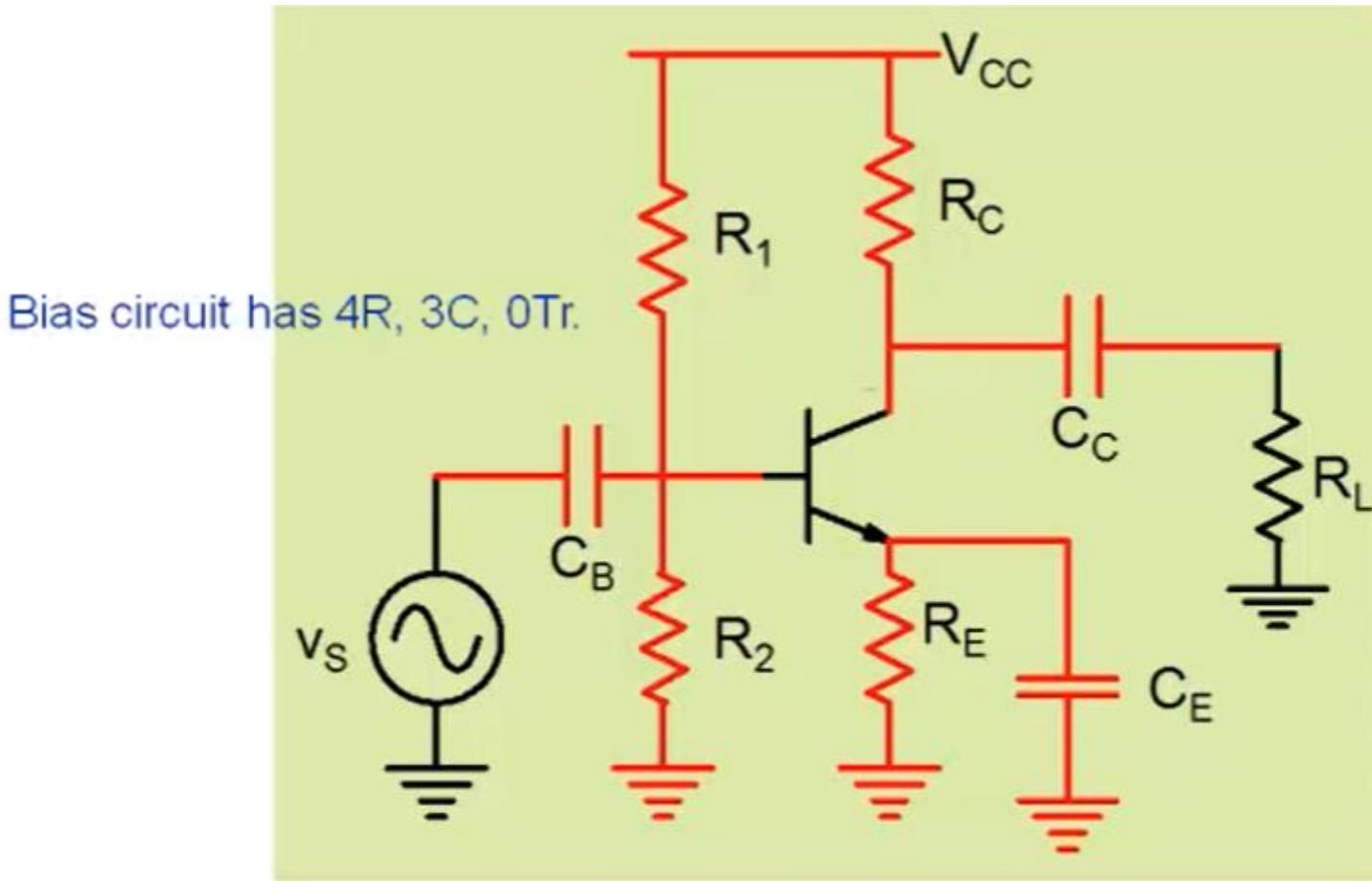
Different biasing circuit for discrete and monolithic (IC) circuit implementation



Resistors and capacitors are 'cheap' and transistors are relatively more expensive.

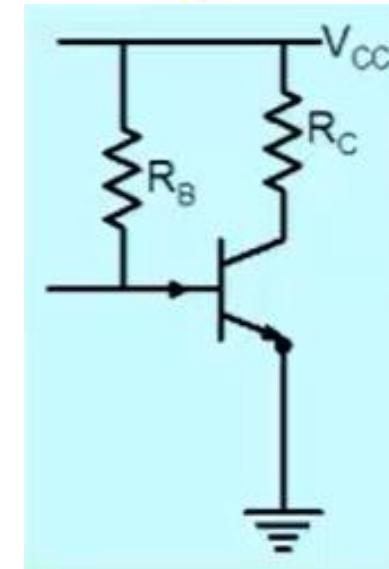
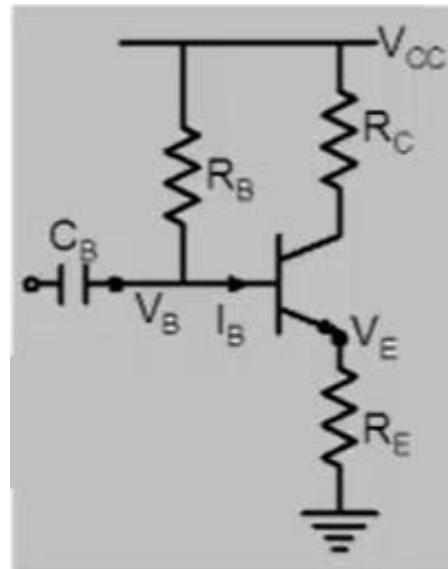
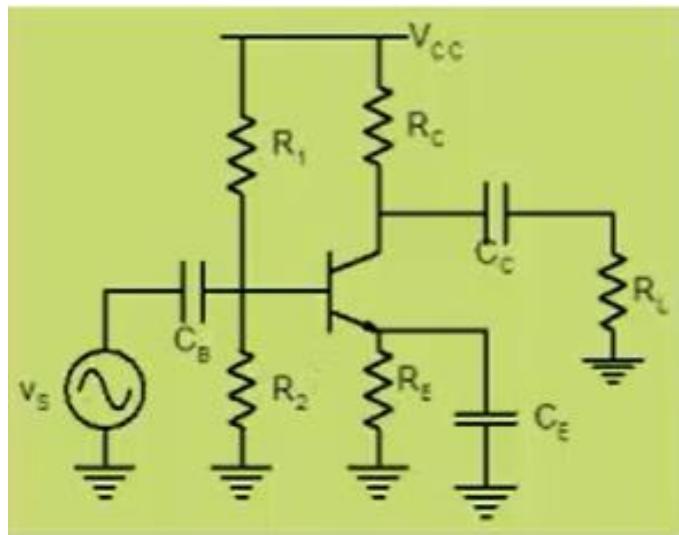
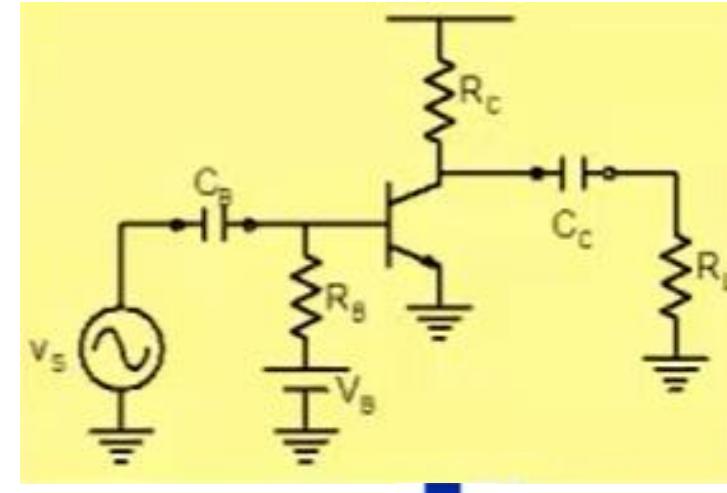
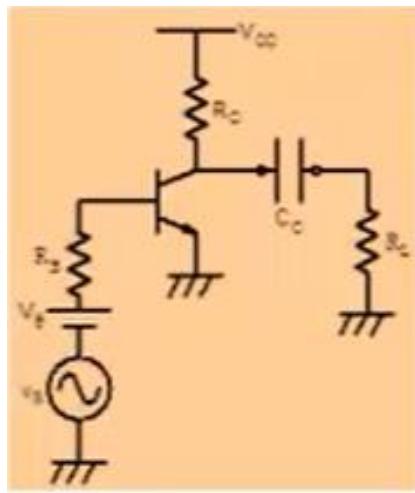
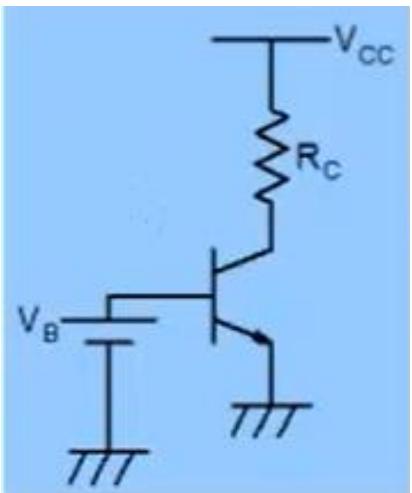
Higher value resistors ($M\Omega$) are expensive and capacitors in pF range only are possible. Passive components are expensive, while transistors are cheap !

A good biasing circuit for discrete implementation

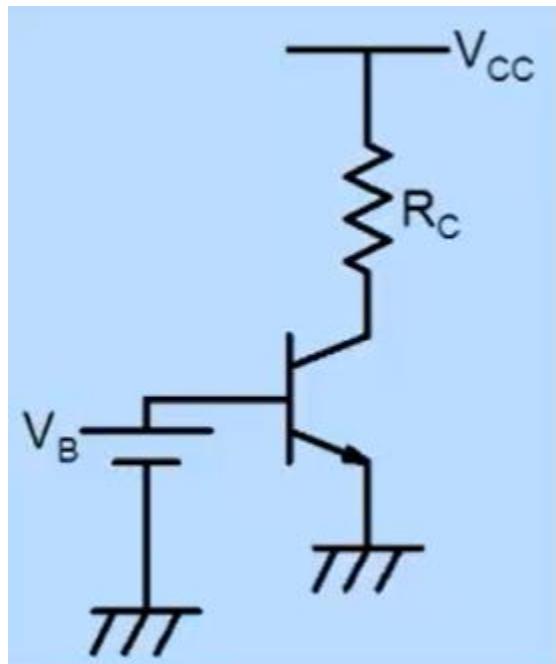


Every Circuit is a solution to one or more set of problems !

Evolution of circuit from simple to complex



BJT amp-1

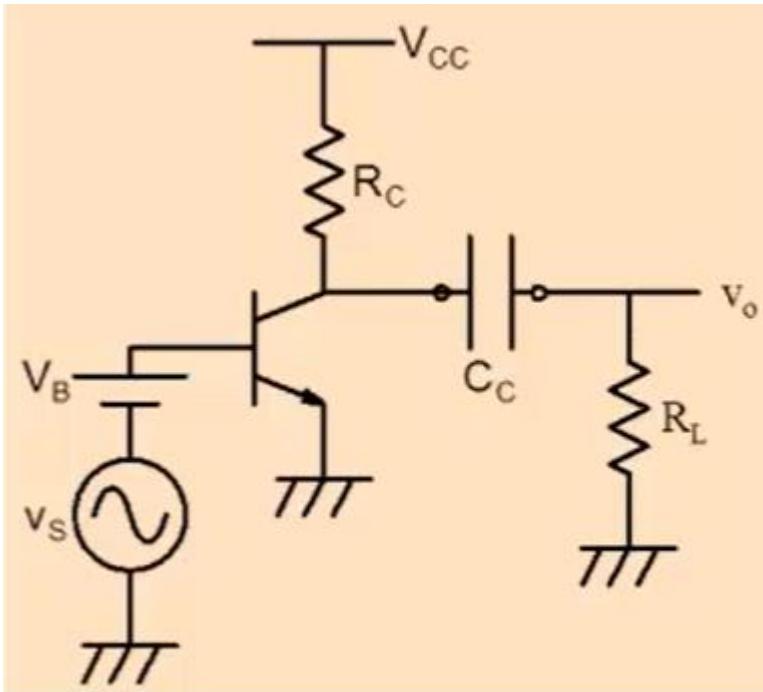


Bias the Transistor in Forward Active Mode

$$I_C \cong I_S \times \exp\left(\frac{V_{BE}}{V_T}\right)$$

$$\Delta I_C \cong I_S \times \exp\left(\frac{V_{BE}}{V_T}\right) \times \frac{\Delta V_{BE}}{V_T}$$

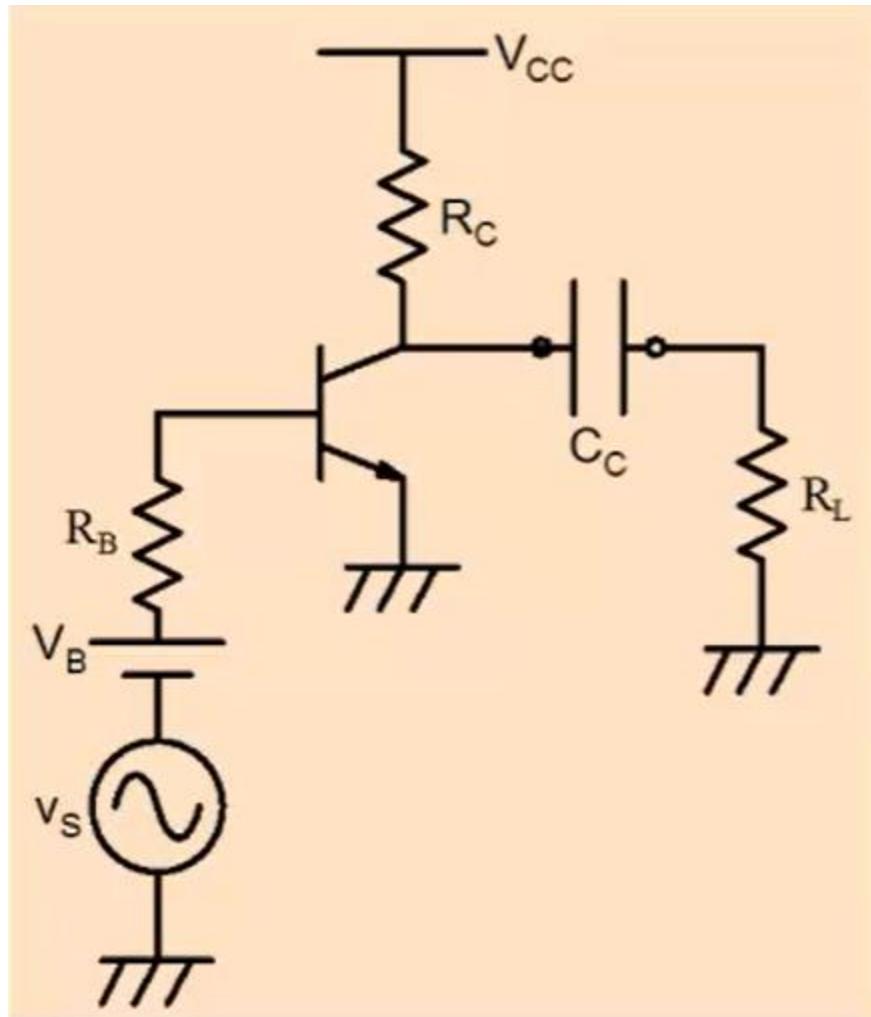
$$\left(\frac{\Delta I_C}{I_C}\right) = \left(\frac{\Delta V_B}{V_B}\right) \times \left(\frac{V_{BE}}{V_T}\right)$$



Apply the signal at the base and Connect the load

Biasing is very sensitive to the biasing voltage and temperature

BJT amp-2



$$I_B = \frac{V_B - V_{BE}}{R_B}$$

$$I_C = \beta \times I_B$$

$$\frac{\Delta I_C}{I_C} = \frac{-\Delta V_{BE} + \Delta V_B}{V_B - V_{BE}}$$

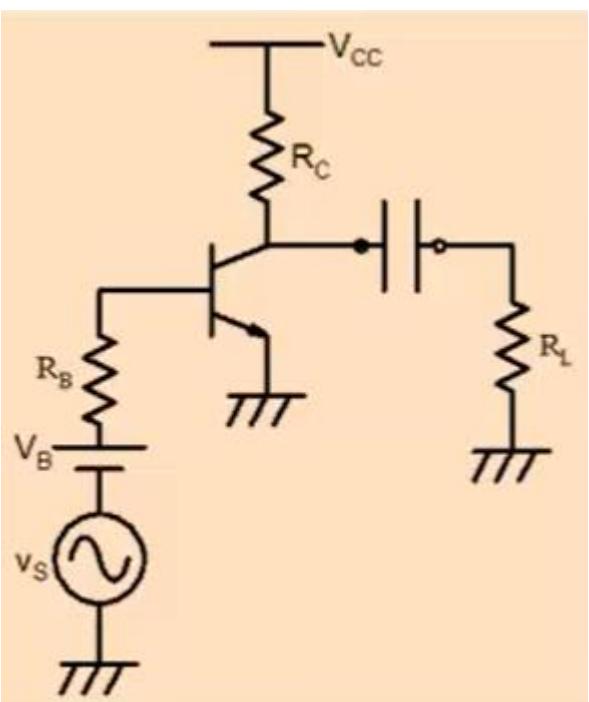
$$\frac{dV_{BE}}{dT} = -2 \text{mV / } ^\circ\text{C}$$

$$\Delta V_{BE} = 100 \text{ mV}$$

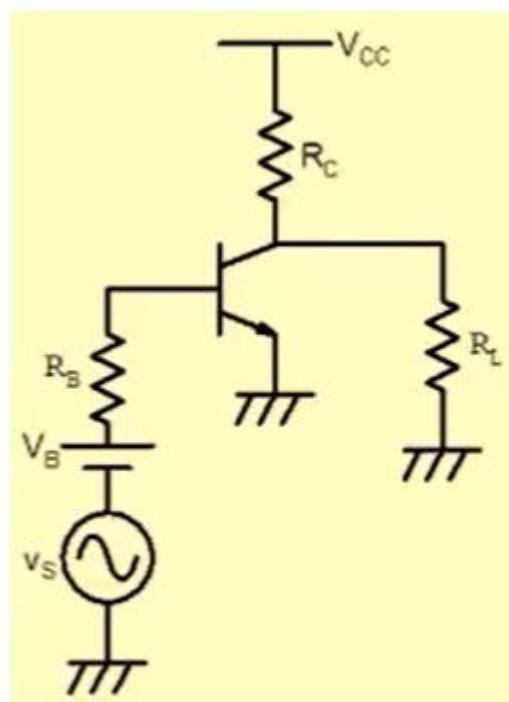
$$V_B - V_{BE} \gg 100 \text{ mV}$$

$$V_B - V_{BE} = I_B R_B \geq 1 \text{ Volt}$$

Why use a capacitor at the output?



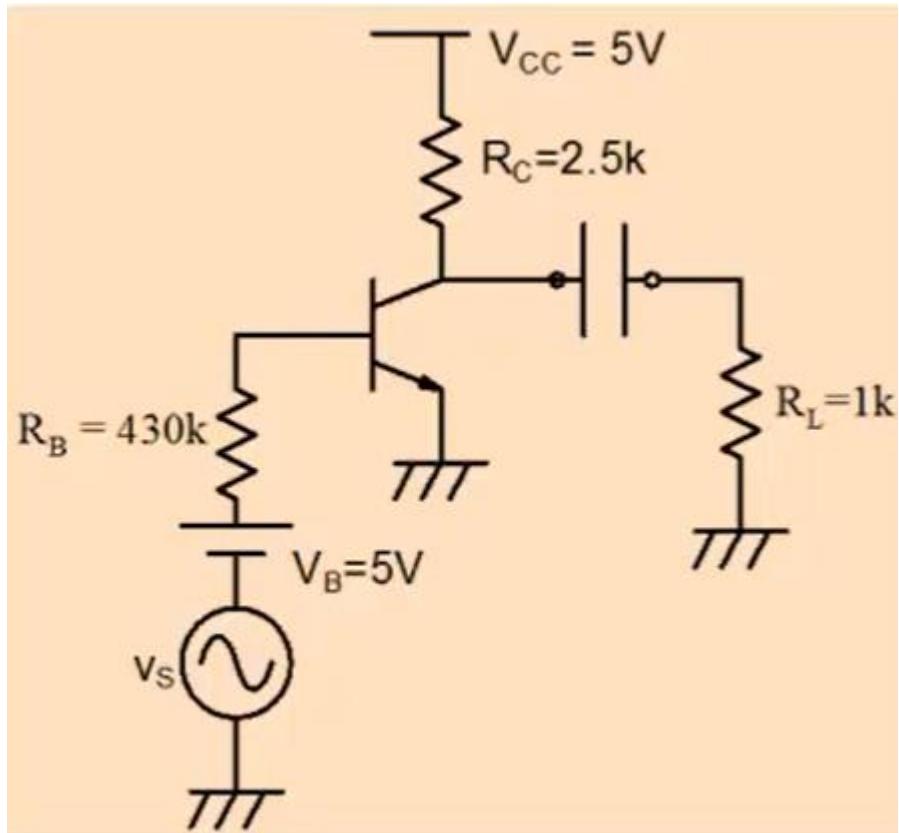
$$V_{CE} = V_{CC} - I_C R_C$$



$$V_{CE} = \frac{V_{CC} - I_C R_C}{1 + R_C / R_L}$$

It may become difficult to obtain the desired value of V_{CE} and bias point becomes load dependent.

Example-1



Bias or quiescent (Q) Point :

$$I_{CQ} = 1mA; \quad V_{CEQ} = 2.5V$$

Design:

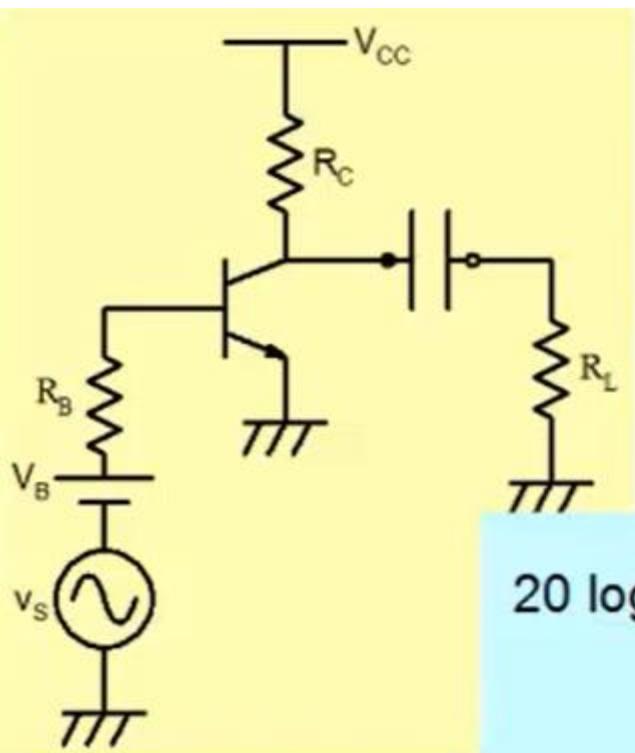
$$I_B = \frac{V_B - V_{BE}}{R_B}; \quad I_C = \beta \times I_B$$

$$V_{CE} = V_{CC} - I_C \times R_C$$

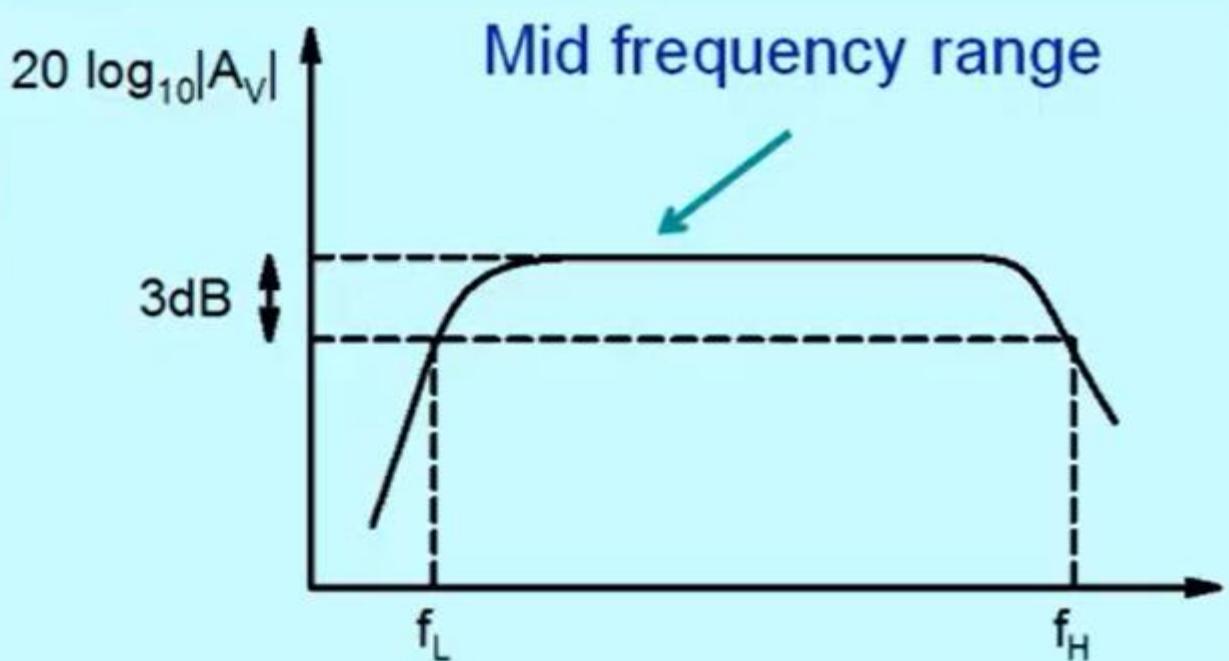
$$I_B R_B > 1W$$

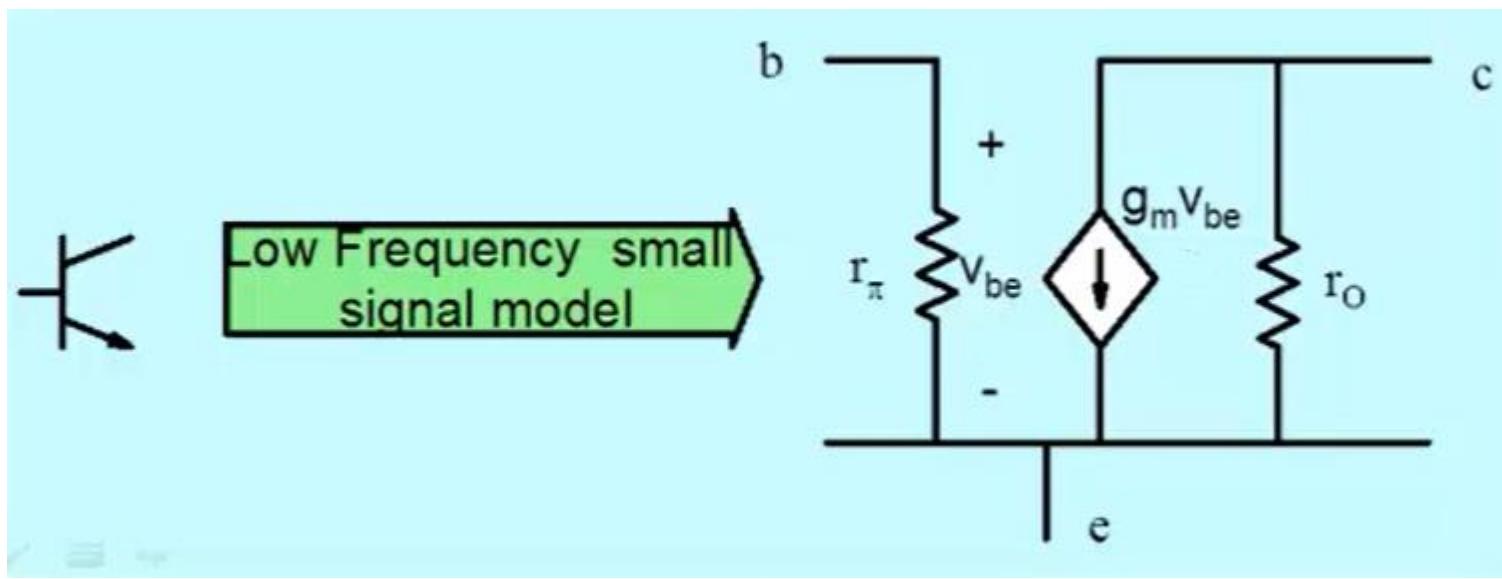
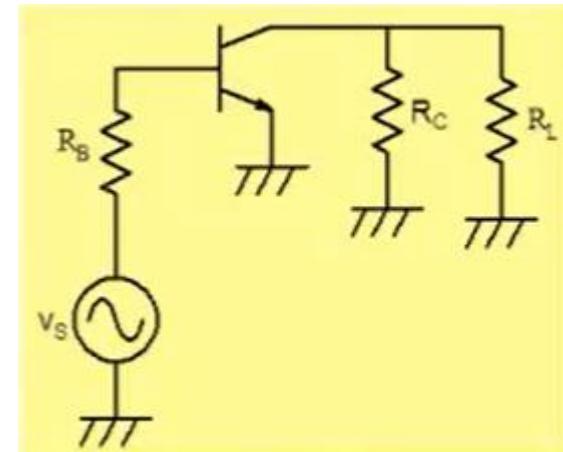
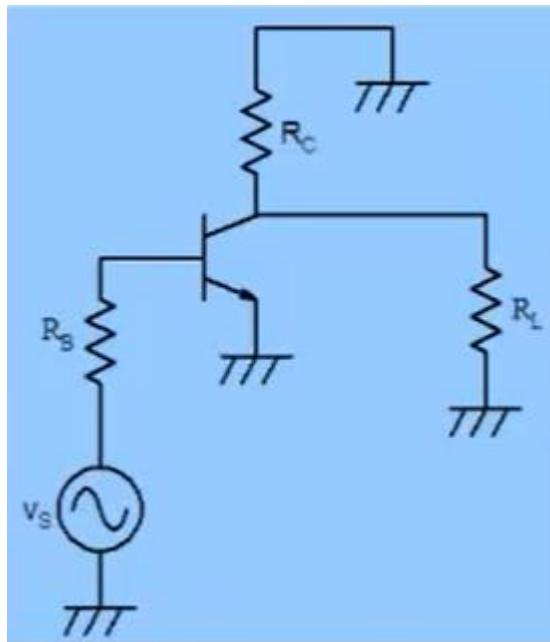
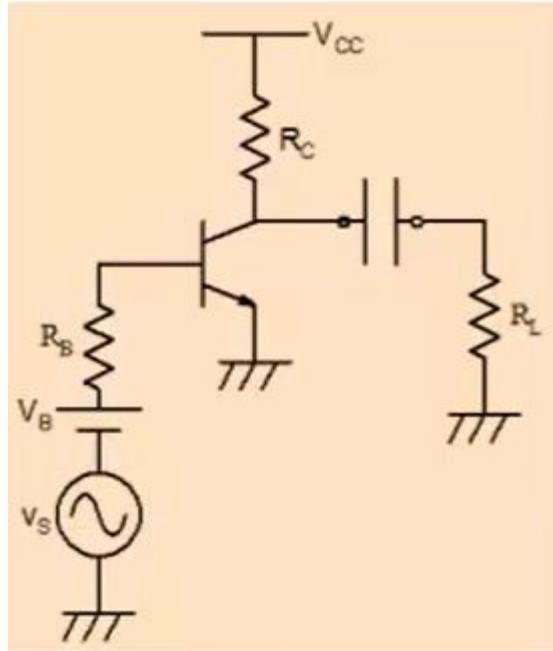
$$R_B = 430k\Omega; \quad R_C = 2.5k\Omega$$

Small Signal Analysis (Mid Frequency Range)

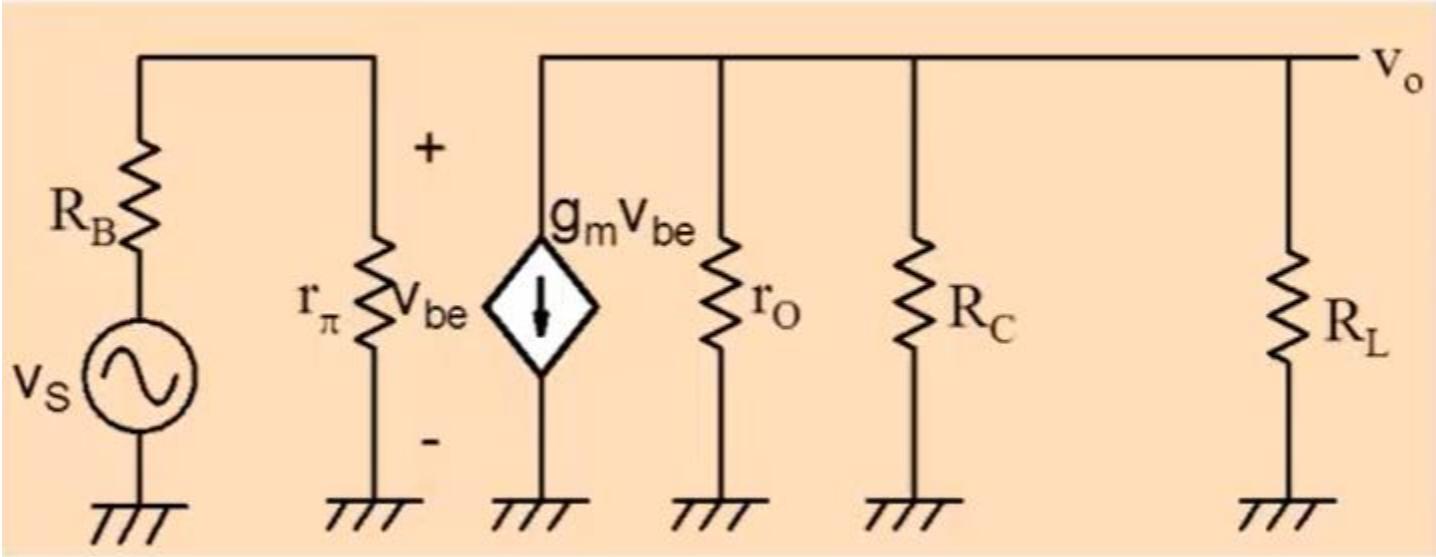


Frequency is high enough for all coupling capacitors to be assumed as short but low enough for all internal transistor capacitances to be considered as open.





Small Signal Analysis

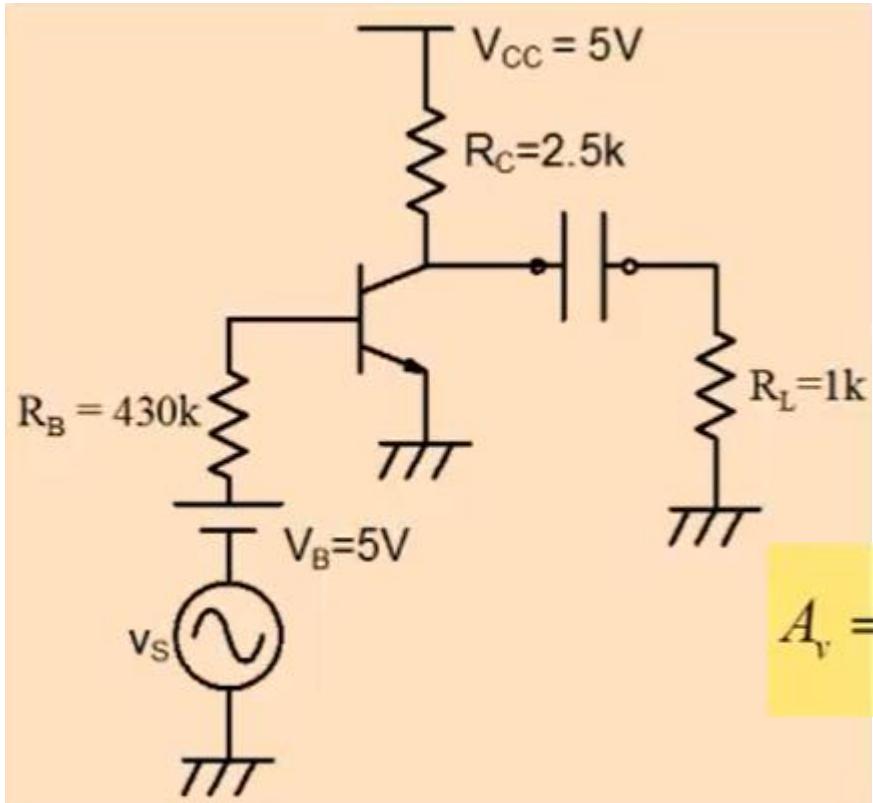


$$v_{be} = \frac{r_\pi}{r_\pi + R_B} v_s$$

$$v_o = - g_m v_{be} \times (r_o \parallel R_C \parallel R_L)$$

$$A_v = - \left(\frac{r_\pi}{r_\pi + R_B} \right) g_m \times (r_o \parallel R_C \parallel R_L)$$

Example-1



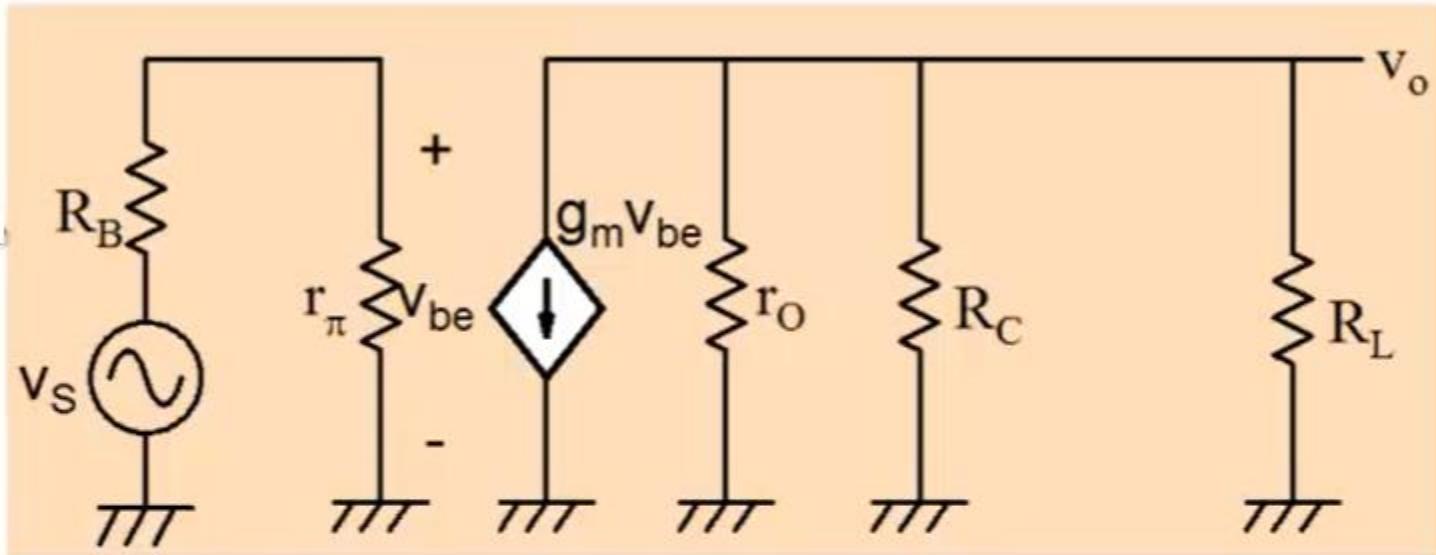
$$I_{CQ} = 1mA; \quad V_{CEQ} = 2.5V$$

$$g_m = 38m\text{S}; \quad r_\pi = 2.6k\Omega; \quad r_o = 100k\Omega$$

$$A_v = - \left(\frac{r_\pi}{r_\pi + R_B} \right) \{ g_m \times (r_o \parallel R_C \parallel R_L) \}$$

$$A_v = (6 \times 10^{-3}) \times 27.2 = 0.164$$

Problem

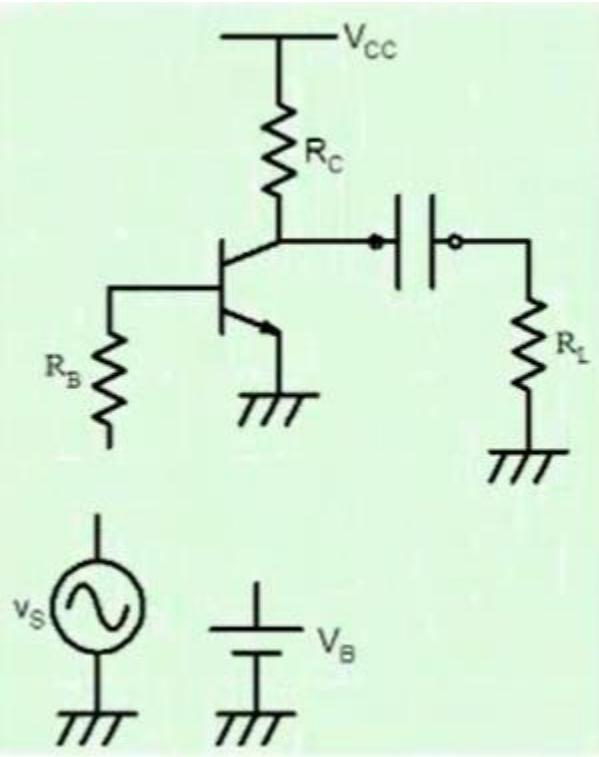
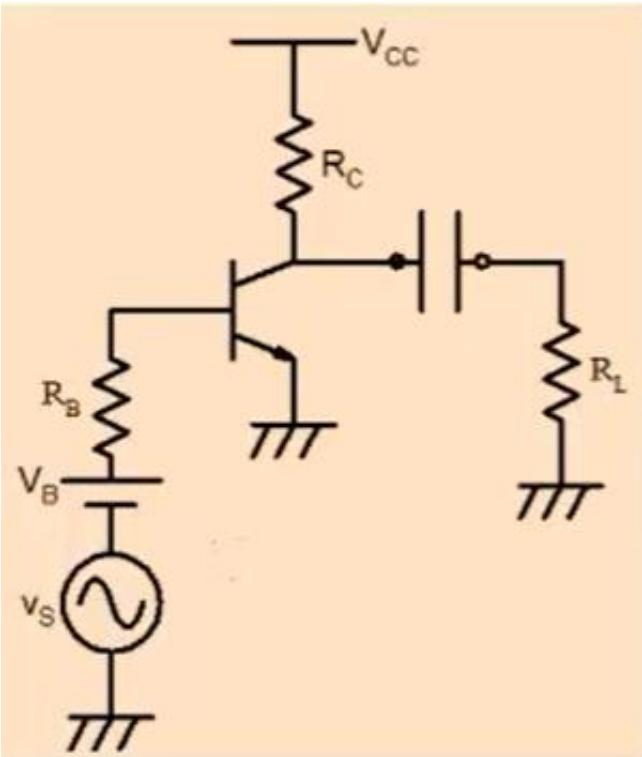


$$A_V \cong \left(\frac{r_\pi}{r_\pi + R_B} \right) g_m R_L$$

$$\left(\frac{r_\pi}{r_\pi + R_B} \right) = \frac{V_T/I_B}{(V_T/I_B) + R_B} = \frac{V_T}{V_T + I_B R_B}$$

A large fraction of input gets dropped across R_B

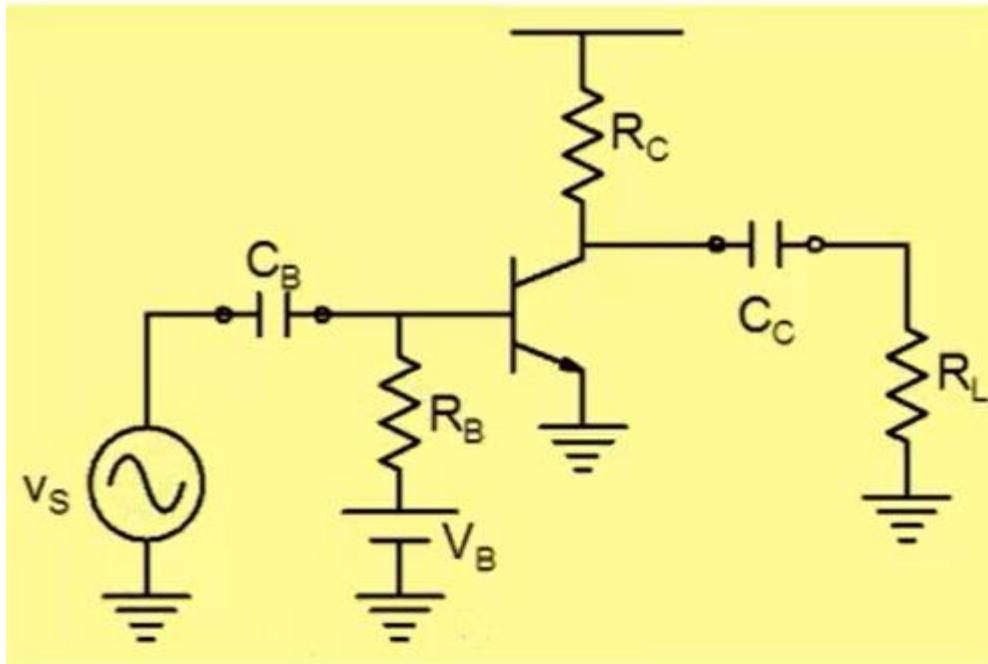
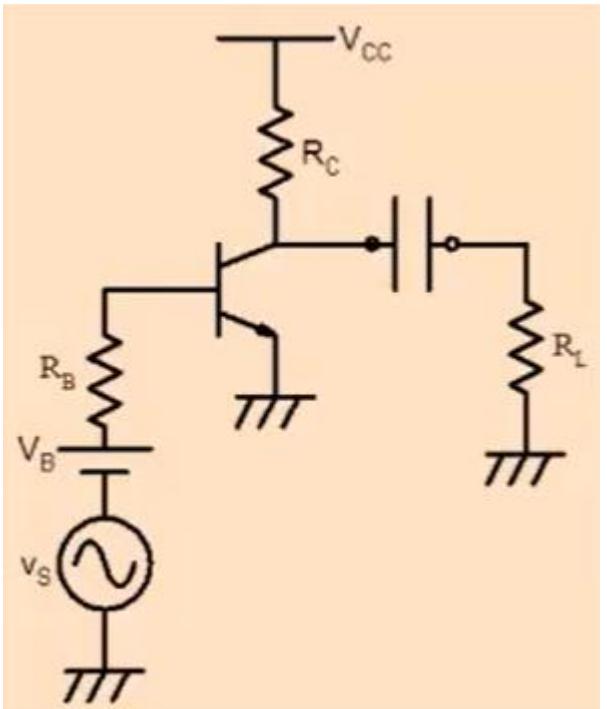
Another Problem



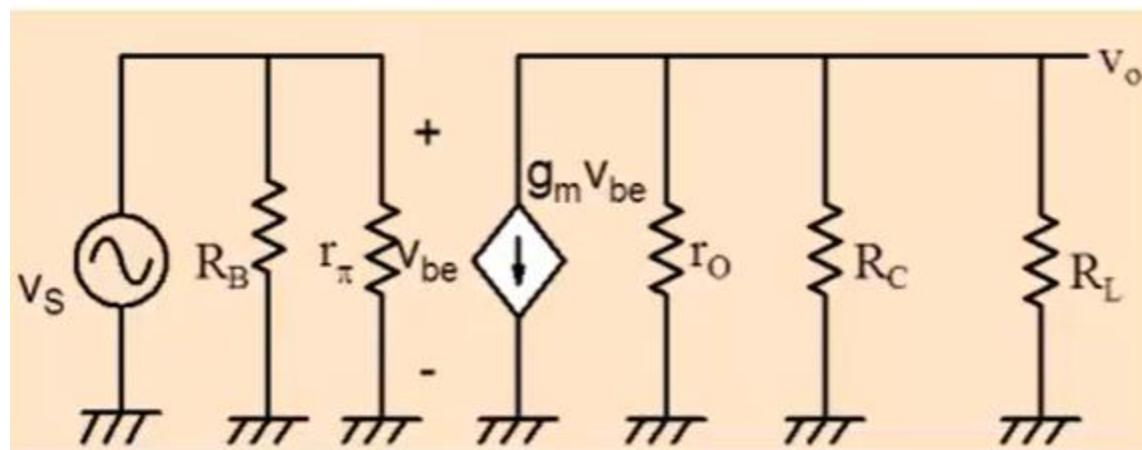
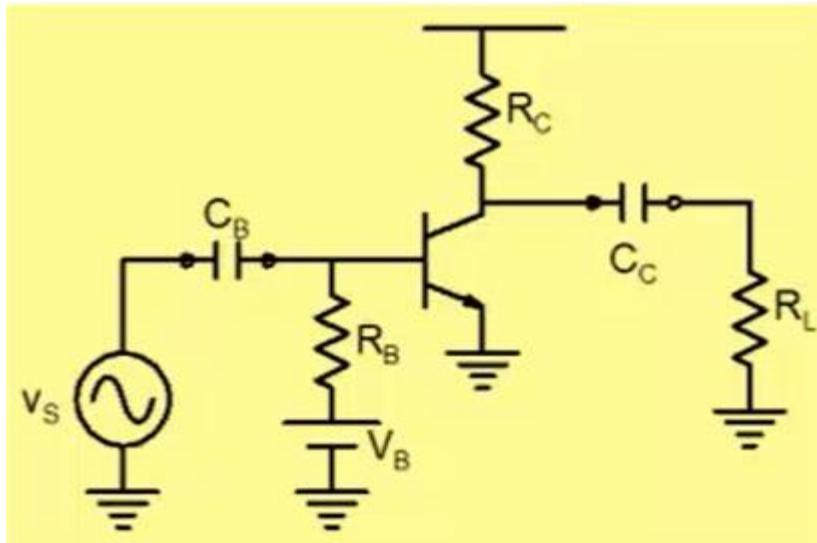
How do we connect v_s and V_B in series when one terminal of both is ground?

Solution

Bypass resistance R_B from the path of the input signal

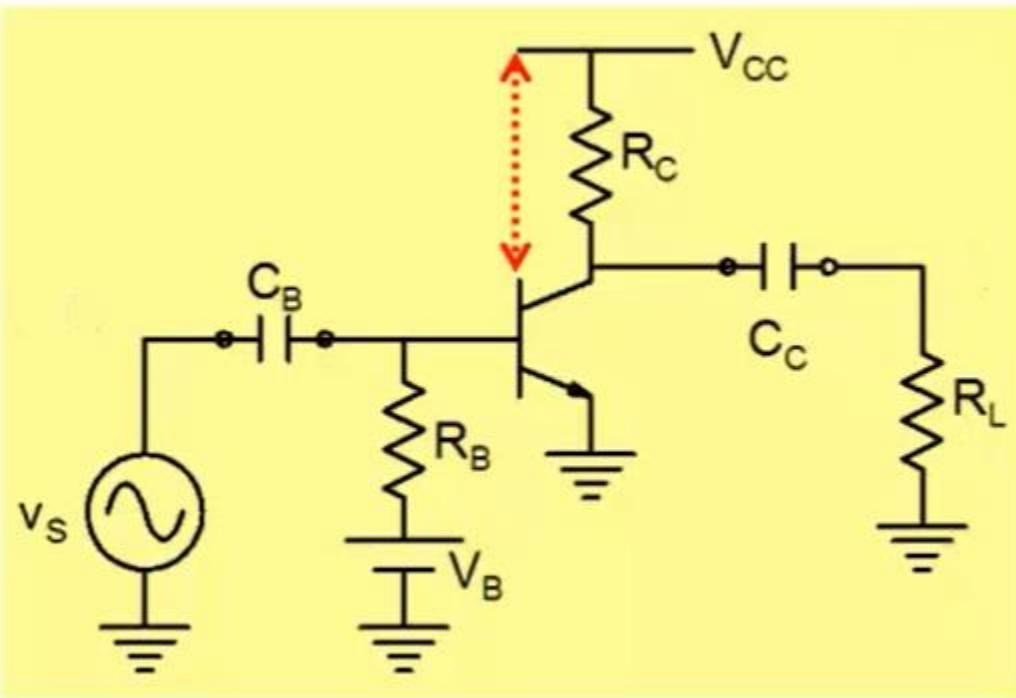


Small Signal Model



$$A_v = -g_m \times r_0 \parallel R_C \parallel R_L$$
$$\cong -g_m \times R_C \parallel R_L$$

$$g_m \times R_C = \frac{I_C \times R_C}{V_T}$$



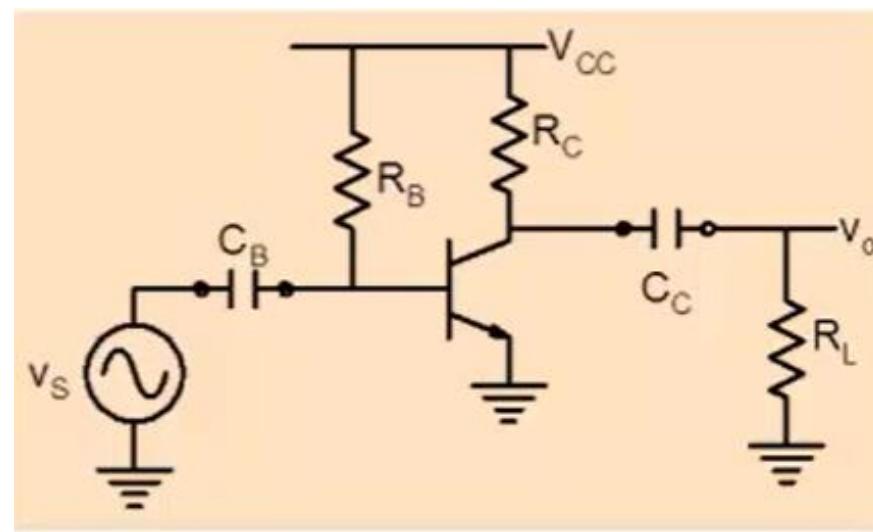
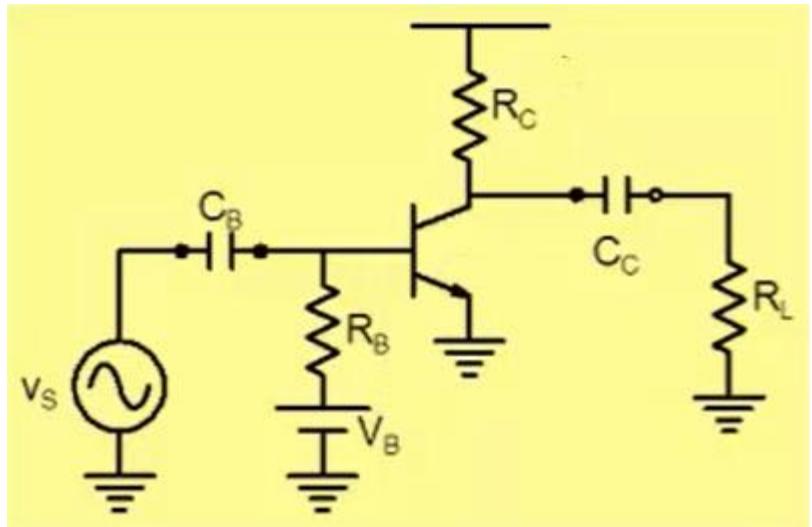
$$A_v = -g_m \times r_0 \parallel R_C \parallel R_L$$

$$\cong -g_m \times R_C \parallel R_L$$

$$g_m \times R_C = \frac{I_C \times R_C}{V_T}$$

Need large voltage drop across collector resistance to achieve high voltage gain

BJT amp-3 Use a Single supply voltage

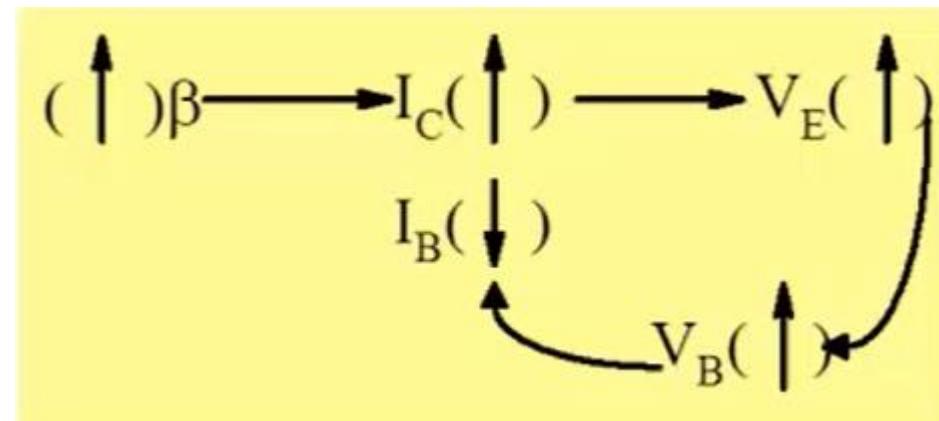
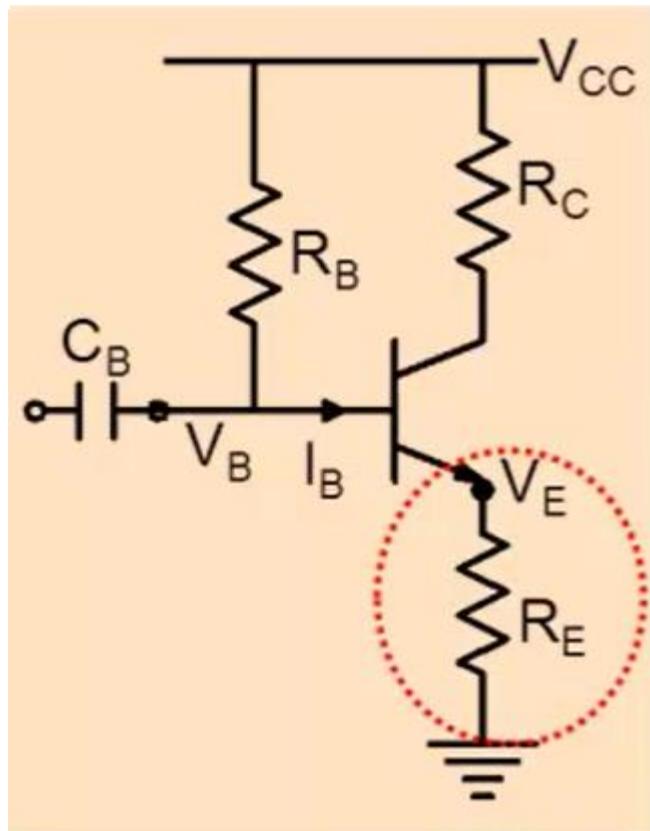


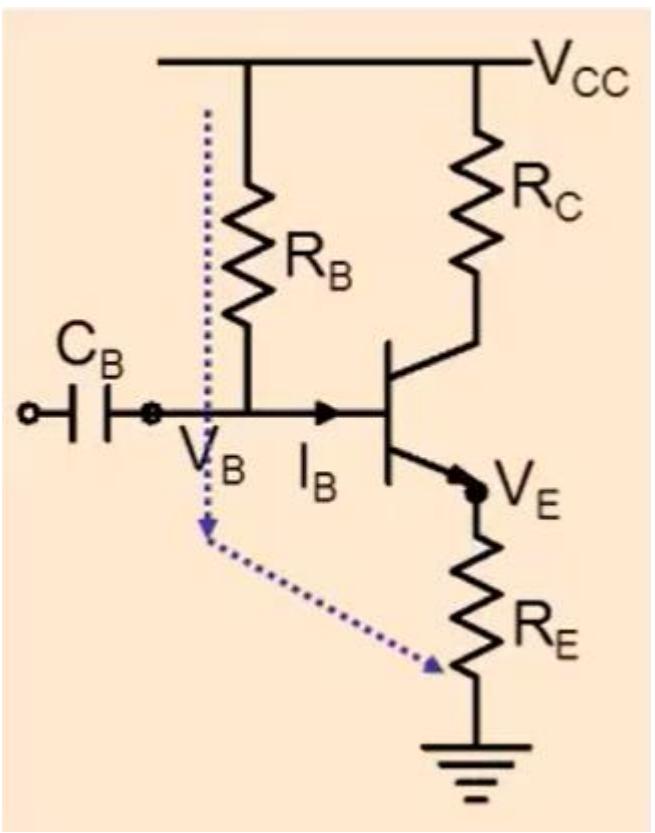
Bias point is very sensitive
to current gain variations

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad I_C = \beta \cdot I_B$$
$$S = \frac{\Delta I_C / I_C}{\Delta \beta / \beta} = 1$$

BJT amp-4

Negative Feedback





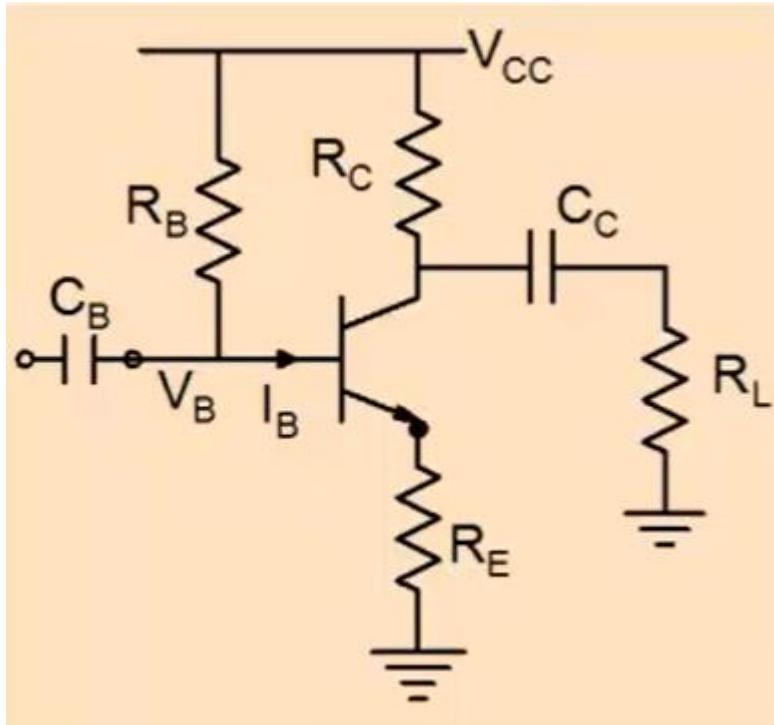
Design Criterion

$$\begin{aligned}V_{CC} &= I_B \times R_B + V_{BE} + I_E \times R_E \\&= \frac{I_C \times R_B}{\beta} + V_{BE} + \frac{(\beta+1)}{\beta} \times I_C \times R_E\end{aligned}$$

$$I_C = \frac{V_{CC} - V_{BE}}{\frac{R_B}{\beta} + R_E}$$

$$S = \frac{\Delta I_C / I_C}{\Delta \beta / \beta} = \frac{1}{1 + \frac{R_E}{R_B / \beta}}$$

$$R_E \gg \frac{R_B}{\beta} \quad I_C \approx \frac{V_{CC} - V_{BE}}{R_E}$$



$$I_C \cong \frac{V_{CC} - V_{BE}}{R_E}$$

KVL: $V_{CC} = I_C R_C + V_{CE} + I_C R_E$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$$

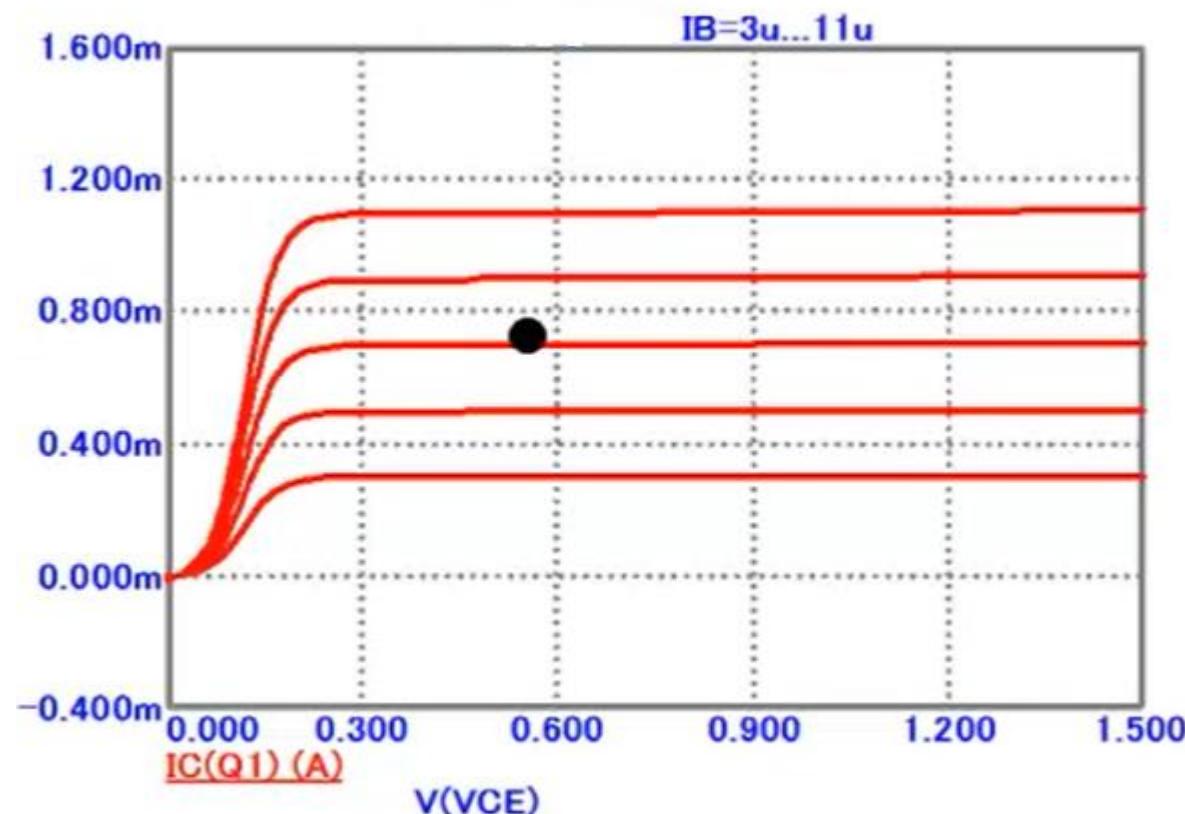
$$\Rightarrow \frac{R_C}{R_E} = \frac{V_{BE} - V_{CE}}{V_{CC} - V_{BE}}$$

Two problems:

$$(1) V_{CE} < V_{BE}$$

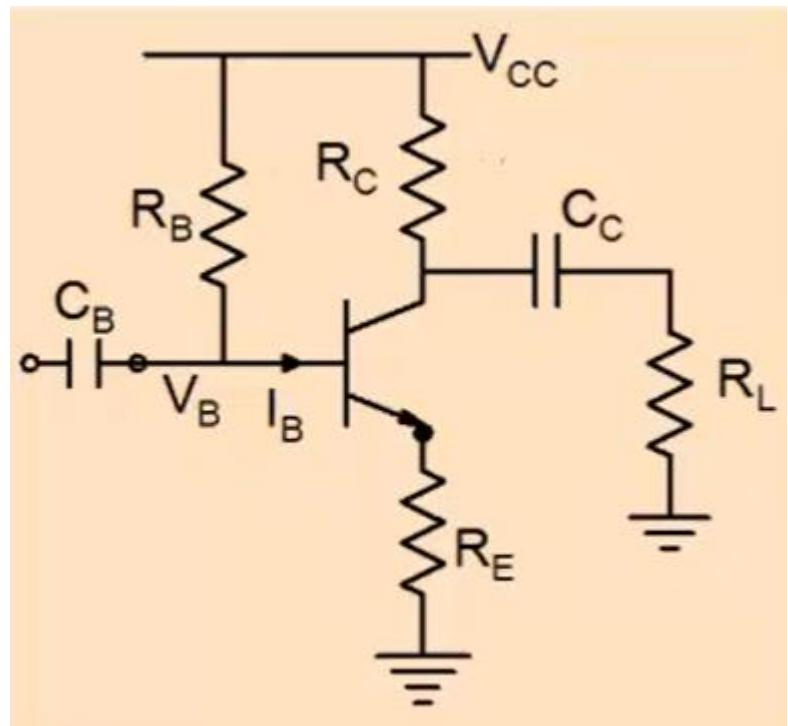
$$(2) R_C < R_E$$

(1) $V_{CE} < V_{BE}$



Transistor is biased close to saturation

Voltage gain will be less than unity !



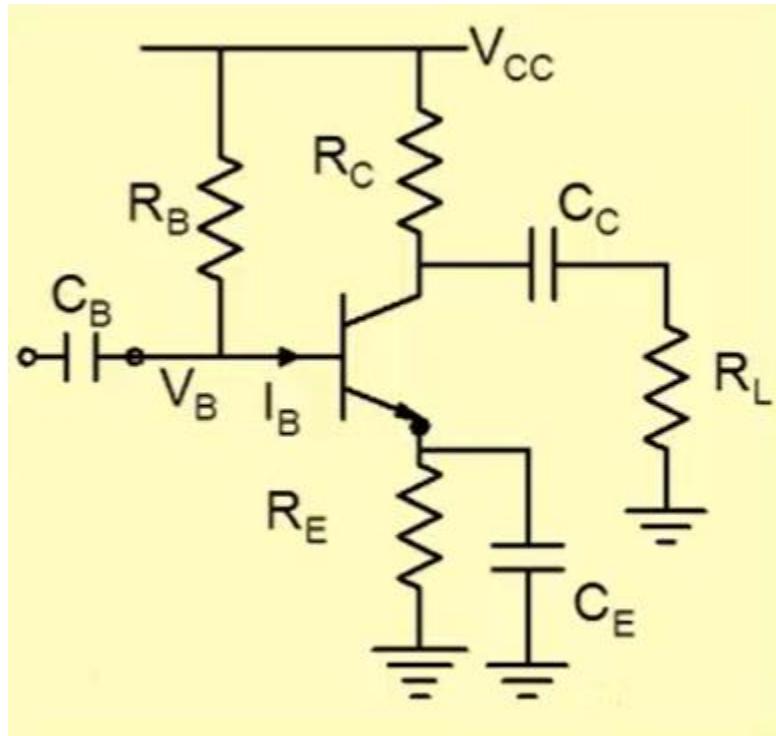
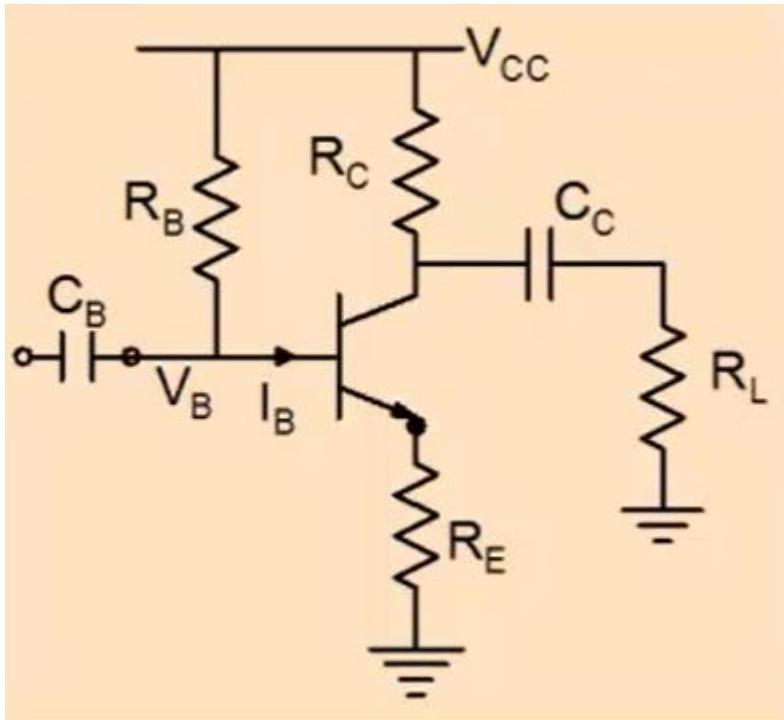
$$\frac{R_C}{R_E} = \frac{V_{BE} - V_{CE}}{V_{CC} - V_{BE}}$$

(2) $R_C < R_E$

$$|A_v| \cong \frac{g_m}{1 + g_m R_E} \times R_C \parallel R_L < \frac{R_C}{R_E}$$

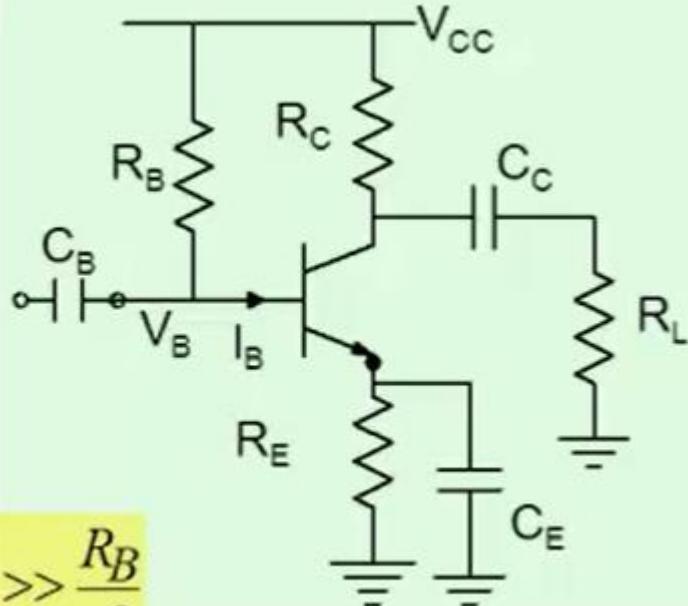
Example: $\frac{R_C}{R_E} = \frac{0.7 - 0.5}{5 - 0.7} = .047$

Bypass the resistor R_E



$$A_v \cong -\frac{g_m}{1 + g_m R_E} \times R_C \parallel R_L$$

$$A_v \cong -g_m \times R_C \parallel R_L$$



$$R_E \gg \frac{R_B}{\beta}$$

$$I_C = \frac{V_{CC} - V_{BE}}{\frac{R_B}{\beta} + R_E} \cong \frac{V_{CC} - V_{BE}}{R_E}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$$

$$A_V = -g_m \times \{R_C \parallel R_L\}$$

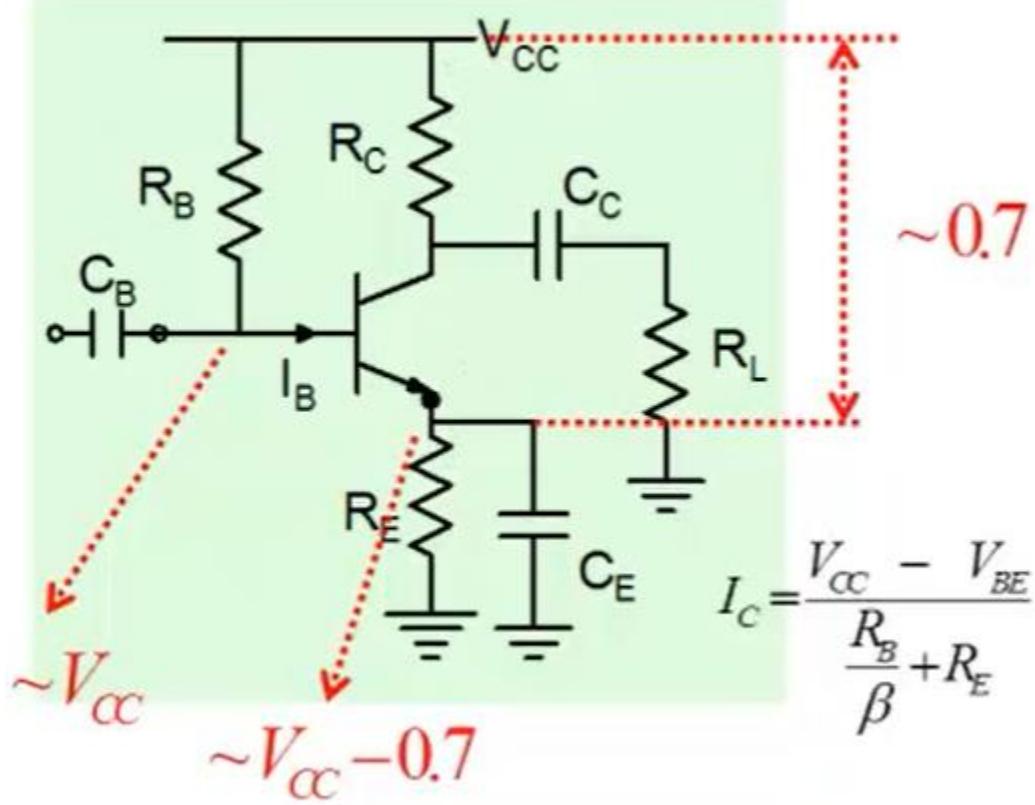
$$|A_V| < g_m R_C$$

$$|A_V| < \frac{I_C R_C}{V_T}$$

$$I_C R_C \leq V_{BE} - V_{CE} \leq 0.5$$

$$A_v < \frac{0.5}{V_T} = 19$$

Very low voltage swing as well !



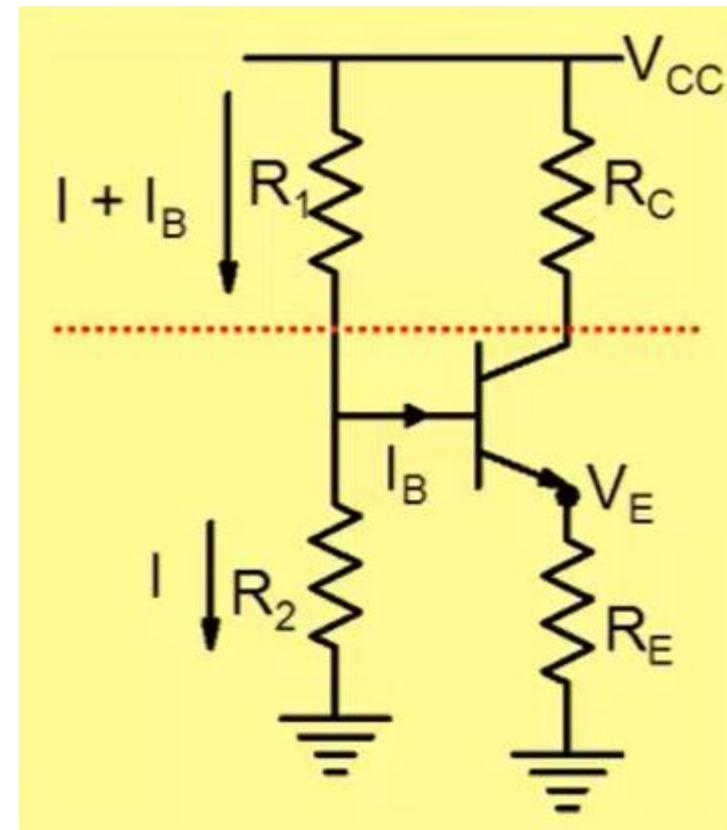
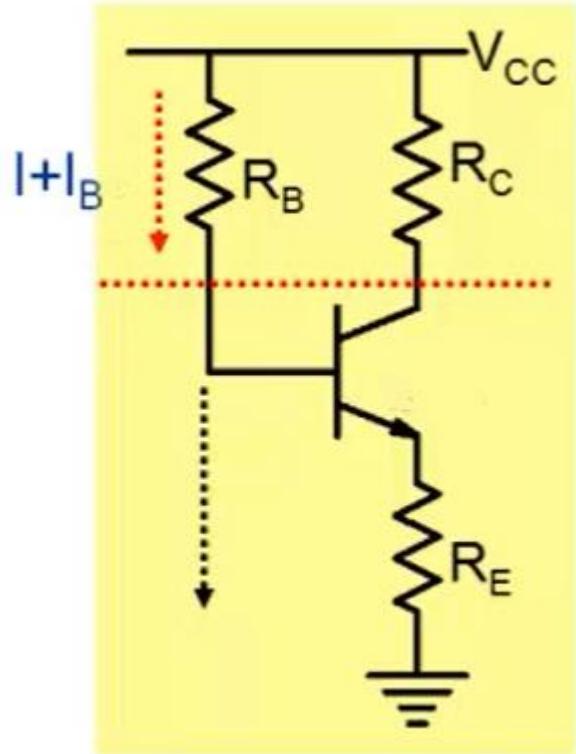
This makes both V_{CE} and voltage gain small

$$I_C = \frac{V_{CC} - V_{BE}}{\frac{R_B + R_E}{\beta}} \approx \frac{V_{CC} - V_{BE}}{R_E}$$

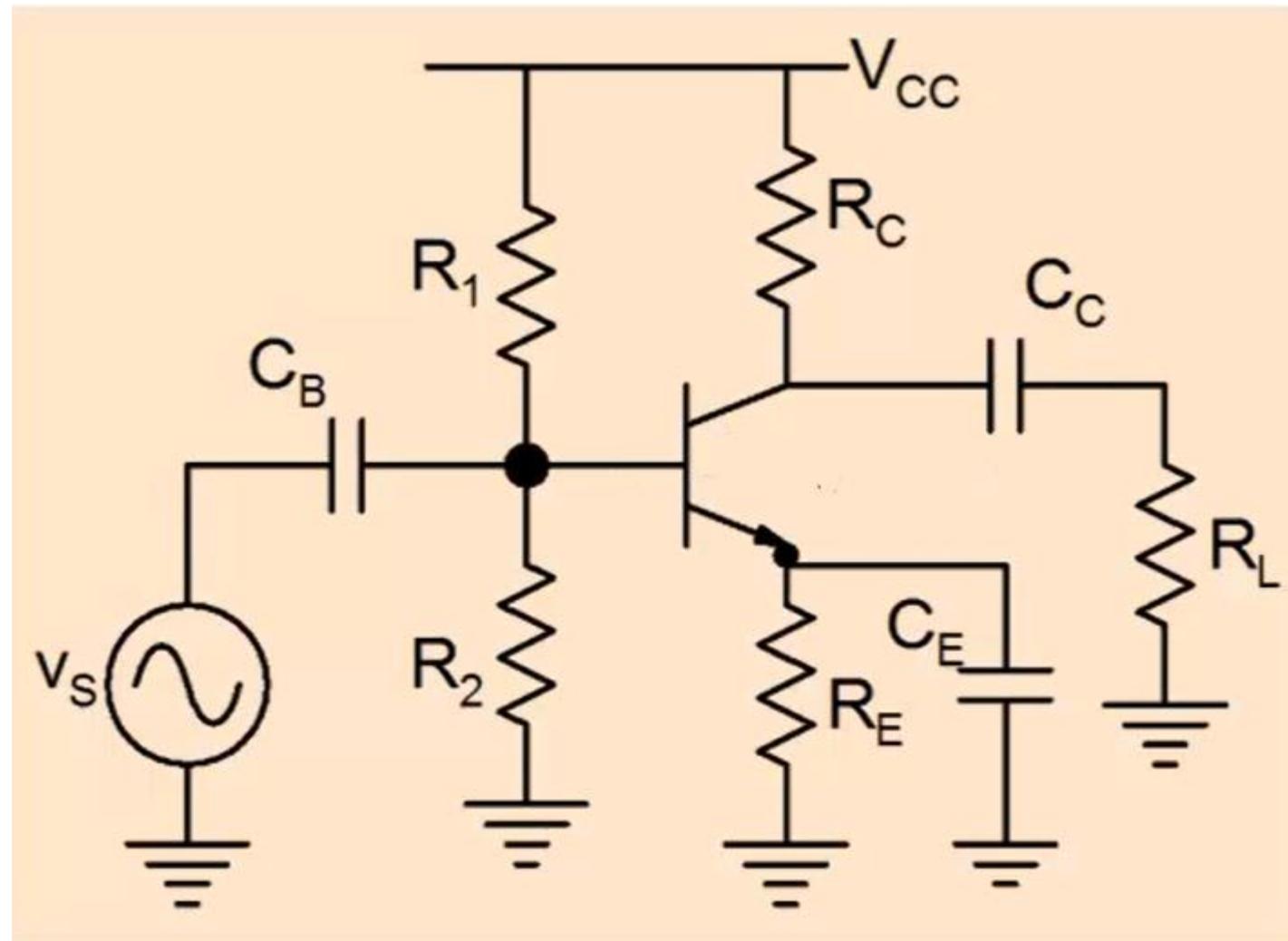
Problem: How do we reduce V_B without making it base current and thus current gain dependent.

We want more drop across R_B but not due to I_B

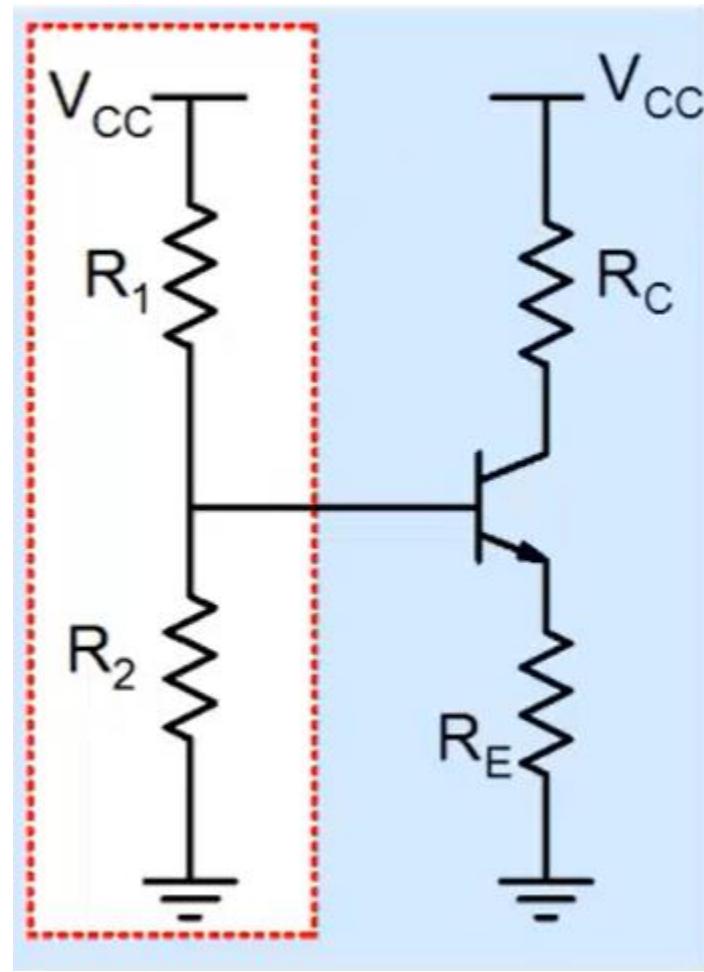
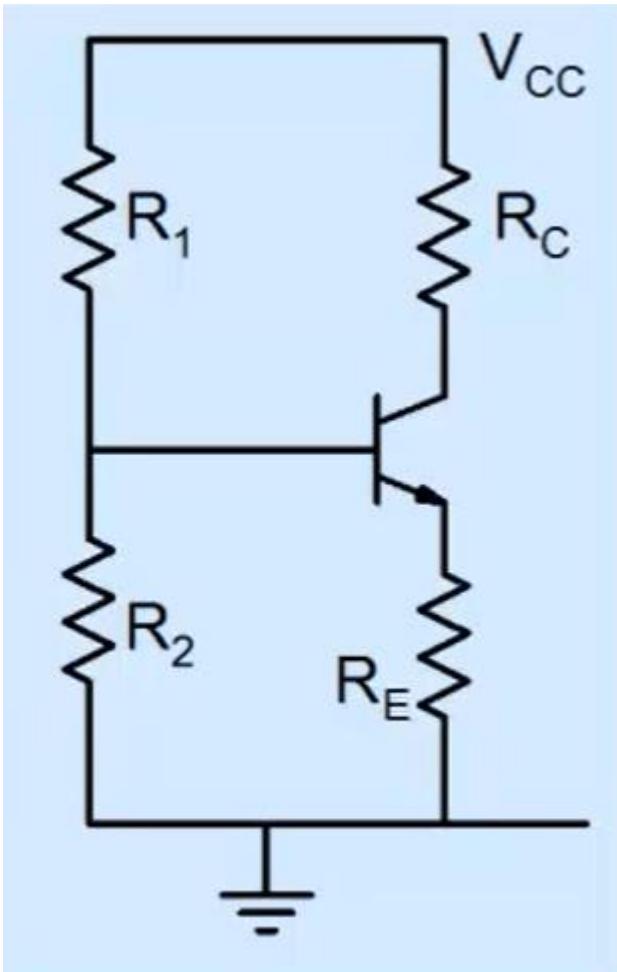
Solution



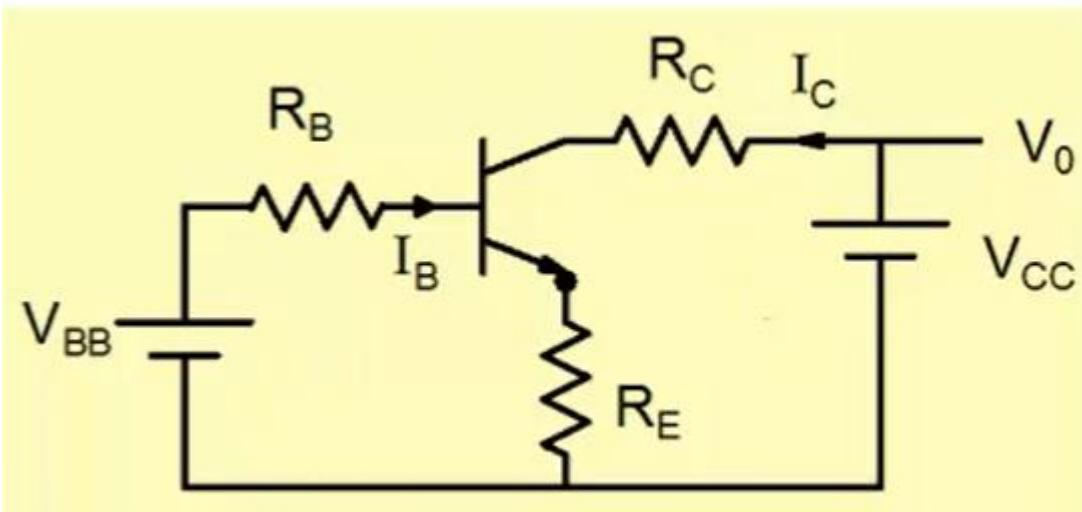
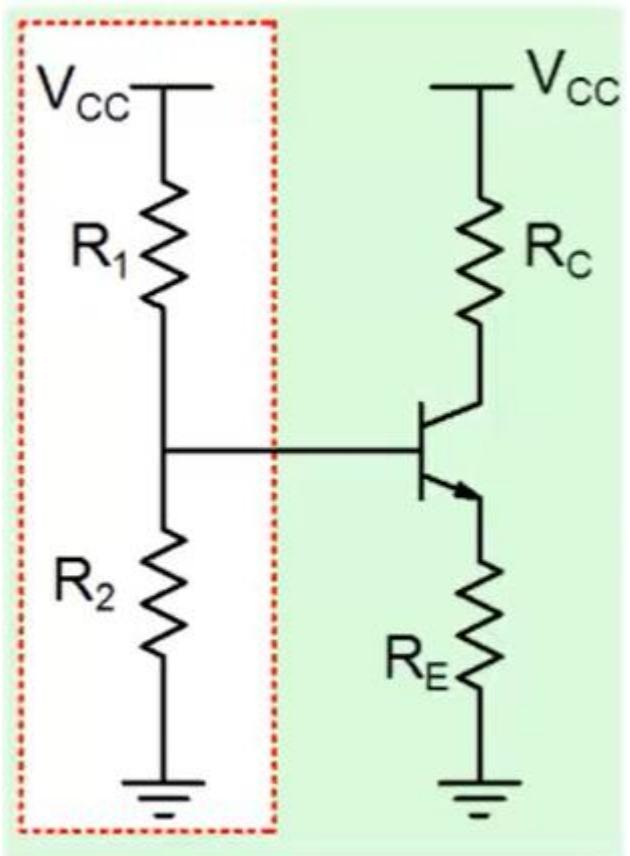
BJT amp-5



Bias Point dc Analysis



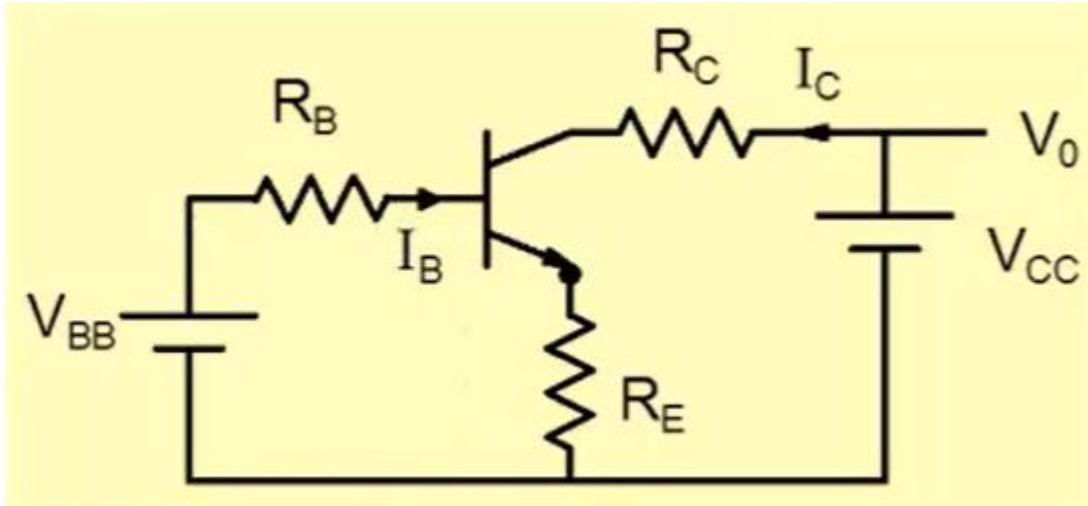
dc Analysis



$$V_{TH} = V_{BB} = \frac{V_{CC}R_2}{R_1 + R_2}$$

$$R_{TH} = R_B = R_1 \parallel R_2$$

dc Analysis



$$V_{BB} \approx I_B R_B + V_{BE} + I_C R_E$$

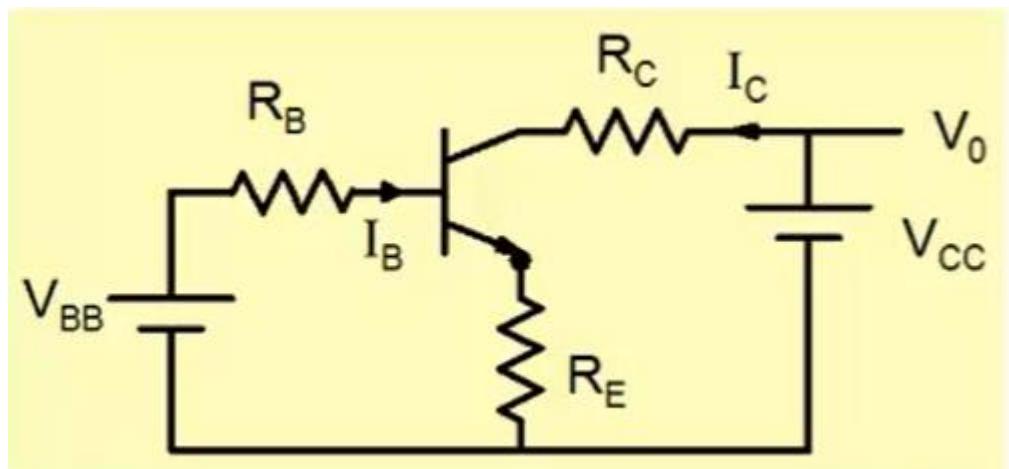
$$I_C = \frac{V_{BB} - V_{BE}}{\frac{R_B}{\beta} + R_E}$$

$$V_{BB} = \frac{V_{CC} R_2}{R_1 + R_2}$$
$$R_B = R_1 \parallel R_2$$

$$S = \frac{\Delta I_C / I_C}{\Delta \beta / \beta} = \frac{1}{1 + \frac{R_E \beta}{R_B}}$$

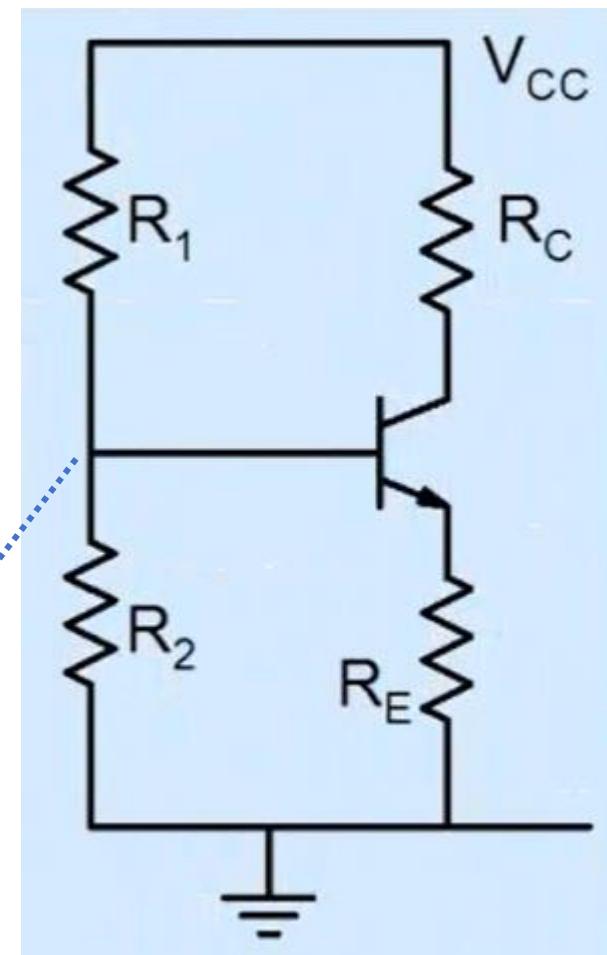
$$R_E \gg \frac{R_B}{\beta}$$

$$R_E \gg \frac{R_B}{\beta}$$

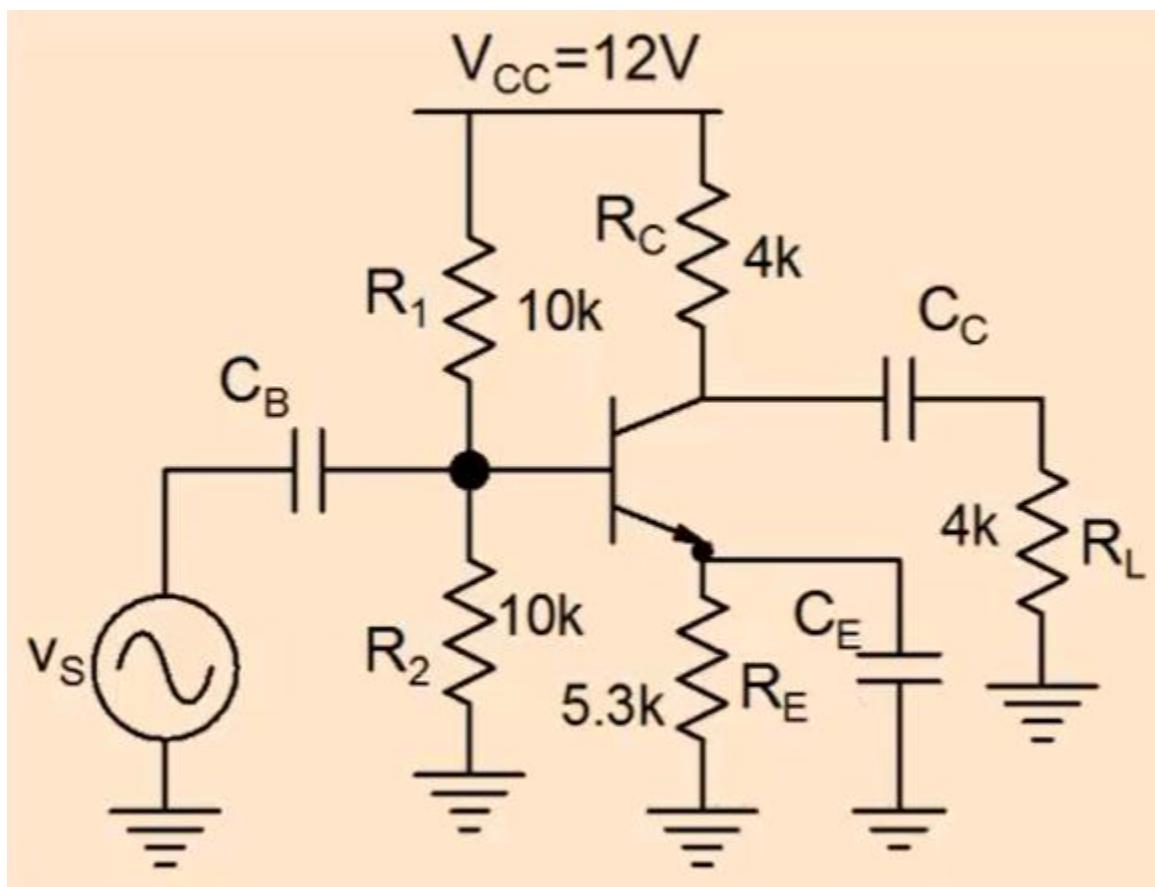


$$\begin{aligned}V_{BB} &= I_B R_B + V_{BE} + I_C R_E \\&\cong V_{BE} + I_C R_E\end{aligned}$$

$$V_{BB} \cong \frac{V_{CC} R_2}{R_1 + R_2}$$



Example-1: Analysis



$$R_B = R_1 \parallel R_2 = 5k$$

$$\frac{R_B}{\beta} = .05k \ll R_E$$

$$V_B = V_{CC} \times \frac{R_2}{R_1 + R_2} = 6V$$

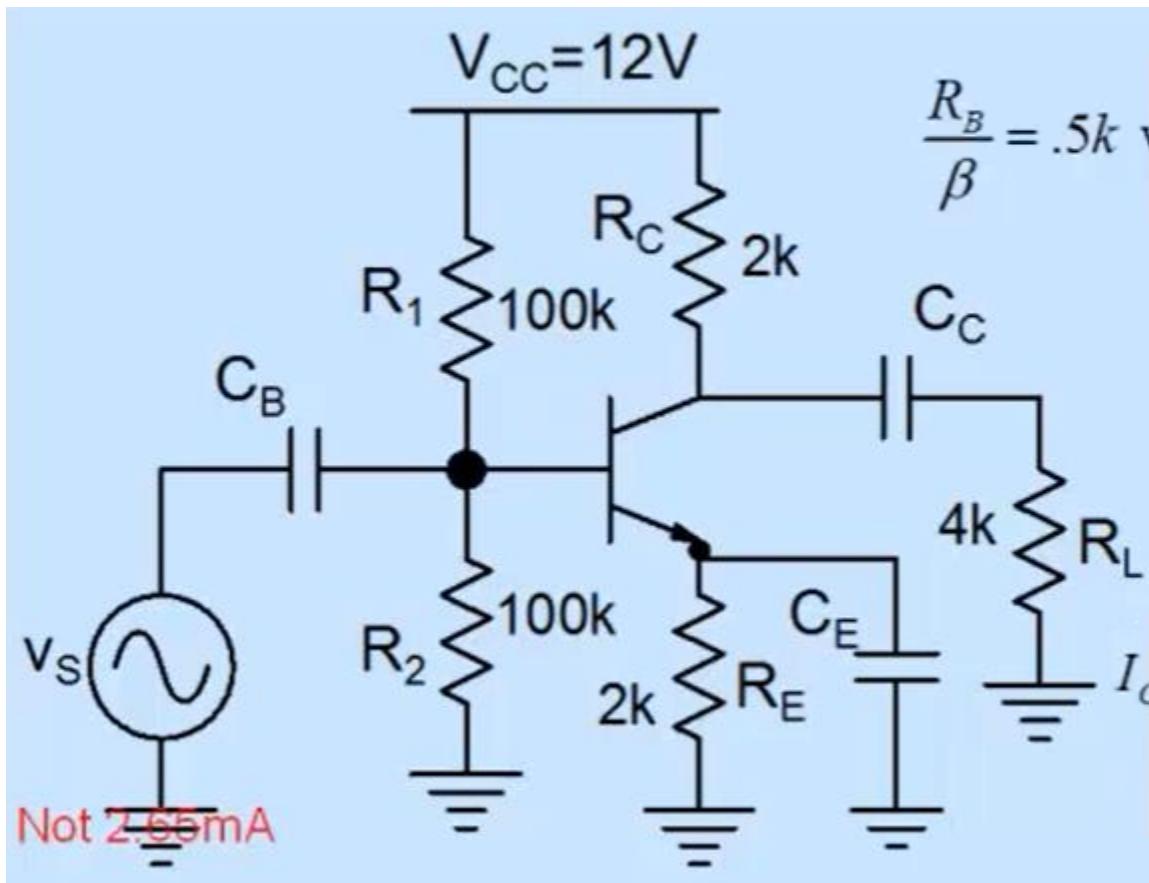
$$V_E = V_B - 0.7 = 5.3V$$

$$I_C \cong I_E = \frac{V_E}{R_E} = 1mA$$

$$V_C = V_{CC} - I_C \times R_C = 8V$$

$$V_{CEQ} = V_C - V_E = 8 - 5.3 = 2.7V$$

Example-2: Analysis



$$R_B = R_1 \parallel R_2 = 50k$$

$\frac{R_B}{\beta} = .5k$ which is comparable to R_E

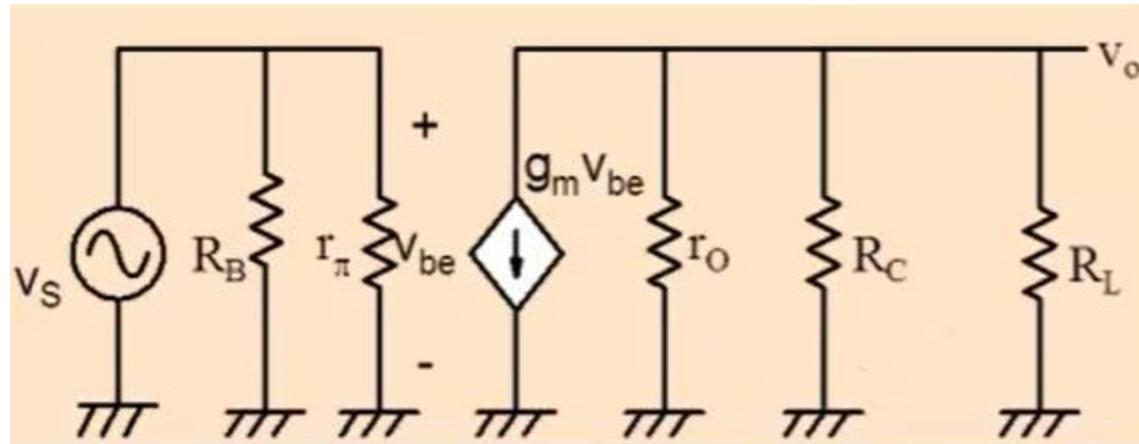
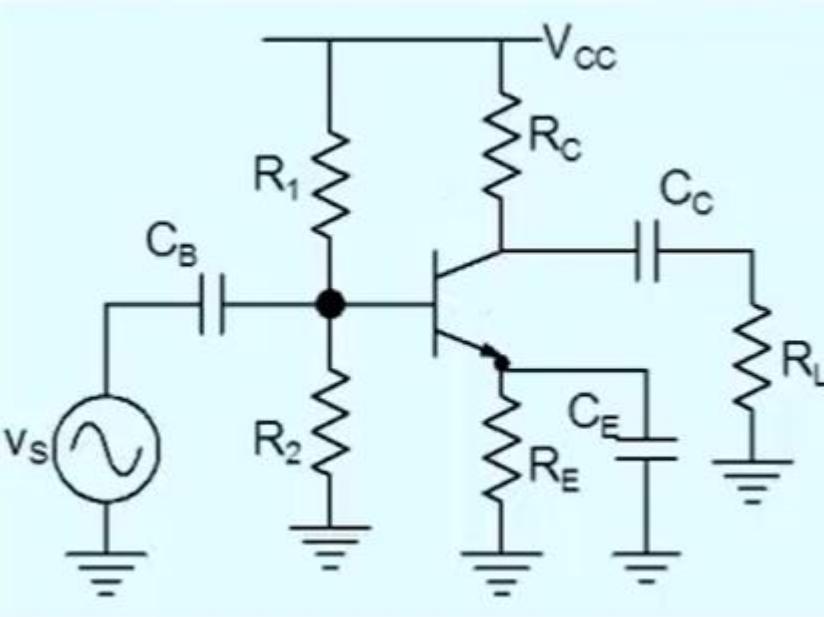
$$V_{BB} = V_{CC} \times \frac{R_2}{R_1 + R_2} = 6V$$

$$I_C \approx I_E = \frac{V_{BB} - 0.7}{\frac{R_B}{\beta} + R_E} = 2.12mA$$

$$\frac{V_{BB} - 0.7}{R_E} = 2.65mA$$

$$V_{CEQ} = 3.52V$$

Small Signal Analysis

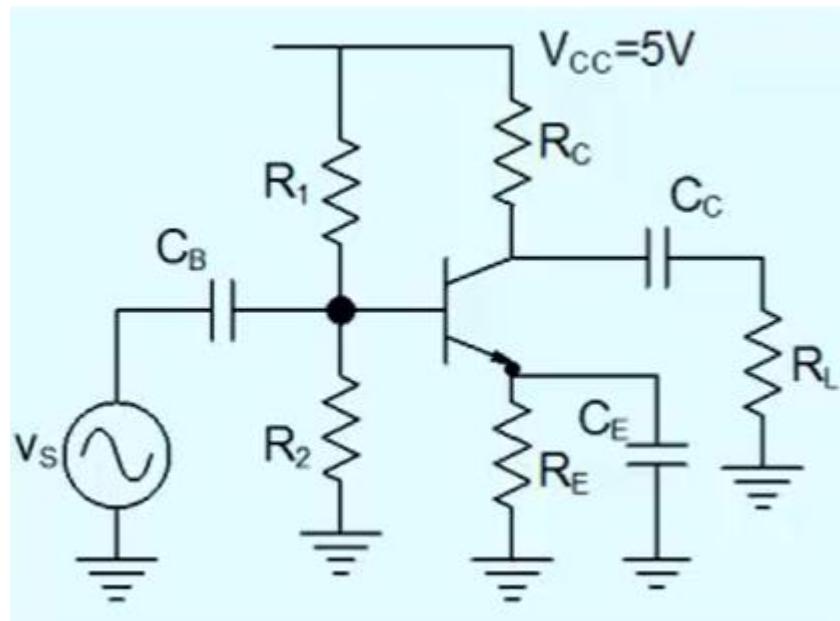


$$A_v = -g_m \times r_0 \parallel R_C \parallel R_L$$
$$\cong -g_m \times R_C \parallel R_L$$

$$g_m \times R_C = \frac{I_C \times R_C}{V_T}$$

Example-3: Design

Design for $I_{CQ} = 1mA$; $V_{CEQ} = 2.5V$



$$V_{BB} = \frac{V_{CC}R_2}{R_1 + R_2}$$

$$R_B = R_1 \parallel R_2$$

$$I_C = \frac{V_{BB} - V_{BE}}{R_B + R_E}$$

Constraints:

$$\frac{R_B}{\beta} \ll R_E$$

$$V_{BB} \gg V_{BE} = 0.7V$$

1. Key Choice: V_{BB}

$$V_{BB} = 1.7V \Rightarrow V_E = 1V; R_E = 1k$$

$$\Rightarrow V_C = 3.5V; R_C = 1.5k$$

2. Key Choice: $R_B \ll R_E \times \beta = 100k$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} = 10k$$



Expect ~10% error

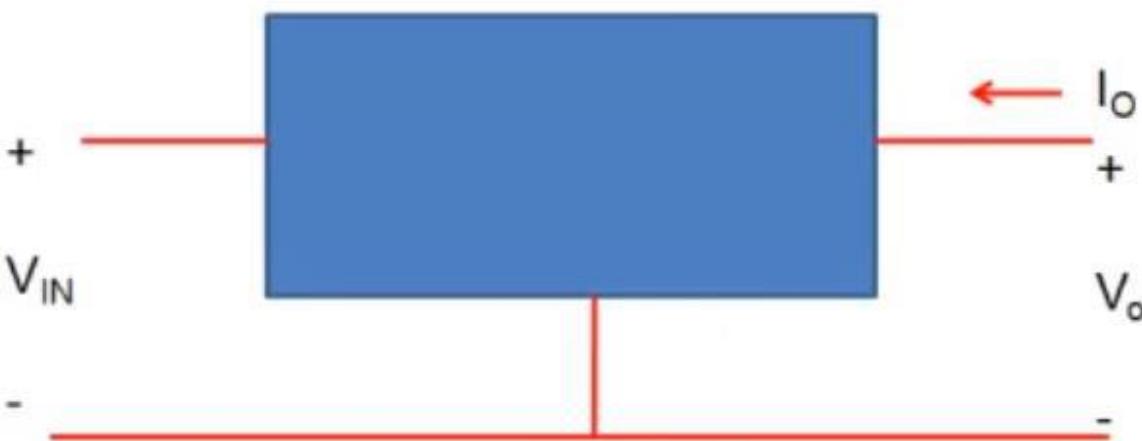
$$V_{BB} = \frac{V_{CC} R_2}{R_1 + R_2} = 1.7V$$

$$R_2 = R_B \times \frac{V_{CC}}{V_{CC} - V_{BB}} = 1.5 \times 10^4 \Omega$$

$$R_1 = R_B \times \frac{V_{CC}}{V_{BB}} = 2.94 \times 10^4 \Omega$$

MOSFET

Transistor

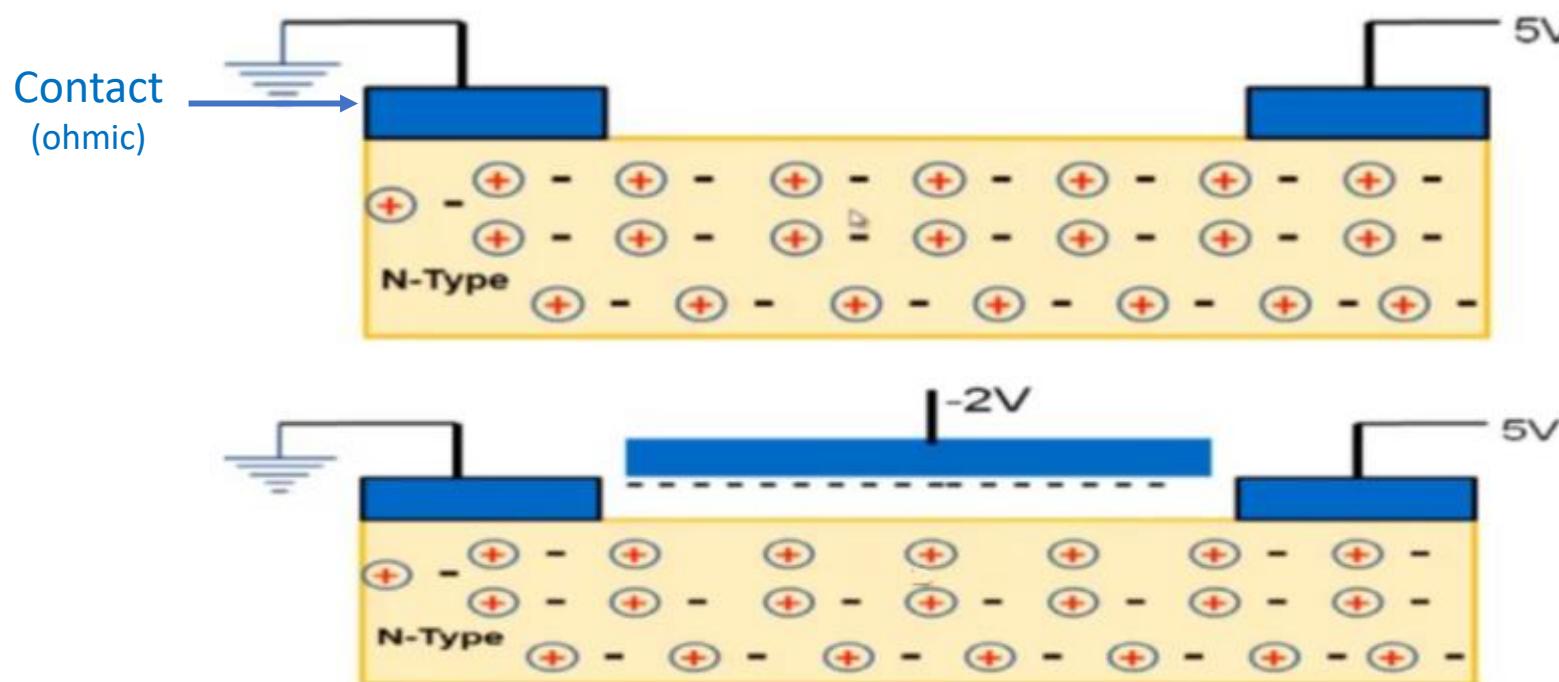
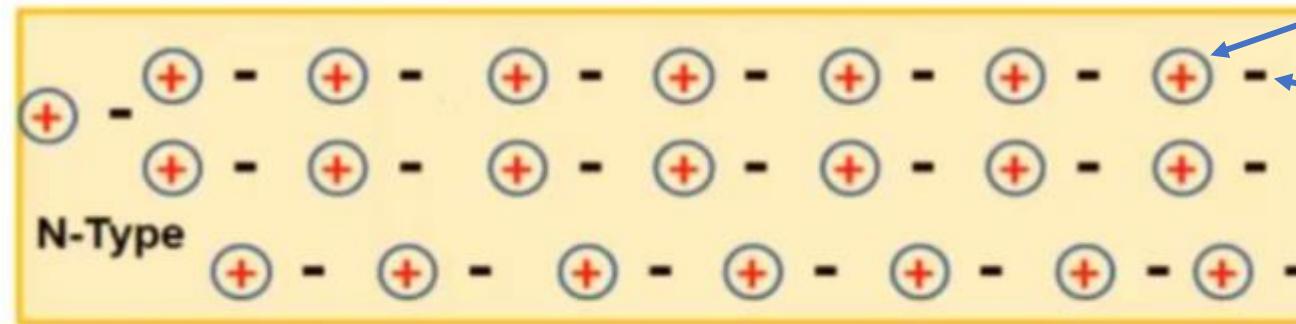


Current I_o is much more sensitive to V_{IN} than V_o

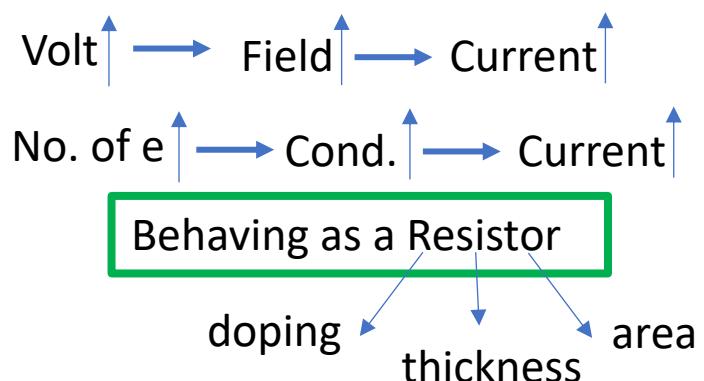
$$\frac{\partial I_o}{\partial V_{in}} \gg \frac{\partial I_o}{\partial V_o}$$

Field Effect Principle

$$\frac{\partial I_o}{\partial V_{in}} \gg \frac{\partial I_o}{\partial V_o}$$



- Amount of current flow depend on applied voltage



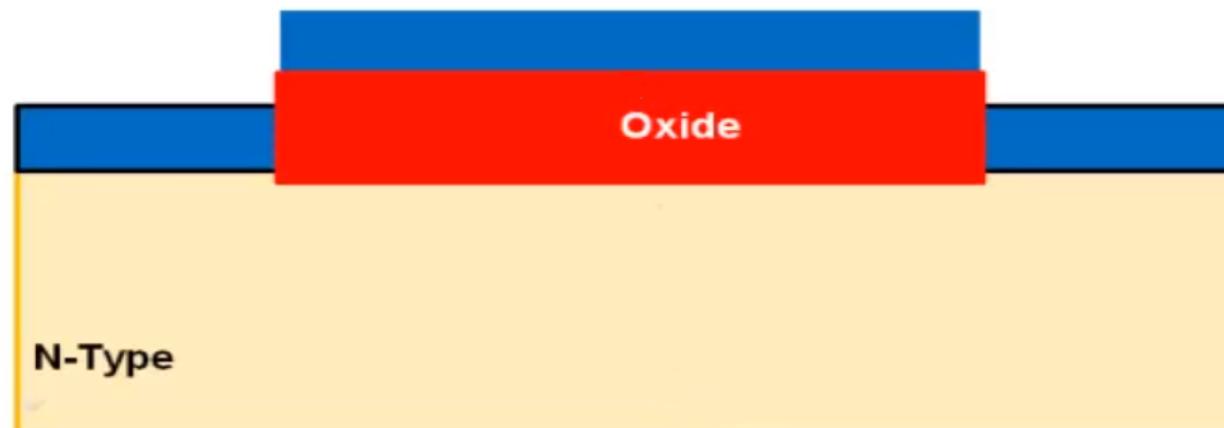
- Take another plate, place very close (by some means) to n-type semiconductor.
- Appy a negative voltage.
- Push the e away from the surface.

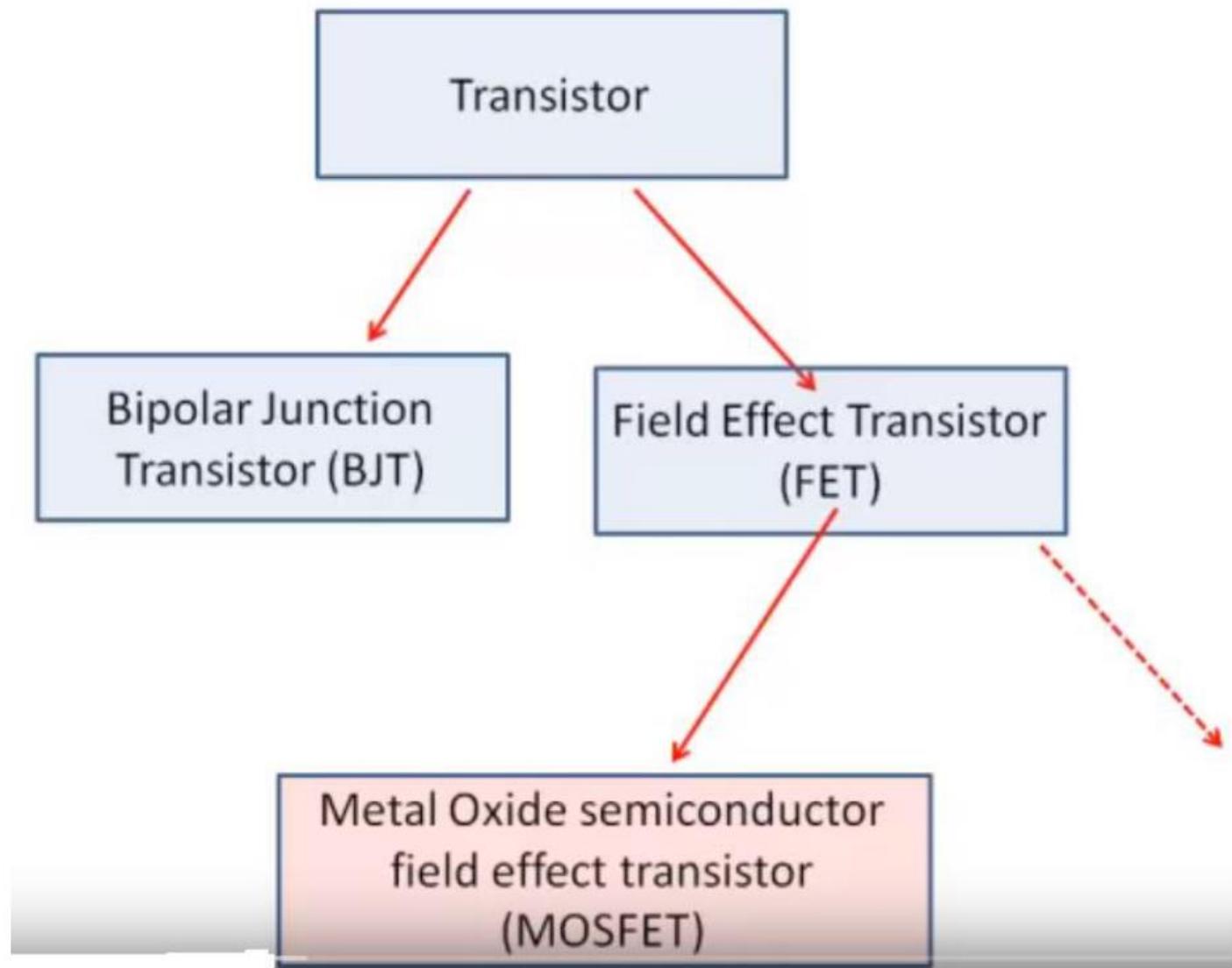
Capacitor

Modulation of conductivity using electric field

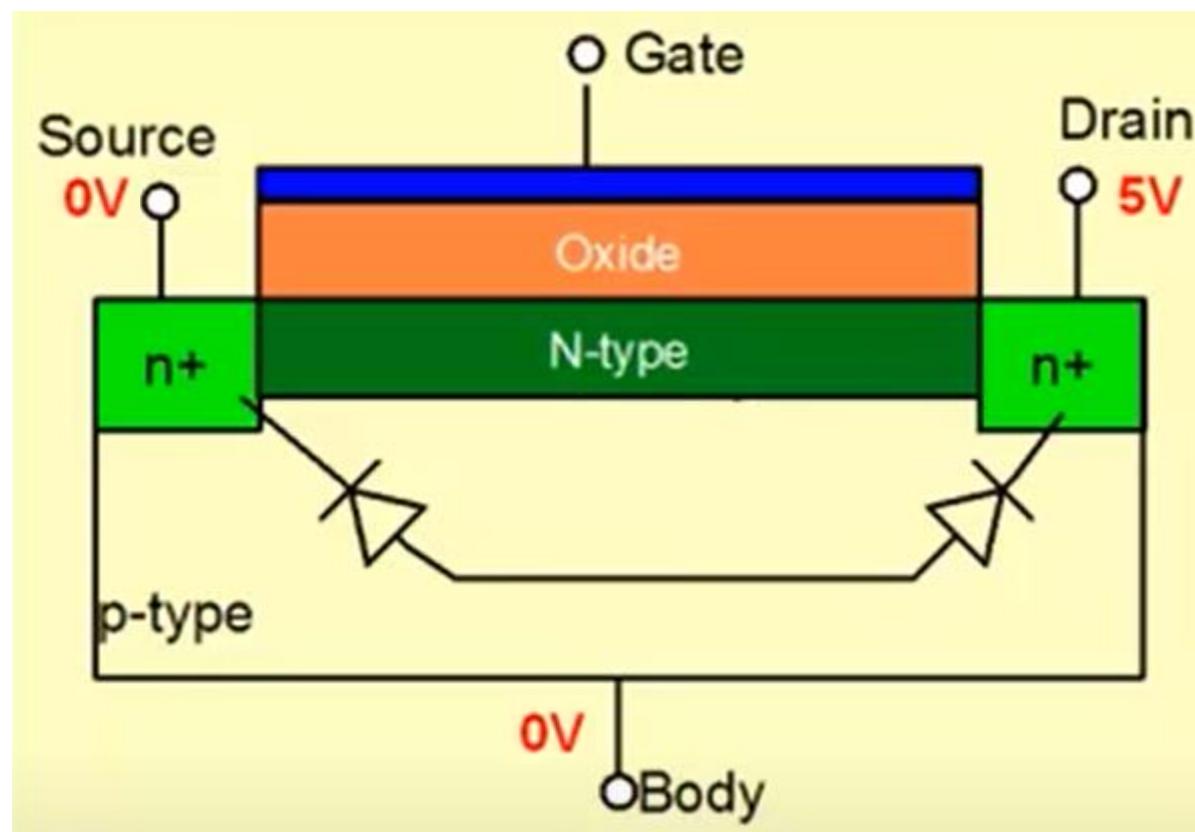
Transconductance

Field Effect Principle



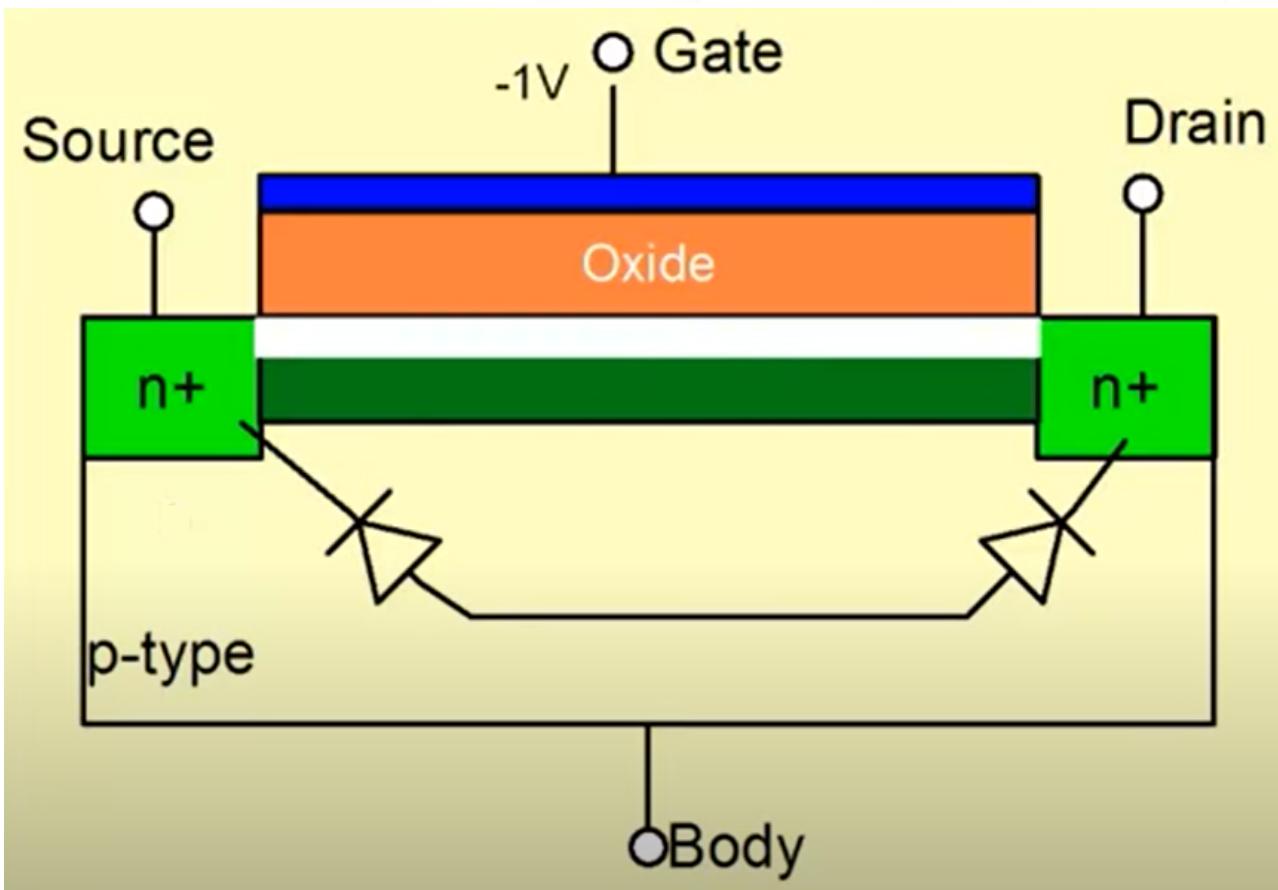


Depletion-Mode Transistor



Depletion-Mode Transistor

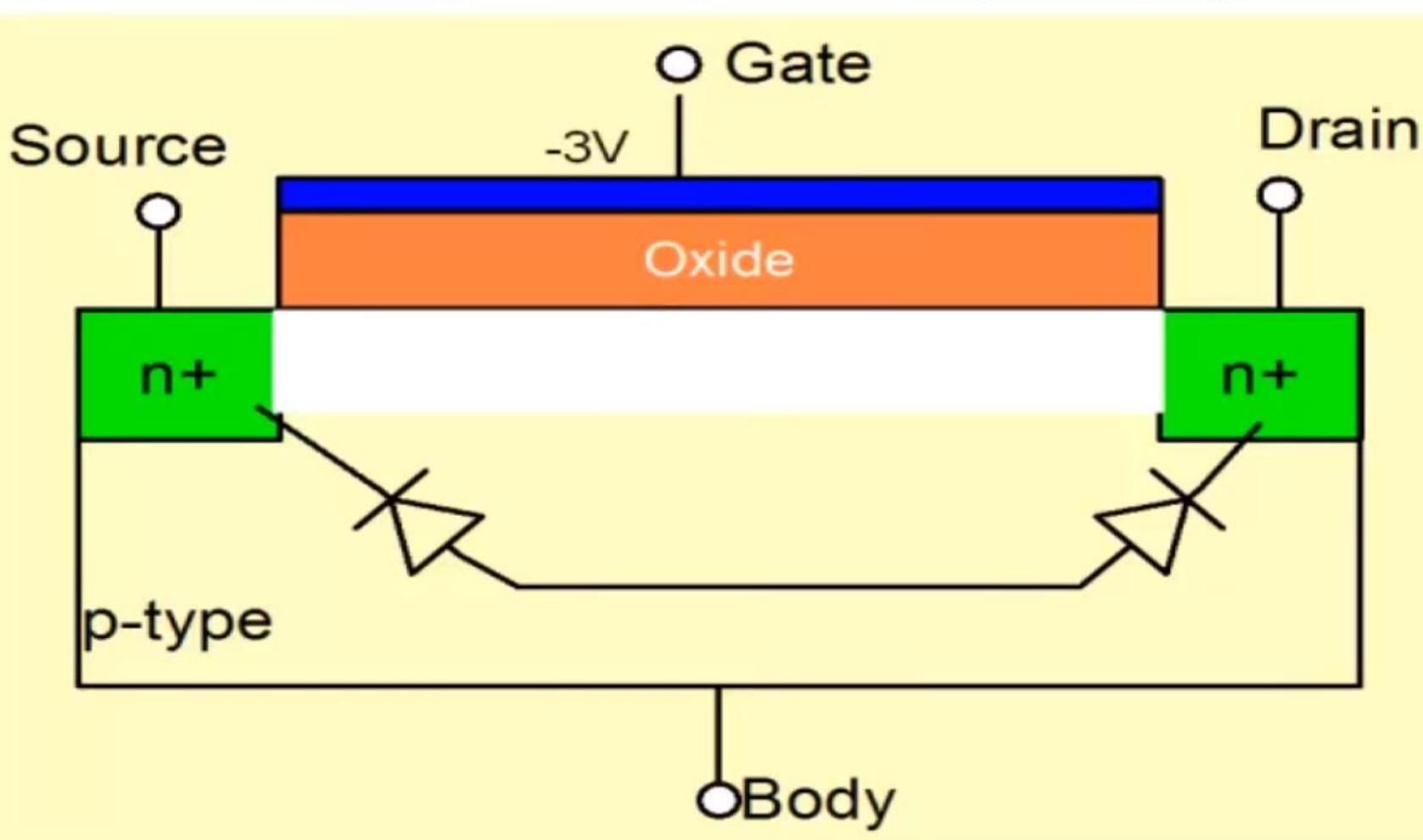
Channel exists at zero gate voltage and is depleted by gate voltage



In a depletion-mode transistor, a channel exists without any gate voltage being applied and current flows when drain voltage is applied.

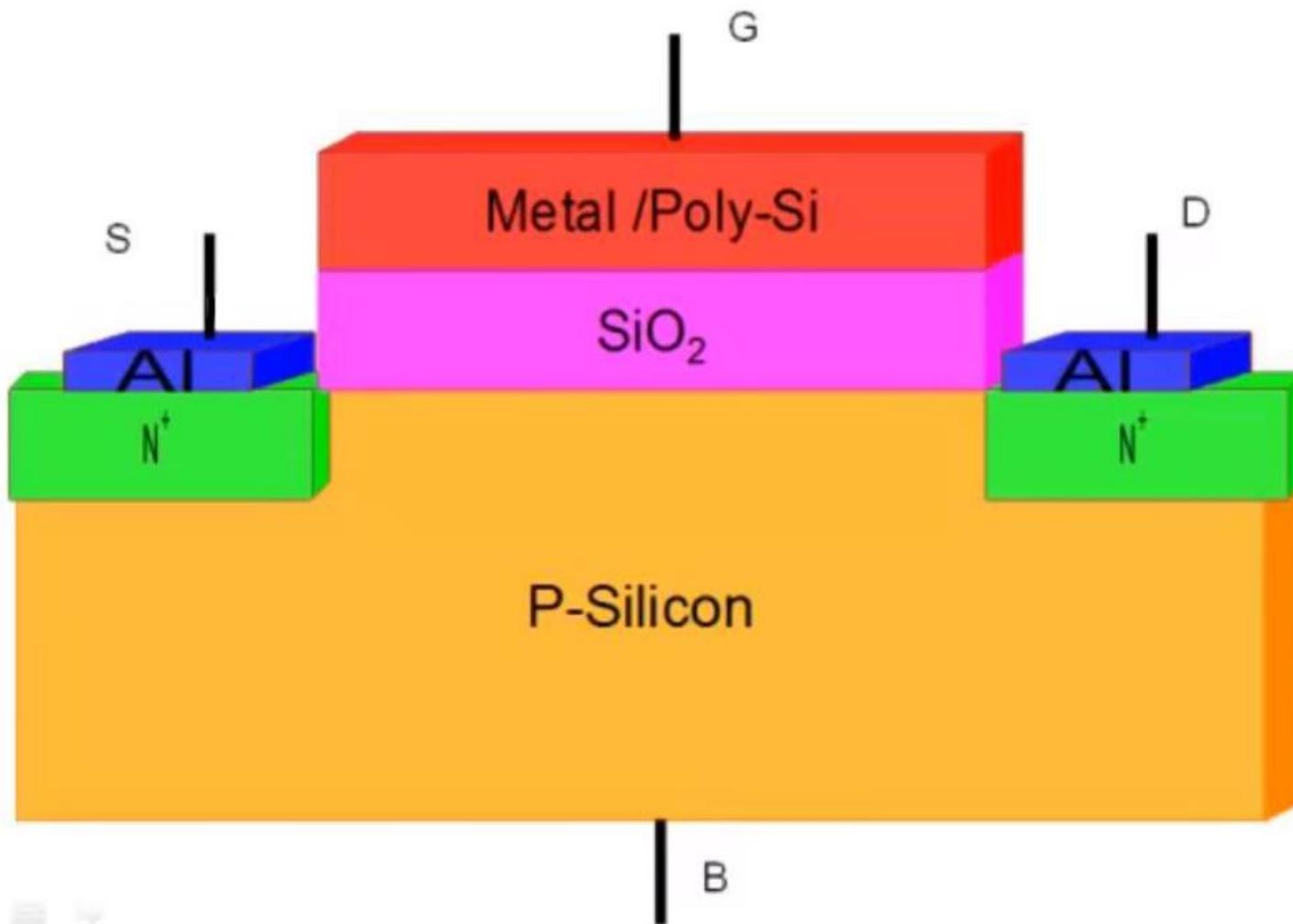
Negative gate voltage is applied to deplete the channel of carriers and cause current to reduce.

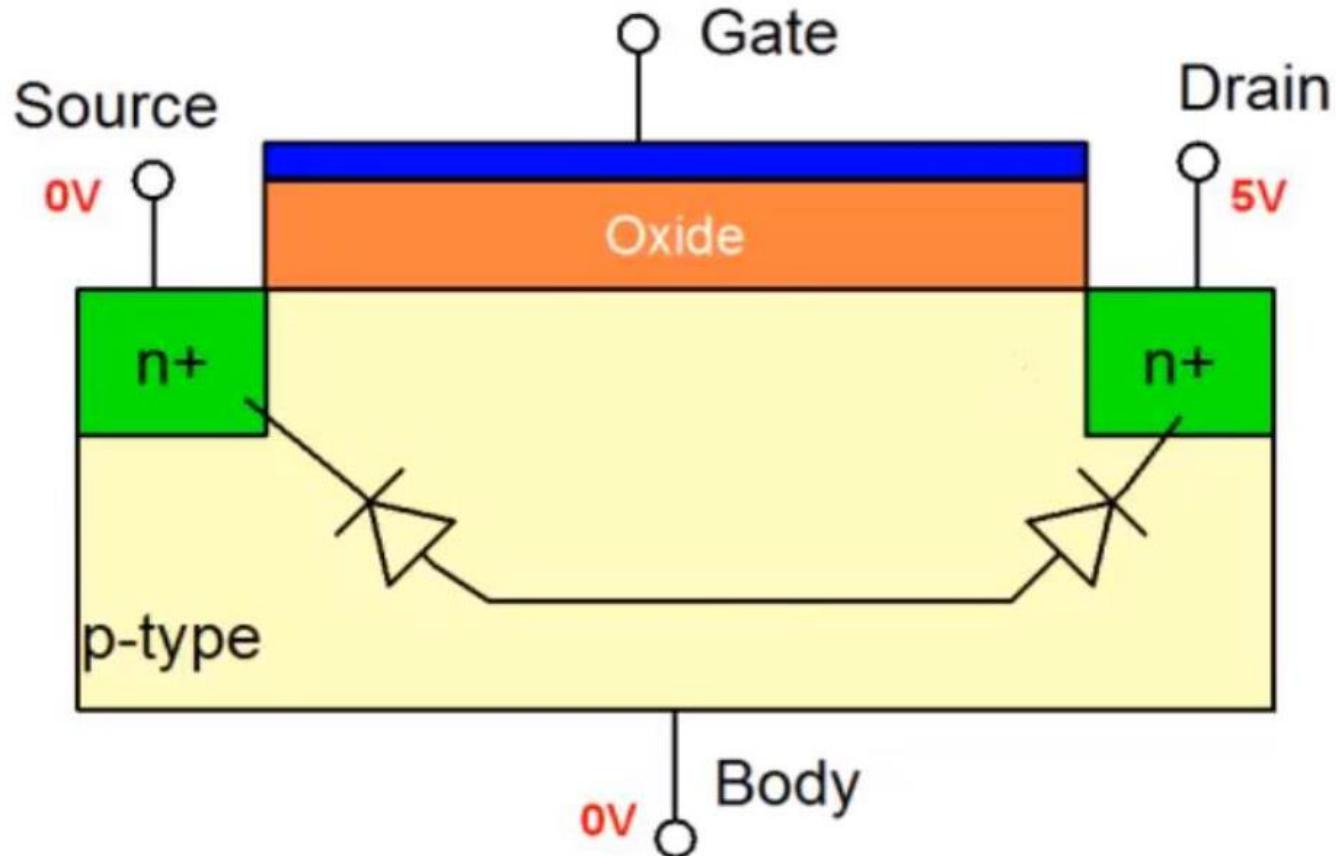
Channel exists at zero gate voltage and is depleted by gate voltage



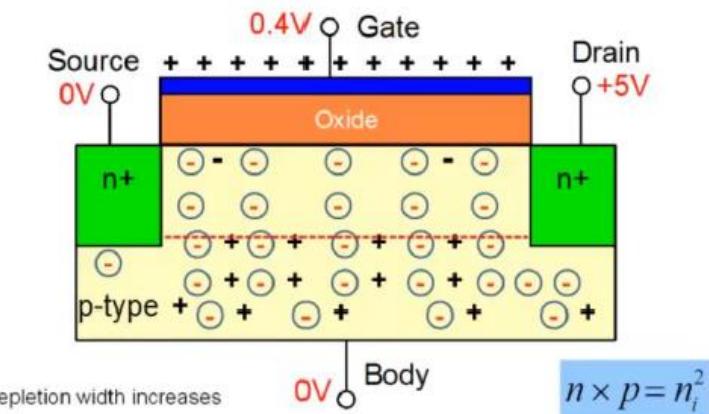
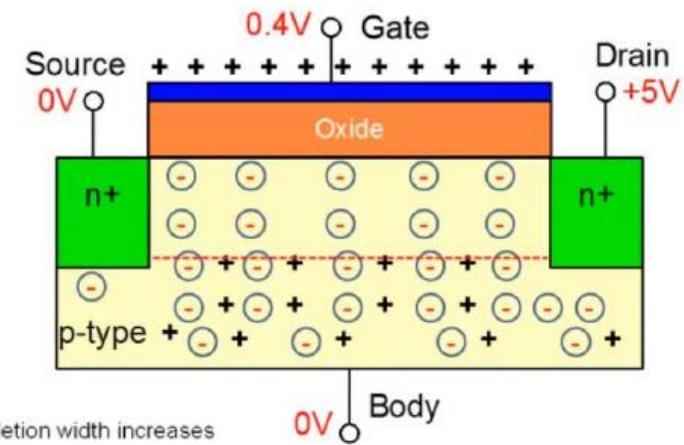
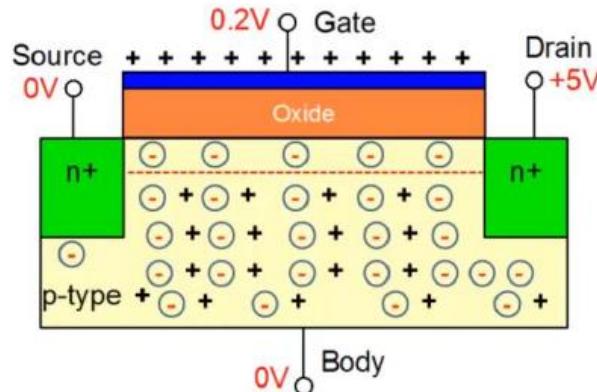
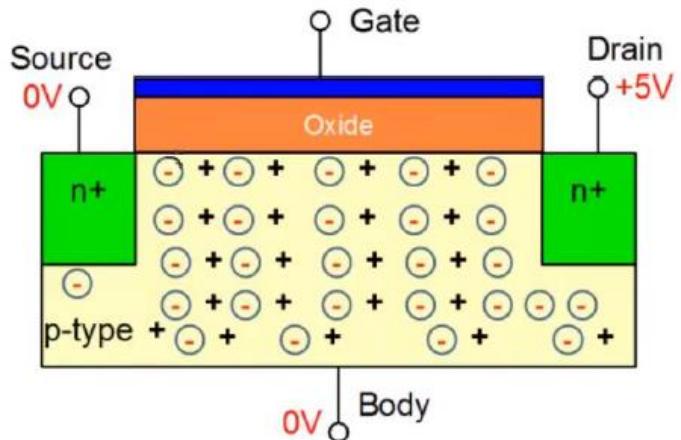
Channel is completely pinched off and current ~zero

NMOS Enhancement mode transistor: Inversion Mode Transistor



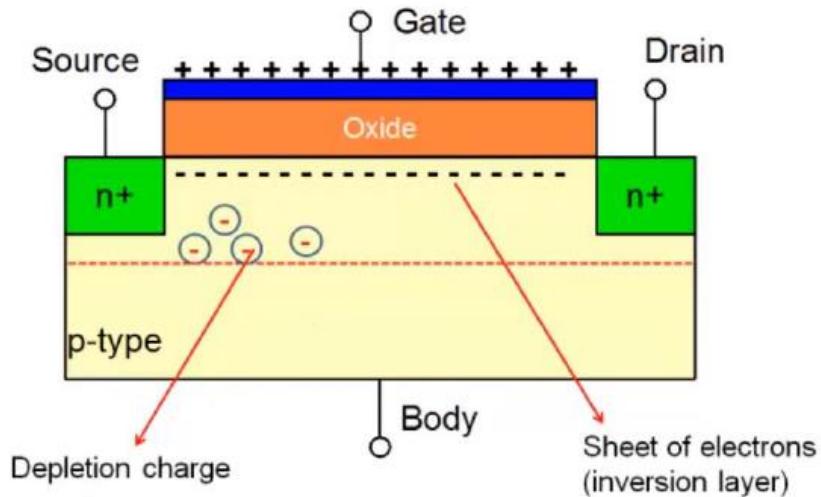


No channel exists when gate voltage is zero and current is zero as well.



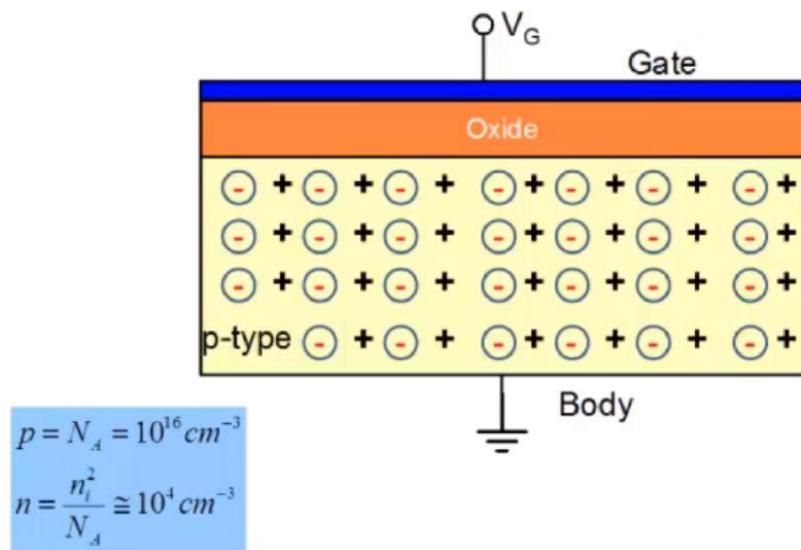
But something interesting happens: electron density at the surface also increases

At a sufficiently large voltage ($>V_{THN}$) a channel of electrons forms at the Si/SiO₂ interface.



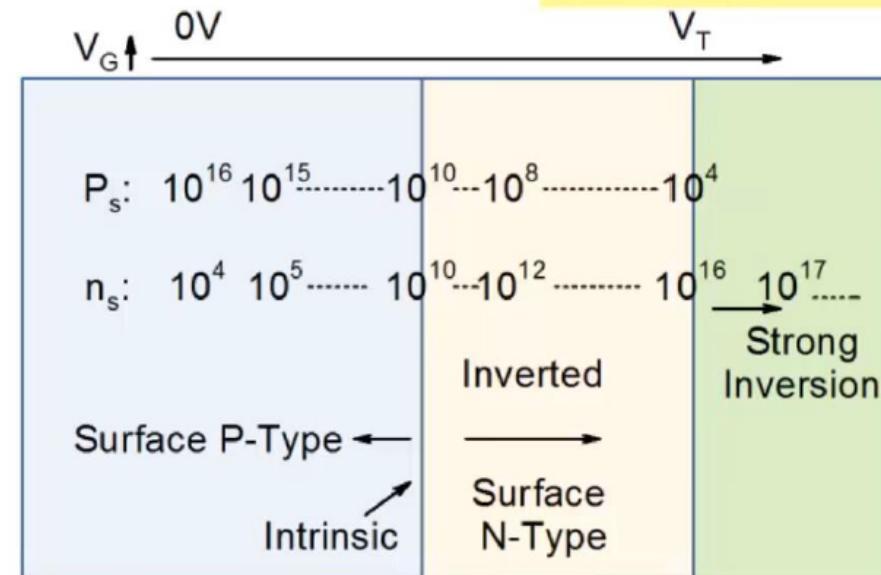
Conductivity modulation at the surface?

MOS capacitor constitutes the heart of a MOSFET



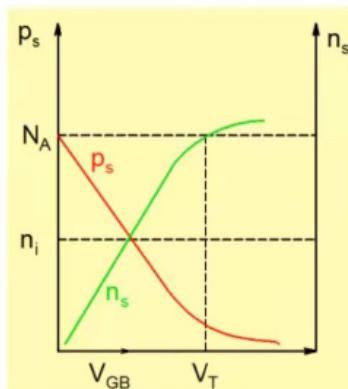
Field Effect...

$$n_s \times p_s = n_i^2 \cong 10^{20} \text{ cm}^{-3}$$



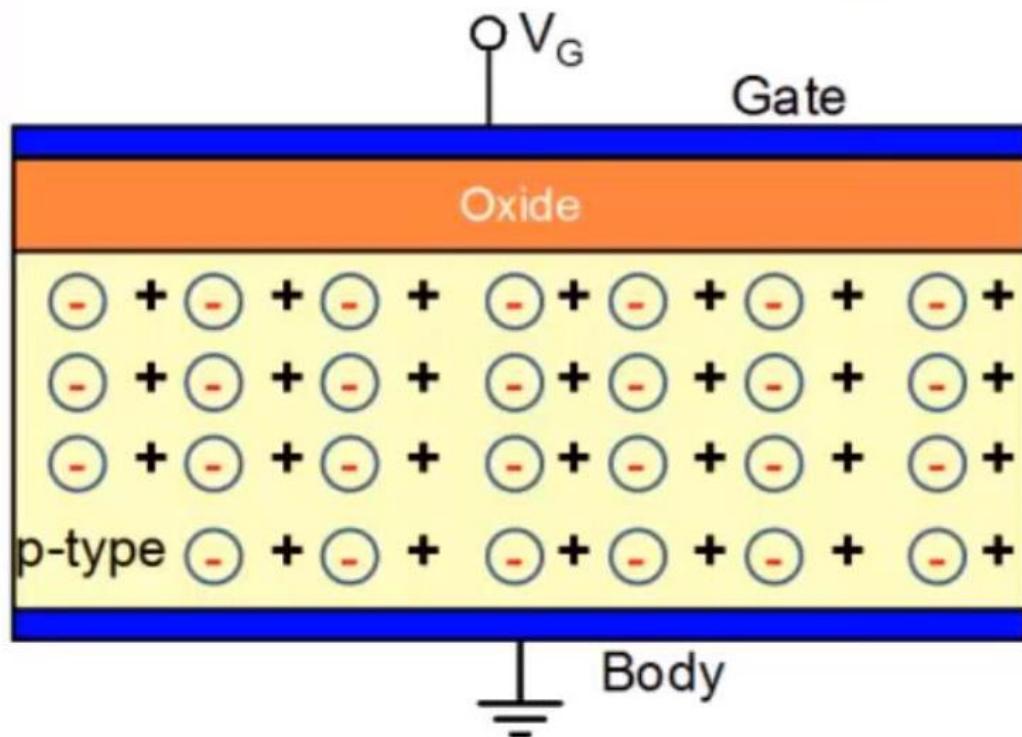
Surface carrier density can be changed from P-type to N-type

Surface Carrier Density



Flat band condition

$$V_G = V_{FB}$$

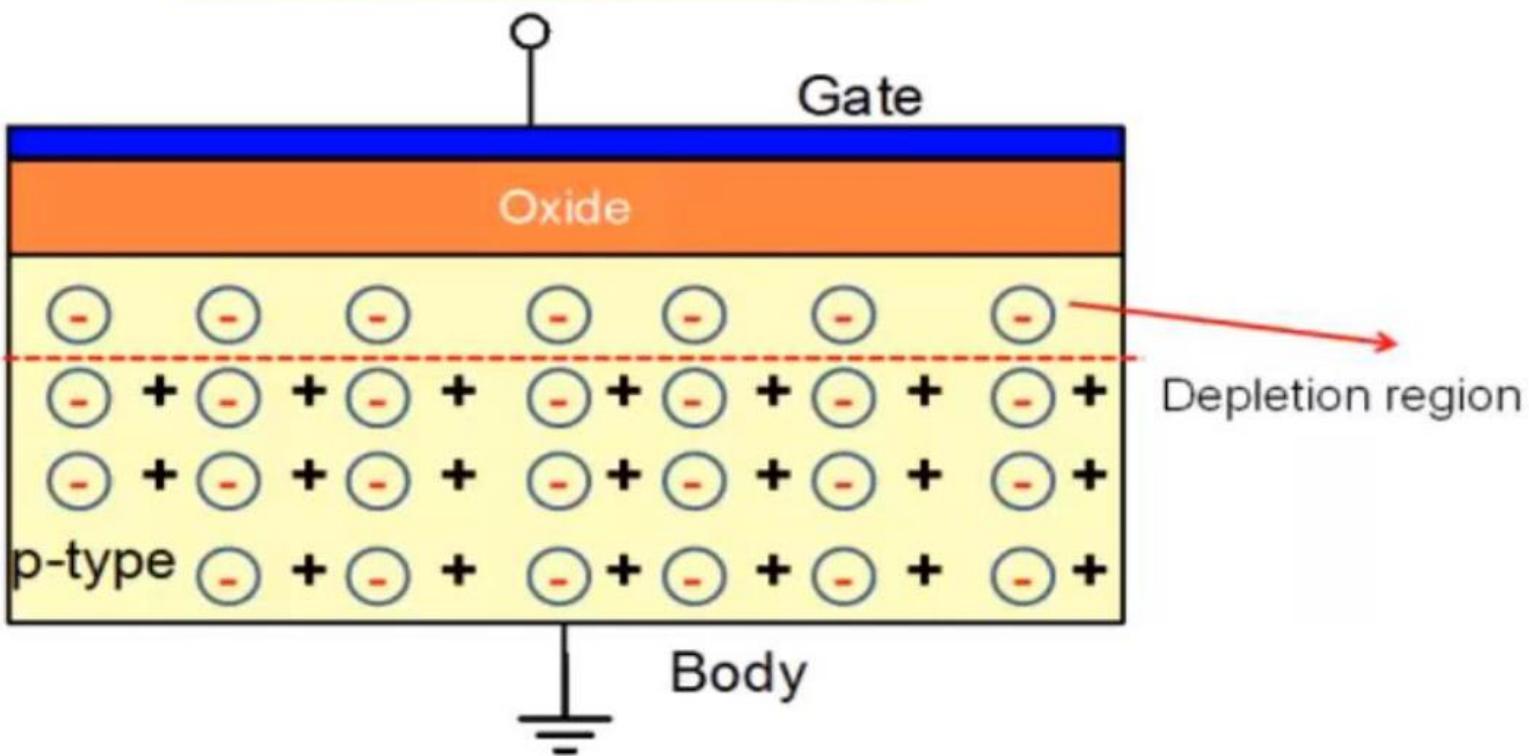


Whenever two different material are brought into contact, an internal potential difference develops like in a pn junction. Thus even when no gate voltage is applied, there is a voltage across the mos capacitor.

$V_G = V_{FB}$; Flat-band condition meaning no NET voltage across the capacitor.
Uniform hole density everywhere

Depletion

$$V_G > V_{FB} \text{ but } V_G < V_{THN}$$

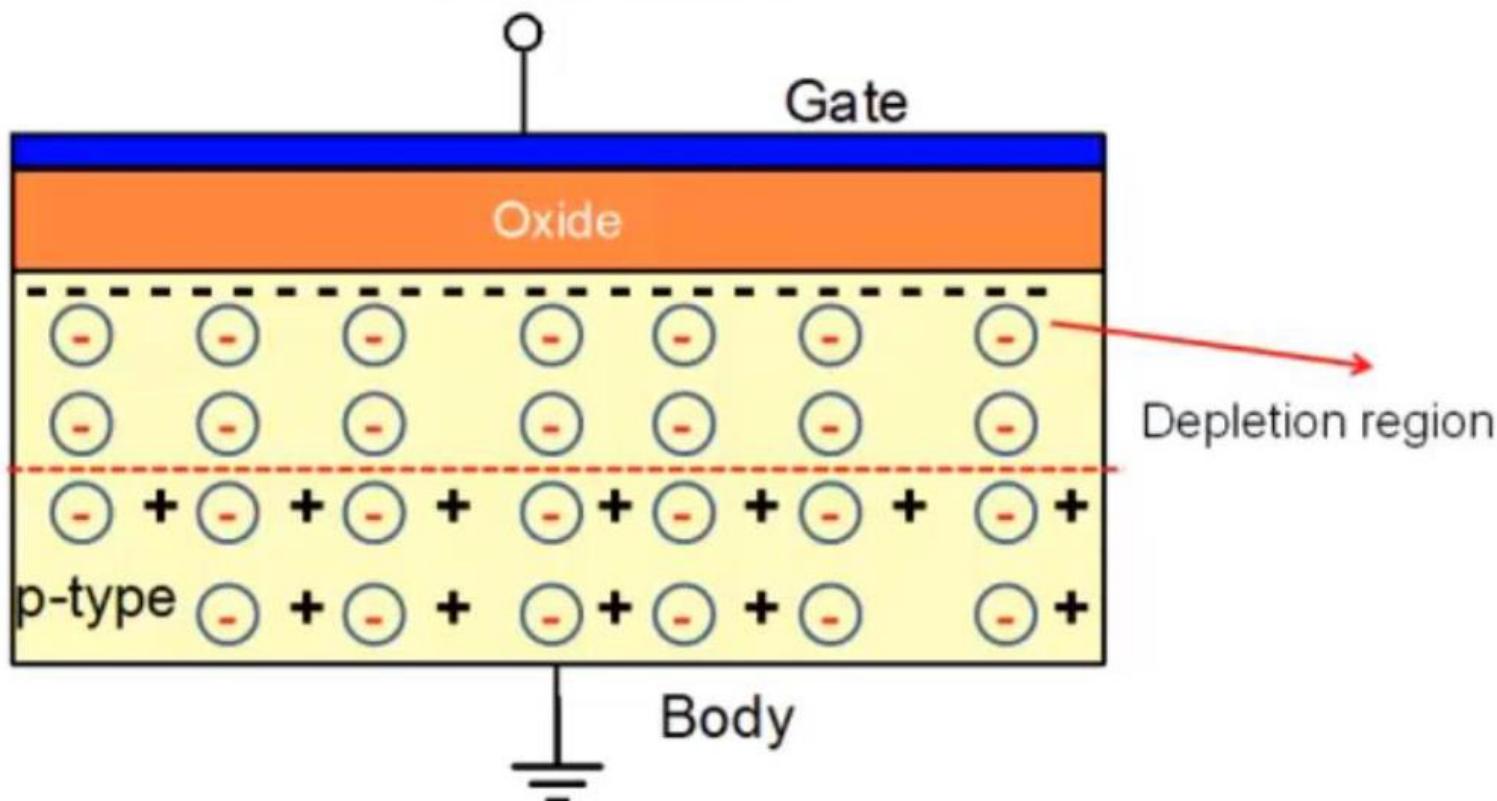


Holes are depleted from the surface $p_S < p_B$

Although $n_s > n_B$ electron density is also very small

Strong Inversion

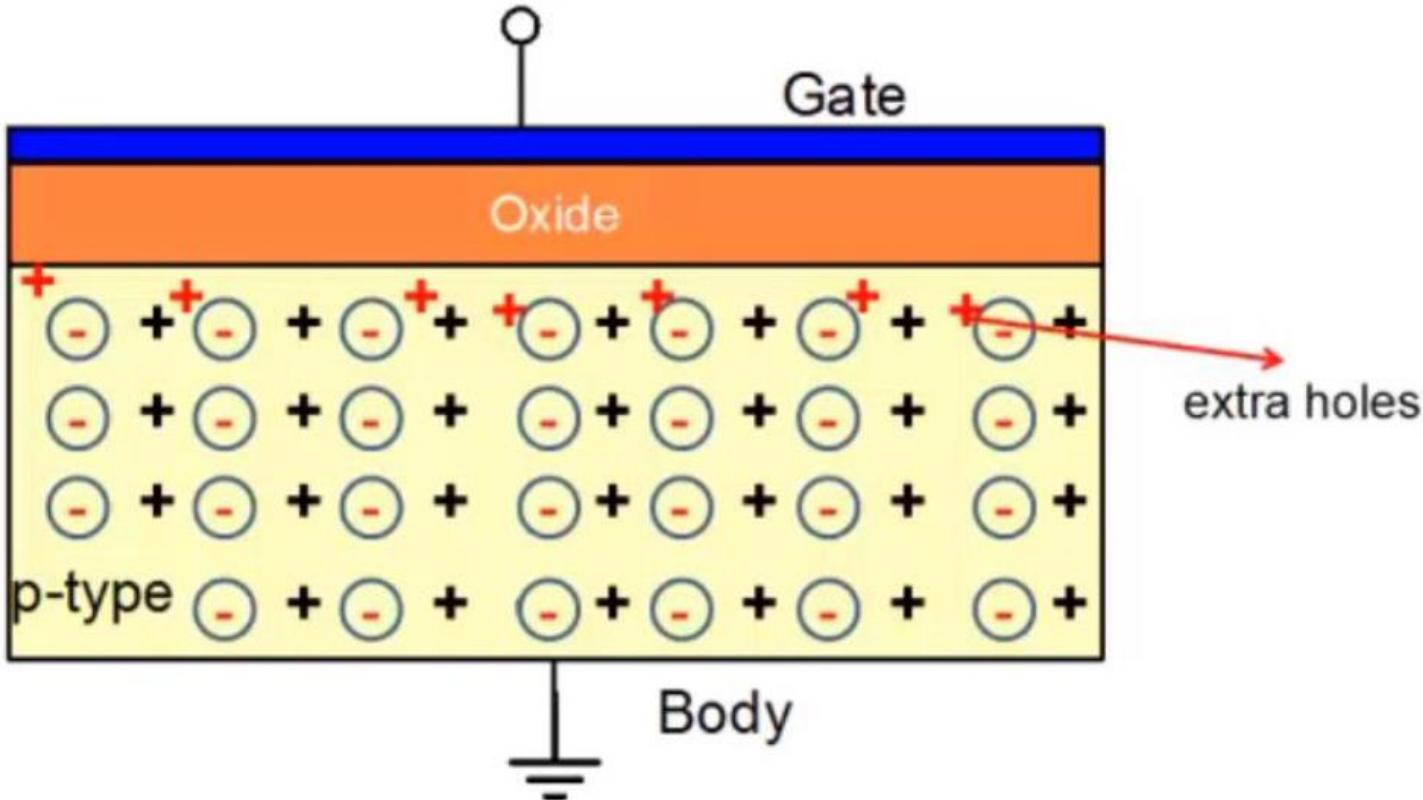
$$V_G > V_{THN}$$



Electrons are accumulated at the surface $n_s \gg N_A$

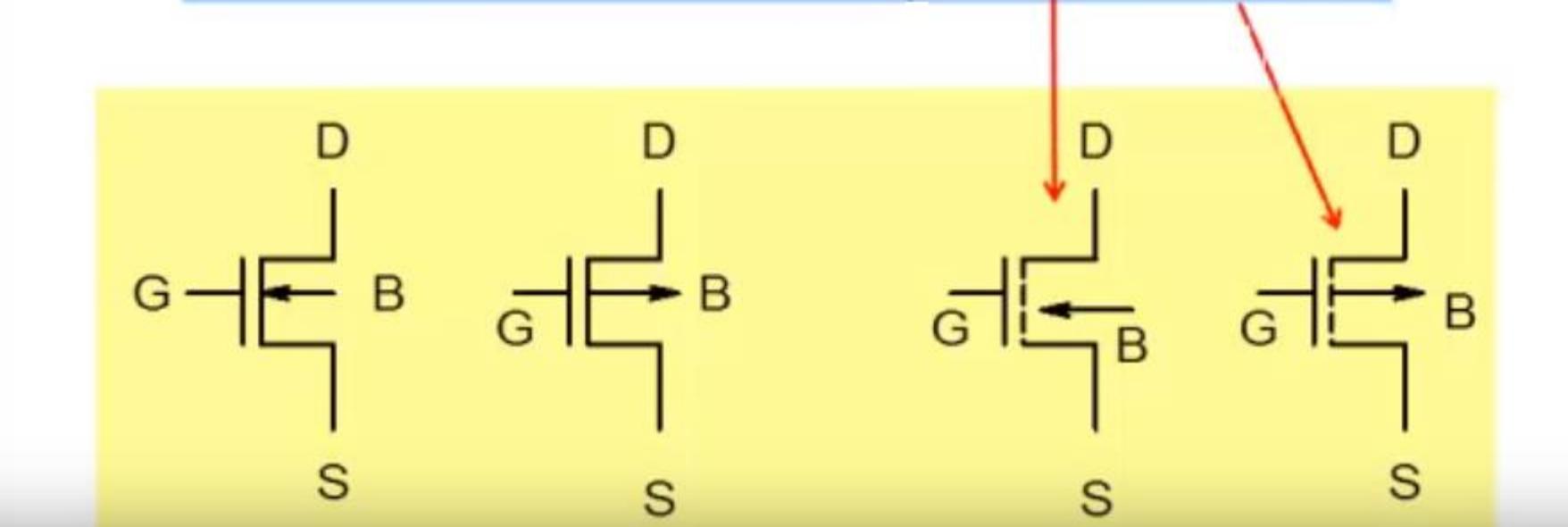
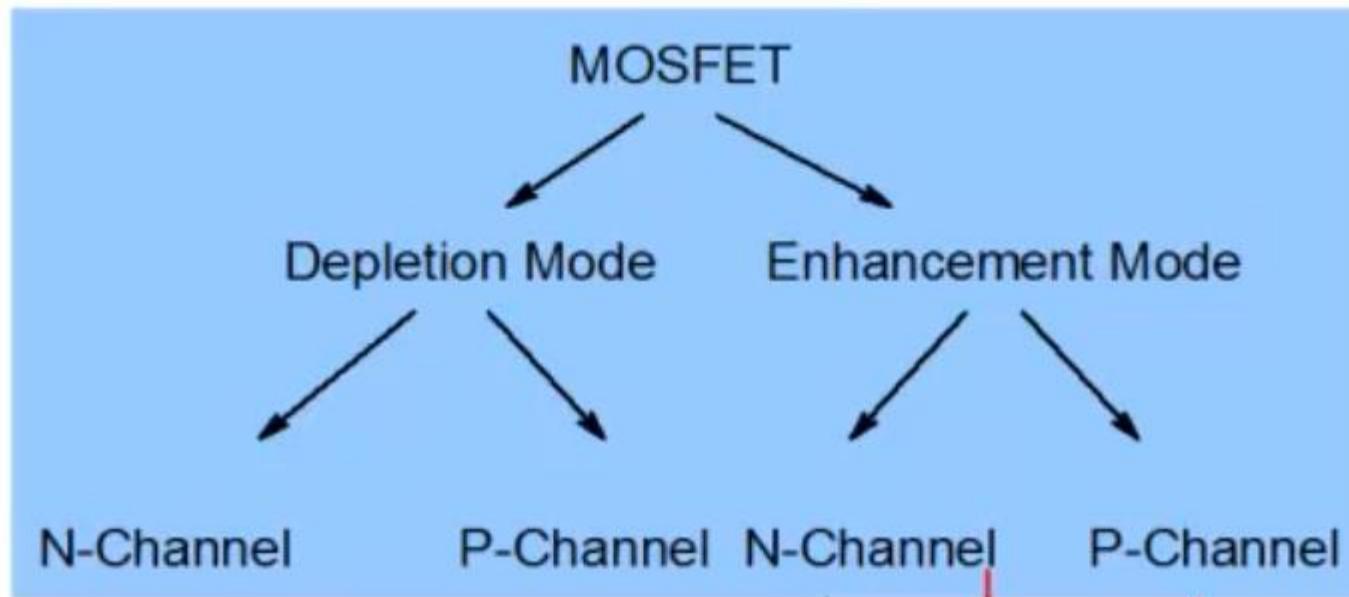
Accumulation

$$V_G < V_{FB}$$

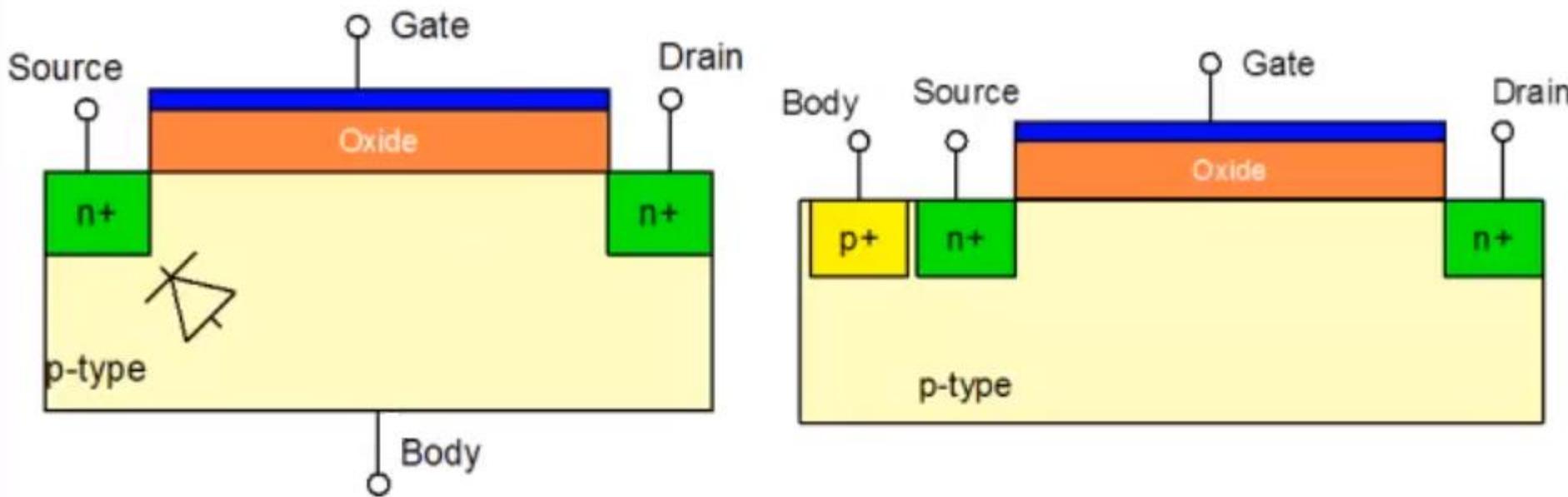
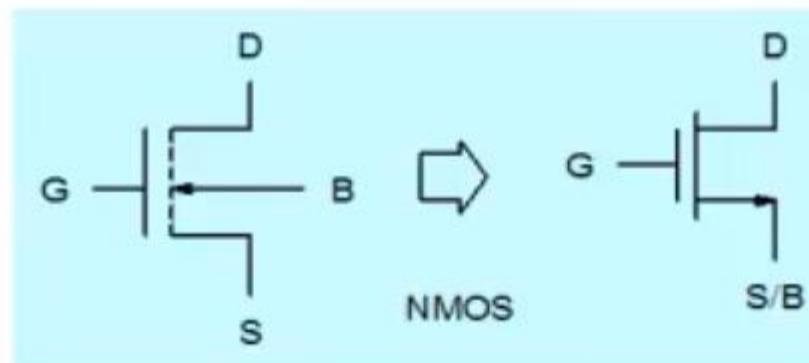


Holes are accumulated at the surface $p_s > p_b$

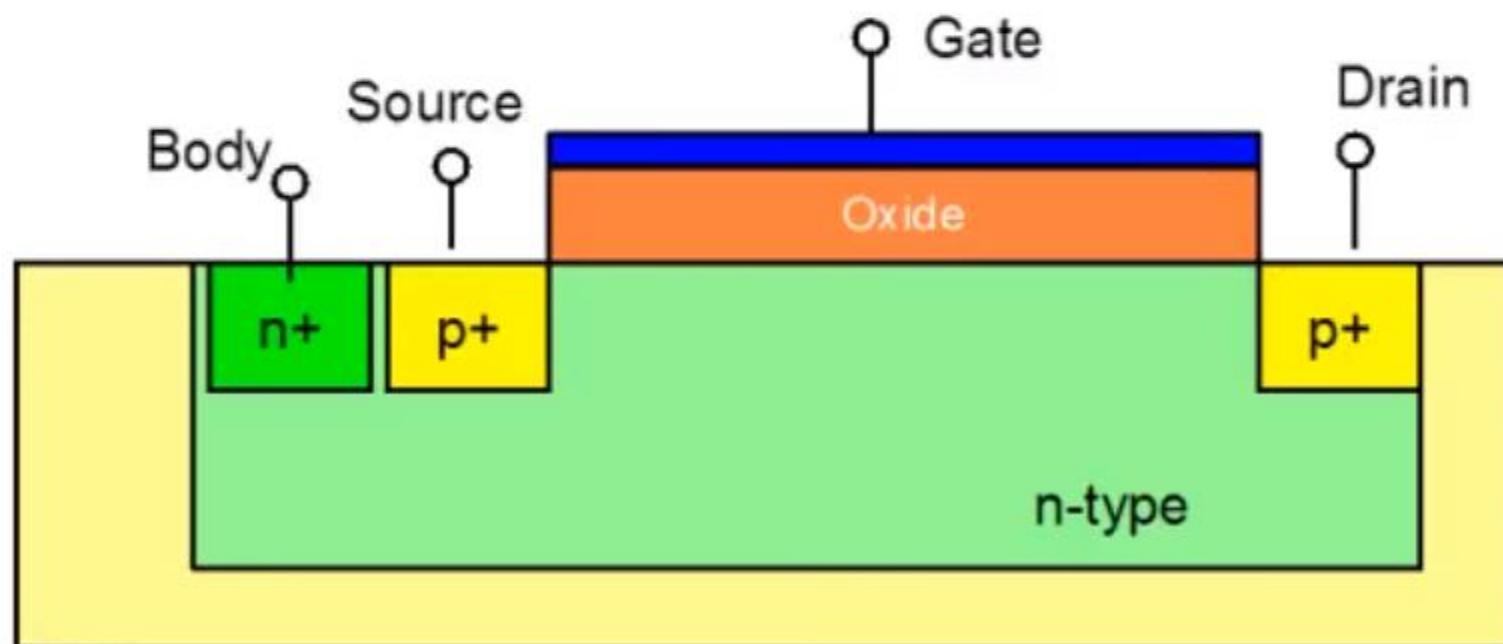
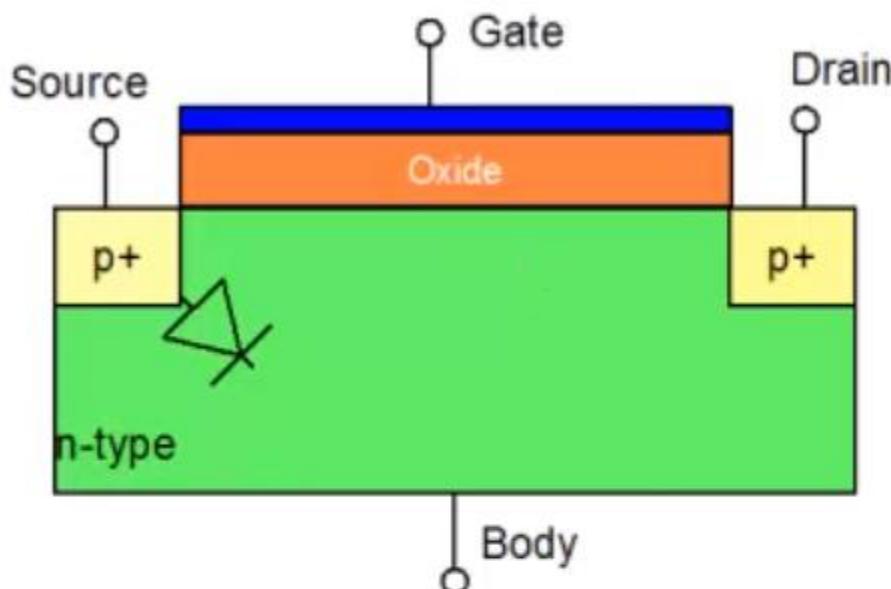
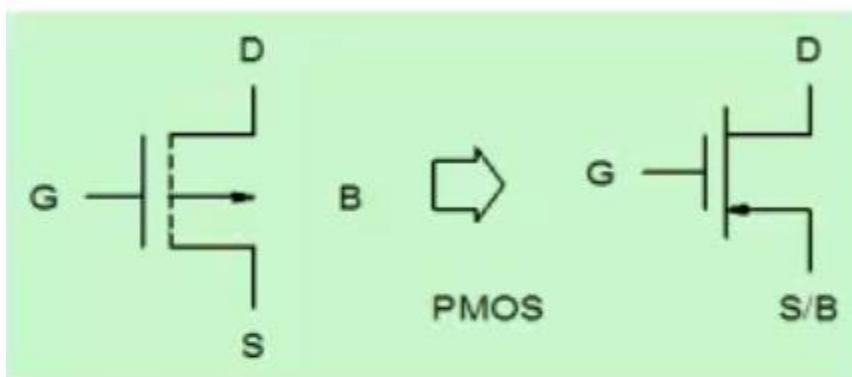
Metal Oxide Semiconductor Field Effect Transistor:

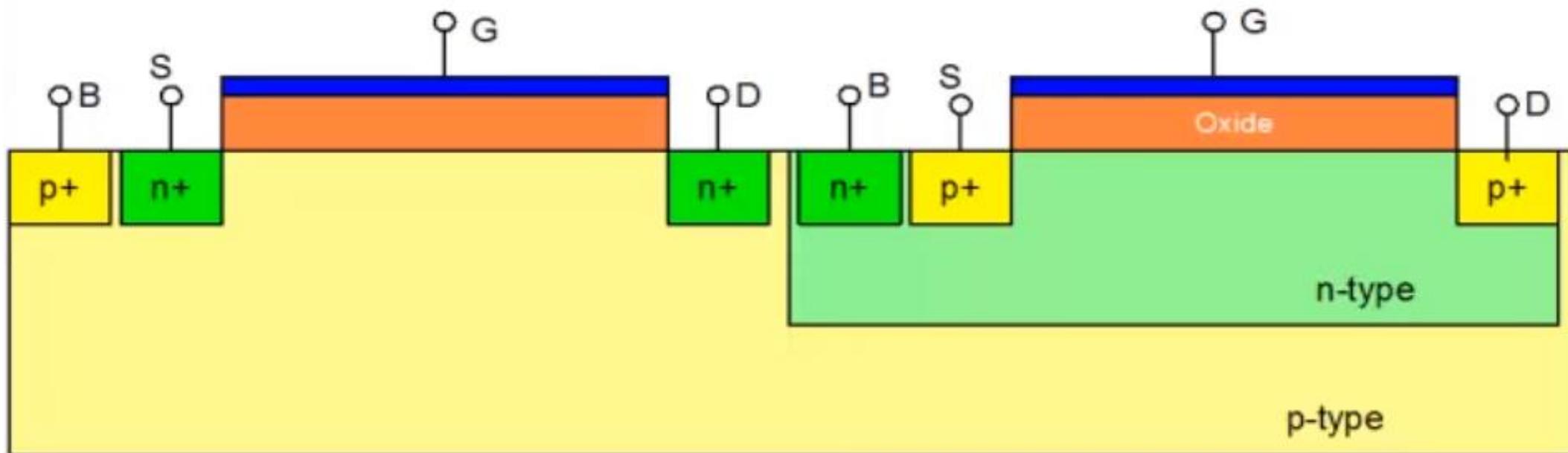


Simplified Symbols and structure

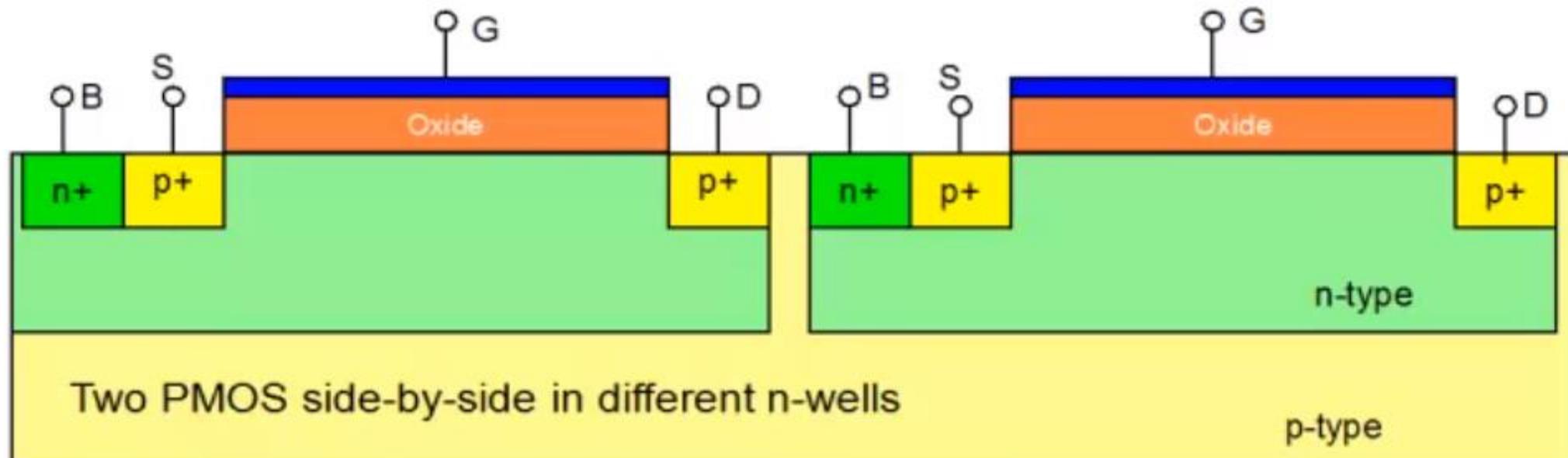
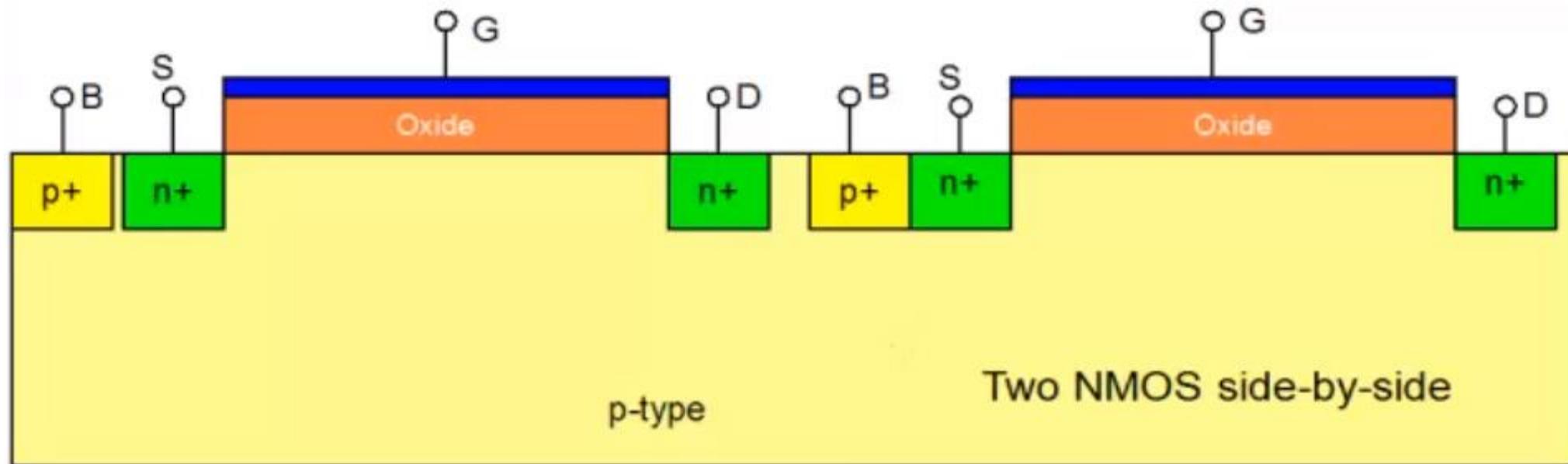


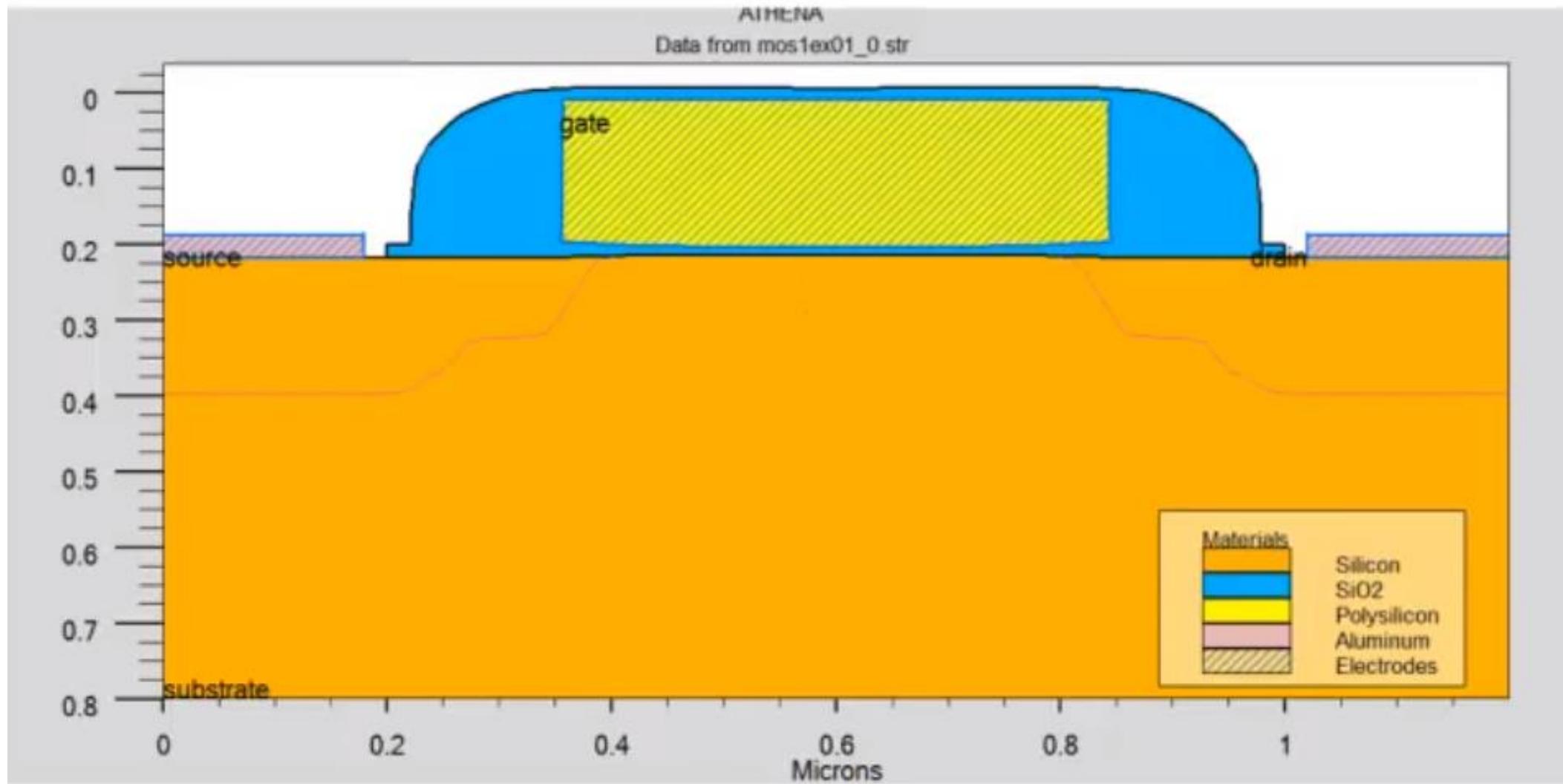
Simplified Symbols and structure

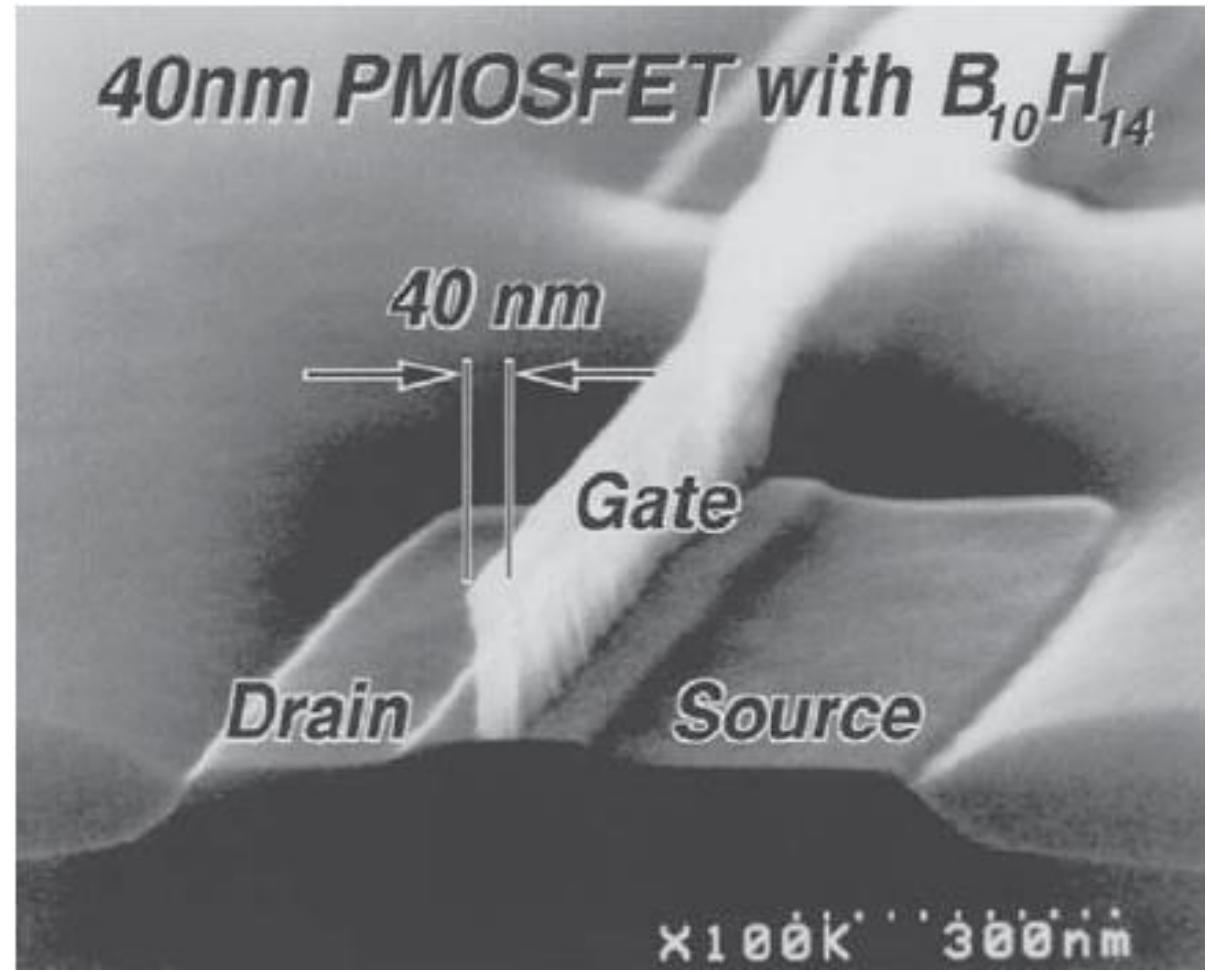
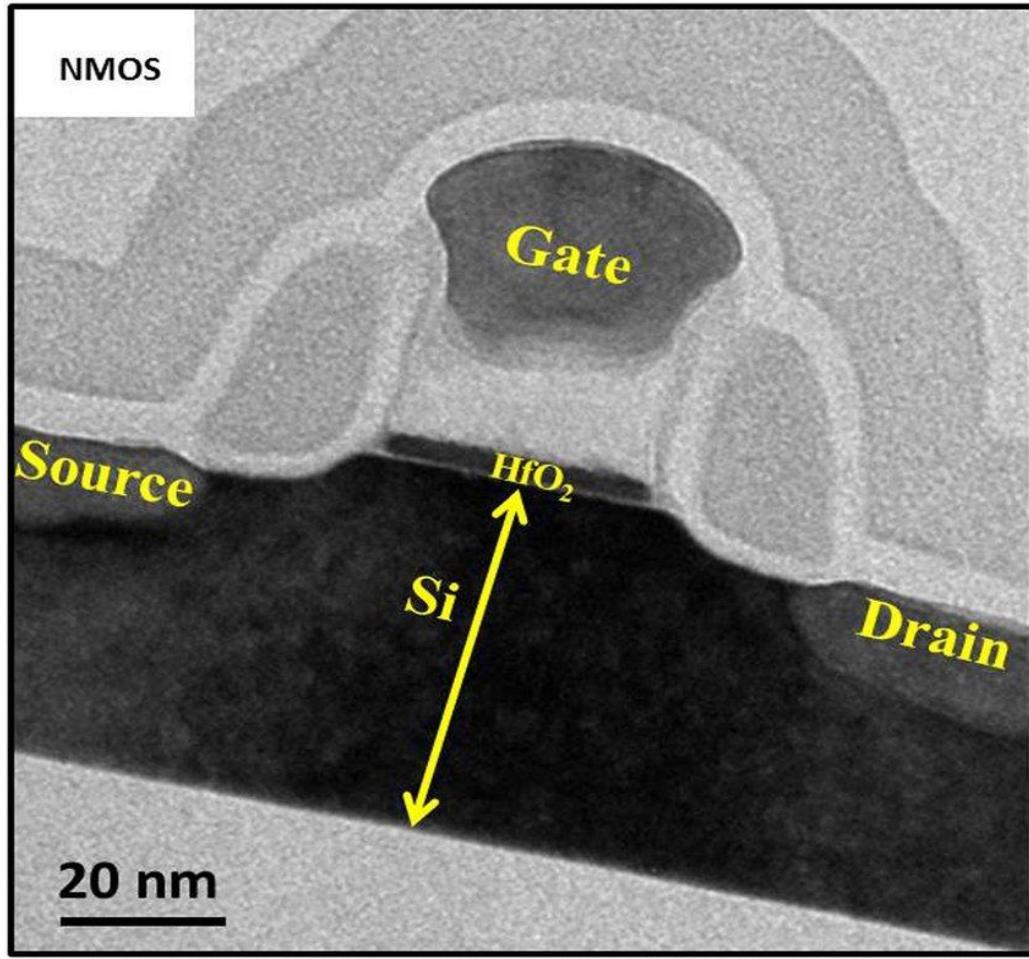




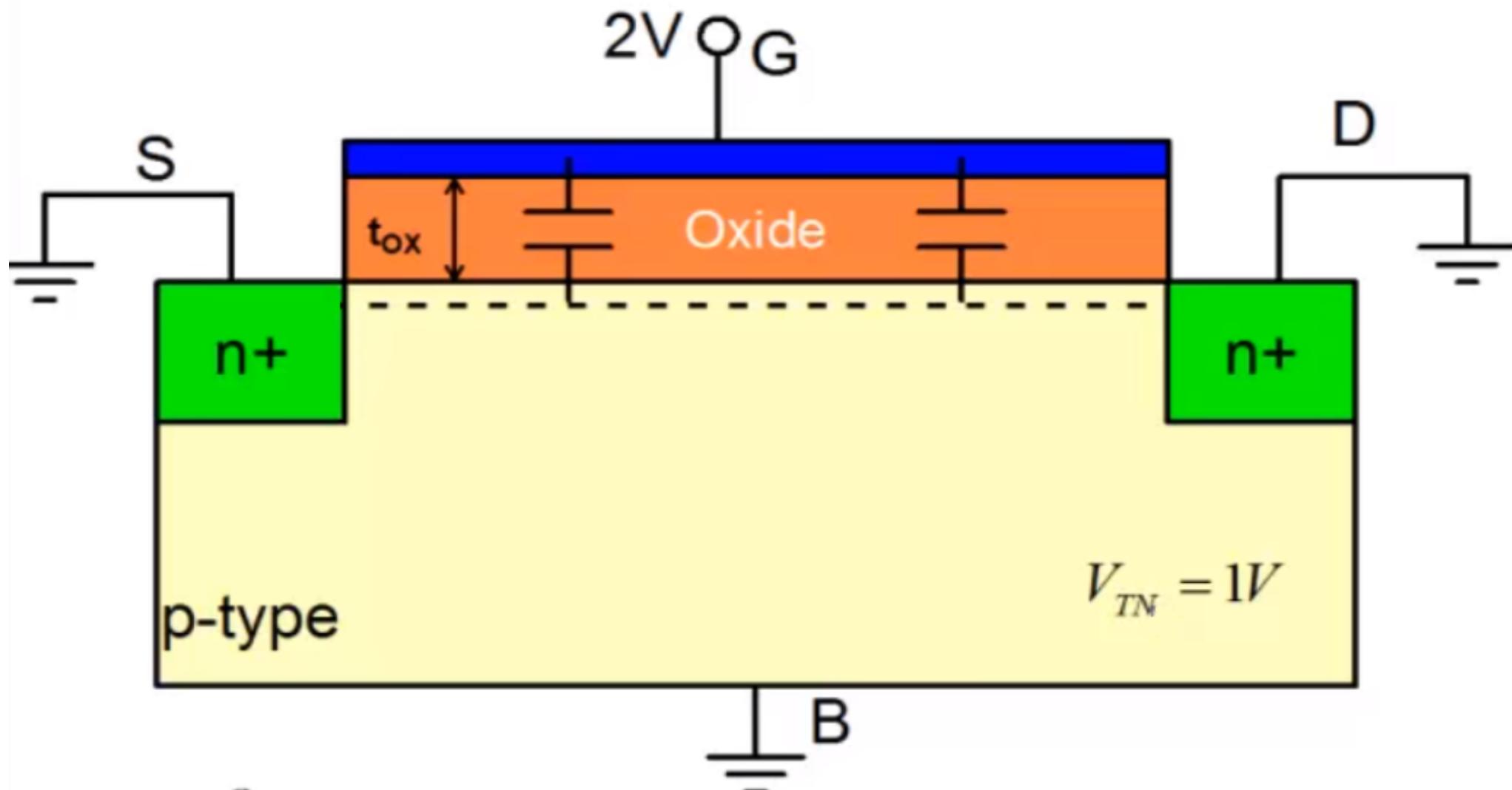
- Body potential of NMOS transistors is same and is normally connected to the most negative voltage in the circuit to ensure that $V_{BS} < 0$ and thus body-source PN junction is reverse biased.
- Each PMOS can be fabricated in a separate individual N-well and thus each pmos body terminal can have a distinct voltage. Normally body and source terminals of PMOS are shorted together.







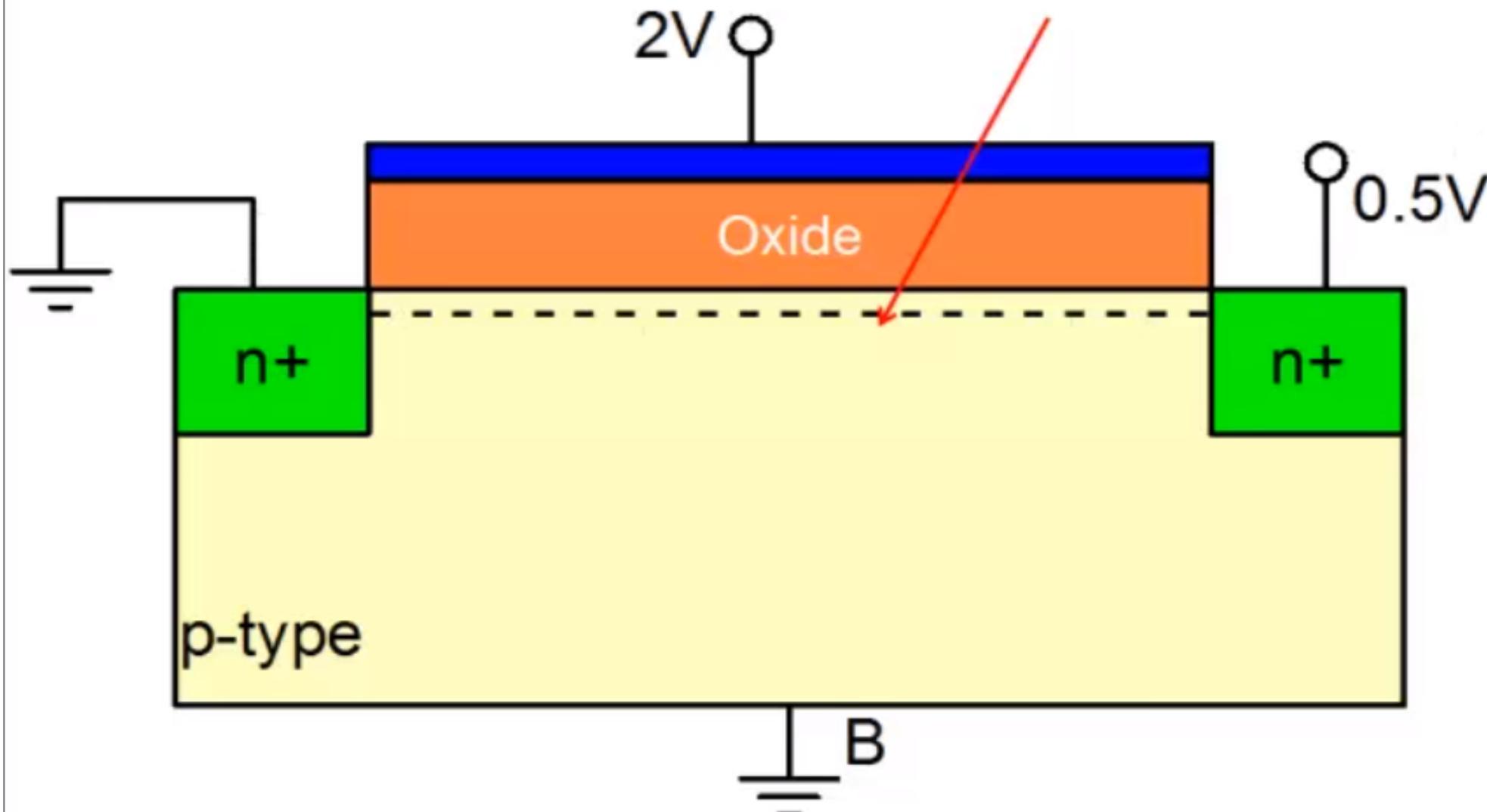
Operation of the MOSFET



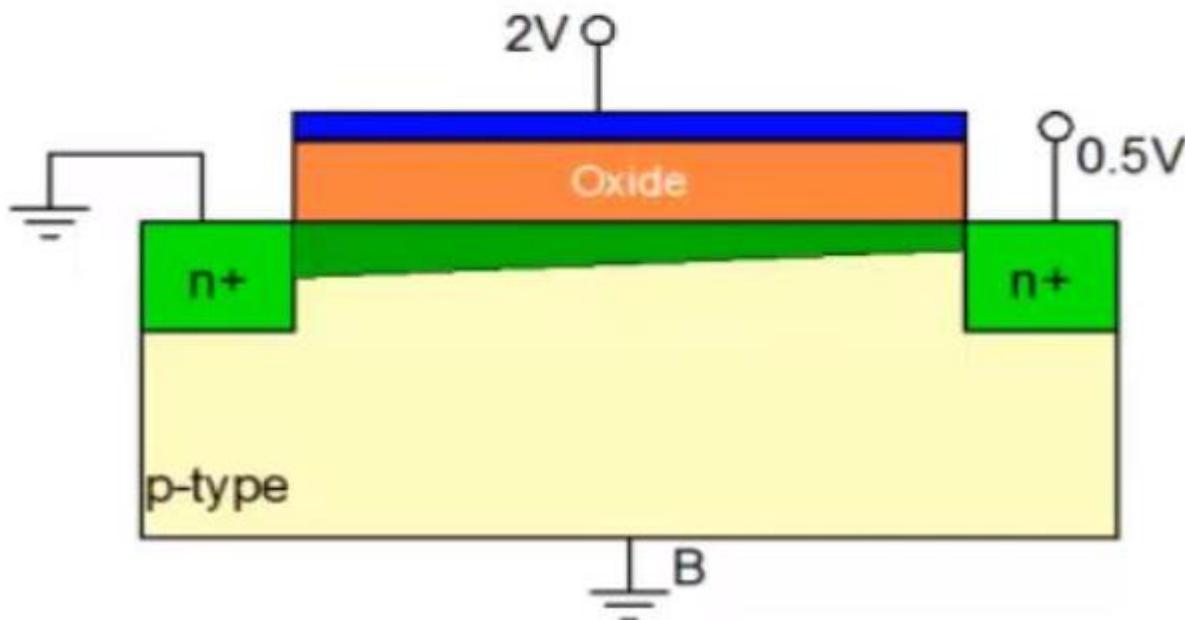
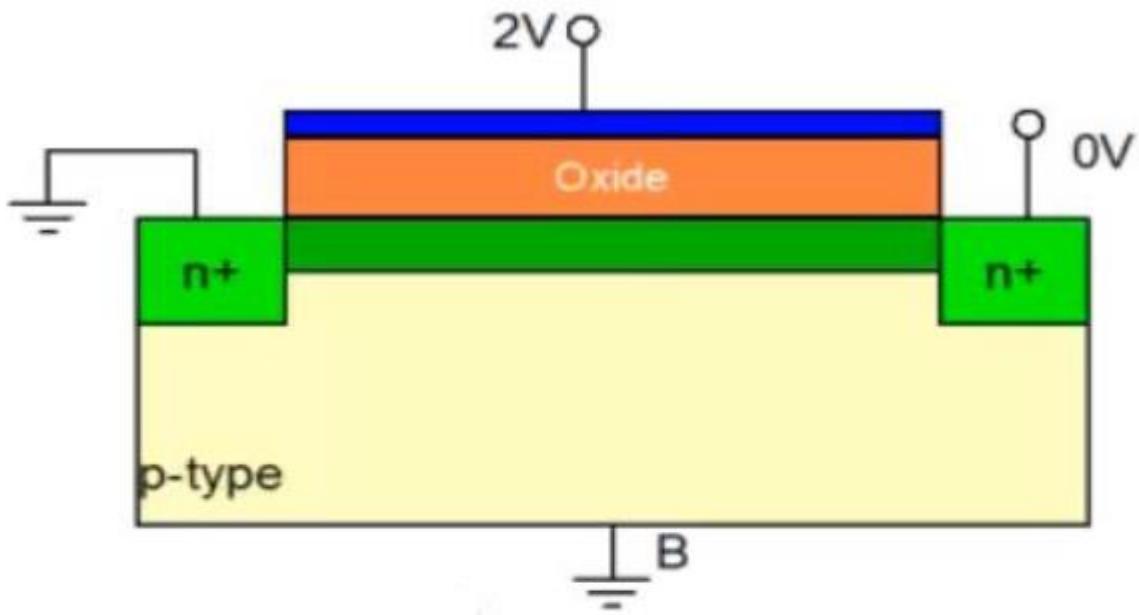
$$C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

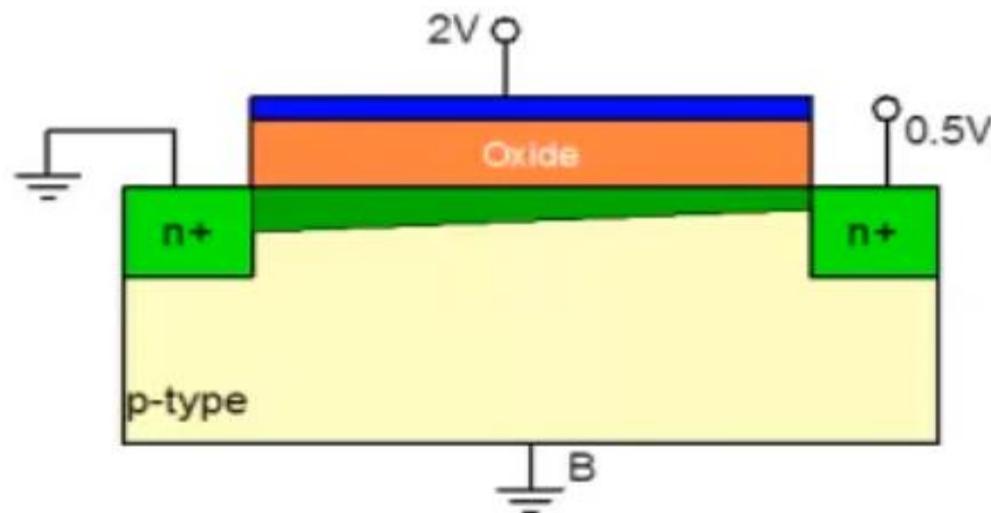
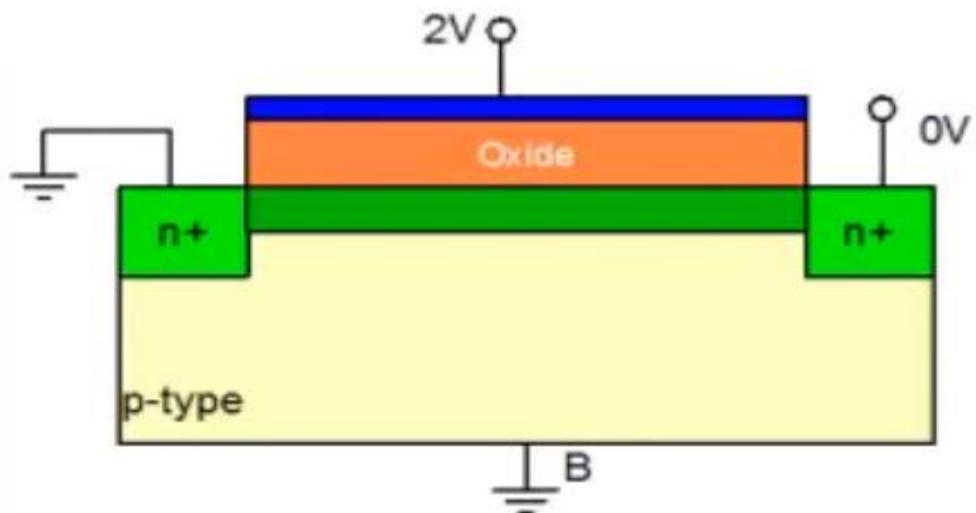
Inversion charge/area : $Q_{inv} = -C_{ox}(V_{GS} - V_{THN})$

$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V(x))$$



When a positive drain voltage is applied, current flows from drain to source and inversion charge density decreases from source to drain end.





$$dR_{ch} = \frac{1}{q\mu n(x)} \frac{dx}{W \times t}$$

$$R_{ch} > R_{cho}$$

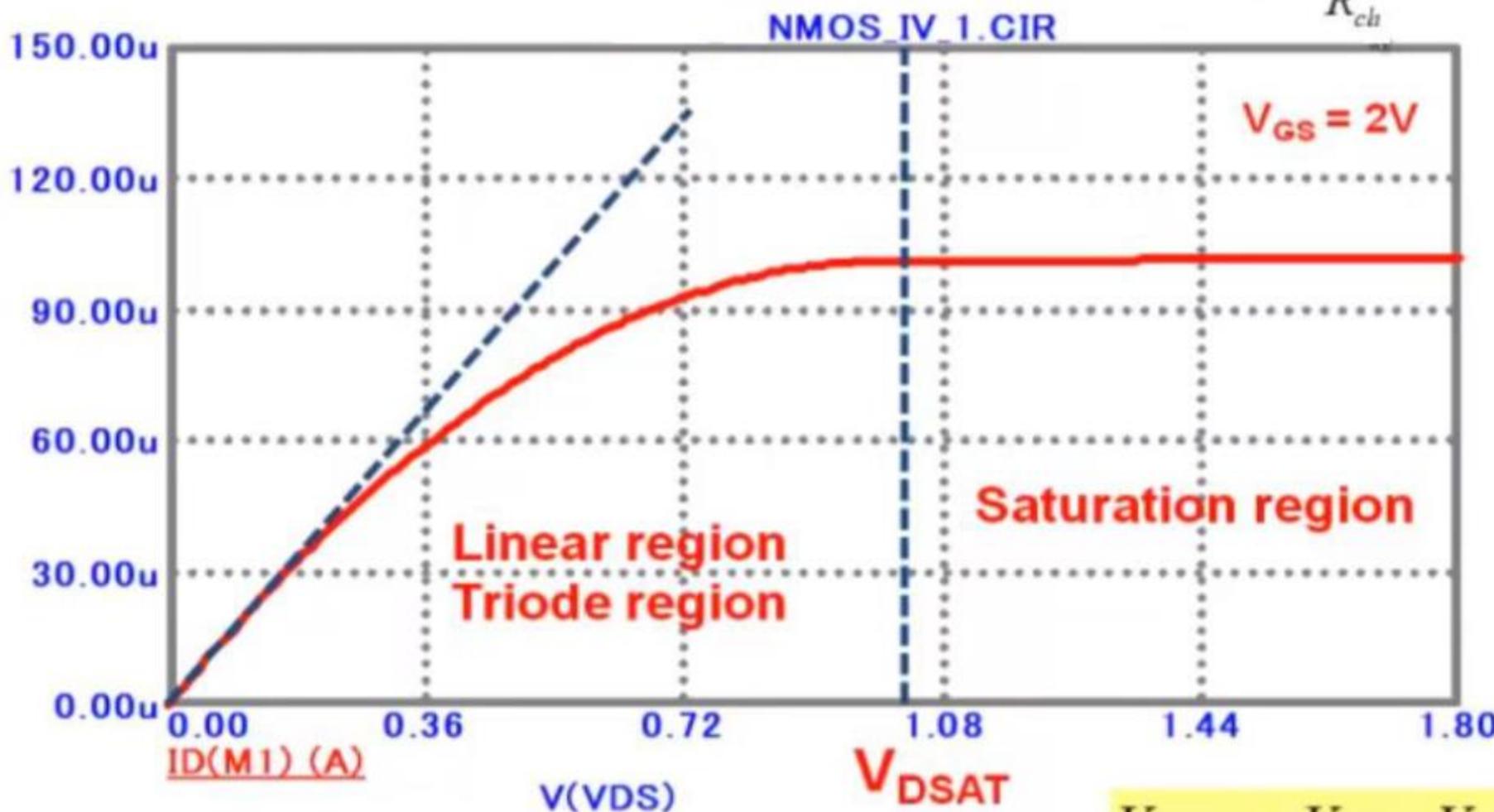
$$R_{ch} \propto \frac{1}{\int Q_{inv} dx}$$

$$I_{DS} = \frac{V_{DS}}{R_{ch}} > 0$$

$$I_{DS} = \frac{V_{DS}}{R_{cho}} = 0$$

As drain voltage increases, channel resistance also increases causing drain current to depart from linear behavior

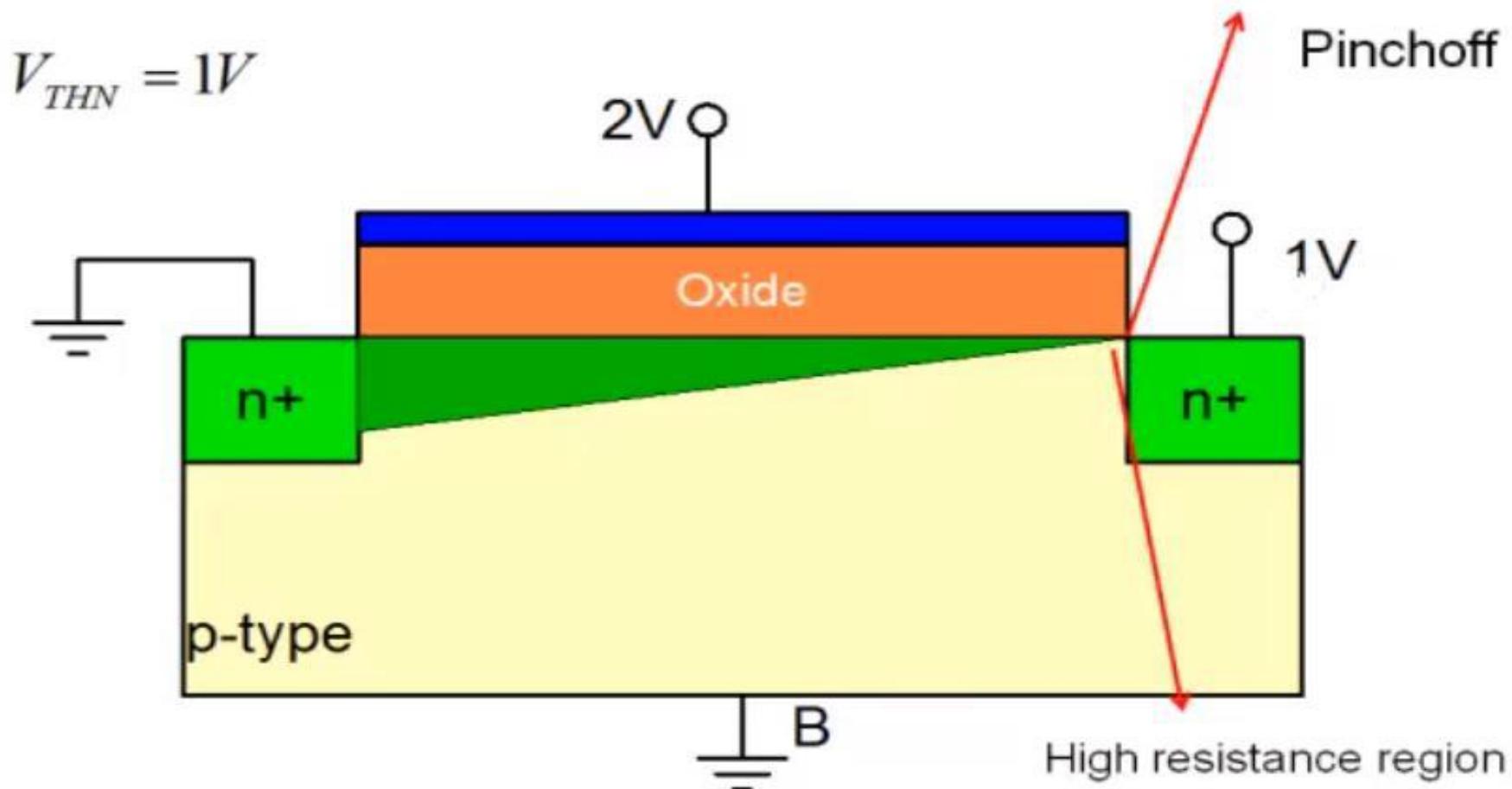
$$I_{DS} = \frac{V_{DS}}{R_{ch}} > 0$$



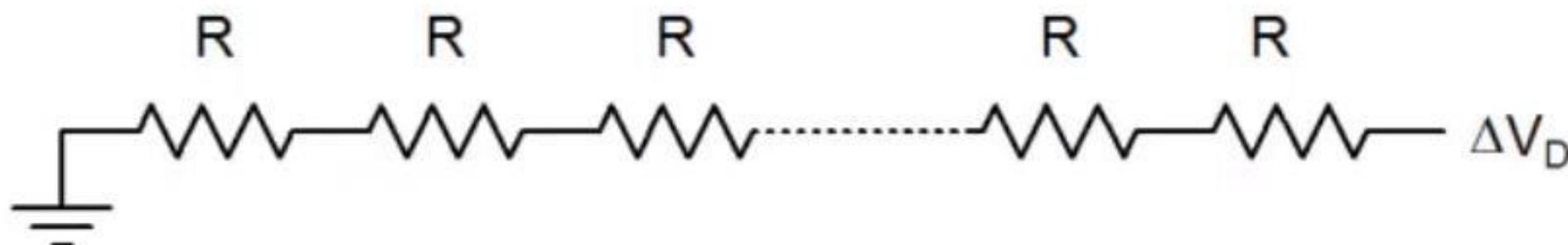
$$V_{DSAT} = V_{GS} - V_{THN}$$

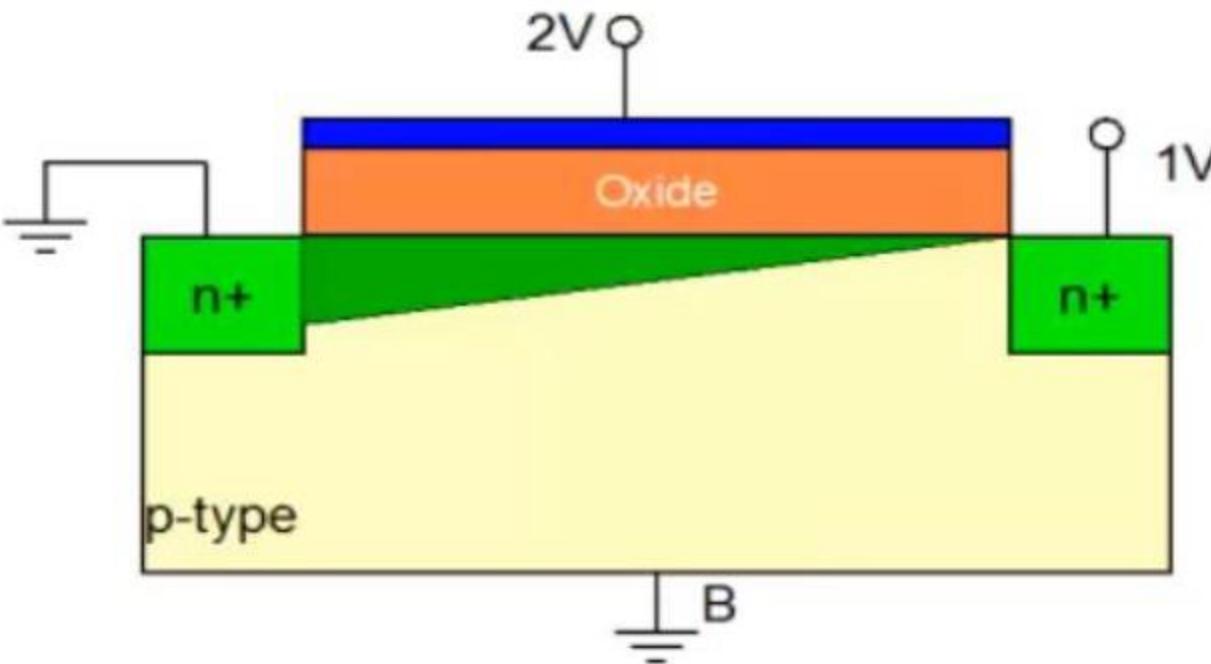
Note that **Saturation in MOSFET is analogous to forward active mode in BJT** and linear region is analogous to saturation in BJT.

$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V(x)) \cong -C_{ox}(2 - 1 - 1) = 0$$

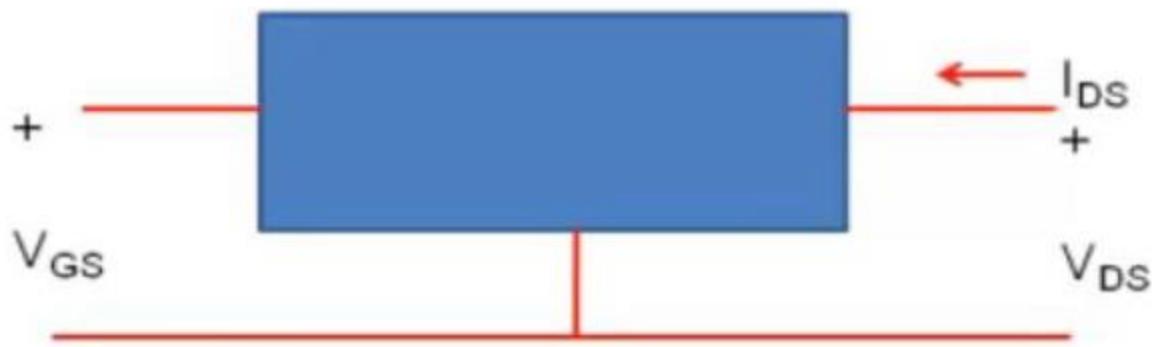


Any further increase in drain bias is absorbed in a small region next to the drain and rest of channel is not much affected and thus current becomes constant.



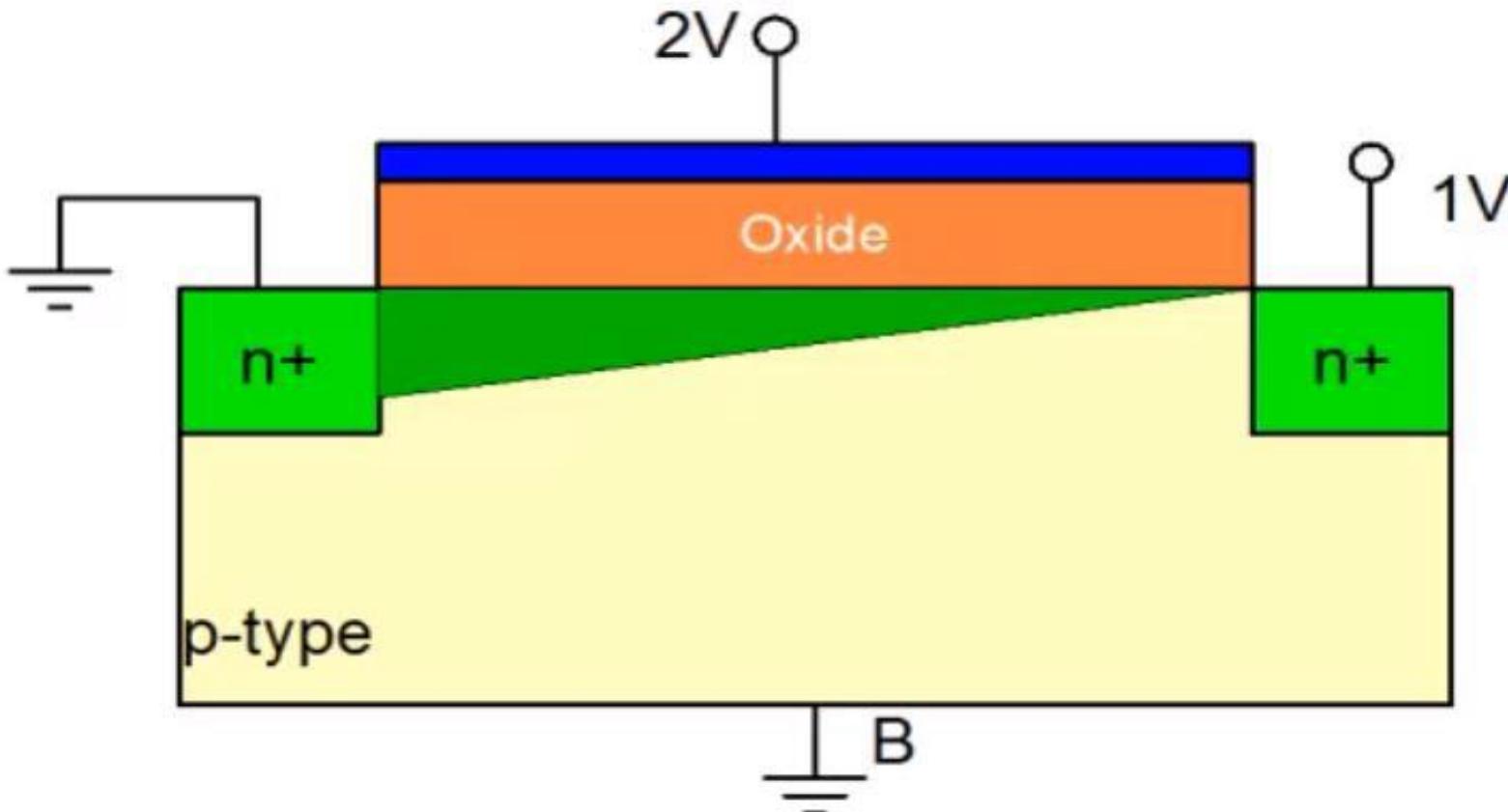


After pinchoff or saturation, drain current does not change much with drain voltage but is still very sensitive to gate voltage. MOSFET can now **AMPLIFY** signals



$$\frac{\partial I_{DS}}{\partial V_{GS}} \gg \frac{\partial I_{DS}}{\partial V_{DS}}$$

The voltage at which pinchoff occurs is the drain-saturation voltage V_{DSAT}

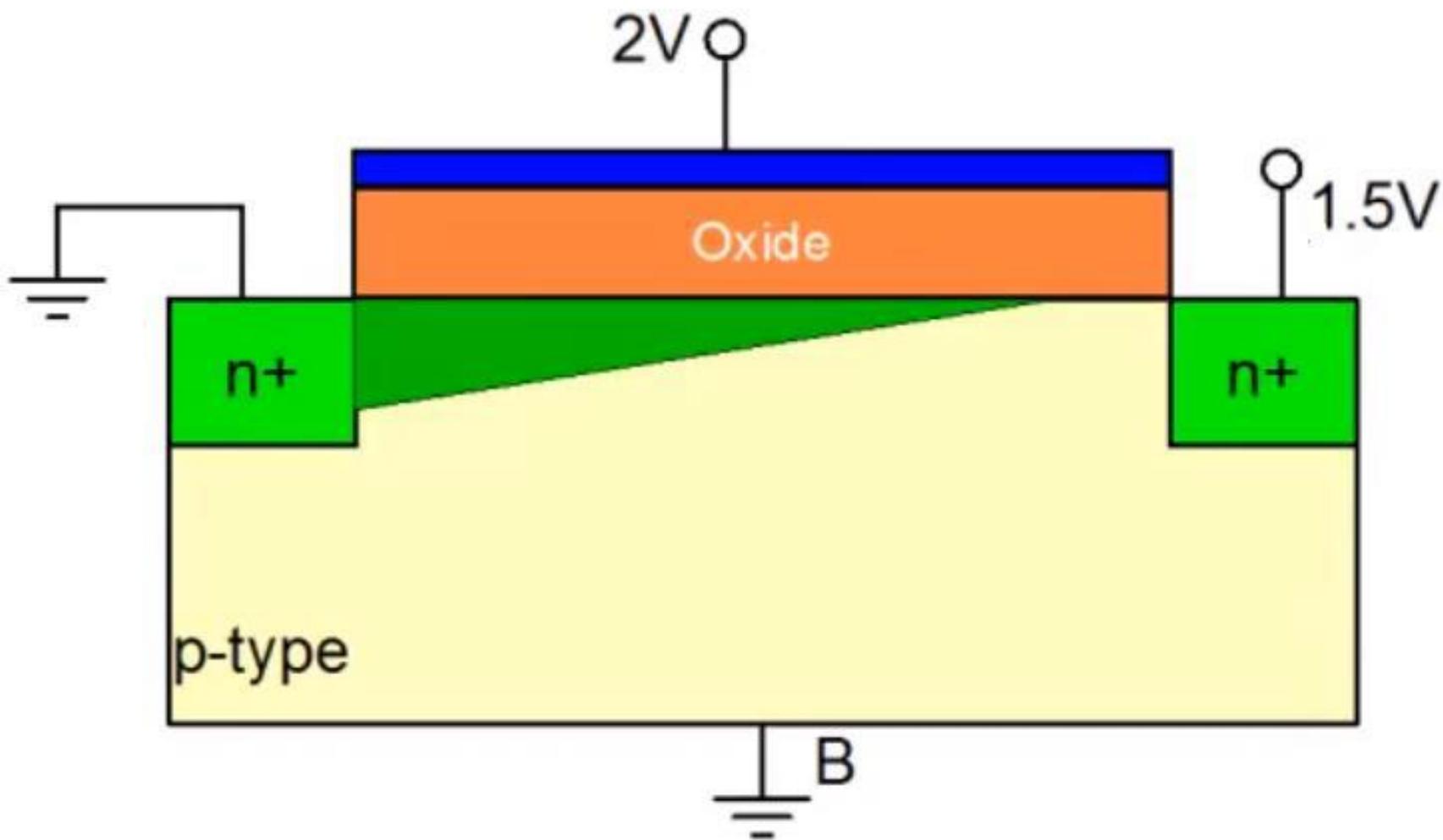


$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V_{DSAT}) \approx 0 \quad V_{DSAT} = V_{GS} - V_{THN}$$

This is a very simple picture. In short channel MOSFETs especially, saturation is a more complicated phenomenon.,

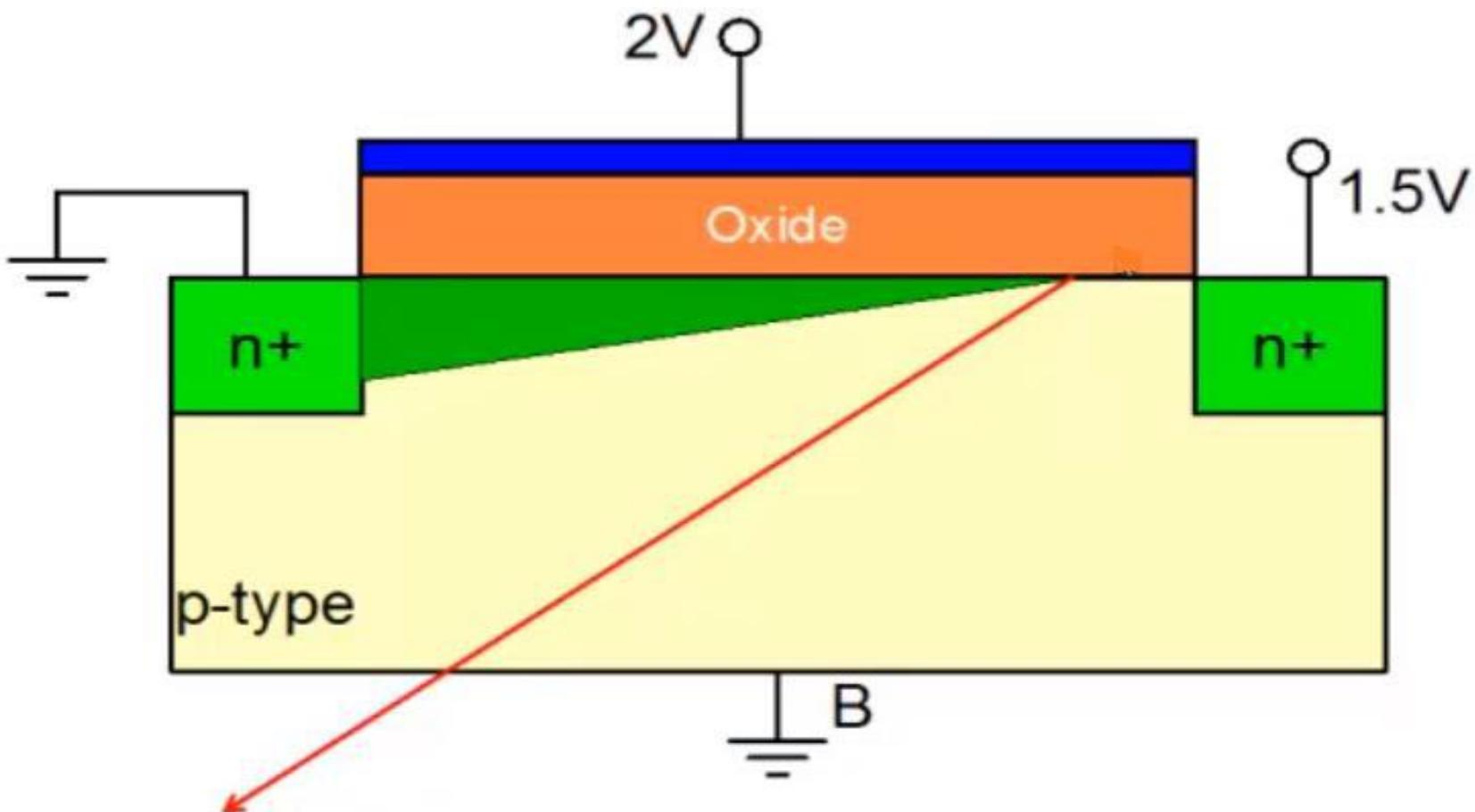
For voltages larger than saturation voltage

$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V(x)) \cong -C_{ox}(2 - 1 - 1) = 0$$



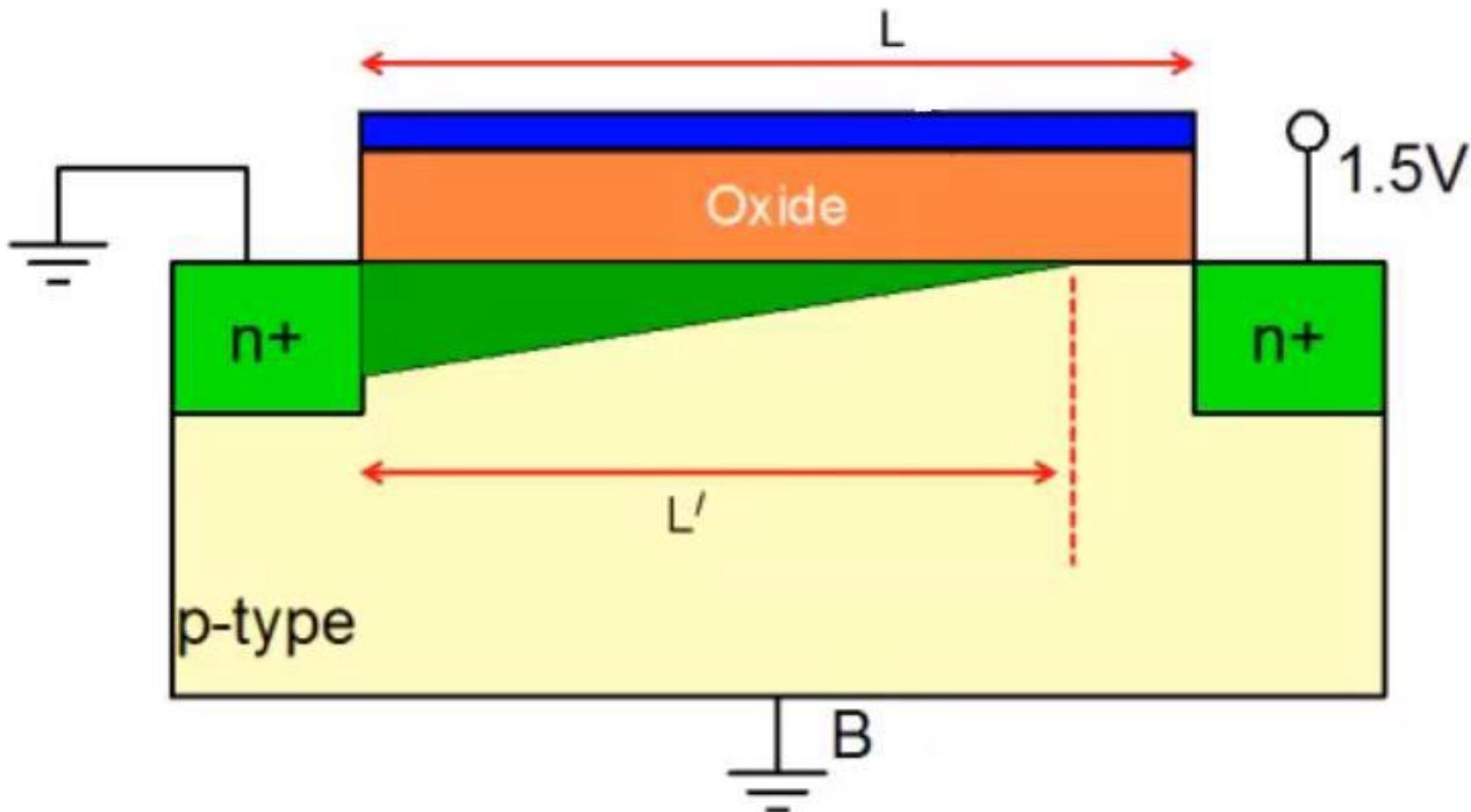
For voltages larger than saturation voltage

$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V(x)) \cong -C_{ox}(2 - 1 - 1) = 0$$

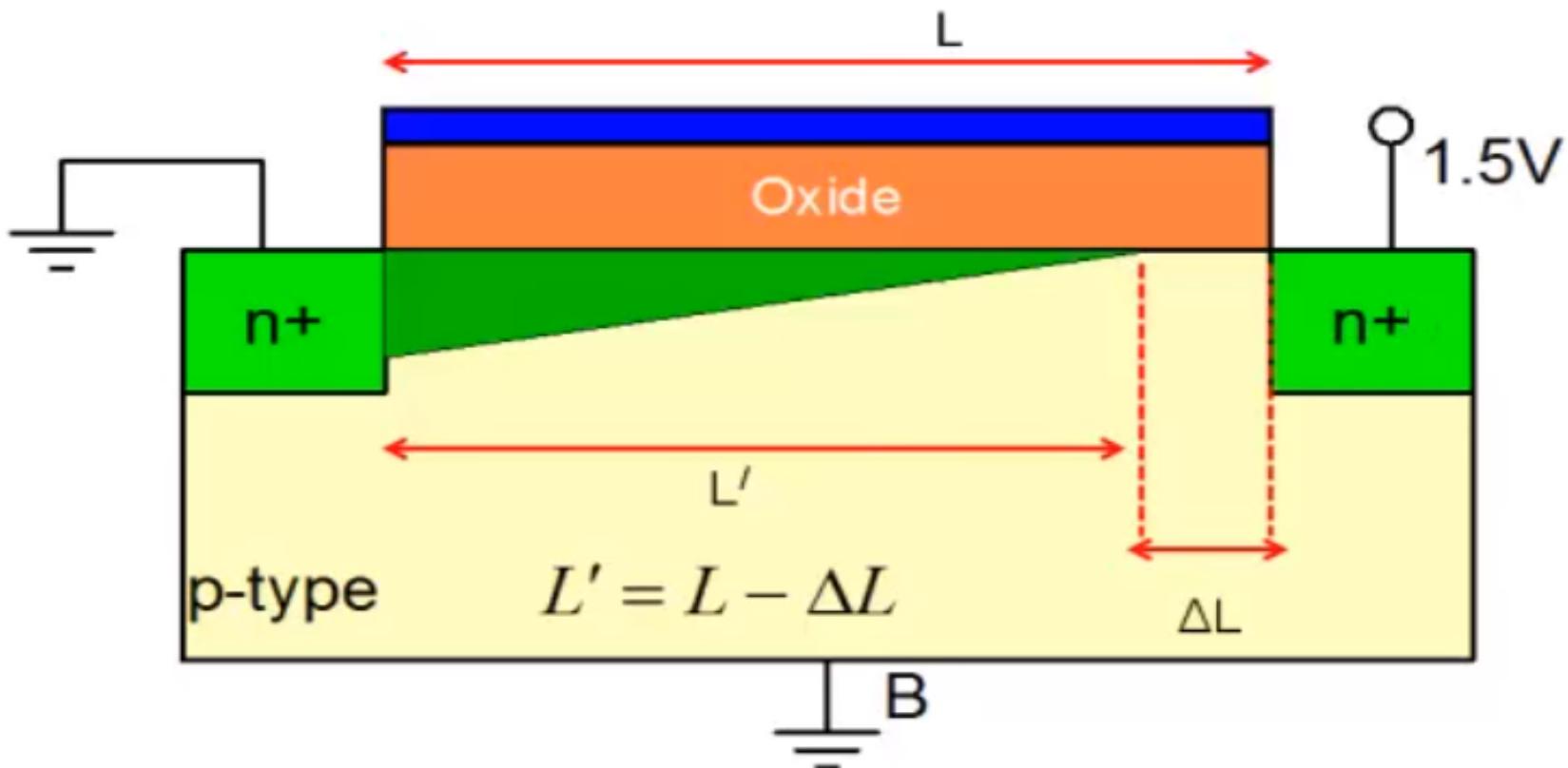


Pinchoff point moves left towards the source end. Voltage is $V_{DSAT} = 1V$

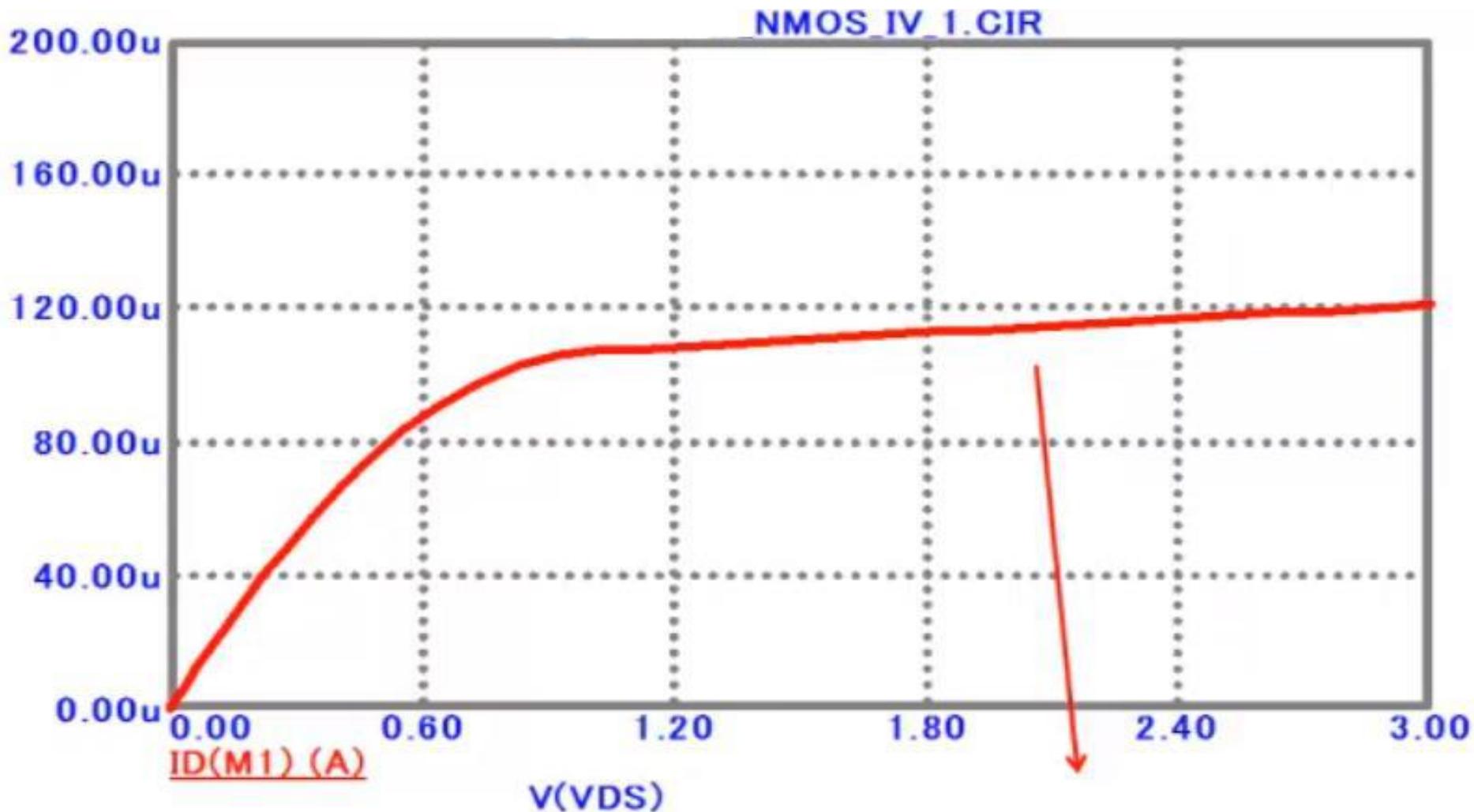
Channel Length Modulation



Channel Length Modulation

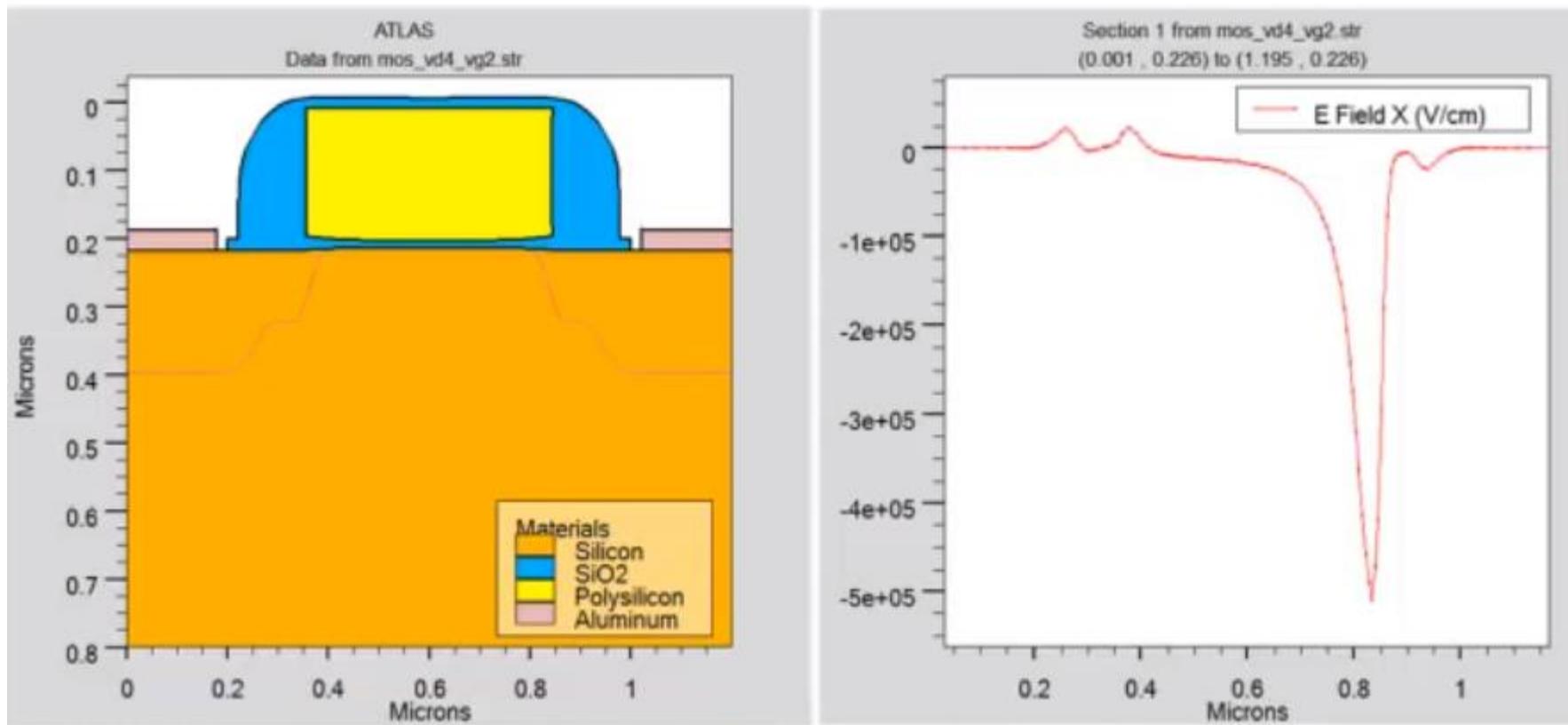


Effective channel length decreases as voltage increases beyond V_{DSAT} . As a result current increases a little with voltage

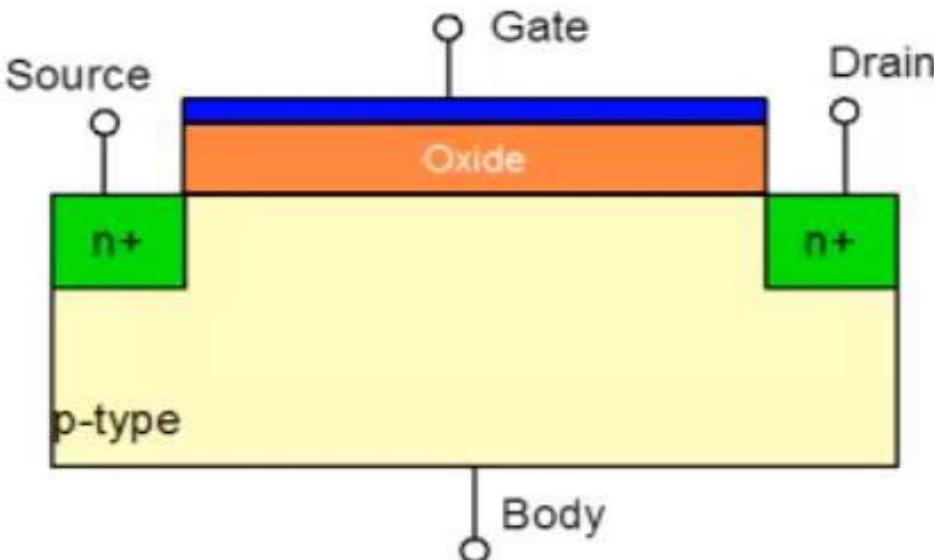


$$I_{DSAT} \times (1 + \lambda \times V_{DS})$$

λ : channel length modulation parameter



Threshold Voltage



$$V_{THN} = V_{THN0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}) \quad V_{THNO} = 1V$$

γ = body parameter Units : \sqrt{V}

$$\gamma = 0.7 V^{1/2}$$

Surface potential : $2\phi_F$

$$2\phi_F = 0.7V$$

$$V_{THNO} = 1V; \gamma = 0.7 V^{1/2}; 2\phi_F = 0.7V$$

$$V_{THN} = V_{THN0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$$

