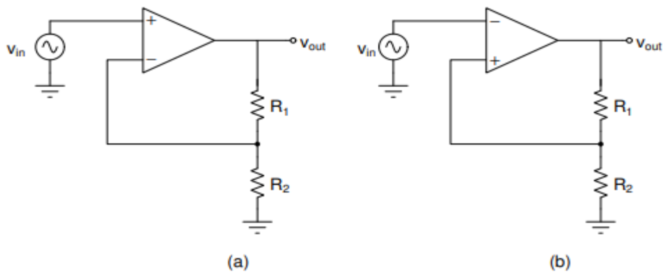
Analog Electronic Circuits Lab Report - Experiment 9

Name: [Chanda Akshay Kumar]
Roll No: [2024102014]
Teammate: [S V Santhosh Yadav]
Roll No: [2024102054]

Experiment 9: Op-Amp Circuits

1. **Voltage Transfer Characteristics (VTC) for Op-Amp in Negative and Positive Feedback Configurations**

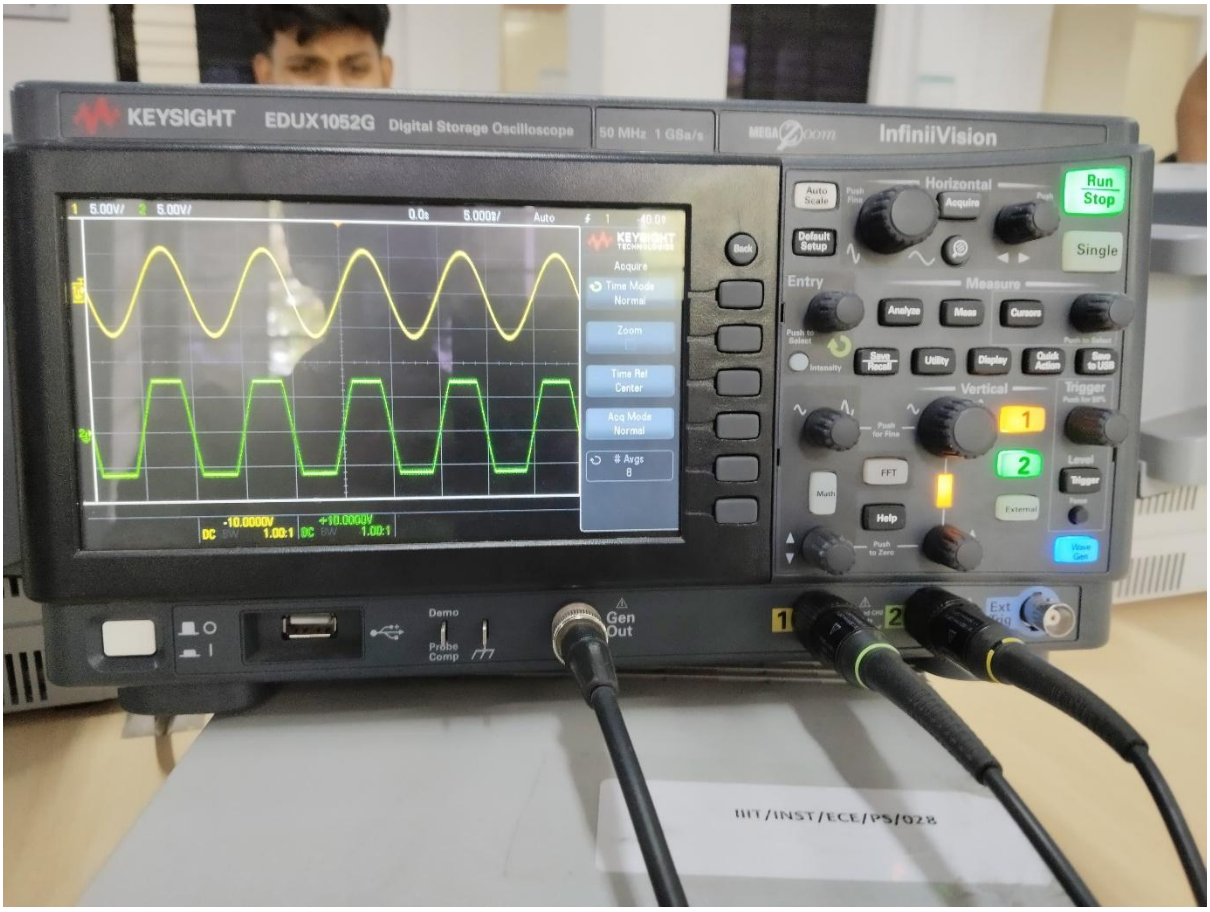


a) Identifying Feedback Type

- **Figure (a):** Negative feedback configuration because the output is connected to the inverting input, causing a fraction of the output to subtract from the input.
- **Figure (b):** Positive feedback configuration because the output is fed back to the non-inverting input, reinforcing the input signal by this output voltage is increased.

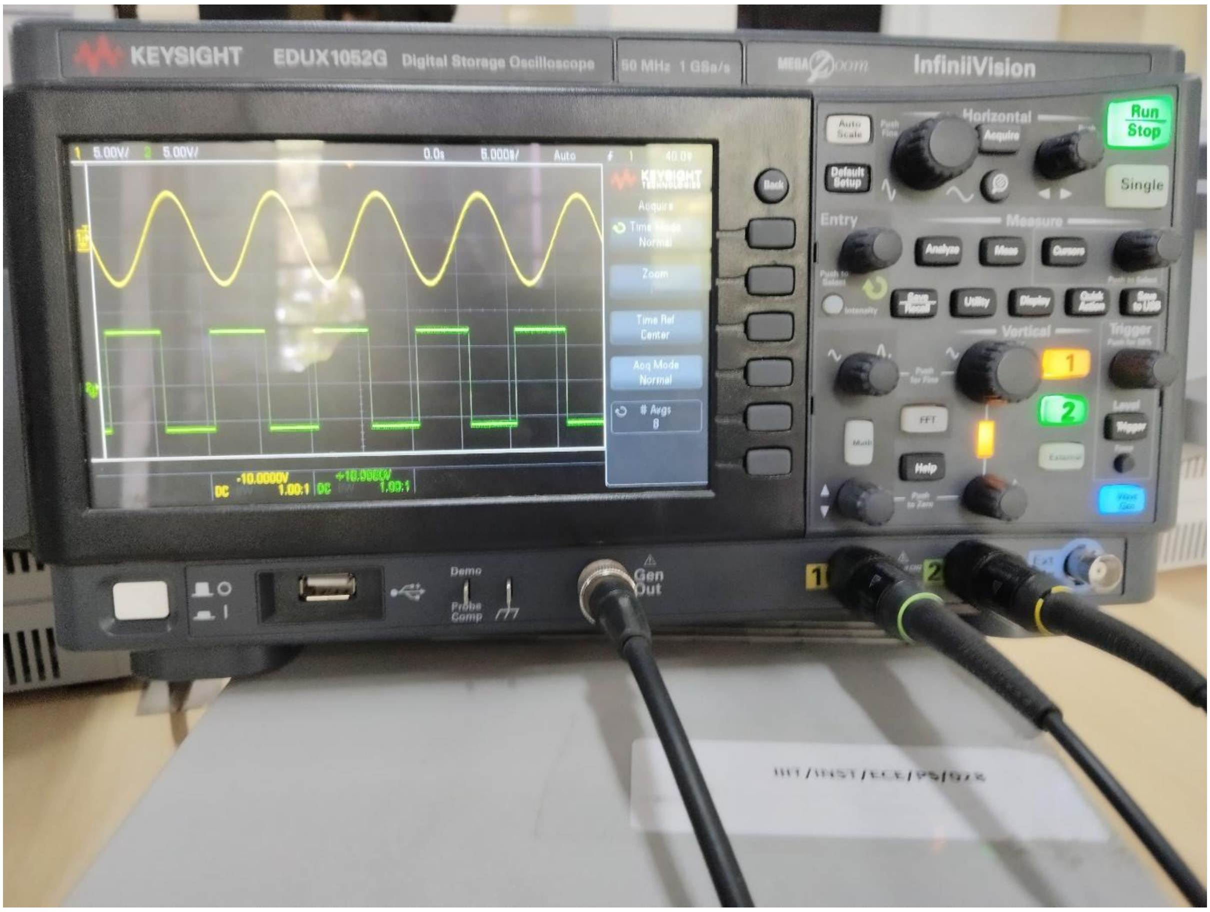
b) Plotting VTC (Vout vs Vin)

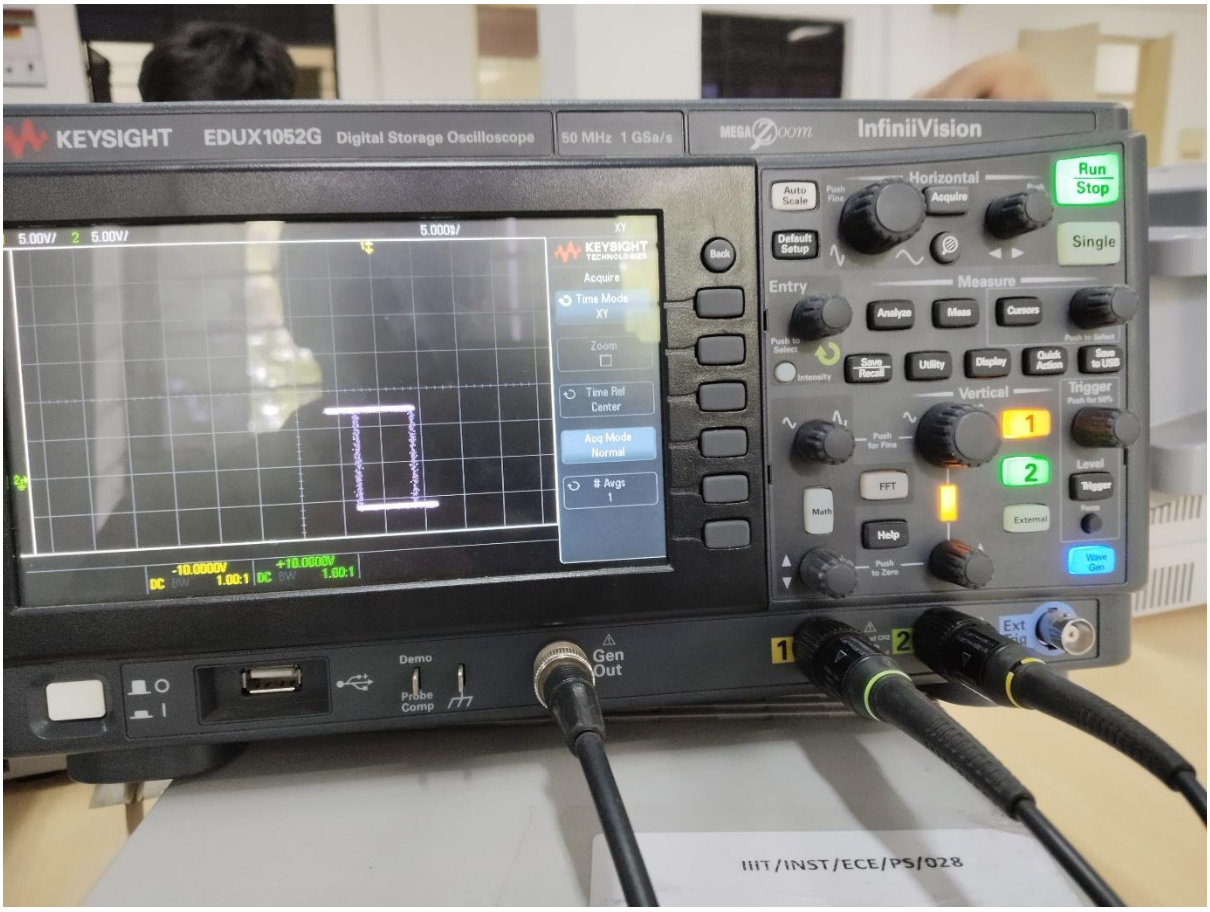
- **Circuit Setup:**
  - Resistors: R1=R2=10 kΩ
  - Supply Voltages: ±8 V
  - Input: Sine wave, Vin=±12 Vpp ,100 Hz
- **Observations:**
  - **Negative Feedback:**
    - Output follows input linearly until saturation.
    - Smooth transition between positive and negative saturation.


KEYSIGHT
EDUX1052G Digital Storage Oscilloscope
50 MHz 1 GSa/s
InfiniiVision
Run Stop
Single
IIIT/INST/ECE/PS/028


KEYSIGHT
EDUX1052G Digital Storage Oscilloscope
50 MHz 1 GSa/s
InfiniiVision
Run Stop
Single
IIIT/INST/ECE/PS/028

- **Positive Feedback:**
  - Output exhibits hysteresis (sudden jumps between +VDD and −VDD).
  - Output remains latched at one extreme until input crosses a threshold.

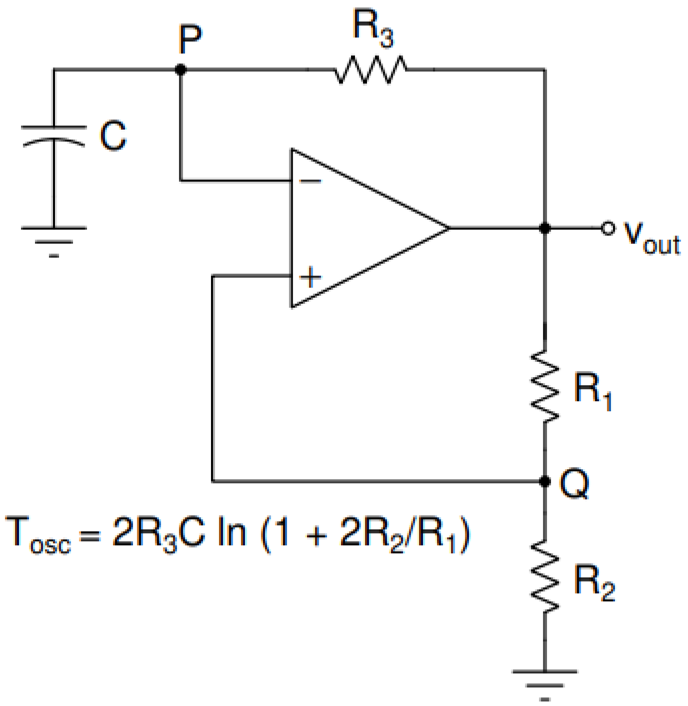




c) Regeneration/Hysteresis

- **Positive Feedback:** Shows hysteresis because the output reinforces input changes, causing rapid switching between saturation levels. Useful in oscillators and Schmitt triggers.
- the op-amp output is at one extreme, such as the positive supply voltage VDD. As the input voltage crosses the upper threshold, the positive feedback causes a rapid switch in the output to the opposite extreme, such as the negative supply voltage -VDD. With the output now at the opposite extreme, the input voltage must drop below the lower threshold for the output to switch back to the original extreme. This hysteresis characteristic enables the Op-amp positive feedback circuit to provide stable and noise‑tolerant switching behaviour.
- The positive feedback reinforces the input signal, resulting in the output regenerating and transitioning to a new state once the input voltage crosses the thresholds.
- **Negative Feedback:** No hysteresis; stabilizes output by counteracting input variations. Used in amplifiers for linear operation.

2. **RC Oscillator (Positive Feedback Example)**

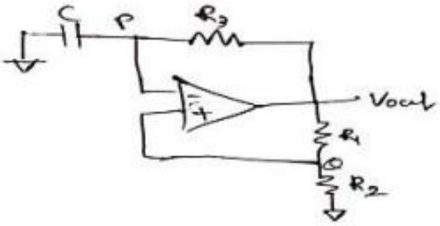


a) Theoretical Frequency Calculation

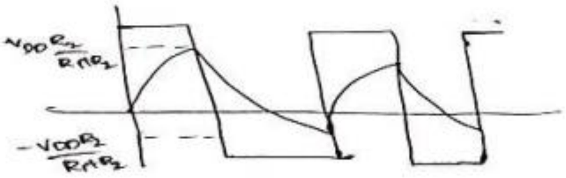
Given:

- R1=R2=10 kΩ
- R3=1 kΩ
- C=1 μF

Formula:



$$T_{osc} = 2R_3C \ln(1 + 2R_2/R_1)$$



$$i_c = i_{R_3}$$

$$C\frac{dv_P}{dt} = \frac{V_{out} - V_P}{R_3}$$

→ for +ve cycle,

$$\int \frac{dt}{R_3C} = \int \frac{dv_P}{V_{out} - V_P} \qquad V_{out} = V_{DD}$$

$$\frac{t}{R_3C} = \int_{-\frac{V_{DD}R_2}{R_1+R_2}}^{\frac{V_{DD}R_2}{R_1+R_2}} \frac{dv_P}{V_{out} - V_P}$$

$$= \ln(V_{out} - V_P)\Big|_{-\frac{V_{DD}R_2}{R_1+R_2}}^{\frac{V_{DD}R_2}{R_1+R_2}}$$

$$= \ln\left(\frac{R_1}{R_1+2R_2}\right)$$

$$T = R_3C\ln\left(1 + \frac{2R_2}{R_1}\right)$$

→ for +ve & -ve cycle (one period)

$$T = 2R_3C\ln\left(1 + \frac{2R_2}{R_1}\right.$$

$T_{osc}=2R_3C\ln(1+2R_2R_1)$

→ $T_{osc}=2\times1k\times1\mu\ln(1+2)=2.197$ ms → $f_{osc}=1T_{osc}=455.12$ Hz

(a) $T = 2R_3 C . \ln\left(1 + \frac{2R_2}{R_1}\right)$

$$= 2 \cdot (1K)(10^{-6}) . \ln\left(1 + \frac{2(10K)}{(10K)}\right)$$

$$= 2(1K)(10^{-6}) . \ln(3)$$

$T = 0.002197224$ sec

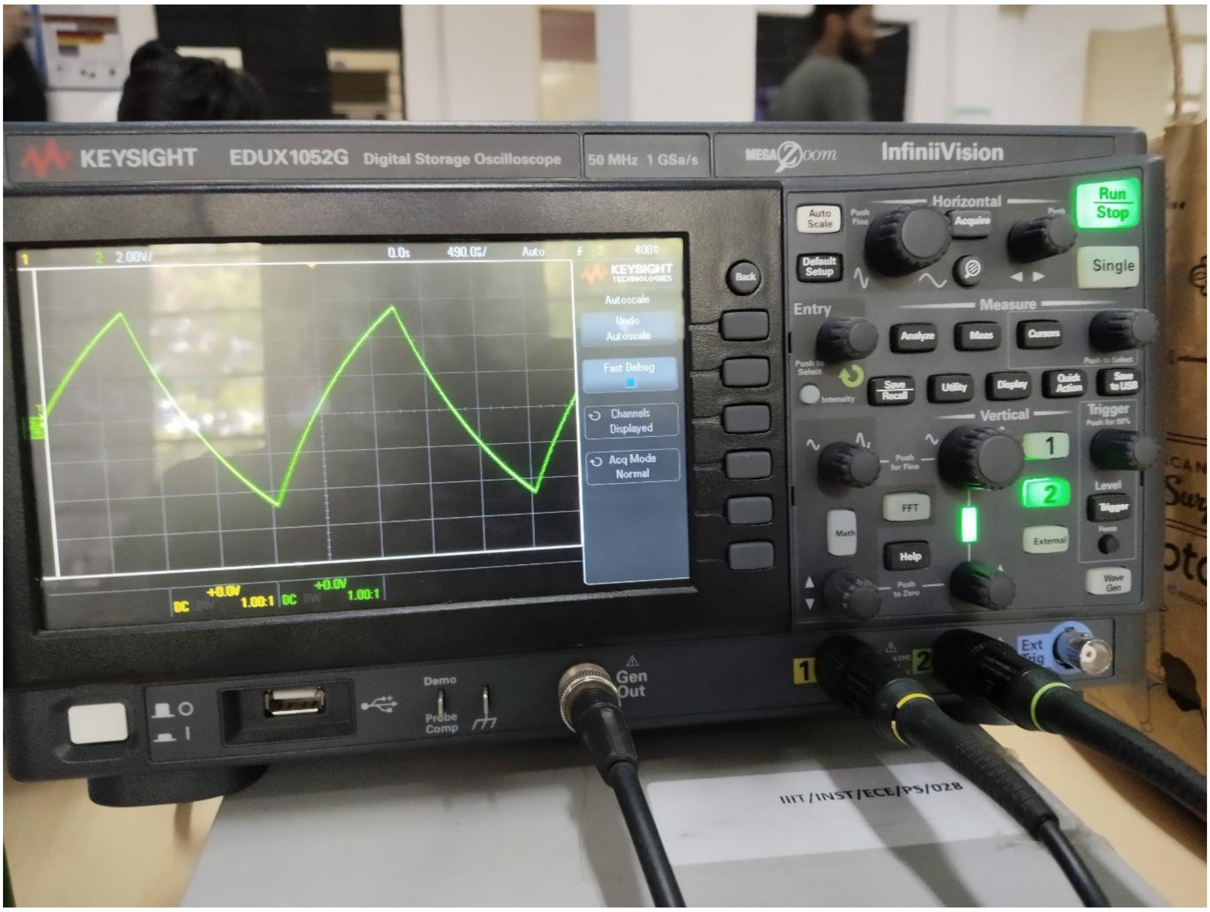
$$f = \frac{1}{T} = \frac{1}{0.002197224}.$$

$f = 455.1199$

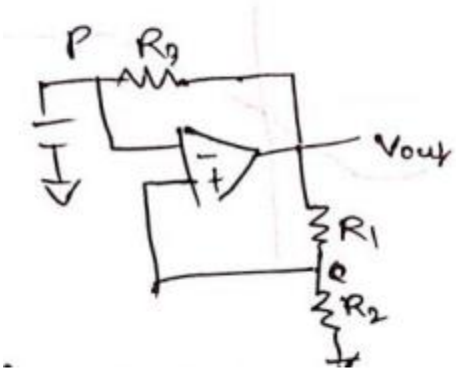
b) Measured Results

- **Observed Frequency:** 441.03 Hz
- **Comparison:** Close to theoretical value (455.12 Hz). Minor deviation due to component tolerances and other non-ideal reasons.

Plot of VP:

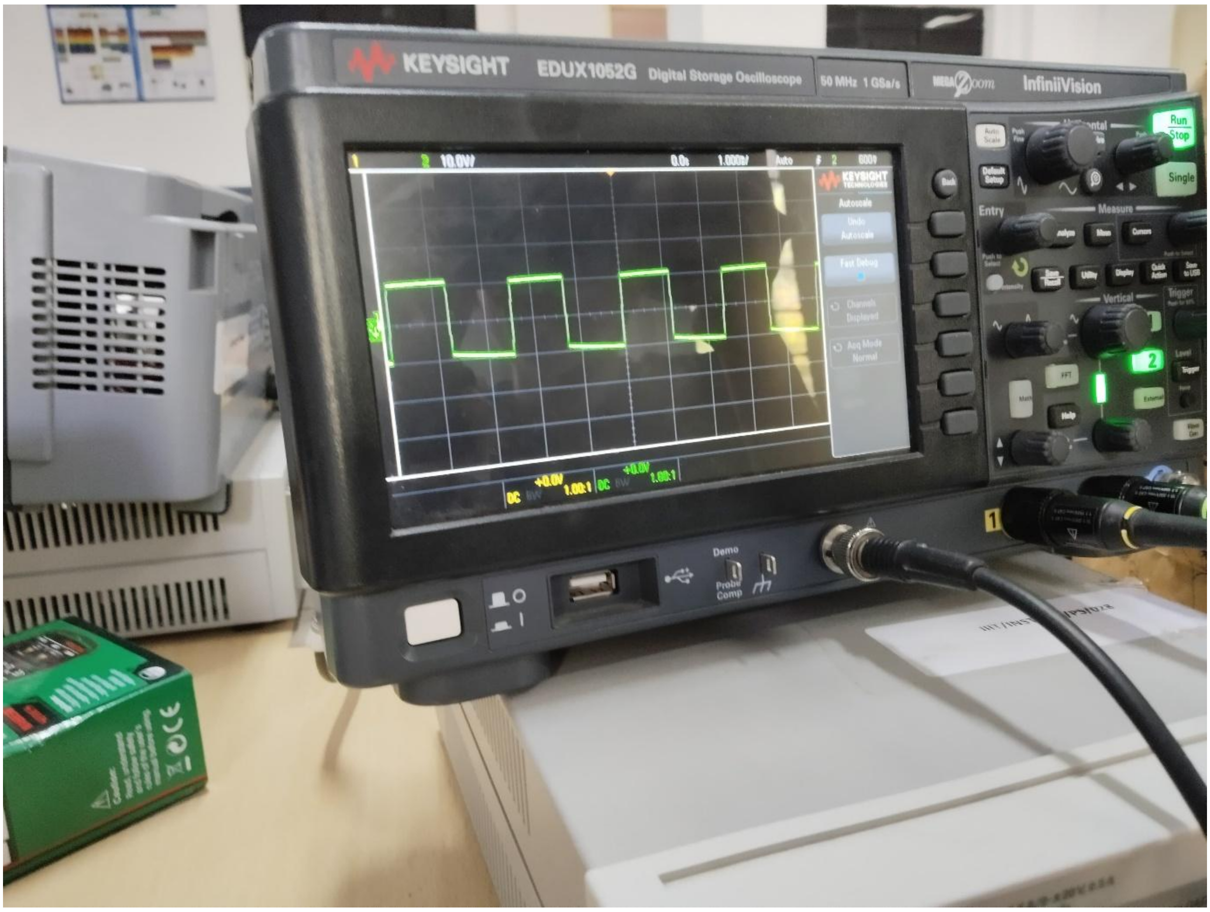


Why Positive Feedback?

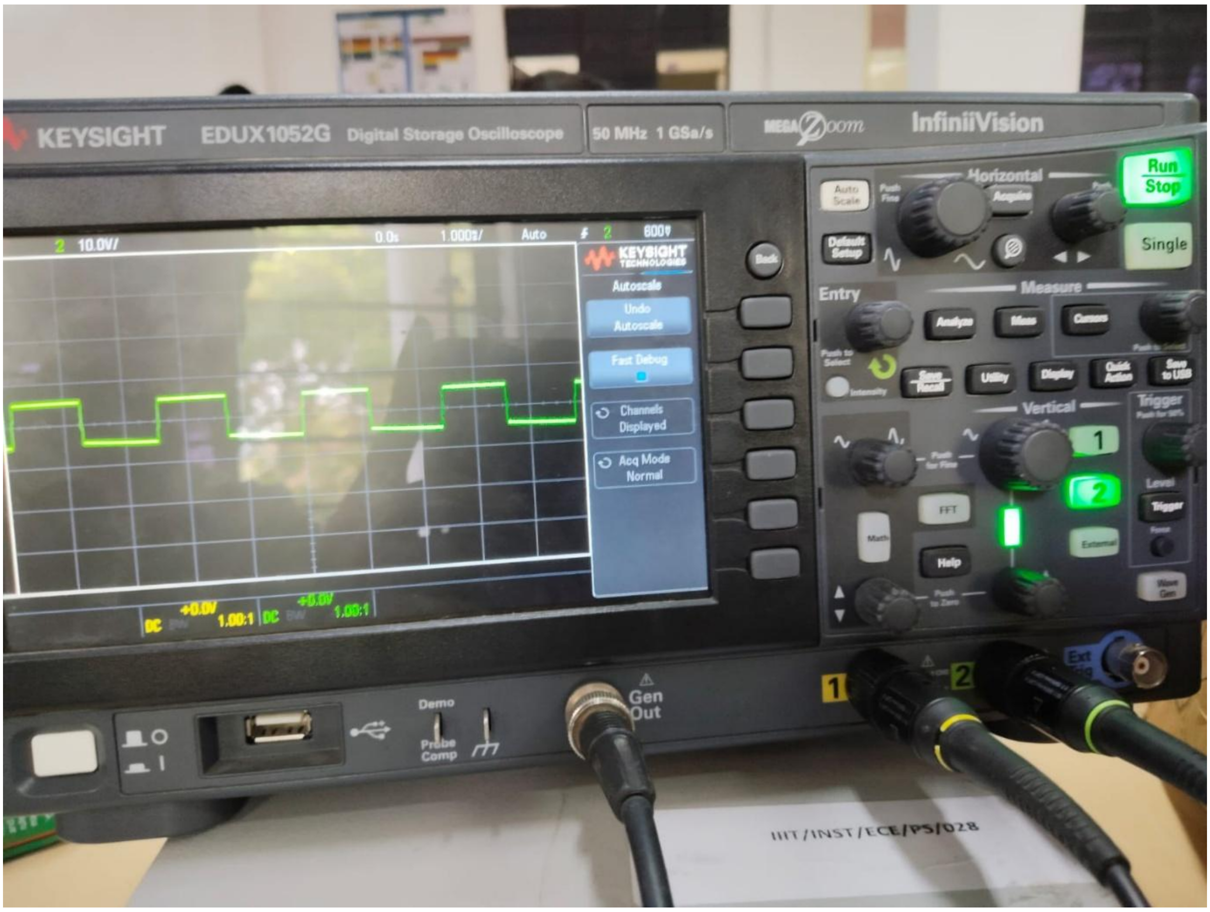
- The RC network introduces phase shift, and positive feedback ensures sustained oscillations by reinforcing the signal.
- 

- Here if vout changes suddenly Vp also changes and which is connected to Non ineverting terminal
- But Vp is changing as capacitor is charging and discharging
- By this some fraction is adding to differerntial input of op-Amp when the input is +ve feedback

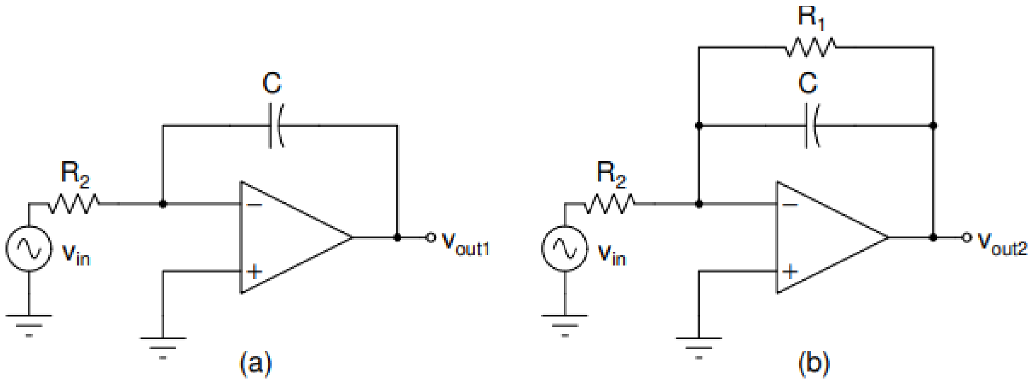
Plot of Vout:



Plot of VQ:



3. **Integrator (Negative Feedback Example)**

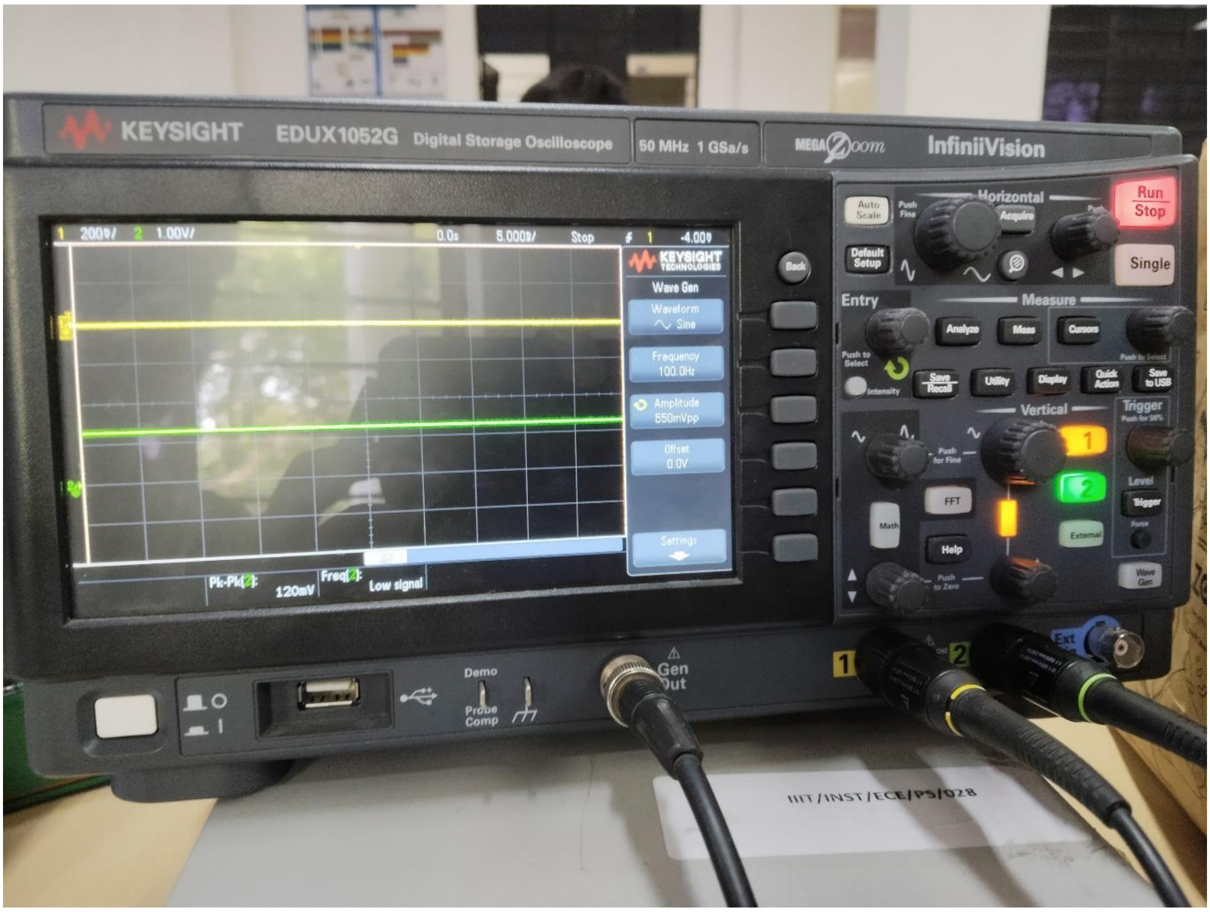


Connecting the circuit above shown and C = 10nF

And R1=10Kohm and R2 = 1kohm

a) Output Saturation with DC Input (Vin = 0V)

- **Observation:** Output saturates to +VDD or −VDD due to op-amp DC offset.



- Integrator continuously accumulates input offset, driving output to saturation.
- In this part of the experiment, the input voltage vin is kept at a constant 0V. However, due to the inherent DC offset of the Op Amp, the output voltage will continuously increase until the Op Amp reaches saturation

b) Preventing Saturation with Parallel Resistor (R1)

- **Observation:** Output does not saturate.
- **Reason:** Resistor R1 limits gain at DC, turning the circuit into an inverting amplifier after capacitor charges fully.
- At steady state (t = ∞), gain for DC-offset is 1+R1/R2
- capacitor gets fully charged, resistor makes the circuit to act as an Inverting amplifier in closed loop configuration

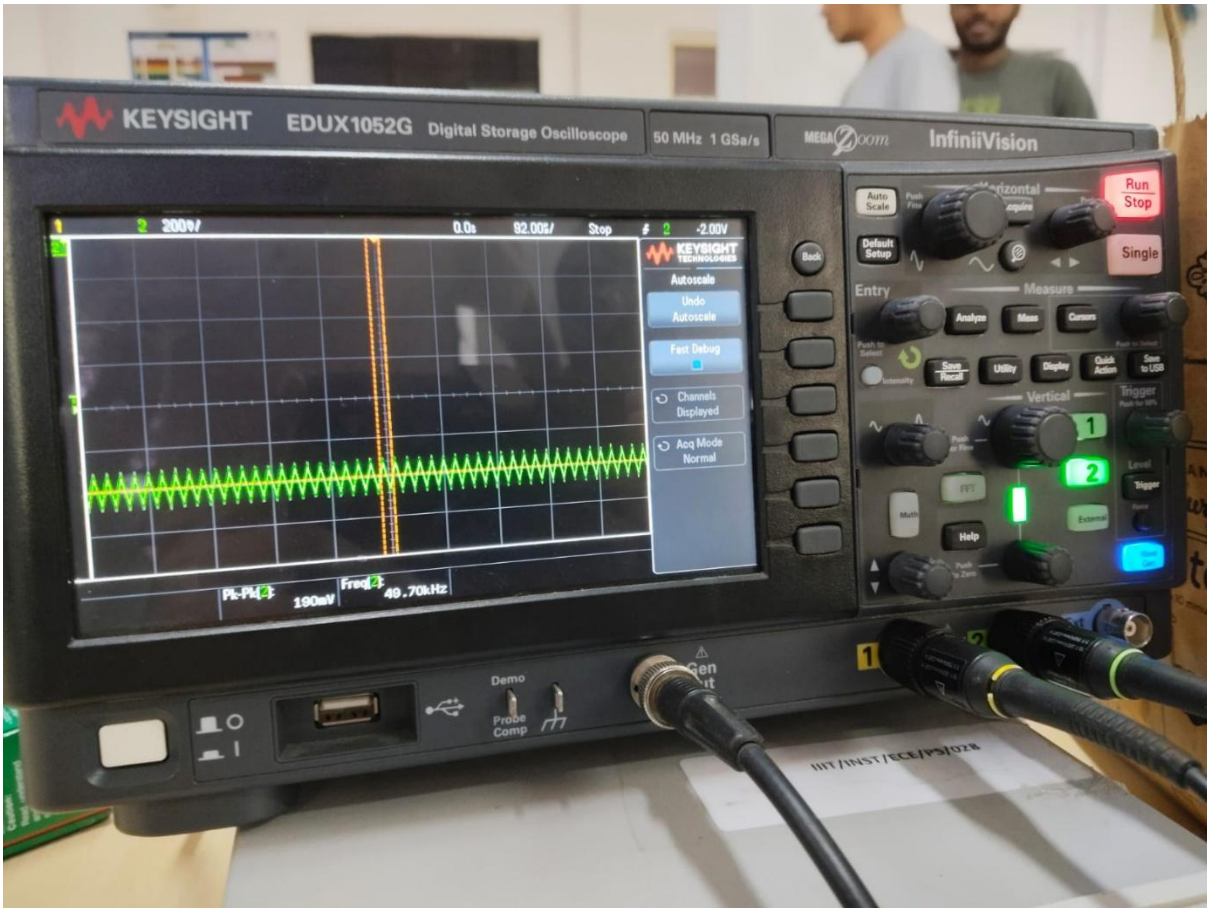
To prevent the op-amp from saturating, a resistor R_1 (with 10 kΩ) is connected across the capacitor in circuit.

- The resistor avoids excessive voltage build-up & ensures the op-amp operates within its *linear range*.

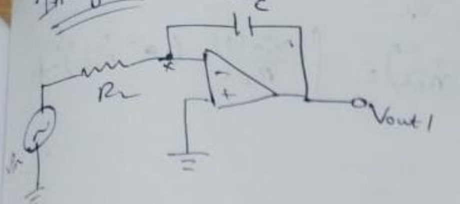
From the above plot, it is evident that op-amp has not reached saturation.
This is due to presence of resistor R_1, which maintains the negative feedback loop even after capacitor is fully charged.

c) Integrator Action with Square Wave Input

- **Input:** 0 (low) and 500 mV (high) , 50 kHz square wave.
- **Output:** Triangular wave (integrated signal).
- **Verification:**
  - Rising input → Negative ramp output.
  - Falling input → Positive ramp output.



Integrator Circuits



$V_+ = 0 \Rightarrow V_- = 0$ (Approximated because Vout is very higher than Vin)

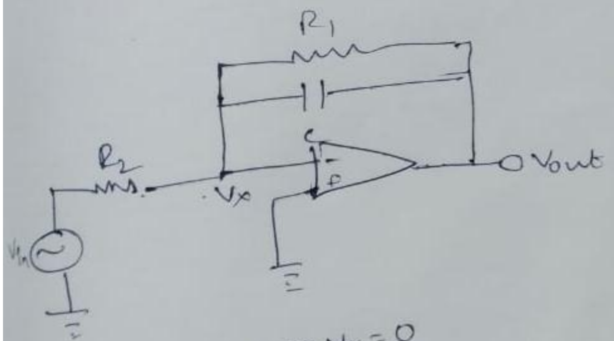
Let us apply KCL at node x

$$\Rightarrow \frac{V_{in}}{R_2} = -C\left(\frac{d}{dt}(V_{out})\right)$$

$$\Rightarrow \frac{dV_{out}}{dt} = -\frac{1}{R_2 C} V_{in}$$

$$\Rightarrow V_{out} = -\frac{1}{R_2 C}\int V_{in}$$

$\Rightarrow$ The above circuit acts as an integrator circuit



$V_+ = 0 \Rightarrow V_x = 0$

$$\Rightarrow C\frac{dV_{out}}{dt} + \frac{V_{out}}{R_1} = \frac{V_{in}}{R_2}$$

$$\frac{dV_{out}}{dt} + \frac{V_{out}}{R_1 C} = \frac{V_{in}}{R_2 C}$$

$$I.F = e^{\int -\frac{1}{R_1 C} dt}$$

$$= e^{-\frac{t}{R_1 C}}$$

$$\left(V_{out}(t)\right)\left(e^{-\frac{t}{R_1 C}}\right) = \int \frac{V_{in}(t)}{R_2 C}\left(e^{-\frac{t}{R_1 C}}\right) dt$$

for square wave

$$V_{out} = \frac{-1}{R_2 C}\int \frac{A}{2} dt \quad \text{+ve cycle}$$

$$= \left(\frac{-A}{2R_2 C}\right) t$$

$$V_{out} = \frac{-1}{R_2 C}\int \frac{-A}{2} dt \quad \text{-ve cycle}$$

$$V_{out} = \frac{A}{2R_2 C} t \qquad = 500m(T/2) + 0$$

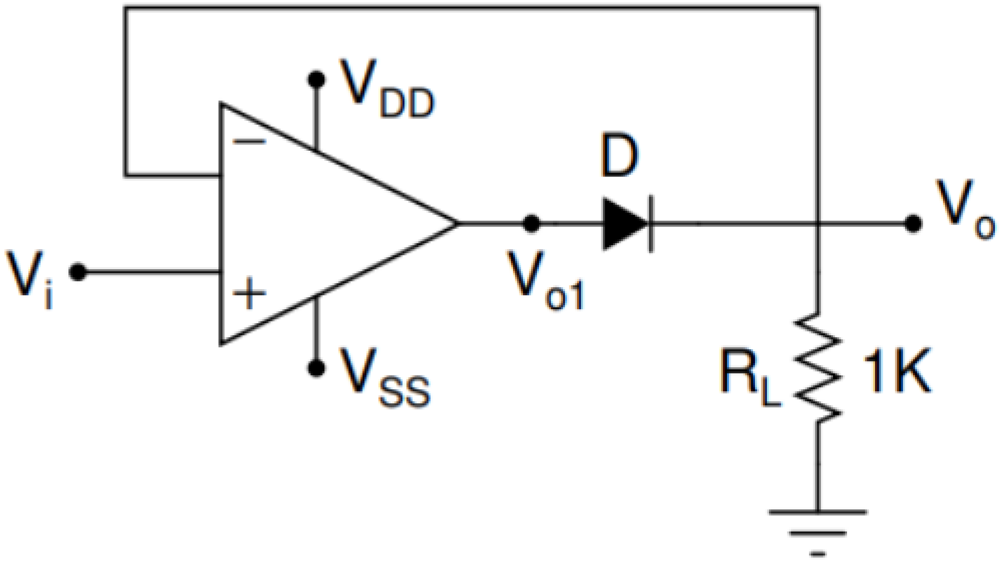
DC offset

↳ Triangular curve

→ we got Integrator.

4. Precision Half-Wave Rectifier (Negative Feedback Example)

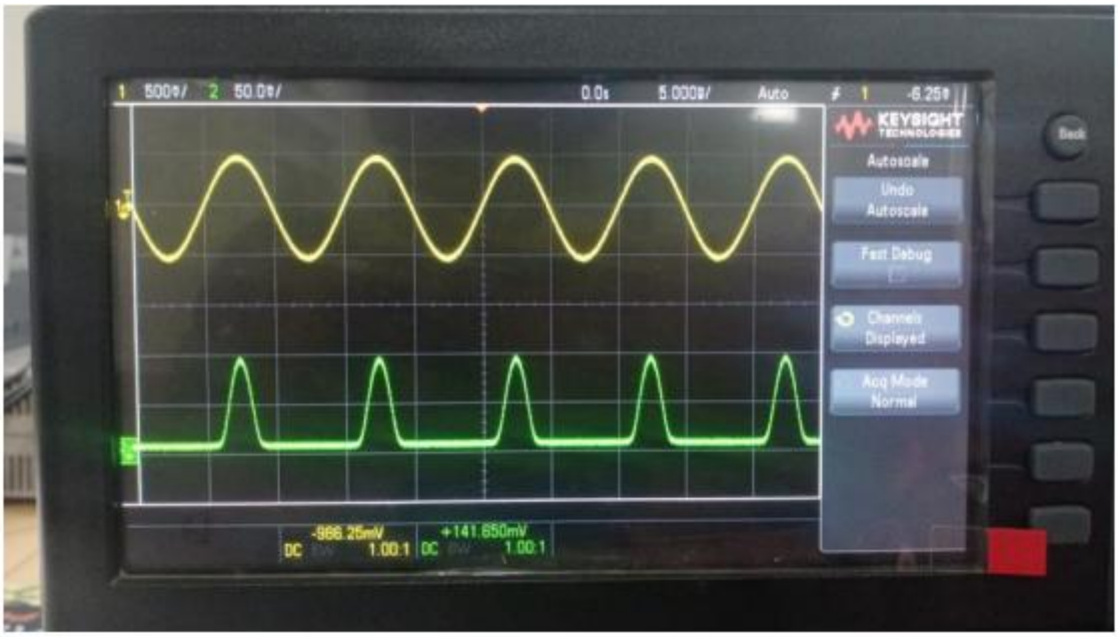
a) Circuit Verification



- **Input:** 1 V peak, 100 Hz sine wave.
- **Output:** Half-wave rectified signal.
- **Observation:** No voltage drop (unlike diode rectifiers).

b) Comparison with Diode Rectifier

- **Diode Rectifier:**
    - 0.7 V drop, distorted output. Because of cutin voltages the voltage is reduced and also no output till the certain voltage

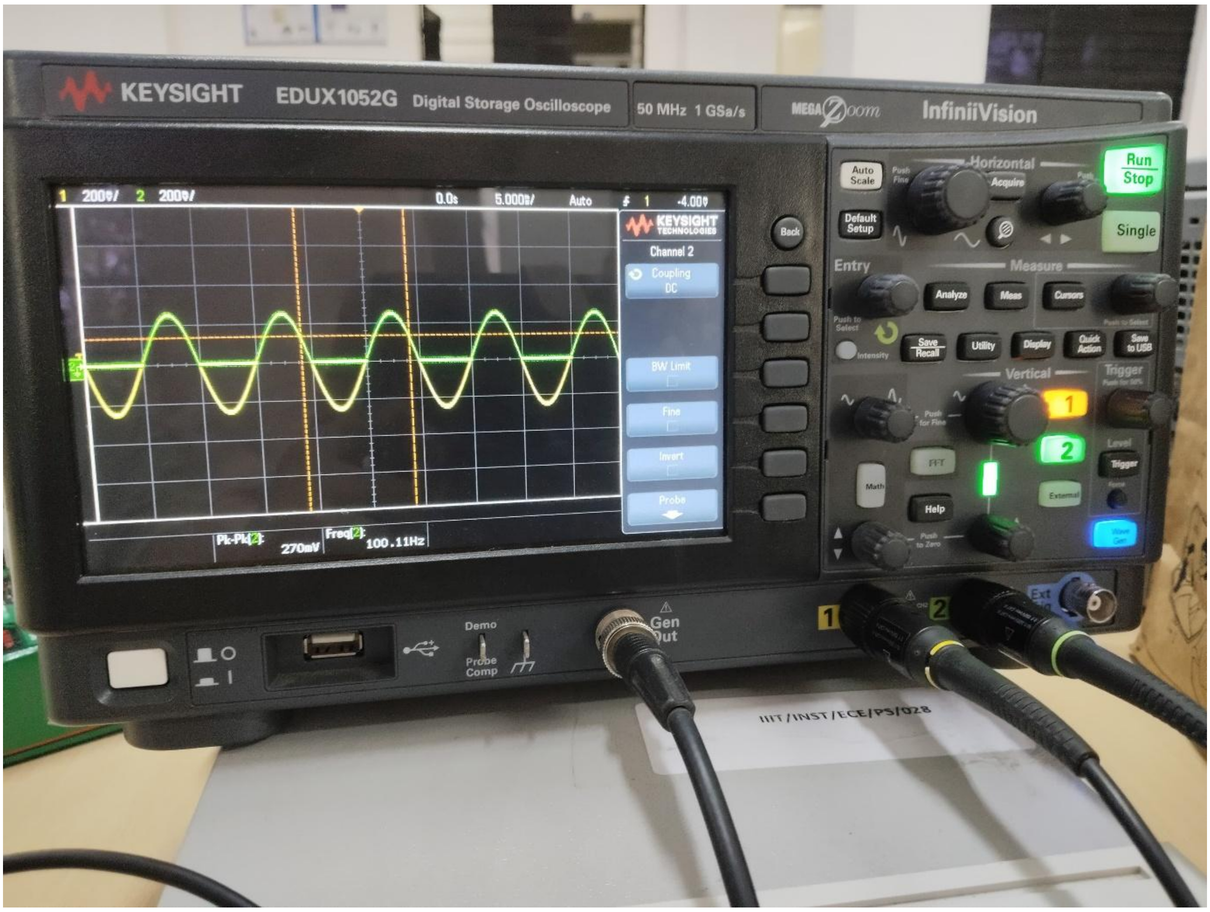


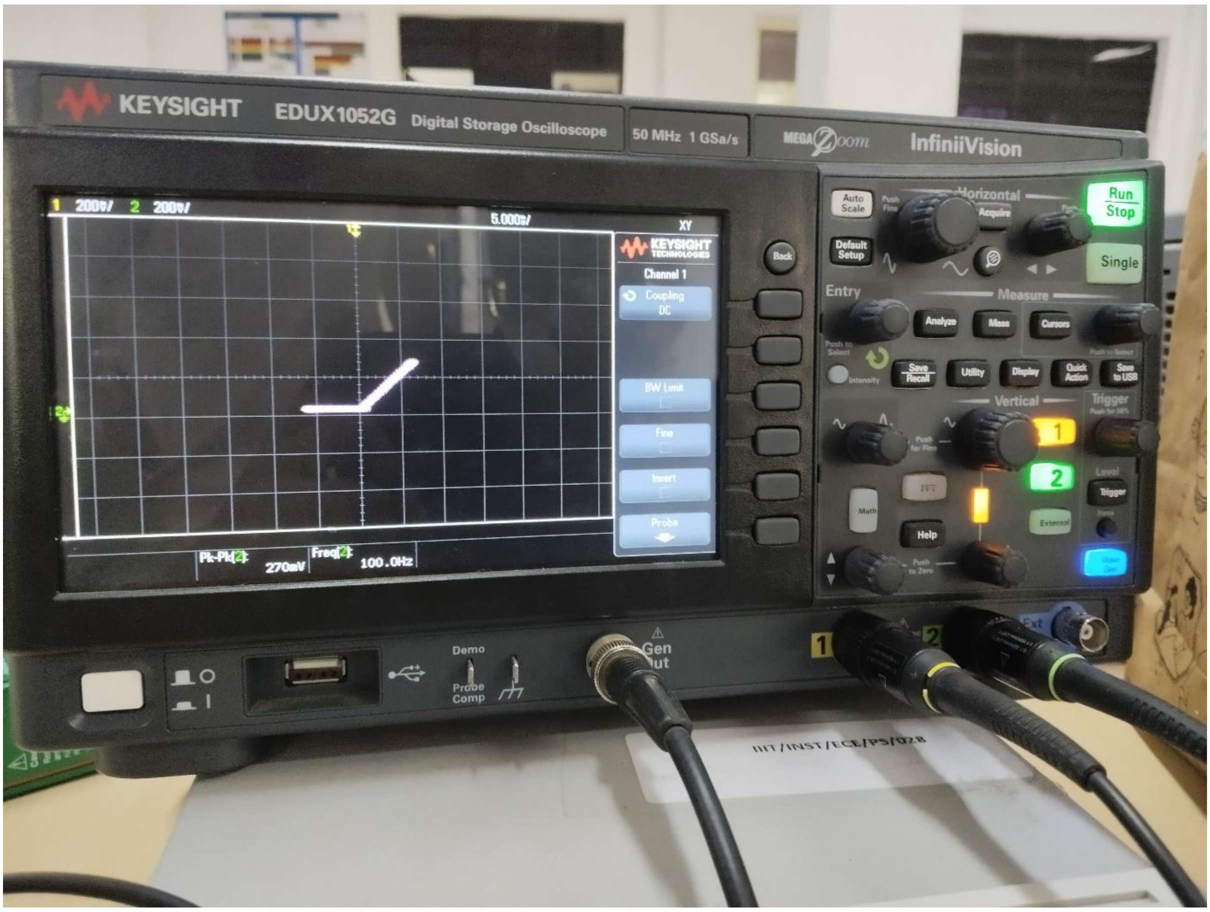
- **Op-Amp Rectifier:**
    - Near-zero drop, precise rectification.
    - Diode conducts only in forward bias (op-amp compensates for reverse bias).

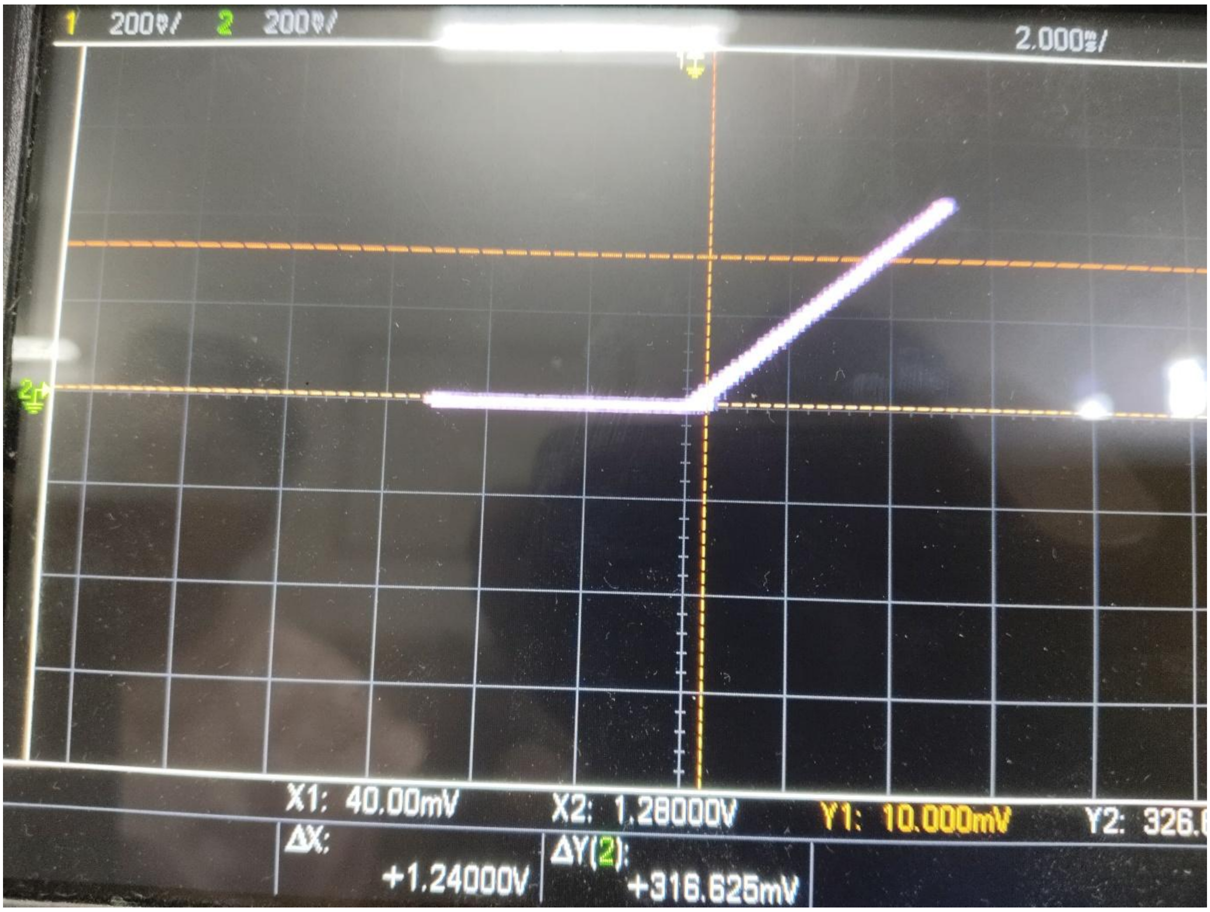
These op-amp based rectifiers are better than diode and resistor based rectifiers. Op-amp based rectifiers are better in terms of accuracy, precision, speed, input impedance, temperature stability, and linearity. Conventional diode-based rectifiers have a voltage drop across the diode, typically around 0.7 volts for silicon diodes. In these rectifiers, the output waveform has a lower amplitude due to the cut in voltage of the diode.

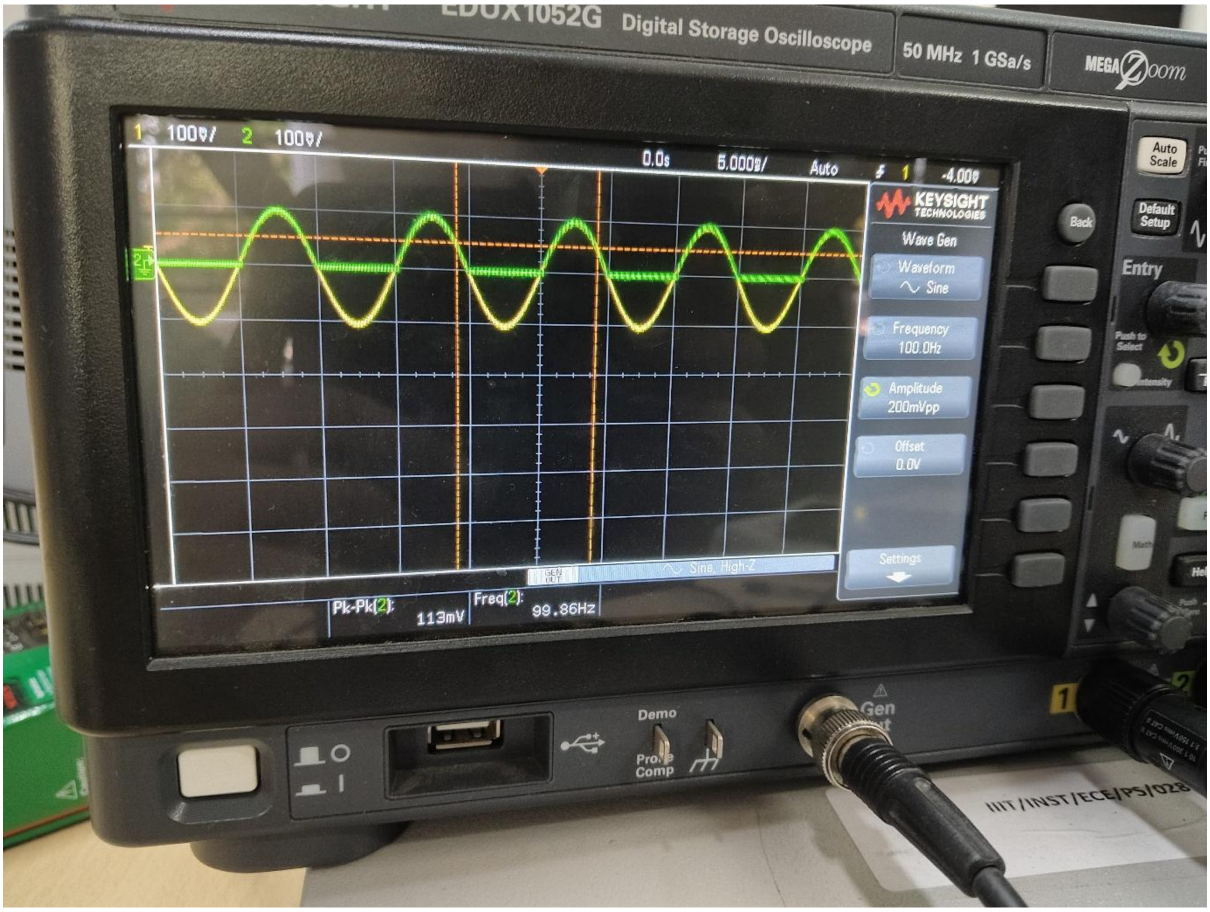
Op-amp rectifiers, on the other hand, can achieve nearly zero voltage drop during rectification. The diode acts as a DC voltage source with reversed polarities, resulting in a decreased output sinusoid amplitude.

In contrast, the Op Amp-based rectifier circuit behaves differently. When the input sinusoid is positive, the Op Amp amplifies it, causing the diode to be forward biased and act as a short circuit


KEYSIGHT
EDUX1052G Digital Storage Oscilloscope
50 MHz 1 GSa/s
InfiniiVision
Pk-Pk(2): 270mV
Freq(2): 100.11Hz


KEYSIGHT
EDUX1052G Digital Storage Oscilloscope
50 MHz 1 GSa/s
InfiniiVision
Pk-Pk(2): 270mV
Freq(2): 100.0Hz

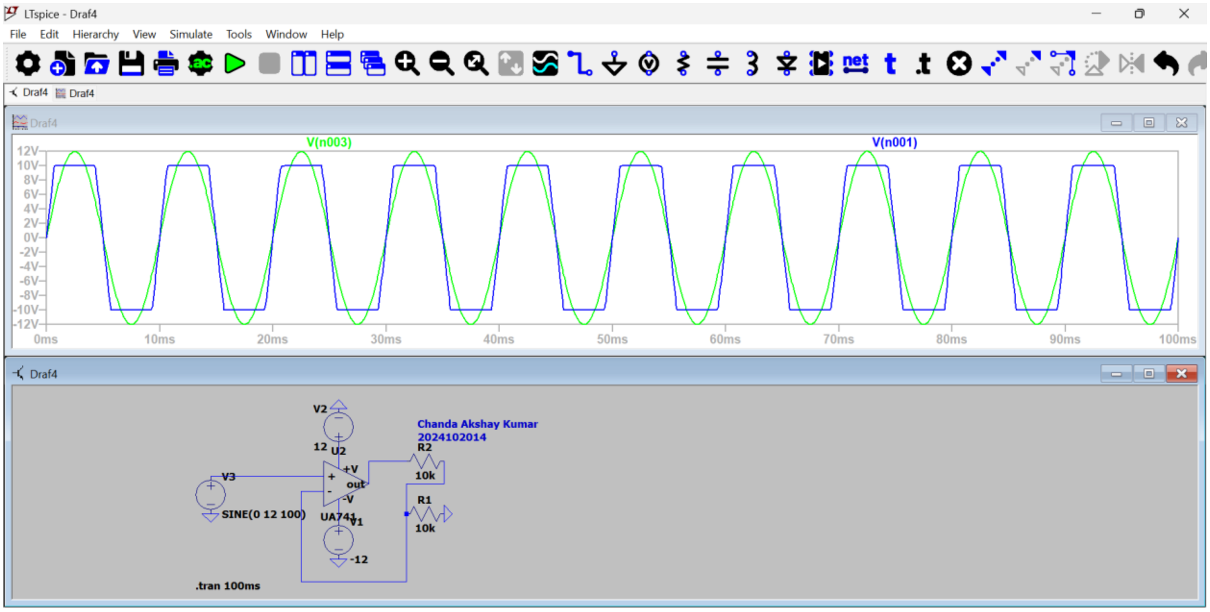

1 200mV/ 2 200mV/
2.000ms/
X1: 40.00mV
X2: 1.28000V
Y1: 10.000mV
ΔX: +1.24000V
ΔY(2): +316.625mV

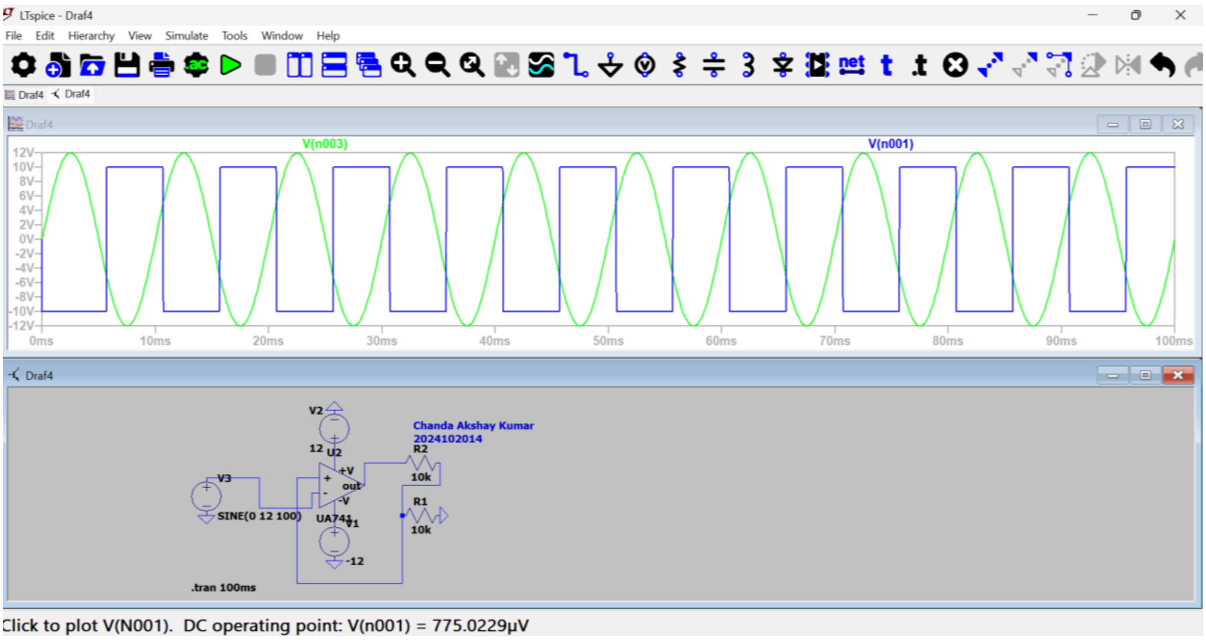

EDUX1052G Digital Storage Oscilloscope
50 MHz 1 GSa/s
MEGA Zoom
1 100mV/ 2 100mV/
0.0s 5.000ms/ Auto
KEYSIGHT TECHNOLOGIES
Wave Gen
Waveform Sine
Frequency 100.0Hz
Amplitude 200mVpp
Offset 0.0V
Settings
Pk-Pk(2): 113mV
Freq(2): 99.86Hz
Auto Scale
Default Setup
Back
Entry
Demo
Probe Comp
IIIT/INST/ECE/PS/028

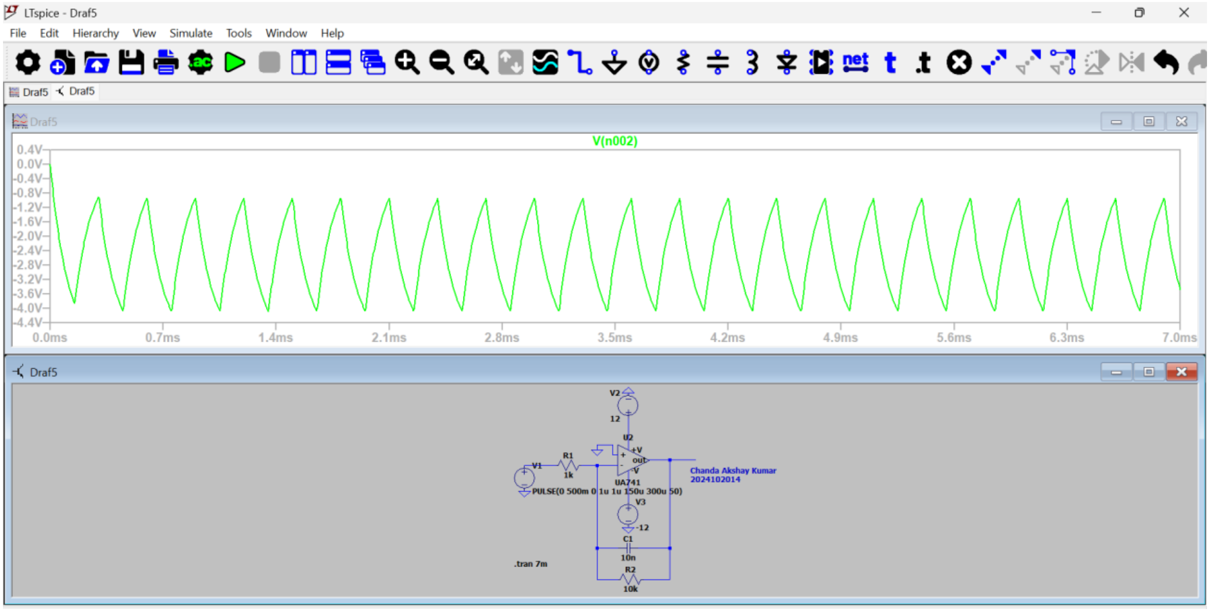
Conclusion

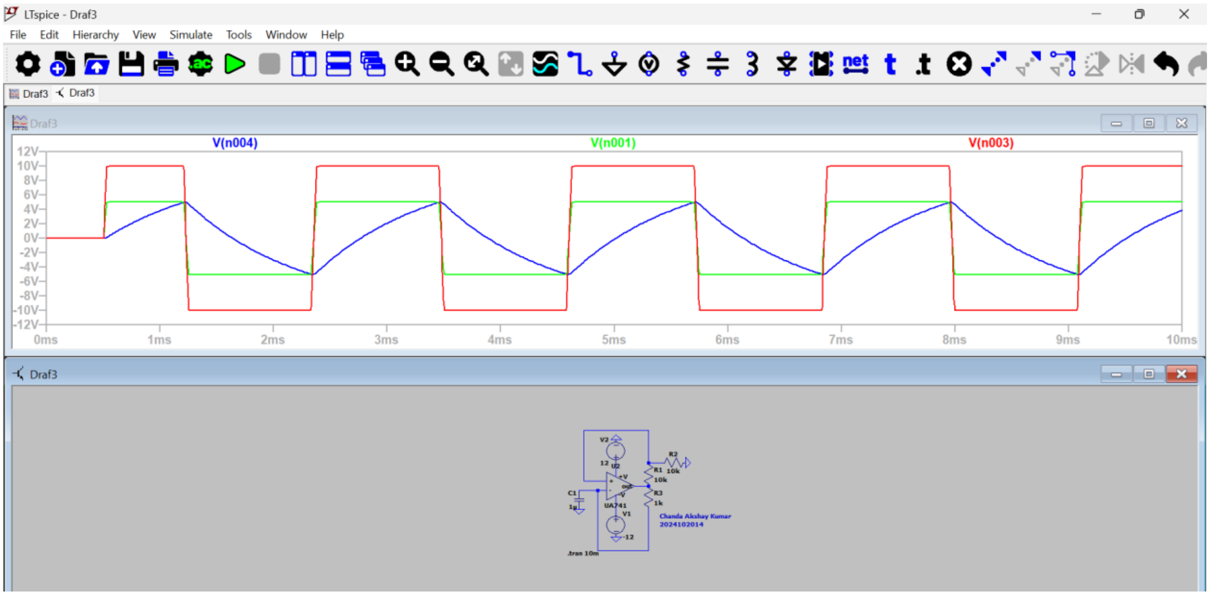
- **Negative Feedback:** Improves stability (integrator, rectifier).
- **Positive Feedback:** Causes hysteresis (oscillators).
- Op-amp circuits outperform passive components in precision applications.

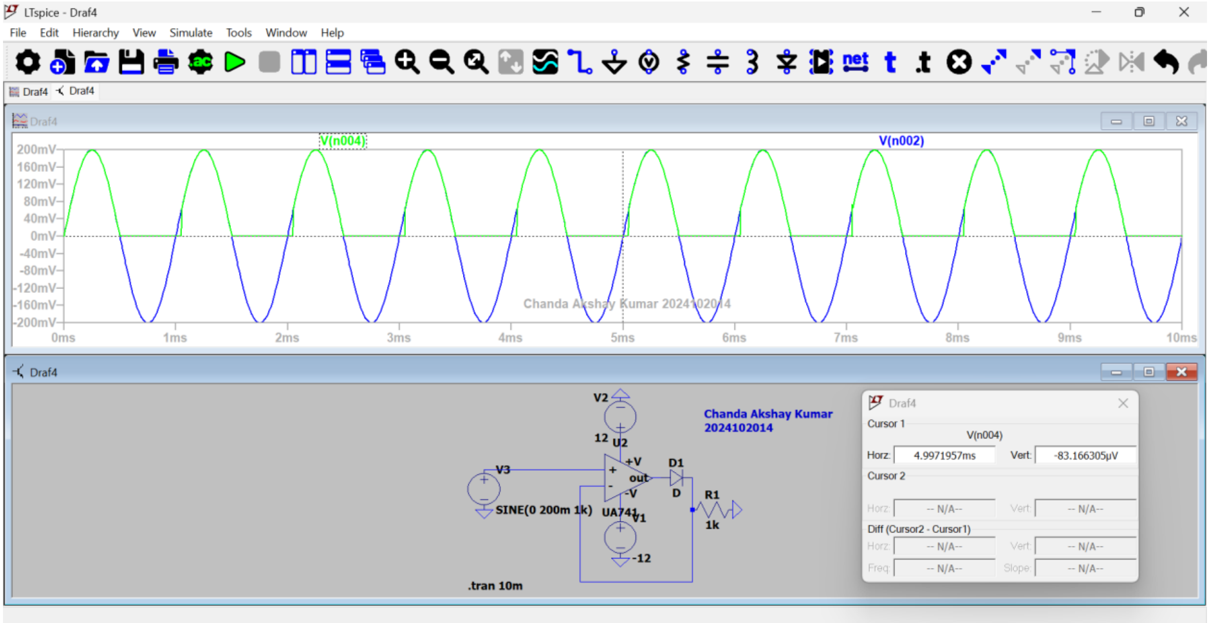
LTSPICE






LTspice - Draf5
File Edit Hierarchy View Simulate Tools Window Help
Draf5
V(n002)
0.4V 0.0V -0.4V -0.8V -1.2V -1.6V -2.0V -2.4V -2.8V -3.2V -3.6V -4.0V -4.4V
0.0ms 0.7ms 1.4ms 2.1ms 2.8ms 3.5ms 4.2ms 4.9ms 5.6ms 6.3ms 7.0ms
V2
12
U2
R1
1k
V1
UA741
PULSE(0 500m 0 1u 1u 150u 300u 50)
V3
-12
C1
10n
R2
10k
.tran 7m
Chanda Akshay Kumar
2024102014


LTspice - Draf3
File Edit Hierarchy View Simulate Tools Window Help
Draf3
V(n004)
V(n001)
V(n003)
12V 10V 8V 6V 4V 2V 0V -2V -4V -6V -8V -10V -12V
0ms 1ms 2ms 3ms 4ms 5ms 6ms 7ms 8ms 9ms 10ms
Chanda Akshay Kumar
2024102014
.tran 10m


LTspice - Draf4
File Edit Hierarchy View Simulate Tools Window Help
V(n004)
V(n002)
200mV
160mV
120mV
80mV
40mV
0mV
-40mV
-80mV
-120mV
-160mV
-200mV
0ms
1ms
2ms
3ms
4ms
5ms
6ms
7ms
8ms
9ms
10ms
Chanda Akshay Kumar 2024102014
V2
12
U2
V3
SINE(0 200m 1k)
UA741
V1
-12
D1
D
R1
1k
.tran 10m
Chanda Akshay Kumar
2024102014
Cursor 1
V(n004)
Horz: 4.9971957ms
Vert: -83.166305µV
Cursor 2
Diff (Cursor2 - Cursor1)