VLSI : Very Large Scale Integration

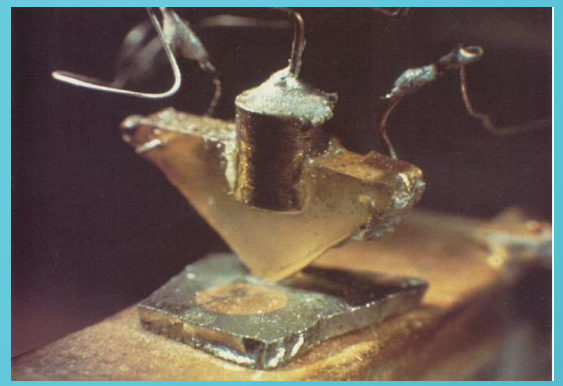
So, what is very large here…..

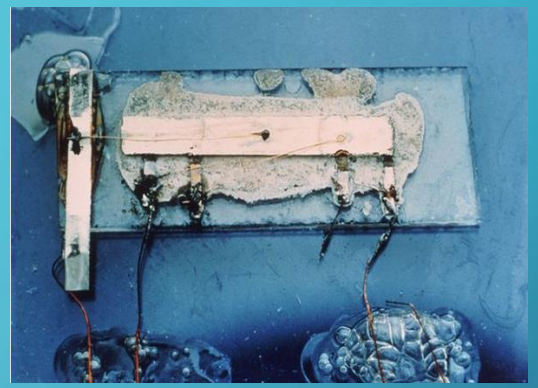
THE 20TH CENTURY

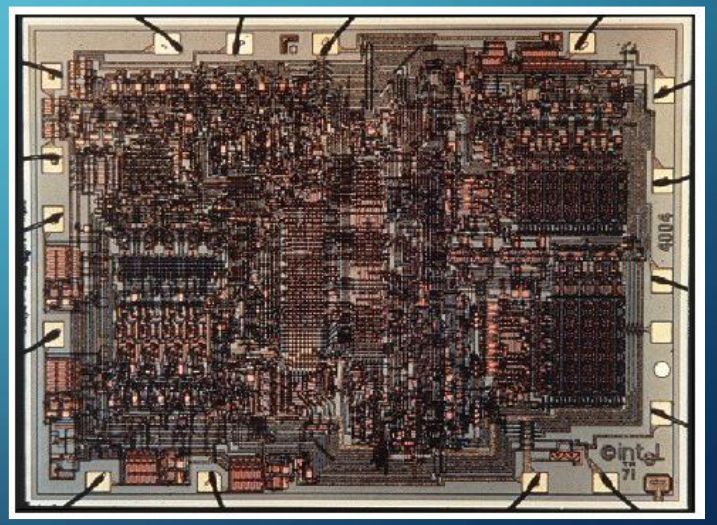
- There were several inventions in 20th century, such as Airplanes, Computers, Space crafts, Nuclear power generators, etc.
- Everything controlled by Electronics.
- Electronics: One of the most important invention in the 20th century.
- What is Electronics: To use the electrons ??????
  - Electronic Circuits
  - Integrated Circuits (ICs)
- Life without Integrated Circuits (ICs): 

EVALUATION

- Vacuum tubes: 1907
- The point contact transistor: 1947
- Junction Transistor: 1949
- First Integrated Circuit: 1958
- Commercial Integrated Logic Gates: 1960
- CMOS and/or PMOS based design (Calc.): 1960’s
- NMOS based Processor (4004, etc.): 1970’s
- CMOS based designs: 1980’s





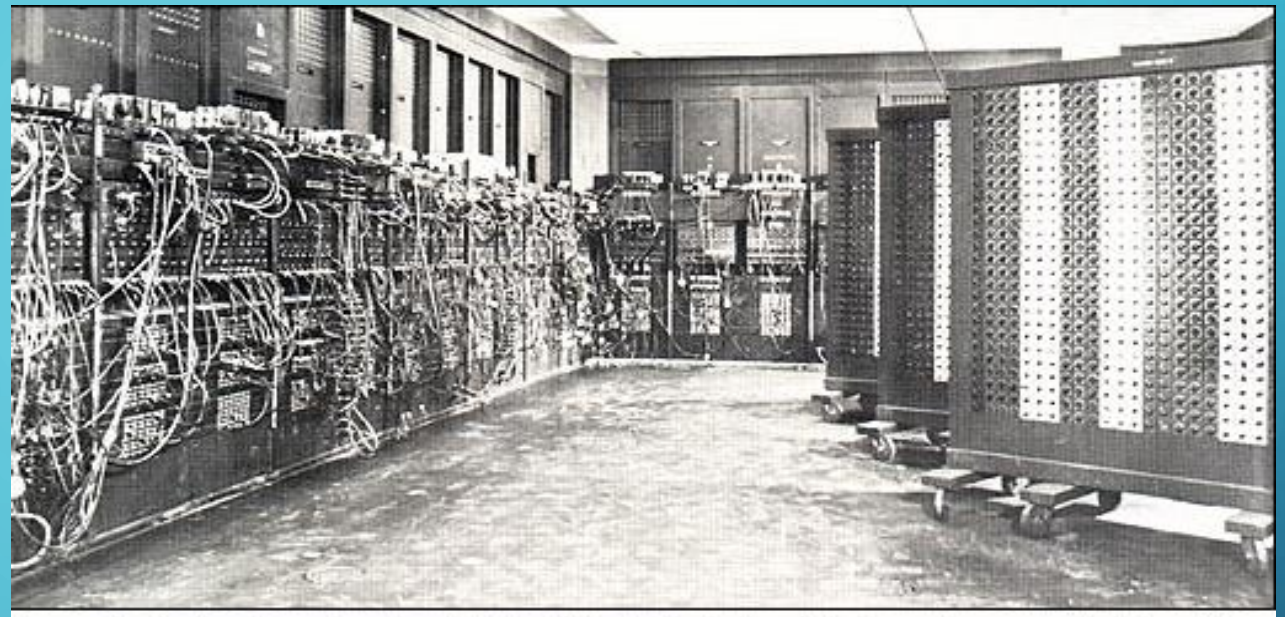


EVALUATION

- 2003:
  - Intel Pentium 4 microprocessor (containing approx. 55million transistor)
  - 512 Mbit DRAM (more than 0.5 billion transistor)
- More than 50% annual growth rate over 45 years.
- No other technology has grown so fast for so long.
- Miniaturization of transistors make this possible.

The Babbage Difference Engine (1832)
25,000 parts
Cost: 17,470 ponds

- Mostly Mechanical System



Among the first assignments given to Eniac, first all-electronics digital computer, was a knotty problem in nuclear physics. It produced the answer in two hours. One hundred engineers using conventional methods would have needed a year to solve the problem

ENIAC: Electronics Numerical Integrator & Computer

- First general purpose electronic computer
- It was a Turing-complete, digital computer capable of being reprogrammed
- Designed by John Mauchly and J. Presper Ekert (1946)
- Big size, huge power, short life time of filaments, doing only basic operations.

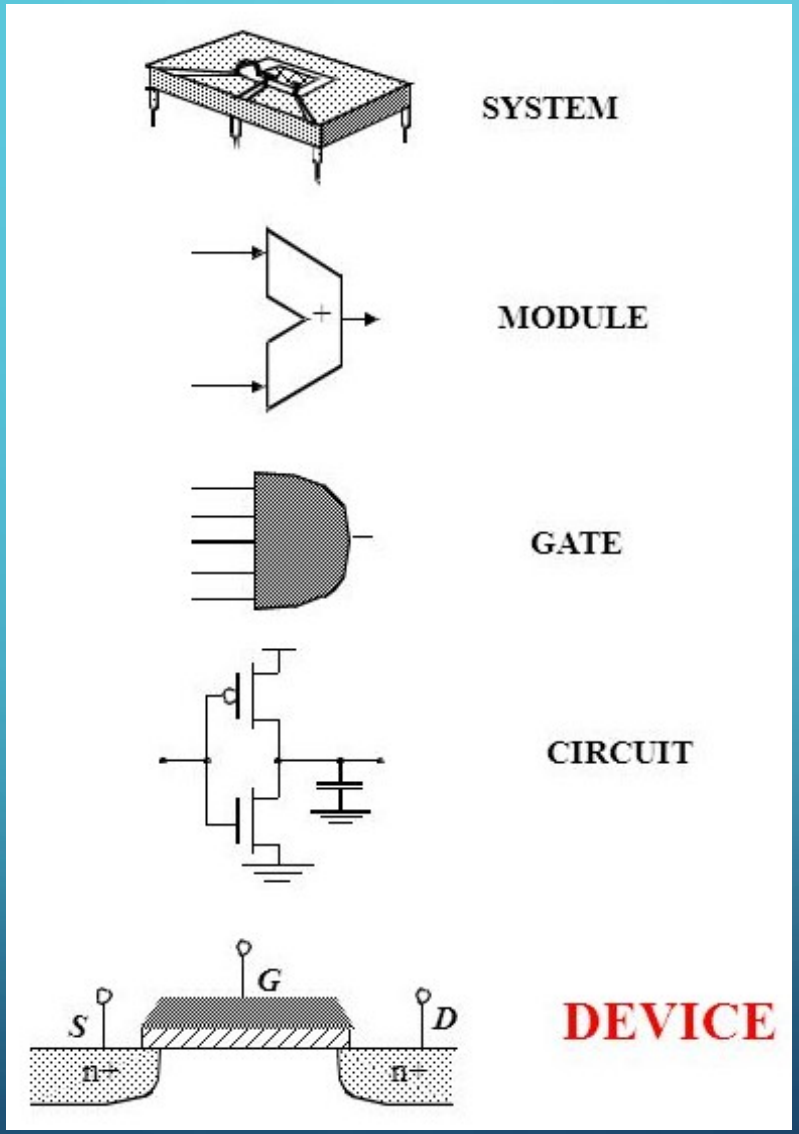
TERMINOLOGY

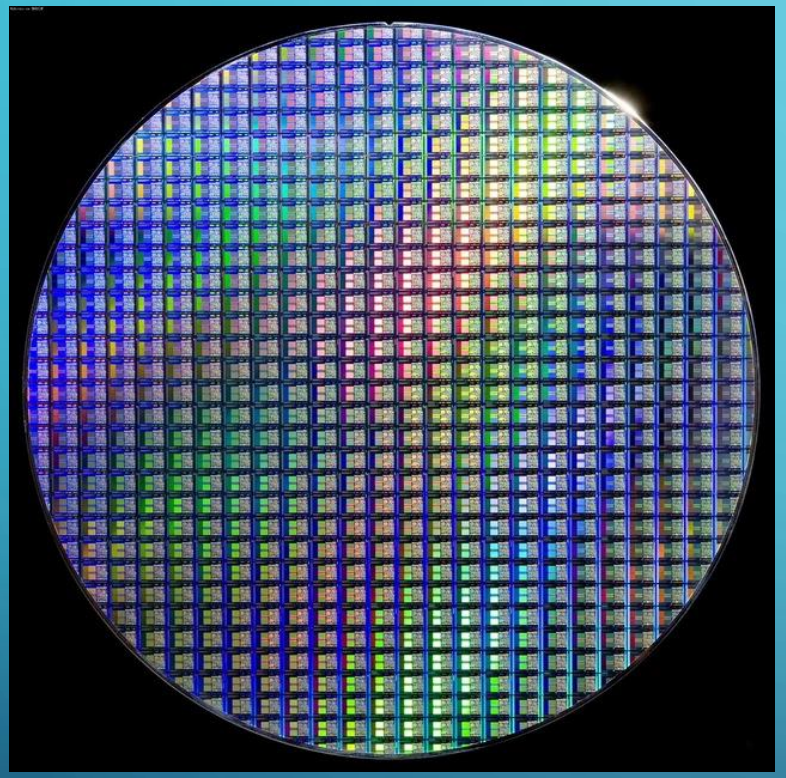
- Small Scale Integration (SSI): the ICs functioned as logic gates, flip-flops, etc.
- Medium Scale Integration (MSI): Multiplexers, decoders, etc.
- Large Scale Integration (LSI): early microprocessors, small memories, PAL, etc.

- Dividing line between LSI and Very Large Scale Integration (VLSI) is somewhat fuzzy. Therefore, number of transistors provides a good criterion.

Technology	Number of gates/transistors* per chip	Examples	Year
SSI	1 to 20	74XX series, 4xxx series	60's
MSI	100 to 1000	74XXX series, 45XX series	70's
LSI	1000 to 10,000/100 to 100,000*	8085,	80's
VLSI	10,000 to 100,000/1,000,000 *	CPLD, FPGA, advanced µC, SoC	90's

ABSTRACTION LEVELS

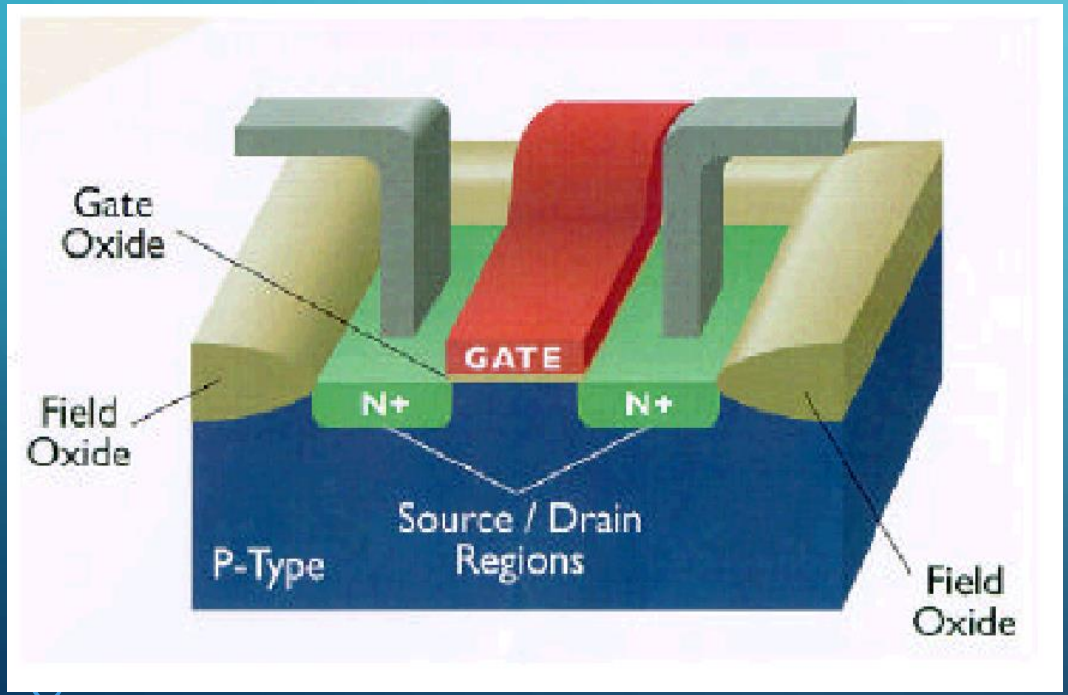


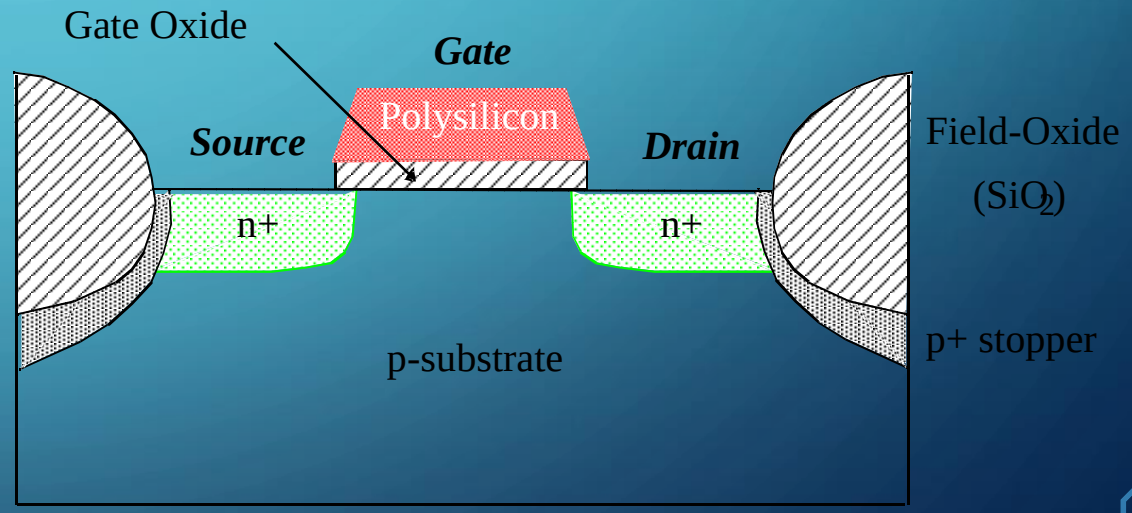



my IC!

The MOS Transistor

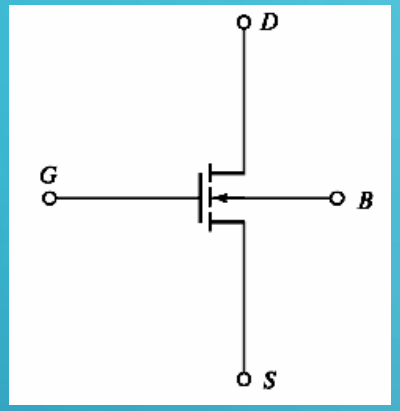
- **MOSFET : Metal Oxide Semiconductor Field Effect Transistor**
- **n-channel MOSFET (nMOS) & p-channel MOSFET (pMOS)**
- **JFET – Junction Field Effect Transistor**





CROSS-SECTION of NMOS Transistor

The top view of nMOS transistor (Enhancement type)



Symbol

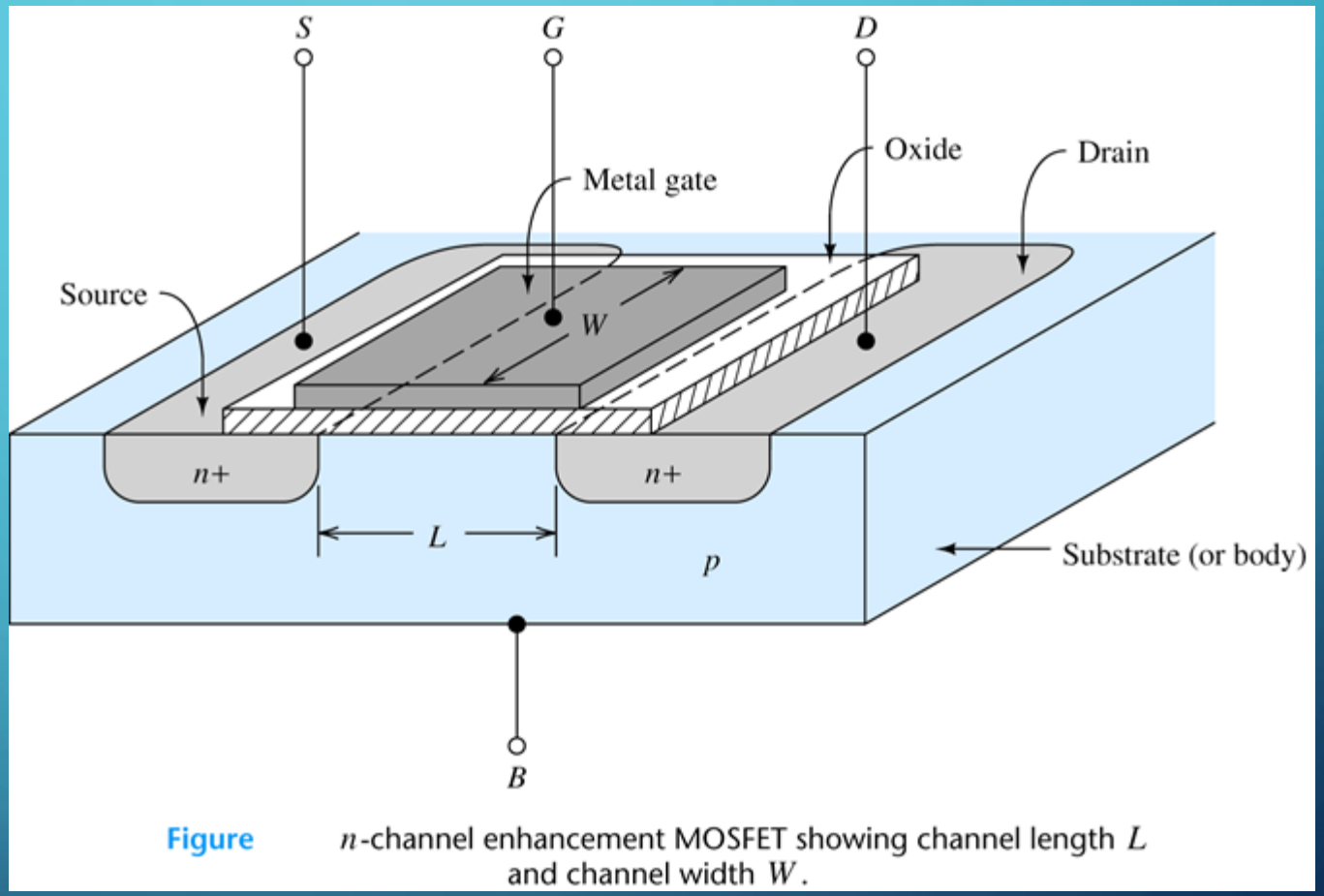
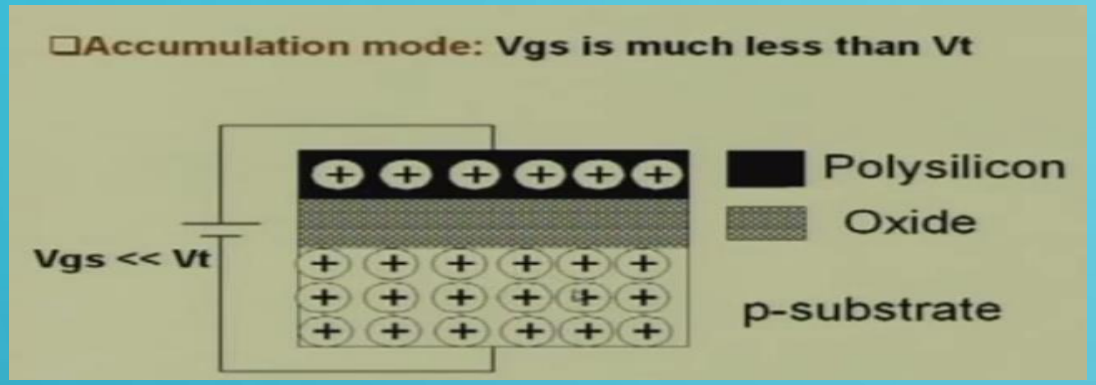
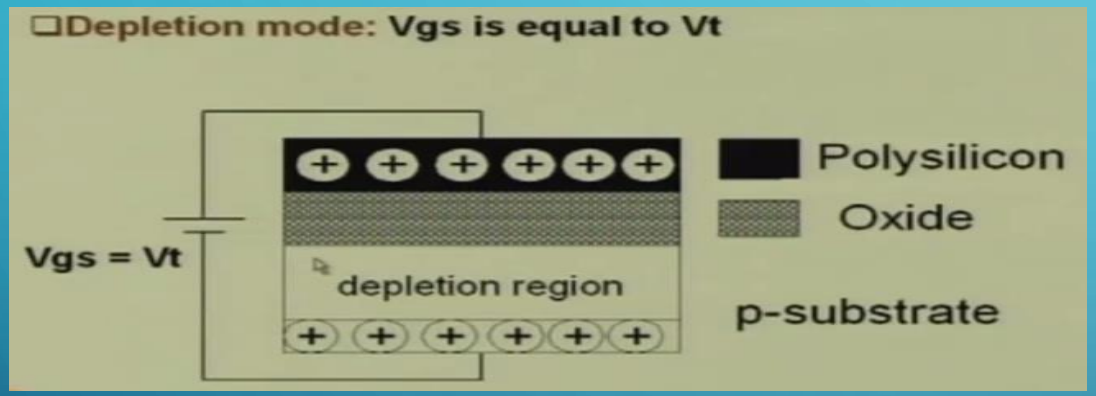


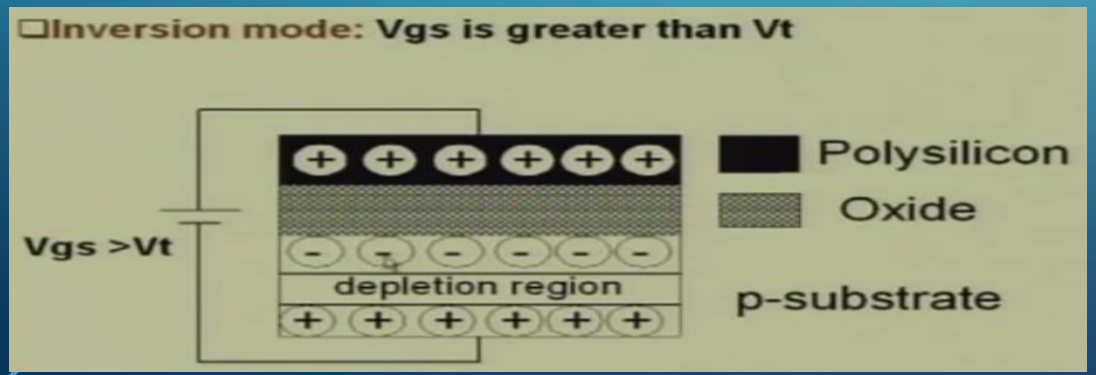
Figure *n*-channel enhancement MOSFET showing channel length L and channel width W.

- Device characteristics depend on L,W, Oxide thickness, doping levels, etc.

Modes of Operation







- **Accumulation: When $V_{gs} << V_t$**
- **Depletion: When $V_{gs} = V_t$**
- **Inversion: When $V_{gs} > V_t$**

V_t is the threshold voltage.
???????

Field Effect???

- Uses an electric field to control the shape and hence the electrical conductivity of a channel.
- FETs are also known as **unipolar transistors** since they involve single-carrier-type operation. (of one type of charge carrier in semiconductor material).
- FET's conductivity is regulated by a voltage applied to a terminal (the gate) which is insulated from the device. The applied gate voltage imposes an electric field into the device, which in turn attracts or repels charge carriers to or from the region between a source terminal and a drain terminal. The density of charge carriers in turn influences the conductivity between the source and drain.
- The FET has several forms, but all have high input impedance. While the conductivity of a non-FET is regulated by the input current (the emitter to base current) and so has a low input impedance.

Let’s now develop an expression/ equation for Drain current (I_D)

Static Characteristics:

$$I_{ds} = \frac{Charge\ induced\ in\ the\ channel\ (Q_c)}{Electron\ transit\ time\ (t_r)}$$

Induced channel is formed in an E-nMOS.

$V_{GS} > V_T$ (Consider *Source* and *Body* are at ground)

Therefore, $I_D = 0$ for $V_{GS} < V_T$ (???, not true, however consider at the moment)

For $V_{GS} > V_T$: MOS begin to conduct
and V_{DS} increases linearly, I_D increases linearly } For small V_{DS}
defined as $V_{DS} \leq V_{GS} - V_T$ .....(1)

For small V_{DS}-

$$I_D = \frac{Q_c}{\tau} \quad .....(2)$$ (Average induced charge (due to electron) flowing from *drain* to *source* per unit time)

Since, $I_D \longrightarrow$ drift current due to field

- The transit time is related to the drift velocity;

$$\tau = \frac{L}{v_d} \quad \text{.....(3)}$$

and $v_d = \mu_n . E$ .....(4) (E= $\frac{V_{DS}}{L}$; assuming *E* is uniform along the length of the channel 'L')

then,

$$I_D = \frac{Q_c \mu_n V_{DS}}{L^2} \quad \text{.....(5)}$$

❖ Now, we know, the gate and body of a MOS form a parallel plate capacitor with oxide (e.g. SiO_2) as a oxide insulator i.e. dielectric. Therefore, the charge Q_c stored in the channel is given as-

$$Q_c = V_G . C_g \longrightarrow V_G \left(\frac{A.\epsilon}{t_{ox}}\right) \longrightarrow V_G . W.L. \left(\frac{\epsilon}{t_{ox}}\right) \quad \text{.....(6)}$$

where;

V_G is gate to channel or plate voltage and

Cg is gate to channel capacitance.

- We know, channel of induced charge is formed, when $V_{GS} > V_T$;
- Therefore, Gate capacitance has plate voltage of $V_G = V_{GS} - V_T$ along the gate from the source to drain for $V_{DS}=0$.
- For $V_{DS}>0$;

The source to channel voltage increases along the length, from 0 at source to V_{DS} at the drain.

Therefore, V_G varies from $(V_{GS} - V_T)$ to $(V_{GS} - V_T - V_{DS})$ along the length of the plate.

Approximation: If we assume the channel voltage increases linearly, then the average or effective voltage-

$$V_G = V_{GS} - V_T - \frac{V_{DS}}{2} \quad \ldots\ldots\ldots\ldots(6)$$

Then,

$$Qc = (V_{GS} - V_T - \frac{V_{DS}}{2}).\ W.\ L.\ (\frac{\epsilon}{t_{ox}})$$

❖ Then,

$$I_D = (V_{GS} - V_T - \frac{V_{DS}}{2}).\ \mu_n.V_{DS}.\frac{W.L}{L^2}.\ (\frac{\epsilon}{t_{ox}}) \quad \text{.....(7)}$$

$$I_D = \frac{1}{2}.\frac{W}{L}.\ \mu_n.C_{ox}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \qquad (C_{ox} = \frac{\epsilon}{t_{ox}}\ ;\ \text{Gate Cap/Area})$$

Or

$$I_D = \frac{W}{L}.\ \mu_n.C_{ox}[2(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}]$$

Or

$$I_D = K[2(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \qquad \text{for } V_{DS} \leq V_{GS}\text{-}V_T \text{ and } V_{GS} > V_T$$

Where K $(= \frac{1}{2}.\frac{W}{L}.\ \mu_n.C_{ox})$ A/V^2 is the device transconductance parameter

$K = \frac{1}{2}.K'(\frac{W}{L})$, where $K' = \mu_n.C_{ox}$ is the process transconductance parameter

- Now, as the V_{DS} increases, the device enter the *saturation* or *pinch-off region*;

$V_{DS} \geq V_{GS} - V_T$ (At $V_{DS} = V_{GS} - V_T$; I_D reaches maximum)

$I_D = K (V_{GS} - V_T)^2$ for $V_{DS} \geq V_{GS} - V_T$ and $V_{GS} > V_T$

Regions of Operation

- Cut-off Region: Accumulation or depletion mode, when no current flows between the source and drain
- Nonsaturated Region: Weak inversion mode when the drain current is dependent on the gate and the drain voltage a.k.a. Triode, linear, ohmic region, etc.
- Saturated Region: Strong inversion mode when the drain current is ideally independent of the drain-to-source voltage

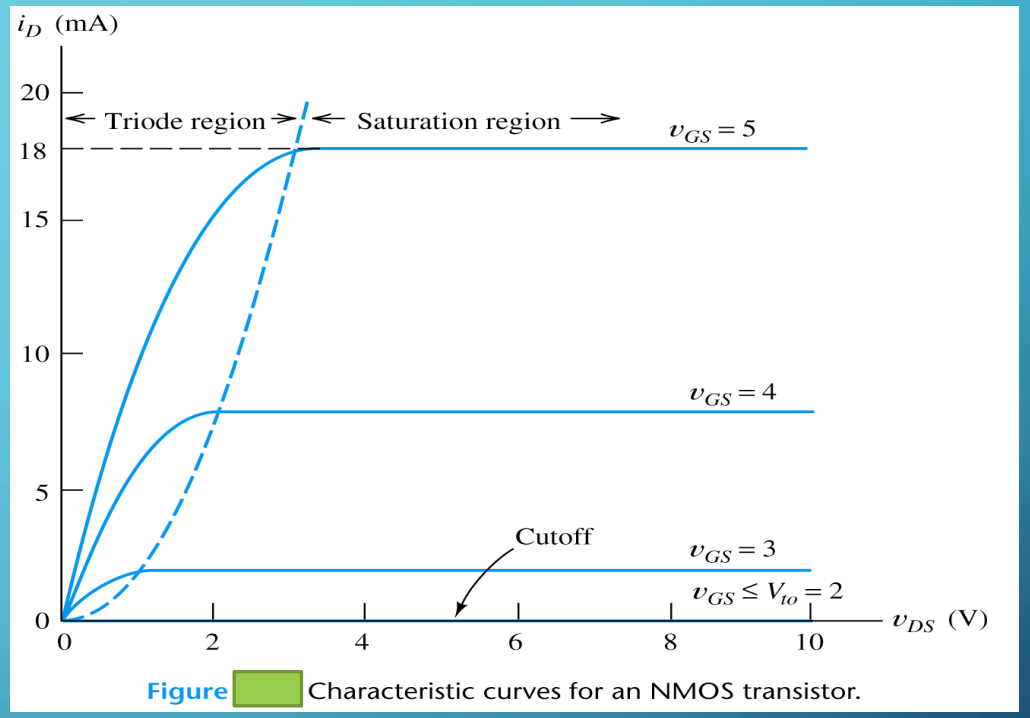


Figure Characteristic curves for an NMOS transistor.

$I_{ds} = 0; for\ V_{GS} < V_t$ **(Cut-off)??**
$I_{ds} = \frac{1}{2}\frac{W}{L}\mu_n C_{ox}[2(V_{gs} - V_t)V_{ds} - V_{ds}^2]$ **(Linear region)** For $V_{gs} \geq V_t$ and $V_{ds} < V_{gs} - V_t$
$I_{ds} = \frac{1}{2}\frac{W}{L}\mu_n C_{ox}(V_{gs} - V_t)^2$ **(Saturation region)** $V_{gs} \geq V_t$ and $V_{ds} > V_{gs} - V_t$

Regions of Operation (shown for nMOS)

Operation in the Cutoff region

PN junction: reverse bias

i_D=0 for v_{GS}<V_t

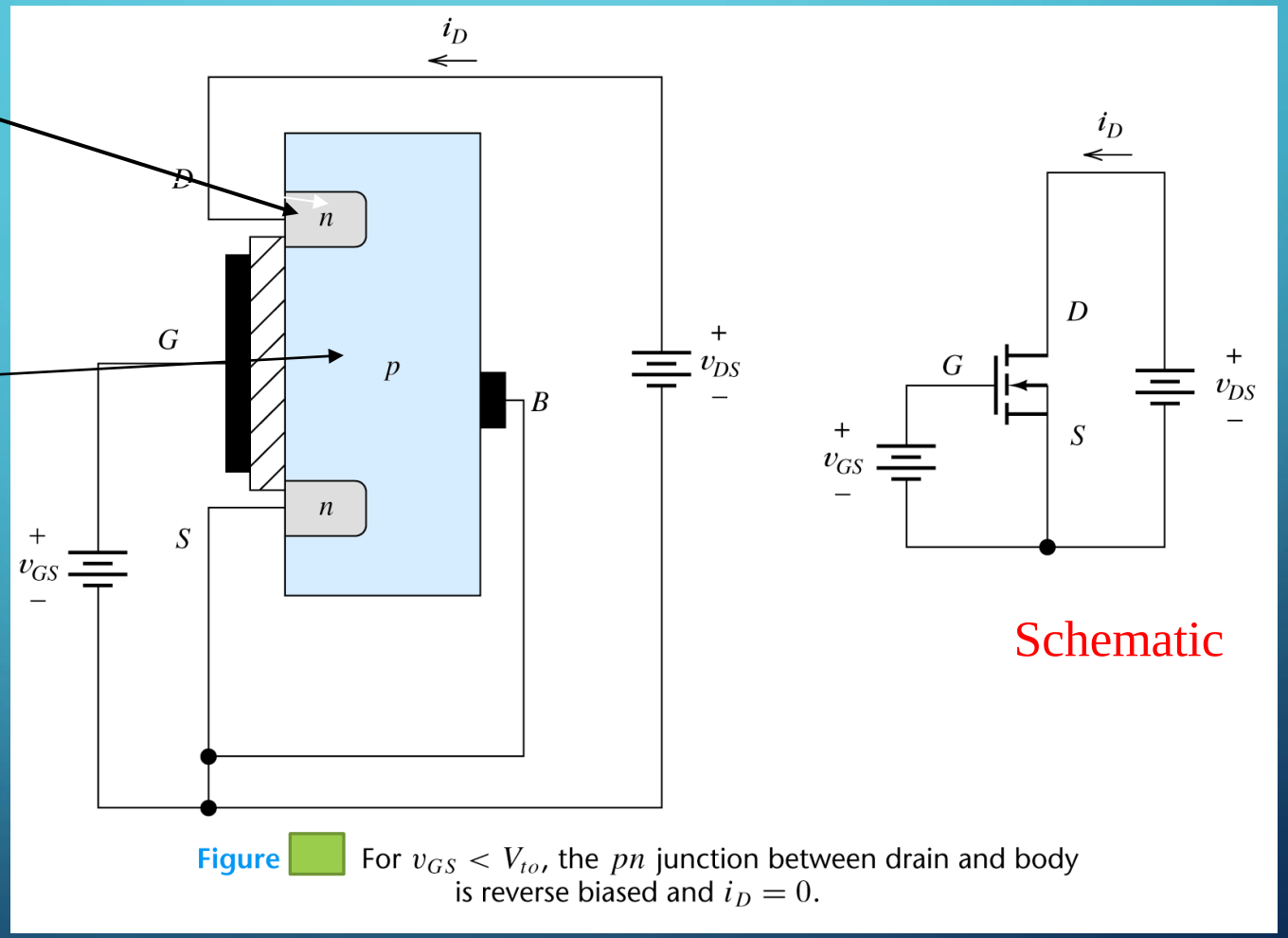


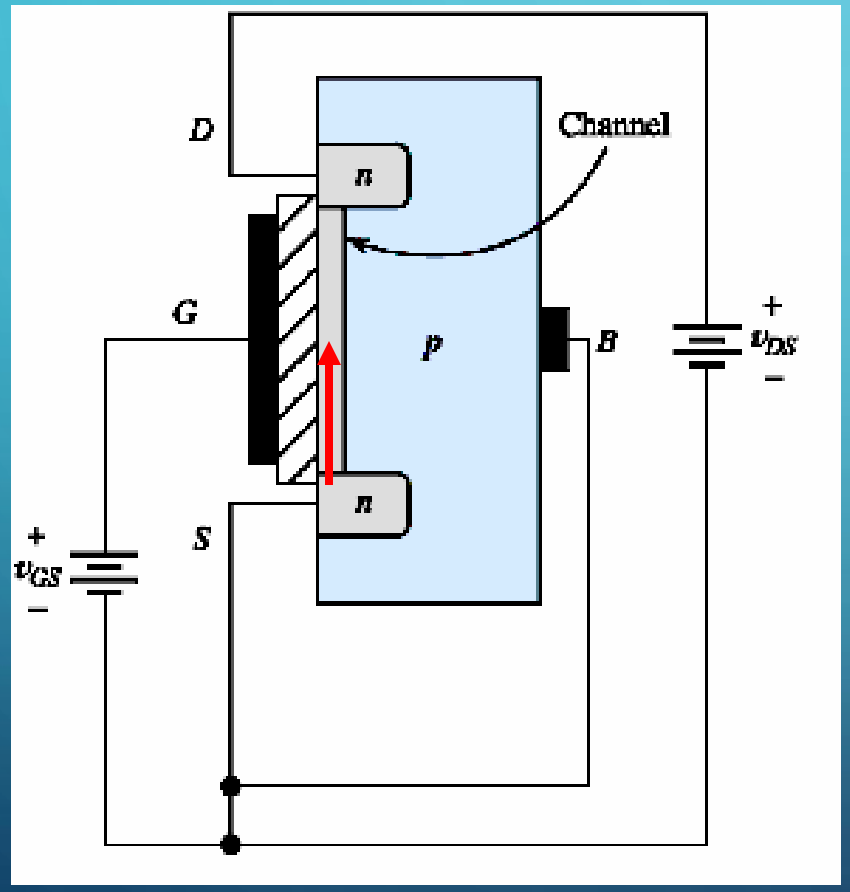
Figure For $v_{GS} < V_{to}$, the pn junction between drain and body is reverse biased and $i_D = 0$.

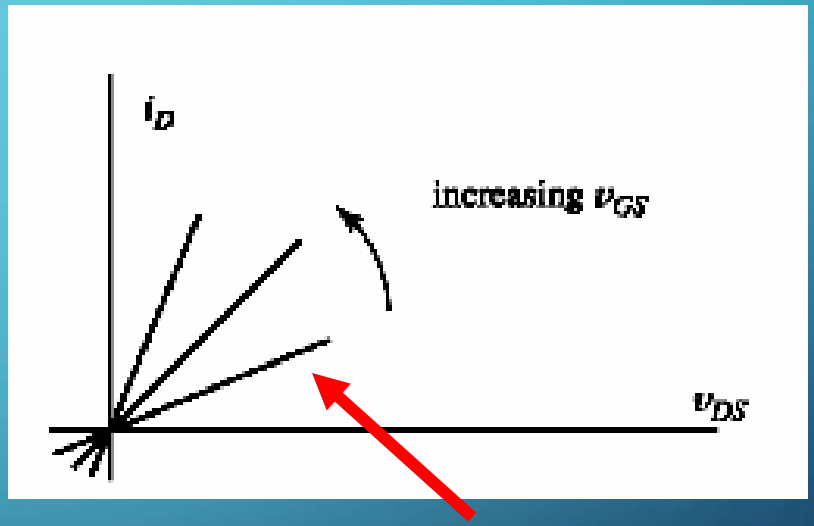
When v_{GS}=0 then i_D=0 until v_{GS}>V_t (V_t –threshold voltage)

Regions of Operation (shown for nMOS), cont.…

Operation in the Triode Region

For $v_{DS} < v_{GS} - V_t$ and $v_{GS} > V_t$; the NMOS is operating in the triode region

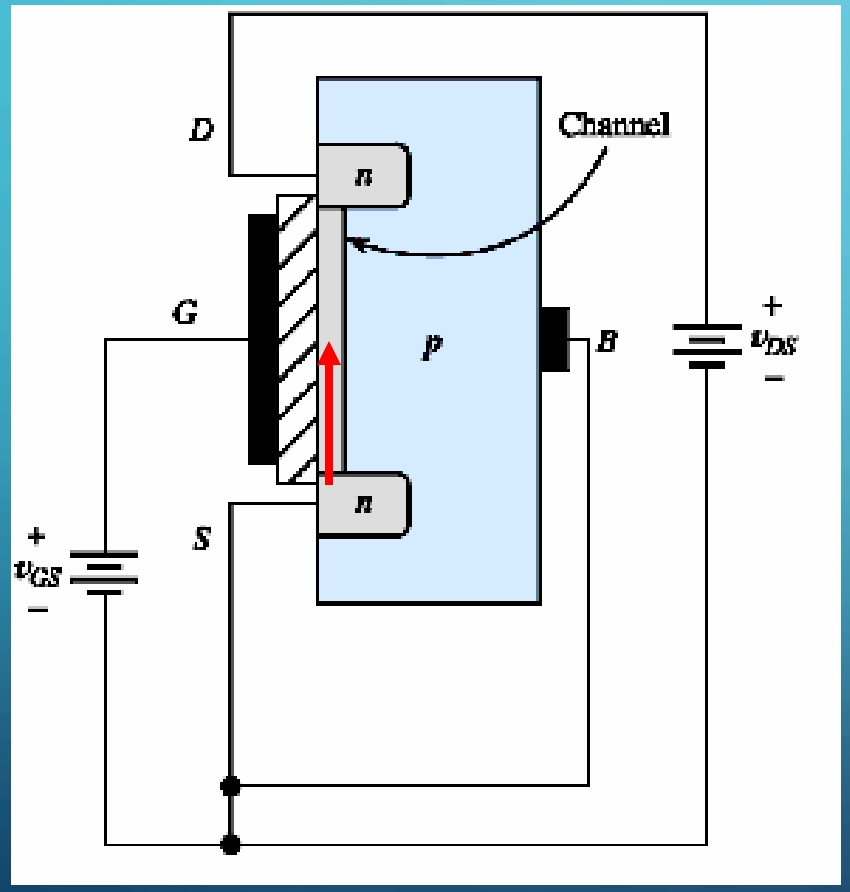




- Resistor like characteristic (R between S & D, Used as voltage controlled R)
- For small v_{DS}, i_D is proportional to the excess voltage $v_{GS} - V_t$

Regions of Operation (shown for nMOS), cont.…

Operation in the Triode Region



$$i_D = K\left[2(v_{GS} - V_{t0})v_{DS} - v_{DS}^2\right]$$

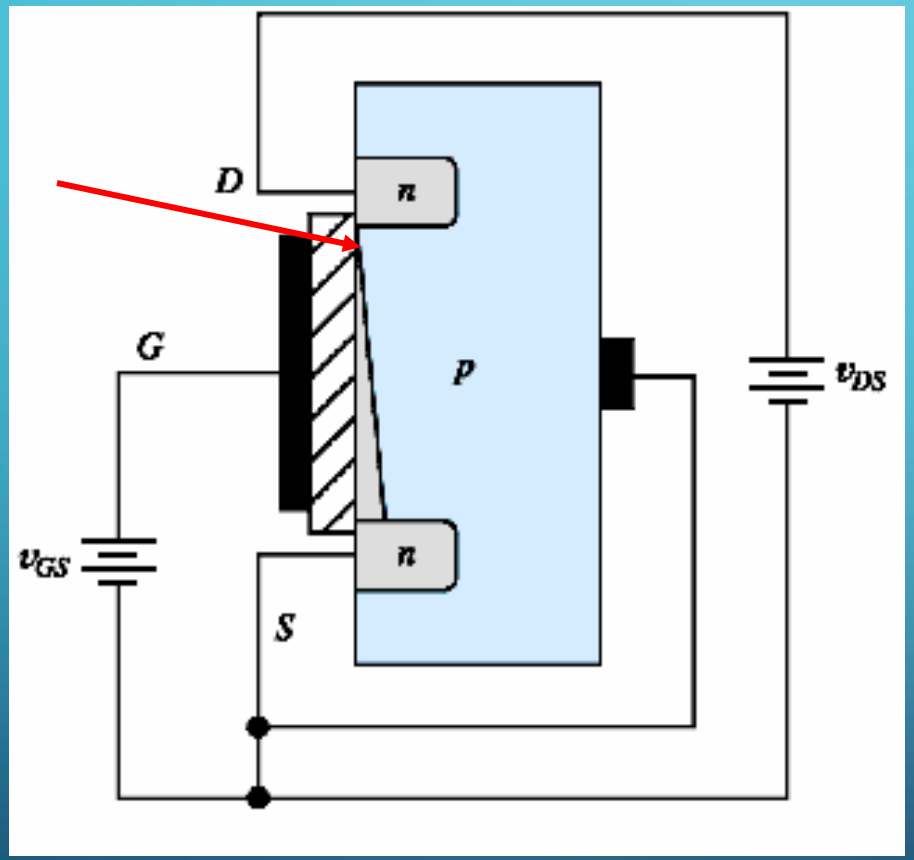
$$K = \left(\frac{W}{L}\right)\frac{KP}{2}$$

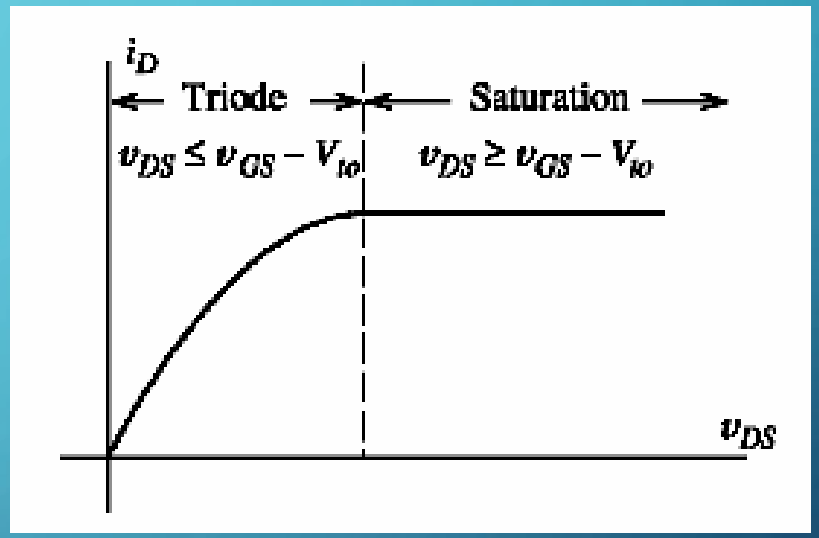
Device parameter KP for NMOSFET is 50 mA/V^2

Regions of Operation (shown for nMOS), cont.…

Operation in the Saturation Region (v_{DS} is increased)

Tapering of the channel - increments of i_D are smaller when v_{DS} is larger





$$i_D = K(v_{GS} - V_{t0})^2$$

Regions of Operation (shown for nMOS), cont.…

Example 1

An nMOS has W=160 mm, L=2 mm, KP= 50 mA/V^2 and V_{to}=2 V.

Plot the drain current characteristic vs drain to source voltage for v_{GS}=3 V.

$$i_D = K\left[2(v_{GS} - V_{t0})v_{DS} - v_{DS}^2\right]$$

$$i_D = K(v_{GS} - V_{t0})^2 \qquad K = \left(\frac{W}{L}\right)\frac{KP}{2}$$

Regions of Operation (shown for nMOS), cont.…

Example 1

Channel length modulation

i_d depends on v_{DS} in saturation region

(approx: i_D =const in saturation region)

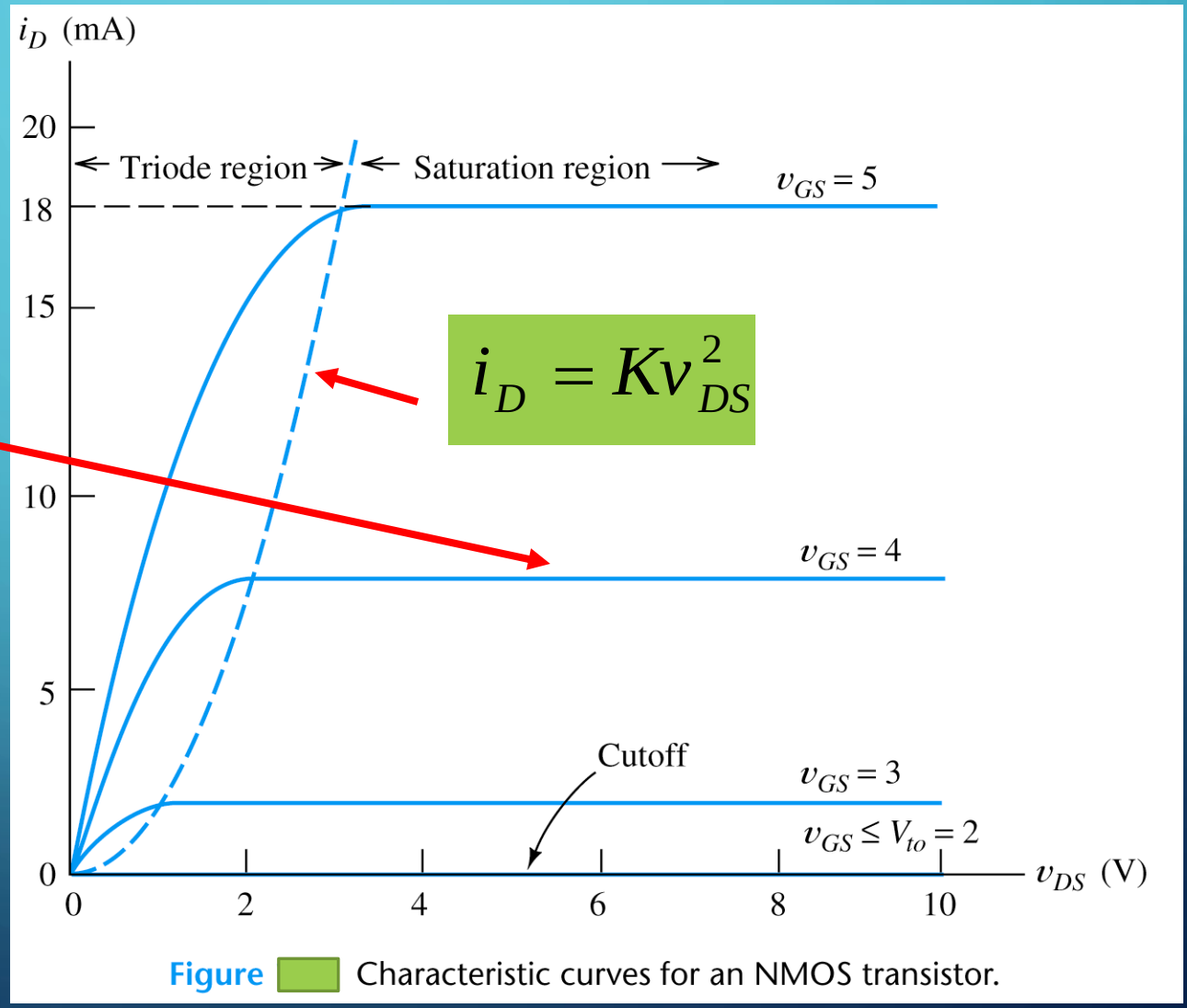


Figure Characteristic curves for an NMOS transistor.

Regions of Operation (shown for pMOS)

It is constructed by interchanging the *n* and *p* regions of n-channel MOSFET.

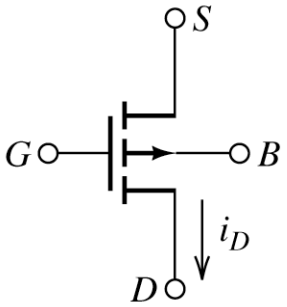
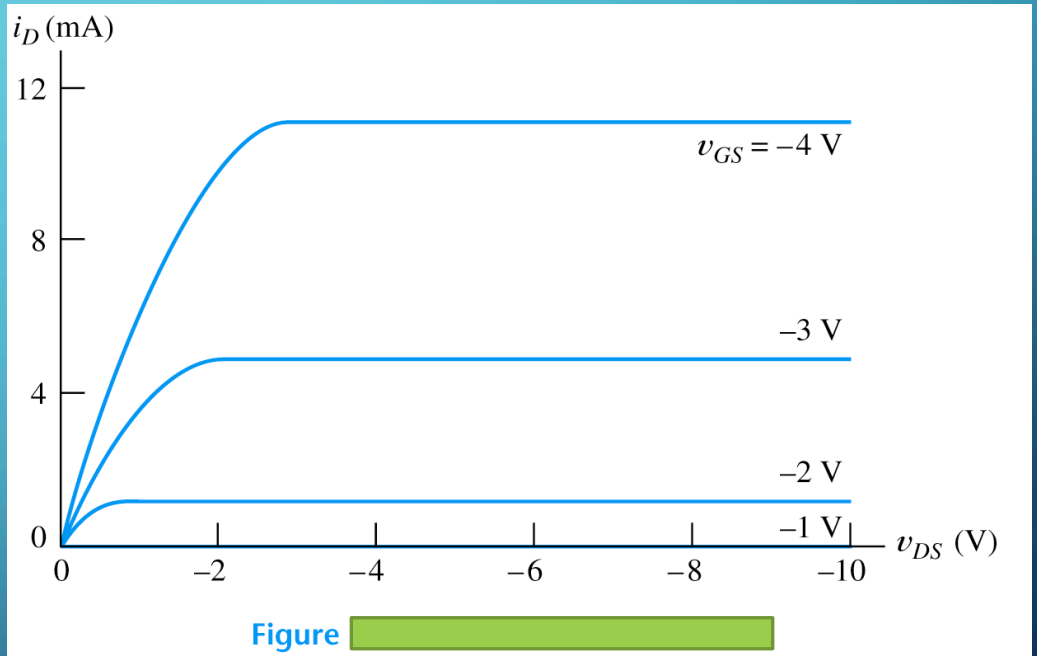


Figure Circuit symbol for PMOS transistor.

How does p-channel MOSFET operate?
-voltage polarities
-i_D current
-schematic



Figure

The Drain Current (I_d) dependence

For a fixed V_{ds} and V_{gs} , the factors that affect the Drain current (I_d) are-

- The channel length (L)- the distance between Source and Drain.
- The channel width (W)
- The threshold voltage (V_t)
- The oxide thickness
- The dielectric constant of the gate insulator
- The mobility of the carriers (electrons or holes)

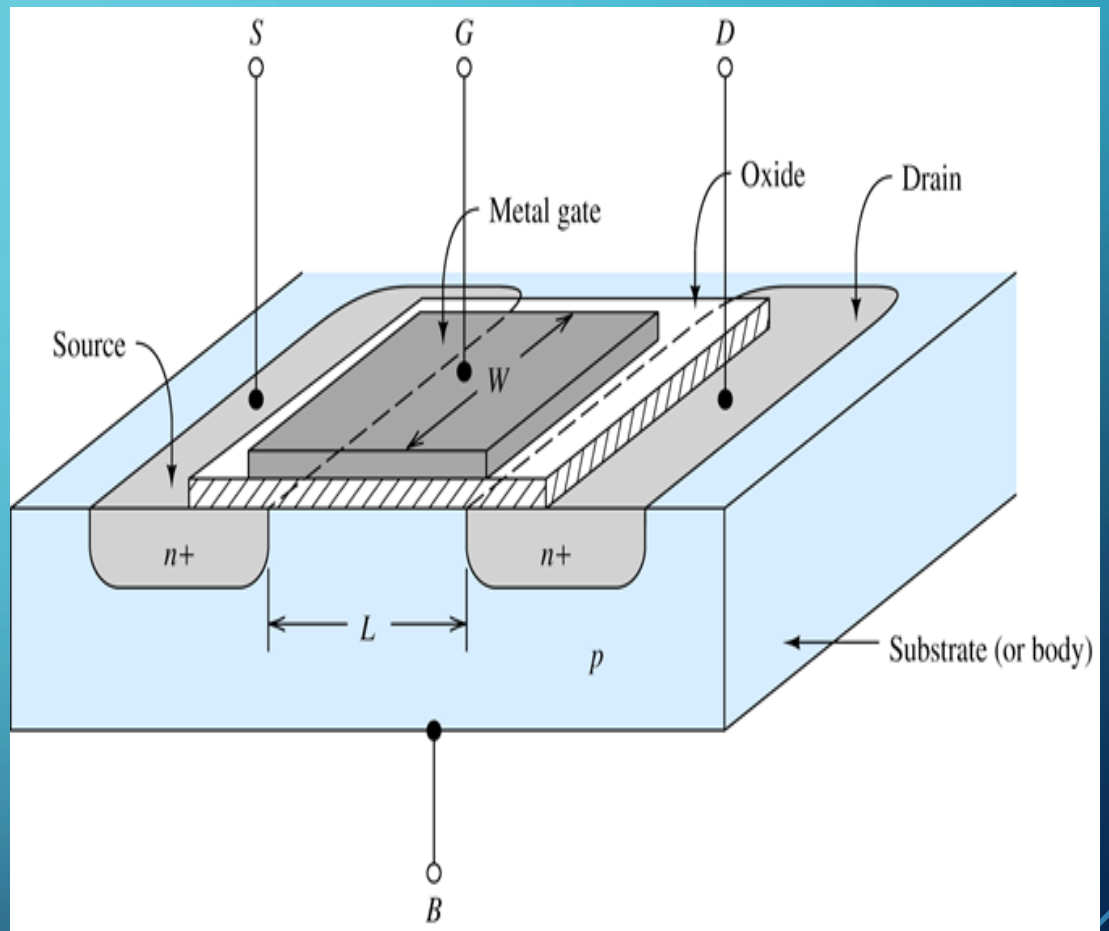
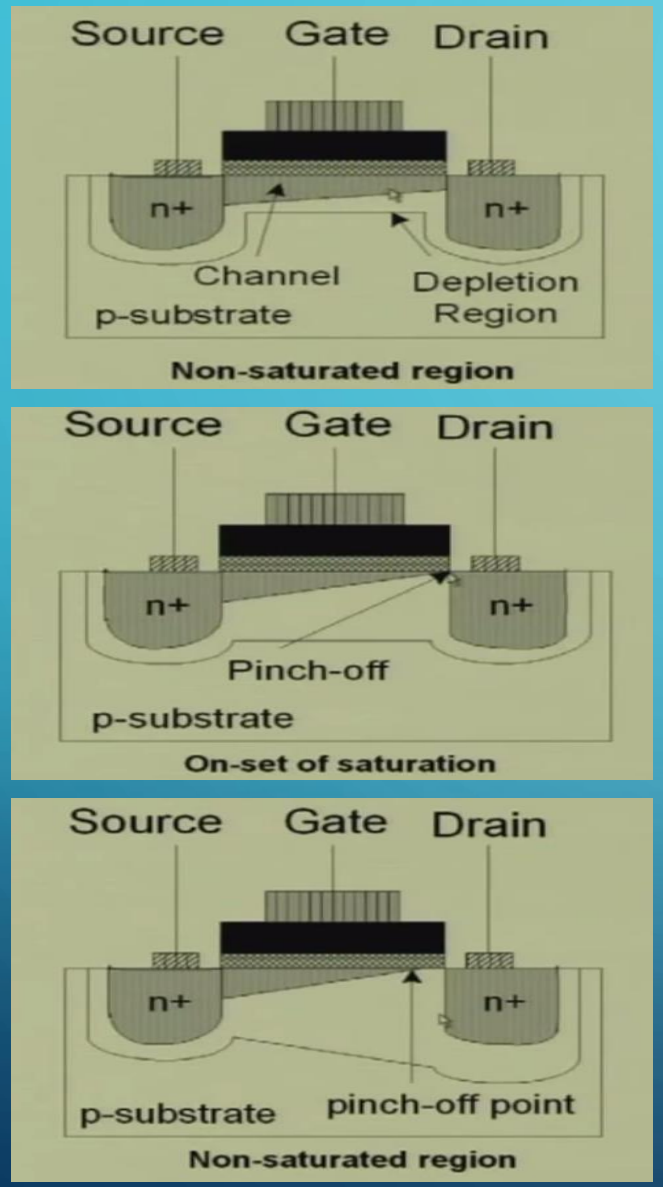


Figure *n*-channel enhancement MOSFET showing channel length *L* and channel width *W*.

What about the excess voltage

- Physically, the I_d increases with the increase in V_{ds} and the peak current occurs, when the channel is pinched-off at *Drain* side.
- Further increase in V_{ds} (drain voltage) beyond the pinched-off voltage ($V_{ds}=V_{gs}-V_t$), reduces the induced channel length. (CLM)
- What about this excess voltage ???? (voltage> $V_{gs}-V_t$)
- This excess voltage appear across the depletion region near the drain and creates a short region of high electric field.
- As a result, the free carriers (electrons or holes) in the narrowed inversion region are accelerated across the depletion region by the field.
- V_{ds} increases, the voltage across the inversion region saturates at pinch-off voltage, while the field in the depletion region increases.
- However, the drift velocity ($V_d= \mu E$) of the channel (e^- or h^+) does not increases with the increasing field.
- Instead, velocity saturation occurs due to inverse dependence of mobility (μ) at high electric fields (E> 10^5 v/cm)

Effects of Channel Length Modulation



- The reduction channel length in pinch-off mode.
- Increase the field across the pinch-off region of the channel.
- With the surface mobility of the channel e^- increasing with field; results slight increase in I_d in pinch-off mode

nMOS depletion type transistor

- Normally ‘ON’
- Channel formation is done by implanting a suitable impurity in the channel.
- A conducting layer is already exists. Therefore, you don’t need a gate voltage to form a channel.
- Current flow, even at V_{gs}=0V.
- To stop current floe, you apply a negative $V_{gs.}$