End-Sem: Analog Electronic Circuits (S25.EC2.103)

Max. Marks: 80 **Time: 3:00 PM-6:00 PM** **Date: 29/04/2025**

NOTE: No query allowed during the exam. Write your assumptions (if any) for each question.

Q1. A curious student like you decides to try a new circuit topology wherein the input is applied to the drain and the output is sensed at the source (**Fig.1**). Assume $\lambda \neq 0$, determine the voltage gain of the circuit and discuss the result. **[10 Marks]**

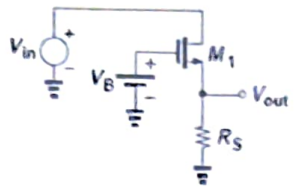


Fig.1

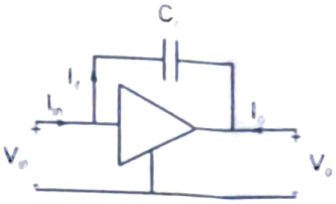


Fig.2

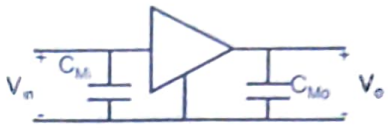


Fig.3

Q2(a). Discuss Miller theorem/effect in the context of amplifiers. How it impacts the amplifier performances? Prove that Miller effect results in an increase in the input capacitance (Just for reference; **Fig.2** and **Fig.3**). **[5 Marks]**

(b). What is open-circuit time constant approach technique? Estimate the upper 3dB cut-off frequency of the given amplifiers (in **Fig.4** and **Fig.5**) using open-circuit time constant approach. **[10 Marks]** Assume Cgsn=4fF, Cgdn=0.4fF, Cdbn= 4fF, Cgdp=0.4fF, Cdbp= 4fF. Also, take the voltage gain of amplifiers equal to -8. What we call amplifier configurations in the given circuits (Fig.4 and Fig.5)? **[Hint:** You may need to estimate the voltage gain at V_{o1} (Fig.5). Gain at this node will suffer from Miller effect. Just need to show gain at V_{o1} is ≤1]

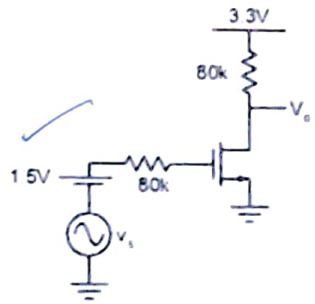


Fig.4

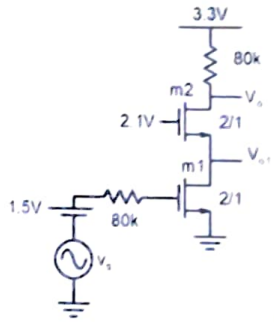


Fig.5

Q 3(a). Consider the circuit shown in **Fig.6**. Calculate the maximum transconductance that M_1 can provide (without going into the triode region). Consider V_{TH}= 0.4 V for NMOS. **[5 Marks]**

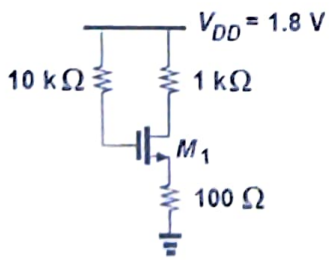


Fig.6

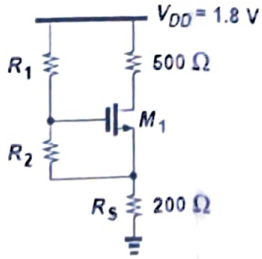


Fig.7

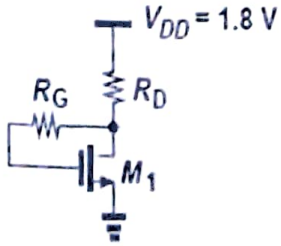


Fig.8

$g_m = \frac{2I_{DS}}{V_{GS} - V_{TH}}$

$= \frac{2I_{DS}}{1.4 - 100I_{DS}}$

$g_m = \frac{2I_{DS}}{V_{DSAT}} = \frac{2\left(\frac{1}{2} K_n (V_{DSAT})^2\right)}{V_{DSAT}}$

$g_m = K_n V_{DSAT}$ $g_m = K_n (V_{GS} - V_{TH})$

(b). Consider the circuit depicted in **Fig.7**, where $W/L = 20/0.18$. Assuming the current flowing through R_2 is one-tenth of ID_1, calculate the values of R_1 and R_2 so that $I_{D1} = 0.5$ mA. Consider $V_{TH} = 0.4V$, $\mu_n C_{ox} = 200\ \mu A/V^2$ for NMOS. **[5 Marks]**

(c). The self-biased stage of **Fig.8** must be designed for a drain current of 1 mA. If M_1 is to provide a transconductance of $1/(100\Omega)$, calculate the required value of R_D. Consider $V_{TH} = 0.4$ V for NMOS. **[5 Marks]**

Q4. The CS stage of **Fig. 9** must provide a voltage gain of 10 with a bias current of 0.5 mA. Assume $\lambda_1 = 0.1\ V^{-1}$, and $\lambda_2 = 0.15\ V^{-1}$. Consider $V_{TH} = 0.4V$, $\mu_n C_{ox} = 200\ \mu A/V^2$ for the NMOS; $V_{TH} = -0.4V$, $\mu_p C_{ox} = 100\ \mu A/V^2$ for the PMOS. [Hint: $r_o = 1/\lambda I_D$] **[2.5+2.5+5+5= 15 Marks]**

(a). Compute the required value of $(W/L)_1$.

(b). if $(W/L)_2 = 20/0.18$, calculate the required value of V_b.

(c). if in the stage of Fig.9, M_2 has a long length so that $\lambda_2 << \lambda_1$. Calculate the voltage gain if $\lambda_1 = 0.1\ V^{-1}$, $(W/L)_1 = 20/0.18$, and $I_D = 1$ mA.

(d). if the circuit of Fig.9 is designed for a bias current of I_1 with certain dimensions for M_1 and M_2. If the width and the length of both transistors are doubled, how does the voltage gain change? Consider two cases: (i) the bias current remains constant, or (ii) the bias current is doubled.

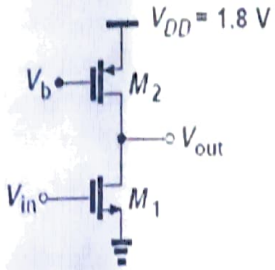


Fig.9

Q5(a). The CG stage depicted in **Fig.10** must provide an input impedance of 50 Ω and an output impedance of 500 Ω. Assume $\lambda = 0$. Consider $V_{TH} = 0.4V$, $\mu_n C_{ox} = 200\ \mu A/V^2$ for the NMOS. **[2+2+2=6Marks]**

i. What is the maximum allowable value of I_D?
ii. With the value obtained in (a), calculate the required value of W/L.
iii. Compute the voltage gain.

(b). The source follower (CD amplifier) shown in **Fig.11** is biased through R_G. Calculate the voltage gain if $W/L = 20/0.18$ and $\lambda = 0.1\ V^{-1}$. Consider $V_{TH} = 0.4V$, $\mu_n C_{ox} = 200\ \mu A/V^2$ for the NMOS. **[4 Marks]**

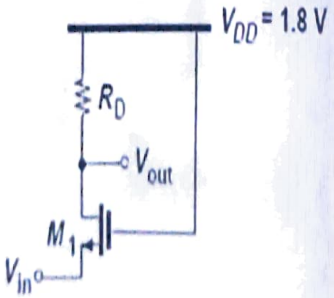


Fig.10

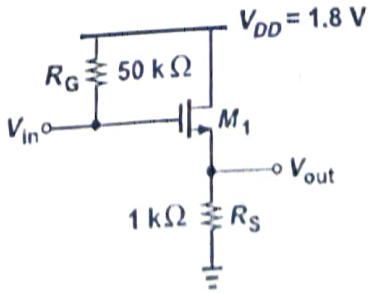


Fig.11

Q6(a). Is there any trade-off between voltage gain and output voltage swing in MOS amplifier? Explain your answer through gain and voltage swing equations. You may consider resistive load common-source amplifier for your explanations. **[5 Marks]**

(b). Compare the common-source (CS), common-gate (CG), and common-drain (CD) amplifier configurations in terms of voltage gain, input impedance, output impedance, voltage swing, and frequency response in general. **[5 Marks]**

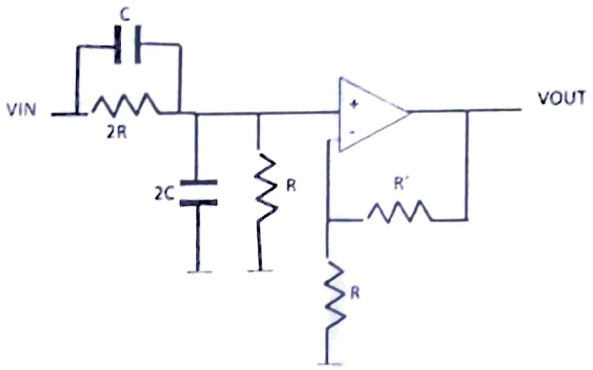
Q7. Draw a small-signal model of a common-source amplifier with **NMOS** active load, estimate voltage gain of this amplifier. Discuss the pros and cons of this amplifier. **[5 Marks]**

OR

Q7. Find the output signal if the input is

- V_{IN}=1V DC
- V_{IN}=1V AC (very high frequency)

Assume the op-amp to be ideal. R=100 Ω, C=1nF and R'=500 Ω



Note: Keep your answers to the point.

*******Best of luck*******

$$g_m = \sqrt{2 k_n I_{DSQ}} = \sqrt{2 k_n \left(\frac{1}{2} k_n\right) (V_{DSAT})^2}$$

$$= k_n V_{DSAT}$$