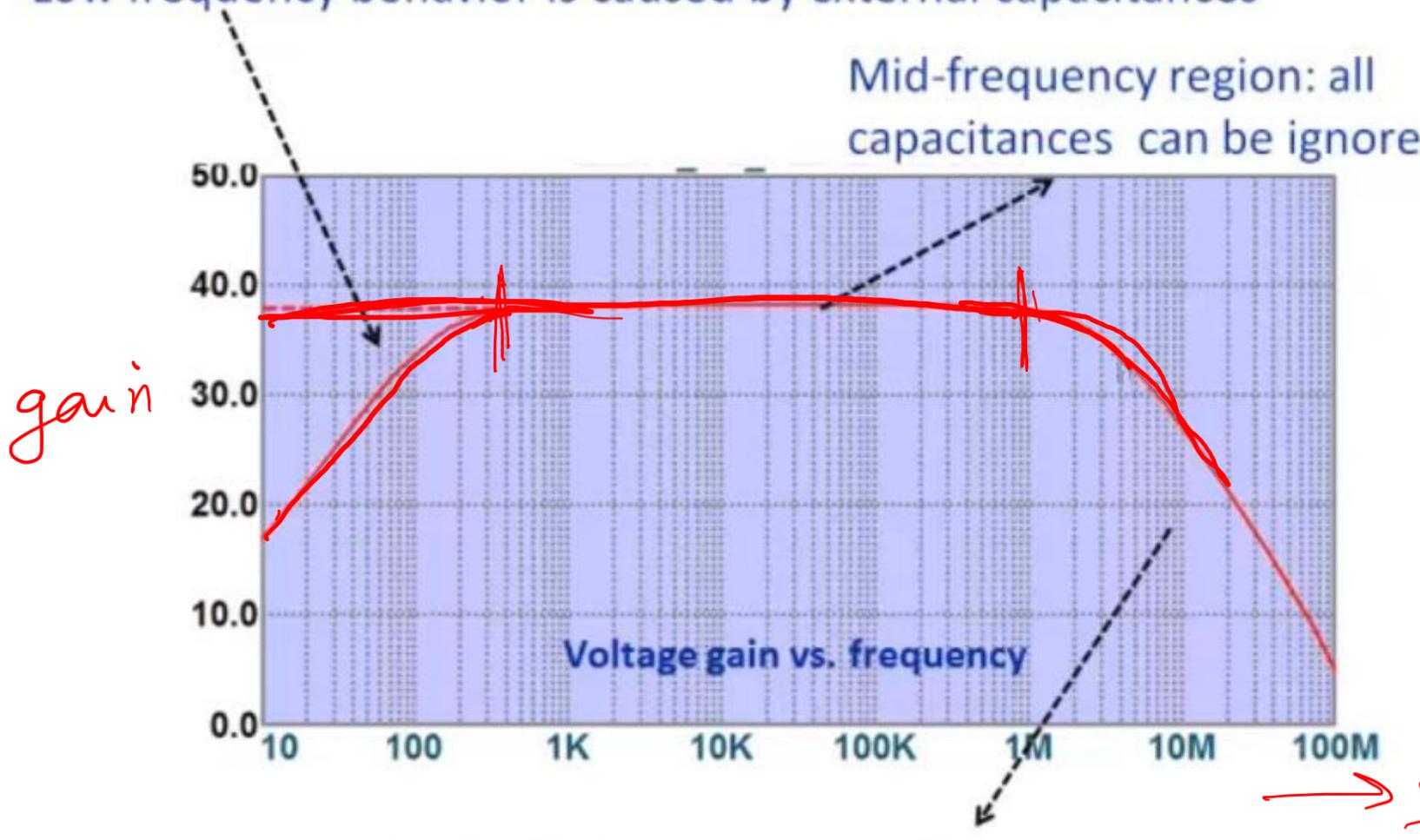


4. Frequency Response

Low frequency behavior is caused by external capacitances

Mid-frequency region: all capacitances can be ignored



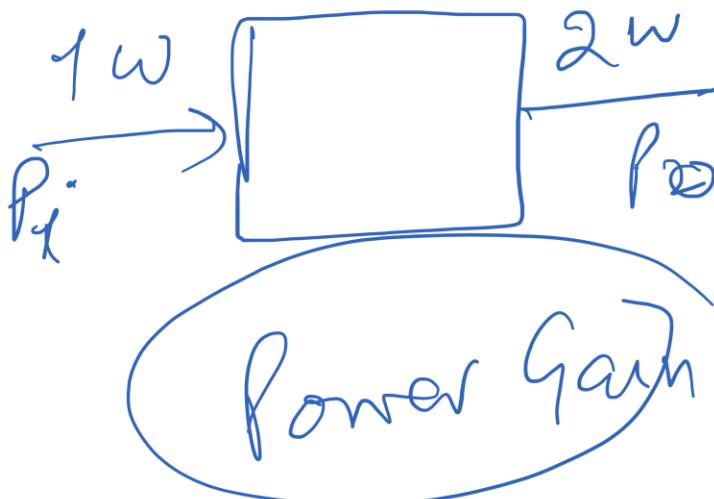
High frequency behavior is caused by internal transistor capacitances

$\text{Bel} \rightarrow$ measure ratio of two power levels

$$\text{Bel} = \log_{10} (P_1/P_2)$$

deci-Bel

$$dB = 10 \log_{10} (P_1/P_2)$$



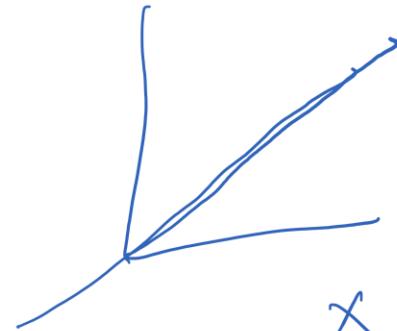
$$dB = 10 \log_{10} \left(\frac{2}{1} \right)$$

$$dB = 10 \log_{10} 2$$

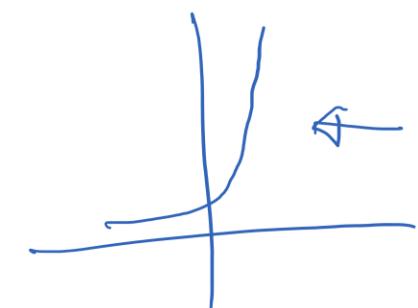
$$= 10 * 0.301$$

$$\approx \underline{\underline{3dB}}$$

$$y = x$$



$$y = 10^x$$



$$\log y = \log 10^x$$

$$\log y = x$$

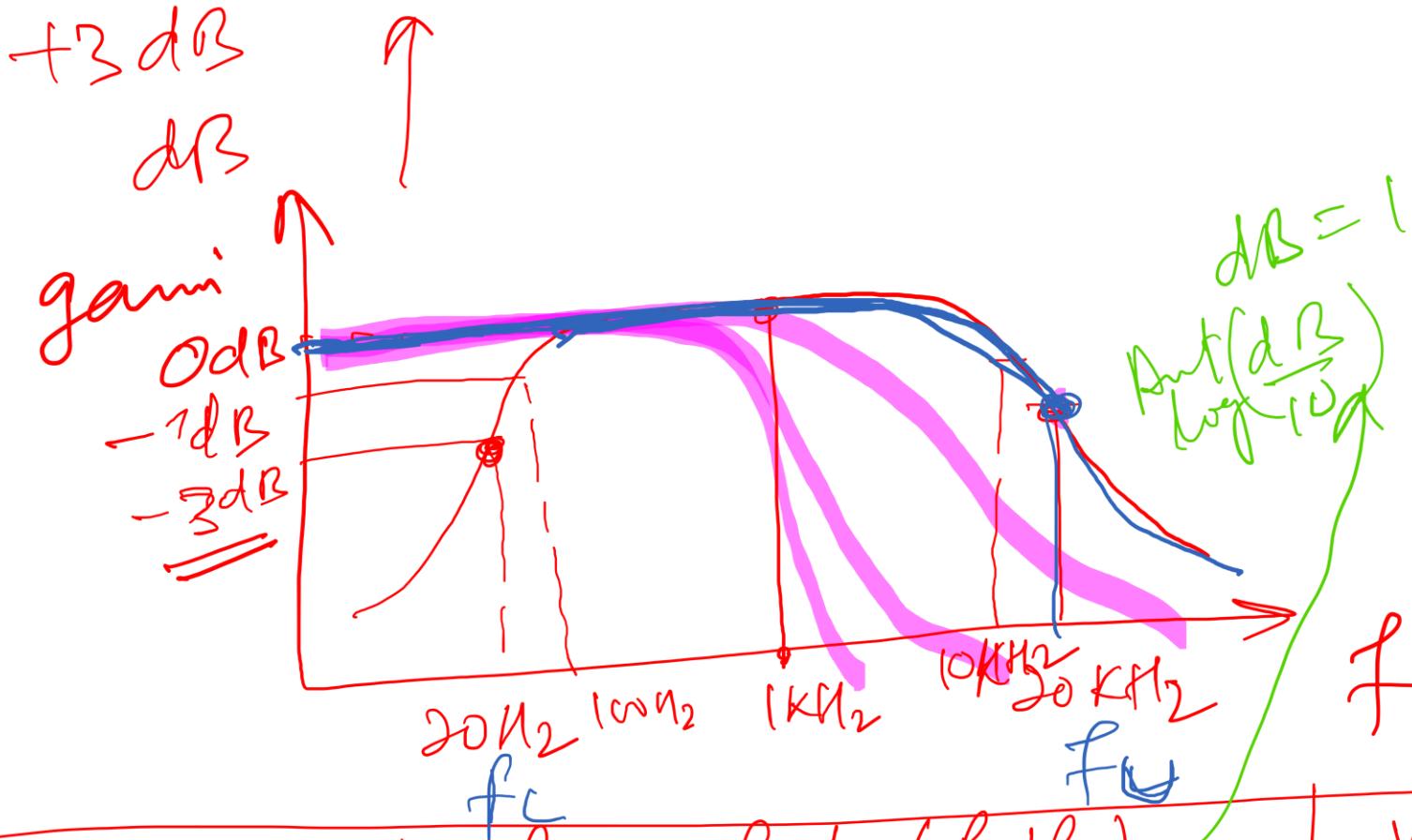
3dB \rightarrow Half power point

$$P = V \cdot I$$
$$P = \frac{V^2}{R}$$

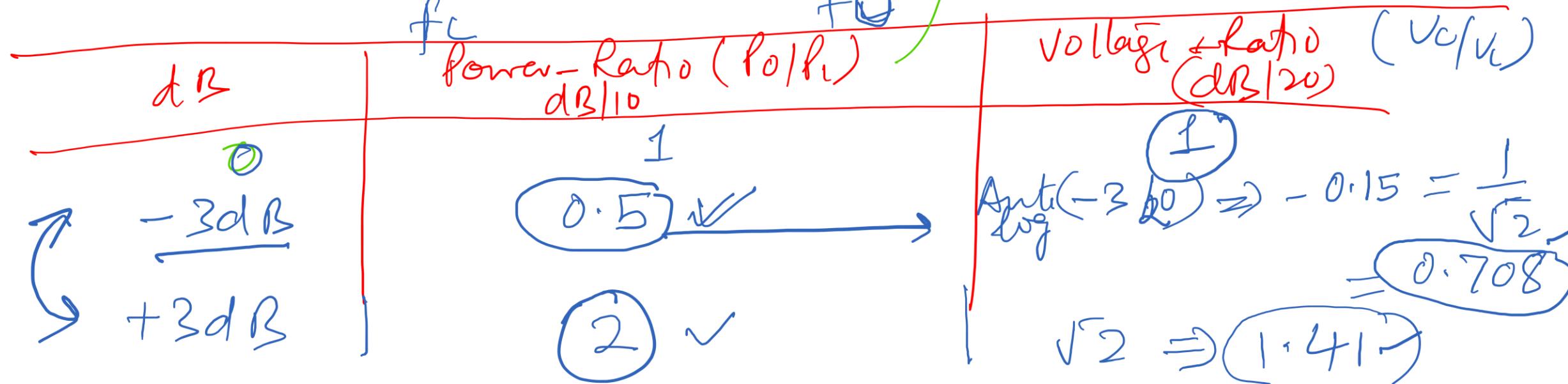
$$P_0 = \frac{V_0^2}{R}$$
$$\check{P}_i = \frac{V_i^2}{R}$$

$$\sqrt{3dB} = \cancel{10 \log_{10}} \left(\frac{V_0^2/R}{V_i^2/R} \right)$$
$$= 10 \log_{10} \left(\frac{V_0}{V_i} \right)^2$$
$$= \cancel{20} \log_{10} \left(\frac{V_0}{V_i} \right)$$

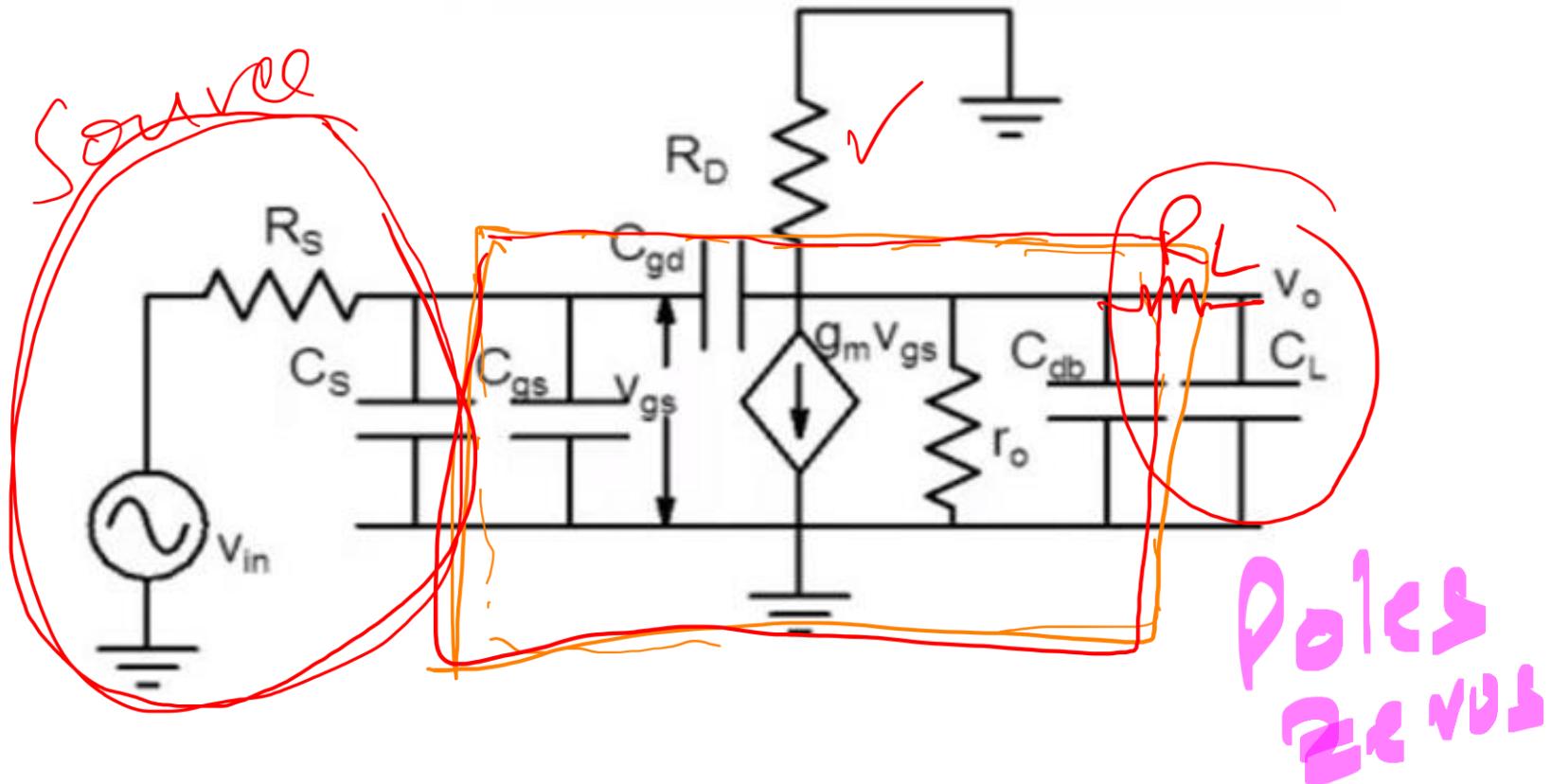
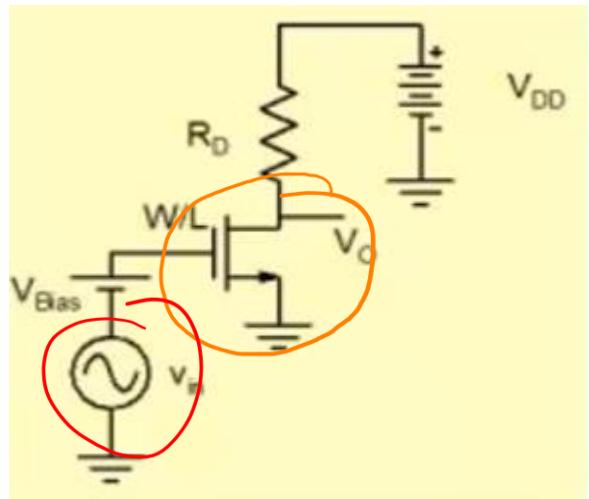
Vol log gain in dB



Audio
App.
20Hz-20kHz



3-dB Upper Cutoff Frequency



The general method for determining frequency response of an amplifier is to carry out analysis of the circuit to obtain the **transfer function** and then obtain the 3dB frequency from there

Open Circuit Time Constant Approach

- A simpler technique which gives approximate answer and is also based on dominant pole approximation is :

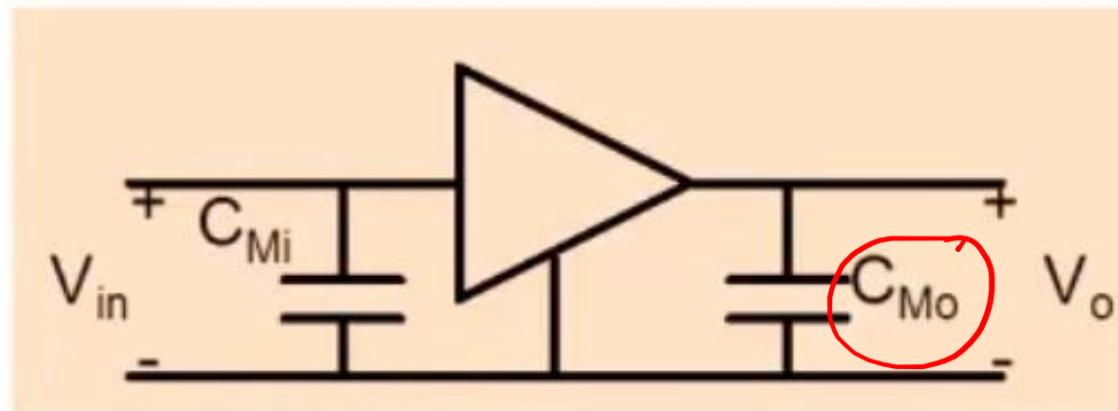
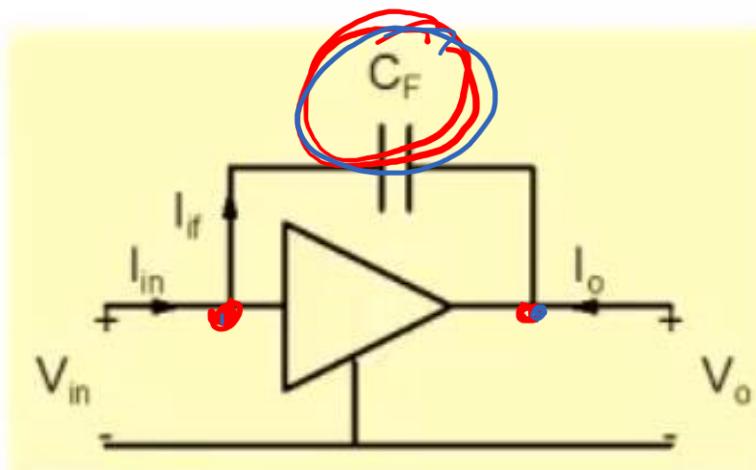
$$f_{3dB} = \frac{1}{2\pi \sum \tau_j}$$

τ_j is the time constant associated with capacitor C_j

$$\tau_j = R_j C_j$$

where R_j is the effective resistance seen by the capacitor when all other capacitors are removed from the circuit

Millers Theorem

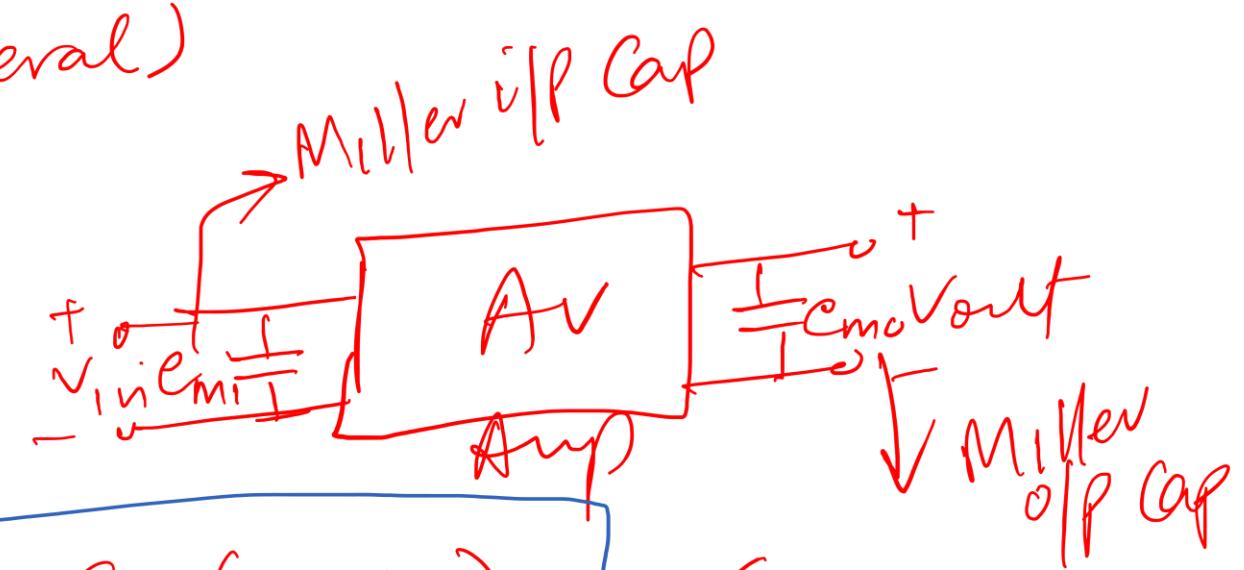
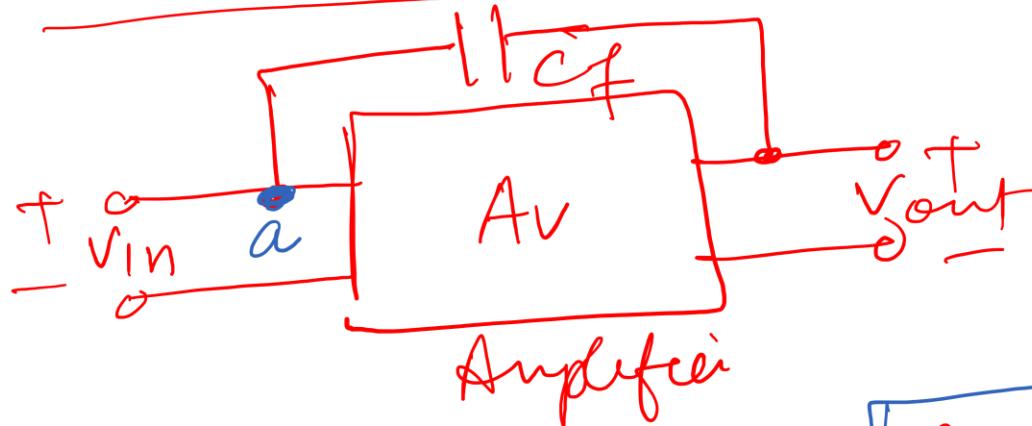


$$C_{Mi} = C_F \times (1 - A_V)$$

$$C_{Mo} = C_F \times \left(1 - \frac{1}{A_V}\right)$$

$A_V \rightarrow$ *voltage gain*

Miller Theorem (In general)



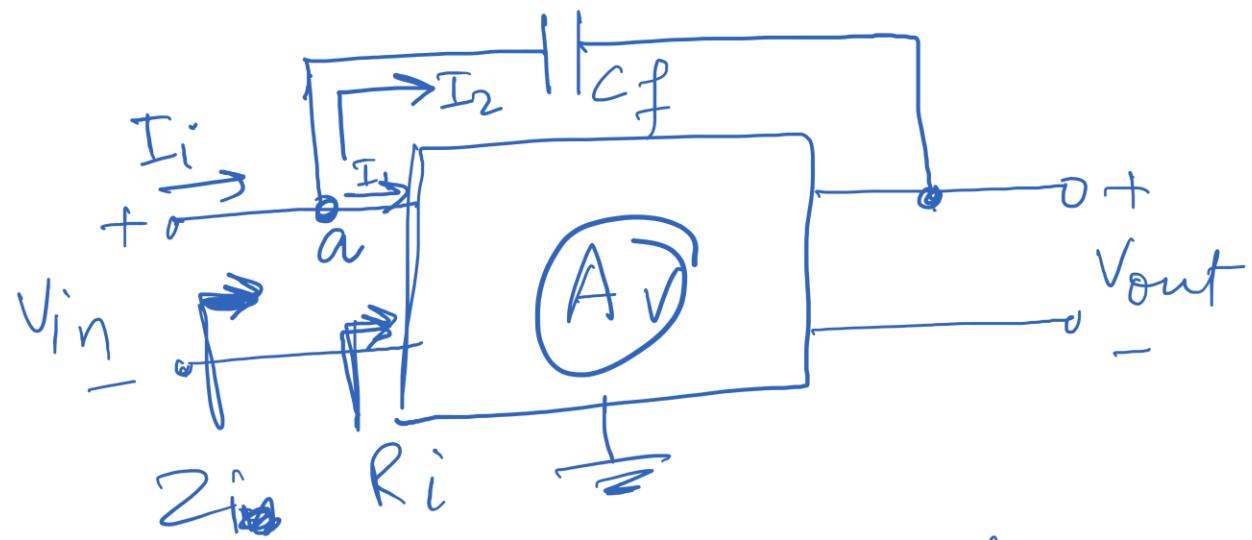
$$C_{ni} = C_f (1 - A_v) \quad \checkmark$$

$$C_{no} = C_f (1 - 1/A_v) \quad \checkmark$$

Cond¹: Amplifier should be Inverting

\downarrow
 A_v is negative

\downarrow
L/P and O/P are in 180° phase shift



→ KCL at node 'a'

$$I_i = I_1 + I_2$$

i.e.

$$\frac{V_{in}}{Z_i} = \frac{V_{in}}{R_i} + \frac{V_{in} - V_{out}}{X C_f}$$

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{X C_f}{(1 - A)}$$

$Z_i \rightarrow$ i/p impedance of entire ckt

$R_i \rightarrow$ impedance looking into Amplifier

$$V_{out} = A \cdot V_{in}$$

$$\frac{1}{Z_i} = \frac{1}{R} + \underbrace{\frac{1}{X_{Cmi}}}_{\textcircled{1}}$$

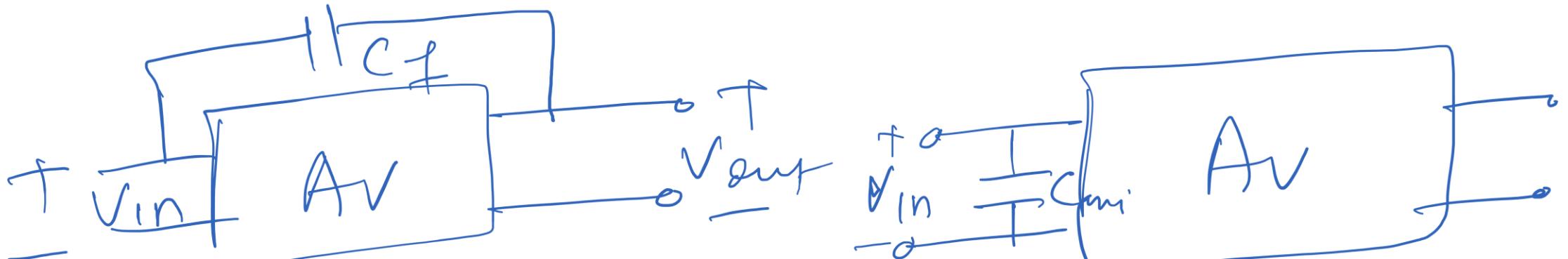
$$X_{Cmi} = \frac{X_C f}{(1 - A_V)}$$

$$X_C = \frac{1}{2\pi f C}$$

i.e

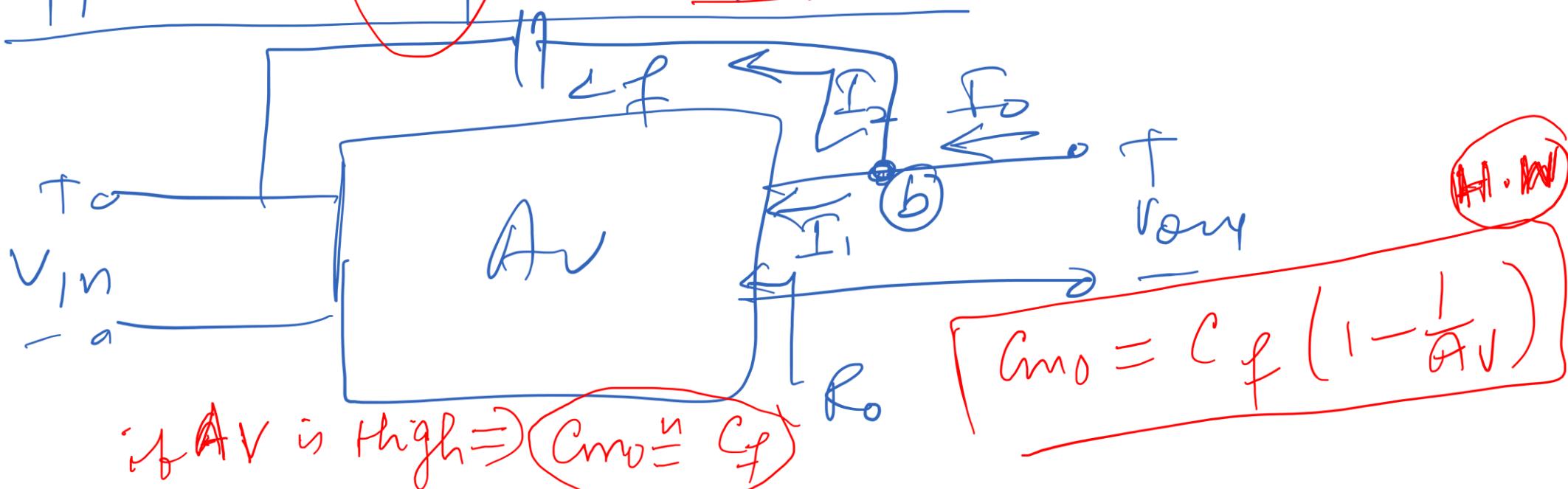
$$\frac{1}{2\pi f C_{mi}} = \frac{1}{2\pi f C_f (1 - A_V)}$$

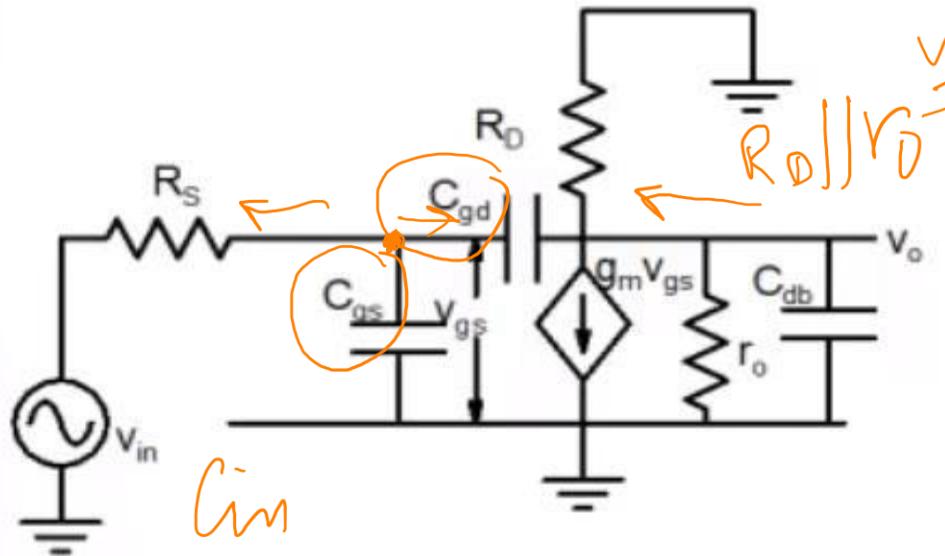
$$C_{mi} = C_f (1 - A_V) \quad \textcircled{2}$$



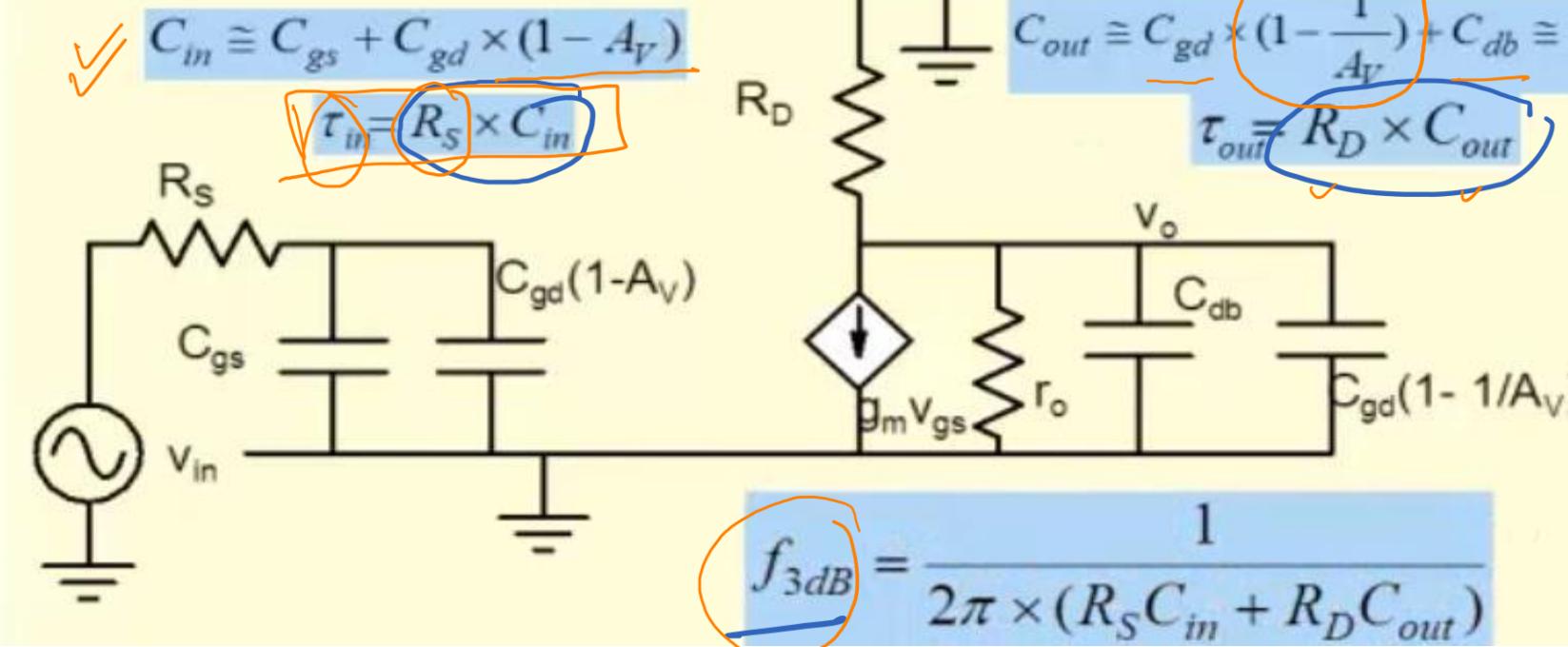
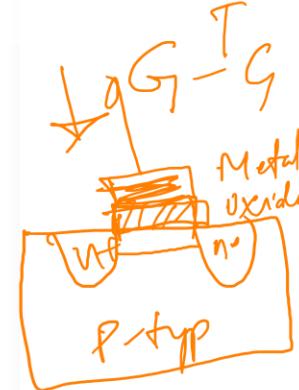
$$\checkmark C_{mi} = C_f (1 - A_V)$$

② Effect of C_f on O/P side



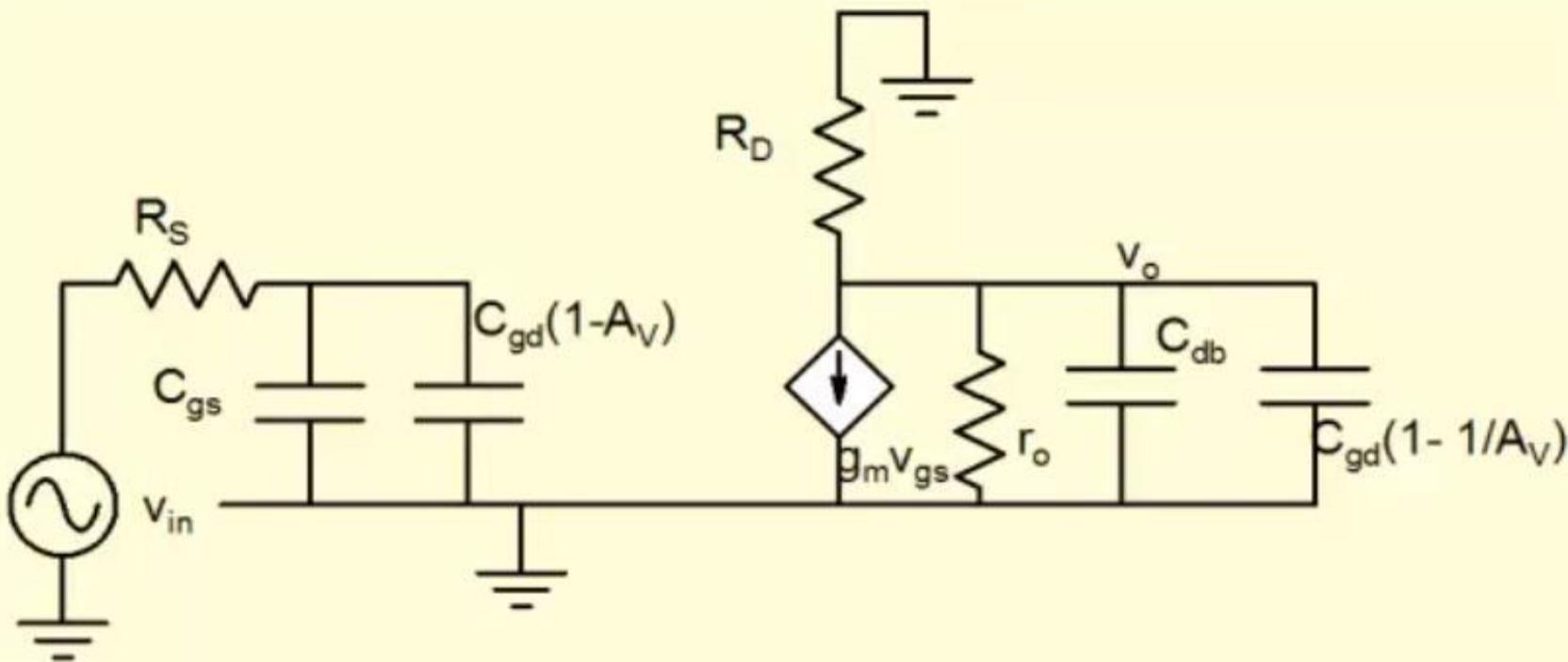


- The estimation of time constants becomes simpler through use of Miller's theorem which allows the capacitance C_{gd} to be split into two capacitances, one at the input and the other at the output.



$$f_{3dB} = \frac{1}{2\pi \times (R_s C_{in} + R_D C_{out})}$$

Key approximation in Miller's theorem



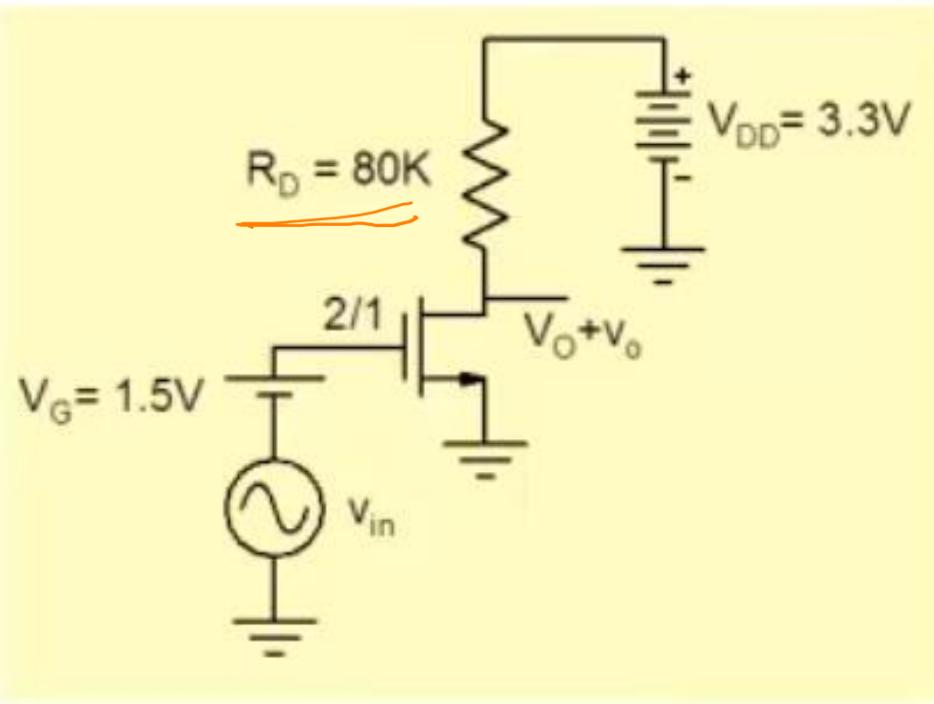
What is A_V ?

For the estimation of capacitance, normally **low frequency** value
for $A_V = -g_m R_D$ is used

~ medium

3dB Upper Cutoff Frequency

(when load is resistive)



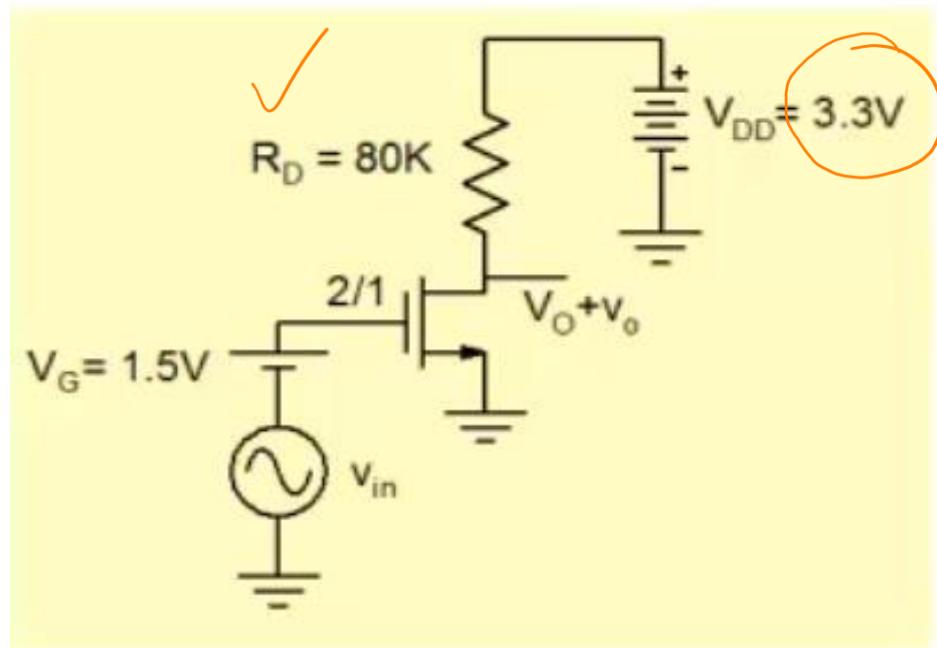
$$C_{gs} = 4 fF \quad C_{gd} = 0.4 fF$$

$$C_{db} = 4 fF$$

$$f_{3dB} = \frac{1}{2\pi} \times \frac{1}{R_S(C_{gs} + C_{gd}(1 + g_m R_D)) + R_D(C_{gd} + C_{db})}$$
$$= 0.45 GHz$$

Summary of the example

(Resistive load)



$$I_{DSQ} = 25\mu A$$

$$\underline{V_{DSQ} = 1.3V; V_{sat} = 0.5V}$$

$$A_V \approx -g_m R_D = -8$$

$$R_O \approx R_D = 80K$$

$$v_{o\max} \leq V_{DSQ} - V_{sat} = 0.8V$$

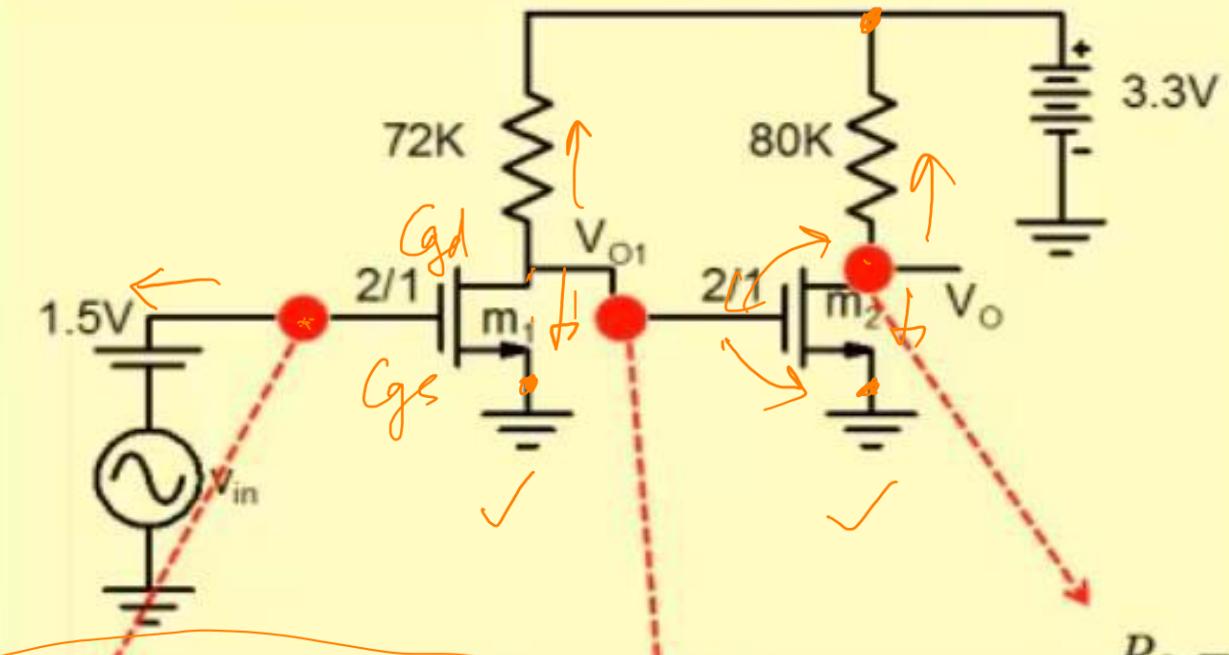
$$v_{o\max 3} \approx I_{DSQ} R_D \| R_L \times \frac{HD_2}{12.5}$$

$$= 0.8V \text{ for } HD_2 = 5\%$$

$$f_{3dB} = \frac{1}{2\pi} \times \frac{1}{R_S(C_{gs} + C_{gd}(1 + g_m R_D)) + R_D(C_{gd} + C_{db})}$$

$$= 0.45GHz$$

Another Example



$$f_{3dB} = \frac{1}{2\pi \sum \tau_j}$$

$$\tau_j = R_j C_j$$

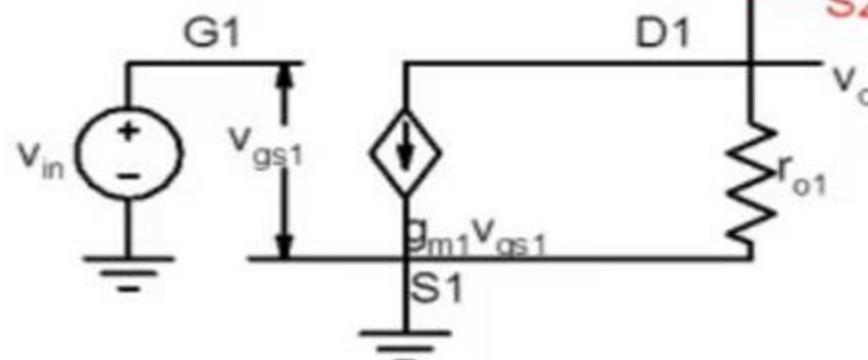
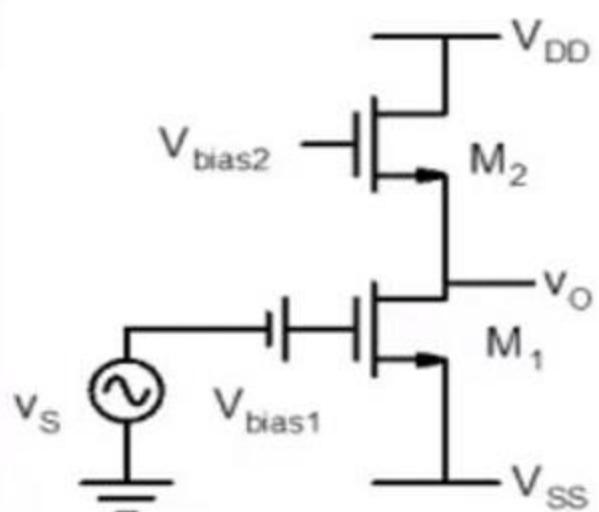
$$R_3 = 80k$$

$$C_3 = C_{db2} + C_{gd2} \times \left(1 - \frac{1}{A_{V2}}\right)$$

$$C_2 = C_{gs2} + C_{gd2} \times (1 - A_{V2}) + C_{db1} + C_{gd1} \times \left(1 - \frac{1}{A_{V1}}\right)$$

CS amplifier with Active Load

CS Amplifier with Active Load (NMOS)

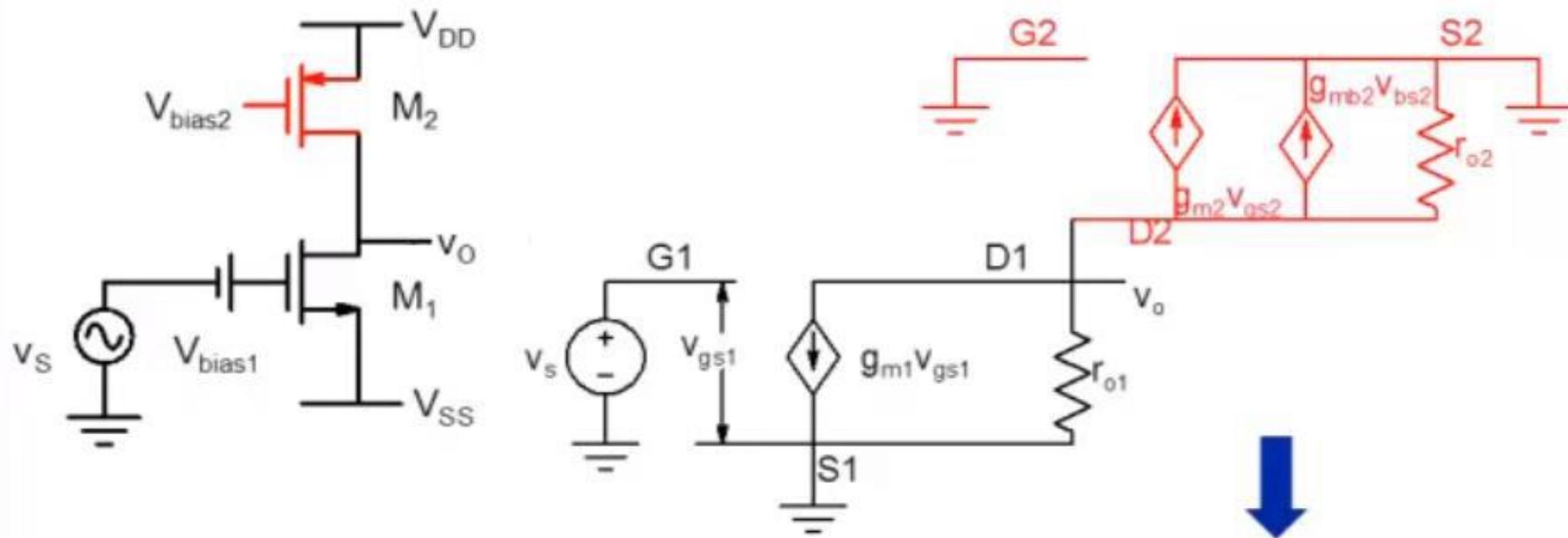


$$v_o = -g_{m1} v_{in} \times \{ r_{o1} \parallel r_{o2} \parallel \frac{1}{g_{m2}(1+\eta)} \}$$

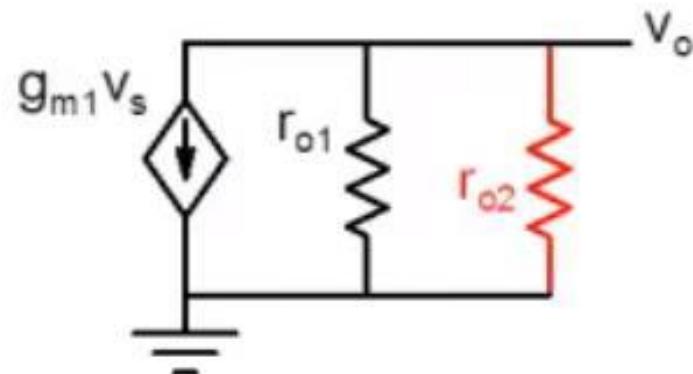
$$A_V \cong - \frac{g_{m1}}{g_{m2}(1+\eta)}$$

$$= \frac{\sqrt{2KP \times (W/L)_1 \times I_{DSQ1}}}{\sqrt{2KP \times (W/L)_2 \times I_{DSQ1}}} \times \frac{1}{1+\eta} = \sqrt{\frac{(W/L)_1}{(W/L)_2}} \times \frac{1}{1+\eta}$$

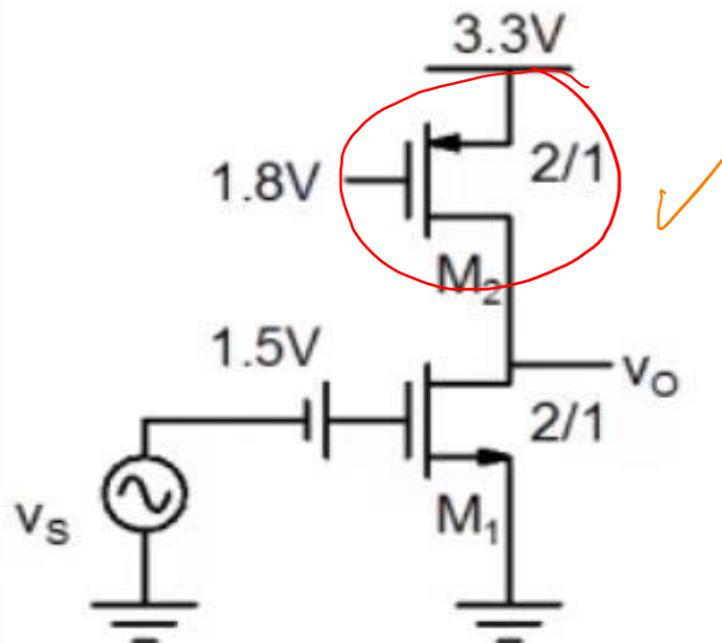
CS Amplifier with PMOS active load



$$A_V = -g_{m1} \times r_{o1} \parallel r_{o2}$$



Example



$$I_{DSQ} = 25 \mu A; V_{DSQ} = 1.65(?)$$

$$g_{mn} = g_{mp} = 100 \mu A/V; r_{on} = r_{op} = 4 M\Omega$$

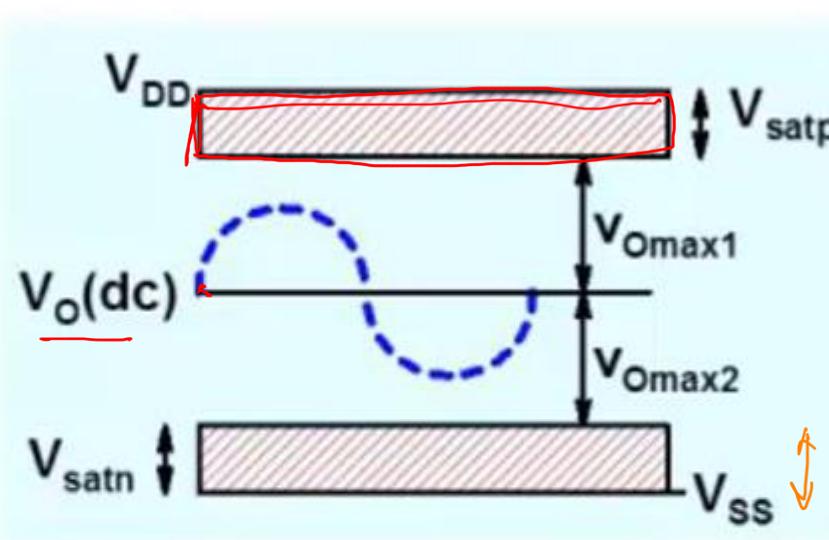
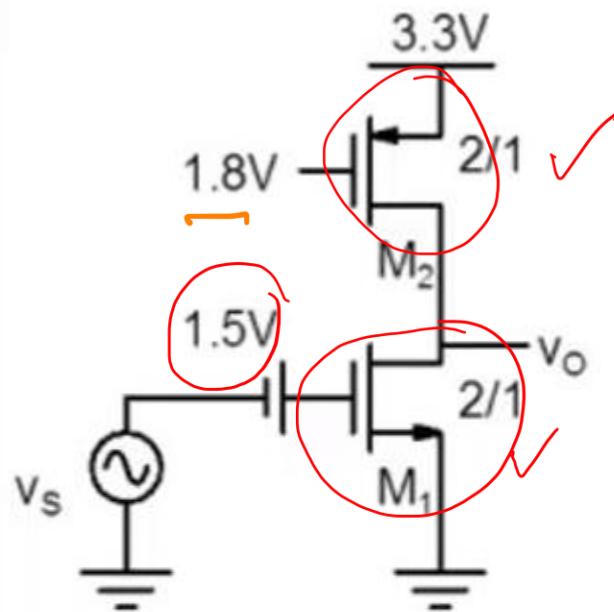
$$\boxed{|A_V| = g_{mn} \times r_{on} \parallel r_{op}}$$

$= -200$

$$\boxed{R_o = r_{on} \parallel r_{op} = 2 M\Omega}$$

Large gain is easily obtained without requiring large resistors which are difficult to fabricate

Output Voltage Swing



$$I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

$$(V_{GS} - V_T) = \sqrt{\frac{I_D}{R(W/L)}}$$

$$v_{o\max 1} = V_{DD} - V_O(dc) - V_{satp}$$

$$v_{o\max 2} = V_O(dc) - V_{ss} - V_{satn}$$

$$v_{o\max 3} \approx I_{DSQ} [r_{op} \parallel r_{on}] \times \frac{H D_2}{12.5}$$

$$3.3 - 1.65 - 0.5 = 1.15V$$

$$V_{sat} = \sqrt{V_{GS} - V_{TN}} = 1.5 - 1 = 0.5$$

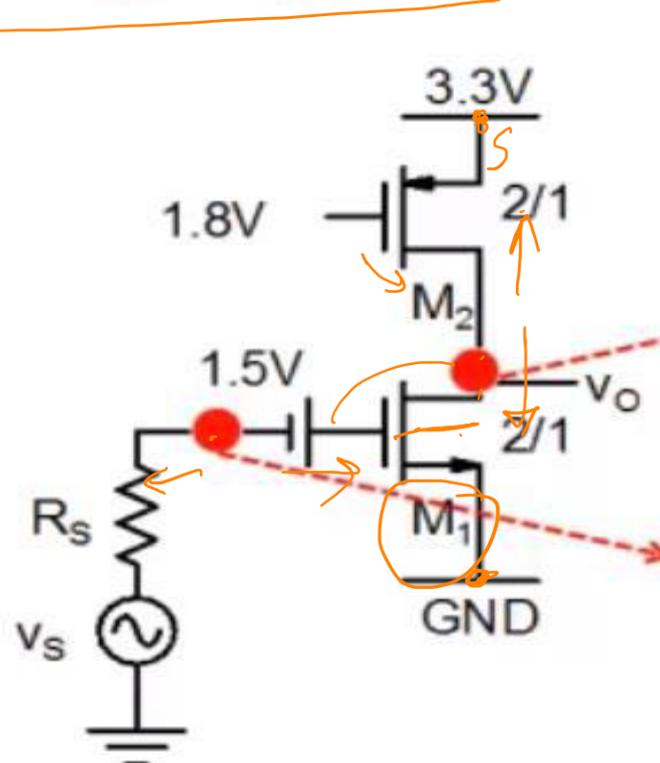
$$V_{ASD} \downarrow T_P$$

How to reduce this?

✓ Harmonic distortion is less of a problem here

Frequency Response

Time Contt
approach



$$f_{3dB} = \frac{1}{2\pi \sum \tau_j} \quad \tau_j = R_j C_j$$

$$R_2 = r_{on} \| r_{op} = 2M\Omega$$

$$C_2 = C_{dbn} + C_{gdn} \times \left(1 - \frac{1}{A_V}\right) + C_{gdp} + C_{dbp}$$

$$R_1 = R_S$$

$$C_1 = C_{gsn} + C_{gdn} \times \left(1 - A_V\right)$$

$$C_{gsn} = 4.0 fF \quad C_{gdn} = 0.4 fF \quad C_{dbn} = 4 fF$$

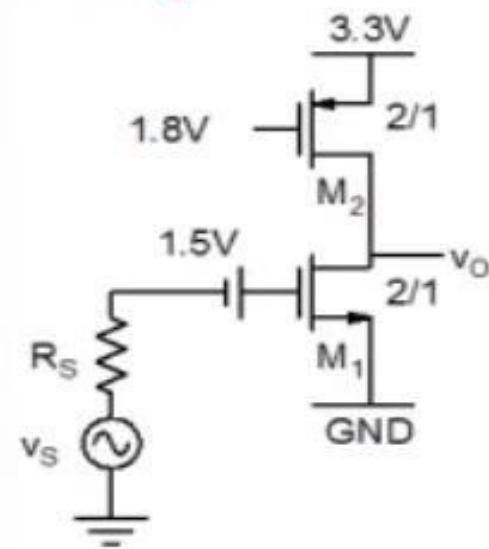
$$C_{gdp} = 0.4 fF \quad C_{dbp} = 4 fF$$

$$C_1 = 84.4 fF; C_2 = 8.8 fF$$

$$f_{3dB} = \frac{1}{2\pi \sum \tau_j} = 9 MHz \text{ for } R_s = 0$$

$$= 1.56 MHz \text{ for } R_s = 1 M\Omega$$

Analysis: Summary



$$I_{DSQ} = 25\mu A$$

$$V_O(dc) = 1.65V$$

$$|A_V| = -200 \quad R_O = 2M\Omega$$

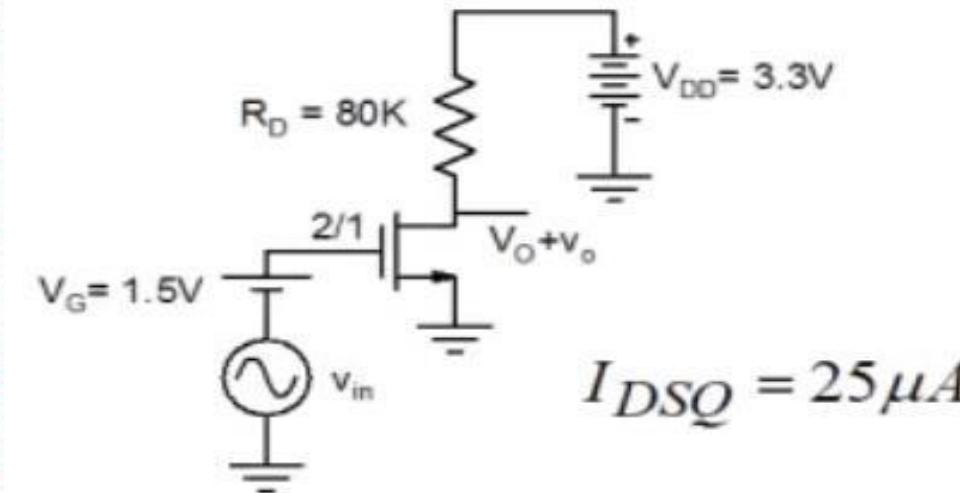
$$v_{o\max 1} = 1.15V$$

$$v_{o\max 2} = 1.15V$$

$$v_{o\max 3} \cong 20V \text{ for } HD_2 = 5\%$$

$$f_{3dB} = 9MHz \text{ for } R_s = 0$$

$$= 1.56MHz \text{ for } R_s = 1M\Omega$$



$$I_{DSQ} = 25\mu A$$

$$V_{DSQ} = 1.3V; V_{sat} = 0.5V$$

$$A_V \cong -g_m R_D = -8 \quad R_O \cong R_D = 80K$$

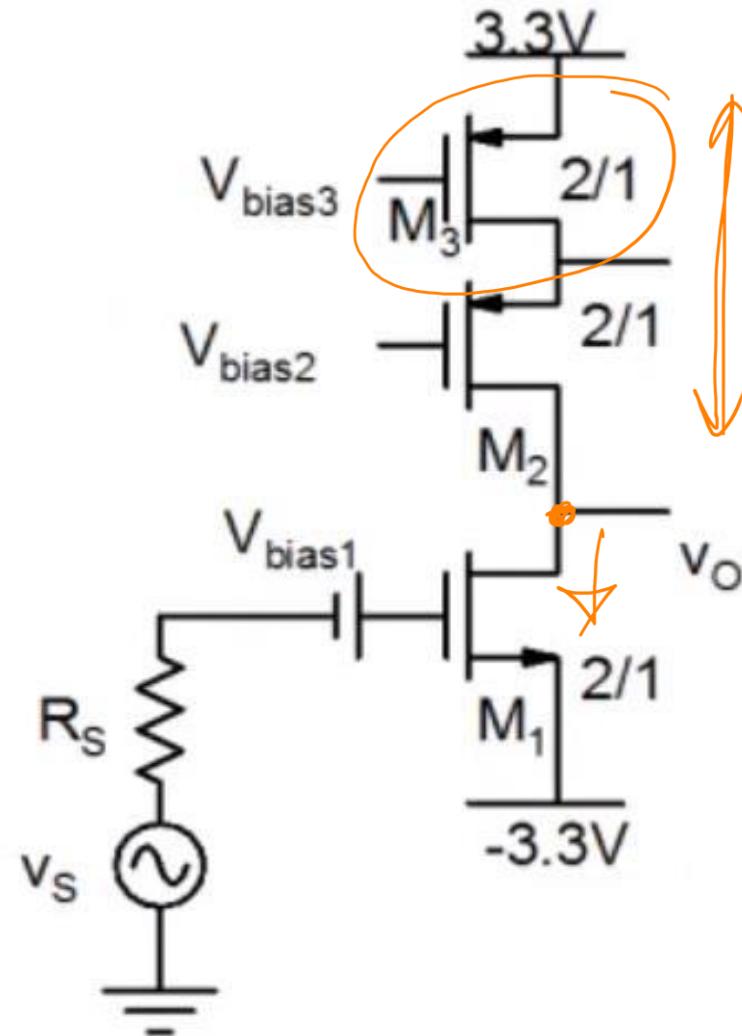
$$v_{om1} \leq 0.8V$$

$$v_{o\max 3} \cong I_{DSQ} R_D \| R_L \times \frac{HD_2}{12.5}$$

$$= 0.8V \text{ for } HD_2 = 5\%$$

$$f_{3dB} = 0.45GHz \text{ for } R_S = 0$$

Higher Voltage gain can be obtained by stacking transistors vertically.



g_m is fixed

Drawback:

- As you increase the resistance, $f_{3dB} \downarrow$
- The additional MOS will also add cap.
- O/P swing ↓