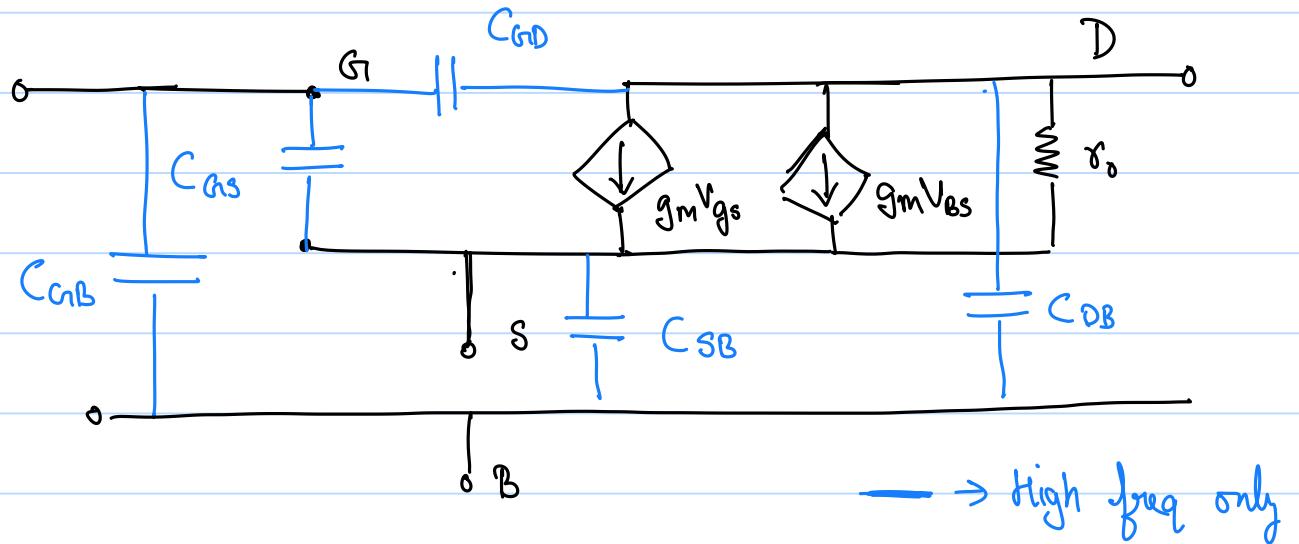
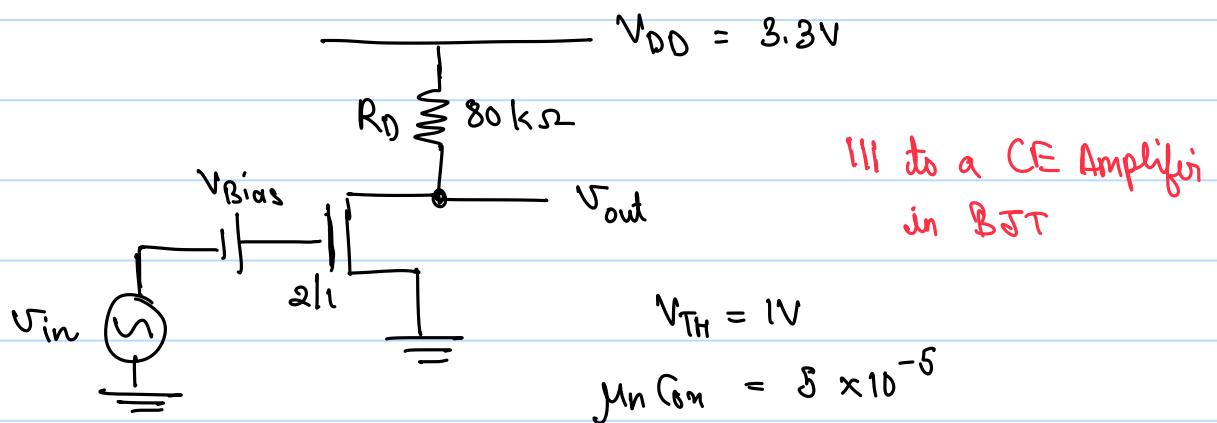


MOSFET Amplifiers

→ Small Signal Model Of NMOS in Saturation :-



→ Common Source Amplifier w/ Resistive Load :-

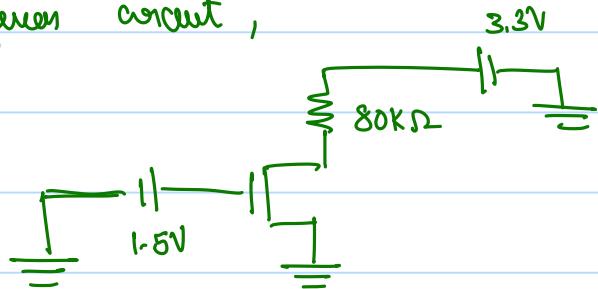


1) Bias Point Analysis :-

1. Derive DC Model of the circuit.
2. Assume Saturation and calculate I_{DSQ} , V_{DSQ}
3. Verify assumption
4. Calculate g_m , r_o .

In the given circuit,

DC :



$$\begin{aligned}
 I_{DSQ} &= \frac{1}{2} \mu_n C_o \frac{W}{L} (V_{GS} - V_{TH})^2 \\
 &= \frac{1}{2} \times 5 \times 10^{-5} \times \frac{2}{1} \times (1.5 - 1)^2 \\
 &= 5 \times 10^{-5} \times 0.5 \\
 &= 25 \mu\text{A}
 \end{aligned}$$

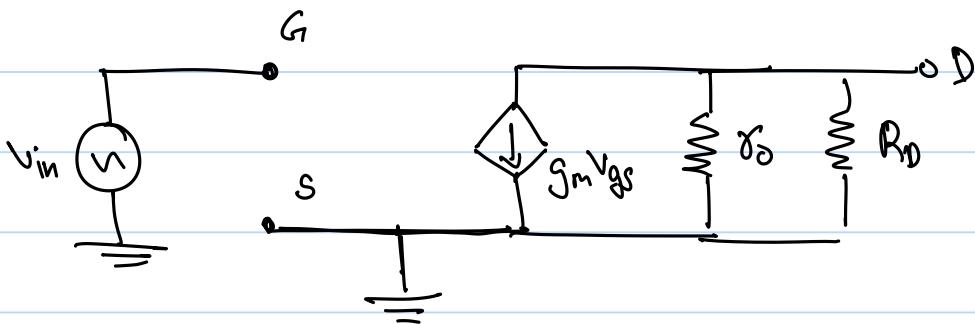
$$\begin{aligned}
 V_{DSQ} &= 3.3 - (80 \times 10^3) (25 \times 10^{-6}) \\
 &= 3.3 - 80 \times 25 \times 10^{-3} \\
 &= 3.3 - 2 = 1.3 \text{V}
 \end{aligned}$$

$$V_{DSAT} = V_{GS} - V_{TH} = 1.5 - 1 = 0.5 \text{V} < V_{DSQ}$$

\Rightarrow MOSFET is in Saturation.

$$g_m = \frac{2I_{DSQ}}{V_{DSAT}} = \frac{50 \times 10^{-6}}{0.5} = \frac{10^{-5}}{10^{-1}} = 10^{-4} \text{ S}$$

- Since I_{DSQ} is smaller in MOSFETs, than the equivalent in BJTs, the value of g_m is smaller in MOSFETs.
- Using the small signal model, we get the gain of the amplifier to be,



$$V_{out} = -g_m v_{gs} (r_o \parallel R_D)$$

$$\Rightarrow A_v = -g_m (r_o \parallel R_D)$$

Due to small g_m , the value of A_v is also small in this configuration.

$$\text{Output impedance} = R_D \parallel r_o \approx R_D$$

Output Voltage Swing :-

There are 2 conditions on V_{out} :

- 1) $V_{out} + V_{DSQ} < V_{DD}$ External Power Source Limitation
- 2) $V_{out} + V_{DSQ} > V_{DSAT}$ Saturation Region

- Due to these conditions, the maximum amplitude of the output signal will be $\min \{ V_{DSQ} - V_{DSAT}, V_{DD} - V_{DSQ} \}$

- Beyond this limit, we will observe clipping at the output.

- Effect of Harmonic Distortion :-

- Harmonic distortion is due to the non-linear relation between I_{DSQ} and V_{GS} . (is Quadratic)

$$I_{DSQ} + i_{ds} = \frac{\beta}{2} (V_{DSQ} + V_{GS} - V_{TH})^2$$

$$\Rightarrow i_{ds} = g_m V_{GS} + \left(\frac{1}{2V_{DSAT}} \right) g_m V_{GS}^2$$

- In our small signal model, we assume V_{GS} is small, so,

$$i_{ds} \asymp g_m V_{GS}$$

- But when approaching higher values, the square term comes into picture, causing Harmonic Distortion

- Taking $V_{GS} = a_0 \sin(2\pi f_0 t)$

$$i_{ds} = g_m a_0 \sin(2\pi f_0 t) + \frac{1}{2V_{DSAT}} g_m a_0^2 \sin^2(2\pi f_0 t)$$

$$= i_{ds} = g_m a_0 \sin(2\pi f_0 t) + \frac{1}{2V_{DSAT}} g_m a_0^2 \left(\frac{1 - \cos 2(2\pi f_0 t)}{2} \right)$$

$$= i_{ds} = g_m a_0 \sin(2\pi f_0 t) + \underbrace{\frac{g_m a_0^2}{4V_{DSAT}}}_{DC \text{ Comp}} - \underbrace{\frac{g_m a_0^2}{4V_{DSAT}} \cos 4\pi f_0 t}_{2nd \text{ Harmonic}}$$

So, we only get 1 additional harmonic and a DC Component in our output.

$$HD_2 = \frac{a_0}{4V_{DSAT}}$$

Change in Amplitude due to 2nd harmonic

$$\Rightarrow HD_2 = \frac{v_{in}}{4V_{DSAT}} \quad (\text{At max } v_{in})$$

$$\Rightarrow v_m = 4 HD_2 V_{DSAT}$$

$$v_o = A_v \times v_{in} \approx g_m r_o \| (R_L \times v_{in}) = \frac{2I_{DQ}}{V_{DSAT}} r_o \| R_L v_{in}$$

$$\Rightarrow v_o = \frac{2I_{DQ}}{V_{DSAT}} r_o \| R_L 4 HD_2 V_{DSAT}$$

$$\Rightarrow v_o = 8 I_{DQ} r_o \| R_L HD_2$$

Usually HD_2 is represented by a percentage

$$\Rightarrow v_o = \frac{I_{DQ} r_o \| R_L HD_2}{12.5} \rightarrow \text{Output } v_o \text{ at max } v_{in}.$$

This is the 3rd limit on the output voltage swing.

$$\therefore \text{Voltage swing} = \min \left\{ v_{DD} - v_{DQ}, v_{DQ} - v_{DSAT}, \frac{I_{DQ} \cdot r_o \| R_L HD_2}{12.5} \right\}$$

$v_{\text{max}1}$ $v_{\text{max}2}$ $v_{\text{max}3}$

But, between V_{oman1} and V_{oman3}

$$V_{oman1} = V_{DD} - V_{DSQ}$$

$$= V_{DD} - R_L I_{DSQ}$$

$$V_{oman3} = \frac{I_{DSQ} (\gamma_0 \parallel R_L) H_2}{12.5}$$

$$\approx \frac{I_{DSQ} R_L H_2}{12.5}$$

Since $\frac{H_2}{12.5} < 1$

$$\Rightarrow V_{oman3} < I_{DSQ} R_L$$

$$\Rightarrow V_{oman3} < V_{oman1}$$

$$\Rightarrow \text{Voltage swing} = \min \{ V_{oman2}, V_{oman3} \}$$

In BJT, harmonic distortion is higher, due to an exponential relation instead of quadratic in MOSFET

- Comparing V_{oman2} and V_{oman3} ,

$$V_{oman2} = V_{DSQ} - V_{DSAT}$$

$$V_{oman3} = I_{DSQ} R_L \parallel \gamma_0 H_2 / 12.5 \approx I_{DSQ} R_L H_2 / 12.5$$

If we increase V_{oman2} by increasing V_{DSQ} , the value of $I_{DSQ} R_L$ drops (by KVL).

Therefore, the optimal value for the bias voltage is when V_{DSQ} is such that $V_{OMA2} = V_{OMA3}$.

- Voltage Gain:

- The gain of our Amplifier currently is $A_V = -g_m R_D$. ($r_o \gg R_D$)

$$g_m = \sqrt{2 I_{DSQ} \beta}, \quad R_D = \frac{V_{DD} - V_{DSQ}}{I_{DSQ}}$$

$$\Rightarrow A_V = \frac{\sqrt{2\beta}}{I_{DSQ}} (V_{DD} - V_{DSQ})$$

- To increase gain,

1) Decrease $I_{DSQ} \Rightarrow$ Decrease Bias voltage / Increase R_D

2) Increase $\beta = k_p \frac{W}{L}$. w/L is under the control of the designer.

- If we need a output voltage less than V_{OM}

$$V_{OM} \leq V_{DSQ} - V_{DSAT}$$

$$V_{DSQ} \geq V_{OM} + V_{DSAT}$$

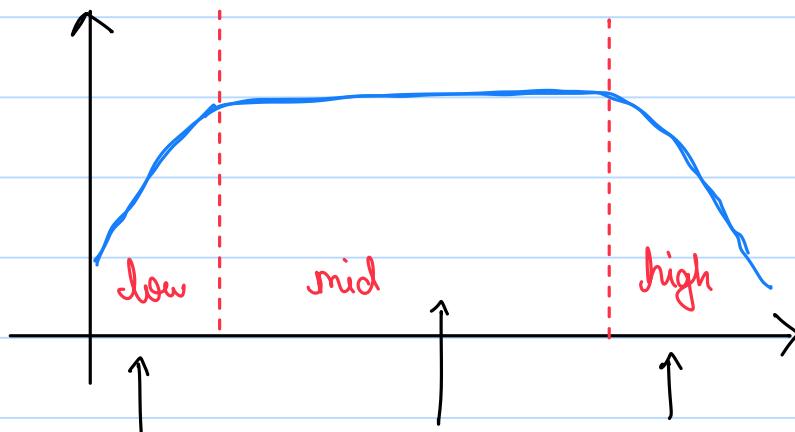
$$\Rightarrow A_V \leq \frac{\sqrt{2\beta}}{I_{DSQ}} (V_{DD} - V_{OM} - V_{DSAT}) \rightarrow \text{Larger } V_{OM} \text{ decreases gain}$$

- In ①, an increase in R_D will increase gain. Decrease in bias also improves gain, until reaching threshold voltage.
- In ② a large W/L gives us better gain.

Both these conclusions are problematic in practice due to the resulting large errors.

To solve this we will use another MOSFET as the load.
(Active load).

- Frequency Response :-

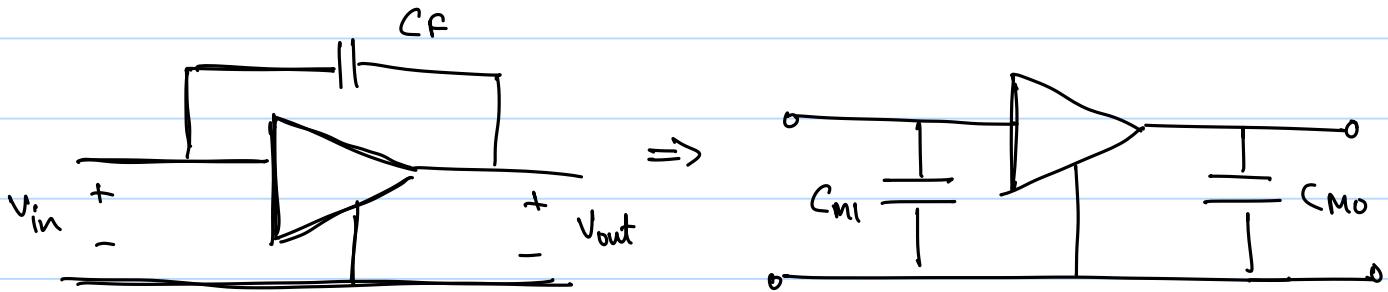


Due to external All Caps. Due to Parasitic Capacitance ignored. Capacitance

- 3dB Cutoff Frequency :-

The high frequency at which the gain of the amplifier decreases to $\sqrt{2}$.

- Miller's Theorem:

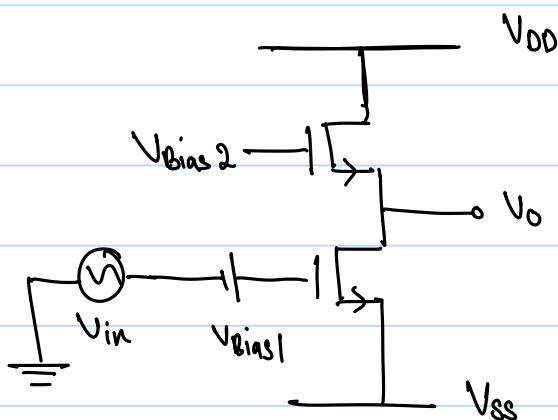


- Capacitance between the input and output terminals of an Amplifier, has an increased effect due to the Amplification of the voltage.

$$C_{M1} = C_F (1 - A_v)$$

$$C_{M2} = C_F (1 - 1/A_v)$$

→ CS Amplifier w/ Active Load :-

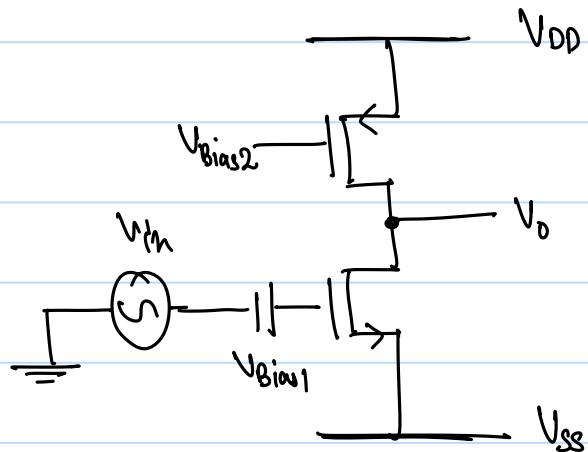


Is not analogous in BJT.

$$\circ \quad A_v = - \frac{g_m 1}{g_m 2 (1+n)} \approx \sqrt{\frac{\omega_1 / L_1}{\omega_2 / L_2}} \times \frac{1}{1+n} \rightarrow \text{If } k_n \text{ is equal}$$

The gain of the active load amplifier is low, since it depends on the ratio of aspect ratios. However, it is very stable with temperature, output voltage, etc.

- W.k.t, impedance of a MOSFET, looking into the source, is very small (Assignment 3). Therefore the overall gain provided by the active load NMOS is small, which reduces the gain.
- Therefore we replace the NMOS with a PMOS, with the drains connected to each other.

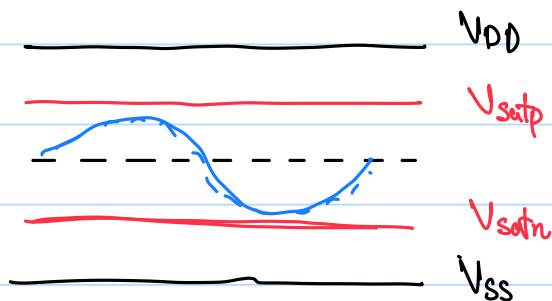


The impedance of a MOSFET looking into the drain is much higher. So we get a better gain, however losing some stability.

$$A_V = -g_m (\tau_{o1} \parallel \tau_{o2})$$

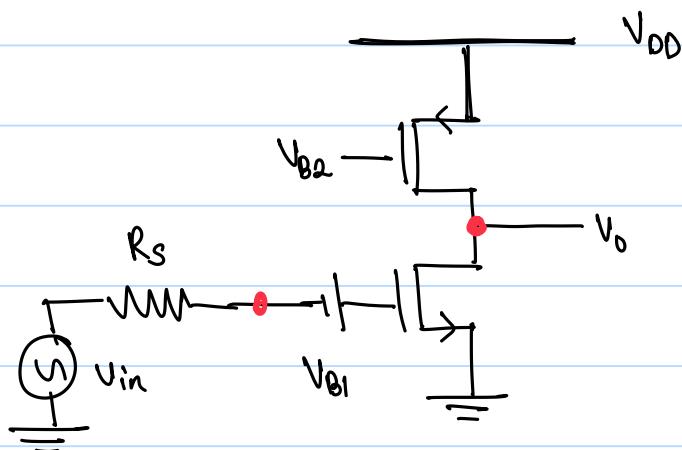
- However, this increases output resistance by a lot.

- Output Voltage swing :-



- $V_{oman1} = V_{DD} - V_{DSQ} - V_{satp}$
 - $V_{oman2} = V_{DSQ} - V_{SS} - V_{satn}$
 - $V_{oman3} = I_{DSQ} r_{on} \frac{kT_0}{12.5} \rightarrow$ since r_{on} is large, it is usually higher than V_{oman1} , V_{oman2}
 - V_{satp}, V_{satn} decrease for larger sizes of MOSFETs.
- } Same if biasing is in the middle
Harmonic Distortion is not a problem anymore.

Frequency Response:



- To calculate the 3dB cutoff frequency of each amplifier (On any amplifier network), the algorithm is,

- Identify all input and output nodes of each amplifier. (Marked above in red)
- For each node j , calculate $\tau_j = R_j C_j$ (R_j = Impedance looking in that node, C_j = Capacitance looking in that node)
- Calculate cutoff frequency using,

$$f_{3dB} = \frac{1}{2\pi \sum \tau_j}$$

In the given amplifier,

$$R_2 = r_{on} \parallel r_{op}$$

$$C_2 = C_{dbn} + C_{gdh} \left(1 - \frac{1}{A_V}\right) + C_{gdp} + C_{dbp}$$

$$R_1 = R_s$$

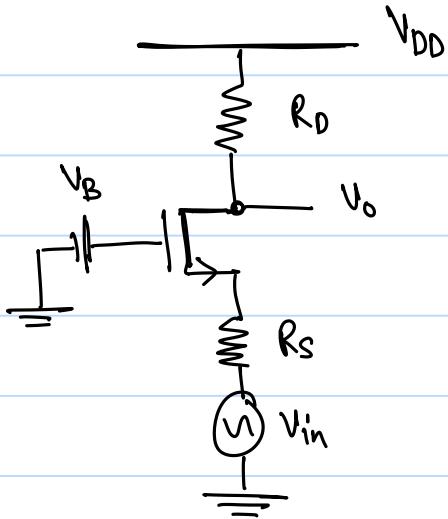
$$C_1 = C_{gsn} + C_{gdh}(1 - A_V)$$

↑
↓
Miller Effect

- Ideally, the 3dB frequency is much smaller in active load than resistive load, mainly due to Miller effect.
- Our gain can be increased by adding more PMOS's. This however increases our output resistance, decreases our 3dB frequency and also limits our voltage swing.

→ Common Gate Amplifier :-

- A major disadvantage in a CS amplifier is the Miller effect.
- In our high frequency model, we see that there is no direct capacitance between the source and drain.
- Therefore, a common gate amplifier will be much more resistant to Miller's effect.



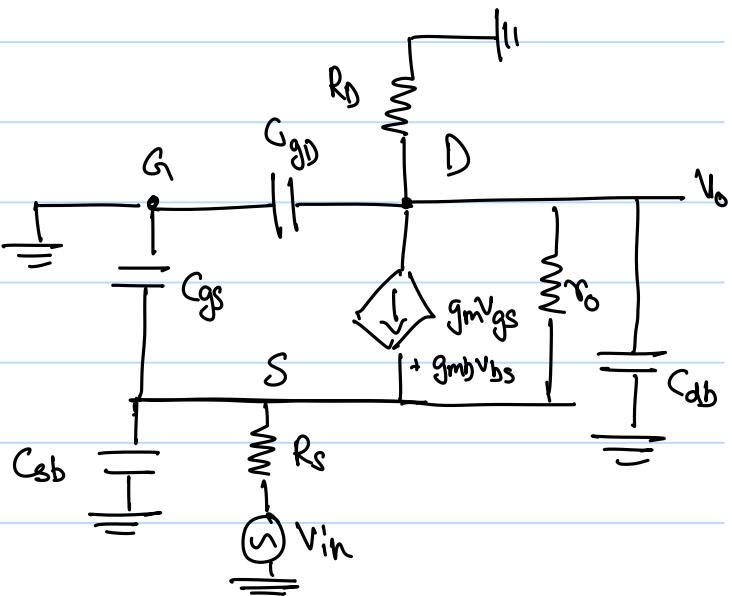
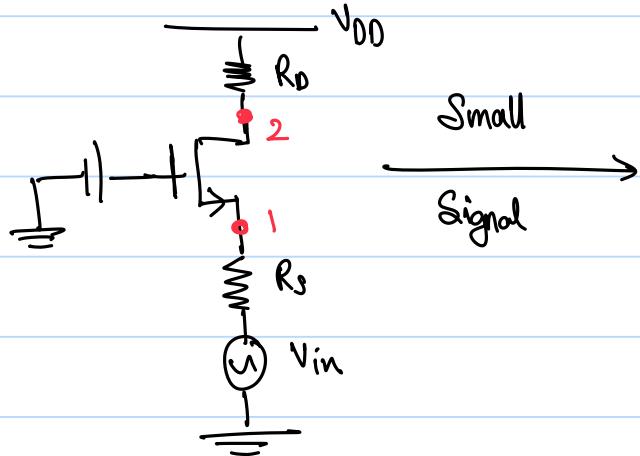
$$A_v = \frac{g_m + g_{mb}}{1 + (g_m + g_{mb})R_s} R_D \approx \frac{g_m}{1 + g_m R_s} R_D$$

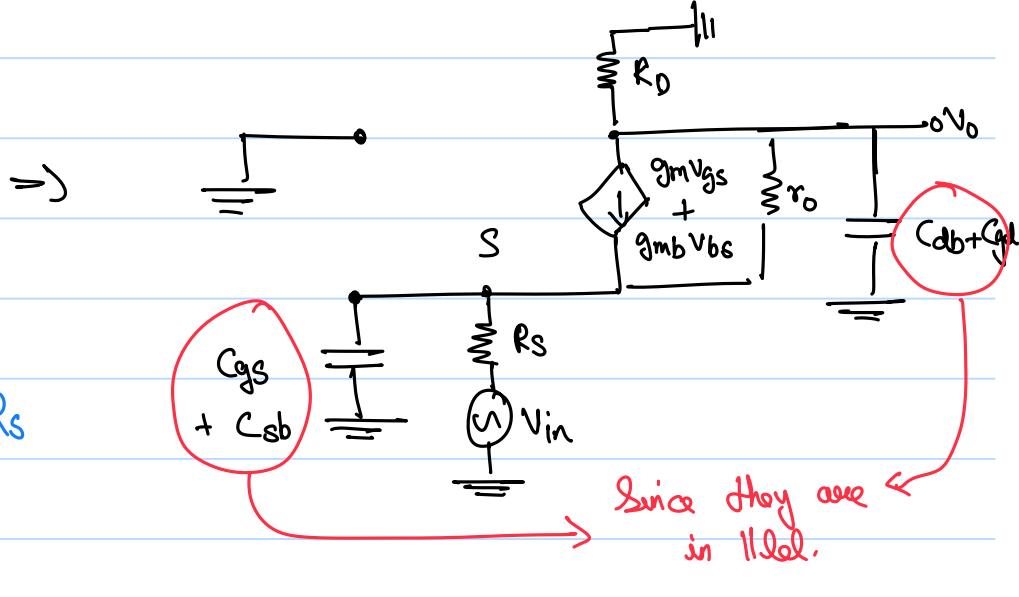
→ In kilo ohms

- Since, the input is applied at the source, the input resistance of the amplifier is very small (CS amplifier has very high imp. impedance)
- The gain is comparable to CS Amplifier if $R_s \ll \frac{1}{g_m}$.

$$\frac{A_v \times Z_{in}}{Z_{out}} = 1 \text{ for small } R_s$$

Frequency Response:





$$\Rightarrow R_i = \frac{1}{g_m + g_{mb}} \parallel R_s$$

$$C_i = C_{gs} + C_{sb}$$

$$R_2 \approx R_D \quad C_2 = C_{db} + C_{gd}$$

$C_{gs} + C_{sb}$ is comparable to $C_{db} + C_{gd}$, whereas $R_i \ll R_2$

$\therefore 3dB$ is dominated by $R_2 C_2$.

$$\Rightarrow f_{3dB} = \frac{1}{2\pi (R_D (C_{db} + C_{gd}))} \xrightarrow{\text{No Miller Effect}}$$

$\therefore f_{3dB}$ of a CG Amplifier is very high.

\rightarrow CS - CG Comparison:

CS

High gain, High i/p impedance

Low Bandwidth

CG

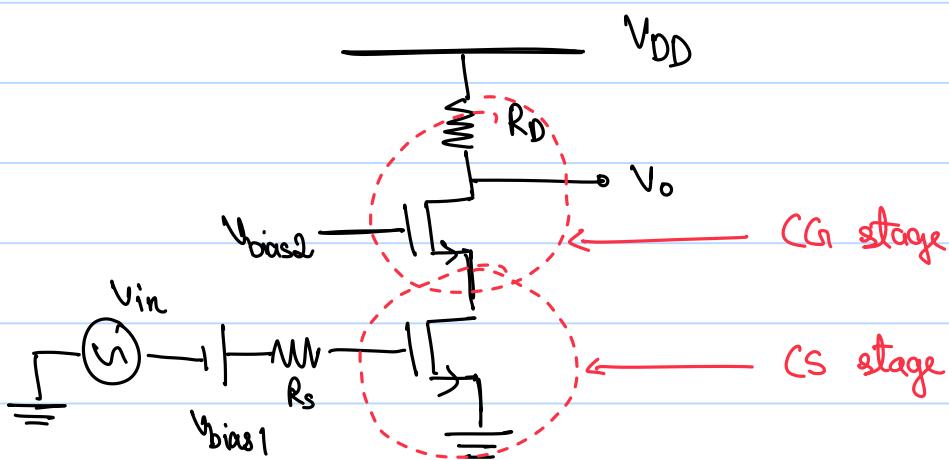
High Bandwidth, Comparable gain

Low i/p impedance

- We can get the best of both worlds by combining both CS and CG amplifier.
- CG Amplifier is a very good transresistance amplifier (current to voltage) due to its low i/p impedance.

Thus, CS Amplifier is a very good voltage to current amplifiers (transconductance amplifier)

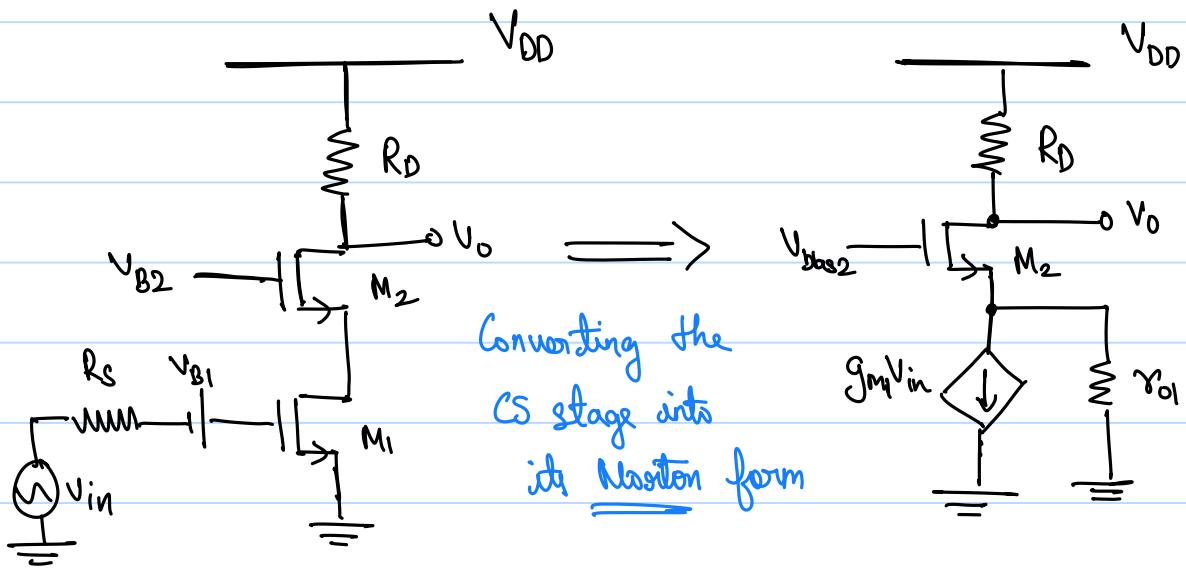
Therefore, our combined amplifier will be,



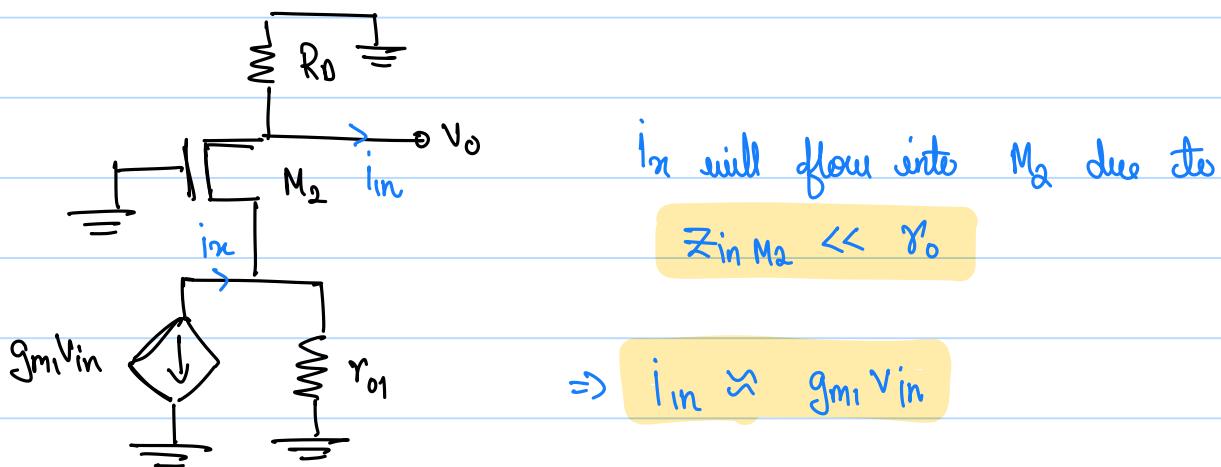
CS - CG Cascode Amplifier

→ Cascode Amplifier :-

- When the drain of one MOSFET is connected to the source of another, the action is termed as Cascoding.
- This amplifier has a gain similar to the CS amplifier with a better bandwidth.

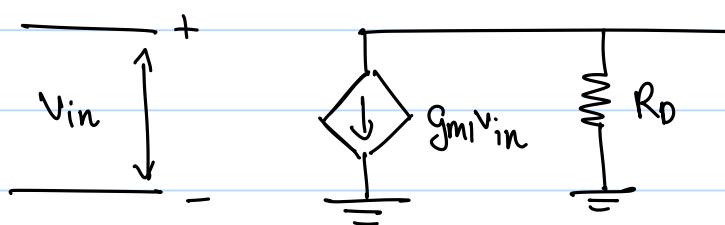


- To get the Norton Equivalent of the CG stage as well,



$$R_{N_o} = R_D \parallel r_o (1 + g_{m2} r_o) \approx R_D$$

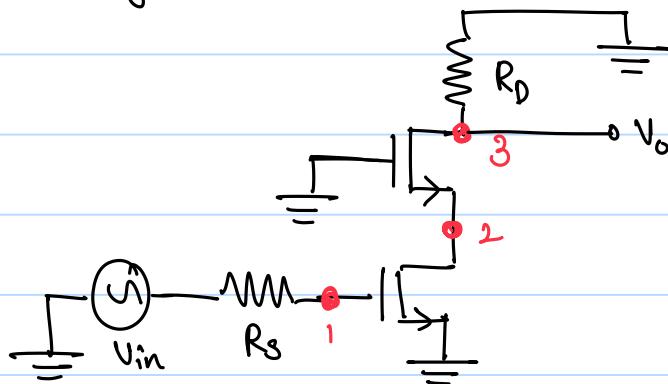
∴ Our final amplifier is,



$$\Rightarrow A_v = -g_{m1} R_D$$

just like a CS amplifier

• Frequency Response :-



①,

$$R_i = R_s \parallel z_{in}(M_1) \approx R_s$$

$$C_i = C_{gs1} + C_{gd1}(1 - A_{V1})$$

②,

$$R_2 = \frac{1}{g_{m2} + g_{mb2}} \left(1 + \frac{R_D}{r_{o2}} \right)$$

$$C_2 = C_{gd1}\left(1 - \frac{1}{A_{V1}}\right) + C_{gs2} + C_{db1} \\ + C_{sb2}$$

③,

$$R_3 = R_D \parallel z_{out}(M_2) \approx R_D$$

$$C_3 = C_{gd2} + C_{db2}$$

- At low gain, the difference in bandwidth is small, but at high gain, the bandwidth of the Cascode amplifier is much higher.

- A disadvantage of a Cascode amplifier is a lower voltage swing.

→ Comparison b/w The Different Architectures :-

CS w/ Resistive load

→ CS w/ PMOS load

low gain for normal R_D

High gain for normal

Miller Effect at high gain

PMOS. Also stable.



CS w/ Cascode PMOS load

Cascode Amplifier

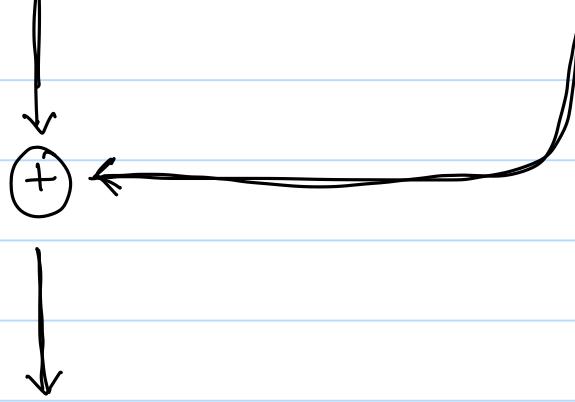
Higher gain. Reduced



Reduced Miller Effect → High Bandwidth

voltage swing

Not much improvement in Gain



Cascode Amplifier w/ PMOS load

Good frequency response and high gain
at a small size

Voltage swing is impacted

(Cascode Amplifier)

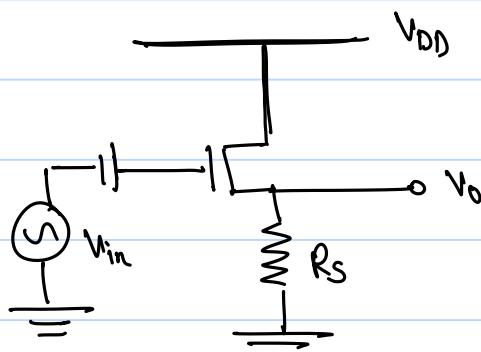
w/ Cascode PMOS load

Higher gain with good
bandwidth

Voltage swing is impacted

→ Common Drain Amplifier :-

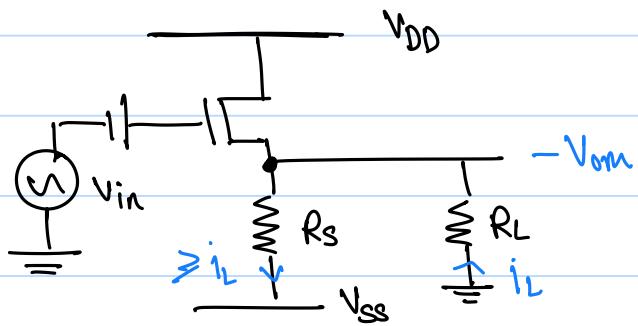
- If we want a high output impedance, CG amplifier cannot be used.
- for each high output, we can take input at the gate and output at the source



$$A_v = \frac{g_m R_s \| r_o}{1 + (g_m + g_{mb}) R_s \| r_o} \approx \frac{g_m R_s}{1 + g_m R_s} < 1$$

- The gain of a CD amplifier is less than 1.

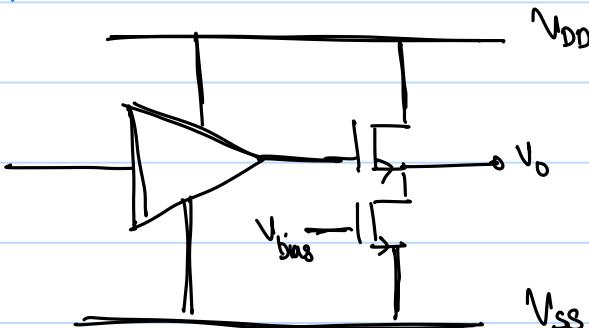
- For high R_s , the amplifier is highly linear, therefore less prone to harmonic distortion.
- Voltage swing:
 - The internal limits on voltage swing is pretty high ($\approx V_{DD}, V_{SS}$), so it is not that limiting.
 - The main limit is the output current drive (how much current the amp. can output)



$$\frac{-V_{om} - V_{ss}}{R_s} \Rightarrow i_L = \frac{V_{om}}{R_L}$$

$$\Rightarrow V_{om} \leq -\frac{V_{ss}}{R_s} \times R_s \| R_L$$

- To make this better, we can use another NMOS (current source)
- In practice while using a CD amplifier, we combine it with a gain stage amplifier.

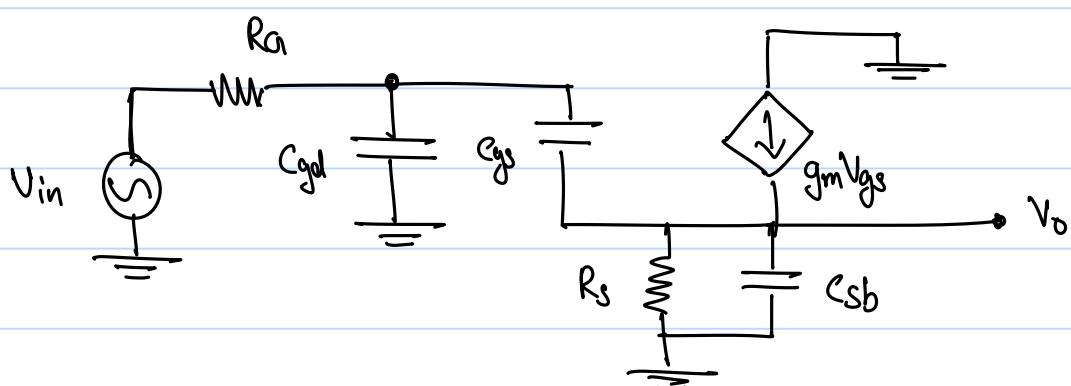


(Gives us low
output impedance)

- Still the output voltage swing of a CD amplifier is low, which is why it is not used that much.

- Frequency Response :-

- Small signal model of CD Amplifier,



- Upon calculation, we get that the bandwidth of a CD amplifier is usually pretty high.

- CD vs CS :-

CS

Need high bias current for
low o/p impedance

Almost rail to rail voltage
swing

FRA impacted by Miller's
offset

CD

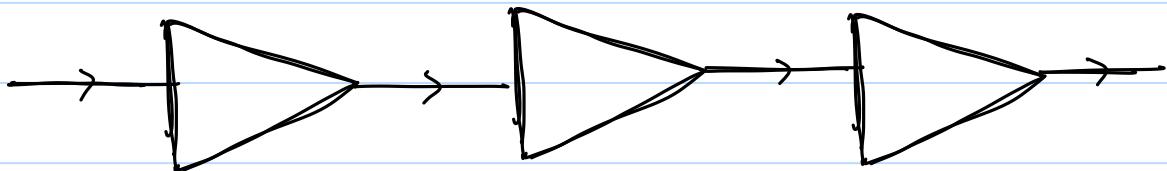
Lower o/p impedance at
lower bias current

swing limited by current
drive, by about a V_T drop

Good frequency response.

→ Conclusion :-

Using the 3 topologies discussed, our final amplifier can be as such,



ilp stage

Common Source

Gain stage

Common Gate

olp stage

Common Drain

- High ilp impedance
- Moderate gain
- High Bandwidth
- High gain w/ Guarding
- Low olp impedance
- High linearity
- PMOS load