Part-2(a) (BJT characterization)

3. (a) Take BC547B npn transistor from the LTSPICE library and make a circuit as shown in Fig. 2(a). Use $V_{CC} = 12\ V$, sweep I_B from 0 to 100 μA in step size of 10 μA and plot V_{BE} with respect to I_B. What is the forward bias emitter-base junction (EBJ) voltage obtained from the plot? Repeat experiment for $V_{CC} = 0\ to\ 12\ V$ in step size of 2 V and give superimposed plots for different V_{CC} on same graph.
(Hint: .dc I_B 0 100u 10u VCC 0 12 2)

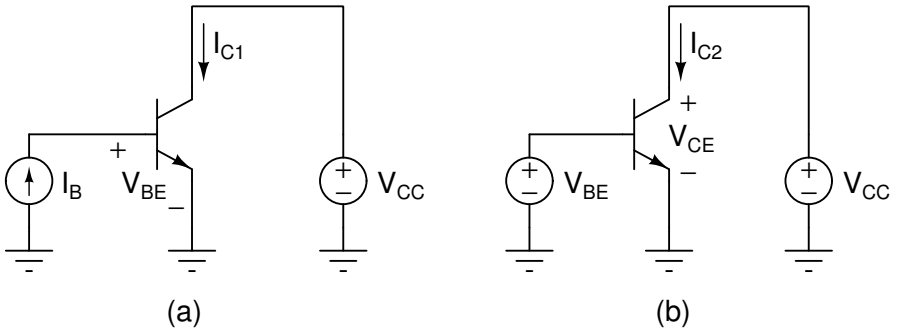

Figure 2

(b) Use the schematic shown in Fig. 2(b) in LTSPICE and plot I_C vs V_{BE} for $V_{CC} = 12\ V$ at 20° C, 30° C, 40° C, 50° C by sweeping V_{BE} from 0 to 0.7 V in step size of 0.01 V. All plots should overlay on same graphical axis.
(Hint: .dc V_{BE} 0 0.7 0.01, .step TEMP 20 50 10 or .step TEMP LIST 20 30 40 50)

(c) For Fig. 2(a), plot I_C vs V_{CE} by sweeping V_{CC} from 0 to 12 V in step size of 0.01 V and sweeping $I_B = 0\ \mu A$ to 100 μA in step size of 10 μA. Clearly mark cut-off, saturation and active modes in your characteristic plot. Find and tabulate incremental current gain $\beta = \frac{\Delta I_C}{\Delta I_B}$ in saturation (at $V_{CE} = 100$ mV) and active (at $V_{CE} = 600$ mV) modes for $I_{B1} = 50$ μA to $I_{B1} = 60$ μA. Comment on the reason for the difference observed. Tabulate the current gain $\beta = \frac{I_C}{I_B}$ at $V_{CE} = 1\ V$ for different values of I_B. Do you observe Early effect. Estimate the value of early voltage (V_A) from your simulations.
(Hint: slope at a point $= y/x = I_C/(V_A + V_{CE})$)

(d) In your exams, I will ask similar plots for a pnp transistor. Therefore practise and repeat above experiments for pnp transistor also. **(No need to submit this part)**

(e) **Practise problems:** All solved examples and exercise problems of Chapter-4 ($7th$ edition) of the reference textbook Sedra and Smith. **(No need to submit this part)**

Part-2(b) (BJT amplifier analysis and design)

4. Fig. 3 shows a common emitter (CE) voltage amplifier. Given that $V_{CC} = 12\ V$, $C_B = 10\ \mu F$, $C_C = 10\ \mu F$, $C_E = 100\ \mu F$, $R_1 = 18.46\ k\Omega$, $R_2 = 2.24\ k\Omega$, $R_E = 2\ k\Omega$, $R_C = 30.3\ k\Omega$, $R_L = 1\ k\Omega$ and $v_{in} = V_m sin(2\pi f_0 t)$ V, where $f_0 = 1\ kHz$. Implement the given circuit using BC547B (NXP) in LTSPICE and simulate following:

(a) Draw the DC picture of the given circuit and calculate theoretically V_C, V_B, V_E, I_C and I_B. Find the mode of operation of BJT in the given circuit.
(Hint: For DC picture: AC sources are replaced with its internal resistance and capacitors act as open (why?). In forward active mode, V_{BE} is fixed ($\approx 0.7\ V$), $I_C = \beta I_B$, β for 547B you know from previous problem.)

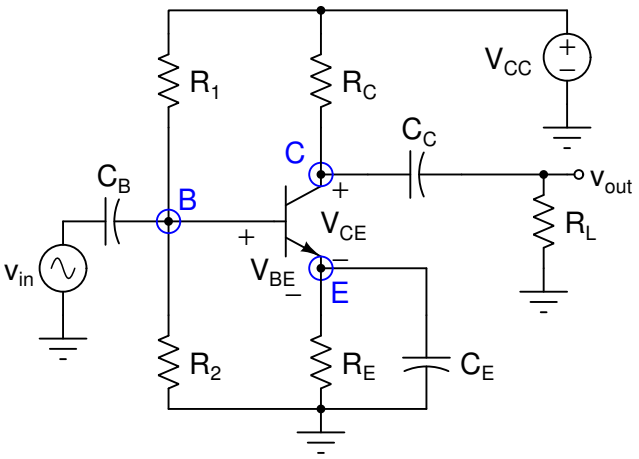

Figure 3

(b) Run operating point simulation (.op) and verify your theoretical values with the simulated values. Give a table showing theoretical and simulated values of different parameters.

(c) Calculate small signal parameters g_m, r_π and r_0 for the transistor.

(d) Draw the signal picture and small signal equivalent of the circuit.
(Hint: Capacitors should be replaced by its impedance values at the given frequency.)

(e) Derive the expression for the small signal voltage gain ($A_v = \frac{v_{out}}{v_{in}}$).

(f) Run transient analysis (.tran 50m) and plot v_{in} and v_{out} for $V_m = 10\ mV$. Verify the gain from transient simulations with the calculated gain in the previous part.

(g) Plot FFT of v_{out} and report differences of 2^{nd}, 3^{rd} and 4^{th} harmonics from the fundamental (1 kHz) component.
(Hint: To plot FFT: on waveform viewer, right click - view - FFT)

(h) By using the parametric sweep, vary the amplitude (V_m) of the input signal and report total harmonic distortion from the spice error log file. Report corresponding FFT plots also. You might observe that with increasing value of V_m, THD increases and FFT also shows prominent harmonics. Why does it happen? Briefly comment with supporting calculations.
(Hint: For parametric sweep: define v_{in} = SINE(0 {Vm} 1k) (NOTE THAT '{}' is must) and use spice directive .step param Vm 10m 200m 50m. For THD: right click on schematic editor - view - SPICE Error Log. For more details and help refer LTSPICE manual shared earlier.)

(i) Run AC analysis (.ac dec 10 1m 1G), plot magnitude and phase of $A_v = \frac{v_{out}}{v_{in}}$ and report DC gain (dB) and -3 dB bandwidth of the amplifier.
(Hint: Comment .tran and other analysis, For v_{in} source in your simulation setup, give V_m a constant value, give AC amplitude = 1)

(j) Now parametrize the resistance R_C and sweep its value from 28 $k\Omega$ to 40 $k\Omega$ in step size of 2 $k\Omega$ and run ac simulation to plot $|A_v| = \frac{v_{out}}{v_{in}}$. Give a table showing DC gain for different values of R_C? Why the gain is changing? Compare two cases (30 $k\Omega$ and 40 $k\Omega$) quantitatively and justify your answers.

5. Redesign (give values of $C_B, C_C, C_E, R_1, R_2, R_E, R_C, I_C, I_B$) the CE amplifier shown in Fig. 3 to achieve same voltage gain with same $R_L = 1\ k\Omega$ and same bandwidth but with reduced supply of 5 V, that is $V_{CC} = 5\ V$. Show design procedure with detailed calculations and report DC, transient and AC simulation results to verify your design. Compare the total DC power ($P_{DC} = V_{CC} \times I_{Drawn}$) consumed for $V_{CC} = 12\ V$ and $5\ V$.