LAB-REPORT-3

NAME : Chanda Akshay Kumar

Roll No : 2024102014

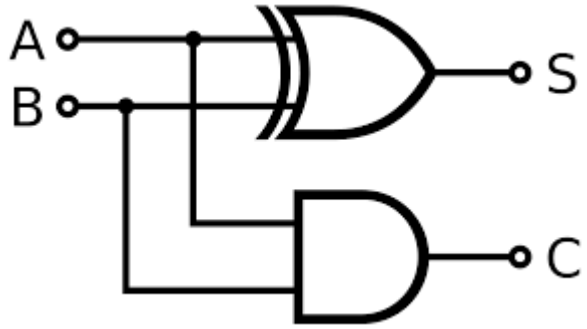
Group No : 07 Teams(9)

Experiment 1: *Half Adder*

Objective: Half Adder using AND and XOR logic gates.

Electronic components used: Disgital testing kit (DSM) , XOR(7486) and AND(7408) IC's .

The reference circuit:



Procedure:

- Place the XOR (74LS86) and AND (74LS08) ICs on a breadboard.
- Connect the power supply (5V) to the Vcc and GND pins of both ICs.
- Connect input A to one input of both the XOR and AND gates.
- Connect input B to the other input of both the XOR and AND gates.
- The XOR gate's output gives the Sum.
- The AND gate's output gives the Carry.
- Optionally, connect LEDs with resistors to visualize the outputs.
- Power the circuit and test with different input combinations.

Conclusion:

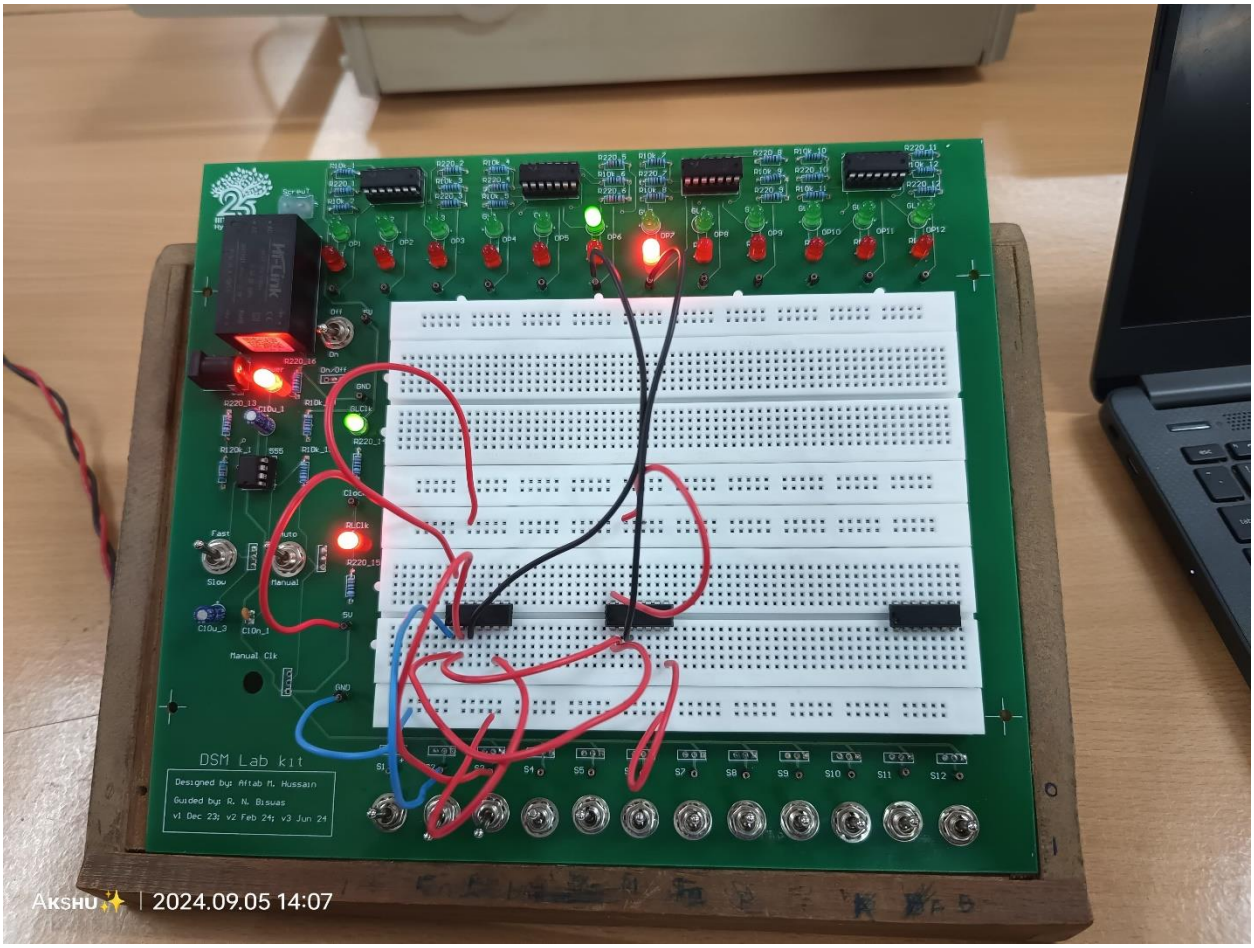
- **S1:** The Sum output (S) is generated by the XOR gate , Boolean algebra expression $S=A \oplus B$.
- **C1:** The Carry output (C) is generated by the AND gate , Boolean expression $C=A \cdot B$.

Truth Table of Half Adder:

Input A	Input B	Sum (S)	Carry (C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The half adder circuit was successfully built and tested, with results aligning with the expected binary addition outputs. This experiment confir ms the correct operation of the circuit and illustrates the fundamental role of logic gates in digital systems.

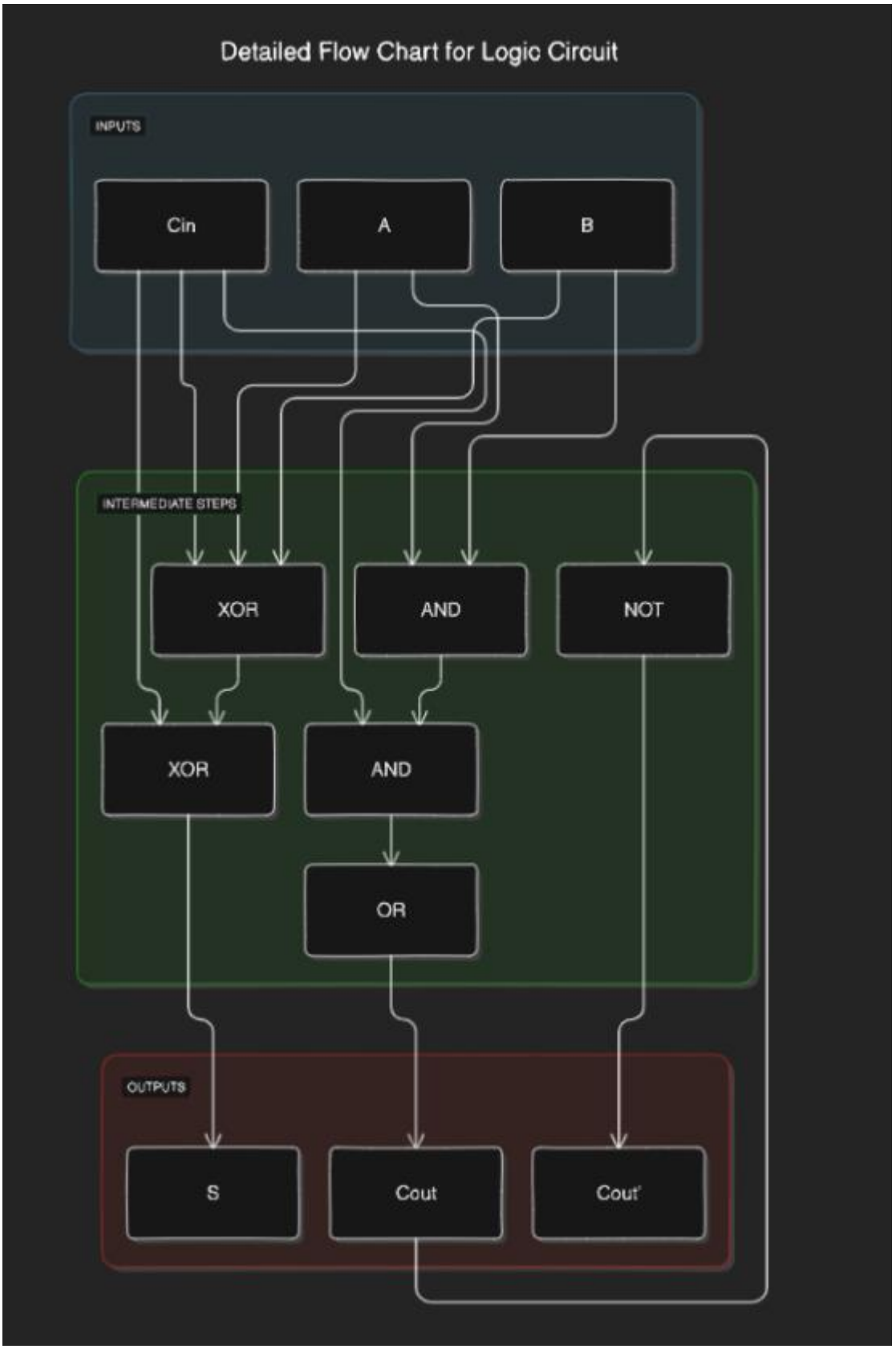
Link for Tinkercad simultation:



Experiment 2: ***Full Adder***

Objective: Full Adder using AND and XOR logic gates.
Electronic components used: Digital testing kit (DSM), XOR(7486) and AND(7408) ICs.

The reference circuit:


Detailed Flow Chart for Logic Circuit
INPUTS
Cin
A
B
INTERMEDIATE STEPS
XOR
AND
NOT
XOR
AND
OR
OUTPUTS
S
Cout
Cout'

Procedure:
• Place the XOR (74LS86) and AND (74LS08) ICs on a breadboard.
• Connect the power supply (5V) to the Vcc and GND pins of both ICs.
• Connect input A to one input of both the XOR and AND gates.
• Connect input B to the other input of both the XOR and AND gates.
• The output of the first XOR gate connects to one input of the second XOR gate; input C connects to the other input.
• The output of the second XOR gate gives the Sum (S).
• Use AND gates to generate carries, then combine them to get the final Carry (C).
• Power the circuit and test with different input combinations.

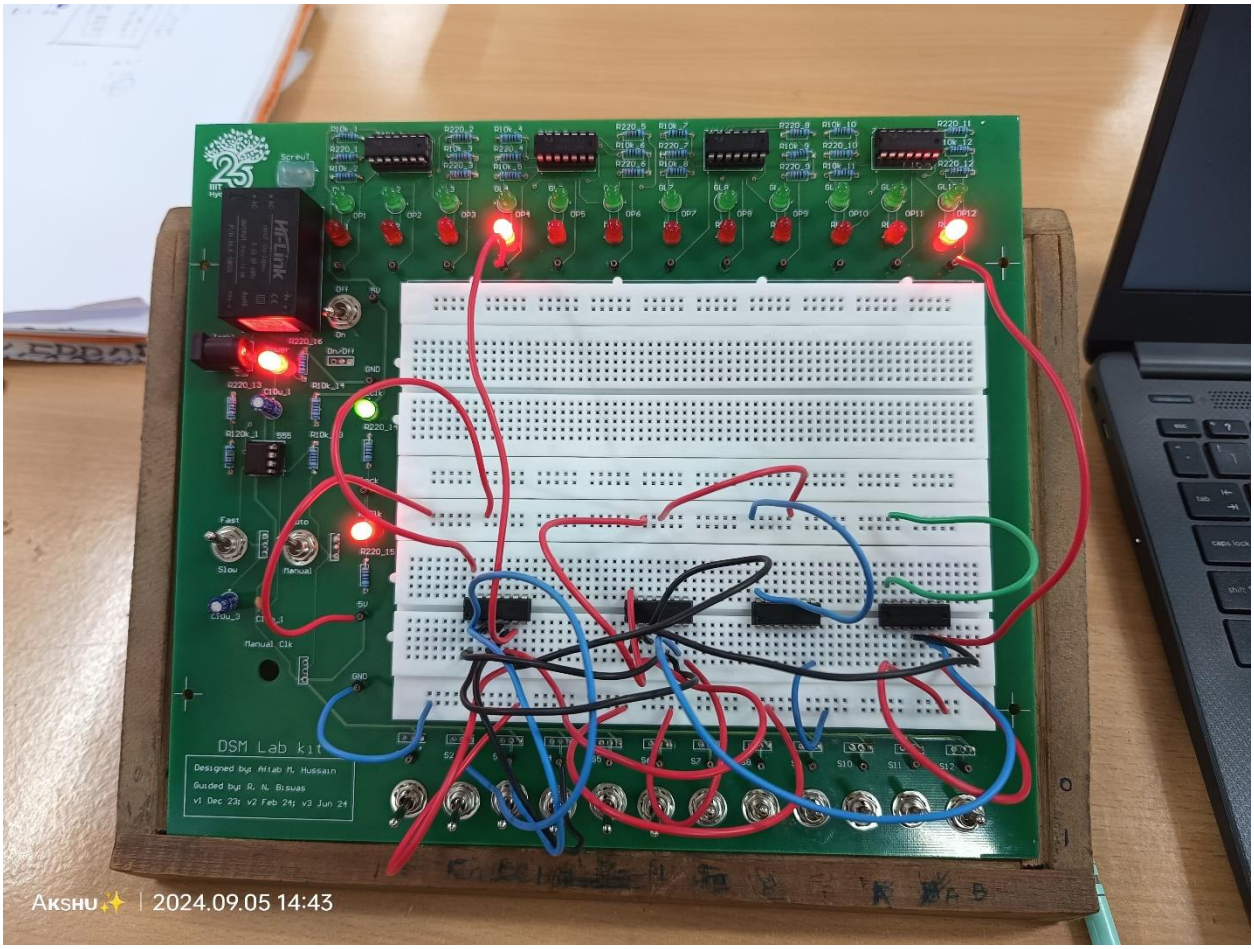
Conclusion:
• **S1:** The Sum output (S) is generated by the XOR gate, Boolean algebra expression $S=A \oplus B \oplus C$.
• **C1:** The Carry output (C) is generated by combining the outputs of the AND gates, Boolean expression $C=(A \cdot B)+((A \oplus B) \cdot C)$.

Truth Table of Full Adder:

Input A	Input B	Input C	Sum (S)	Carry (C)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

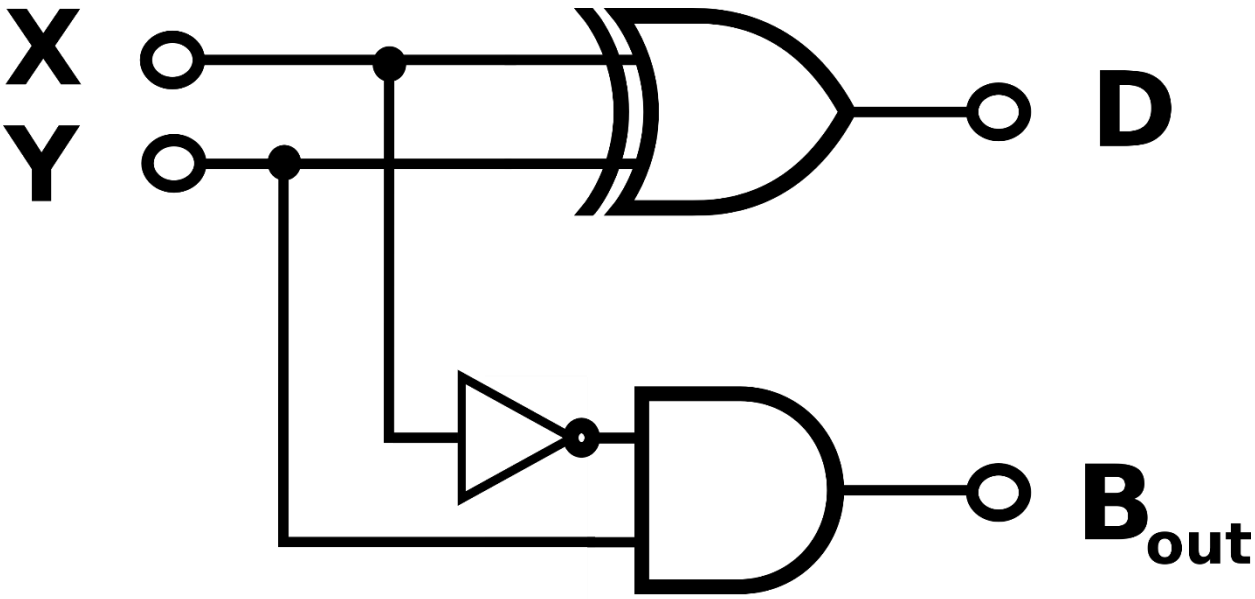
The full adder circuit was successfully built and tested, with results matching the expected binary addition outputs. This experiment demonstrates the correct functionality of the circuit and highlights the integration of logic gates in digital arithmetic operations.

Link for Tinkercad simultation:


DSM Lab kit
Designed by Aftab M. Hussain
Guided by R. N. Biswas
v1 Dec 23; v2 Feb 24; v3 Jun 24
Manual Clk
Fast
Slow
Manual
Auto
Dn/Off
GND
5V
AKSHU✨ | 2024.09.05 14:43

Experiment 3: *Half Subtractor*

Objective: Half Subtractor using AND and XOR logic gates.
Electronic components used: Digital testing kit (DSM), XOR(7486) and AND(7408) ICs.
The reference circuit:



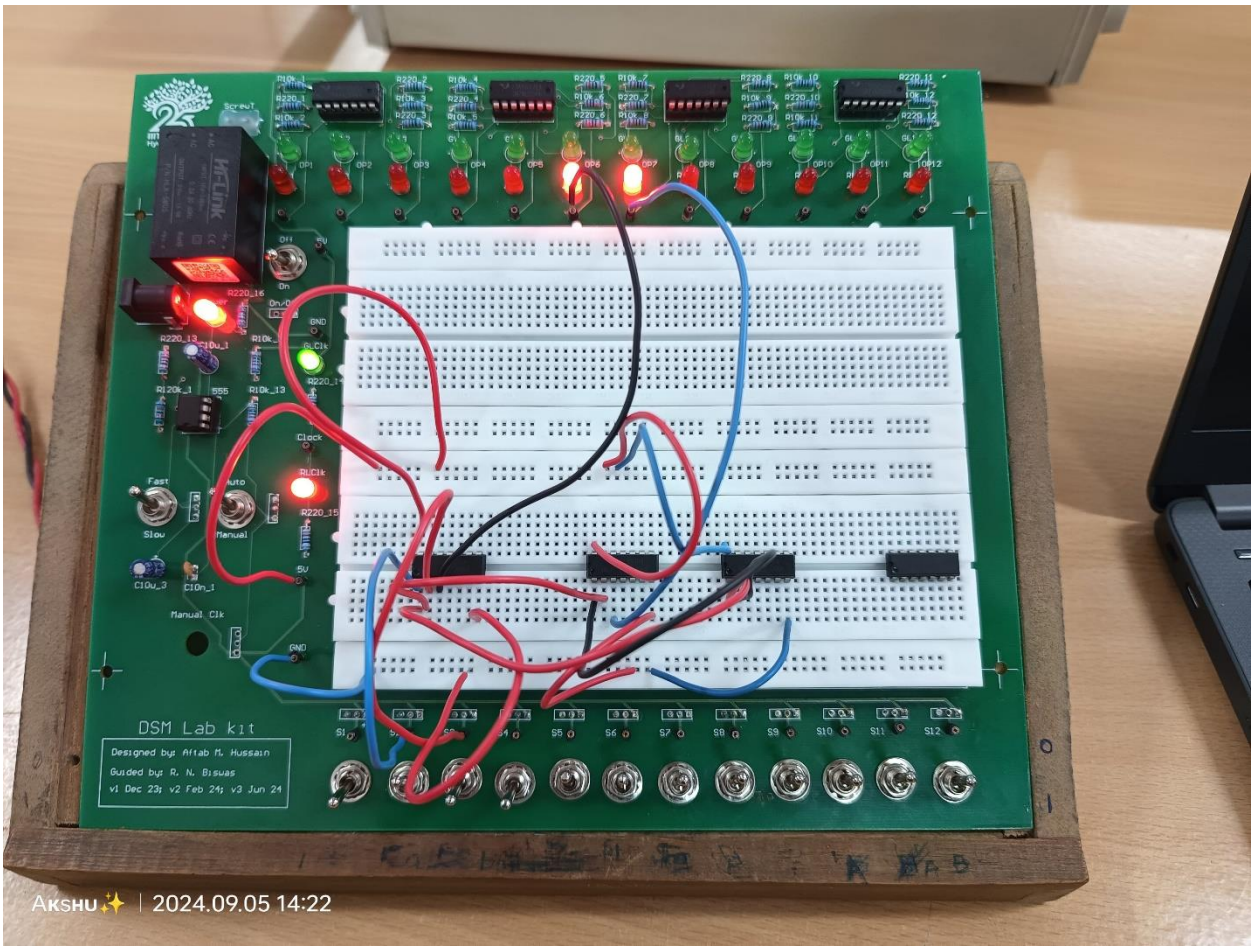
Procedure:
• Place the XOR (74LS86) and AND (74LS08) ICs on a breadboard.
• Connect the power supply (5V) to the Vcc and GND pins of both ICs.
• Connect input A to one input of the XOR gate and input B to the other input.
• The XOR gate's output gives the Difference (D).
• Connect input A to the NOT gate, then connect the output of the NOT gate and input B to the AND gate.
• The output of the AND gate gives the Borrow (B).
• Power the circuit and test with different input combinations.
Conclusion:
• **D1:** The Difference output (D) is generated by the XOR gate, Boolean algebra expression $D=A \oplus B$.
• **B1:** The Borrow output (B) is generated by the AND gate after inverting A, Boolean expression $B=A^{-} \cdot$ **Truth Table of Half Subtractor:**

Input A	Input B	Difference (D)	Borrow (B)
0	0	0	0
0	1	1	1
1	0	1	0

1	1	0	0

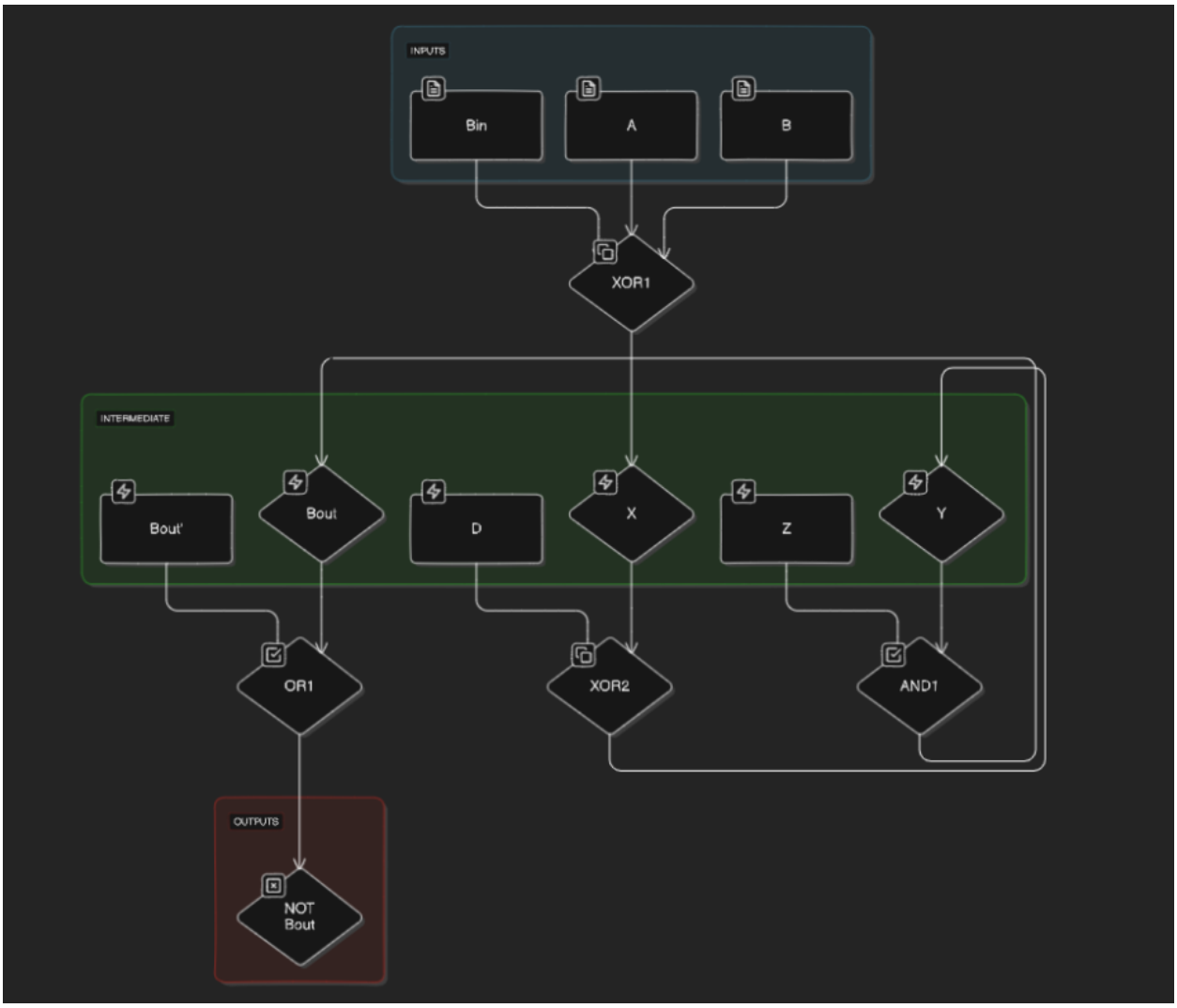
The half subtractor circuit was successfully built and tested, with results consistent with the expected binary subtraction outputs. This experiment validates the operation of the circuit and reinforces the application of logic gates in digital subtraction.

Link for Tinkercad simultation:



Experiment 4: *Full Subtractor*

Objective: Full Subtractor using AND, NOT, and XOR logic gates.
Electronic components used: Digital testing kit (DSM), XOR(7486), AND(7408), and NOT(7404) ICs.
The reference circuit:



Procedure:
• Place the XOR (74LS86), AND (74LS08), and NOT (74LS04) ICs on a breadboard.
• Connect the power supply (5V) to the Vcc and GND pins of all ICs.
• Connect input A and B to the first XOR gate.
• The output of the first XOR gate connects to one input of the second XOR gate; input C connects to the other input.
• The output of the second XOR gate gives the Difference (D).
• Connect input B and C to the first AND gate to generate the first borrow (B1).
• Connect input A to a NOT gate, and then connect the output of the NOT gate and input B to the second AND gate to generate the second borrow (B2).
• Finally, combine the outputs of the AND gates using XOR logic to generate the final Borrow (B).
• Power the circuit and test with different input combinations.

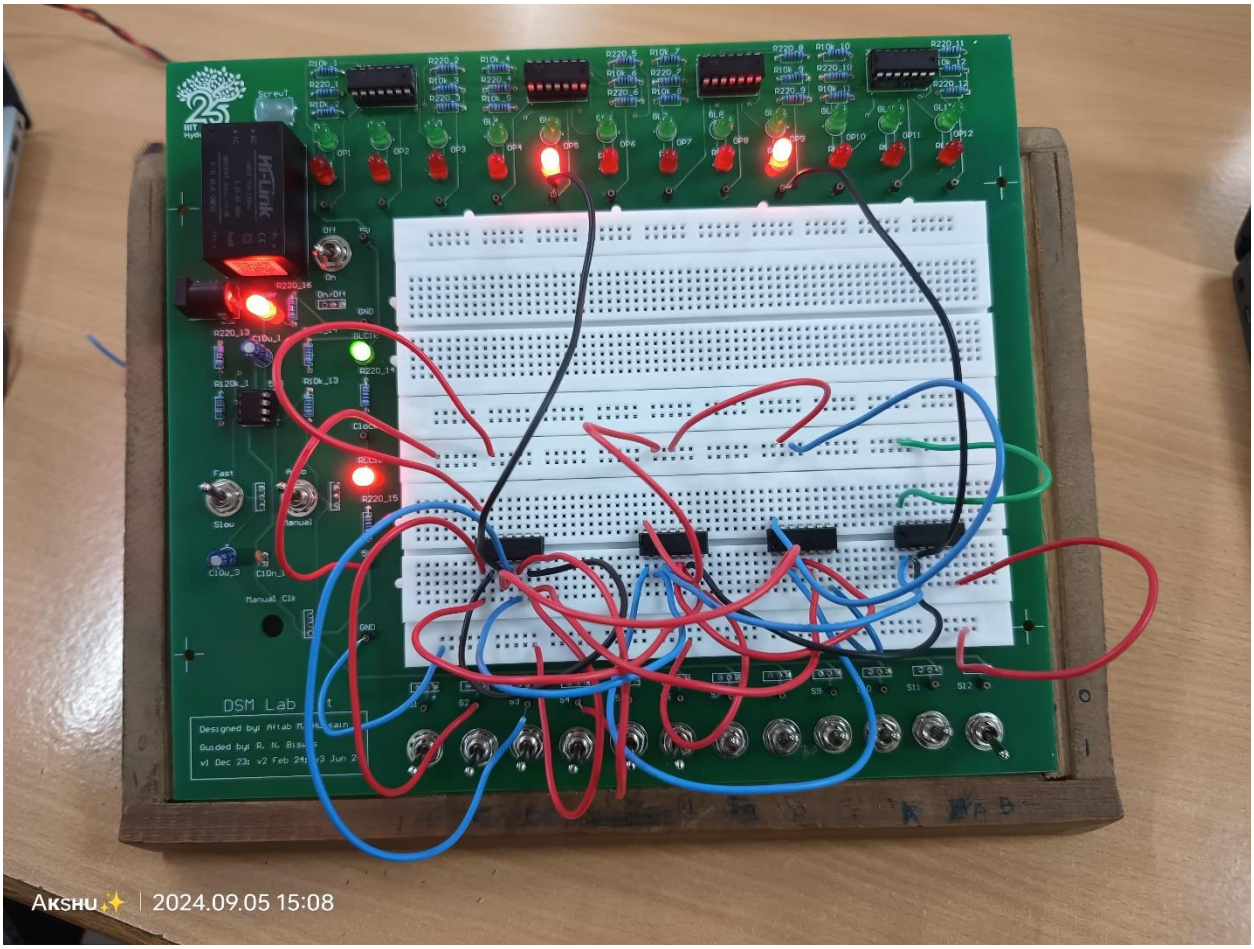
Conclusion:
• **D1:** The Difference output (D) is generated by the second XOR gate, Boolean algebra expression $D=A \oplus B \oplus C$.
• **B1:** The Borrow output (B) is generated by combining the outputs of the AND gates, Boolean expression $B=(\bar{A} \cdot B)+(B \cdot C)$.

Truth Table of Full Subtractor:

Input A	Input B	Input C	Difference (D)	Borrow (B)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

The full subtractor circuit was successfully built and tested, with results corresponding to the expected binary subtraction outputs. This experiment affirms the accurate functionality of the circuit and underscores the importance of logic gates in complex digital arithmetic.

Link for Tinkercad simultation:


DSM Lab
Akshu✨ | 2024.09.05 15:08