Total No. of Questions—**8**]　　　　　　　[Total No. of Printed Pages—**2**

Seat
No.

[5459]-203

S.E. (IT) (I Sem.) EXAMINATION, 2018
DIGITAL ELECTRONICS AND LOGIC DESIGN
(2015 PATTERN)

Time : Two Hours　　　　　　　　　　**Maximum Marks : 50**

N.B. :— (i)　Answer question nos. **1** *or* **2**, **3** *or* **4**, **5** *or* **6** and **7** *or* **8**.

　　(ii)　Neat diagrams must be drawn wherever necessary.

　　(iii)　Assume suitable data, if necessary.

1.　(a)　Compare TTL and CMOS logic families.　　　　　　[6]

　　(b)　Minimize the given Boolean expression using Quine-McCuskey method :　　　　　　[6]

　　　　$F(A, B, C, D) = \Sigma m (0, 1, 3, 7, 8, 9, 11, 15)$.

Or

2.　(a)　Convert the following numbers in Binary form :　　　[6]

　　　(i)　$(125.12)_{10} = (?)_2$

　　　(ii)　$(337.025)_8 = (?)_2$

　　　(iii)　$(5DB.FA)_{16} = (?)_2$

　　(b)　Implement given function using 8 : 1 MUX and logic gates. [6]
　　　　$F(A, B, C, D) = \Sigma m (0, 1, 3, 4, 8, 9, 15)$.

3.　(a)　Design and implement T flip-flop using SR flip-flop.　　[6]

　　(b)　Draw state diagram to detect sequence 101 using Moore Modeling and Mealy modeling style.　　　　　　[6]

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4. (*a*) Give comparison of Combinational circuit with Sequential circuit. Draw and explain one-bit memory cell using NAND gates. [6]

(*b*) Design sequence generator to generate sequence 1010 using shift register. [6]

5. (*a*) Design and implement given functions F1 and F2 using suitable PAL : [7]

$$F1(A, B, C) = \Sigma m (0, 1, 3, 6, 7);$$

$$F2(A, B, C) = \Sigma m (1, 2, 4, 6)$$

(*b*) Write the comparison of FPGA and CPLD. [6]

6. (*a*) Draw and explain various components used in ASM chart. [6]

(*b*) Implement Full adder circuit using suitable PLA. [7]

7. (*a*) Explain data objects used in VHDL with appropriate examples. [6]

(*b*) Write VHDL code (Entity and Architecture) for Full adder using Behavioural modeling style. [7]

8. (*a*) Explain difference between Sequential statements and Concurrent statements used in VHDL with suitable examples. [6]

(*b*) Write VHDL code for half-adder using structural modeling style. [7]