Total No. of Questions—8]　　　　　　　[Total No. of Printed Pages—2

Seat
No.

[5352]-572

S.E. (I.T.) (I-Sem.) EXAMINATION, 2018

COMPUTER ORGANIZATION AND ARCHITECTURE

(2015 PATTERN)

Time : Two Hours　　　　　　　　　　　Maximum Marks : 50

N.B. :—　(*i*)　Neat diagram must be drawn wherever necessary.

(*ii*)　Figures to the right indicate full marks.

(*iii*)　Assume suitable data, if necessary.

1.　(*a*)　State and explain marketing metrics–MIPS, MFLOPS and Amdahl's law.　[6]

(*b*)　Draw and explain processor organisation.　[6]

Or

2.　(*a*)　Find CPU time, for program having 10×10^6 instructions which is executed on processor having CPI 1.0, clock rate of 4 GHz.　[6]

(*b*)　Give classification of instruction based on function.　[6]

3.　(*a*)　Explain MESI protocol with diagram.　[6]

(*b*)　A cache has 256 blocks of 16 words each, memory is 64k words. Find sizes, if cache used :　[7]

(*i*)　Direct mapping

(*ii*)　Fully Associative mapping.

4. (*a*) Draw and explain hardwired control unit. [6]

(*b*) Write control sequence for the execution of the following instructon : [7]

ADD (R_3) + R_1 where R_1 ← R_1 + (R_3).

5. (*a*) What is instruction pipelining ? How it improves performance of computer ? [6]

(*b*) Explain dynamic branch prediction and delayed branch prediction for MIPS pipeline with suitable diagram and example. [6]

Or

6. (*a*) Draw and exaplain 5 stage MIPS pipeline. [6]

(*b*) Describe in brief any *one* pipeline hazard and its solution. [6]

7. (*a*) Draw and explain multicore architecture. [7]

(*b*) What is cluster computing ? Explain its benefits. [6]

Or

8. (*a*) Explain multithreading. Describe its various types with suitable diagrams. [7]

(*b*) Write short notes on : [6]

(*i*) Core Duo

(*ii*) Core-i7.