Total No. of Questions—8	Total	No.	of	Questions-	-8
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Seat	
No.	6

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S.E. (E&TC/Electronics) (I Sem.) EXAMINATION, 2018 DIGITAL ELECTRONICS (2015 PATTERN)

			(2015 PATTERN)		
Time: Two Hours Maximum Marks: 50					
<i>N.</i> .	В.	:—	(i) Answer Q. No. 1 or Q. No. 2, Q. No. 3	or Q. No. 4,	
			Q. No. 5 or Q. No. 6, Q. No. 7 or Q.	No. 8.	
			(ii) Neat diagrams must be drawn wherever	necessary.	
			(iii) Figures to the right indicate full marks.		
			(iv) Assume suitable data, if necessary.		
Q	1	a	Design a full adder using two half adders.	4 M	
		b	Minimize the following expression using k-map and	4 M	
			implement using logic gates		
			$Y=\sum m(4,5,6,7,12,13,14,15)$		
		С	State the types of shift register and explain any one of them	4 M	
			C, So.		
Q	2	a	Design 3 bit synchronous counter using Delay flip flop(D-FF)	6 M	
		В	Design 4:1 MUX using 2:1 MUX	6 M	
			*	0.1	
Q	3	a	Explain Mealy and Moore circuits with diagram?	6 M	
		b	Draw and explain operation of Tri-state TTL inverter?	6 M	
				· ·	
Q	4	a	Explain the terms related to ASM chart.	6 M	
			I. state box		
			II.Decision box		
			III.conditional box		
		b	Draw and explain the working of 2 input CMOS Inverter	6 M	

Q	5	a	Implement the following functions using PLA	6 M
			$F1=\sum m(0,2,4,6)$	
			$F2=\sum m(2,3,6,7)$	
		b	Explain the characteristics of DRAM.	4M
		c	State various types of ROMS and their applications.	3M
Q	6	a	Draw the internal organization of asynchronous SRAM	6 M
		b	Explain the general architecture of CPLD	4M
		С	Explain the difference between PLA and PAL	3M
Q	7	a	Draw and explain block diagram of microcontroller	6 M
		b	Explain stack operation and stack pointer register of 8051	4M
		С	What are the different modes of timer of 8051?	3M
Q	8	a	Explain 8051 port structure with neat diagram	6 M
			66,00	
		b	Explain the use of DPTR	4M
		С	State salient features of 8051 microcontroller	3M
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			9.7	
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