Total No. of Questions—**8**] [Total No. of Printed Pages—**4**

Seat No.	

[5152]-536

S.E. (E&TC/Electronics) (II Sem.) EXAMINATION, 2017

INTEGRATED CIRCUITS

(2015 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. **:—** (*i*) Answer Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4**, Q. No. **5** *or* Q. No. **6**, and Q. No. **7** *or* Q. No. **8**.

(*ii*) Neat diagrams must be drawn wherever necessary.

(*iii*) Figures to the right indicate full marks.

(*iv*) Use of calculator is allowed.

(*v*) Assume suitable data, if necessary.

1. (*a*) Define the following characteristics of Op-amp : [6]

(*i*) Input bias and offset current

(*ii*) CMRR

(*iii*) Bandwidth

(*iv*) Slew Rate.

(*b*) Draw an Inverting Summing amplifier with three input. Derive an expression for its output voltage : [6]

$$V_0 = -(V_a + V_b + V_c)$$

P.T.O.

Or

2. (*a*) An emitter biased Dual input balanced output differential amplifier has the following specifications : [6]

$V_{CC} = -V_{EE} = 10$ V, $R_{C1} = R_{C2} = 2.7$ kΩ and $R_E = 5.6$ kΩ, Transistor array is CA3086 with $\beta_{ac} = \beta_{dc} = 100$ and $V_{BE} = 0.715$ V. Calculate :

(*i*) Voltage Gain (Ad)

(*ii*) Input Resistance (Ri)

(*iii*) Output Resistance (Ro)

(*b*) Draw the circuit diagram of Practical Integrator along with frequency response and explain its operation. [6]

3. (*a*) Explain with a neat circuit diagram woking of inverting Schmitt trigger using Op-Amp. Also give the equation for triggering points. [6]

(*b*) With neat circuit diagram, explain current to voltage converter. [6]

Or

4. (*a*) Draw and explain square wave generator using Op-Amp and give expression for output frequency. [6]

(*b*) An 8-bit DAC converter has a resolution of 10 m V/bit. Find the analog output voltage for the following digital input : [6]

(1) 1000 1010

(2) 0001 0000

5. (*a*) With the help of neat block diagram explain operation of PLL. Define the term "lock range" and "Capture range". [7]

(*b*) Design a second order low pass filter with higher cut-off frequency of 2 kHz with pass gain is 1.5. Draw the designed circuit and sketch its frequency response. [6]

$R_2 = R_3 = R$ and $C_2 = C_3 = C$

Assume C = 0.01 µf and R_1 = 10 kΩ.

Or

6. (*a*) With the help of neat circuit diagram explain the operation of RC phase shift oscillator. [6]

(*b*) Design a wide band pass filter for f_L = 100 Hz, f_H = 1 kHz and pass band gain equal to 4. Also calculate the value of its quality factor 'Q'. Assume : [7]

C' = 0.01 µf and C = 0.05 µf

R_1' = 10 kΩ and R_1 = 10 kΩ

7. (*a*) Calculate output frequency 'f_0', Lock range 'Δf_L', Capture range 'Δf_C' of a PLL. If R_T = 10 kΩ, C_T = 0.01 µf, filter capacitor C = 10 µf and Internal resistance = 3.6 kΩ. Assume ± V = 10V. [6]

(*b*) Draw and explain wide band pass filter. Draw its frequency response. [7]

Or

8. (*a*) Draw neat circuit diagram of Voltage Controlled Oscillator (VCO) and derive expression for output frequency. [7]

(*b*) Design an Active notch filter for rejecting the mains frequency of 50 Hz. Draw detailed design circuit diagram. Assume C = 0.47 μf. [6]