Total No. of Questions : 8] **SEAT No. :**

P3665 **[Total No. of Pages : 2**

[5461]-561

B.E. (E&TC)

VLSI DESIGN AND TECHNOLOGY

(2015 Pattern)

Time : 2.30 Hours] ***[Max. Marks : 70***

Instructions to the candidates:

1) ***Answer Q. 1 or Q. 2, Q. 3 or Q.4 Q.5 or Q.6 and Q.7 or Q.8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right side indicate full marks.***
4) ***Use of calculator is allowed.***
5) ***Assume suitable data if necessary.***

Q1) a) Explain subprograms in detail. **[6]**
i) Functions and
ii) Procedures

b) Write short note on clock distribution technique. **[7]**

c) Draw CPLD XC9500 series architecture and explain in detail. **[7]**

OR

Q2) a) Draw HDL design flow and explain in brief. **[6]**

b) Explain clock skew and write in detail about positive and negative clock skew. **[7]**

c) Draw and explain the architecture of FPGA XC4000 series with neat diagram. **[7]**

Q3) a) Explain CMOS inverter circuit with neat diagram and plot voltage transfer characteristics. **[8]**

b) Explain static and dynamic power dissipation analysis of CMOS inverter circuit. **[8]**

OR

Q4) a) Explain in detail latch up effect, latch up prevention techniques and comment on system level approach to avoid latch ups. **[8]**

b) Draw circuit diagram of transmission gate and explain in detail. **[8]**

P.T.O.

Q5) a) Write in detail lambda rules with diagram. **[10]**

b) Explain cross talk in detail. **[8]**

OR

Q6) a) Write in detail micron based design rules. **[10]**

b) Write short note on Layout Vs Schematic and Explain LVS checking process. **[8]**

Q7) a) What is JTAG, explain in detail. **[8]**

b) Explain Built in Self Test (BIST). **[8]**

OR

Q8) a) Draw and explain architecture of TAP controller. **[8]**

b) Describe types of faults? Explain with schematics. **[8]**

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