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Seat No.	
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[5352]-573

S.E. (IT) (I Sem.) EXAMINATION, 2018

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2015 PATTERN)

Time : Two Hours

Maximum Marks : 50

N.B. :— (i) Answer Q. Nos. 1 or 2, 3 or 4, 5 or 6 and 7 or 8.
(ii) Neat diagram must be drawn wherever necessary.
(iii) Assume suitable data, if necessary.

1. (a) Do the following [6]
 - (i) $(27.50)_2 - (68.75)_2$ Using 2's complement method.
 - (ii) Convert the decimal number 25 into Binary format, Excess -3 format and BCD format
 - (b) Design Full subtractor circuit using decoder IC 74138 [6]
- OR**
- 2 (a) Define following terms related to logic families [6]
 - (i) Power dissipation
 - (ii) Fan-in
 - (iii) Fan-out
 - (iv) Noise margin
 - (v) Propagation delay
 - (vi) Figure of Merit
 - (b) Draw and explain 4 bit BCD adder using IC 7483. [6]
- 3 (a) Compare Asynchronous counter with Synchronous counter. Design MOD 11 up counter using IC 74191. [6]
 - (b) Draw and explain 4 bit Ring counter. Write the Truth Table for same showing all possible states if initial state is 1100. [6]

P.T.O.

OR

- 4 (a) Design and draw MOD 56 counter using IC 7490 and explain its operation. [6]
(b) Draw and explain 4 bit SISO and SIPO shift register. Give applications of each. [6]
- 5 (a) Draw ASM chart for 2bit binary up counter with mode control input M such that [7]
For M = 1 Counter counts Up
For M = 0 Counter holds present state.
Design the circuit using multiplexer controller method.
(b) Design 4:1 multiplexer using suitable PAL [6]

OR

- 6 (a) Design 3 bit Binary to Gray code converter using suitable PLA [7]
(b) Draw and explain Internal Architecture of CPLD in detail. [6]
- 7 (a) What is VHDL? Explain components of VHDL in detail with example of 2 input [6]
AND gate.
(b) Write VHDL code (Entity and Architecture) for 4:1 Multiplexer using Dataflow [7]
modeling method
- OR**
- 8 (a) Compare sequential and concurrent statements in VHDL with suitable example [6]
(b) Write VHDL code (Entity and Architecture) in Behavior modeling style for 2 bit [7]
synchronous up/down counter. Consider
Mode = 0 Up counting
Mode = 1 Down counting