Total No. of Questions—**8**] [Total No. of Printed Pages—**3**

Seat No.	

[5252]-536

S.E. (E&TC/Electronics) (Second Semester) EXAMINATION, 2017

INTEGRATED CIRCUITS

(2015 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. **:—** (*i*) Answer Q. **1** *or* Q. **2**, Q. **3** *or* Q. **4**, Q. **5** *or* Q. **6** and Q. **7** *or* Q. **8**.

(*ii*) Neat diagrams must be drawn wherever necessary.

(*iii*) Figures to the right side indicate full marks.

(*iv*) Use of calculator is allowed.

(*v*) Assume suitable data if necessary.

1. (*a*) Justify, how constant current source is used in place of R_E to improve CMRR for differential amplifier. [6]

(*b*) Draw neat circuit diagram of three Op-amp Instrumentation amplifier and derive its output equation. [6]

Or

2. (*a*) An emitter biased Dual input balanced output differential amplifier has the following specifications :

V_{CC} = ± 10 V, R_{C1} = R_{C2} = 3.7 kΩ and R_E = 4.2 kΩ, β_{ac} = β_{dc} = 100 & V_{BE}, = 0.7 V. Calculate : [6]

(1) Voltage Gain (Ad)

(2) Input Resistance (Ri)

(3) Output Resistance (Ro).

P.T.O.

(*b*) Draw the circuit diagram of Practical differentiator along with frequency response and explain its operation. [6]

3. (*a*) Explain with a neat circuit diagram working of inverting precession full wave rectifier with its waveform. [6]

(*b*) With neat circuit diagram, explain voltage to current converter with grounded load. [6]

Or

4. (*a*) Draw and explain circuit of Sample and Hold circuit using Op-amp with its waveform. [6]

(*b*) The output of 8-bit ADC with all 1's when V_i = 5 V, find its :

(1) Resolution

(2) Digital output code, If V_i = 1.7 V. [6]

5. (*a*) Define the term "Lock range", "Capture range" and "Free running frequency" and explain transfer characteristics of PLL. [7]

(*b*) Design a first order low pass filter with higher cut-off frequency of 1 kHz with pass gain '2'. Draw the designed circuit diagram. Assume C = 0.1 μ_f and R_f = 10 kΩ. [6]

Or

6. (*a*) With the help of neat circuit diagram explain the operation of Wien bridge oscillator. [6]

(*b*) Design a wide bandpass filter having f_L = 400 Hz, f_H = 2 kHz and pass band 4. Also calculate the bandwidth. [7]

Assume : C' = 0.01 μ*f* and C = 0.05 μ*f*

R_1' = 10 kΩ and R_1 = 10 kΩ

7. (*a*) Calculate output frequency 'f_0', Lock range 'Δf_L', Capture range 'Δf_C' of a PLL, If R_T = 1 kΩ, C_T = 0.1 μf, filter capacitor C = 1 μf and internal resistance = 3.6 kΩ. Asuume ± V = 10V. [6]

(*b*) Design all pass filters with a phase shift of –135°. At a frequency of 2 kHz at the output. Draw detailed designed circuit diagram. Assume C = 0.1 μf and R_1 = 10 kΩ. [7]

Or

8. (*a*) Write short notes on application of PLL : [6]

(1) Frequency Multiplier

(2) FM Demodulator.

(*b*) Design a first order high pass filter with higher cut-off frequency of 10 kHz with pass gain '1.5'. Draw the designed circuit diagram. Assume C = 0.01 μ*f* and R_1 = 10 kΩ. [7]