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## S.E. (E & TC/Electronics) (I Sem.) EXAMINATION, 2019 DIGITAL ELECTRONICS (2015 PATTERN)

Time: Two Hours Maximum Marks: 50

## Instructions to the candidates:

- 1) Attempt Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.
- 4) Assume suitable data, if necessary.
- 5) Use of logarithmic tables, slide rule and electronic non programmable calculator is allowed.

Q1	a.	Design 3 bit binary to grey code converter	06
	b	Convert D F/F to J/K F/F	06
		OR OR	
Q2	а	Design Even bit parity checker	06
	b	Design 3 bit twisted ring counter	06
			3
Q3	а	Design sequence detector to detect10110	06
	b	Give comparisons between TTL, ECL and CMOS logic families	04
	С	Draw and explain SR Flip Flop using NAND gates.	02
		OR OR	
Q4	а	Draw and explain TTL to CMOS interface.	06
	b	Compare Moor and Mealy Machine	04
	c	What is Clock Skew and Clock jitter?	02
Q5	а	Implement following using PLA	06
		F1 = AB'+AC+A'BC'	
		F2 = (AC+BC)	
	b	List Various semiconductor memory with their characteristic.	07

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Q6	а	Explain PROM with diagram	06
	b	List Various Programmable logic Devices with their characteristic	07
Q7	а	List & explain Mode of Timer/ Counter for 8051	0.5
Ų,	b	Write short note on 8051 feature	05 04
	С	Mention any four addressing modes of 8051?	
	C	OR	04
Q8	а	Draw and explain Program Status Word	05
~~	b	Compare Microcontroller & Microprocessor	04
	c	Explain the Instruction for arithmetic's with examples	04
	Ü	Supplemental designation of distance of with examples	04
		Explain the Instruction for arithmetic's with examples	
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		Draw and explain Program Status Word Compare Microcontroller & Microprocessor Explain the Instruction for arithmetic's with examples	•

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