**MICROPROCESSORS AND INTERFACING**

Project

***IC Tester***



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Project submitted in partial fulfilment of the requirements of the course **Microprocessors and Interfacing**

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**Problem Statement**

**Q2: IC TESTER**

Design a Microprocessor based Tester to test the logical functioning of the following chips:

1. 7400

2. 7408

3. 7432

4. 7486

5. 747266

The IC to be tested will be inserted in a 14 pin ZIF socket. The IC number is to be entered via a keyboard.

The keyboard has keys 0-9, backspace, enter and test.

The user places the IC in the ZIF socket closes it – then enters the IC No, followed by enter key.

The IC No. is displayed on the 7-segment display.

The testing will start once the user presses test key.

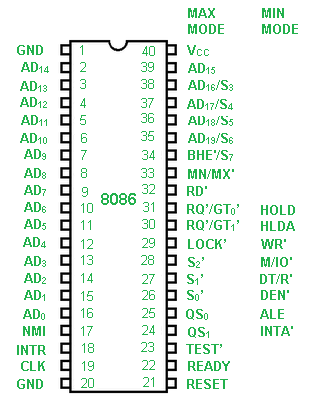
After Test the result PASS/FAIL must be displayed on the 7-segment display.

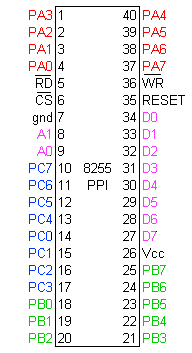
**Assumptions Made**

* The Test key performs its function only after the Enter key is pressed.
* The user cannot enter digits while PASS/FAIL is being displayed.
* The ALP has been made assuming that there is no debounce when a key is pressed in Proteus.

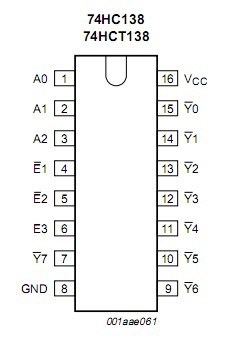
**Components Used**

1. **8086** Microprocessor - 1 No
2. **8255-A** (Programmable Peripheral Interface with 24 I/O lines) - 2 Nos
3. **74HC138** (3:8 Decoder) - 3 Nos
4. **74HC245** (Octal BUS transceivers with tri-state output) - 2 Nos
5. **74HC373** (Octal D-Type transparent latches with tri-state outputs) - 3 Nos
6. **7SEG-MPX6-CA-BLUE** (6 Digit, 7-Segment Anode Display) -1 No
7. **6116** (16K <2Kx8> Static RAM)- 2 Nos
8. **2732** (32K <4Kx8> EPROM)- 4 Nos
9. **BUTTON** (SPST Push Button)- 16 Nos
10. **SW- SPDT-MOM** (Interactive SPDT Switch with Momentary Action)
11. **7400** (Quadruple 2-input positive NAND gates)
12. **7408** (Quadruple 2-input positive AND gates)
13. **7432** (Quadruple 2-input positive OR gates)
14. **7486** (Quadruple 2-input exclusive OR gates)
15. **747266** (Quadruple 2-input exclusive NOR gates)
16. Simple 2-Input AND gate - 1 Nos
17. Simple 2-Input OR gate - 4 Nos
18. Simple digital Inverter - 2 Nos
19. **8284** (Clock generator chip implemented in proteus using the internal clock of 8086)
20. **ZIF Socket** (Designed using ‘Default’ Terminals in Proteus)

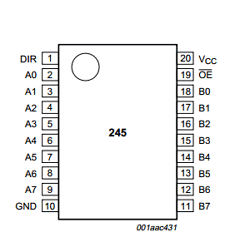
**8086 Microprocessor**

**8255A -** Programmable Peripheral Interface with 24 I/O lines****

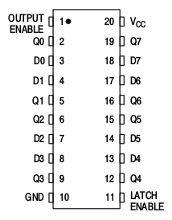
**74HC138 -** 3:8 Decoder



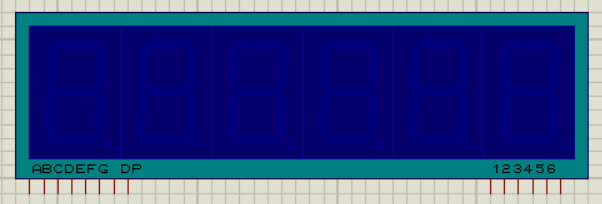
**74HC245 -** Octal BUS transceivers with tri-state output

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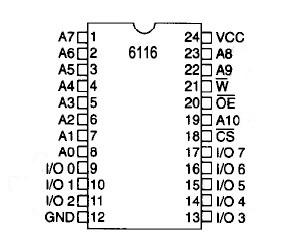
**74HC373 -** Octal D-Type transparent latches with tri-state outputs



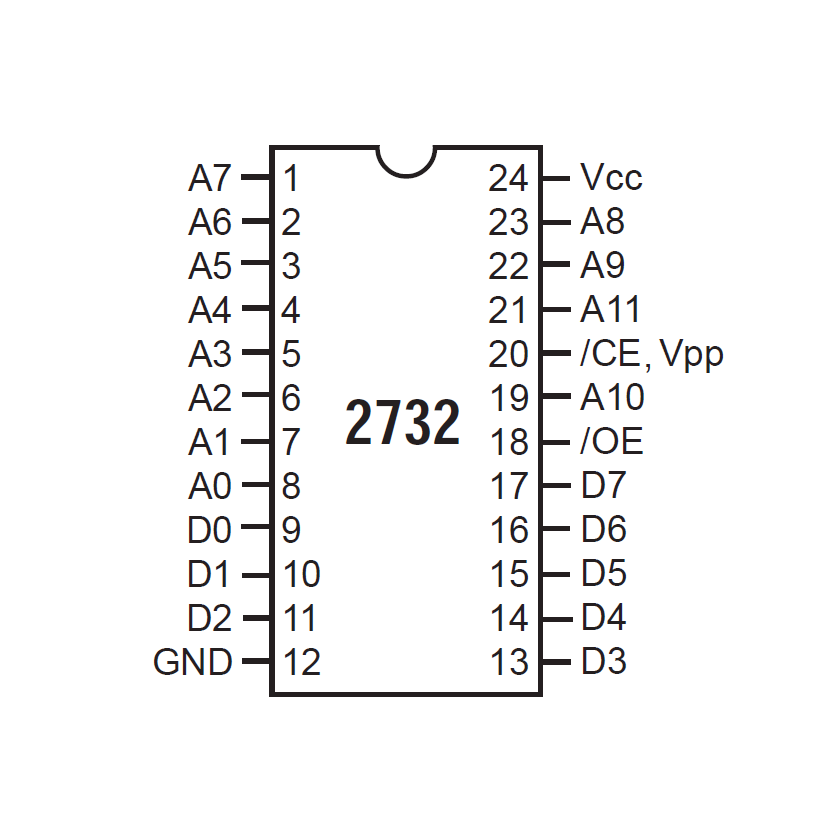
**7SEG MPX6 CA BLUE** - 6 Digit, 7-Segment Anode Display



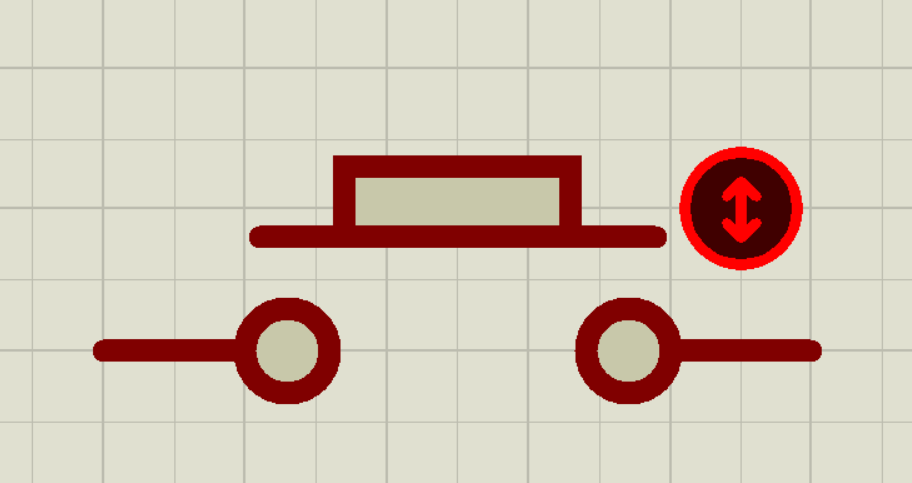
**6116** - 16K <2Kx8> Static RAM



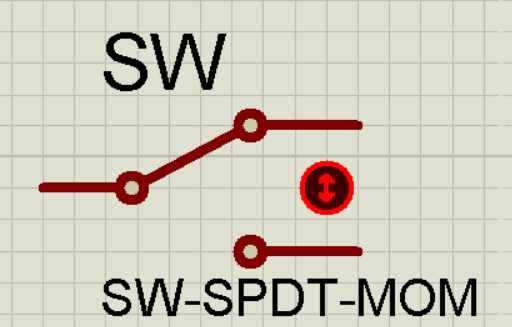
**2732** - 32K <4Kx8> EPROM



**BUTTON** - SPST Push Button

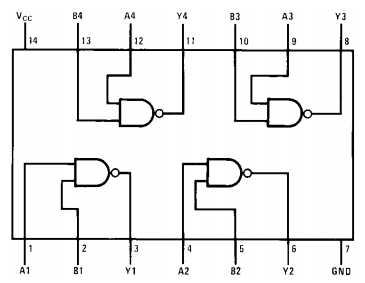


**SW SPDT MOM** - Interactive SPDT Switch with Momentary Action

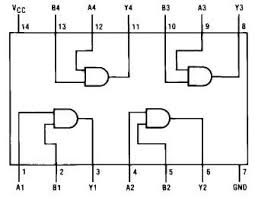


**ZIF Socket** - Designed using ‘Default’ Terminals in Proteus****

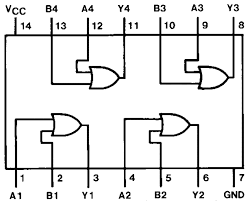
**7400** - Quadruple 2-input positive NAND gates

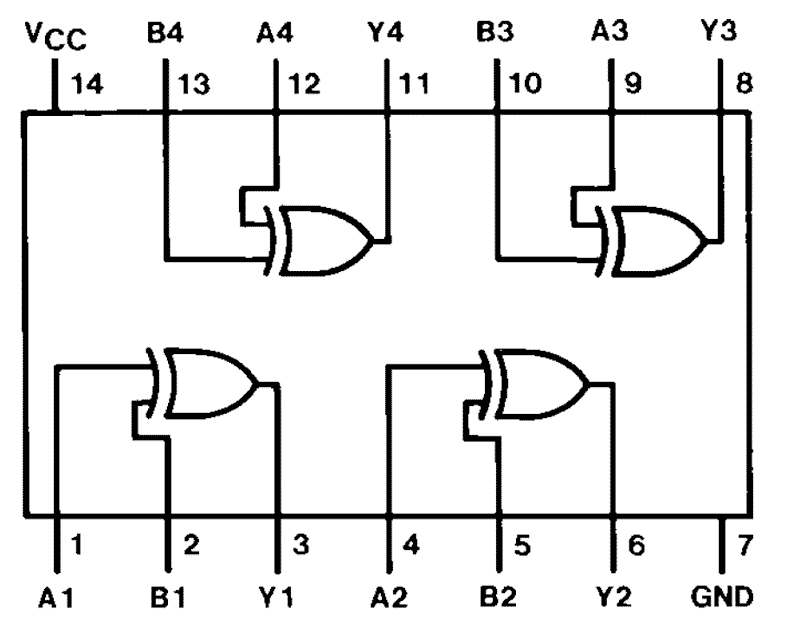


**7408** - Quadruple 2-input positive AND gates

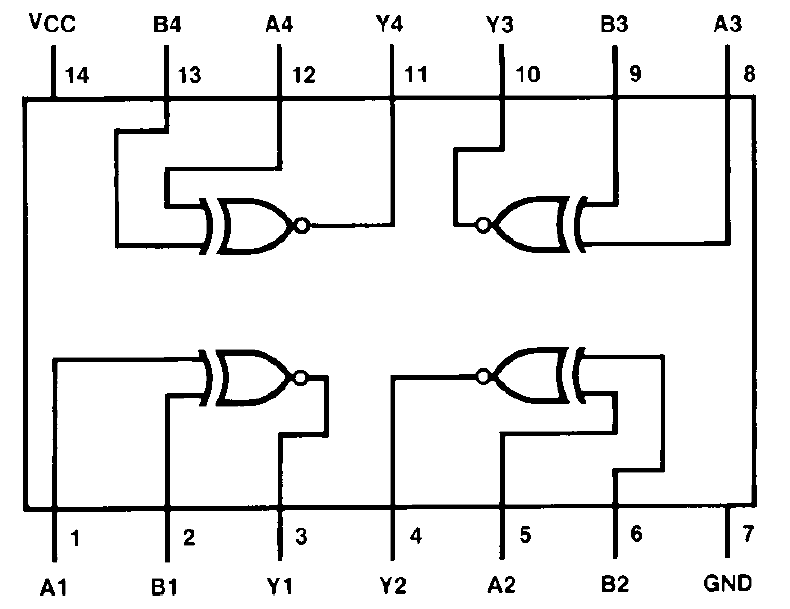


**7432** - Quadruple 2-input positive OR gates

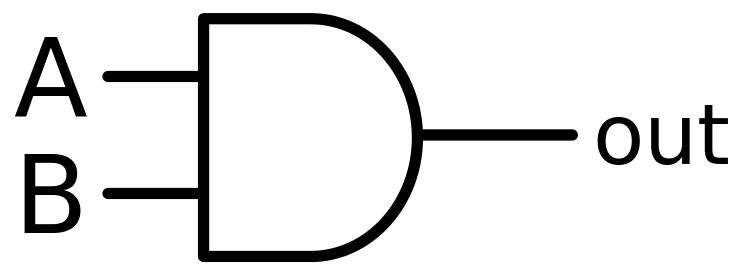


**7486** - Quadruple 2-input exclusive OR gates

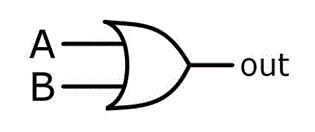
**747266** - Quadruple 2-input exclusive NOR gates



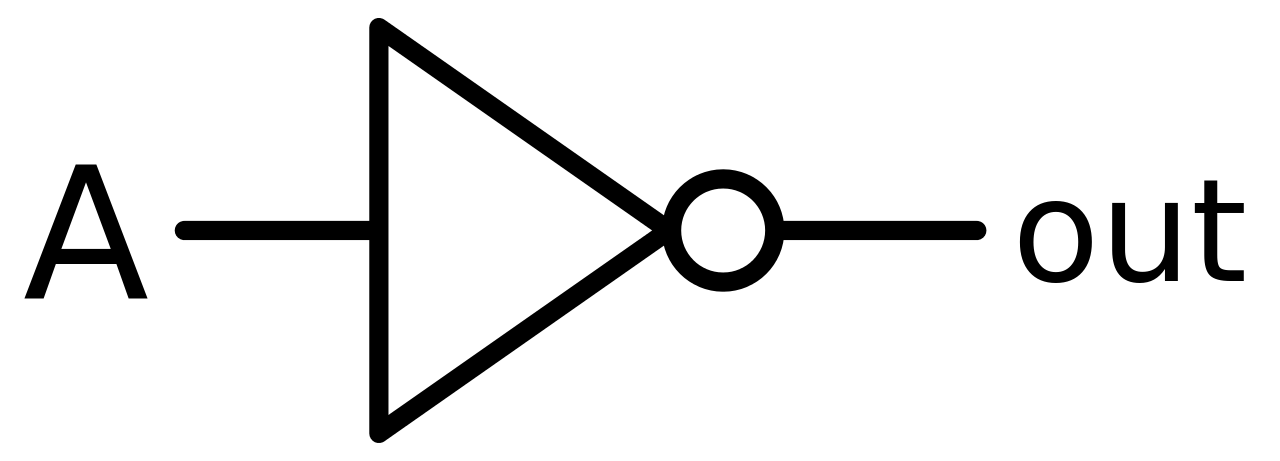
**Simple 2-Input AND gate**

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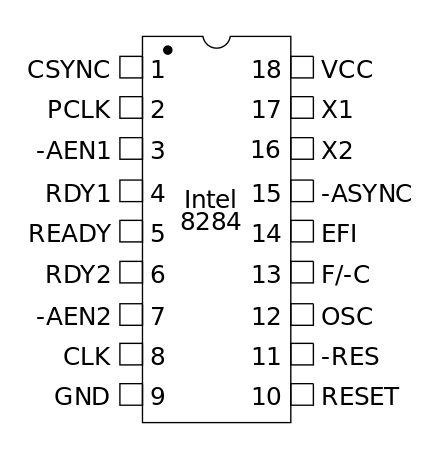
**Simple 2-Input OR gate**

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**Simple digital Inverter**

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**8284** - Clock generator chip implemented in proteus using the internal clock of 8086

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**Design Specifications**

The following ICs can be tested: 7400, 7408, 7432, 7486 and 747266. The IC to be tested will be inserted in a 14 pin ZIF socket. This has been implemented in Proteus using default terminals in the format of a ZIF socket.

The user enters the IC number using a keyboard having keys 0-9, backspace, enter and test. A maximum of 6 numbers can be entered.

The numbers entered by the user will be displayed on the 6-digit seven segment display.

Backspace can be used to erase the previous number entered. No action will take place if there are no numbers being displayed.

After entering the IC number, the user will press the enter key. Upon pressing enter, no input will be taken, except for the test key.

The testing will start once the user presses the test key.

After testing is completing, PASS/FAIL is displayed on the 7-segment display for approx. 4 seconds. During this time, no input on the keyboard will be taken from the user.

After approx. 4 seconds, the PASS/FAIL will be cleared and the IC tester is now ready to take another input from the user.

**Interfacing and I/O Port Allocation**

**Memory Interfacing**

The following memory chips have been used :

* 2732 - 32K (4K x 8) = 4KB EPROM each - 2 banks starting at 00000H
* 6116 - 16K (2K x 8) = 2KB Static RAM each - 2 banks starting at 02000H
* 2732 - 32K (4K x 8) = 4KB EPROM each - 2 banks starting at FE000H

**Memory Allocation:**

ROM1(Even) - 00000H, 00002H, 00004H …., 01FFEH

ROM1(Odd) - 00001H, 00003H, 00005H, …., 01FFFH

RAM1(Even) - 02000H, 02002H, 02004H, …., 02FFEH

RAM1(Odd) - 02001H, 02003H, 02005H, …., 02FFFH

ROM2(Even) - FE000H, FE002H, FE004H, …., FFFFEH

ROM2(Odd) - FE001H, FE003H, FE005H, …., FFFFFH

**ROM1 - 00000H -> 01FFFH**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A9 | …. | A0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ... | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | ... | 1 |

**RAM1 - 02000H -> 02FFFH**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A9 | …. | A0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | ... | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | ... | 1 |

**ROM2 - FE000H -> FFFFFH**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A9 | …. | A0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | ... | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | …. | 1 |

**NOTE** : Here we see that address lines A13, A14 and A15 are unique for every component. Hence, we use these lines as select lines to our decoders for the memory banks.

**I/O Interfacing**

We have used two 8255As for our I/O devices.

The addresses allocated are :

1. 8255A-1 :
   1. Port A - 00H
   2. Port B - 02H
   3. Port C - 04H
   4. Control Register - 06H

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

1. 8255A-2 :
   1. Port A - 10H
   2. Port B - 12H
   3. Port C - 14H
   4. Control Register - 16H

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |

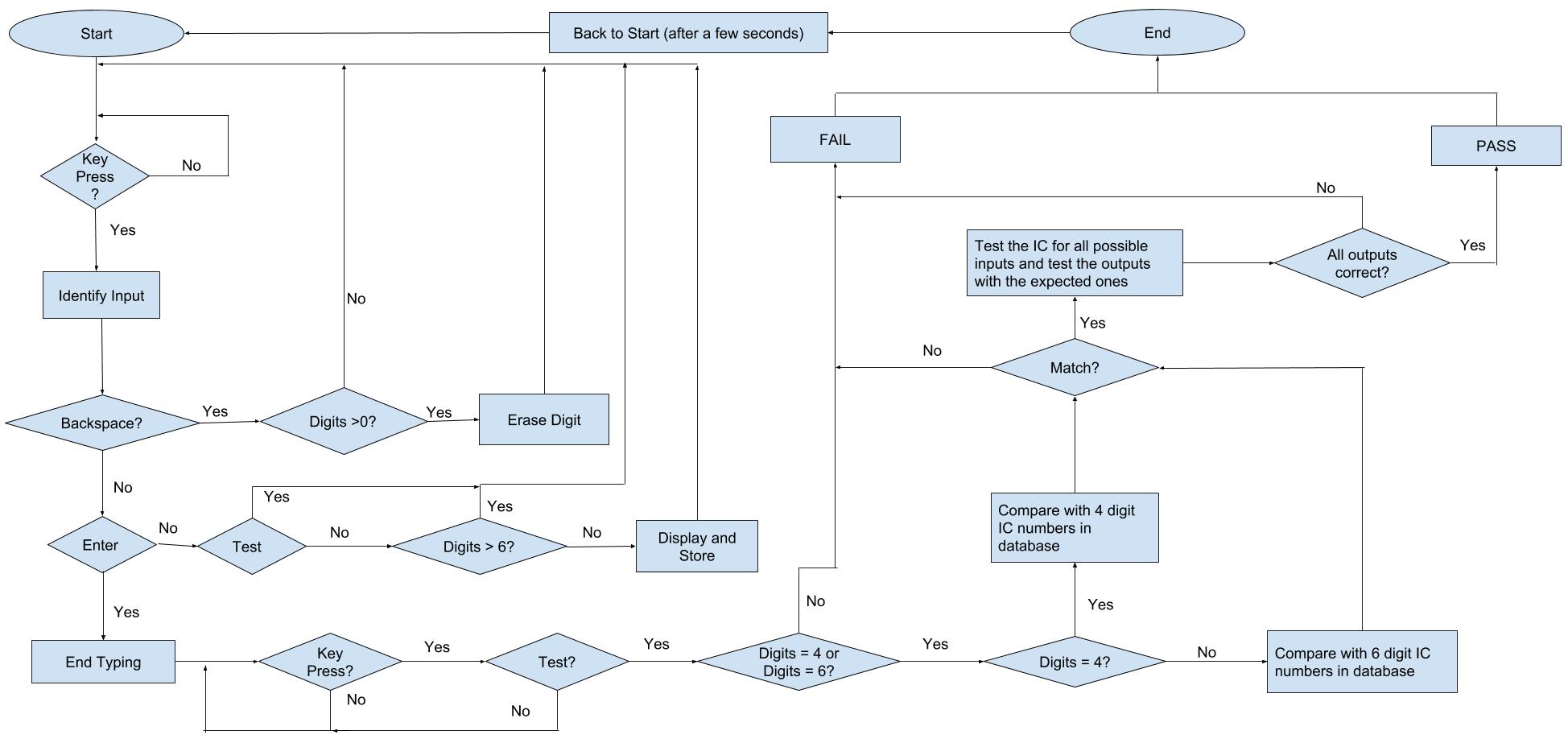
**NOTE** : As we can see that A3, A4 and A5 have different values for the two different 8255s, but they share the same values for the different ports of the same 8255. Hence, we use these as our select lines in our decoder for the I/O devices.

**Port Allocation**

1. 8255A-1 :
   1. Port A - 8 pins as outputs from the 8255, which are the inputs to the 7-segment display
   2. Port B - 6 pins as outputs from the 8255, which are the enables to each 7-segment display
   3. Port C -
      1. Port C-lower - 4 pins as outputs from the 8255, inputs to the keyboard
      2. Port C-upper - 4 pins as inputs to the 8255, outputs from the keyboard.
2. 8255A-2:
   1. Port A - 6 pins as outputs from the 8255, which are inputs to the ZIF socket pins: P1, P2, P12, P13, P5 and P9.
   2. Port B - 2 pins as inputs to the 8255, which are outputs from the ZIF socket pins: P3 and P11.
   3. Port C -
      1. Port C-lower - 2 pins: P4 and P10.
      2. Port C-upper - 2 pins: P6 and P8.

**NOTE** : Logic of 8255A-2

There are 5 types of logic ICs in our database (7400, 7408, 7432, 7486 and 747266). Of these 5 ICs, 4 of them share the same pins in terms of outputs and inputs to the IC. But the IC 747266 shares the same pins for only 2 of the gates, while the other two are inverted. The pins P1, P2, P12, P13, P5 and P9 are always inputs to the logic gates, so Port-A is always output from the port, the pins P3 and P11 are always outputs from the logic gates, so Port-B is always input to the port. When the first 4 logic ICs are being tested, pins P4 and P10 are inputs to the logic gates and pins P6 and P8 are outputs from the logic gates, hence the Port-C-Lower is output from the port and the Port-C-Upper is the input to the port. But when the 747266 IC is being tested, pins P6 AND P8 are inputs to the logic gates and pins P4 and P10 are outputs from the logic gates, hence the the two half ports of Port-C switch roles.

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