```verilog
// Q. Assume timescale to be 1ps/1ps.Generate a 25MHz square wave for the signal clk


//solution. Time Period=(1/frequency)=(1/(25X10^6)=40 nano-seconds

//testbench code :-
module tb;
  reg clk;
  always begin
    clk=1'b0;
    #20;
    clk=1'b1;
    #20;
  end
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars;
    #200;
    $finish();

  end
endmodule
```