```
testbench.sv
```

```
1 // Q. Generating 9MHz square waveform for signal sclk,assuming timescale 1ns and 3 digit precision
4 //solution. Time Period=(1/frequency)=(1/(9X10^6)=111.111 nano-seconds
5 //Half Time Period=(time period)/2=55.555 ns
7 //testbench code :-
   timescale 1ns/1ps
9 module tb;
    reg sclk=1'b0;
11
    always #55.555 sclk=~sclk;
12
    initial begin
      $dumpfile("dump.vcd");
13
14
      $dumpvars;
      #200:
15
      $finish();
16
17
18
    end
19 endmodule
```

```
Share

    Log

# KERNEL: Time resolution set to 1ps.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
# SLP: Elaboration phase ... done : 0.0 [s]
# SLP: Generation phase ...
# SLP: Generation phase ... done : 0.0 [s]
# SLP: Finished : 0.1 [s]
# SLP: 0 primitives and 2 (100.00%) other processes in SLP
# SLP: 1 (100.00%) signals in SLP and 0 interface signals
# ELAB2: Elaboration final pass complete - time: 0.1 [s].
# KERNEL: SLP loading done - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of simulation is reduced.
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: SLP simulation initialization done - time: 0.0 [s].
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 4665 kB (elbread=427 elab2=4104 kernel=134 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# RUNTIME: Info: RUNTIME_0068 testbench.sv (16): $finish called.
# KERNEL: Time: 200 ns, Iteration: 0, Instance: /tb, Process: @INITIAL#12_1@.
# KERNEL: stopped at time: 200 ns
# VSIM: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
Finding VCD file...
./dump.vcd
[2023-07-18 18:34:19 UTC] Opening EPWave...
Done
```

```
→Code:-
```

endmodule

// Q. Generating 9MHz square waveform for signal sclk,assuming timescale 1ns and 3 digit precision

```
//solution. Time Period=(1/frequency)=(1/(9X10^6)=111.111 nano-seconds
//Half Time Period=(time period)/2=55.555 ns

//testbench code :-

'timescale 1ns/1ps

module tb;

reg sclk=1'b0;

always #55.555 sclk=~sclk;

initial begin

$dumpfile("dump.vcd");

$dumpvars;

#200;

$finish();
```