A Neural-Network-Based Space-Vector PWM Controller for a Three-Level Voltage-Fed Inverter Induction Motor Drive

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***Abstract*—A neural-network-based implementation of space-vector modulation (SVM) of a three-level voltage-fed inverter is proposed in this paper that fully covers the linear undermodulation region. A neural network has the advantage of very fast implementation of an SVM algorithm, particularly when a dedicated application-specific IC chip is used instead of a digital signal processor (DSP). A three-level inverter has a large number of switching states compared to a two-level inverter and, therefore, the SVM algorithm to be implemented in a neural network is considerably more complex. In the proposed scheme, a three-layer feedforward neural network receives the command voltage and angle information at the input and generates symmetrical pulsewidth modulation waves for the three phases with the help of a single timer and simple logic circuits. The artificial-neural-network (ANN)-based modulator distributes switching states such that neutral-point voltage is balanced in an open-loop manner. The frequency and voltage can be varied from zero to full value in the whole undermodulation range. A simulated DSP-based modulator generates the data which are used to train the network by a backpropagation algorithm in the MATLAB Neural Network Toolbox. The performance of an open-loop volts/Hz speed-controlled induction motor drive has been evaluated with the ANN-based modulator and compared with that of a conventional DSP-based modulator, and shows excellent performance. The modulator can be easily applied to a vector-controlled drive, and its performance can be extended to the overmodulation region.**

***Index Terms*—Induction motor drive, neural network, space-vector pulsewidth modulation, three-level inverter.**

I. Introduction

THREE-LEVEL insulated-gate-bipolar-transistor (IGBT)- or gate-turn-off-thyristor (GTO)-based voltage-fed converters have recently become popular for multimegawatt drive applications because of easy voltage sharing of devices and superior harmonic quality at the output compared to the conventional two-level converter at the same switching frequency. Space-vector pulsewidth modulation (PWM) has recently grown as a very popular PWM method for voltage-fed converter ac drives because it offers the advantages of improved PWM quality and extended voltage range in the undermodulation region. A difficulty of space-vector modulation (SVM) is that it requires complex and time-consuming online computation by a digital signal processor (DSP) [1]. The online computational burden of a DSP can be reduced by using lookup tables. However, the lookup table method tends to give reduced pulsewidth resolution unless it is very large.

The application of artificial neural networks (ANNs) is recently growing in the power electronics and drives areas. A feedforward ANN basically implements nonlinear input–output mapping. The computational delay of this mapping becomes negligible if parallel architecture of the network is implemented by application-specific IC (ASIC) chip. A feedforward carrier-based PWM technique, such as SVM, can be looked upon as a nonlinear mapping phenomenon where the command phase voltages are sampled at the input and the corresponding pulsewidth patterns are established at the output. Therefore, it appears logical that a feedforward backpropagation-type ANN which has high computational capability can implement an SVM algorithm. Note that the ANN has inherent learning capability that can give improved precision by interpolation unlike the standard lookup table method.

This paper describes feedforward ANN-based SVM implementation of a three-level voltage-fed inverter. In the beginning, SVM theory for a three-level inverter is reviewed briefly. The general expressions of time segments of inverter voltage vectors for all the regions have been derived and the corresponding time intervals are distributed so as to get symmetrical pulse widths and neutral-point voltage balancing. Based on these results, turn-on time expressions for switches of the three phases have been derived and plotted in different modes. A complete modulator is then simulated, and the simulation results help to train the neural network. The performance of a complete volts/Hz-controlled drive system is then evaluated with the ANN-based SVM and compared with the equivalent DSP-based drive control system. Both static and dynamic performance appear to be excellent.

II. SVM Strategy for Neural Network

Neural-network-based SVM for a two-level inverter has been described in the literature [2], [3]. It will now be extended to a

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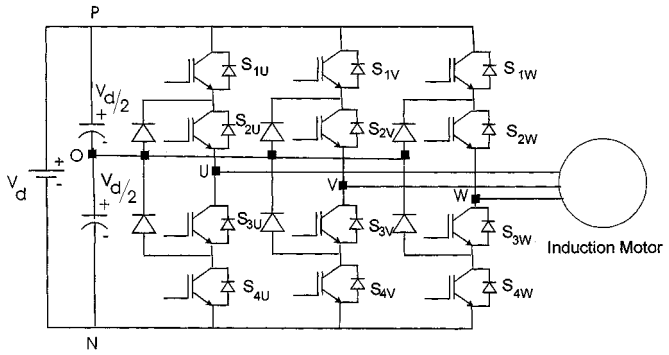

Fig. 1. Schematic diagram of three-level inverter with induction motor load.

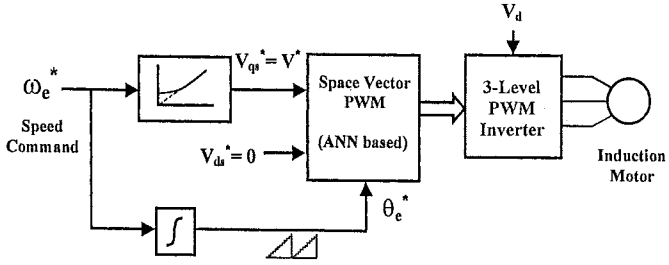

Fig. 2. Open-loop volts/Hz speed control using the proposed neural-network-based PWM controller.

three-level inverter. Of course, the SVM implementation for a three-level inverter is considerably more complex than that of a two-level inverter [1], [4]–[7]. Fig. 1 shows the schematic diagram of a three-level IGBT inverter with induction motor load. For ac–dc–ac power conversion, a similar unit is connected at the input in an inverse manner. The phase U, for example, gets the state P (positive bus voltage) when the switches S_{1U} and S_{2U} are closed, whereas it gets the state N (negative bus voltage) when S_{3U} and S_{4U} are closed. At neutral-point clamping, the phase gets the O state when either S_{2U} or S_{3U} conducts depending on positive or negative phase current polarity, respectively. For neutral-point voltage balancing, the average current injected at O should be zero. Fig. 2 shows the volts/Hz-controlled induction motor drive with the proposed ANN-based space-vector PWM which will be described later. The neural network receives the voltage ($V_{qs}^* = V^*$) and angle (θ_e^*) signals at the input as shown, and generates the PWM pulses for the inverter. For a vector-controlled drive with synchronous current control, the ANN will have an additional voltage component (V_{ds}^*), which is shown to be zero in this case. The switching states of the inverter are summarized in Table I, where U, V, and W are the phases and P, N, and O are dc-bus points, as indicated before. Fig. 3(a) shows the representation of the space voltage vectors for the inverter, and Fig. 3(b) shows the same figure with $3^3 = 27$ switching states indicating that each phase can have P, N, or O state. There are 24 active states and the remaining are zero states (PPP, OOO, and NNN) that lie at the origin. Evidently, neutral current will flow through the point O in all the states except the zero states and outer hexagon corner states. As shown in Fig. 3(a), the hexagon has six sectors (A–F) as shown and each sector has four regions (1–4), giving altogether 24 regions of

TABLE I
SWITCHING STATES OF THE INVERTER ($X = U, V, W$)

Switching States	S_{1X}	S_{2X}	S_{3X}	S_{4X}	V_{XO}
P	ON	ON	OFF	OFF	$+V_d/2$
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	$-V_d/2$

operation. The inner hexagon covering region 1 of each sector is highlighted. The command voltage vector (V^*) trajectory, shown by a circle, can expand from zero to that inscribed in the larger hexagon in the undermodulation region. The maximum limit of the undermodulation region is reached when the modulation factor $m \leq 0.907$ where $m = V^*/V_{1\text{sw}}$ (V^* = command or reference voltage magnitude and $V_{1\text{sw}}$ = peak value of phase fundamental voltage at square-wave condition). Note that a three-level inverter must operate below the square-wave ($m < 1.0$) condition.

A. Operation Modes and Derivation of Turn-On Times

In this paper, as indicated in Fig. 3(a), mode 1 is defined if the V^* trajectory is within the inner hexagon, whereas mode 2 is defined for operation outside the inner hexagon. In a hybrid mode (covering modes 1 and 2), the V^* trajectory will pass through regions 1 and 3 of all the sectors. In space-vector PWM, the inverter voltage vectors corresponding to the apexes of the triangle which includes the reference voltage vector are generally selected to minimize harmonics at the output. Fig. 3(c) shows the sector A triangle formed by the voltage vectors V_0, V_2 and V_5. If the command vector V^* is in region 3 as shown, the following two equations should be satisfied for space-vector PWM:

$$V_1 T_a + V_3 T_b + V_4 T_c = V^* T_s/2 \tag{1}$$

$$T_a + T_b + T_c = T_s/2 \tag{2}$$

where T_a, T_b, and T_c are the respective vector time intervals and T_s = sampling time. Table II shows the analytical time expressions for T_a, T_b, and T_c for all the regions in the six sectors where θ_e = command voltage vector angle [see Fig. 3(c)] and $n = \sqrt{3}V^*/V_d$ (V^* = command voltage and V_d = dc-link voltage). These time intervals are distributed appropriately so as to generate symmetrical PWM pulses with neutral-point voltage balancing. Table III shows the summary of selected switching sequences of phase voltages for all the regions in the six sectors [4]. Note that the sequence in opposite sectors (A–D, B–E, and C–F) is selected to be of a complimentary nature for neutral-point voltage balancing. Fig. 4 shows the corresponding PWM waves of the three phases in all the four regions of sector A. Each switching pattern during $T_s/2$ is repeated inversely in the next $T_s/2$ interval with appropriate segmentation of T_a, T_b, and T_c intervals in order to generate symmetrical PWM waves. The figure also indicates, for example, turn-on time of P ($T_{UP\text{-ON}}$) and N ($T_{UN\text{-ON}}$) states of phase voltage U in mode 1. These wave patterns are, respectively, defined as pulsed and notched waves. It can be shown that similar wave patterns are also valid for the sectors C and E (odd sector). If PWM waves are plotted in the even sector (B, D or F), it can be shown that P states appear as notched waves whereas N states appear as

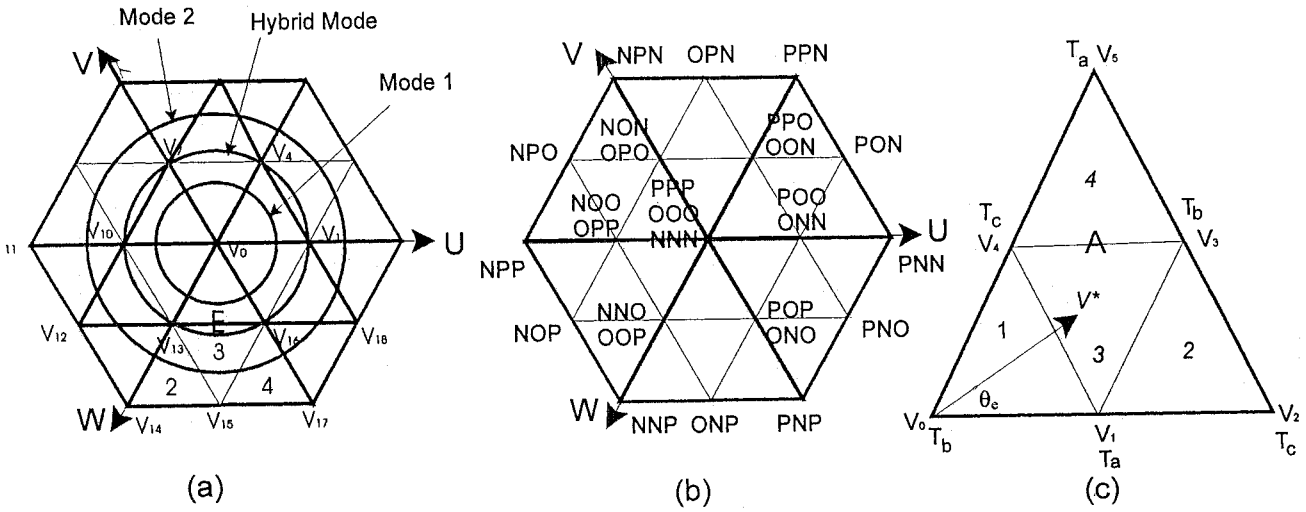

Fig. 3. Space voltage vectors of a three-level inverter. (a) Space-vector diagram showing different sectors and regions. (b) Space-vector diagram showing switching states. (c) Sector A space vectors indicating switching times.

pulsed waves. The turn-on times for different phases can be derived with the help of Table II and Fig. 4 for all the regions in the six sectors. For example, the phase-U turn-on time expressions in mode 1 can be derived as

$$T_{UP\text{-ON}}=\begin{bmatrix} \frac{3T_s}{8}-KV^*\sin\left(\theta_e+\frac{\pi}{3}\right), & \text{for } S=A \\ \frac{3T_s}{8}-KV^*\sqrt{3}\cos(\theta_e), & \text{for } S=B \\ \frac{3T_s}{8}+KV^*\sin\left(\theta_e-\frac{\pi}{3}\right), & \text{for } S=C \\ \frac{3T_s}{8}-KV^*\sin\left(\theta_e+\frac{\pi}{3}\right), & \text{for } S=D \\ \frac{3T_s}{8}-KV^*\sqrt{3}\cos(\theta_e), & \text{for } S=E \\ \frac{3T_s}{8}+KV^*\sin\left(\theta_e-\frac{\pi}{3}\right), & \text{for } S=F \end{bmatrix} \tag{3}$$

$$T_{UN\text{-ON}}=\begin{bmatrix} \frac{3T_s}{8}+KV^*\sin\left(\theta_e+\frac{\pi}{3}\right), & \text{for } S=A \\ \frac{3T_s}{8}+KV^*\sqrt{3}\cos(\theta_e), & \text{for } S=B \\ \frac{3T_s}{8}-KV^*\sin\left(\theta_e-\frac{\pi}{3}\right), & \text{for } S=C \\ \frac{3T_s}{8}+KV^*\sin\left(\theta_e+\frac{\pi}{3}\right), & \text{for } S=D \\ \frac{3T_s}{8}+KV^*\sqrt{3}\cos(\theta_e), & \text{for } S=E \\ \frac{3T_s}{8}-KV^*\sin\left(\theta_e-\frac{\pi}{3}\right), & \text{for } S=F \end{bmatrix} \tag{4}$$

where $K=\sqrt{3}T_s/4V_d$ and S denotes the sector name.

Similarly, the corresponding expressions for mode 2 can be derived as shown in (5) and (6), shown at the bottom of the next page, where R indicates the region number. Similar equations can also be derived for V and W phases. Because of waveform symmetry, the turn-off times (see Fig. 4) can be given as

$$T_{UP\text{-OFF}}=T_s-T_{UP\text{-ON}} \tag{7}$$

$$T_{UN\text{-OFF}}=\frac{T_s}{2}-T_{UN\text{-ON}} \tag{8}$$

and the corresponding P and N state pulsewidths are evident from the figure. The remaining time interval in a phase corresponds to zero state as indicated. Equations (3) and (4) can be expressed in the general form

$$T_{U\text{-ON}}=T_B+V^*g(\theta_e) \tag{9}$$

where $T_B=3T_s/8$ is the bias time and $g(\theta_e)$ = turn-on signal at unit voltage. Fig. 5 shows the plot of (9) for both P and N states at several magnitudes of V^*. Mode 1 ends when the curves reach the saturation level $T_s/2$. Both the $g(\theta_e)$ functions are symmetrical but are opposite in phase. Fig. 6 shows the similar plots of (5) and (6) in mode 2 which are at higher voltages. Note that the curves are not symmetrical because of saturation at $T_s/2$. The saturation of $T_{UN\text{-ON}}$ in sector A mode 2 is evident from the waveforms of Fig. 4(b)–(d). Mode 2 ends in the upper limit when the turn-on time curves touch the zero line. For phases V and W, the curves in Figs. 5 and 6 are similar but mutually phase shifted by $2\pi/3$ angle. Note that both $T_{UP\text{-ON}}$ and $T_{UN\text{-ON}}$ vary linearly with V^* magnitude in the whole undermodulation range except the saturation regions. It is possible to superimpose both Figs. 5 and 6 with the common bias time $3T_s/8$ and variable V^*. The digital word corresponding to $g(\theta_e)$ as a function of angle θ_e for both P and N states in all the phases and in all the modes can be generated by simulation for training a neural network. Then, $T_{UP\text{-ON}}$ and $T_{UN\text{-ON}}$ values can be solved from the equations corresponding to the superimposed Figs. 5 and 6.

III. Neural-Network-Based Space-Vector PWM

The derivation of turn-on times and the corresponding $g(\theta_e)$ functions, as discussed above, permits neural-network-based SVM implementation using two separate sections: one is the neural net section that generates the $g(\theta_e)$ function from the angle θ_e and the other is linear multiplication with the voltage signal V^*. Fig. 7 shows the neural network topology with the peripheral circuits to generate the PWM waves. It consists of a 1–24–12 network with sigmoidal activation function for middle and output layers. The network receives the θ_e angle at the input and generates 12 turn-on time signals as shown with four outputs for each phase (i.e., two for P and two for N states) which are correspondingly defined as $g_{UP1}(\theta_e)$, $g_{UP2}(\theta_e)$, $g_{UN1}(\theta_e)$, and $g_{UN1}(\theta_e)$ for phase U. This segmentation complexity is introduced for avoiding sector identification and use of only one timer at the output which will be explained later. These outputs are multiplied by the signal V^*, scaled by the factor K', and digital words $W_{T\text{-ON}}$ are generated for each channel as indicated in the figure. These signals are compared with the output of a single UP/DOWN counter and processed through a logic block to generate the PWM outputs.

$$T_{UP\text{-ON}} = \begin{Bmatrix} \frac{3T_s}{8} + \frac{T_s}{8} - 2KV^* \sin\left(\theta_e + \frac{\pi}{3}\right), & \text{for } S = A,\ R = 2, 3, 4 \\ \begin{bmatrix} \frac{3T_s}{8} + \frac{T_s}{8} - 2KV^*\sqrt{3}\cos(\theta_e), & \text{for } S = B,\ R = 2 \\ \frac{3T_s}{8} - \frac{T_s}{8} + 2KV^* \sin\left(\theta_e - \frac{\pi}{3}\right), & \text{for } S = B,\ R = 3 \\ \frac{3T_s}{8} + \frac{T_s}{8}, & \text{for } S = B,\ R = 4 \end{bmatrix} \\ \frac{3T_s}{8} + \frac{T_s}{8}, & \text{for } S = C,\ R = 2, 3, 4 \\ \frac{3T_s}{8} + \frac{T_s}{8}, & \text{for } S = D,\ R = 2, 3, 4 \\ \begin{bmatrix} \frac{3T_s}{8} + \frac{T_s}{8}, & \text{for } S = E,\ R = 2 \\ \frac{3T_s}{8} - \frac{T_s}{8} - 2KV^* \sin\left(\theta_e + \frac{\pi}{3}\right), & \text{for } S = E,\ R = 3 \\ \frac{3T_s}{8} + \frac{T_s}{8} - 2KV^*\sqrt{3}\cos(\theta_e), & \text{for } S = E,\ R = 4 \end{bmatrix} \\ \frac{3T_s}{8} + \frac{T_s}{8} + 2KV^* \sin\left(\theta_e - \frac{\pi}{3}\right), & \text{for } S = F,\ R = 2, 3, 4 \end{Bmatrix} \tag{5}$$

$$T_{UN\text{-ON}} = \begin{Bmatrix} \frac{3T_s}{8} + \frac{T_s}{8}, & \text{for } S = A,\ R = 2, 3, 4 \\ \begin{bmatrix} \frac{3T_s}{8} + \frac{T_s}{8}, & \text{for } S = B,\ R = 2 \\ \frac{3T_s}{8} - \frac{T_s}{8} + 2KV^* \sin\left(\theta_e + \frac{\pi}{3}\right), & \text{for } S = B,\ R = 3 \\ \frac{3T_s}{8} + \frac{T_s}{8} + 2KV^*\sqrt{3}\cos(\theta_e), & \text{for } S = B,\ R = 4 \end{bmatrix} \\ \frac{3T_s}{8} + \frac{T_s}{8} - 2KV^* \sin\left(\theta_e - \frac{\pi}{3}\right), & \text{for } S = C,\ R = 2, 3.4 \\ \frac{3T_s}{8} + \frac{T_s}{8} + 2KV^* \sin\left(\theta_e + \frac{\pi}{3}\right), & \text{for } S = D,\ R = 2, 3, 4 \\ \begin{bmatrix} \frac{3T_s}{8} + \frac{T_s}{8} + 2KV^*\sqrt{3}\cos(\theta_e), & \text{for } S = E,\ R = 2 \\ \frac{3T_s}{8} - \frac{T_s}{8} - 2KV^* \sin\left(\theta_e - \frac{\pi}{3}\right), & \text{for } S = E,\ R = 3 \\ \frac{3T_s}{8} + \frac{T_s}{8}, & \text{for } S = E,\ R = 4 \end{bmatrix} \\ \frac{3T_s}{8} + \frac{T_s}{8}, & \text{for } S = F,\ R = 2, 3, 4 \end{Bmatrix} \tag{6}$$

TABLE II
ANALYTICAL TIME EXPRESSIONS OF VOLTAGE VECTORS IN DIFFERENT REGIONS AND SECTORS

Sector		Region-1	Region-2	Region-3	Region-4
A	T_a	$nT_s\sin(\pi/3-\theta_e)$	$T_s[1-n\sin(\theta_e+\pi/3)]$	$T_s/2[1-2n\sin\theta_e]$	$T_s/2[2n\sin\theta_e-1]$
	T_b	$T_s/2[1-2n\sin(\theta_e+\pi/3)]$	$nT_s\sin\theta_e$	$T_s/2[2n\sin(\theta_e+\pi/3)-1]$	$nT_s\sin(\pi/3-\theta_e)$
	T_c	$nT_s\sin\theta_e$	$T_s/2[2n\sin(\pi/3-\theta_e)-1]$	$T_s/2[1+2n\sin(\theta_e-\pi/3)]$	$T_s[1-n\sin(\theta_e+\pi/3)]$
B	T_a	$nT_s\sin(\theta_e-\pi/3)$	$T_s/2[2n\sin(\theta_e+\pi/3)-1]$	$T_s/2[1-2n\sin(\theta_e+\pi/3)]$	$T_s[1-n\sin\theta_e]$
	T_b	$T_s/2[1-2n\sin\theta_e]$	$nT_s\sin(\theta_e-\pi/3)$	$T_s/2[2n\sin\theta_e-1]$	$nT_s\sin(\theta_e+\pi/3)$
	T_c	$nT_s\sin(\theta_e+\pi/3)$	$T_s[1-n\sin\theta_e]$	$T_s/2[1-2n\sin(\theta_e-\pi/3)]$	$T_s/2[2n\sin(\theta_e-\pi/3)-1]$
C	T_a	$nT_s\sin\theta_e$	$T_s[1-n\sin(\theta_e-\pi/3)]$	$T_s/2[1+2n\sin(\theta_e+\pi/3)]$	$-T_s/2[1+2n\sin(\theta_e+\pi/3)]$
	T_b	$T_s/2[1-2n\sin(\theta_e-\pi/3)]$	$-nT_s\sin(\theta_e+\pi/3)$	$T_s/2[2n\sin(\theta_e-\pi/3)-1]$	$nT_s\sin\theta_e$
	T_c	$-nT_s\sin(\theta_e+\pi/3)$	$T_s/2[2n\sin\theta_e-1]$	$T_s/2[1-2n\sin\theta_e]$	$T_s[1-n\sin(\theta_e-\pi/3)]$
D	T_a	$-nT_s\sin\theta_e$	$T_s/2[2n\sin(\theta_e-\pi/3)-1]$	$T_s/2[1-2n\sin(\theta_e-\pi/3)]$	$T_s[1+n\sin(\theta_e+\pi/3)]$
	T_b	$T_s/2[1+2n\sin(\theta_e+\pi/3)]$	$-nT_s\sin\theta_e$	$-T_s/2[1+2n\sin(\theta_e+\pi/3)]$	$nT_s\sin(\theta_e-\pi/3)$
	T_c	$nT_s\sin(\theta_e-\pi/3)$	$T_s[1+n\sin(\theta_e+\pi/3)]$	$T_s/2[1+2n\sin\theta_e]$	$-T_s/2[1-2n\sin\theta_e]$
E	T_a	$-nT_s\sin(\theta_e+\pi/3)$	$T_s[1+n\sin\theta_e]$	$T_s/2[1+2n\sin(\theta_e-\pi/3)]$	$T_s/2[2n\sin(\pi/3-\theta_e)-1]$
	T_b	$T_s/2[1+2n\sin\theta_e]$	$nT_s\sin(\pi/3-\theta_e)$	$-T_s/2[1+2n\sin\theta_e]$	$-nT_s\sin(\theta_e+\pi/3)$
	T_c	$nT_s\sin(\pi/3-\theta_e)$	$-T_s/2[1+2n\sin(\theta_e+\pi/3)]$	$T_s/2[1+2n\sin(\theta_e+\pi/3)]$	$Ts[1+\sin\theta_e]$
F	T_a	$nT_s\sin(\theta_e+\pi/3)$	$-T_s/2[1+2n\sin\theta_e]$	$T_s/2[1+2n\sin\theta_e]$	$T_s[1+n\sin(\theta_e-\pi/3)]$
	T_b	$T_s/2[1+2n\sin(\theta_e-\pi/3)\}$	$nT_s\sin(\theta_e+\pi/3)$	$Ts/2[2n\sin(\pi/3-\theta_e)-1]$	$-nT_s\sin\theta_e$
	T_c	$-nT_s\sin\theta_e$	$T_s[1+n\sin(\theta_e-\pi/3)]$	$T_s/2[1-2n\sin(\theta_e+\pi/3)]$	$-T_s/2[1+2n\sin(\theta_e+\pi/3)-1]$

TABLE III
SEQUENCING OF SWITCHING STATES IN DIFFERENT SECTORS AND REGIONS

Sector		Region-1	Region-2	Region-3	Region-4
A	U_A	NOOOPPP	OPPP	OOPPP	OPPP
	V_A	NNOOOPP	NNOO	NOOOP	OOPP
	W_A	NNNOOOP	NNNO	NNNOO	NNNO
B	U_B	PPOOONN	PPOO	POOON	OONN
	V_B	PPPOOON	PPPO	PPPOO	PPPO
	W_B	POOONNN	ONNN	OONNN	ONNN
C	U_C	NNNOOOP	NNNO	NNNOO	NNNO
	V_C	NOOOPPP	OPPP	OOPPP	OPPP
	W_C	NNOOOPP	NNOO	NOOOP	OOPP
D	U_D	POOONNN	ONNN	OONNN	ONNN
	V_D	PPOOONN	PPOO	POOON	OONN
	W_D	PPPOOON	PPPO	PPPOO	PPPO
E	U_E	NNOOOPP	NNOO	NOOOP	OOPP
	V_E	NNNOOOP	NNNO	NNNOO	NNNO
	W_E	NOOOPPP	OPPP	OOPPP	OPPP
F	U_F	PPPOOON	PPPO	PPPOO	PPPO
	V_F	POOONNN	ONNN	OONNN	ONNN
	W_F	PPOOONN	PPOO	POOON	OONN

A. ANN Output Signal Segmentation and Processing

It was mentioned before that, in the PWM waves of the odd sector (A, C, or E), P states appear as pulsed waves and N states appear as notched waves (see Fig. 4). On the other hand, in the even sector (B, D, or F) P states appear as notched waves and N states appear as pulsed waves. This can be easily verified by drawing waveforms in any of these sectors. In order to avoid a sector identification (odd or even) problem and use only one timer, the ANN output signals are segmented and processed through logic circuits to generate the PWM waves. As mentioned above, each phase output signal is resolved into P and N pairs of component signals. The segmentation and processing

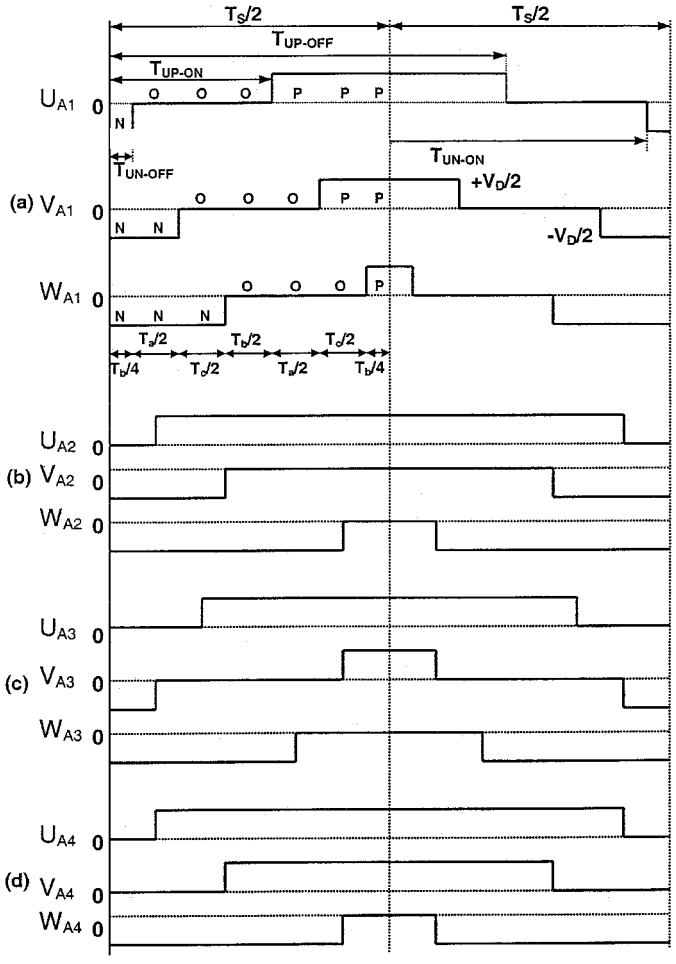

Fig. 4. Waveforms showing sequence of switching states for the four regions in sector A. (a) Region 1 ($\theta_e = 30^\circ$). (b) Region 2 ($\theta_e = 15^\circ$). (c) Region 3 ($\theta_e = 30^\circ$). (d) Region 4 ($\theta_e = 45^\circ$).

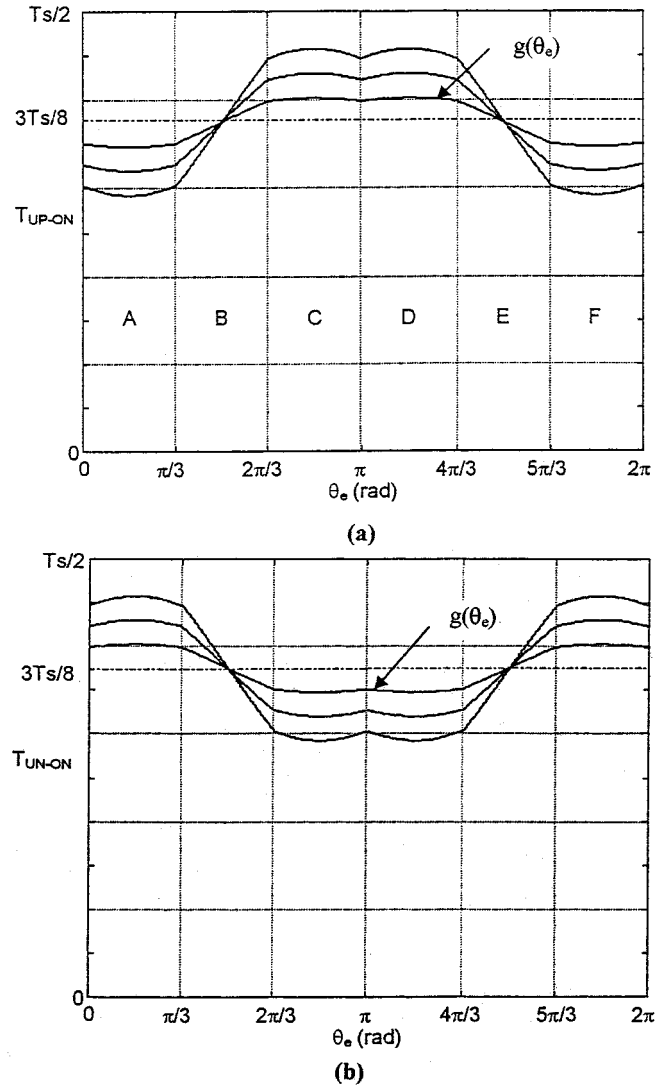

Fig. 5. Calculated plots of turn-on time for phase U in mode 1. (a) Turn-on time for P state ($T_{UP\text{-}\mathrm{ON}}$). (b) Turn-on time for N state ($T_{UN\text{-}\mathrm{ON}}$).

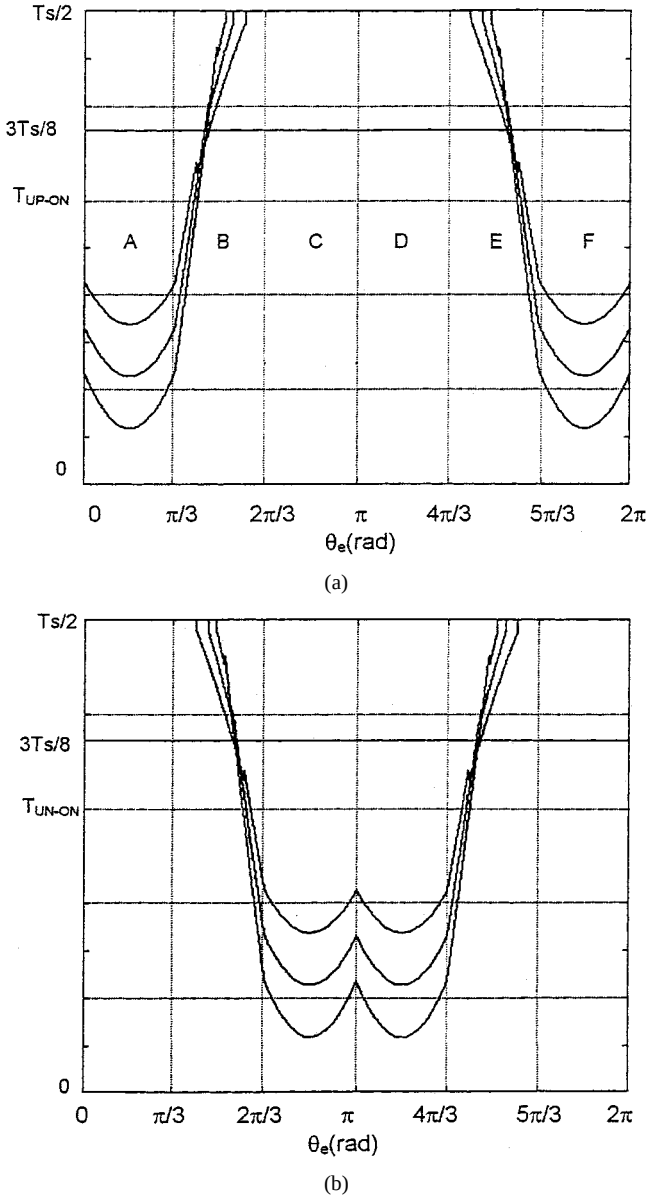

Fig. 6. Calculated plots of turn-on time for phase U in mode 2. (a) Turn-on time for P state ($T_{UP\text{-}\mathrm{ON}}$). (b) Turn-on time for N state ($T_{UN\text{-}\mathrm{ON}}$).

of all the component signal pairs are similar, and we will discuss here, as an example, for U phase P state pairs only, i.e., $g_{UP1}(\theta_e)$ and $g_{UP2}(\theta_e)$. Fig. 8 shows this segmentation in different sectors that relate to the total signal $g_{UP}(\theta_e)$ which is defined with respect to the bias point $(3/8)T_s$. If the command V^* lies in the odd sector A, C, or E, the turn-on time functions can be given as

$$g_{UP1}(\theta_e) = \frac{3}{8}T_s + g_{UP}(\theta_e) \tag{10}$$

$$g_{UP2}(\theta_e) = \frac{T_s}{2} \tag{11}$$

and the corresponding digital words are

$$W(g_{UP1}) = W_{TB} + K'V^* g_{UP}(\theta_e) \tag{12}$$

$$W(g_{UP2}) = W(T_s/2) \tag{13}$$

where W_{TB} corresponds to time $(3/8)T_s$ and $W(g_{UP2})$ is always saturated to the corresponding time $T_s/2$. For the even sectors B, D, and F, the corresponding signal expressions are

$$g_{UP1}(\theta_e) = -\frac{T_s}{2} \tag{14}$$

$$g_{UP2}(\theta_e) = \left(\frac{T_s}{8} - g_{UP}(\theta_e)\right) \tag{15}$$

as indicated in the figure. The corresponding expressions for digital words are

$$W(g_{UP1}) = 0 \tag{16}$$

$$W(g_{UP2}) = \frac{1}{3}W_{TB} - K'V^* g_{UP}(\theta_e). \tag{17}$$

Note that $W(g_{UP1})$ in these sectors are negative and clamped to zero level. Fig. 9 explains the timer and logic operation with

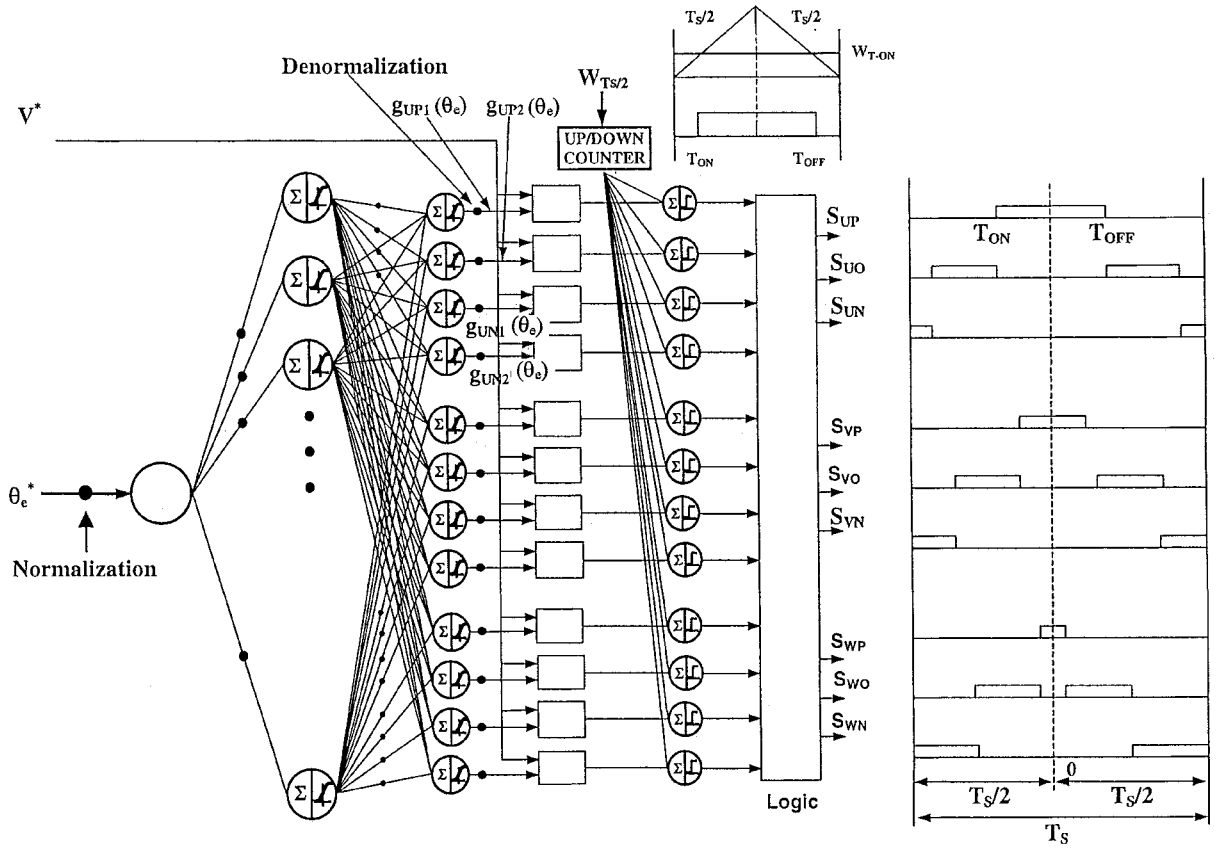

Fig. 7. Feedforward neural-network (1–24–12)-based space-vector PWM controller.

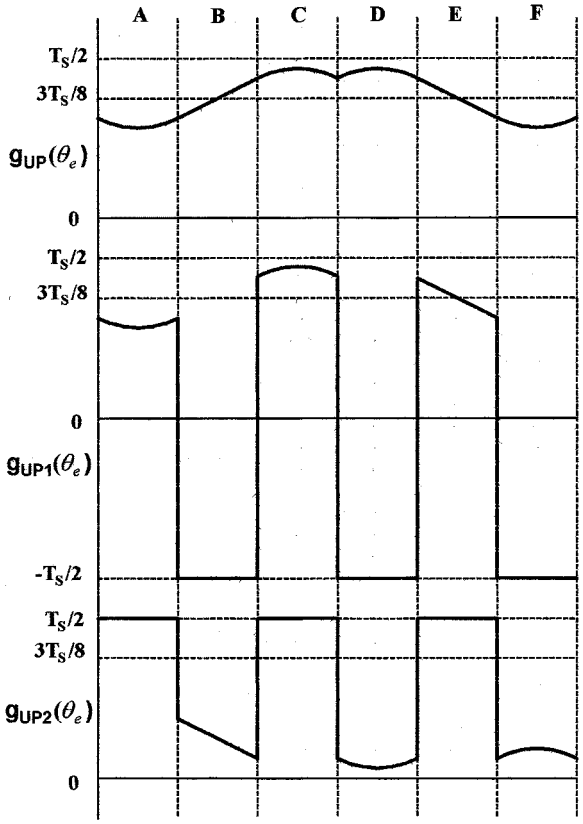

Fig. 8. Segmentation of neural network output for U-phase P states.

$W(g_{UP1})$ and $W(g_{UP2})$ signals only. Similar operations are performed with the P and N signals of all the phases and all the sectors to derive the correct switching signals. Fig. 4 verifies the waveform generation for all the regions in sector A, and Fig. 7 illustrates waves for sector A region 1 only.

TABLE IV
PARAMETERS OF MACHINE AND INVERTER

DC link voltage (V_d): 3000 V	
Sampling time (T_s): 1 ms (1.0 kHz switching frequency)	
Induction motor:	3 phase, 60 hp, 1700 V, 6-pole
	Frequency range: 0-60 Hz
	Power factor (full load): 0.85
	Stator resistance (R_s): 2.8 Ohm
	Rotor resistance (R_r): 2.12 Ohm
	Stator leakage inductance (L_{ls}): 21.114 mH
	Rotor leakage inductance (L_{lr}): 21.114 mH
	Magnetizing inductance (L_m): 724.261 mH

IV. PERFORMANCE EVALUATION

The drive performance was evaluated in detail by simulation with the neural network which was trained and tested offline in the undermodulation range (V_s = 10–1603 V and f_s = 0–50 Hz) with sampling time T_s = 1.0 ms (f_c = 1.0 kHz). The training data were generated by simulation of the conventional SVM algorithm. The θ_e angle training of the network was performed in the full cycle with an increment of 2°. The training time was typically half-a-day with a 600-MHz Pentium-based PC, and it took 12 000 epochs for SSE (sum of squared error) = 0.008. Note that due to learning or interpolation capability,

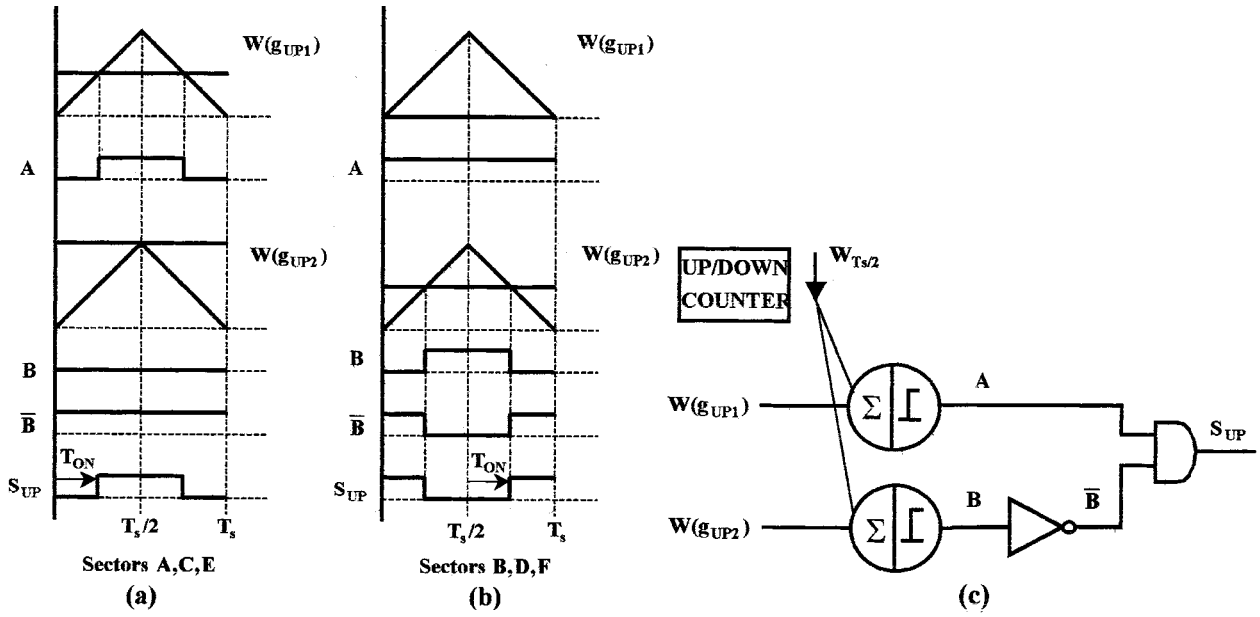

Fig. 9. Explanation of timer and logic operation.

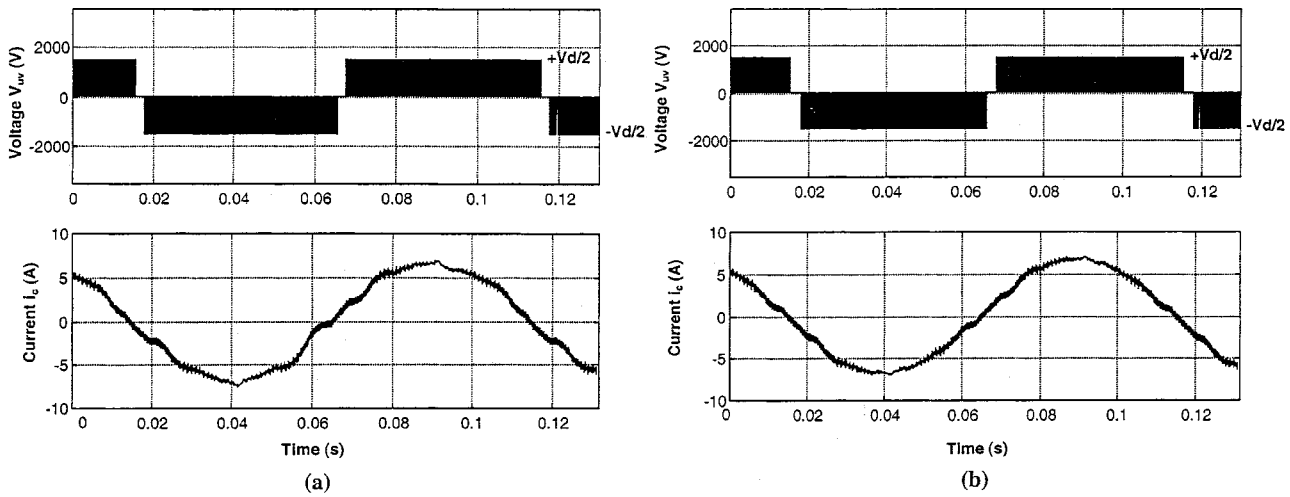

Fig. 10. Machine line voltage and phase current waves in mode 1 (10 Hz). (a) Neural-network-based SVM. (b) Equivalent DSP-based SVM.

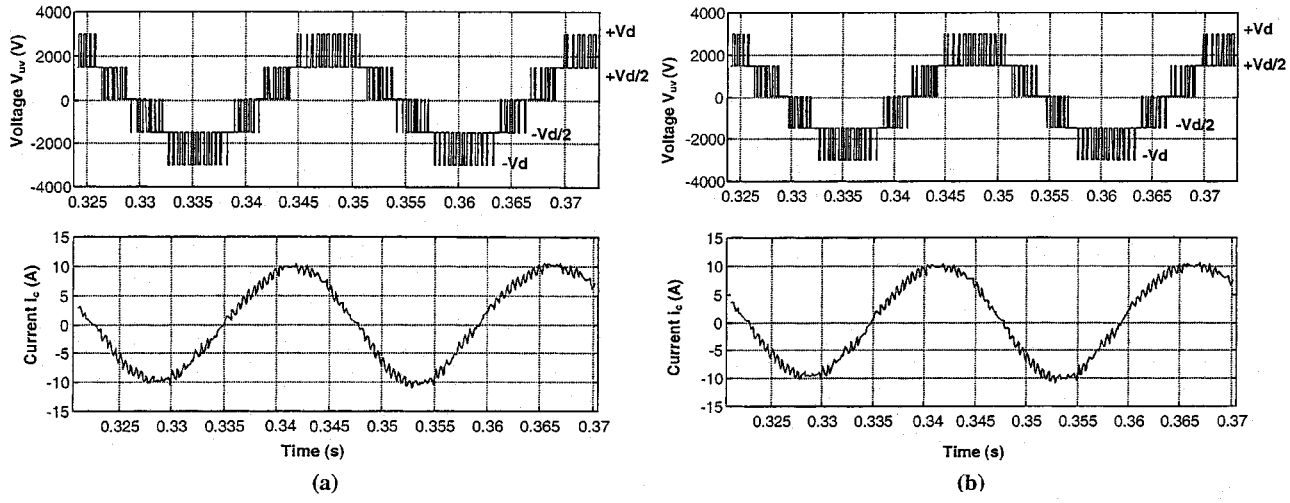

Fig. 11. Machine line voltage and phase current waves in mode 2 (40 Hz). (a) Neural-network-based SVM. (b) Equivalent DSP-based SVM.

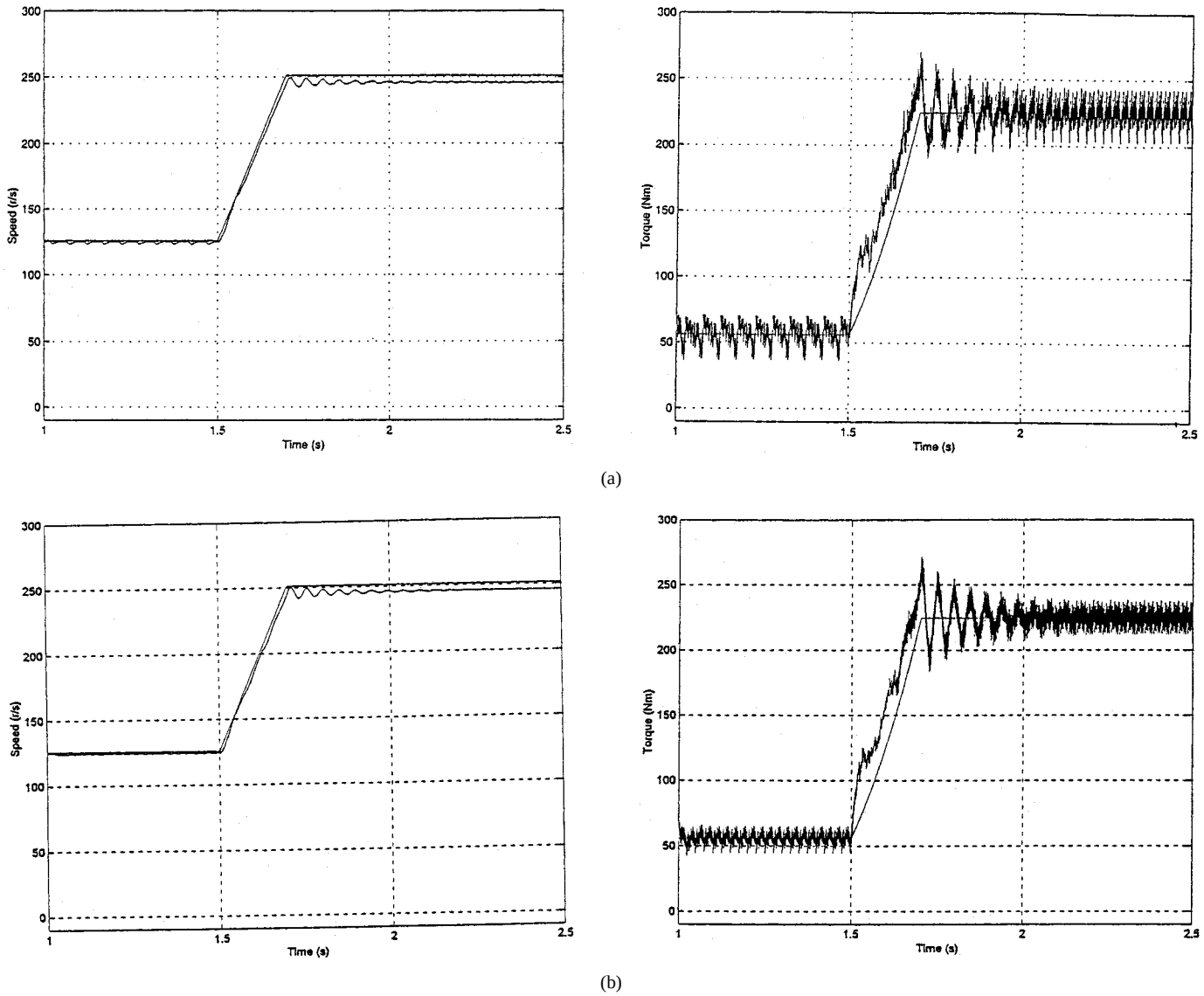

Fig. 12. Volts/Hz-controlled drive dynamic performance with (a) neural-network-based SVM and (b) equivalent DSP-based SVM.

the ANN operates at a higher resolution. The network is solved every sampling time to establish the pulsewidth signals at the output. Table IV gives the parameters of the machine and the inverter for simulation study. Fig. 10(a) shows the machine line voltage and current waves at steady state in mode 1 which compares well with the corresponding DSP-based waves shown in Fig. 10(b). Fig. 11 shows the similar comparison for mode 2 operation. Fig. 12 shows the typical dynamic performance comparison of the drive during acceleration where acceleration torque is very low due to slow acceleration. The machine has a speed-sensitive load torque (T_L) which is evident from the figure. The low switching frequency of the inverter gives large ripple torque of the machine.

V. Conclusion

A feedforward neural-network-based space-vector pulsewidth modulator for a three-level inverter has been described that operates very well in the whole undermodulation region. In the ANN-based SVM technique, the digital words corresponding to turn-on time are generated by the network and then converted to pulsewidths by a single timer. The training data were generated by simulation of a conventional SVM algorithm, and then a backpropagation technique in the MATLAB-based Neural Network Toolbox [8] was used for offline training. The network was simulated with an open-loop volts/Hz-controlled induction motor drive and evaluated thoroughly for steady-state and dynamic performance with a conventional DSP-based SVM. The performance of the ANN-based modulator was found to be excellent. The modulator can be easily applied for a vector-controlled drive. Unfortunately, no suitable ASIC chip is yet commercially available [9] to implement the controller economically. The Intel 80170 ETANN (electrically trainable analog ANN) was introduced some time ago, but was withdrawn from the market due to a drift problem. However, considering the technology trend, we can be optimistic about the availability of a large economical digital ASIC chip with high resolution.

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