1 Experiment No. 1

2 Experiment Title

Introduction to MICROWIND 3.0
Design and Analyze nMOS and pMOS layout ensuring proper DRC.

3 Objective

The main objectives of this report are:

- To introduce the use of Microwind 3.0 software for designing and simulating MOSFET transistors (nMOS and pMOS)
- To explain the theory and working process of nMOS and pMOS transistors.
- To demonstrate the step-by-step fabrication process of nMOS and pMOS transistors using diffusion layers, polysilicon, and the MOS generator tool in Microwind ensuring proper DRC.

4 Theory

MICROWIND 3.0 is a specialized software tool designed for the simulation and design of microelectronic circuits at the layout level. It allows users to design, simulate, and analyze semiconductor components like MOSFETs (nMOS and pMOS), digital circuits, and analog circuits by providing a graphical interface that bridges the gap between circuit design and physical layout.

4.1 Microwind 3.0 Interface Overview

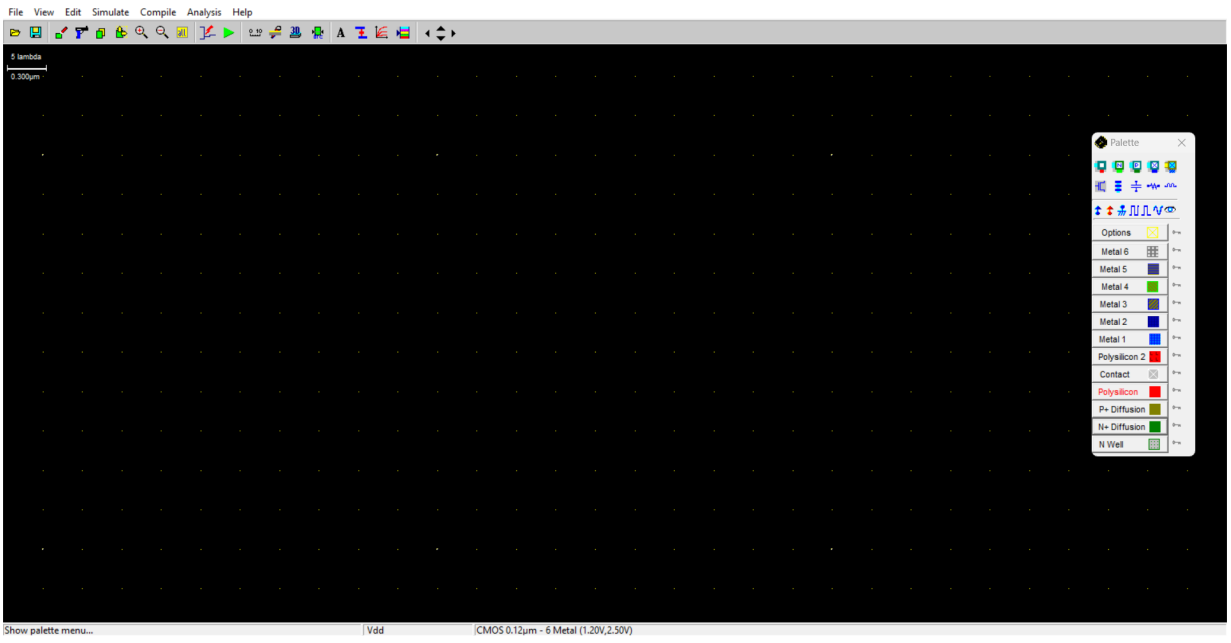


Figure 1: Openning Window

The Microwind 3.0 interface consists of several key components, each serving a specific purpose in circuit design and simulation. The main parts of the interface include:

- Menu Bar
- Toolbar
- Palette
- Simulation Window
- DRC (Design Rule Check)

4.1.1 Menu Bar

The menu bar provides access to a wide range of functionalities, organized into several categories:

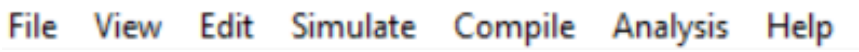
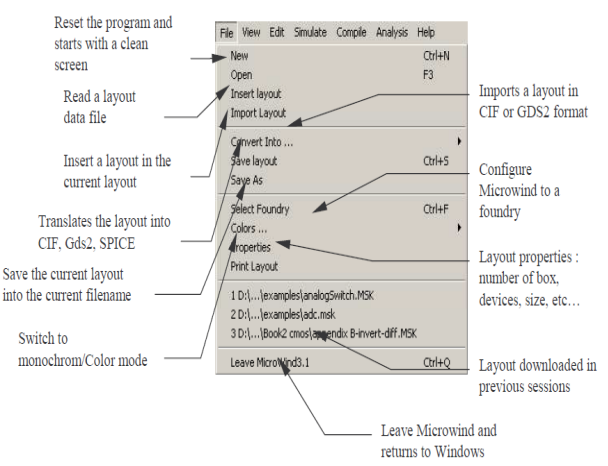
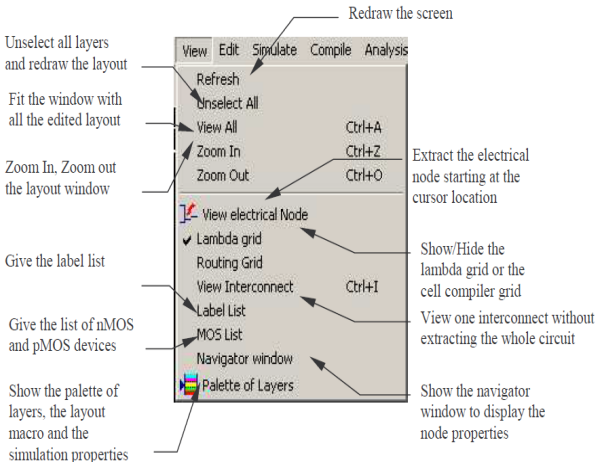


Figure 2: Menu Bar

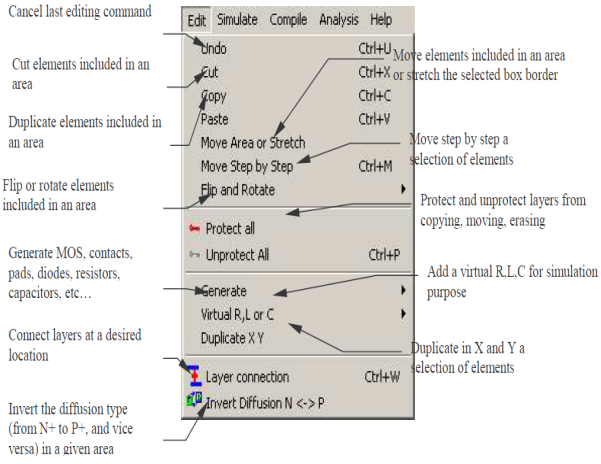
- **File Menu ,View Menu & Edit Menu :**



(a) File Menu



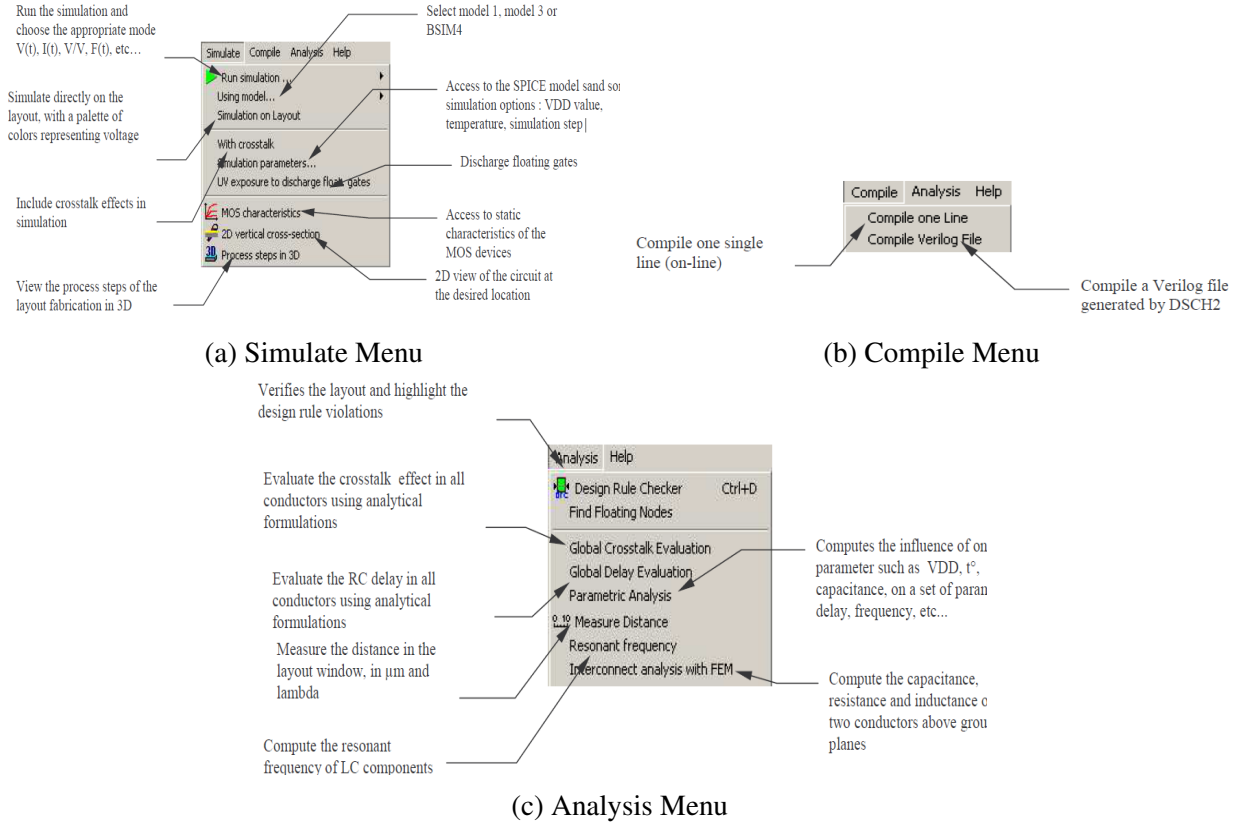
(b) View Menu



(c) Edit Menu

Figure 3: File Menu ,View Menu & Edit Menu

- **Simulate Menu ,Compile Menu & Analysis Menu :**



(a) Simulate Menu (b) Compile Menu

(c) Analysis Menu

Figure 4: Simulate Menu ,Compile Menu & Analysis Menu

Description about these menus are given below:

1. **File Menu:** The File menu allows to create, open, save, and manage design files in Microwind, as well as print layouts.

2. **View Menu:** The View menu offers options to zoom, display gridlines, and toggle visibility of layers or design elements in the layout.

3. **Edit Menu:** The Edit menu provides tools for copying, pasting, deleting, and modifying elements in the design, such as wires or components.

4. **Simulate Menu:** The Simulate menu enables running simulations of the circuit to observe signal behavior and performance under various conditions.

5. **Compile Menu:** The Compile menu is used to compile the layout into a netlist, converting the physical design into a file that can be used for simulation.

6. **Analysis Menu:** The Analysis menu offers tools for analyzing electrical properties, such as signal timing, power consumption, and transistor characteristics.

4.1.2 Tool Bar

Figure 5: Tool Bar

Description about these icons are given below:

Table 1: Toolbar in Microwind 3.0

	Open a layout file (MSK format)		Extract and simulate the circuit
	Save the layout file in MSK format		Measure the distance in lambda and micron between two points
	Draw a box using the selected layer of the palette		2D vertical aspect of the device
	Delete boxes or text.		Step by step fabrication of the layout in 3D
	Copy boxes or text		Design rule checking of the circuit. Errors are notified in the layout
	Stretch or move elements		Add a text to the layout. The text may include simulation properties.
	Zoom In		Connect the lower to the upper layers at the desired location using appropriate contacts.
	Zoom Out		Static MOS characteristics
	View all the drawing		View the palette
	Extract and view the electrical node pointed by the cursor		Move the layout up, left, right, down

4.1.3 Palette

The palette contains various tools and options for placing circuit components like transistors, wires, contacts, and vias. Each category is organized based on its function in the layout.

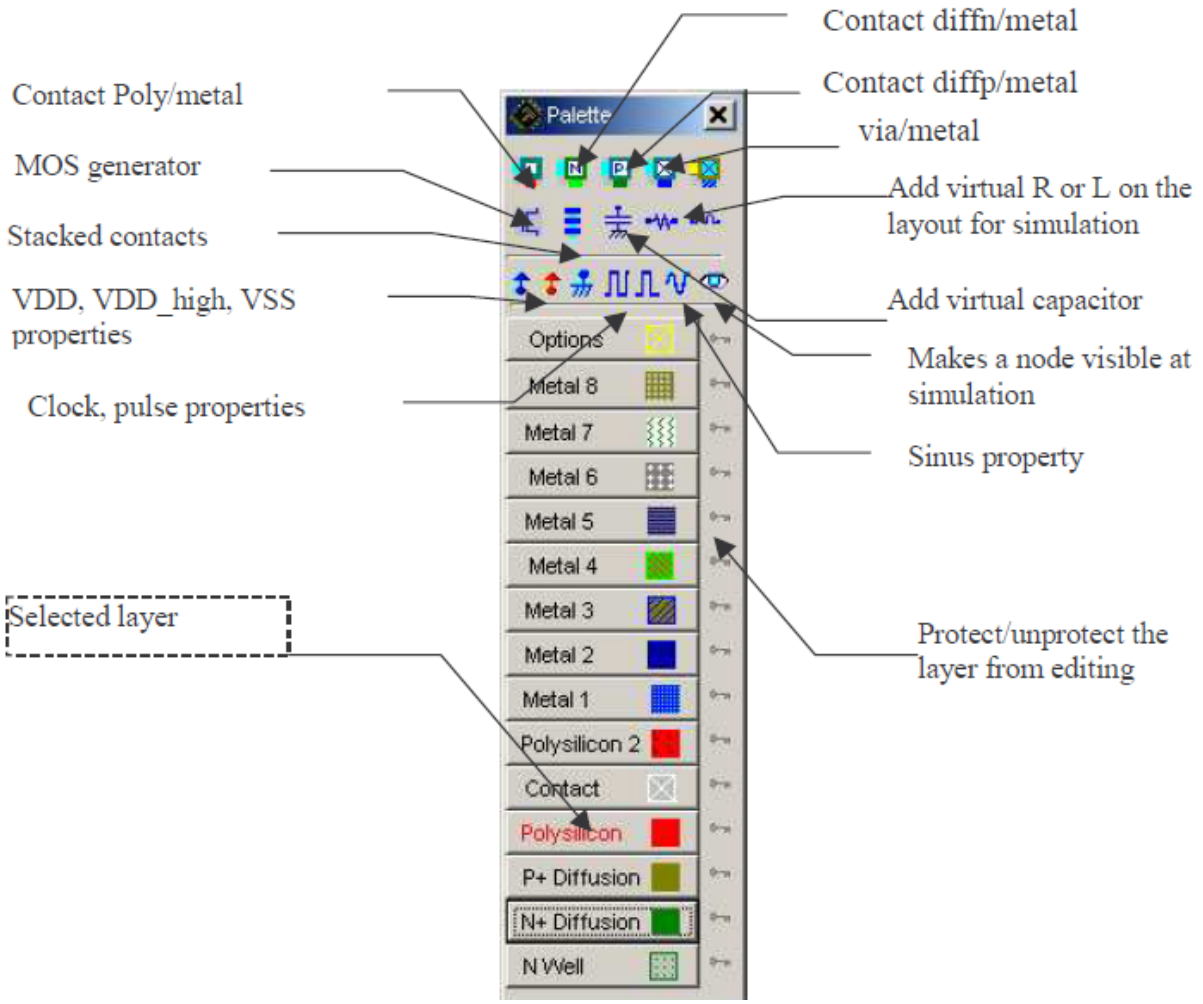


Figure 6: Palette in Microwind 3.0

4.1.4 Simulation Window

The simulation window shows the results of running an electrical simulation on your layout. This could be in the form of waveforms, timing analysis, or voltage/current plots. During simulation, the voltage, current, and logic levels of different nodes in the circuit can be visualized using waveforms. This allows users to verify that the circuit is operating as expected. The simulation window also supports timing analysis for digital circuits. Important timing parameters such as delay, rise and fall times, and propagation delays can be measured.

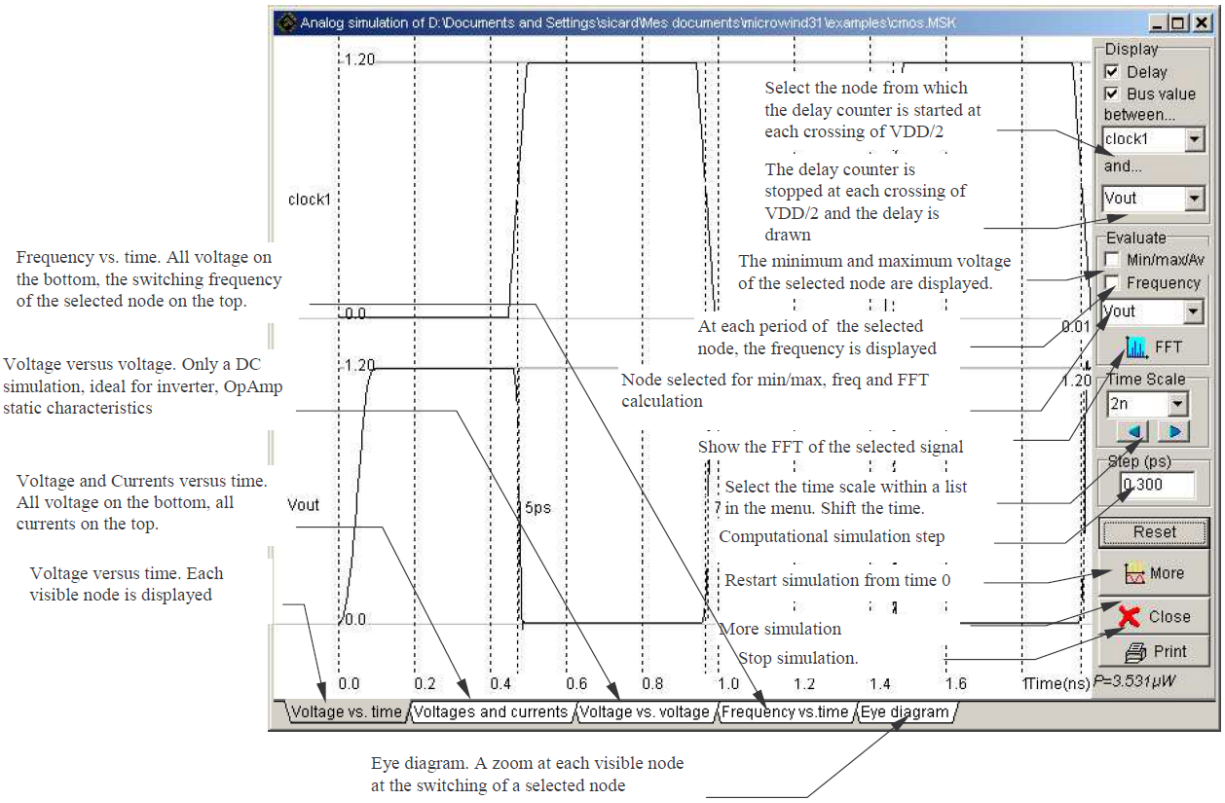


Figure 7: Simulation Window in Microwind 3.0

4.1.5 DRC (Design Rule Check)

Microwind's layout editor includes a built-in DRC system that alerts users to any violations of the design rules (e.g., minimum distance between components, minimum width for metal layers). This ensures that the layout conforms to the technological requirements for fabrication.

4.2 Theory of nMOS and pMOS Transistors

4.2.1 nMOS Transistor

The **nMOS transistor** is a type of MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) where the majority charge carriers are electrons. In nMOS, when a positive voltage is applied to the gate terminal, it attracts electrons towards the gate, forming a conductive channel between the source and drain, allowing current to flow from the drain to the source.
The key characteristics of an nMOS transistor include:

- It turns ON when a positive voltage is applied to the gate.
- Electrons are the majority carriers in the nMOS.
- When the gate voltage is zero or below the threshold voltage, the transistor is OFF, and no current flows.

4.2.2 pMOS Transistor

The **pMOS transistor** is the opposite of nMOS, where the majority charge carriers are holes. When a negative voltage is applied to the gate terminal, it attracts holes, forming a conductive channel, and allows current to flow from the source to the drain.

The key characteristics of a pMOS transistor include:

- It turns ON when a negative voltage is applied to the gate.
- Holes are the majority carriers in the pMOS.
- When the gate voltage is zero or positive, the transistor is OFF.

4.2.3 Strong 0 - Poor 1 and Strong 1 - Poor 0 Concept

The strength of the 0 and 1 states in nMOS and pMOS transistors comes from their ability to pass or drive voltages effectively. This behavior is related to the nature of the carriers that control the current flow in the transistors—electrons in nMOS and holes in pMOS.

1. **nMOS Transistor:**
   (a) **Strong 0:** In an nMOS transistor, when it is ON (the gate voltage is high), it connects the output to ground (0V), meaning it pulls the output low efficiently. Electrons, which are the majority charge carriers in nMOS, are highly mobile and can pull the output to a low voltage (strong 0) quickly and with little resistance.
   (b) **Poor 1:** When an nMOS transistor tries to pass a high voltage (logical 1), it does so inefficiently because it connects the output to the power supply (V_{dd}) through a pull-up resistor or pMOS. Electrons are not as good at pulling up the voltage to a strong 1 as pMOS transistors. As a result, the output may only reach a slightly higher voltage, but not a full logical high, which is why it's considered a poor 1.
2. **pMOS Transistor:**
   (a) **Strong 1:** A pMOS transistor is ON when its gate is at a low voltage (typically 0V). When ON, it connects the output to the power supply (V_{dd}) and can pull the output voltage high (logical 1) very effectively. Holes, which are the majority charge carriers in pMOS transistors, can easily move towards the source terminal, enabling a strong high voltage at the output (strong 1).
   (b) **Poor 0:** A pMOS transistor does not pass a low voltage (logical 0) very well because holes are less efficient at pulling the output voltage down to 0V. Thus, when a pMOS transistor is used to pass a logical 0, it results in a higher voltage (closer to V_{dd}), leading to a poor 0.

4.3 Fabrication Process of nMOS and pMOS in Microwind

4.3.1 Using Diffusion Layer and Polysilicon

In Microwind,we can fabricate an nMOS or pMOS transistor using the following steps:

1. **nMOS Transistor:**
   (a) Draw the *n-diffusion* layer to define the region for the source and drain.
   (b) Place the *polysilicon* layer over the diffusion to form the gate terminal.
   (c) The intersection of the polysilicon and diffusion layer forms the channel of the transistor.
   (d) Add *contacts* to the diffusion regions to form the source and drain terminals.

(e) Complete the circuit by ensuring proper DRC.

2. **pMOS Transistor:**

   (a) Draw the *p-diffusion* layer to define the region for the source and drain.

   (b) Place the *polysilicon* layer over the diffusion to form the gate terminal.

   (c) The intersection of the polysilicon and diffusion layer forms the channel of the transistor.

   (d) Add *contacts* to the diffusion regions to form the source and drain terminals.

   (e) Add *n-well* to the whole transistor region of Vdd++(5V).

   (f) Complete the circuit by ensuring proper DRC..

4.3.2 Using MOS Generator in Microwind

Microwind also provides an automatic tool called the **MOS Generator** to simplify the transistor creation process. Here are the steps to fabricate nMOS and pMOS transistors using the MOS Generator:

1. **nMOS Transistor:**

   (a) Open the MOS Generator tool.

   (b) Select *nMOS* from the options.

   (c) Adjust the width and length of the transistor as required.

   (d) The MOS Generator automatically generates the necessary diffusion, polysilicon, and contact layers.

2. **pMOS Transistor:**

   (a) Open the MOS Generator tool.

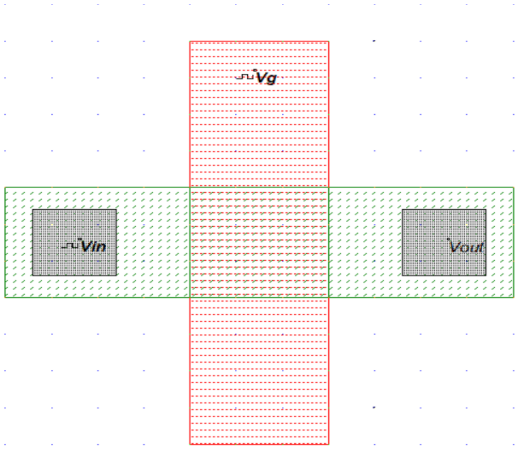
   (b) Select *pMOS* from the options.

   (c) Adjust the width and length of the transistor as required.

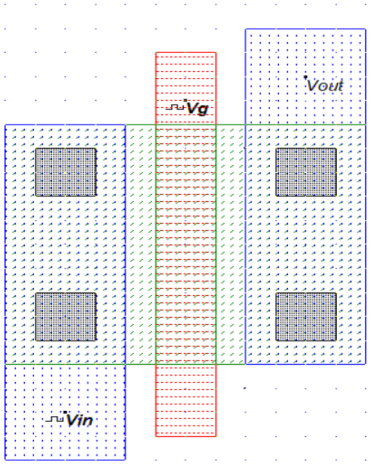
   (d) The MOS Generator automatically generates the necessary diffusion, polysilicon, and contact layers.

Using the MOS Generator is particularly efficient, as it automates the design of the transistor structure, reducing the time and complexity involved in manual layout.

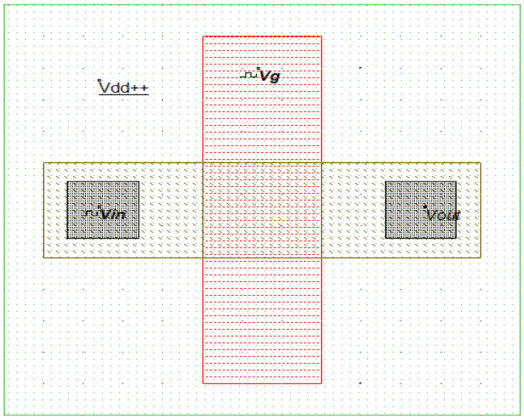
5 Schematic Layout



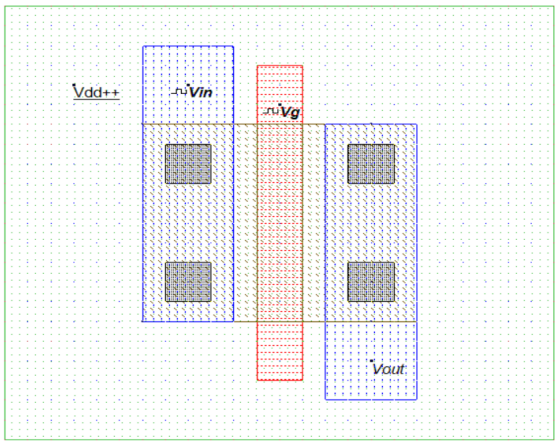
(a) nMOS



(b) nMOS (using MOS Generator)



(c) pMOS

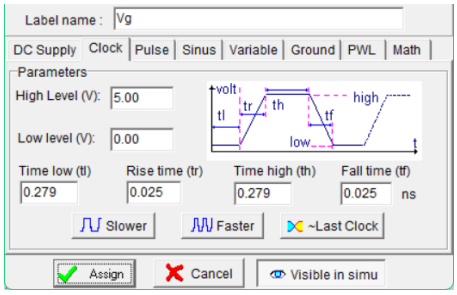


(d) pMOS (using MOS GENERATOR)

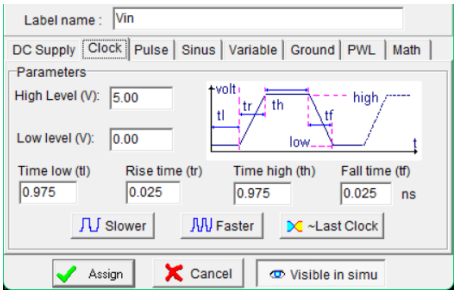
Figure 8: Design of nMos and pMos layout ensuring proper DRC.

6 Specification

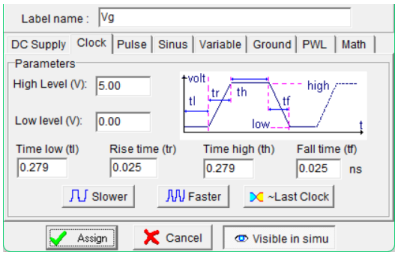
6.1 nMOS and pMOS



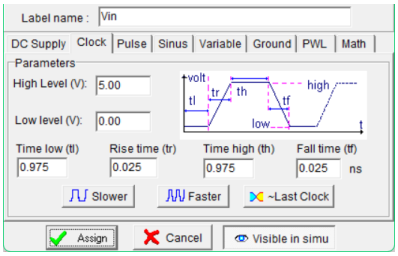
(a) Vg for nMOS



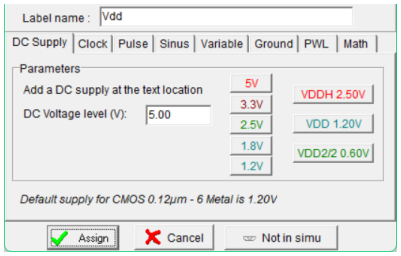
(b) Vin for nMOS



(c) Vg for pMOS



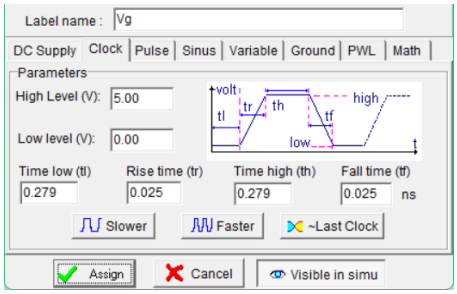
(d) Vin for pMOS



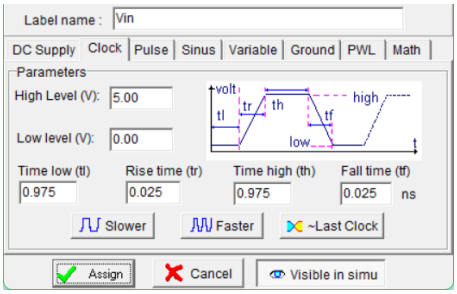
(e) Vdd for pMOS

Figure 9: Specifications of nMOS and pMOS layout

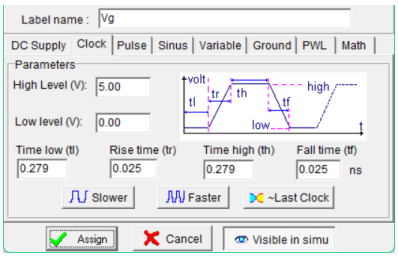
6.2 nMOS and pMOS using MOS Generator



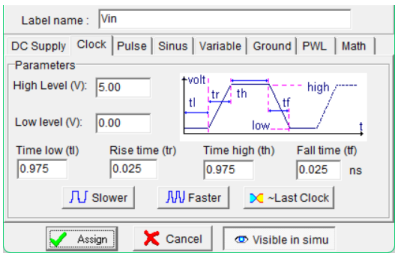
(a) Vg for nMOS (using MOS Generator)



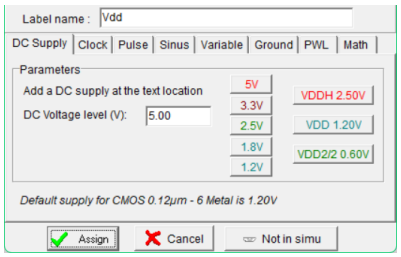
(b) Vin for nMOS (using MOS Generator)



(c) Vg for pMOS (using MOS Generator)



(d) Vin for pMOS (using MOS Generator)

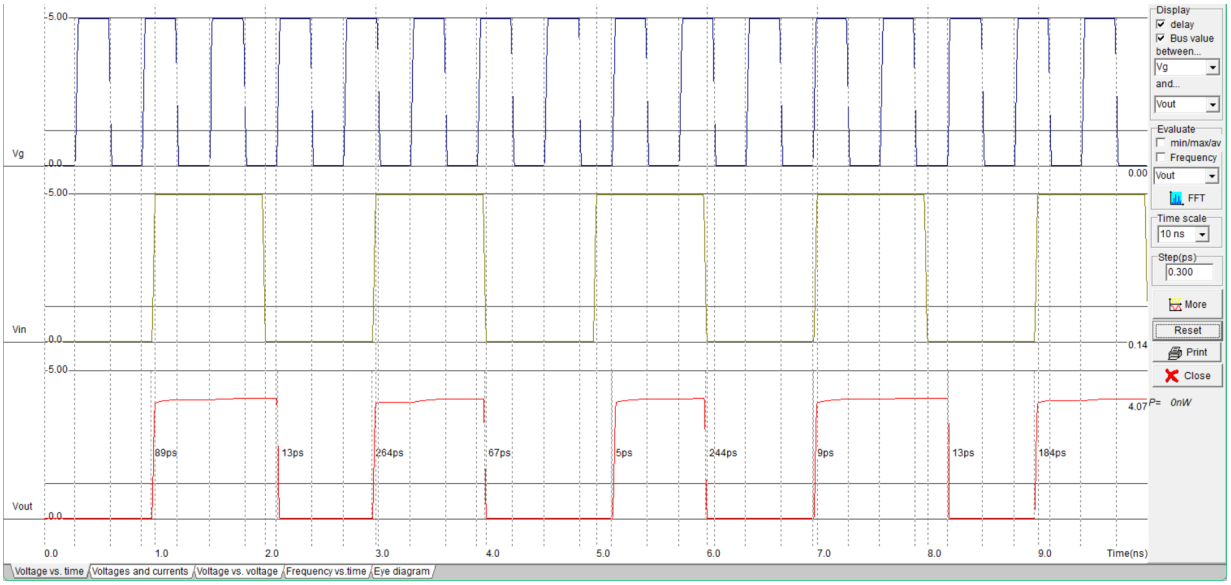


(e) Vdd for pMOS (using MOS Generator)

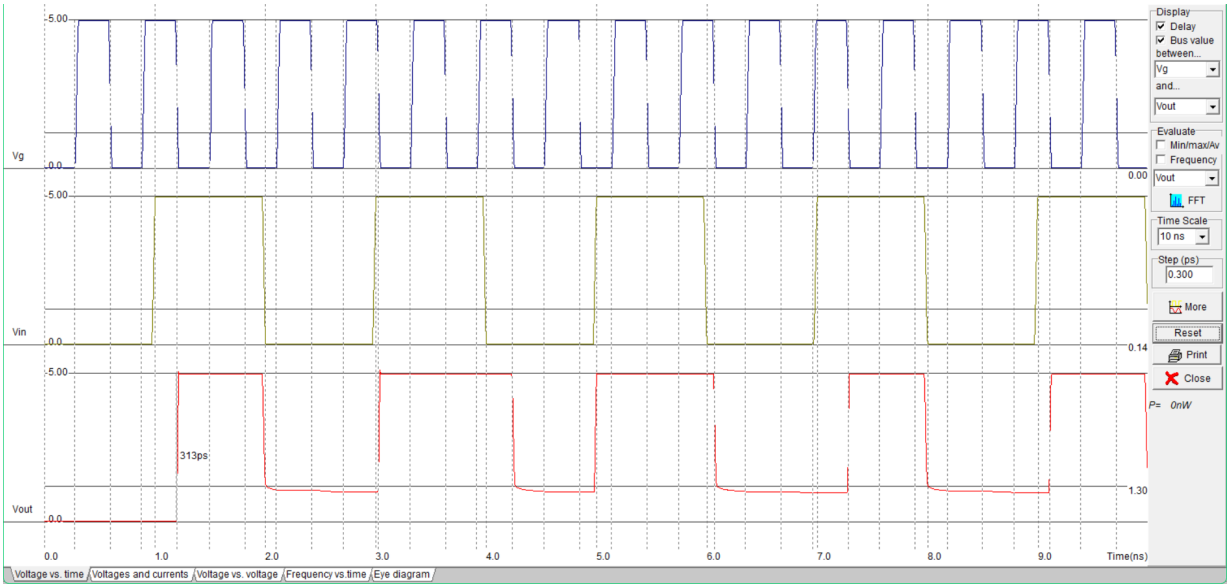
Figure 10: Specifications of nMOS and pMOS (using MOS Generator)

7 Output Waveshape

7.1 nMOS and pMOS



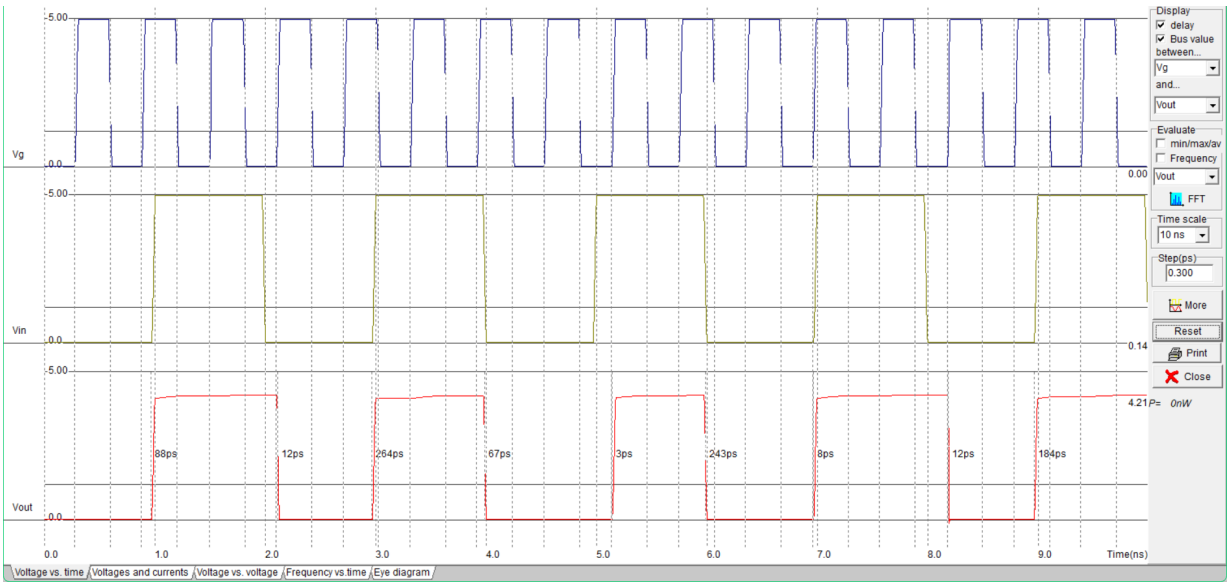
(a) nMOS



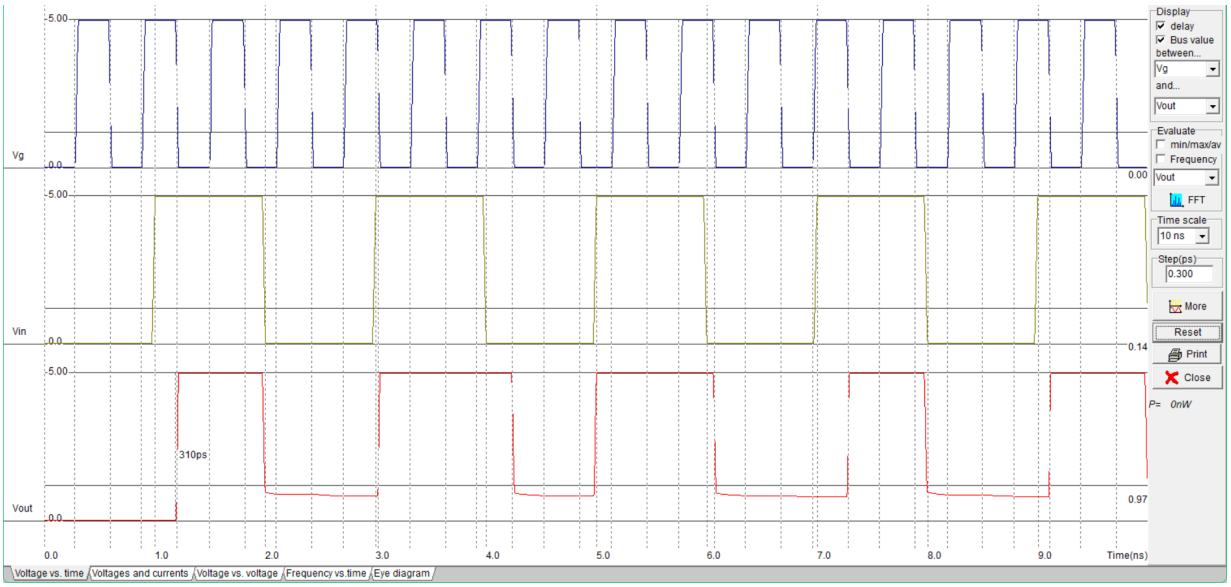
(b) pMOS

Figure 11: Output Waveshape of Fabricated nMOS and pMOS

7.2 nMOS and pMOS using MOS Generator



(a) nMOS using MOS Generator



(b) pMOS using MOS Generator

Figure 12: Output Waveshape of nMOS and pMOS (using MOS Generator)

8 Discussion

In this lab report, we utilized Microwind 3.0 to design and simulate nMOS and pMOS transistors, focusing on both their theoretical understanding and practical fabrication steps. The software's user-friendly interface, featuring a variety of menus such as File, View, Edit, Simulate, Compile, and Analysis, enabled efficient layout creation and simulation of MOS transistors.

The nMOS transistor was explored as a "strong 0, poor 1" device, where it conducts well to ground, making it effective for creating strong logical zeros, but less efficient at generating logical ones. Conversely, the pMOS transistor operates as a "strong 1, poor 0" device, excelling at producing strong logical ones, but offering weaker performance when pulling signals to zero.

The fabrication of both nMOS and pMOS transistors using Microwind involved defining diffusion layers and polysilicon gates, with the MOS generator providing a streamlined way to create layouts. This allowed us to visualize the physical structure and electrical characteristics of the transistors, and also perform simulations to verify their output voltage based on input voltage and ground voltage.

The simulation results confirmed the theoretical expectations regarding the performance of nMOS and pMOS transistors, highlighting their complementary nature in digital logic circuits.