1 Experiment No. 6

2 Experiment Title

Design and Analyze 2 Input XOR and XNOR Gates Using 1Finger MOS on MICROWIND 3.0

3 Objective

The main objectives of this report are:

- To design and analyze XOR and XNOR gates using CMOS inverters.
- To compare the performance of XOR and XNOR gates in terms of output voltage levels and switching characteristics.
- To verify the logical behavior of the XOR and XNOR gates using truth tables.
- To simulate the gate designs using MICROWIND 3.0 and understand the impact of circuit configurations on output behavior.

4 Theory

4.1 CMOS XOR Gate

A 2-input CMOS XOR gate is constructed using both pMOS and nMOS transistors in a configuration that performs the exclusive OR function. The output is high (logic '1') only when the inputs A and B are different, i.e., when one is logic '1' and the other is logic '0'. If both inputs are the same (either logic '0' or logic '1'), the output is low (logic '0'). The logic function of the 2-input CMOS XOR gate can be expressed as:

$$Y = A \oplus B = (A \cdot \overline{B}) + (\overline{A} \cdot B)$$

where: - A and B are the inputs, and - Y is the output of the XOR gate.

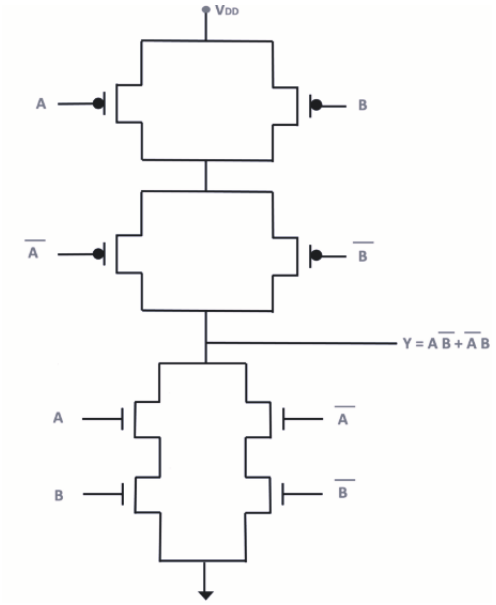

Figure 1: CMOS XOR-Gate

But in CMOS implementation,we use

$$Y = \overline{\overline{A \oplus B}} = (A \cdot B) + (\overline{A} \cdot \overline{B})$$

The truth table for a 2-input XOR gate is shown below:

Table 1: Truth Table for 2-Input CMOS XOR Gate

A	B	Y (XOR Output)
0	0	0
0	1	1
1	0	1
1	1	0

4.2 CMOS XNOR Gate

A 2-input CMOS XNOR gate is constructed similarly to the XOR gate, but with an additional inverter at the output. The output is high (logic '1') when both inputs A and B are the same, and low (logic '0') when they are different. The logic function of the 2-input CMOS XNOR gate can be expressed as:

$$Y = \overline{A \oplus B} = (A \cdot B) + (\overline{A} \cdot \overline{B})$$

where: - A and B are the inputs, and - Y is the output of the XNOR gate.

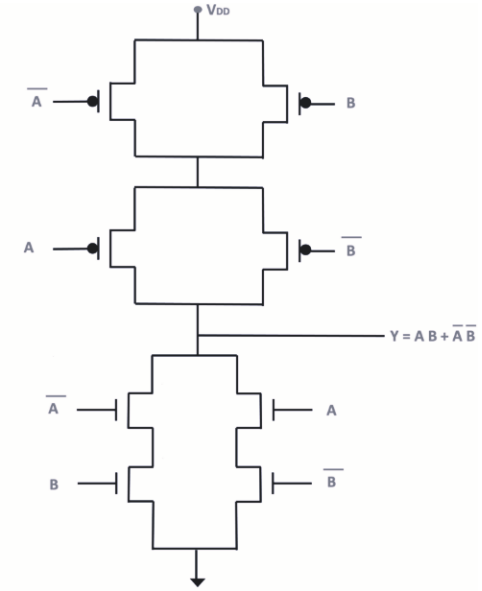

Figure 2: CMOS XNOR-Gate

But in CMOS implementation,we use

$$Y = \overline{\overline{\overline{\overline{A \oplus B}}}} = (A \cdot \overline{B}) + (\overline{A} \cdot B)$$

The truth table for a 2-input XNOR gate is shown below:

Table 2: Truth Table for 2-Input CMOS XNOR Gate

A	B	Y (XNOR Output)
0	0	1
0	1	0
1	0	0
1	1	1

5 Schematic Layout

5.1 XOR Gate using 1 Finger MOS

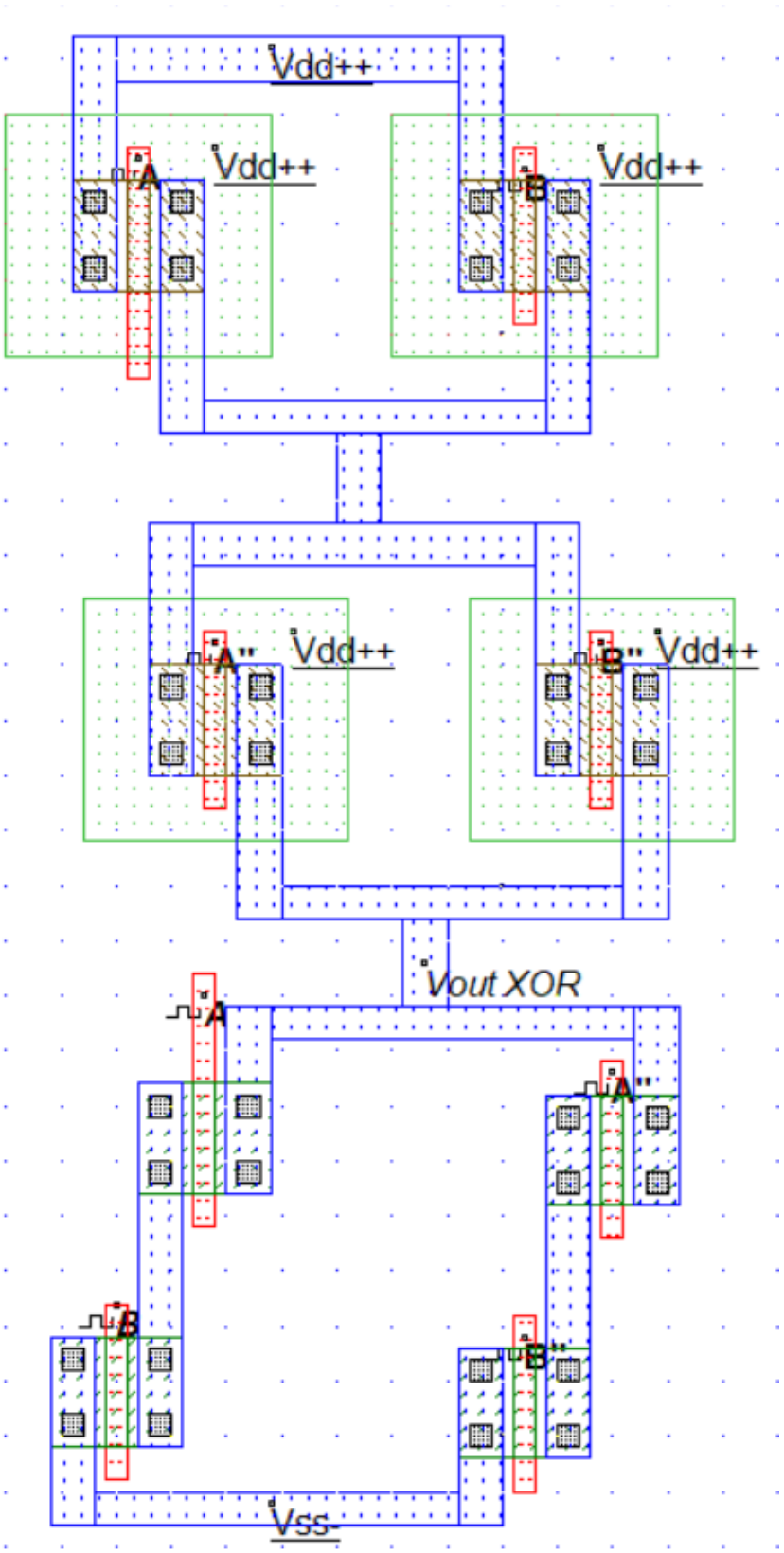

Figure 3: Design layout of XOR-Gate using 1 Finger MOS

5.2 XNOR Gate using 1 Finger MOS

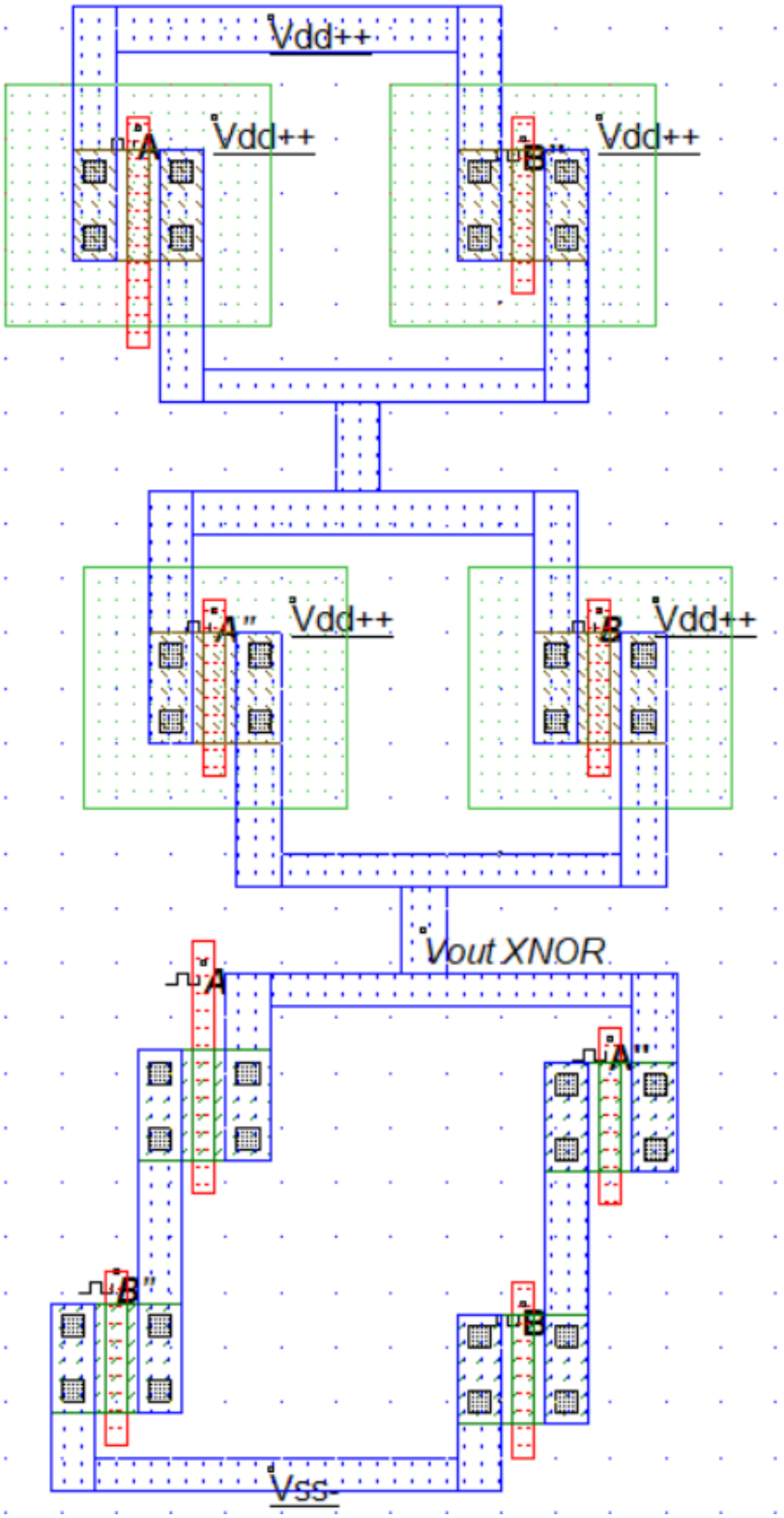

Figure 4: Design layout of XNOR-Gate using 1 Finger MOS

6 Specification

Table 3: MOSFET Dimensions for nMOS and pMOS Transistors

MOS	**Width** (μm)	**Length** (μm)	**Width** (λ)	**Length** (λ)
nMOS	0.600	0.120	10	2
pMOS	0.600	0.120	10	2

Table 4: Parameters of Input Clock Signal for XOR-Gate and XNOR-Gate

Parameter	**Value**	**Unit**
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.225	ns
Rise Time (tr)	0.001	ns
Time High (th)	0.225	ns
Fall Time (tf)	0.001	ns

(a) Input clock signal of A

Parameter	**Value**	**Unit**
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.452	ns
Rise Time (tr)	0.001	ns
Time High (th)	0.452	ns
Fall Time (tf)	0.001	ns

(b) Input clock signal of B

Table 5: Parameters of Input Clock Signal for XOR-Gate and XNOR-Gate

Parameter	**Value**	**Unit**
High Level (V)	0.00	V
Low Level (V)	5.00	V
Time Low (tl)	0.225	ns
Rise Time (tr)	0.001	ns
Time High (th)	0.225	ns
Fall Time (tf)	0.001	ns

(a) Input clock signal of $\bar{A}$

Parameter	**Value**	**Unit**
High Level (V)	0.00	V
Low Level (V)	5.00	V
Time Low (tl)	0.452	ns
Rise Time (tr)	0.001	ns
Time High (th)	0.452	ns
Fall Time (tf)	0.001	ns

(b) Input clock signal of $\bar{B}$

Table 6: Parameters for Vdd+ and Vss-

Parameter	**Value**	**Unit**
Vdd+	5.00	V
Vss-	0.00	V

7 Output Waveshape

7.1 CMOS XOR Gate

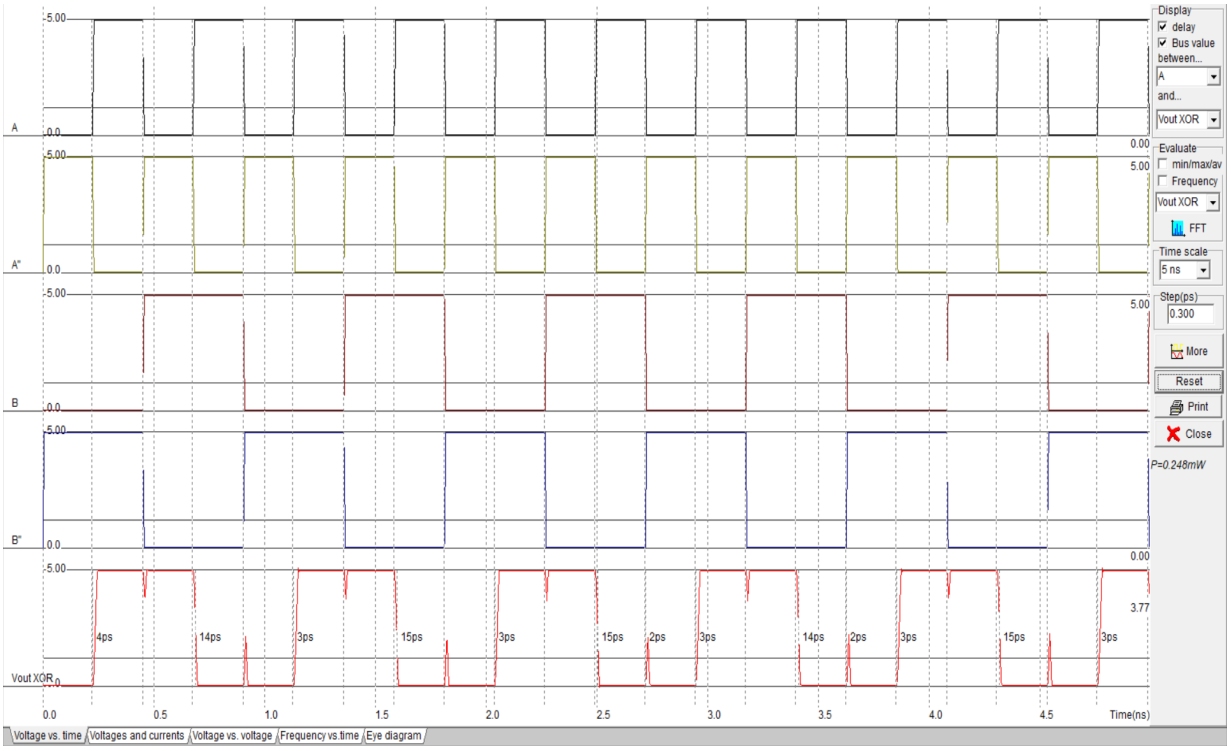

Figure 5: Output Waveshape of XOR-Gate using 1 Finger MOS

7.2 CMOS XNOR Gate

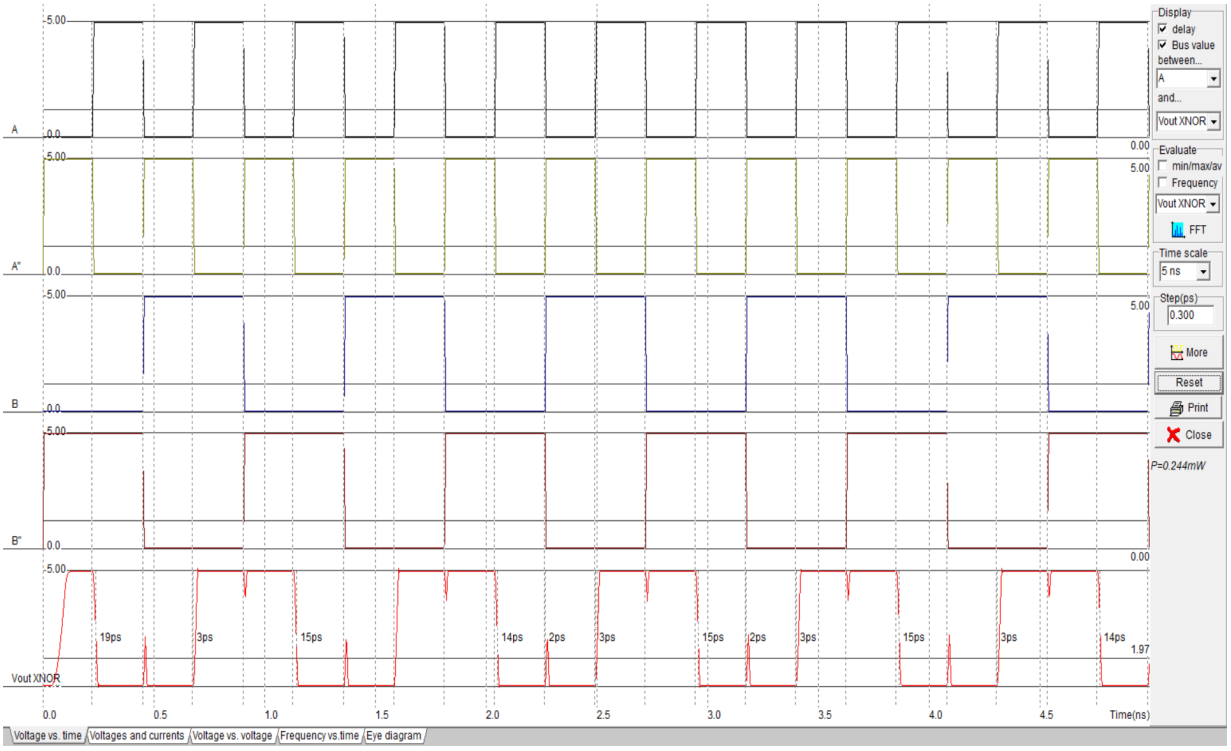

Figure 6: Output Waveshape of XNOR-Gate using 1 Finger MOS

8 Discussion

The characteristics of CMOS XOR and XNOR gates were analyzed based on the input signals A and B and the corresponding output signal Y. It was observed that the output of the XOR gate was the complement of the output of the XNOR gate for all input combinations, indicating that they are logical inverses of each other. The truth tables confirmed that when the XOR gate output is logic high, the XNOR gate output is logic low, and vice versa.

During testing, the XOR gate exhibited some voltage fluctuations during state transitions, which were also present in the XNOR gate. This behavior in the XOR and XNOR gate could be attributed to the charge and discharge dynamics of its pMOS and nMOS transistors during switching. Despite these fluctuations, both gates adhered to the expected logical behavior as outlined in the truth table.