1 Experiment No. 2

2 Experiment Title

Design and Analyze CMOS Inverter and Tristate Inverter ensuring proper DRC using MICROWIND 3.0

3 Objective

The main objectives of this report are:

- To design and simulate a CMOS inverter using MICROWIND 3.0.
- To ensure proper compliance with Design Rule Check (DRC) requirements during the design process.
- To design and simulate a tri-state inverter using MICROWIND 3.0
- To analyze the functionality and switching characteristics of both CMOS and tri-state inverters.

4 Theory

4.1 CMOS Inverter

A CMOS inverter, also known as a complementary metal-oxide-semiconductor inverter, is the most basic building block in digital electronics. It consists of a PMOS (p-type MOSFET) and an NMOS (n-type MOSFET) transistor connected in a complementary manner. The CMOS inverter has two input states: logic 0 (low) and logic 1 (high). The output switches between the supply voltage (logic 1) and ground (logic 0), depending on the input.

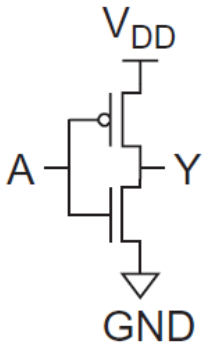


Figure 1: CMOS Inverter

Truth Table for CMOS Inverter:

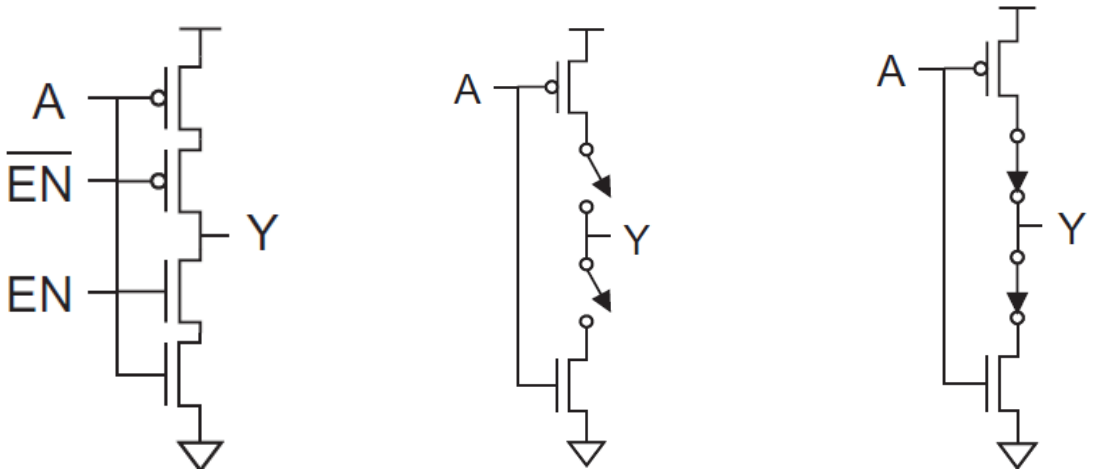
Input (A)	Output (Y)
0	1
1	0

Table 1: Truth table of CMOS inverter

The PMOS transistor is ON when the input is low (logic 0), connecting the output to the supply voltage (V_{DD}), producing a logic high output. The NMOS transistor is OFF in this state, preventing current from flowing to the ground. Conversely, when the input is high (logic 1), the NMOS transistor is ON, connecting the output to ground (logic 0), while the PMOS transistor is OFF. This complementary action ensures low power dissipation, as current flows only during switching events.

4.2 Tri-state Inverter

A tri-state inverter extends the functionality of a CMOS inverter by adding an enable signal, which controls the output state. In addition to logic 0 and 1, the tri-state inverter can have a high-impedance state (Z), which effectively disconnects the output from the circuit. This is useful in bus systems where multiple devices share the same communication line.



(a) Tristate Inverter (b) EN=0 , Y='Z' (c) EN=1 , Y=$\bar{A}$

Figure 2: Tristate Inverter

Truth Table for Tri-state Inverter:

Input (A)	Enable (EN)	Output (Y)
0	1	1
1	1	0
X	0	Z

Table 2: Truth table of tri-state inverter

When the enable signal (E) is active (logic 1), the inverter behaves like a normal CMOS inverter, producing an inverted output. When the enable signal is low (logic 0), the output enters a high-impedance (Z) state, effectively disconnecting it from the circuit.

4.3 Working Process of Designing a CMOS Inverter using MICROWIND 3.0

Designing a CMOS inverter in MICROWIND 3.0 involves the following steps:

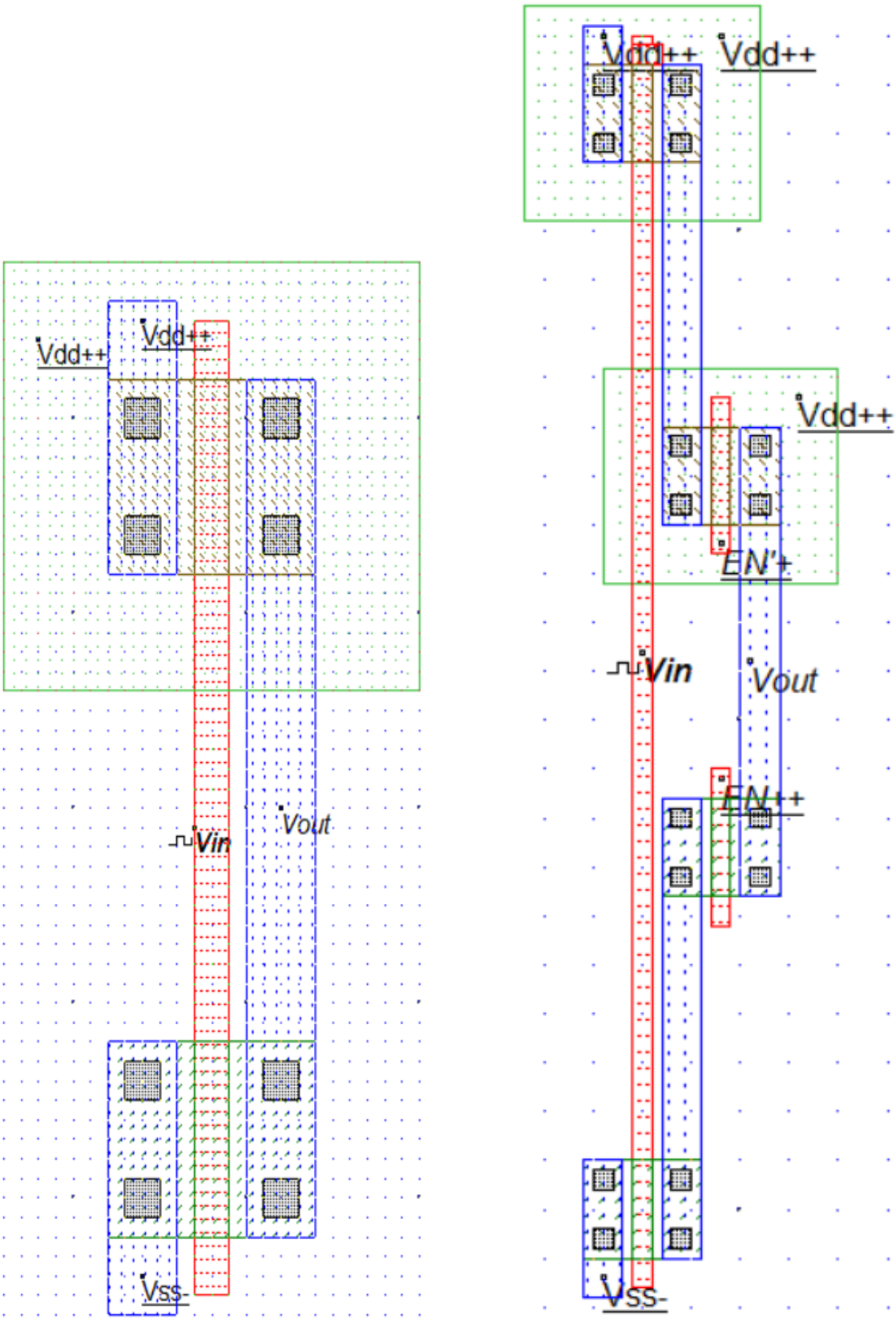
1. **Create a New Layout:** Open MICROWIND 3.0 and create a new project. The tool provides a blank canvas for designing the layout at the transistor level.
2. **Place PMOS and NMOS Transistors:** Using MOS Generator, place a PMOS transistor in the upper part of the layout and an NMOS transistor in the lower part. The transistors are connected at the output node.
3. **Connect Power and Ground:** Connect the source of the PMOS to the power supply (V_{DD}) and the source of the NMOS to the ground.
4. **Define Input and Output:** The input is connected to the gates of both the PMOS and NMOS transistors, while the output is taken from the common drain terminal.
5. **Run DRC:** After completing the layout, run the DRC tool to ensure that the design follows all the required fabrication rules.
6. **Simulate the Inverter:** Perform a transient simulation to observe the input-output behavior and verify the inverter operation.

4.4 Working Process of Designing a Tri-state Inverter using MICROWIND 3.0

Designing a tri-state inverter follows a similar process but with an additional enable signal. The steps are as follows:

1. **Create a New Layout:** Start a new project in MICROWIND 3.0.
2. **Place Transistors:** Place PMOS and NMOS transistors as in the CMOS inverter design. Additionally, include a control transistor that manages the enable signal.
3. **Connect Enable Signal:** The enable signal controls whether the output is active or in a high-impedance state by controlling DC power supply.
4. **Connect Input and Output:** Connect the input to the gates of the PMOS and NMOS transistors. The output is taken from the drains.
5. **Run DRC:** Check the layout using the DRC tool to ensure that no design rules are violated.
6. **Simulate the Tri-state Inverter:** Simulate the inverter to check how the circuit behaves with the enable signal in both active and inactive states.

5 Schematic Layout



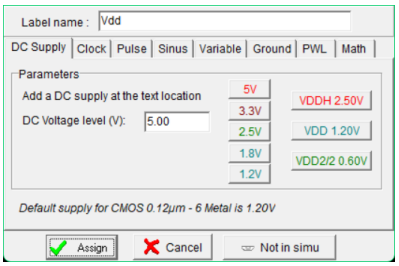
(a) CMOS Inverter

(b) Tristate Inverter

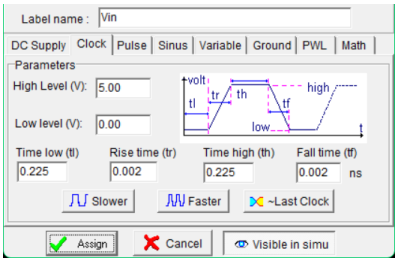
Figure 3: Design layout of CMOS Inverter and Tristate Inverter

6 Specification

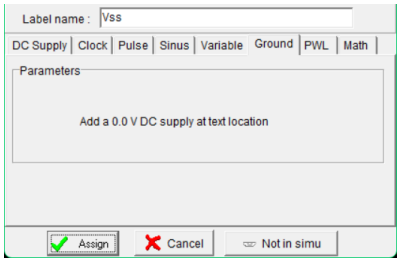
1. CMOS Inverter



(a) Vdd



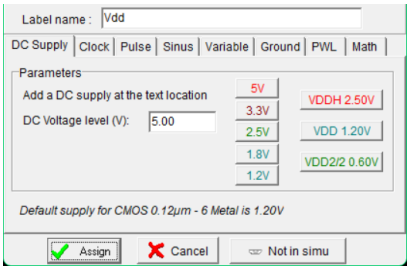
(b) Vin



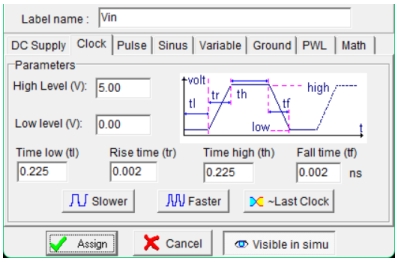
(c) Vss

Figure 4: Specifications of CMOS Inverter

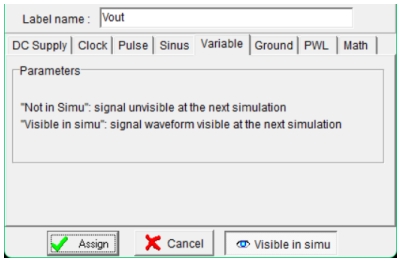
2. Tristate Inverter



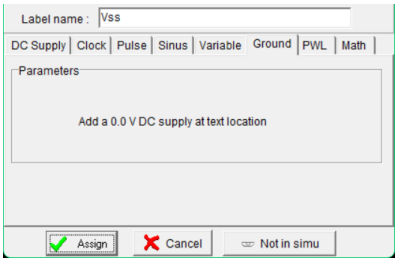
(a) Vdd



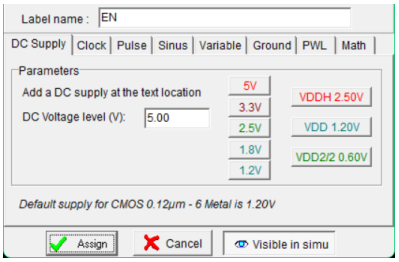
(b) Vin



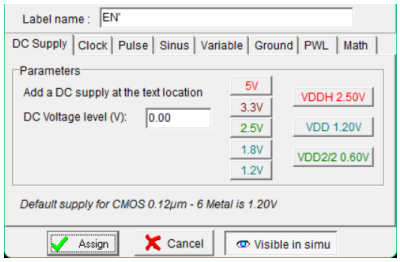
(c) Vout



(d) Vss



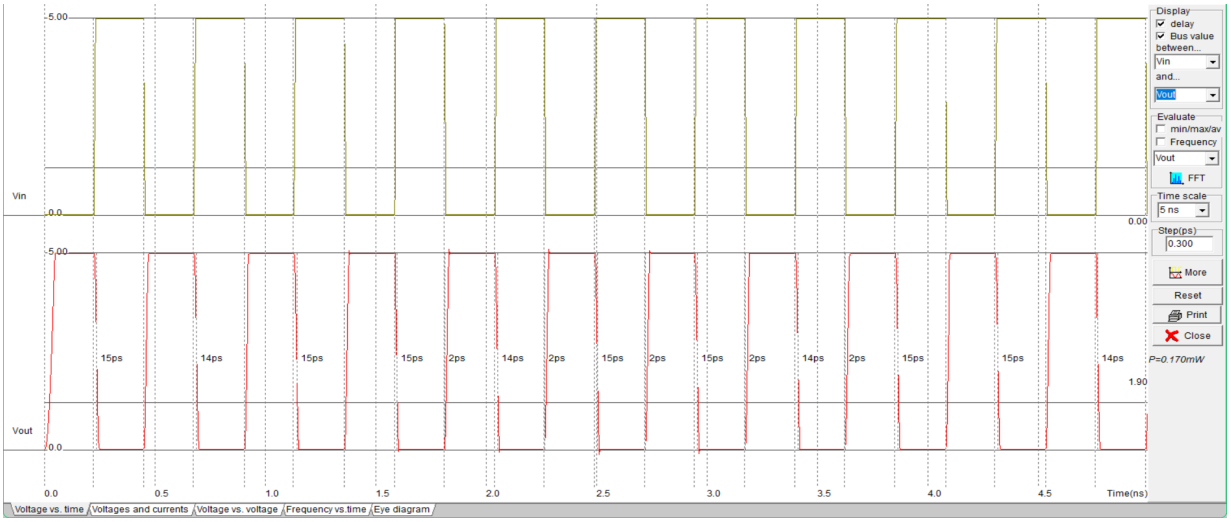
(e) EN



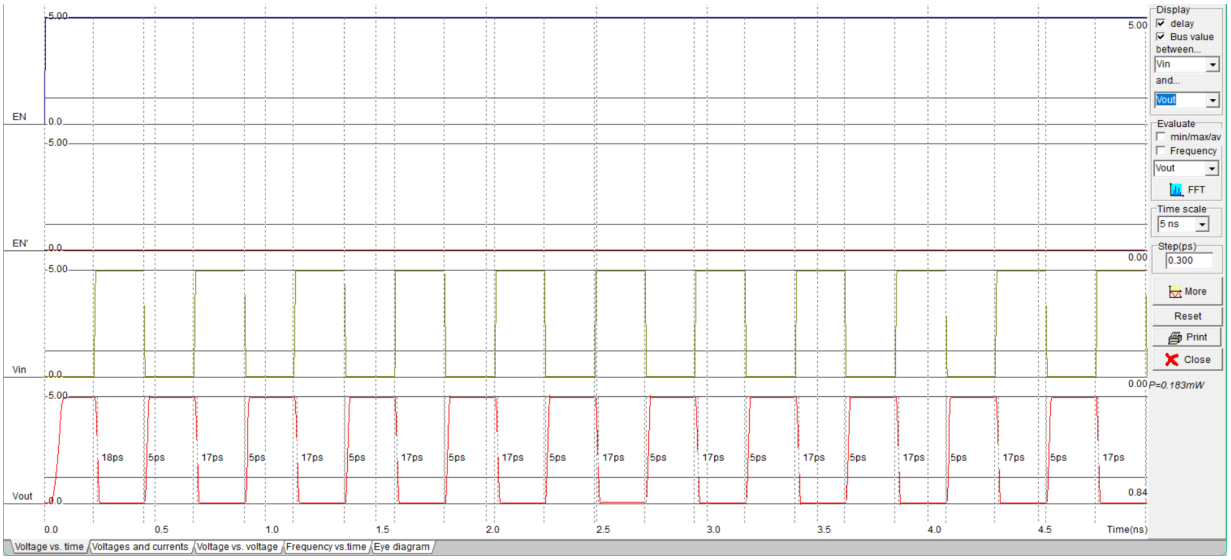
(f) EN'

Figure 5: Specifications of Tristate Inverter

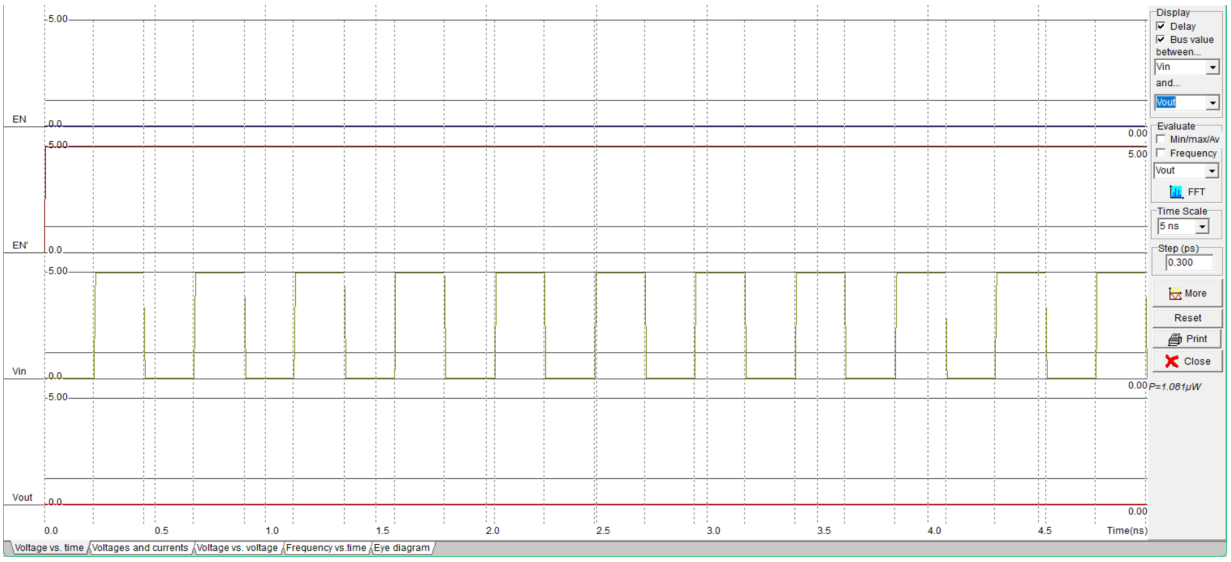
7 Output Waveshape



(a) CMOS Inverter



(b) Tristate Inverter when EN=5.00V & EN'=0.00V



(c) Tristate Inverter when EN=0.00V & EN'= 5.00V

Figure 6: Output Waveshape of Fabricated CMOS Inverter and Tristate Inverter

8 Discussion

In this experiment, the design and analysis of CMOS and tri-state inverters were carried out using MICROWIND 3.0, with particular emphasis on ensuring proper Design Rule Check (DRC) compliance. The CMOS inverter was designed by placing a PMOS and NMOS transistor in a complementary configuration. The input signal $(Vin)$was connected to the gates of both transistors, while the output$(Vout)$ was obtained from the common drain. It was observed during the simulation that the inverter properly switched between logic states, confirming the correct operation of the device.

For the tri-state inverter, instead of using an additional transistor, enable signals EN and EN' were manually created. These signals controlled the output state, with EN connected to 5V and EN' to 0V, and vice versa. The inverter successfully transitioned between active and high-impedance states during the simulation, validating the manual control of the enable signals.

Overall, the designs were successfully simulated, with both inverters meeting the required operational characteristics. The low power dissipation of the CMOS inverter and the correct functionality of the tri-state inverter in managing output states were observed, confirming the designs' effectiveness.