1 Experiment No. 3

2 Experiment Title

Design and Analyze a 2 Input NAND and AND Gate Using 1 Finger and 2 Finger MOS on MICROWIND 3.0

3 Objective

The main objectives of this report are:

- To design and simulate NAND & AND gate using 1-finger and 2-finger MOS transistors.
- To analyze the operation and characteristics of 2-input NAND and AND gates.
- To understand the logical behavior and verify the truth table of NAND and AND gates using input signals A and B.

4 Theory

4.1 2-Input CMOS NAND Gate

A 2-input CMOS NAND gate is constructed using both PMOS and NMOS transistors. When either of the inputs A or B is at logic '0' (low), one of the PMOS transistors will be ON, allowing the output F to be pulled high, resulting in logic '1' at the output. Only when both inputs are at logic '1', both NMOS transistors will conduct, pulling the output low (logic '0'). The logic function of the 2-input CMOS NAND gate can be expressed as:

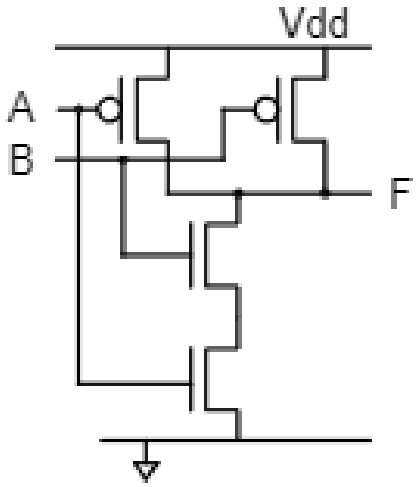


Figure 1: CMOS NAND-Gate

$$F = \overline{A \cdot B}$$

The truth table for a 2-input NAND gate is shown below:

Table 1: Truth Table for 2-Input CMOS NAND Gate

A	B	F (NAND Output)
0	0	1
0	1	1
1	0	1
1	1	0

4.2 2-Input CMOS AND Gate

The 2-input CMOS AND gate can be derived by using a 2-input NAND gate followed by a CMOS inverter. This configuration results in the output F being high only when both inputs A and B are high. The logic function of the 2-input CMOS AND gate is given as:

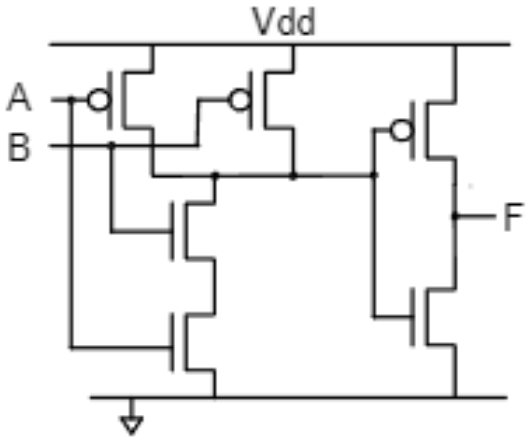


Figure 2: CMOS AND-Gate

$$F = A \cdot B$$

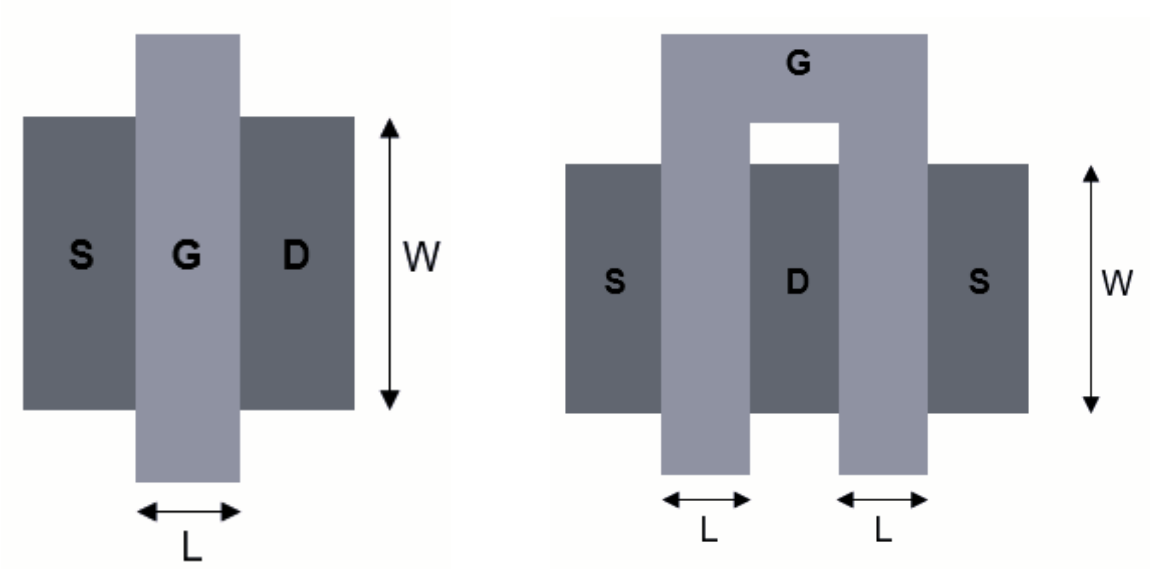
The truth table for a 2-input AND gate is shown below:

Table 2: Truth Table for 2-Input CMOS AND Gate

A	B	F (AND Output)
0	0	0
0	1	0
1	0	0
1	1	1

4.3 1-Finger and 2-Finger MOS Fabrication

MOS transistors can be designed using different fabrication techniques to optimize the performance, area, and power consumption.
In the context of semiconductor design, **"1 finger MOS"** refers to a single-gate Metal Oxide Semiconductor (MOS) transistor where the gate electrode is a single, continuous strip, while **"2 finger MOS"** means the gate is divided into two separate, parallel strips, essentially creating two smaller "fingers" of the gate, all sharing the same source and drain regions; the key difference is the number of gate fingers, which affects the transistor's electrical characteristics, particularly its current handling capability and parasitic capacitance.
By dividing the gate into multiple fingers, the effective gate width increases, allowing for a higher current flow while maintaining a smaller overall transistor area.



(a) 1 Finger MOS (b) 2 Finger MOS

Figure 3: Multiple fingers layout (MOSFET transistor)

4.3.1 Advantages

1. **Improved RF performance:** Multi-finger design reduces gate resistance, leading to better high-frequency performance in RF circuits.

2. **Lower parasitic capacitance:** Dividing the gate into smaller sections can decrease parasitic capacitance, improving circuit speed and power efficiency.

3. **Better matching:** When designing identical transistors with multiple fingers, the matching between them is often improved due to the similar layout and reduced variations.

5 Schematic Layout

5.1 NAND GATE using 1 Finger MOS

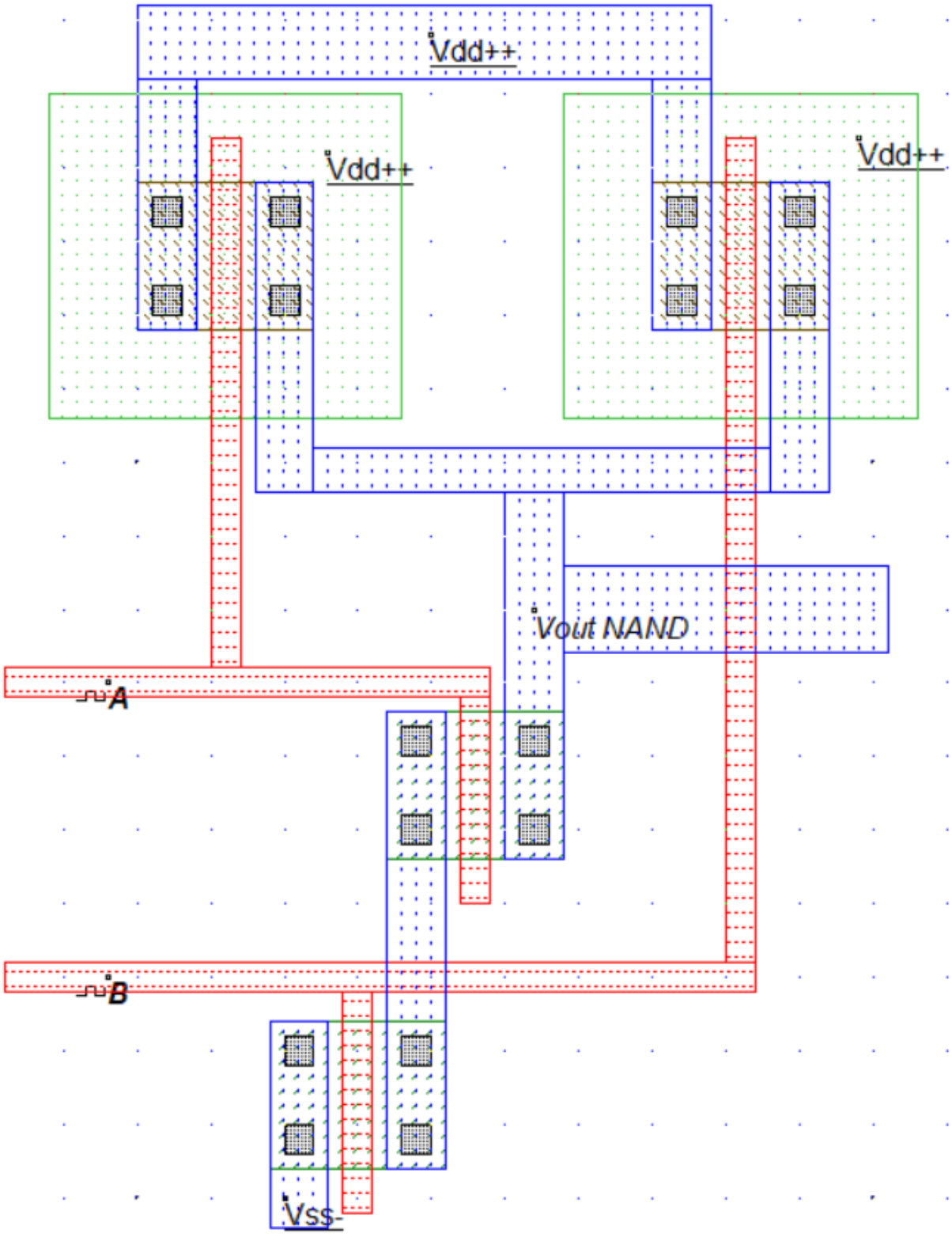


Figure 4: 2 Input NAND-Gate using 1 Finger MOS

5.2 AND Gate using 1 Finger MOS

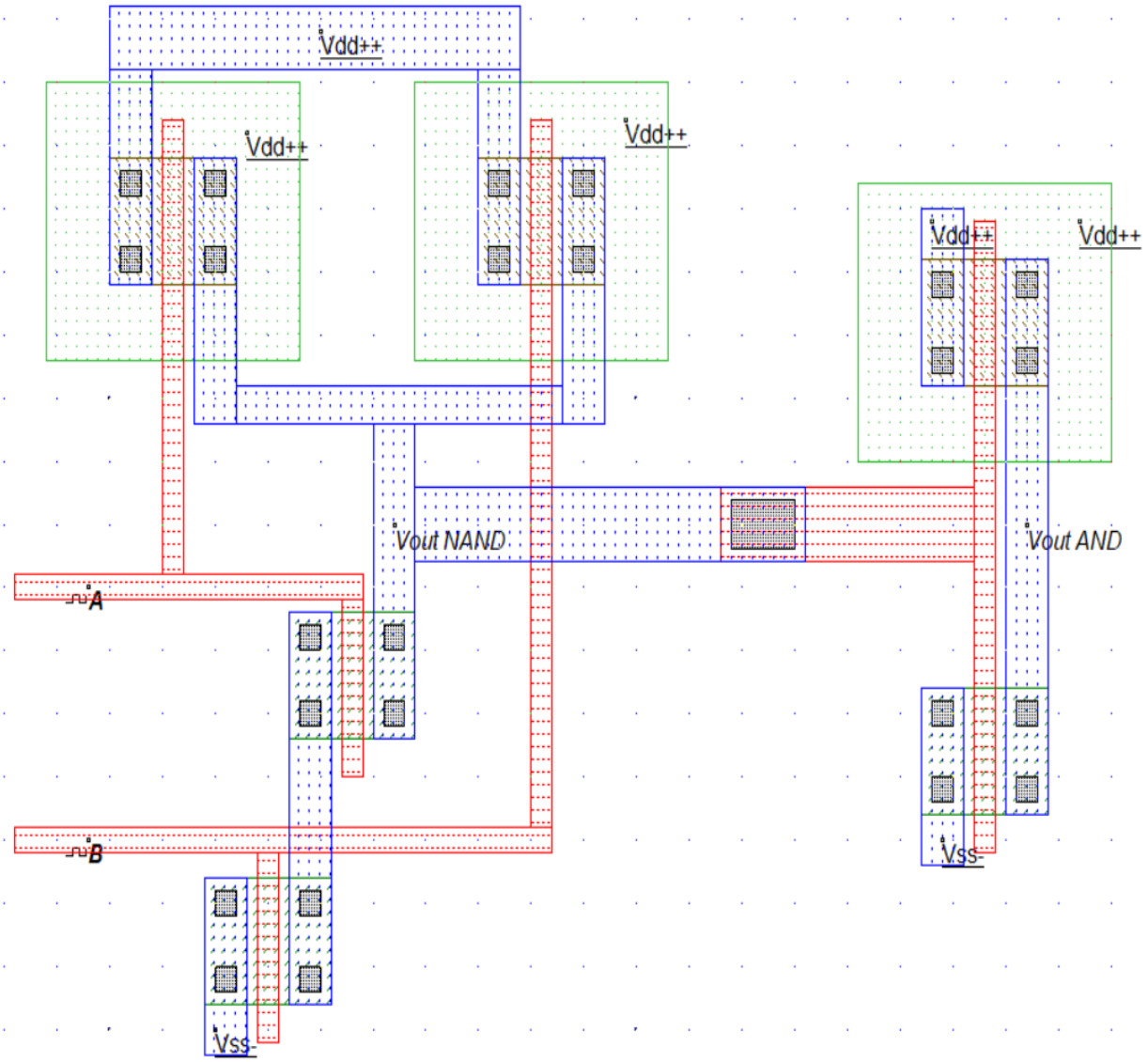


Figure 5: 2 Input AND-Gate using 1 Finger MOS and a CMOS

5.3 NAND Gate using 2 Finger MOS

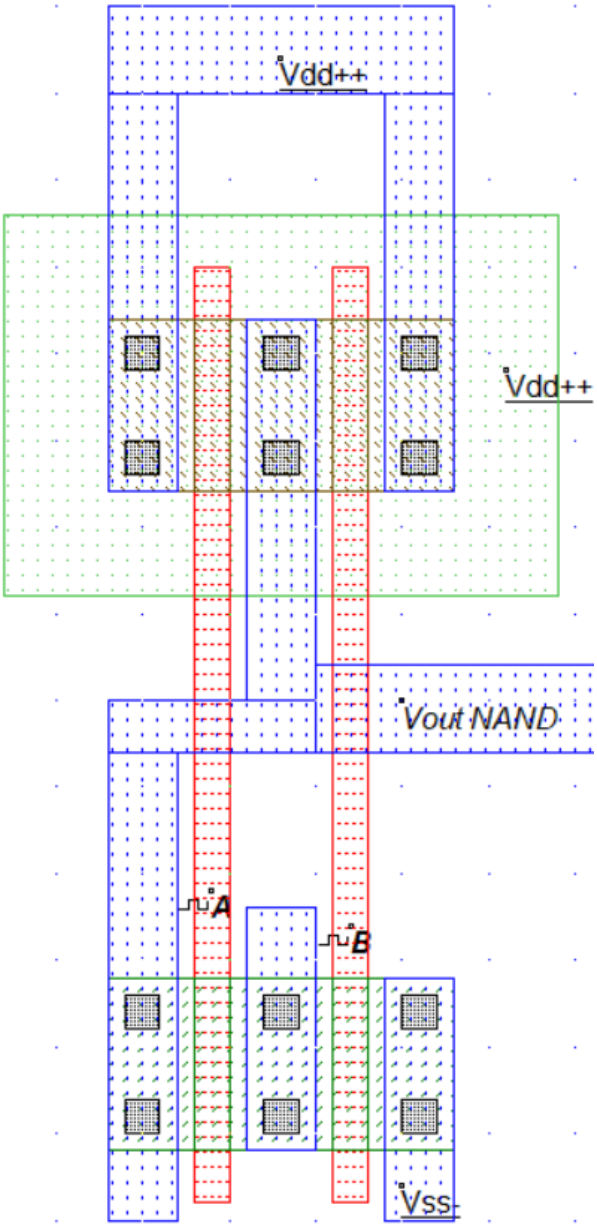


Figure 6: 2 Input NAND-Gate using 2 Finger MOS

5.4 AND Gate using 2 Finger MOS

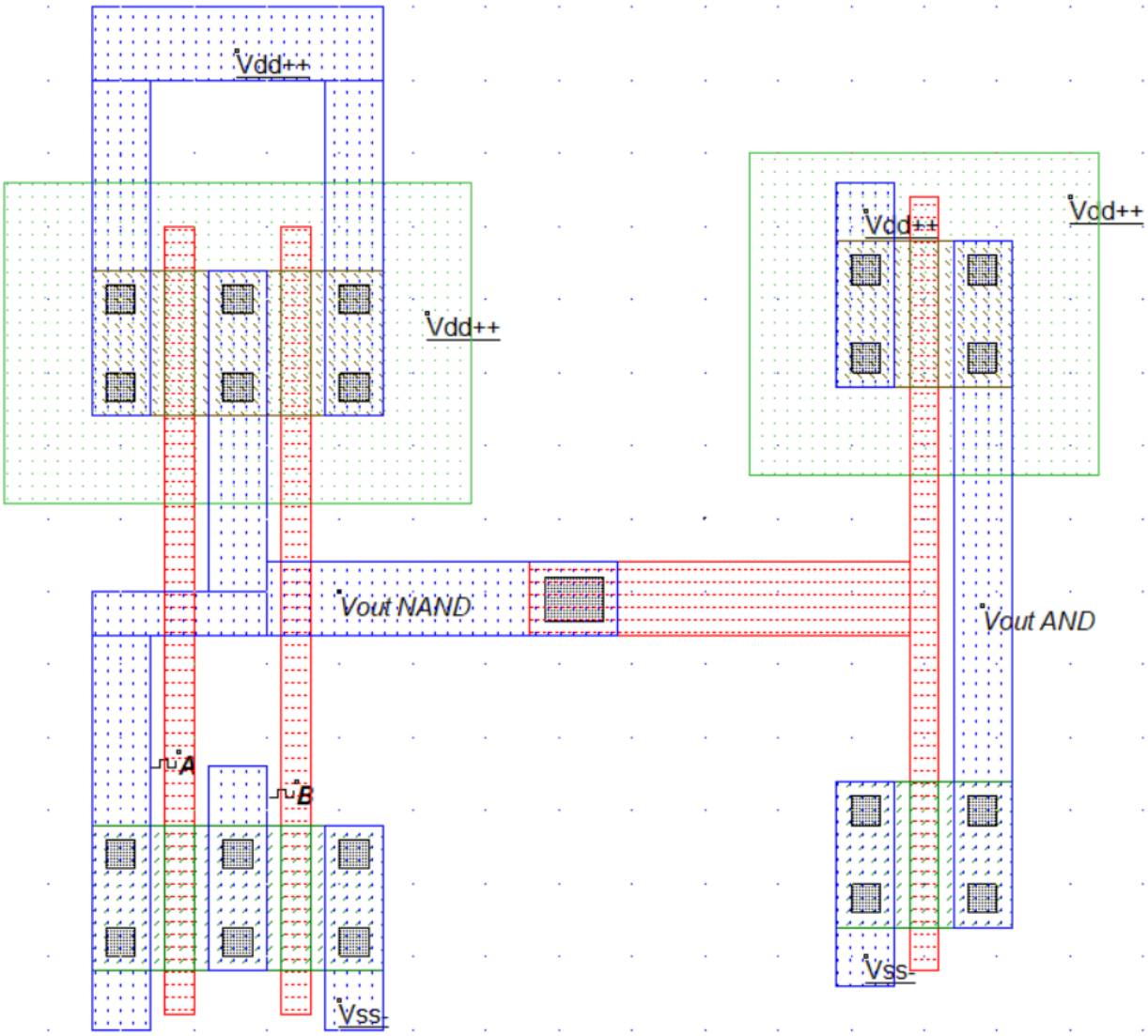


Figure 7: 2 Input AND-Gate using 2 Finger MOS and a CMOS

6 Specification

Table 3: MOSFET Dimensions for nMOS and pMOS Transistors

MOS	**Width** (μm)	**Length** (μm)	**Width** (λ)	**Length** (λ)
nMOS	0.600	0.120	10	2
pMOS	0.600	0.120	10	2

Table 4: Parameters of Input Clock Signal for 1 Finger NAND-Gate and AND-Gate

Parameter	**Value**	**Unit**
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.225	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.225	ns
Fall Time (tf)	0.002	ns

(a) Input clock signal of A

Parameter	**Value**	**Unit**
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.452	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.452	ns
Fall Time (tf)	0.002	ns

(b) Input clock signal of B

Table 5: Parameters of Input Clock Signal for 2 Finger NAND-Gate and AND-Gate

Parameter	**Value**	**Unit**
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.452	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.452	ns
Fall Time (tf)	0.002	ns

(a) Input clock signal of A

Parameter	**Value**	**Unit**
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.225	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.225	ns
Fall Time (tf)	0.002	ns

(b) Input clock signal of B

Table 6: Parameters for Vdd+ and Vss-

Parameter	**Value**	**Unit**
Vdd+	5.00	V
Vss-	0.00	V

7 Output Waveshape

7.1 NAND-Gate & AND-Gate using 1 Finger MOS

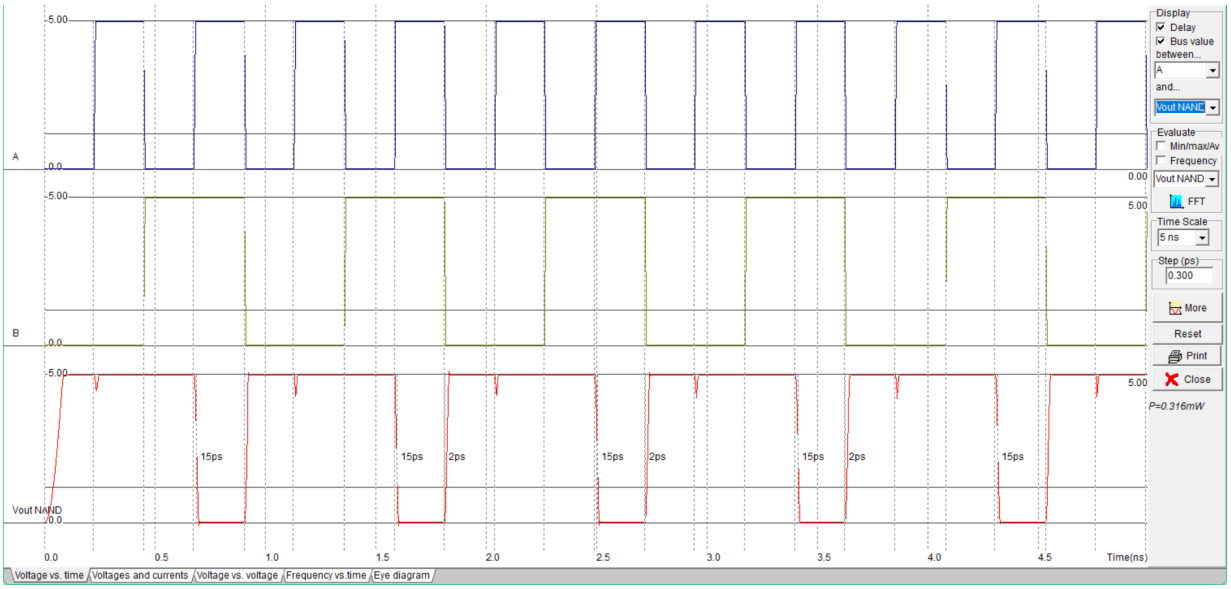


Figure 8: Output Waveshape of 2 Input NAND-Gate using 1 Finger MOS

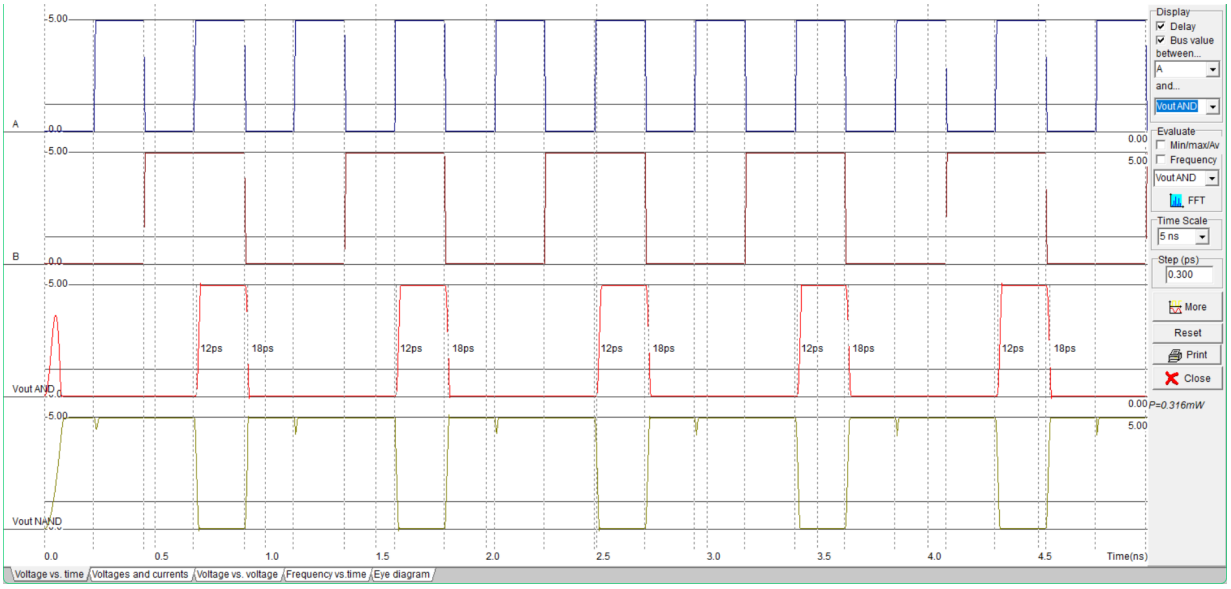


Figure 9: Output Waveshape of 2 Input NAND-Gate and AND-Gate using 1 Finger MOS

7.2 NAND-Gate & AND-Gate using 2 Finger MOS

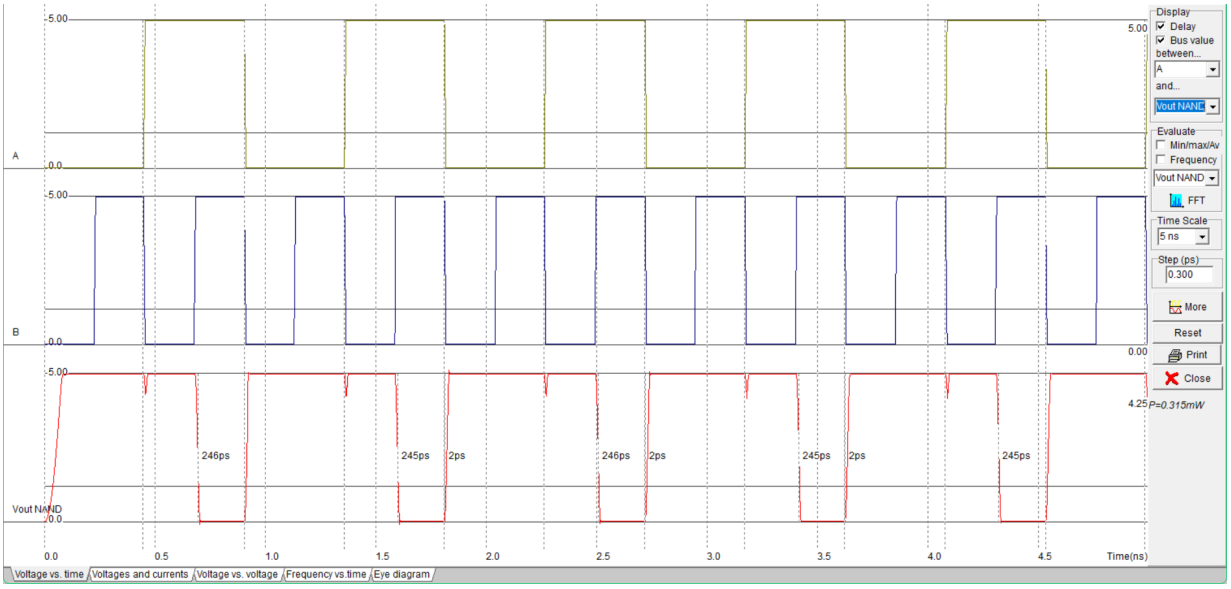


Figure 10: Output Waveshape of 2 Input NAND-Gate using 2 Finger MOS

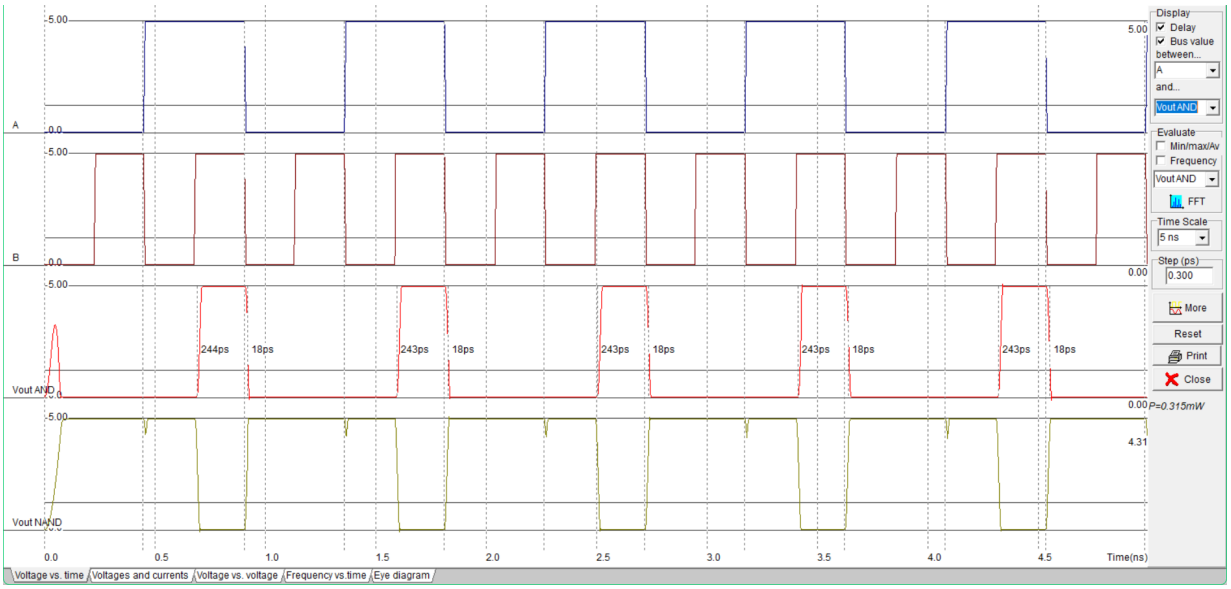


Figure 11: Output Waveshape of 2 Input NAND-Gate and AND-Gate using 2 Finger MOS

8 Discussion

The characteristics of 2-input CMOS NAND and AND gates were analyzed based on the input signals A and B and the corresponding output signal F. It was observed that the output of the AND gate was the complement of the output of the NAND gate for all input combinations, indicating that they are logical inverses of each other. The truth tables verified that when the AND gate output is logic high, the NAND gate output is logic low, and vice versa.

During testing, the NAND gate exhibited some initial voltage flickering during state transitions, which was not observed in the AND gate. This behavior in the NAND gate was likely due to initial charge and discharge dynamics associated with its internal structure and switching characteristics. Despite the flickering, both gates followed the expected logical behavior as described in the truth table.