1 Experiment No. 4

2 Experiment Title

Design and Analyze a 2 Input NOR and OR Gate Using 1 Finger and 2 Finger MOS on MICROWIND 3.0

3 Objective

The main objectives of this report are:

- To design and simulate NOR & OR gate using 1-finger and 2-finger MOS transistors.
- To analyze the operation and characteristics of 2-input NOR and OR gates.
- To understand the logical behavior and verify the truth table of NOR and OR gates using input signals A and B.

4 Theory

4.1 2-Input CMOS NOR Gate

A 2-input CMOS NOR gate is constructed using both pMOS and nMOS transistors. When either of the inputs A or B is at logic '1' (high), one of the nMOS transistors will be ON, allowing the output F to be pulled low, resulting in logic '0' at the output. Only when both inputs are at logic '0', both pMOS transistors will conduct, pulling the output high (logic '1'). The logic function of the 2-input CMOS NOR gate can be expressed as:

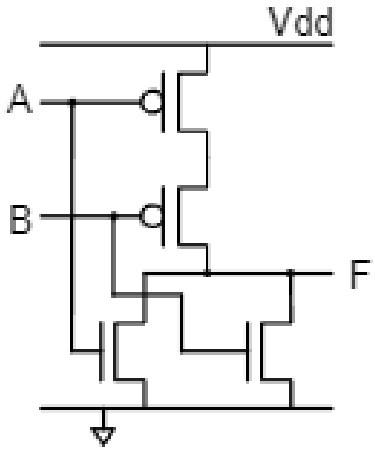


Figure 1: CMOS NOR-Gate

$$F = \overline{A + B}$$

where: - A and B are the inputs, and - F is the output of the NOR gate.

The truth table for a 2-input NOR gate is shown below:

Table 1: Truth Table for 2-Input CMOS NOR Gate

A	B	F (NOR Output)
0	0	1
0	1	0
1	0	0
1	1	0

4.2 2-Input CMOS OR Gate

A 2-input CMOS OR gate can be constructed by first creating a 2-input NOR gate using both pMOS and nMOS transistors, and then inverting the output. When either of the inputs A or B is at logic '1' (high), the output of the NOR gate is pulled low, and inverting this low output results in logic '1'. When both inputs are at logic '0', the NOR gate output is pulled high, and inverting this high output results in logic '0' at the final output. The logic function of the 2-input CMOS OR gate can be expressed as:

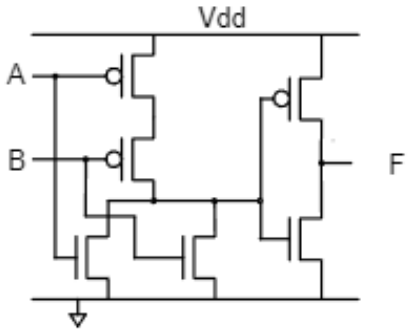


Figure 2: CMOS OR-Gate

$$F = A + B$$

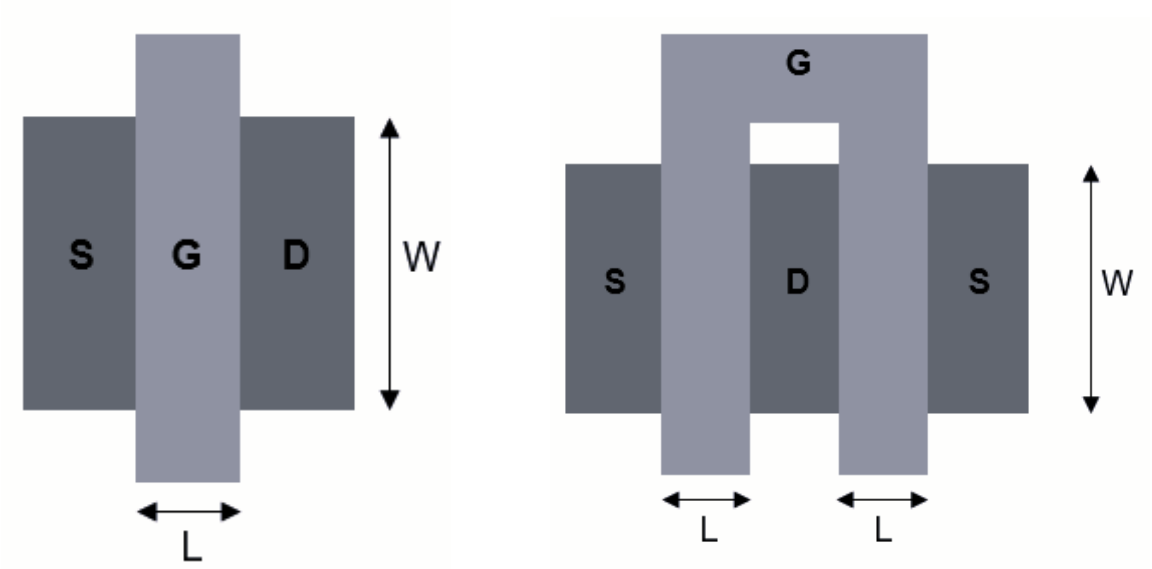
where: - A and B are the inputs, and - F is the output of the OR gate.
The truth table for a 2-input OR gate is shown below:

Table 2: Truth Table for 2-Input CMOS OR Gate

A	B	F (OR Output)
0	0	0
0	1	1
1	0	1
1	1	1

4.3 1-Finger and 2-Finger MOS Fabrication

MOS transistors can be designed using different fabrication techniques to optimize the performance, area, and power consumption.
In the context of semiconductor design, **"1 finger MOS"** refers to a single-gate Metal Oxide Semiconductor (MOS) transistor where the gate electrode is a single, continuous strip, while **"2 finger MOS"** means the gate is divided into two separate, parallel strips, essentially creating two smaller "fingers" of the gate, all sharing the same source and drain regions; the key difference is the number of gate fingers, which affects the transistor's electrical characteristics, particularly its current handling capability and parasitic capacitance.
By dividing the gate into multiple fingers, the effective gate width increases, allowing for a higher current flow while maintaining a smaller overall transistor area.



(a) 1 Finger MOS (b) 2 Finger MOS

Figure 3: Multiple fingers layout (MOSFET transistor)

4.3.1 Advantages

1. **Improved RF performance:** Multi-finger design reduces gate resistance, leading to better high-frequency performance in RF circuits.

2. **Lower parasitic capacitance:** Dividing the gate into smaller sections can decrease parasitic capacitance, improving circuit speed and power efficiency.

3. **Better matching:** When designing identical transistors with multiple fingers, the matching between them is often improved due to the similar layout and reduced variations.

5 Schematic Layout

5.1 NOR Gate using 1 Finger MOS

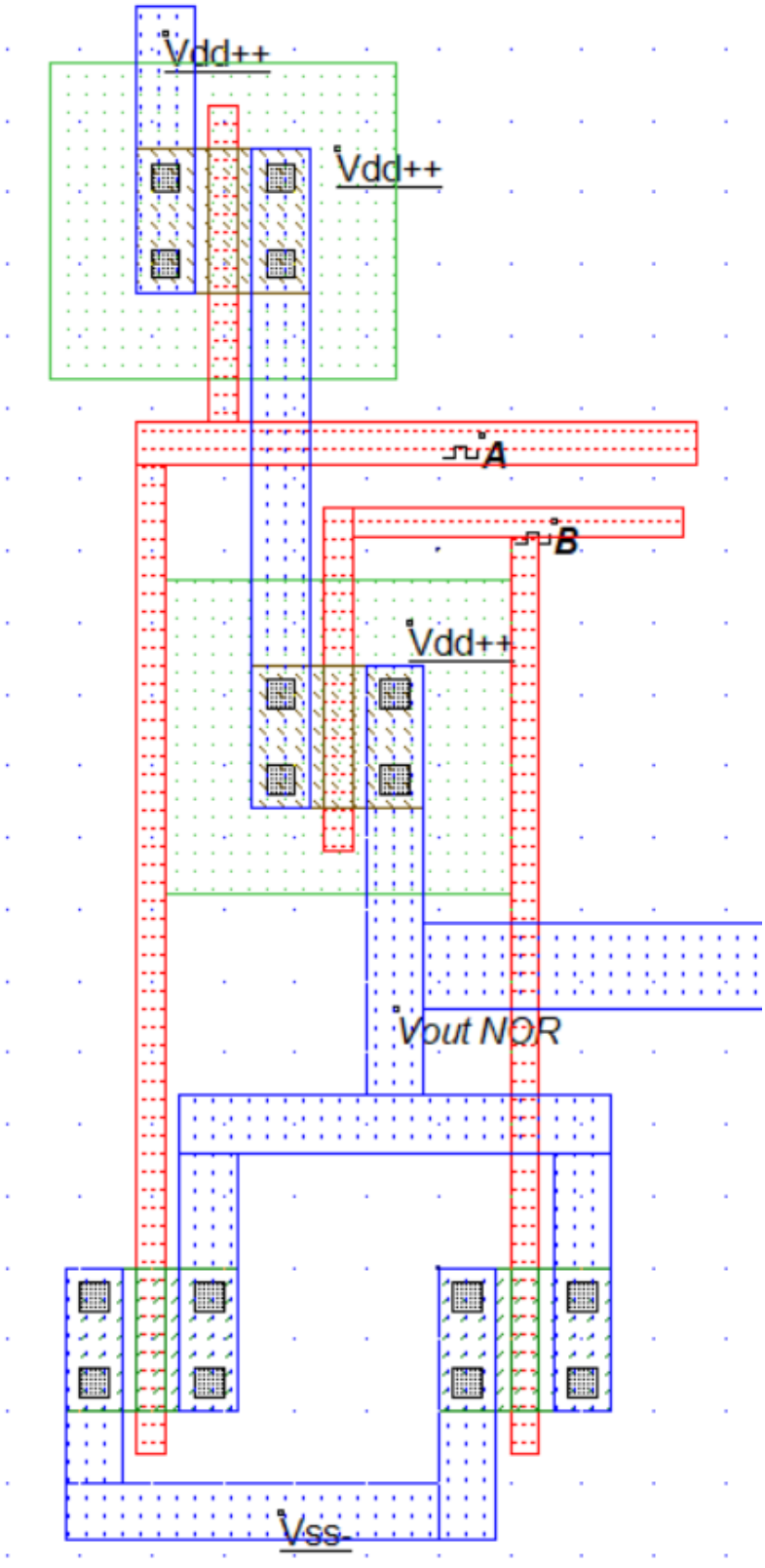


Figure 4: 2 Input NOR-Gate using 1 Finger MOS

5.2 OR Gate using 1 Finger MOS

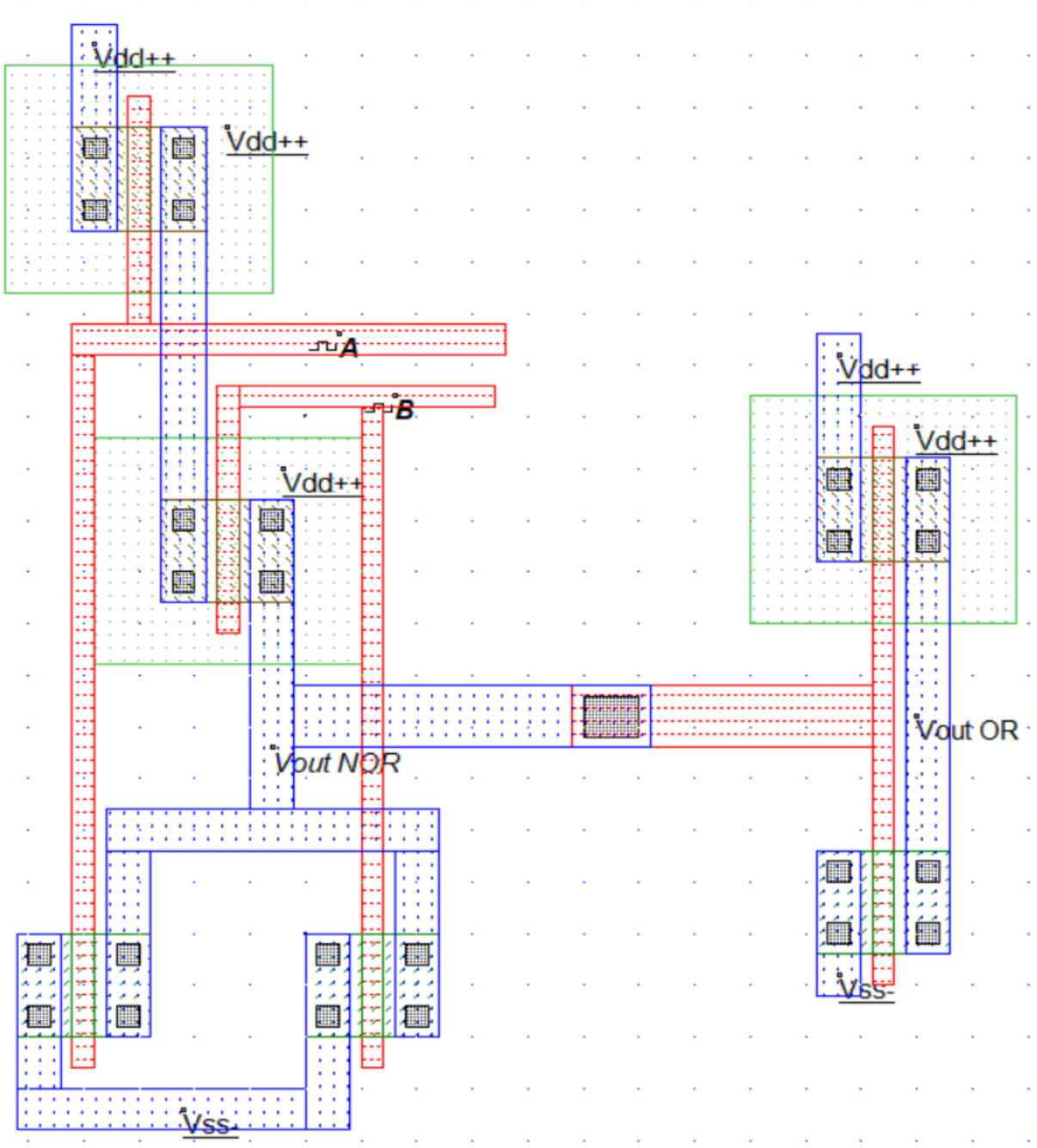


Figure 5: 2 Input OR-Gate using 1 Finger MOS and a CMOS

5.3 NOR Gate using 2 Finger MOS

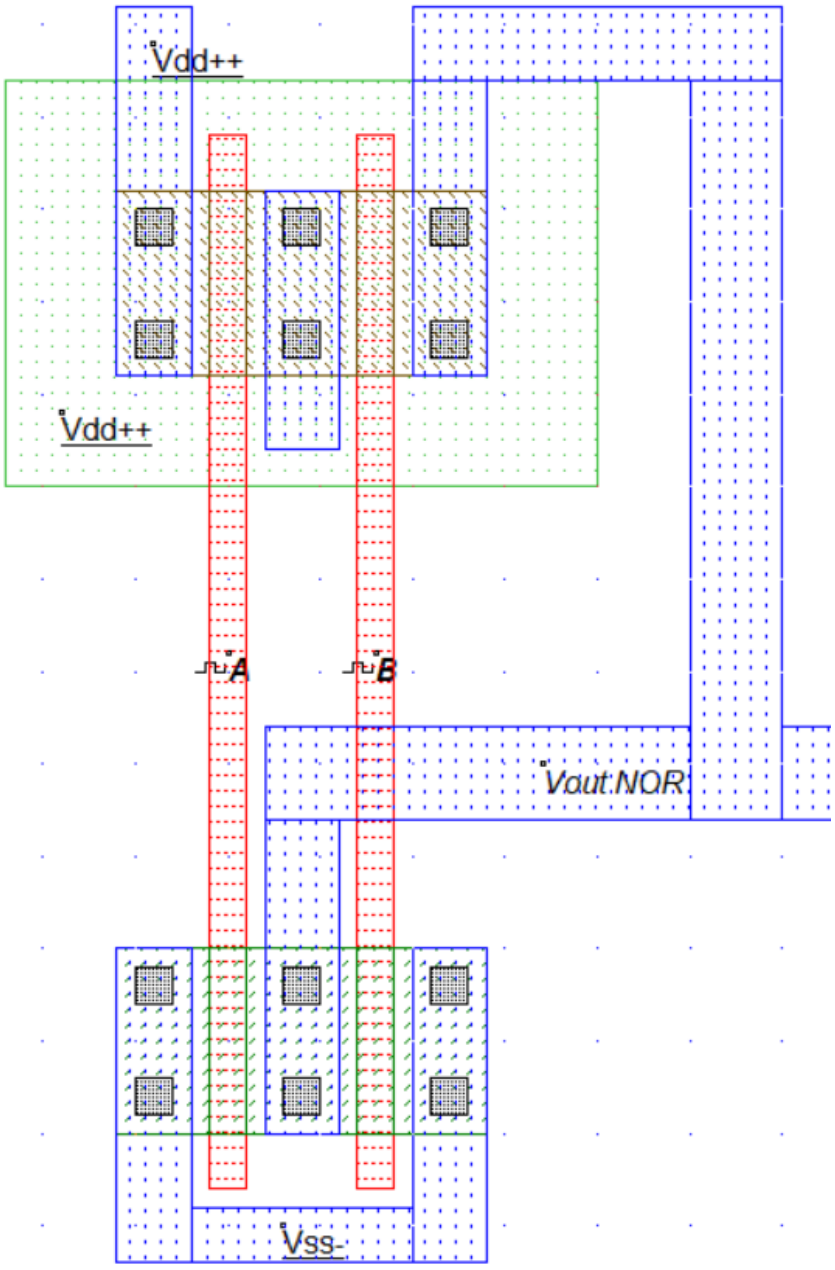


Figure 6: 2 Input NOR-Gate using 2 Finger MOS

5.4 OR Gate using 2 Finger MOS

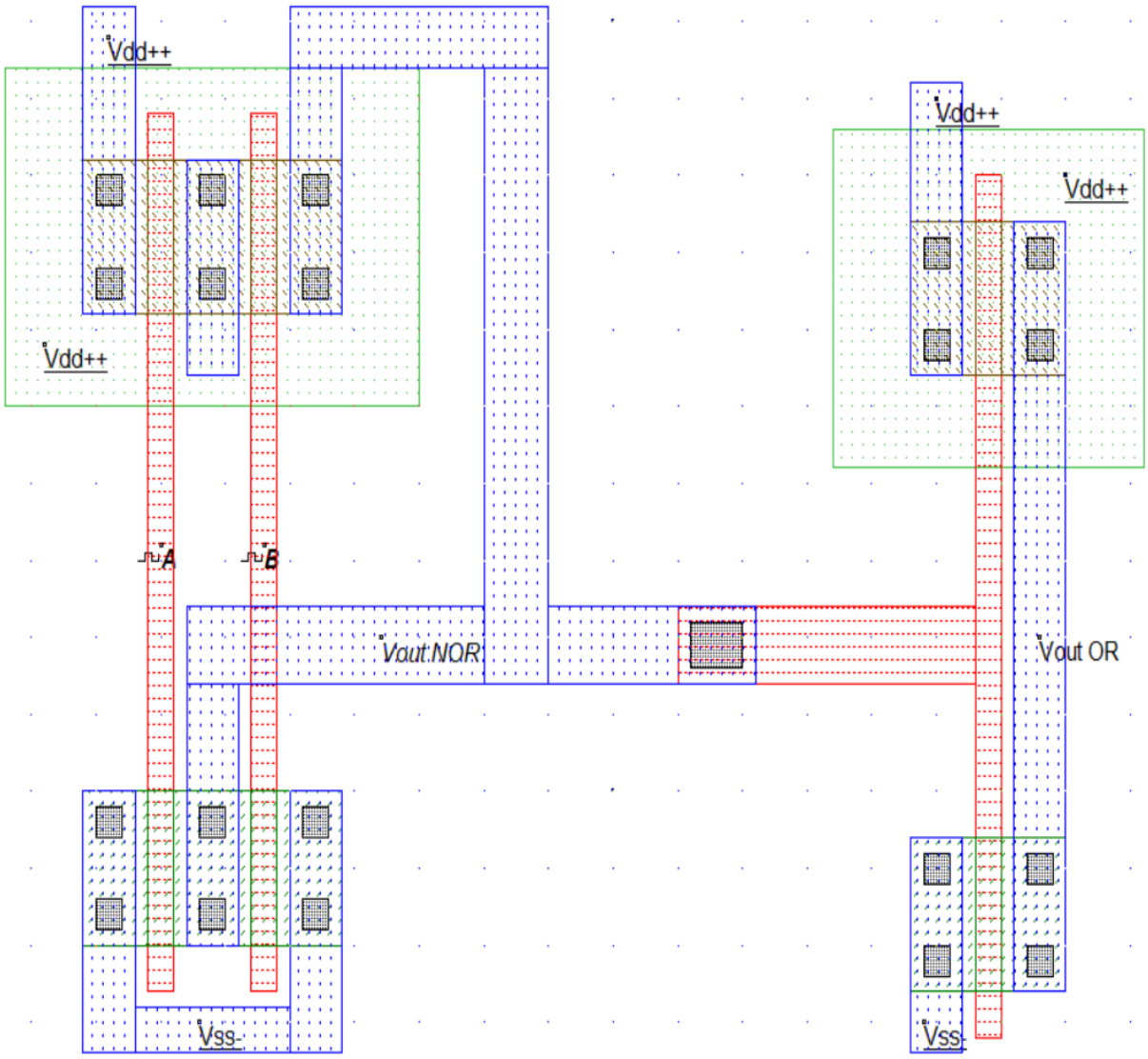


Figure 7: 2 Input OR-Gate using 2 Finger MOS and a CMOS

6 Specification

Table 3: MOSFET Dimensions for nMOS and pMOS Transistors

MOS	**Width** (μm)	**Length** (μm)	**Width** (λ)	**Length** (λ)
nMOS	0.600	0.120	10	2
pMOS	0.600	0.120	10	2

Table 4: Parameters of Input Clock Signal for 1 Finger NOR-Gate and OR-Gate

Parameter	Value	Unit
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.225	ns
Rise Time (tr)	0.001	ns
Time High (th)	0.225	ns
Fall Time (tf)	0.001	ns

(a) Input clock signal of A

Parameter	Value	Unit
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.451	ns
Rise Time (tr)	0.001	ns
Time High (th)	0.451	ns
Fall Time (tf)	0.001	ns

(b) Input clock signal of B

Table 5: Parameters of Input Clock Signal for 2 Finger NOR-Gate and OR-Gate

Parameter	Value	Unit
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.225	ns
Rise Time (tr)	0.001	ns
Time High (th)	0.225	ns
Fall Time (tf)	0.001	ns

(a) Input clock signal of A

Parameter	Value	Unit
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.451	ns
Rise Time (tr)	0.001	ns
Time High (th)	0.451	ns
Fall Time (tf)	0.001	ns

(b) Input clock signal of B

Table 6: Parameters for Vdd+ and Vss-

Parameter	Value	Unit
Vdd+	5.00	V
Vss-	0.00	V

7 Output Waveshape

7.1 NOR-Gate & OR-Gate using 1 Finger MOS

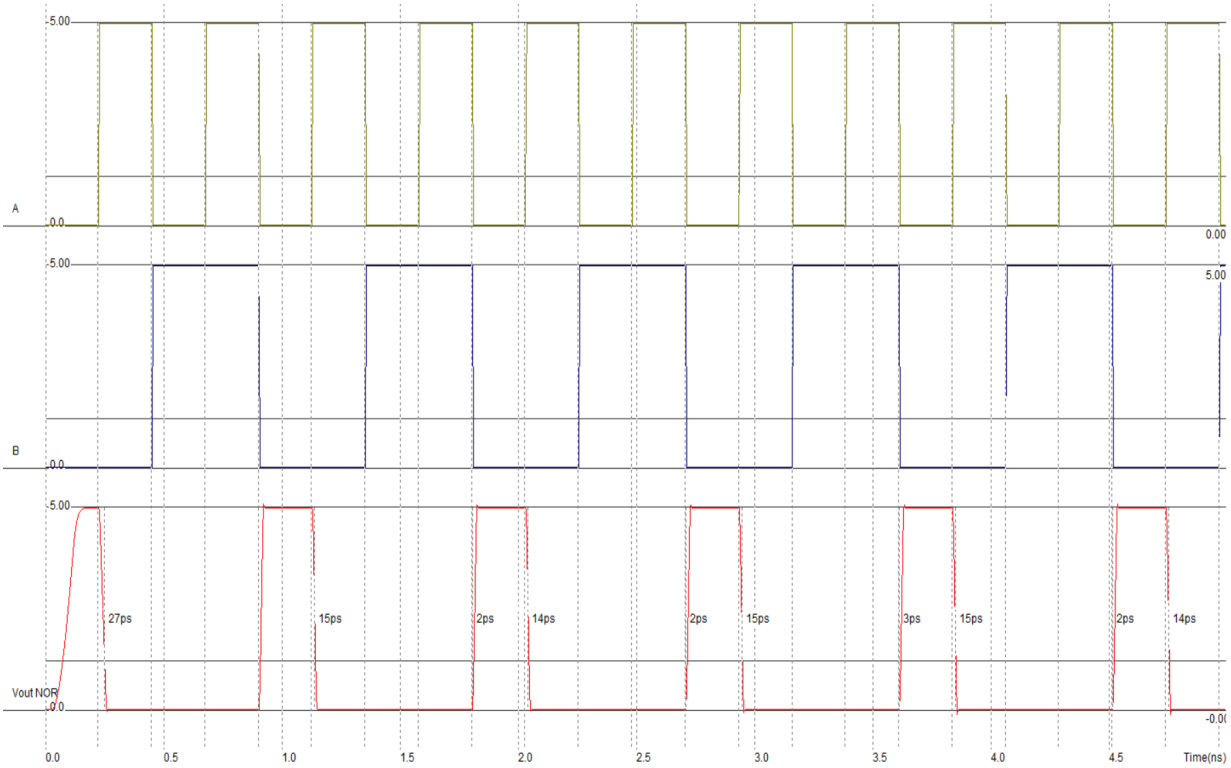


Figure 8: Output Waveshape of 2 Input NOR-Gate using 1 Finger MOS

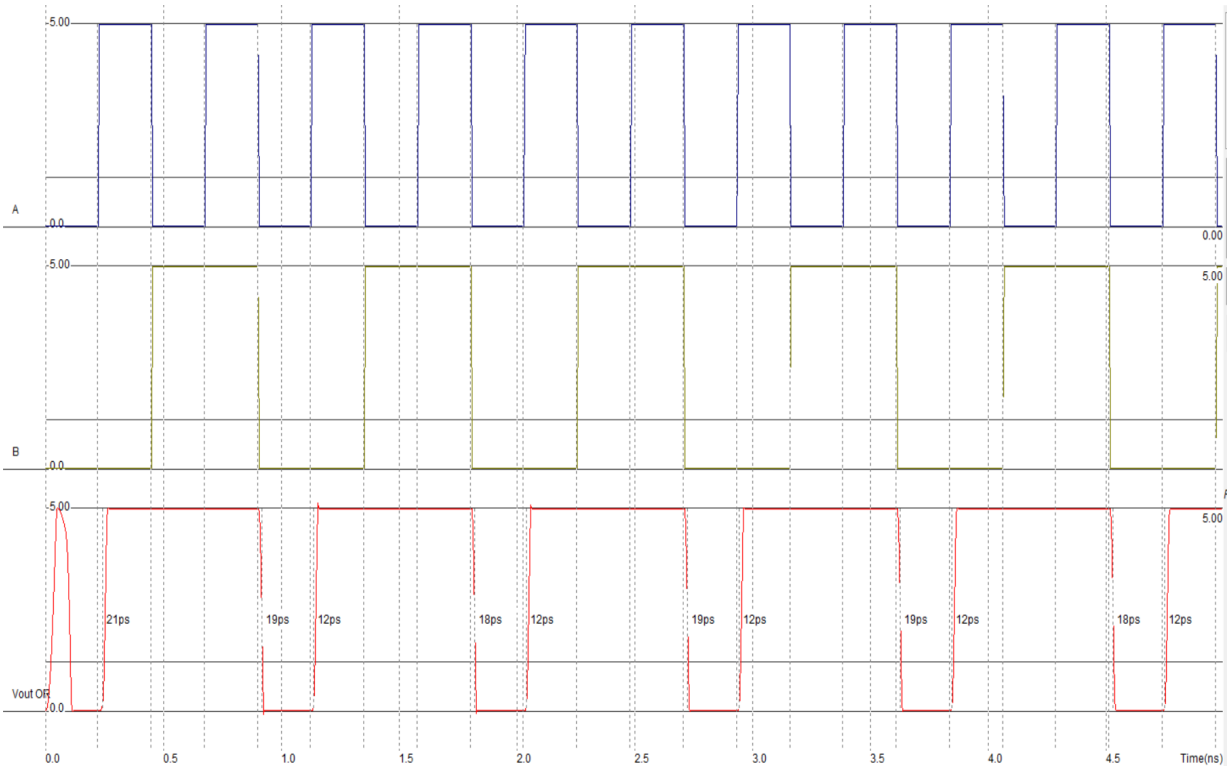


Figure 9: Output Waveshape of 2 Input OR-Gate using 1 Finger MOS

7.2 NOR-Gate & OR-Gate using 2 Finger MOS

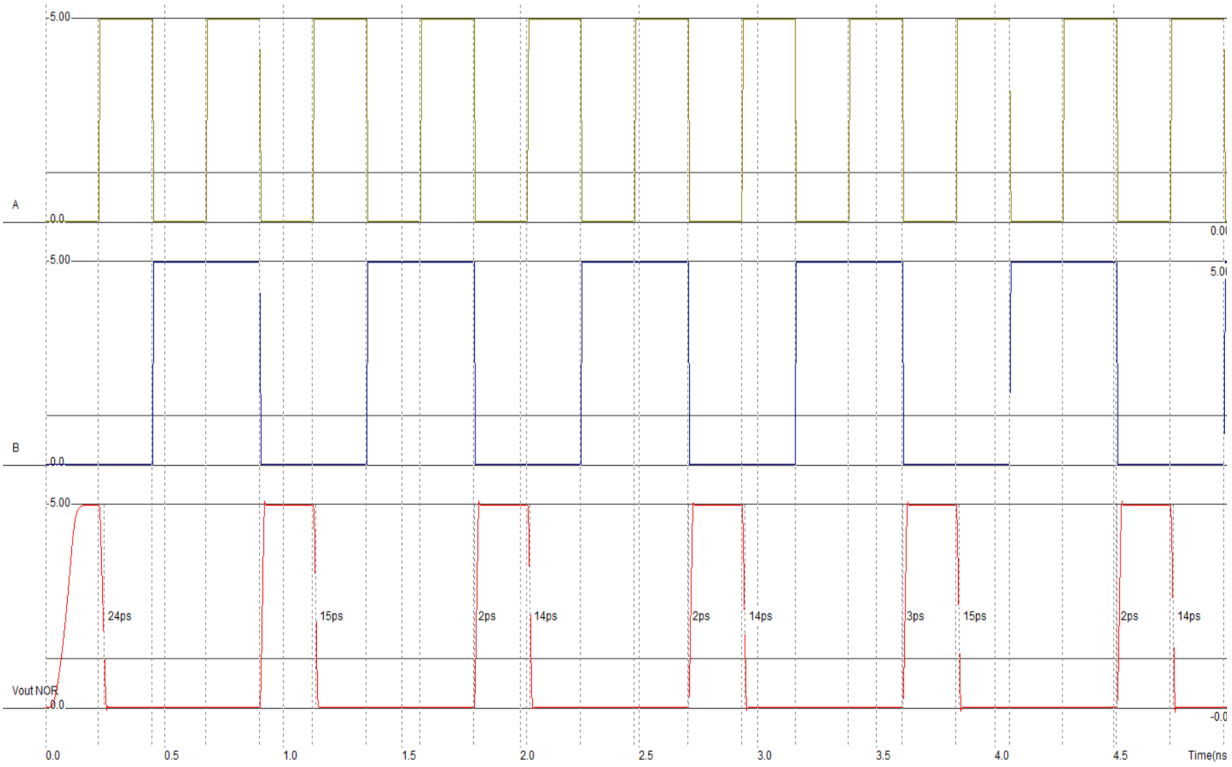


Figure 10: Output Waveshape of 2 Input NOR-Gate using 2 Finger MOS

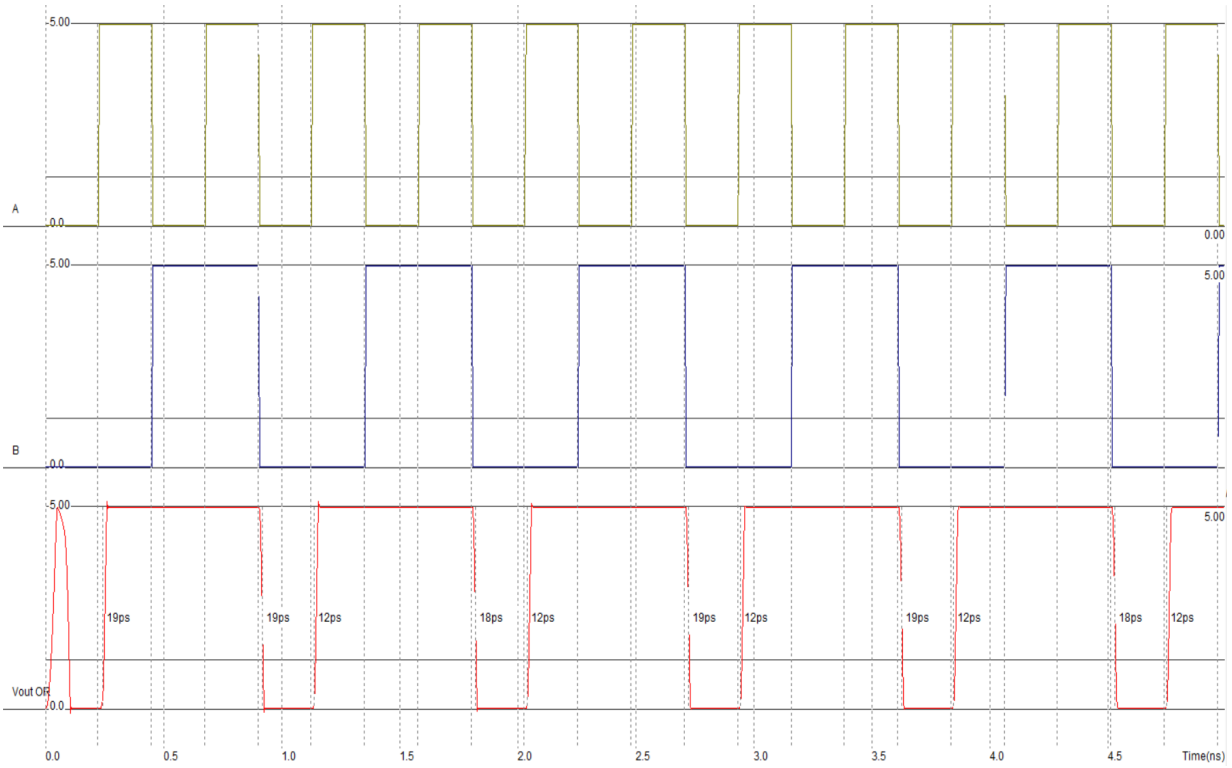


Figure 11: Output Waveshape of 2 Input OR-Gate using 2 Finger MOS

8 Discussion

The characteristics of 2-input CMOS NOR and OR gates were analyzed based on the input signals A and B and the corresponding output signal F. It was observed that the output of the OR gate was the complement of the output of the NOR gate for all input combinations, indicating that they are logical inverses of each other. The truth tables confirmed that when the OR gate output is logic high, the NOR gate output is logic low, and vice versa.

During testing, the NOR gate exhibited some initial voltage fluctuations during state transitions, which were not present in the OR gate. This behavior in the NOR gate could be attributed to the charge and discharge dynamics of its pMOS and nMOS transistors during switching. Despite these fluctuations, both gates adhered to the expected logical behavior as outlined in the truth table.