1 Experiment No. 9

2 Experiment Title

Design and Analyze of 2×1 and 4×1 MUX on MICROWIND 3.0.

3 Objective

The main objectives of this report are:

- To understand the working principle of a transmission gate.
- To design and simulate 2×1 , 4×1 MUX on MICROWIND 3.0.

4 Theory

The circuit shown is a **transmission gate**, which consists of a pMOS and an nMOS transistor connected in parallel. It is controlled by complementary signals S and $\overline{S}$.

Working Principle

1. **Inputs and Outputs:**
   (a) **Input (**A**)**: Signal to be transmitted.
   (b) **Output (**Y**)**: Signal after passing through the transmission gate.
   (c) **Control Signals (**S **and** $\overline{S}$**)**:
   S is the control signal , $\overline{S}$ is the complement of S.

$\bar{S}$	S	Output (Y)
1	0	A
0	1	N\A

2. **Operation:**
   (a) When $S = 1$ and $\overline{S} = 0$:
      i. Both nMOS and pMOS are **ON**.
      ii. The input A is passed to the output Y with minimal resistance.
   (b) When $S = 0$ and $\overline{S} = 1$:
      i. Both nMOS and pMOS are **OFF**.
      ii. The input A is disconnected from the output Y.

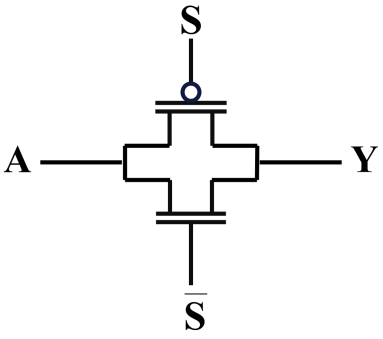

Figure 1: Transmission Gate

4.1 2x1 Multiplexer

A multiplexer is a combinational circuit that selects one of many input signals and forwards the selected input to a single output line. A 2x1 multiplexer has two input lines (A and B), one select line (S), and one output line (Y).

4.1.1 Working Principle

The output of the 2x1 multiplexer is given by the Boolean equation:

$$Y = \overline{S} \cdot A + S \cdot B$$

A 2x1 multiplexer selects one of two input signals (A or B) based on a control signal (S) and outputs the selected input to Y. The working process is as follows:

$\bar{S}$	S	Selected Input
1	0	A
0	1	B

Below is the simplified transistor-level implementation of a 2x1 multiplexer:

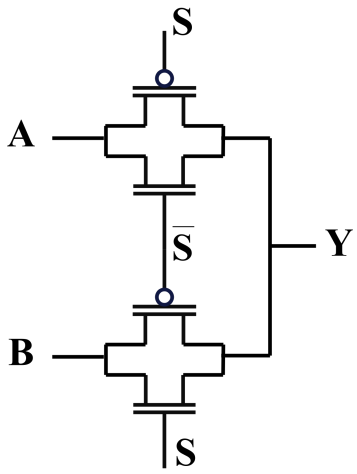

Figure 2: 2×1 Multiplexer Design using Transmission Gate

When S = 0:

- The input A is selected, and its value is passed to the output Y.
- This happens because the top pMOS transistor (controlled by S) turns **ON**, allowing A to pass to the output.

When S = 1:

- The input B is selected, and its value is passed to the output Y.
- In this case, the bottom pMOS transistor (controlled by S) turns **ON**, enabling B to pass to the output.

This multiplexer uses complementary logic to ensure that only one path is active at a time.

4.2 4x1 Multiplexer

A 4x1 multiplexer is a combinational circuit that selects one of four input signals (A, B, C, or D) based on two control signals (S_1 and S_0) and outputs the selected input to Y. This implementation uses transmission gates for efficient signal selection.
The selection process depends on the control signals as shown in the truth table below:

S_0	S_1	Selected Input
0	0	A
0	1	C
1	0	B
1	1	D

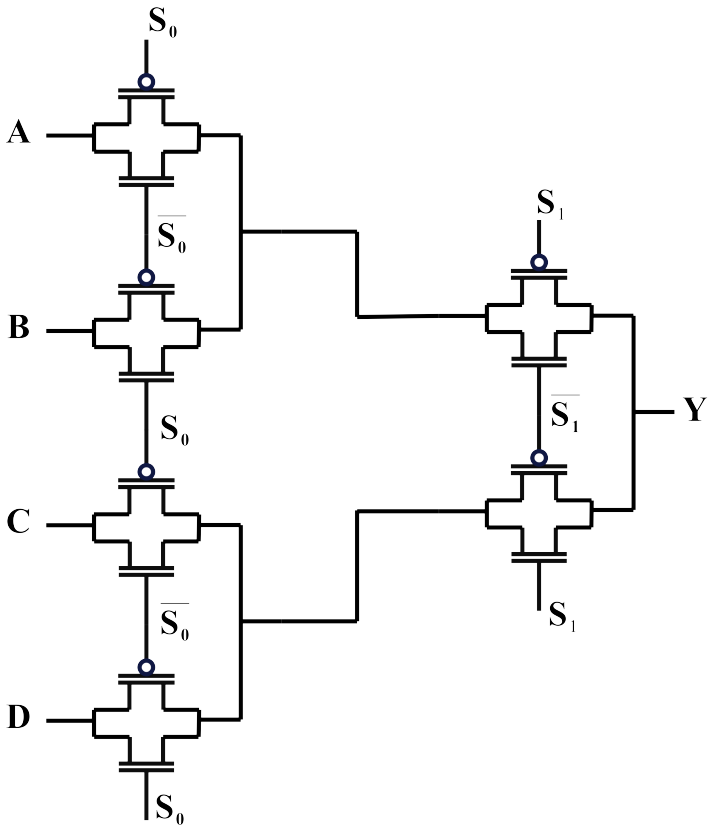

Figure 3: 4×1 Multiplexer Design using Transmission Gate

Working of 4x1 Multiplexer using Transmission Gates

- **When** $S_1 = 0$ **and** $S_0 = 0$**:** The transmission gate connected to input A is activated, allowing A to pass to the output Y.
- **When** $S_0 = 0$ **and** $S_1 = 1$**:** The transmission gate connected to input C is activated, allowing C to pass to the output Y.
- **When** $S_0 = 1$ **and** $S_1 = 0$**:** The transmission gate connected to input B is activated, allowing B to pass to the output Y.
- **When** $S_0 = 1$ **and** $S_1 = 1$**:** The transmission gate connected to input D is activated, allowing D to pass to the output Y.

5 Schematic Layout

5.1 2×1 Multiplexer

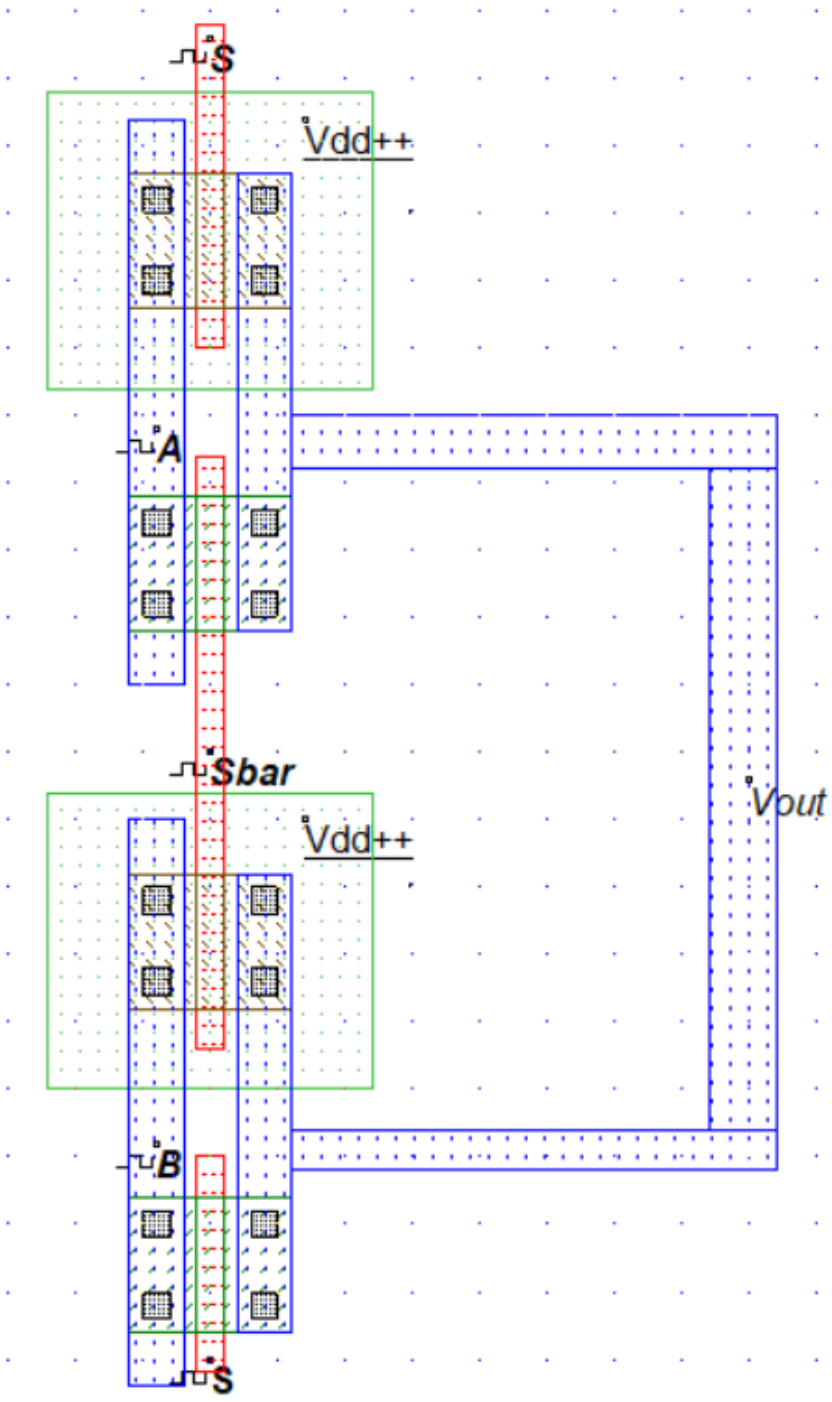

Figure 4: 2×1 Multiplexer Design

5.2 4×1 Multiplexer

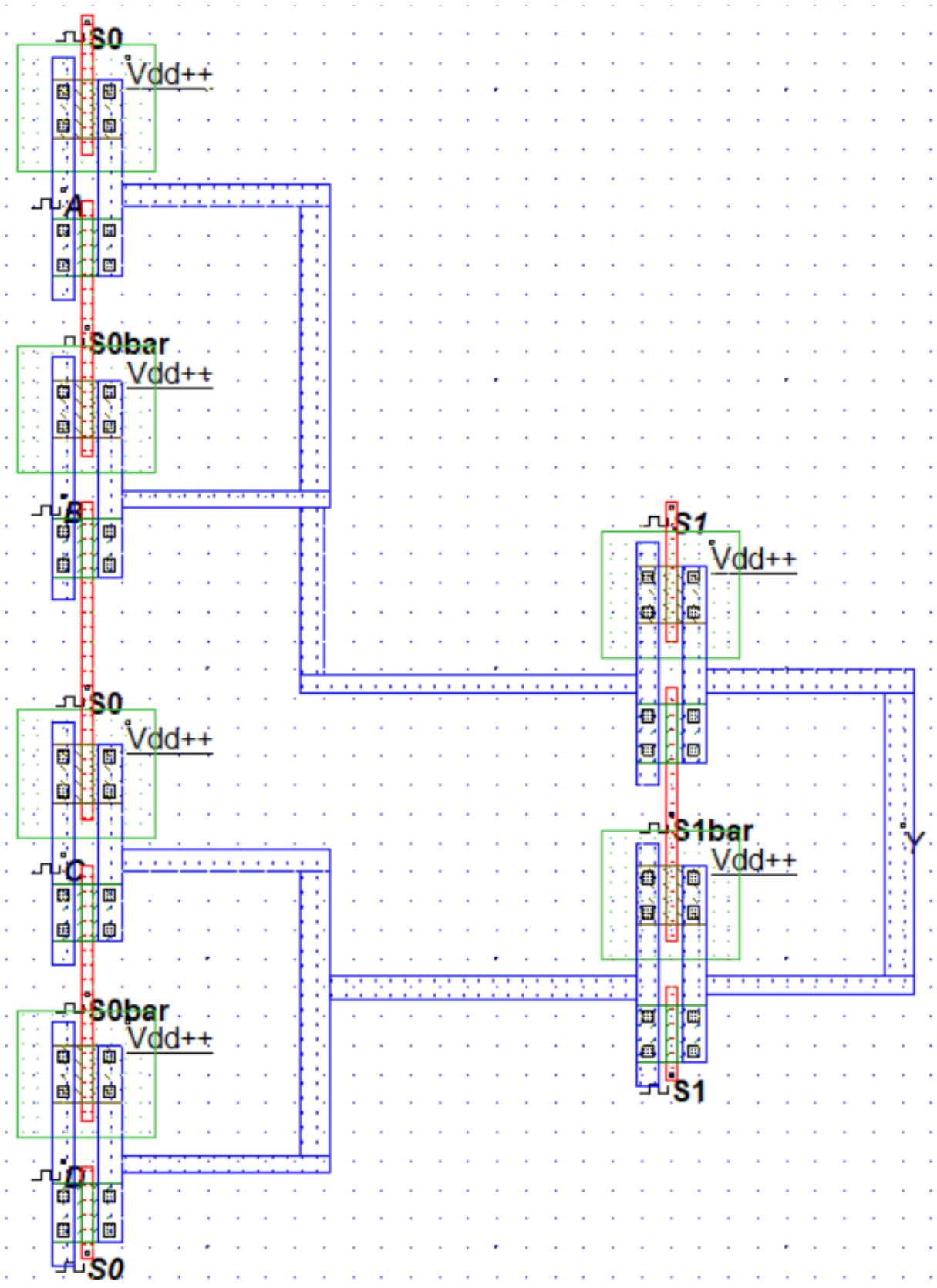

Figure 5: 4×1 Multiplexer Design

5.3 4×1 Multiplexer using nMOS Pass-Transistors

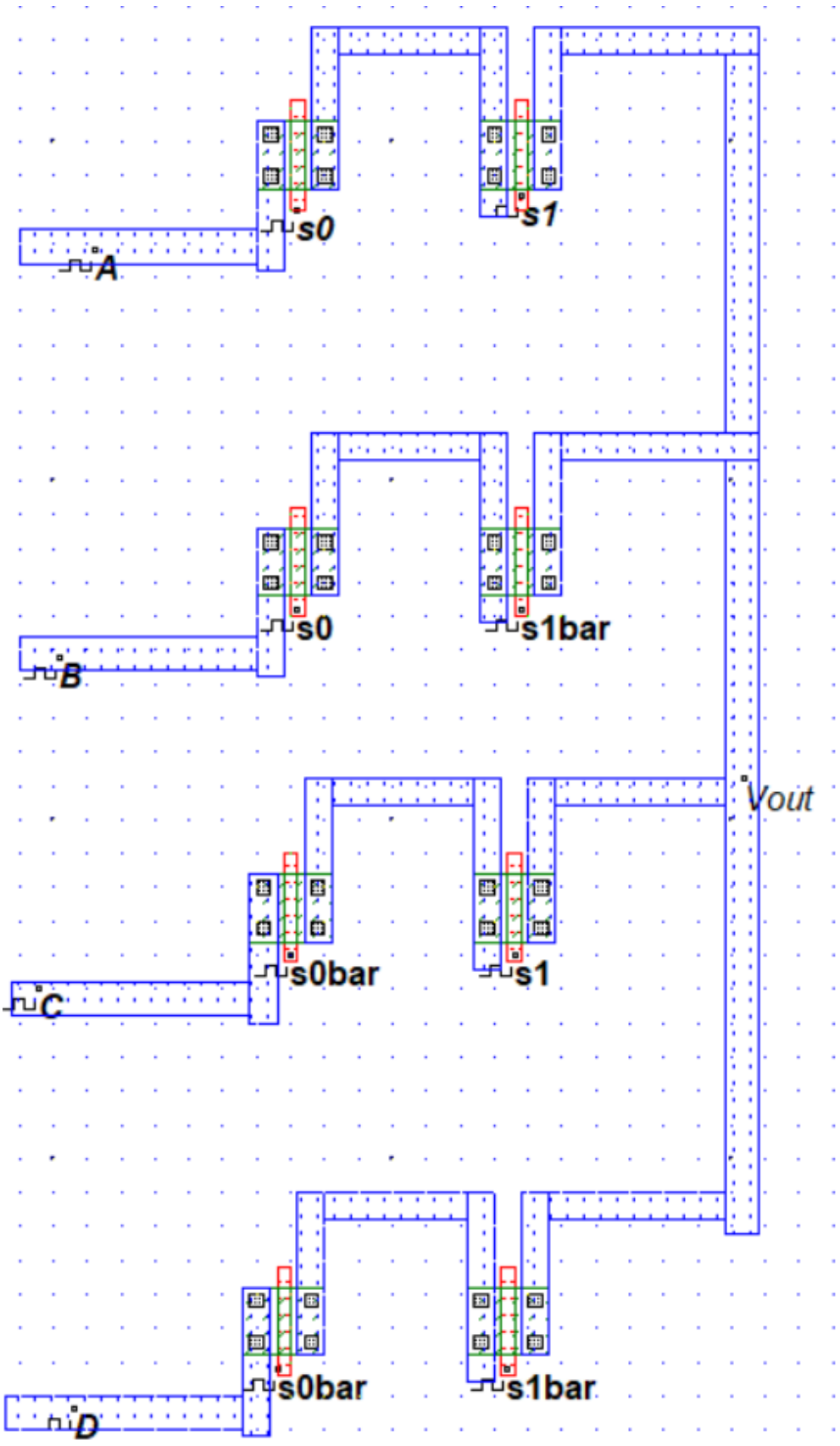

Figure 6: 4×1 Multiplexer Design using nMOS Pass-Transistors

6 Specification

Table 1: MOSFET Dimensions for nMOS and pMOS Transistors

MOS	**Width** (μm)	**Length** (μm)	**Width** (λ)	**Length** (λ)
nMOS	0.600	0.120	10	2
pMOS	0.600	0.120	10	2

6.1 2×1 Multiplexer

Table 2: Parameters of Input Clock Signals for A,B S0 & S0bar

Parameter	**Value**	**Unit**
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.225	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.225	ns
Fall Time (tf)	0.002	ns

(a) Input clock signal of A

Parameter	**Value**	**Unit**
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.452	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.452	ns
Fall Time (tf)	0.002	ns

(b) Input clock signal of B

Parameter	**Value**	**Unit**
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.450	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.450	ns
Fall Time (tf)	0.002	ns

(c) Input clock signal of S0

Parameter	**Value**	**Unit**
High Level (V)	0.00	V
Low Level (V)	5.00	V
Time Low (tl)	0.450	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.450	ns
Fall Time (tf)	0.002	ns

(d) Input clock signal of S0bar

Table 3: Parameters for Vdd+ and Vss-

Parameter	**Value**	**Unit**
Vdd+	5.00	V
Vss-	0.00	V

6.2 4×1 Multiplexer

Table 4: Parameters of Input Clock Signals for A,B,C,D S0, S0bar, S1 & S1bar

Parameter	Value	Unit
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.225	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.225	ns
Fall Time (tf)	0.002	ns

(a) Input clock signals for A & B

Parameter	Value	Unit
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.450	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.450	ns
Fall Time (tf)	0.002	ns

(b) Input clock signals for C & D

Parameter	Value	Unit
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.450	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.450	ns
Fall Time (tf)	0.002	ns

(c) Input clock signal of S0

Parameter	Value	Unit
High Level (V)	0.00	V
Low Level (V)	5.00	V
Time Low (tl)	0.450	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.450	ns
Fall Time (tf)	0.002	ns

(d) Input clock signal of S0bar

Parameter	Value	Unit
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.900	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.900	ns
Fall Time (tf)	0.002	ns

(e) Input clock signal of S1

Parameter	Value	Unit
High Level (V)	0.00	V
Low Level (V)	5.00	V
Time Low (tl)	0.900	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.900	ns
Fall Time (tf)	0.002	ns

(f) Input clock signal of S1bar

Table 5: Parameters for Vdd+ and Vss-

Parameter	Value	Unit
Vdd+	5.00	V
Vss-	0.00	V

6.3 4×1 Multiplexer using nMOS pass transistors

Table 6: Parameters of Input Clock Signals for A,B,C,D S0, S0bar, S1 & S1bar

Parameter	Value	Unit
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	1	ns
Rise Time (tr)	0.001	ns
Time High (th)	1	ns
Fall Time (tf)	0.001	ns

(a) Input clock signals for A

Parameter	Value	Unit
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.500	ns
Rise Time (tr)	0.001	ns
Time High (th)	0.500	ns
Fall Time (tf)	0.001	ns

(b) Input clock signals for B

Parameter	Value	Unit
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.255	ns
Rise Time (tr)	0.001	ns
Time High (th)	0.255	ns
Fall Time (tf)	0.001	ns

(c) Input clock signals for C

Parameter	Value	Unit
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.062	ns
Rise Time (tr)	0.001	ns
Time High (th)	0.062	ns
Fall Time (tf)	0.001	ns

(d) Input clock signals for D

Parameter	Value	Unit
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	1	ns
Rise Time (tr)	0.001	ns
Time High (th)	1	ns
Fall Time (tf)	0.001	ns

(e) Input clock signal of S0

Parameter	Value	Unit
High Level (V)	0.00	V
Low Level (V)	5.00	V
Time Low (tl)	1	ns
Rise Time (tr)	0.001	ns
Time High (th)	1	ns
Fall Time (tf)	0.001	ns

(f) Input clock signal of S0bar

Parameter	Value	Unit
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	2	ns
Rise Time (tr)	0.001	ns
Time High (th)	2	ns
Fall Time (tf)	0.001	ns

(g) Input clock signal of S1

Parameter	Value	Unit
High Level (V)	0.00	V
Low Level (V)	5.00	V
Time Low (tl)	2	ns
Rise Time (tr)	0.001	ns
Time High (th)	2	ns
Fall Time (tf)	0.001	ns

(h) Input clock signal of S1bar

Table 7: Parameters for Vdd+ and Vss-

Parameter	Value	Unit
Vdd+	5.00	V
Vss-	0.00	V

7 Output Waveshape

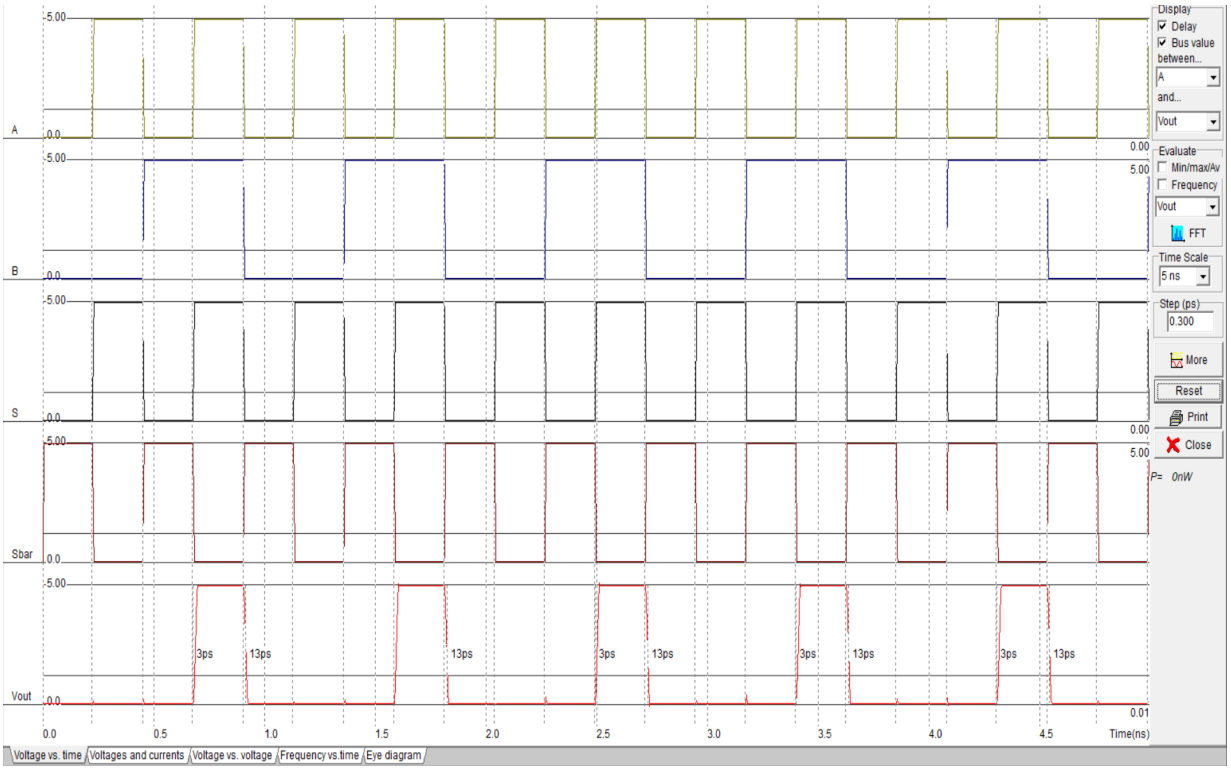

Figure 7: Output waveshape of 2×1 Multiplexer

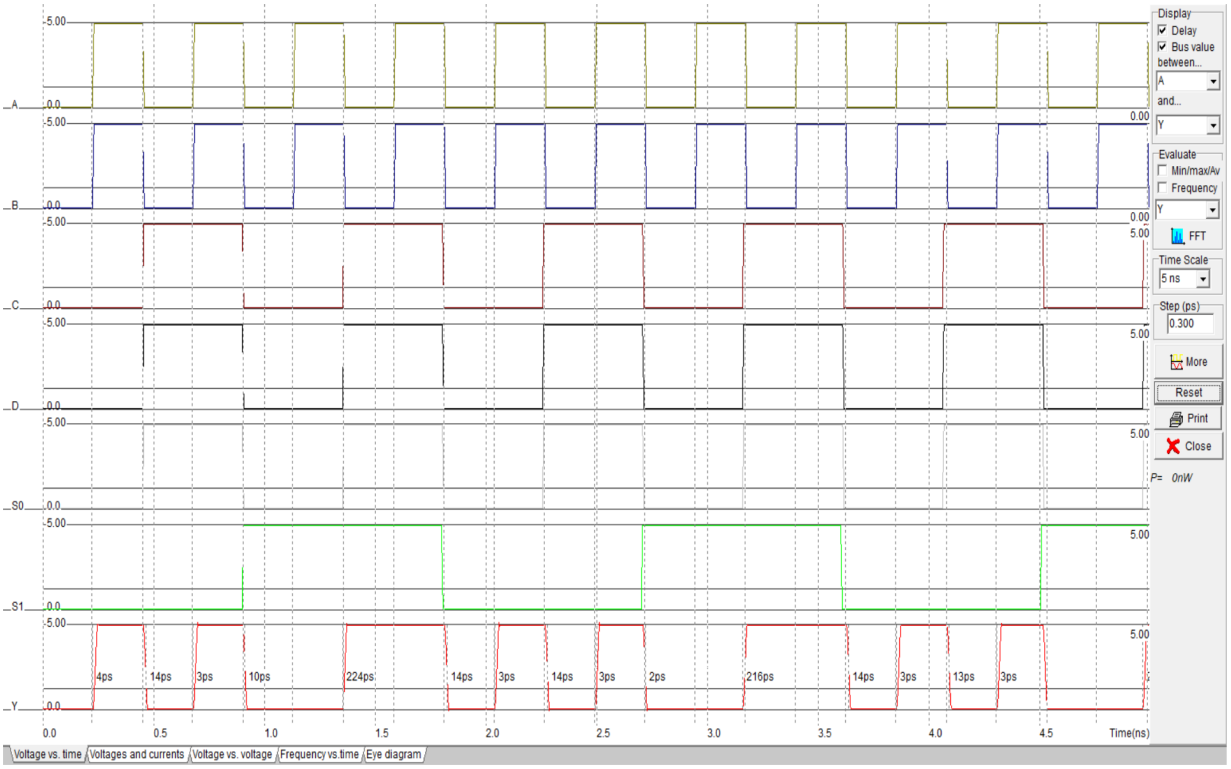

Figure 8: Output waveshape of 4×1 Multiplexer

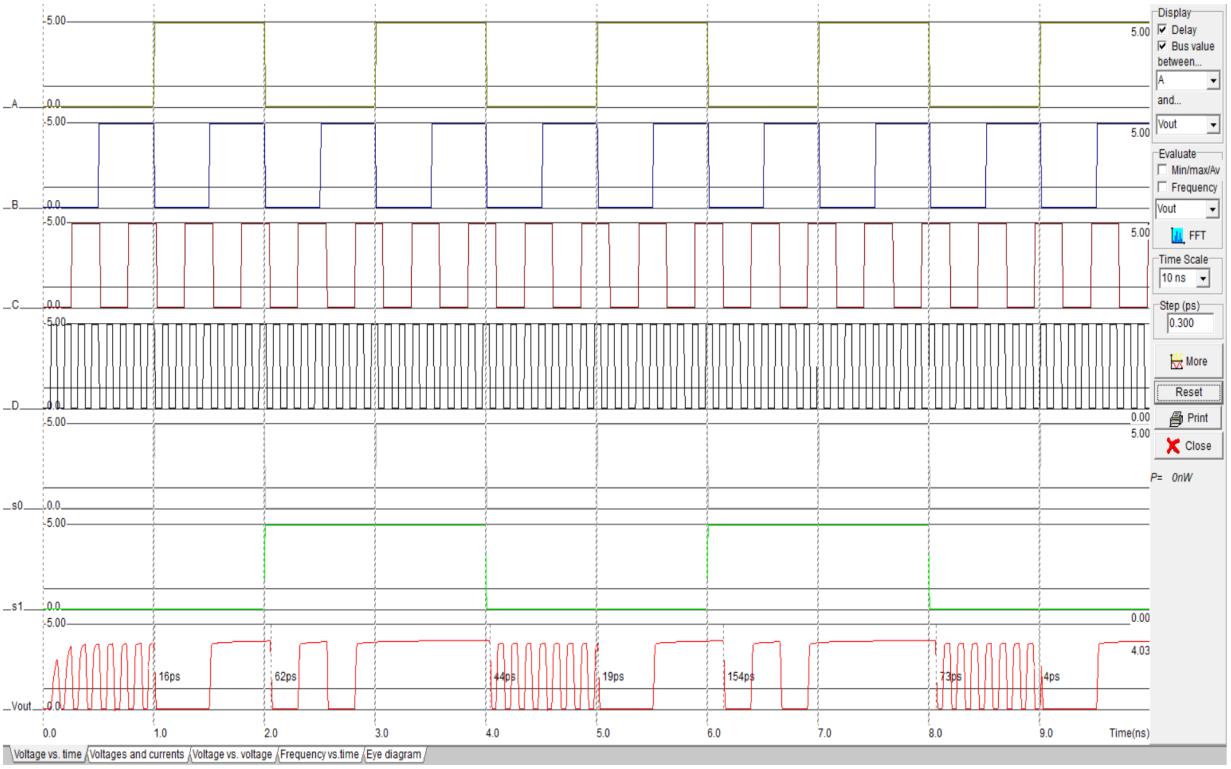

Figure 9: Output waveshape of 4×1 Multiplexer using nMOS Pass-Transistors

8 Discussion

In this experiment, 2x1 and 4x1 multiplexers were designed using transmission gates, and the working principle of the transmission gate was analyzed. The circuits were tested under various input conditions to verify their behavior. The input signals were applied to the gates, and the corresponding output responses were observed.

It was noted that for the 2x1 multiplexer, when the control signal S_0 was high, the input signal A was observed at the output. Conversely, when S_0 was low, the input signal B appeared at the output, ensuring the correct operation of the 2x1 multiplexer.

On the other hand, for the 4x1 multiplexer, two control signals, S_0 and S_1, were used. For better understanding, the frequencies of input signals A and B were set to the same value, and the frequencies of C and D were also set to the same value but different from A and B. Additionally, the frequencies of S_0 and S_1 were taken as double relative to each other to cover all four input conditions. It was clearly observed that the output switched between A, B, C, and D for different combinations of S_0 and S_1, confirming the correct operation of the 4x1 multiplexer.

The experiment demonstrated the effectiveness of using complementary signals (S and $\overline{S}$) to control the transmission gate. The results obtained were consistent with theoretical expectations, validating the design and functionality of the circuit.

Overall, the practical implementation of the transmission gate and multiplexers was successfully carried out, and their characteristics were thoroughly investigated.