1 Experiment No. 5

2 Experiment Title

Design and analyze a 2 input NAND & NOR gate using nMOS inverter with Enhancement & Resistive Load using MICROWIND 3.0

3 Objective

The main objectives of this report are:

- To design and analyze 2-input NAND and NOR gates using nMOS inverters with resistive and enhancement mode loads.
- To evaluate the performance of resistive and enhancement mode loads in terms of output voltage levels characteristics.
- To simulate and verify the logical behavior of NAND and NOR gates using MICROWIND 3.0 software.

4 Theory

4.1 nMOS Inverter with Enhancement Mode (Pull-Up) Load

An nMOS inverter with an enhancement mode (pull-up) load consists of two nMOS transistors: the driving transistor (T_1) and the load transistor (T_2). The load transistor T_2 is connected between the power supply V_{DD} and the output node, while T_1 is connected between the output and ground. The gate of T_2 is connected to V_{DD} to keep it ON when both inputs are low.

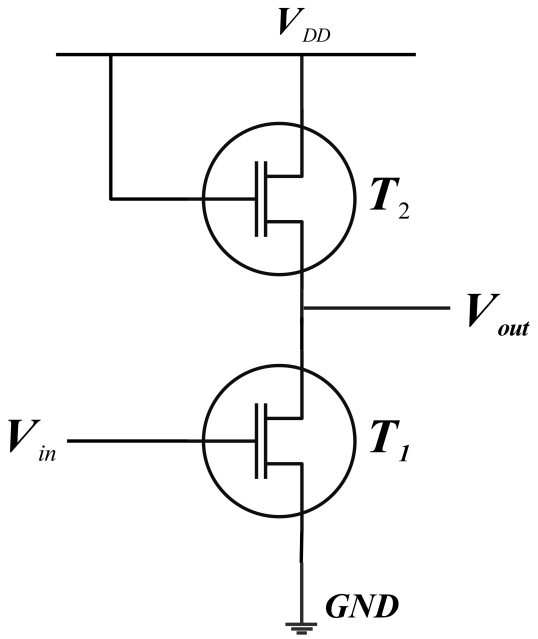


Figure 1

- When the input V_{in} is low (logic '0'), T_1 is OFF, and T_2 pulls the output V_{out} high to V_{DD}.
- When V_{in} is high (logic '1'), T_1 turns ON, pulling V_{out} low to 0V.

4.2 nMOS Inverter with Resistive Load

An nMOS inverter with a resistive load consists of an nMOS transistor (T_1) and a resistor (R_L). The resistor is connected between the power supply V_{DD} and the output node, while T_1 is connected between the output and ground. The operation can be summarized as follows:

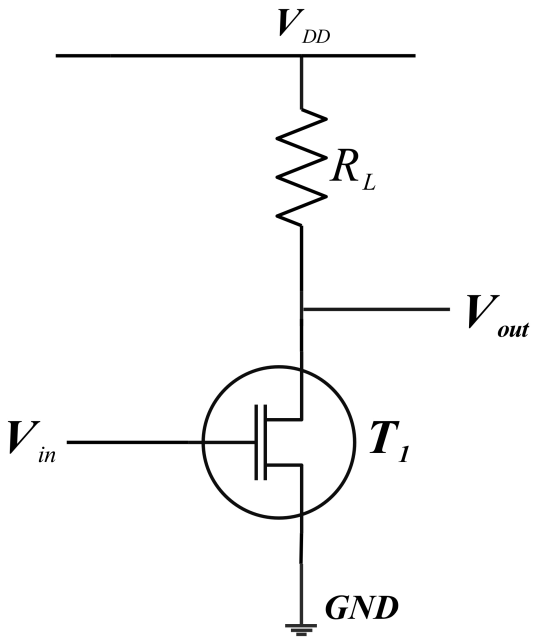


Figure 2

- When the input V_{in} is low (logic '0'), M_1 is OFF, and the output V_{out} is pulled high to V_{DD}.
- When V_{in} is high (logic '1'), M_1 turns ON, pulling V_{out} low to 0V.

The output voltage V_{out} is given by:

$$V_{out} = V_{DD} - I_D \cdot R$$

where: - I_D is the drain current through the nMOS transistor.

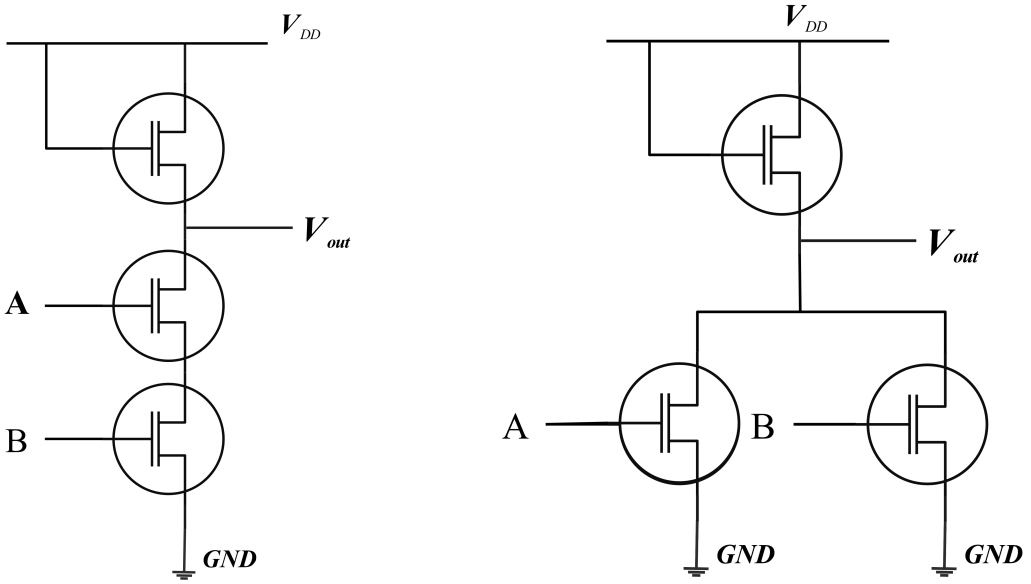
The resistive load leads to higher power dissipation, as there is a direct current path from V_{DD} to ground when M_1 is ON. Additionally, the switching speed is limited by the time constant:

$$\tau = R \cdot C_{out}$$

where: - C_{out} is the output capacitance.

4.3 Implemention of Gate Using nMOS Inverters

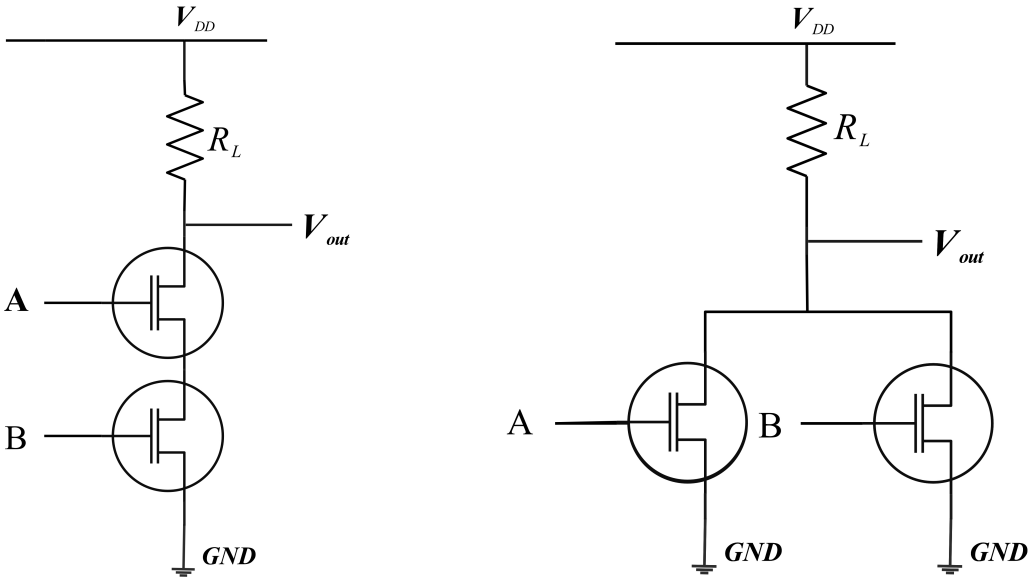
4.3.1 nMOS Inverter using Enhancement Load



(a) NAND-Gate (b) NOR-Gate

Figure 3: Circuit Diagram of NAND-Gate & NOR-Gate using nMOS Inverter with Enhancement Load

4.3.2 nMOS Inverter using Resistive Load



(a) NAND-Gate (b) NOR-Gate

Figure 4: Circuit Diagram of NAND-Gate & NOR-Gate using nMOS Inverter with Resistive Load

5 Schematic Layout

5.1 NAND-Gate using nMOS Inverter with Enhancement Load

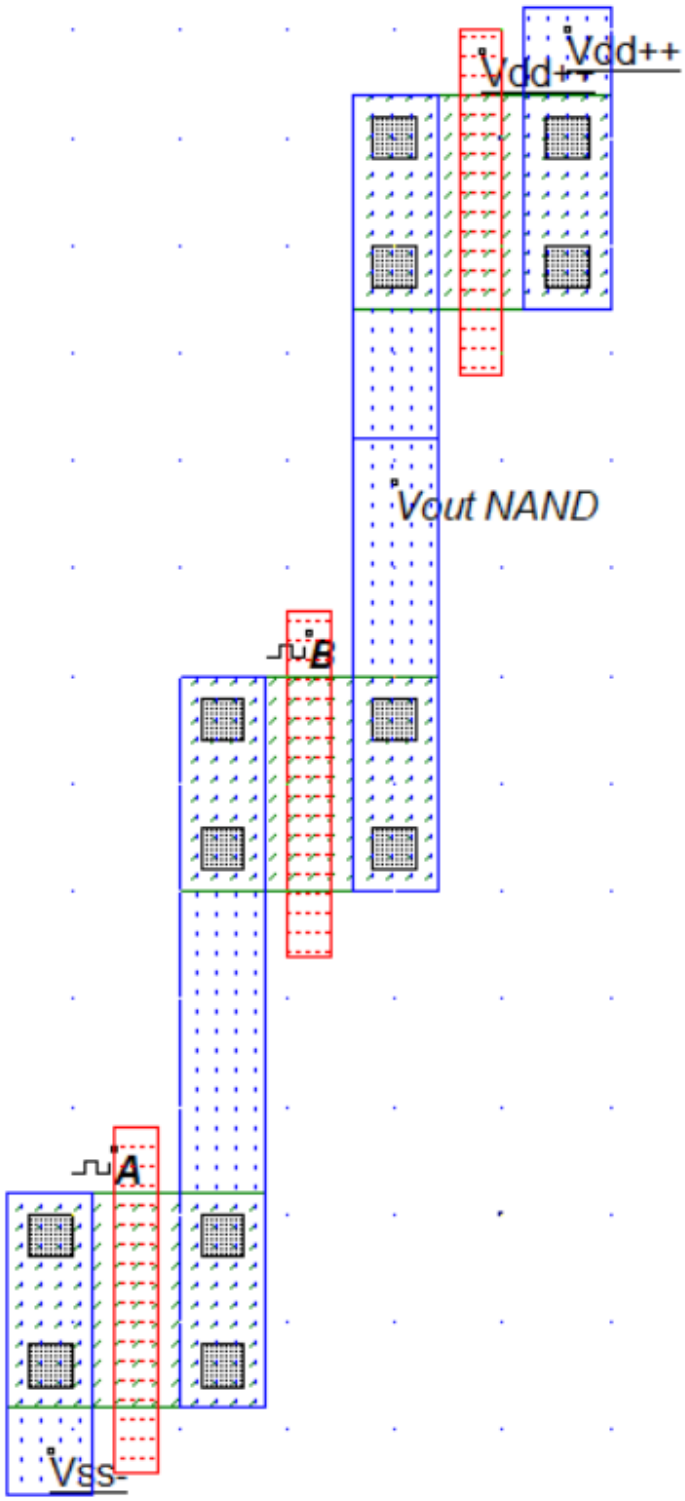


Figure 5: Design layout of NAND-Gate using nMOS Inverter with Enhancement Load

5.2 NOR-Gate using nMOS Inverter with Enhancement Load

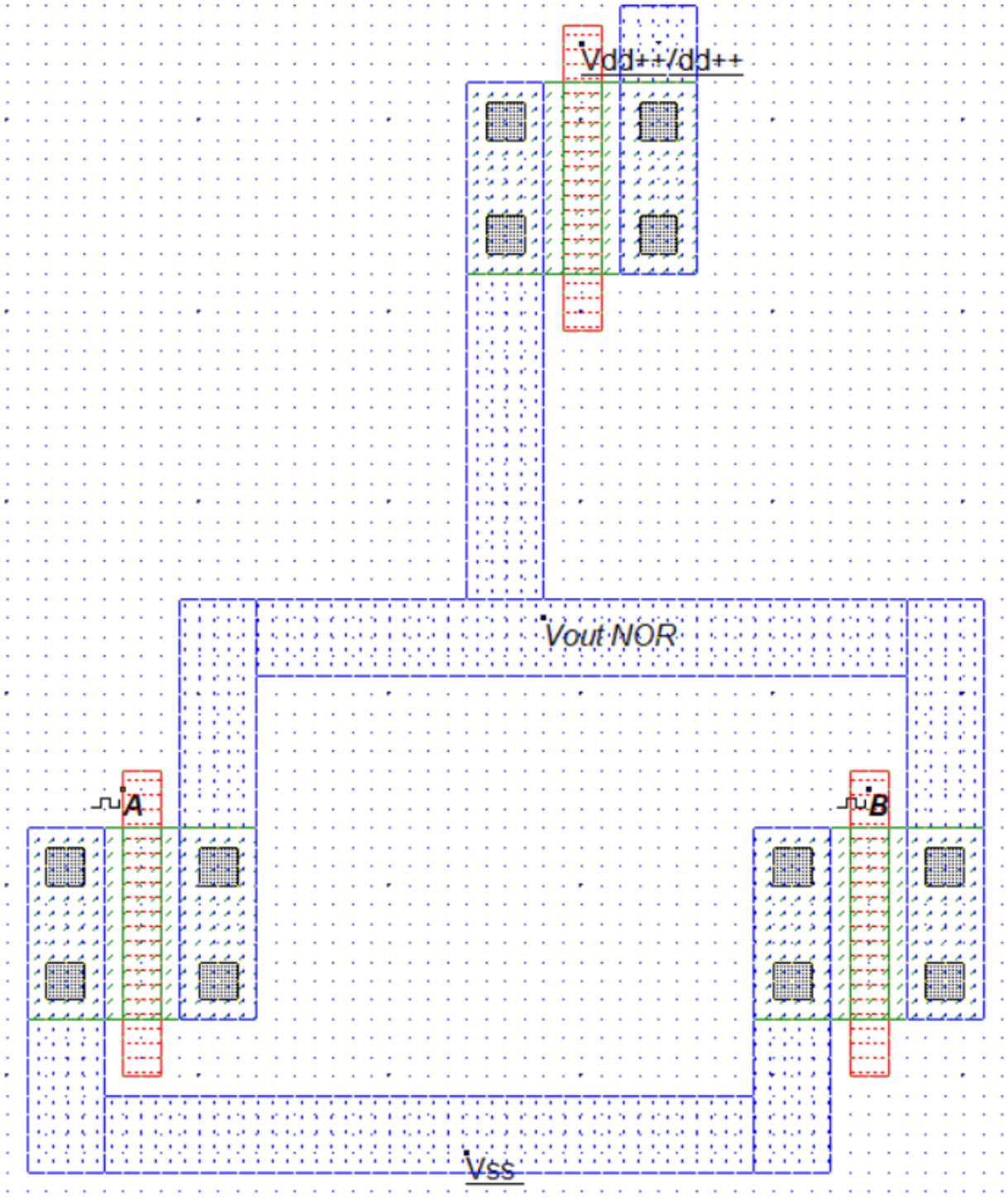
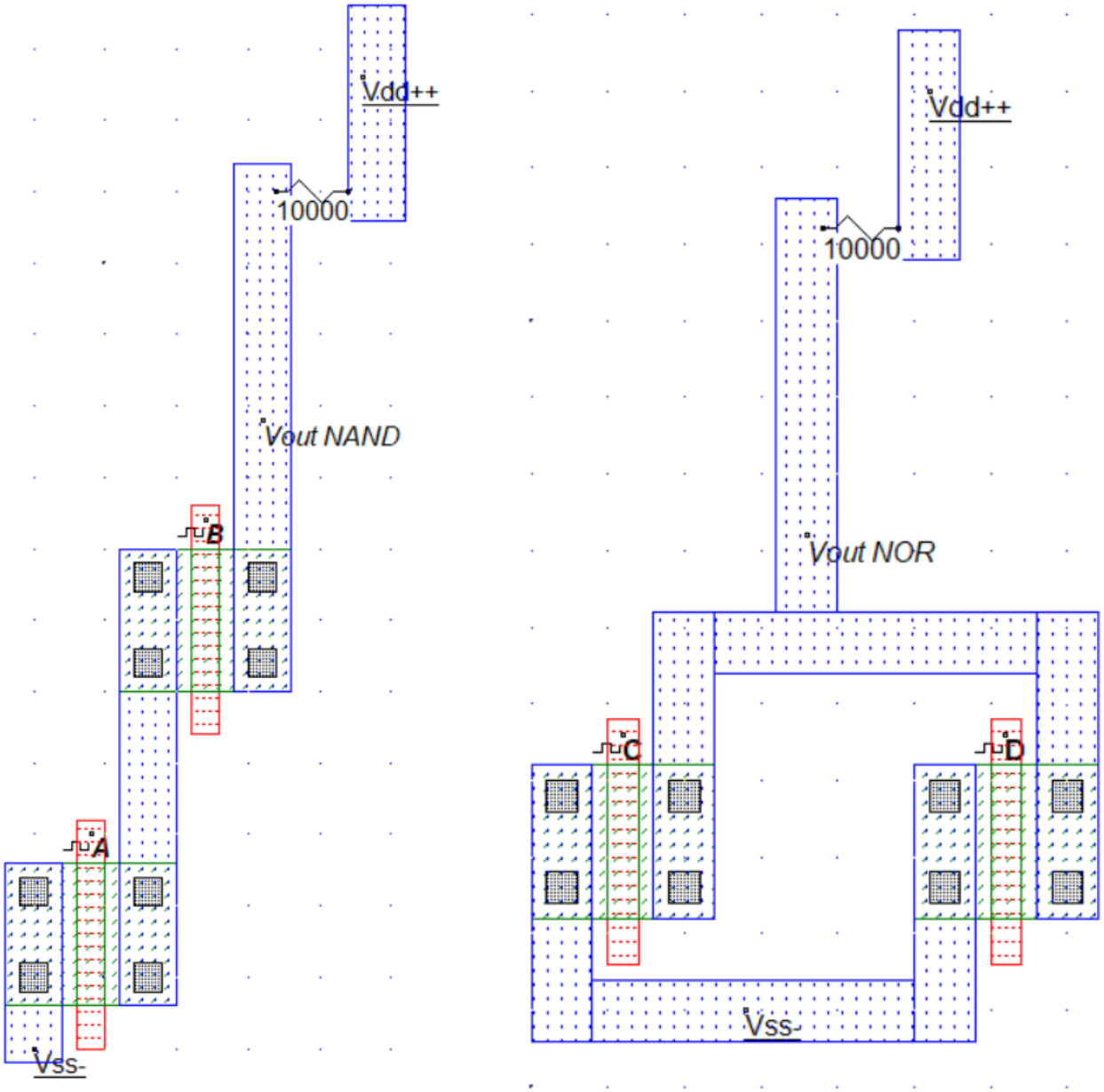


Figure 6: Design layout of NOR-Gate using nMOS Inverter with Enhancement Load

5.3 NAND-Gate & NOR-Gate using nMOS Inverter with Resistive Load



(a) NAND-Gate (b) NOR-Gate

Figure 7: Design layout of NAND-Gate & NOR-Gate using nMOS Inverter with Resistive Load

6 Specification

Table 1: MOSFET Dimensions for nMOS and pMOS Transistors

MOS	**Width** (μm)	**Length** (μm)	**Width** (λ)	**Length** (λ)
nMOS	0.600	0.120	10	2
pMOS	0.600	0.120	10	2

Table 2: Parameters of Input Clock Signal for 1 Finger NAND-Gate and AND-Gate

Parameter	**Value**	**Unit**
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.225	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.225	ns
Fall Time (tf)	0.002	ns

(a) Input clock signal of A

Parameter	**Value**	**Unit**
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.452	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.452	ns
Fall Time (tf)	0.002	ns

(b) Input clock signal of B

Table 3: Parameters of Input Clock Signal for 2 Finger NAND-Gate and AND-Gate

Parameter	**Value**	**Unit**
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.452	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.452	ns
Fall Time (tf)	0.002	ns

(a) Input clock signal of A

Parameter	**Value**	**Unit**
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.225	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.225	ns
Fall Time (tf)	0.002	ns

(b) Input clock signal of B

Table 4: Parameters for Vdd+, Vss- and Load Resistance

Parameter	**Value**	**Unit**
Vdd+	5.00	V
Vss-	0.00	V
Resistance	10000	Ω

7 Output Waveshape

7.1 nMOS Inverter with Enhancement Load

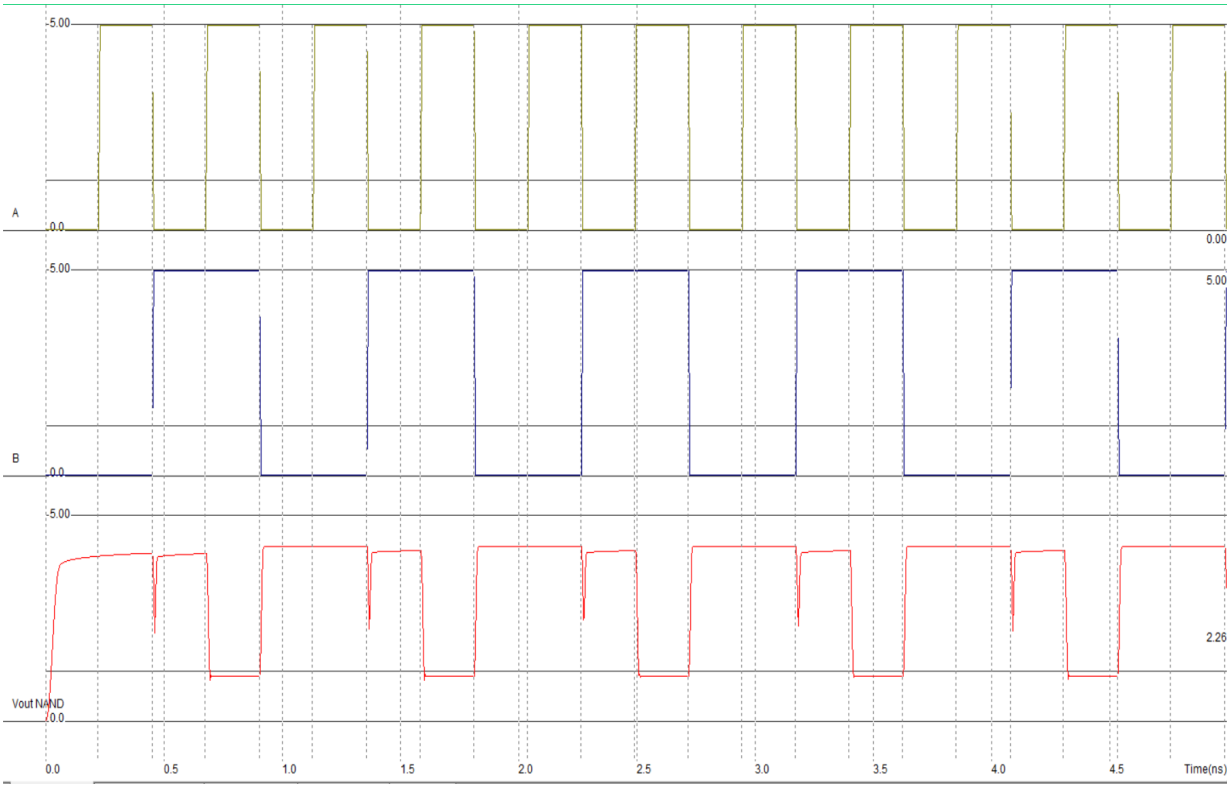


Figure 8: 2 Input NAND-Gate using nMOS Inverter with Enhancement Load

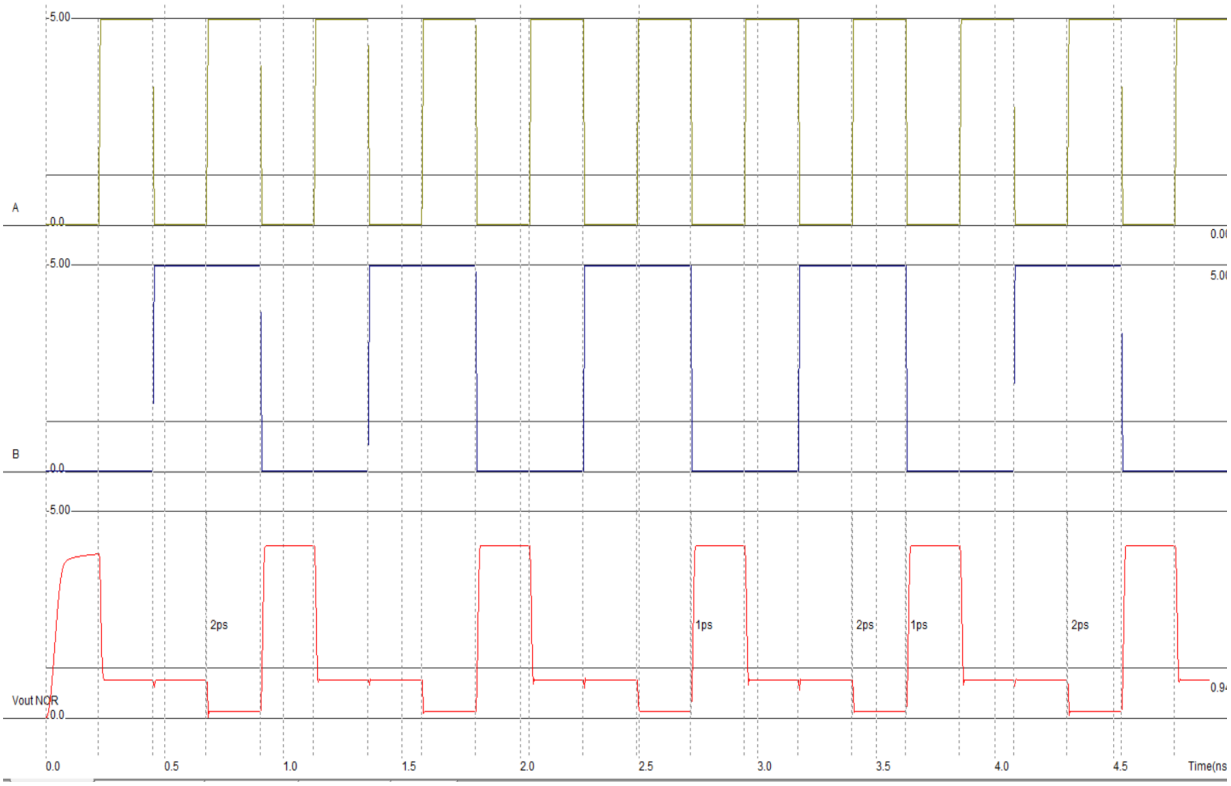


Figure 9: 2 Input NOR-Gate using nMOS Inverter with Enhancement Load

7.2 nMOS Inverter with Resistive Load

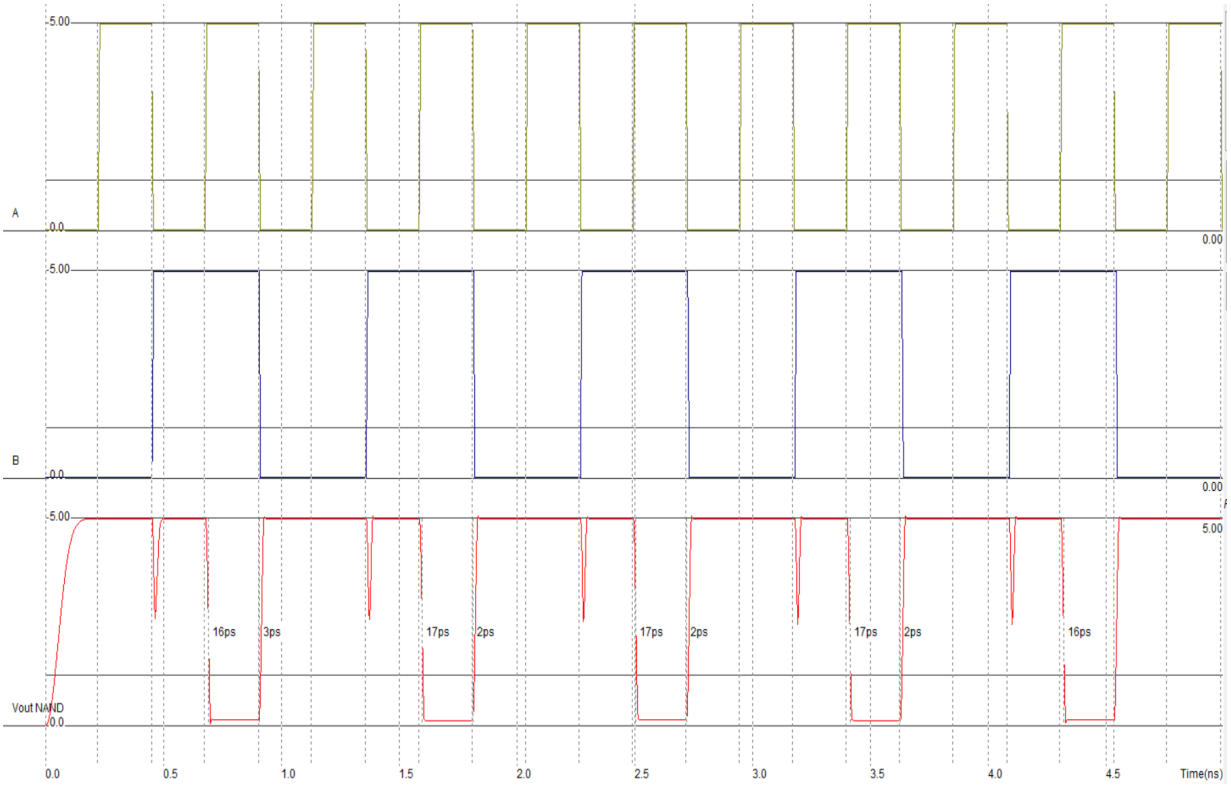


Figure 10: 2 Input NAND-Gate using nMOS Inverter with Resistive Load

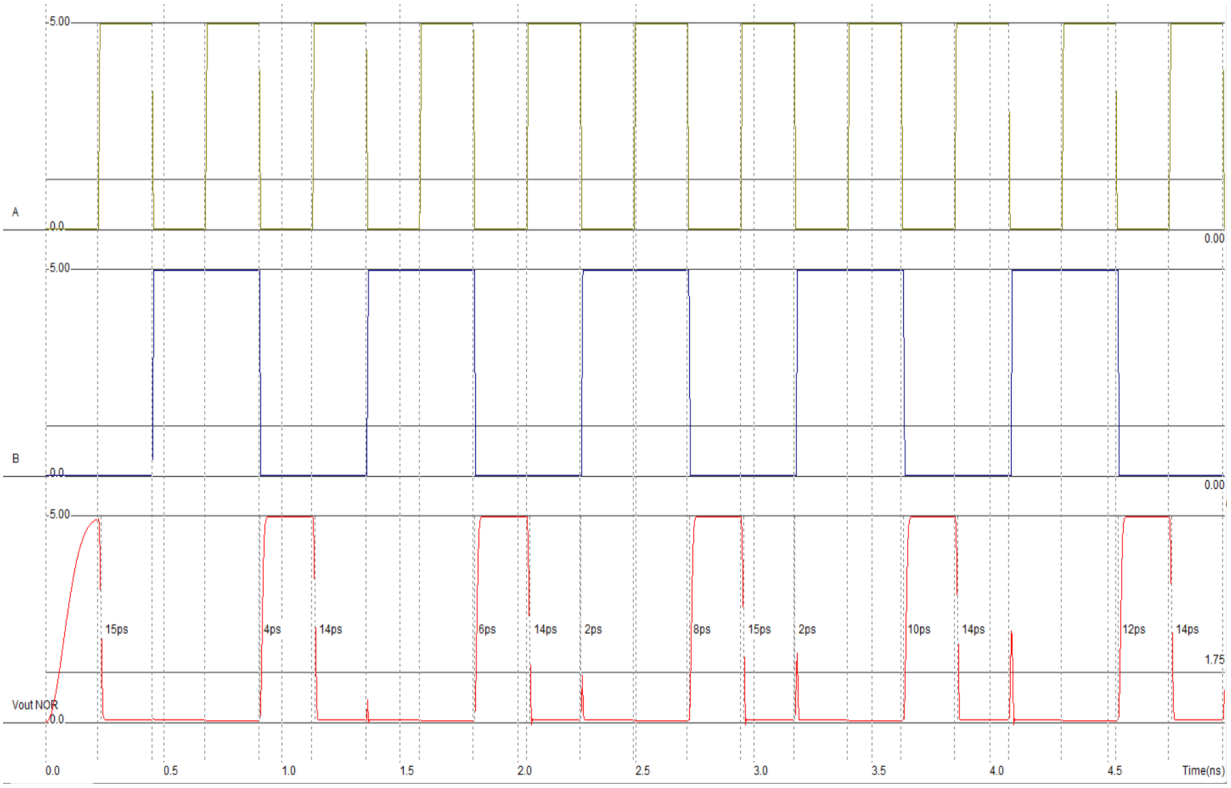


Figure 11: 2 Input NOR-Gate using nMOS Inverter with Resistive Load

8 Discussion

The characteristics of 2-input NAND and NOR gates were analyzed using nMOS inverters with resistive and enhancement mode loads. It was observed that for the resistive load configuration, the output voltage improved with an increase in load resistance. This is because a higher load resistance reduces the voltage drop across the resistor, resulting in a higher V_{out}. As the output voltage V_{out} is given by: $V_{out} = V_{DD} - I_D \cdot R$

In the enhancement mode load configuration, the output voltage was not perfectly zero. This was due to the finite on-resistance (R_{on}) of the load transistor, which caused a small voltage drop across the nMOS transistor T_1. On the other hand, the output voltage was perfectly high, as the load transistor (T_2) could fully pull V_{out} to V_{DD} without any voltage drop. The simulation results confirmed that both configurations followed the expected logical behavior for the NAND and NOR gates as per their truth tables.