1 Experiment No. 8

2 Experiment Title

Design and analyze 4 Input logic gate ensuring proper DRC on MICROWIND 3.0

3 Objective

The main objectives of this report are:

- To design and analyze 4 Input logic gate using MICROWIND 3.0.
- To ensure proper compliance with Design Rule Check (DRC) requirements during the design process.

4 Theory

4.1 nMOS Inverter with Enhancement Mode (Pull-Up) Load

An nMOS inverter with an enhancement mode (pull-up) load consists of two nMOS transistors: the driving transistor (T_1) and the load transistor (T_2). The load transistor T_2 is connected between the power supply V_{DD} and the output node, while T_1 is connected between the output and ground. The gate of T_2 is connected to V_{DD} to keep it ON when both inputs are low.

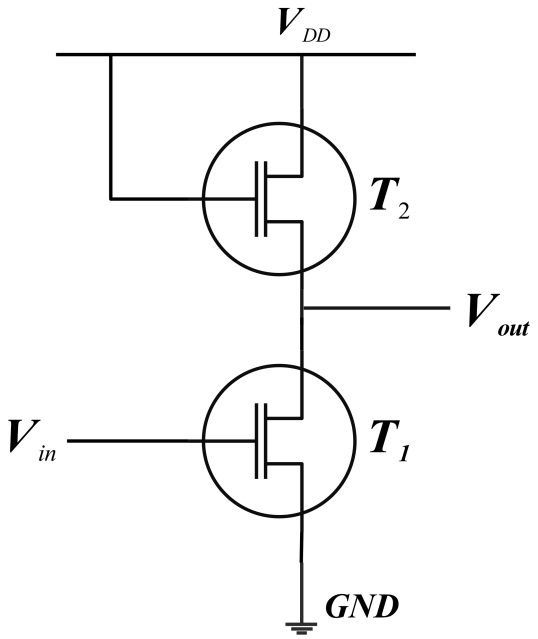

Figure 1: nMOS Inverter with Enhancement Mode (Pull-Up) Load

- When the input V_{in} is low (logic '0'), T_1 is OFF, and T_2 pulls the output V_{out} high to V_{DD}.
- When V_{in} is high (logic '1'), T_1 turns ON, pulling V_{out} low to 0V.

4.2 Proposed Boolean Expression:

$$Y = \overline{(A + A \cdot B + A \cdot B \cdot C \cdot D)}$$

4.3 Circuit Diagram

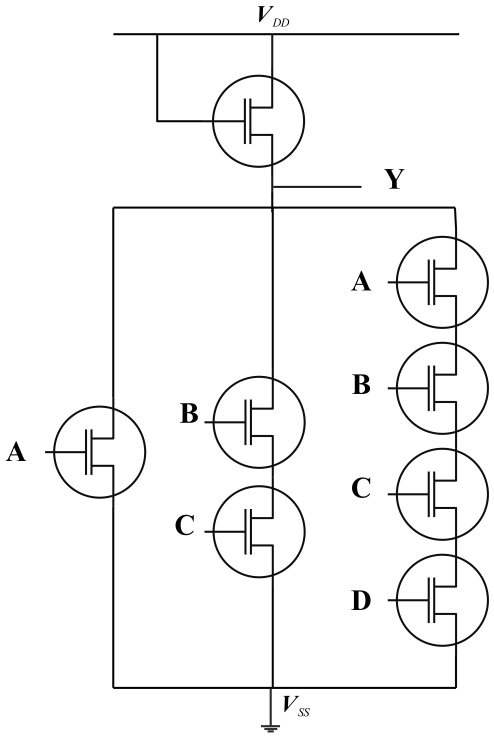

Figure 2: Y = $\overline{A + A.B + A.B.C.D}$

4.4 Truth Table

A	B	C	D	Intermediate $A + A \cdot B + A \cdot B \cdot C \cdot D$	Y $\overline{(A + A \cdot B + A \cdot B \cdot C \cdot D)}$
0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	0	1
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	0
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	1	0

5 Schematic Layout

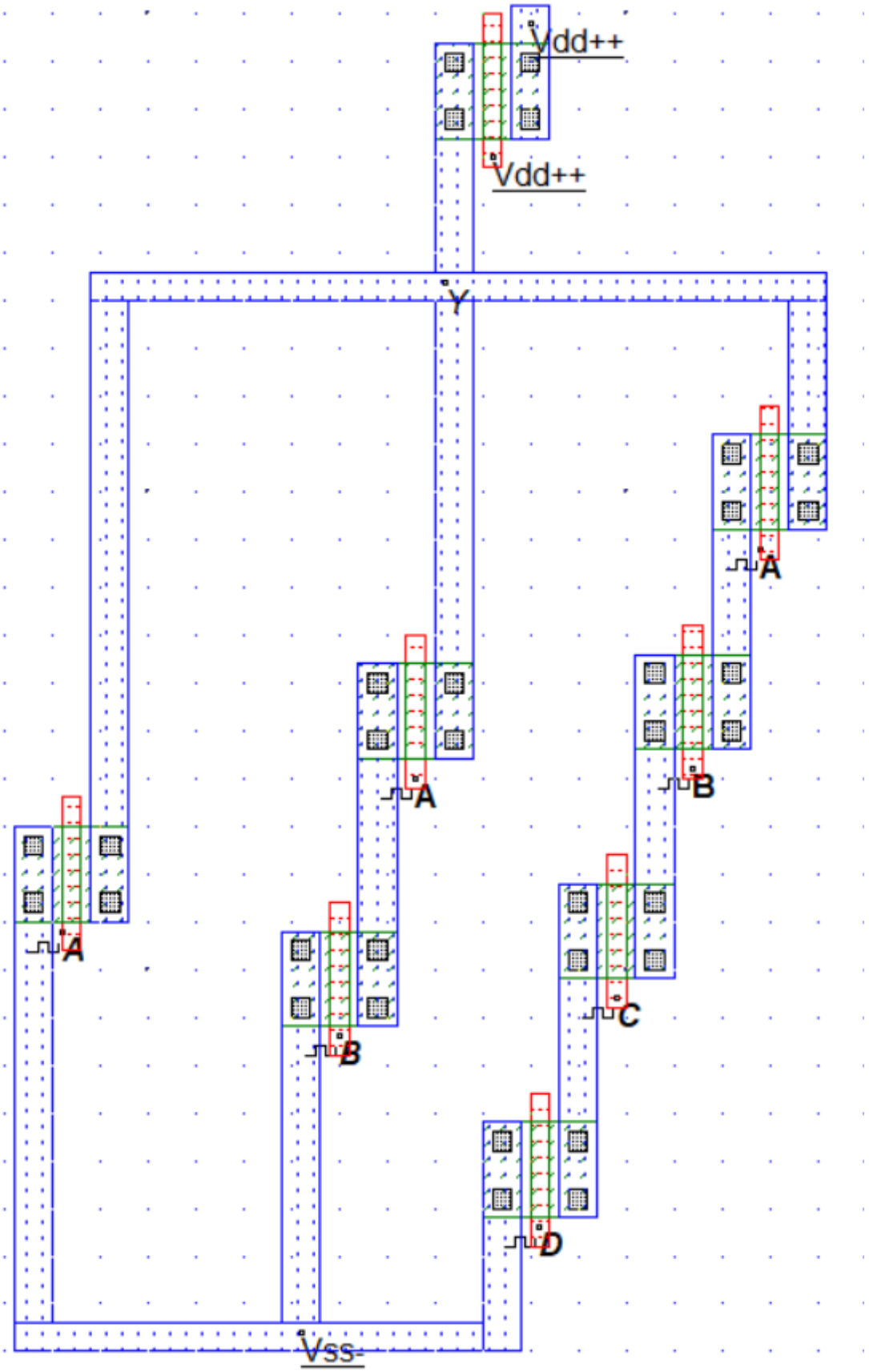

Figure 3: Y = $\overline{A + A.B + A.B.C.D}$ using nMOS Inverter with Enhancement Load

6 Specification

Table 1: MOSFET Dimensions for nMOS and pMOS Transistors

MOS	**Width** (μm)	**Length** (μm)	**Width** (λ)	**Length** (λ)
nMOS	0.600	0.120	10	2

Table 2: Parameters of Input Clock Signals for A,B,C & D

Parameter	**Value**	**Unit**
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.225	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.225	ns
Fall Time (tf)	0.002	ns

(a) Input clock signal of A

Parameter	**Value**	**Unit**
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.452	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.452	ns
Fall Time (tf)	0.002	ns

(b) Input clock signal of B

Parameter	**Value**	**Unit**
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	0.906	ns
Rise Time (tr)	0.002	ns
Time High (th)	0.906	ns
Fall Time (tf)	0.002	ns

(c) Input clock signal of C

Parameter	**Value**	**Unit**
High Level (V)	5.00	V
Low Level (V)	0.00	V
Time Low (tl)	1.814	ns
Rise Time (tr)	0.002	ns
Time High (th)	1.814	ns
Fall Time (tf)	0.002	ns

(d) Input clock signal of D

Table 3: Parameters for Vdd+ and Vss-

Parameter	**Value**	**Unit**
Vdd+	5.00	V
Vss-	0.00	V

7 Output Waveshape

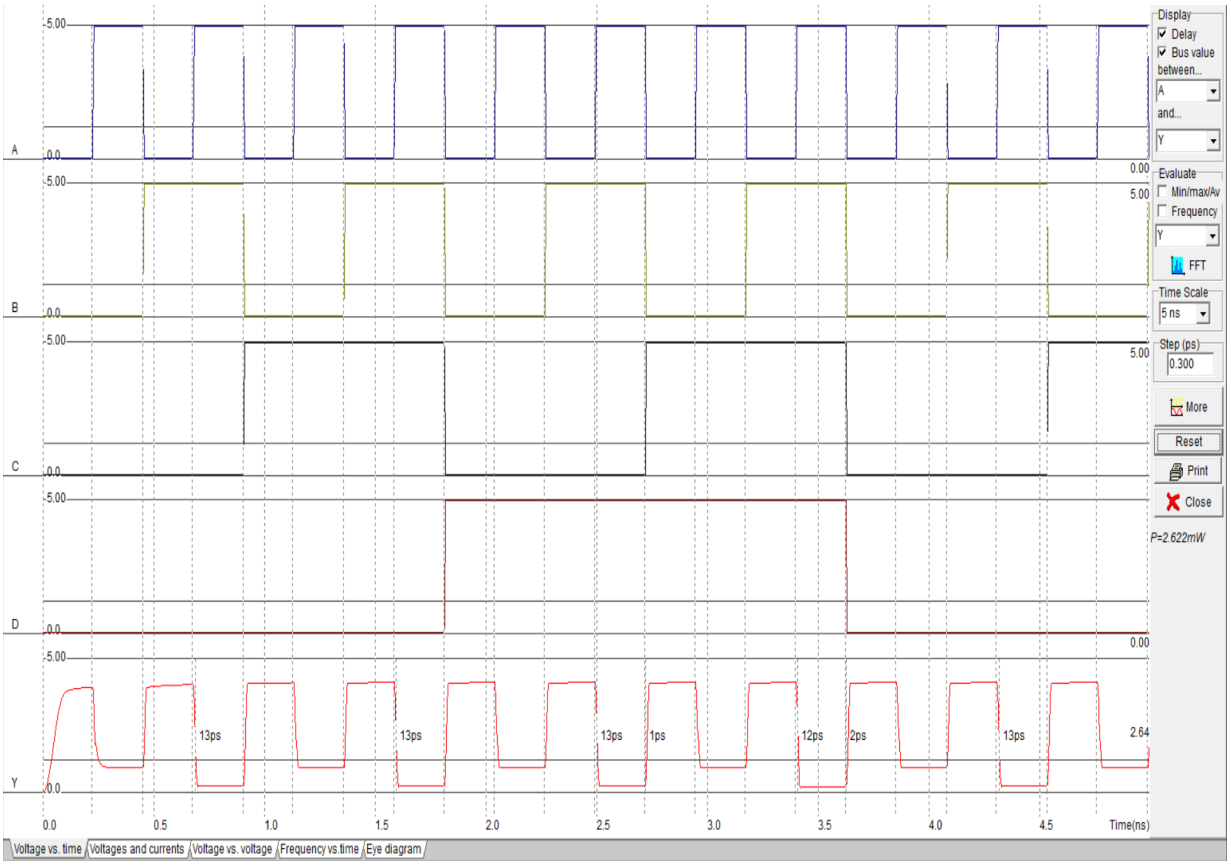

Figure 4: Output Waveshape of 4 Input logic gate [Y = $\overline{A + A.B + A.B.C.D}$]

8 Discussion

In the lab, we were tasked with designing and analyzing a 4-input logic gate while ensuring proper Design Rule Checking (DRC).
The proposed Boolean expression was:

$$Y = \overline{(A + A \cdot B + A \cdot B \cdot C \cdot D)}$$

For this Boolean expression, the circuit diagram, truth table, and waveform were designed before simulations. An nMOS inverter with an enhancement load was used for easier design implementation.
From the truth table, it was clearly observed that the output (Y) is the inverse of the input A's clock signals. Specifically, when the input signal A was high, the entire circuit's output was low; conversely, when A was low, the output was high, even though there were three additional input signals with different frequencies. The input signals were applied with different frequency to analyze the Boolean expression circuit according to the truth table. It was confirmed that the output accurately followed the predicted truth table.