

# **PCB Material Selection for High-speed Digital Designs**

# Outline

- **Printed Circuit Boards (PCBs) for High-speed Digital (HSD) applications**
- **PCB factors that limit High-speed Digital performance**
- **PCB material selection process and Isola product solutions**
- **Summary**

# What is High-speed Digital?

- **Digital signaling requiring use of high frequency design to preserve signal integrity**
  - Traces electrically behave as transmission lines
  - Crosstalk, attenuation, impedance mismatch are important
- **Common rule of thumb for threshold associated with trace electrical length**
$$t_d > t_r/4$$
  - $t_d$  = line delay=delay/unit length\*line length
  - $t_r$  = 20% - 80% signal rise time

# High-speed Digital Definitions

- In the 1990s digital signaling in electronics in 100 Mhz range was “high speed”
- Chips and computer performance have increased dramatically driving data rates to the Gbps range
- Today, data rates frequently exceed 10 Gbps and 25 Gbps signaling will be used to meet new demands

# HSD Applications

- **Products utilizing high-performance PCBs include:**
  - Servers
  - Routers
  - Storage Area Networks
  - Power Amplifiers
  - Transceiver Modules
  - High Speed Data Channels (PCIe4 for example)
- **Greatest demands on PCBs are those with highest data rates & longest channel lengths**

# Ever Increasing “Need for Speed”

- **Rapid growth of server, network & internet traffic drives need for higher data rates**
- **Key contributors of data demand include:**
  - Internet Consumer Applications
  - Cloud Computing and Storage
  - Virtual Servers
  - Advances in Scientific and Financial Computing

# Hardware Response to Demand

- **Availability of 100G servers**
- **Migration to 100G Gen 2 using 4x25 Gbps channels**
- **IEEE-standard 802.3bj expected to be finalized mid-2014 defining 4-lane PHY for operation over PCB backplane**



Juniper T1600, Brocade MLX,  
Cisco CRS-3

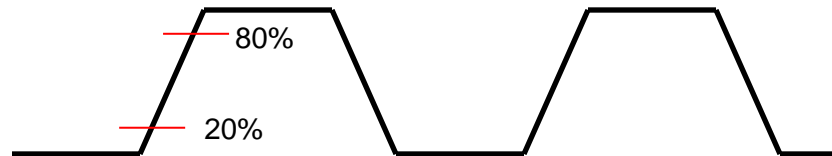
# RF/Microwave vs HSD PCBs

- **RF/microwave PCBs traditionally have only a few layers, in some cases just one or two**
- **PCBs for HSD applications often have 20 or more layers with hundreds of traces**
- **Materials suitable for RF/microwave may not be suitable for HSD due to processing considerations necessary for 20+ layer products**



# RF/Microwave and HSD Similarities

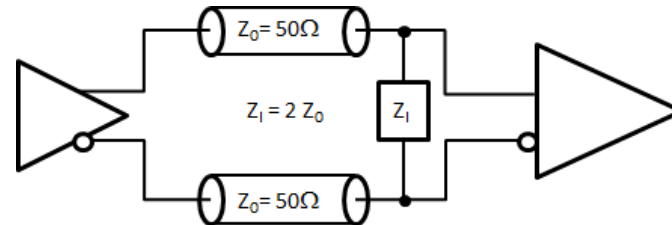
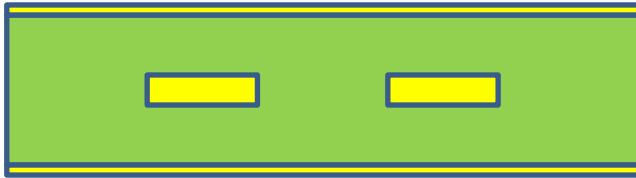
- For RF/microwave PCBs sinusoidal signals travel through PCB material and experience loss and distortion due to  $D_k$  &  $D_f$ , skin effects
- For HSD PCBs trapezoidal-shaped digital waveforms travel through material experience attenuation, pulse broadening, timing errors



- Frequency of concern for material properties can be the same in both cases

# Differential Signaling and HSD PCBs

- Differential signaling uses a differential pair of transmission lines
- The transmission lines have equal and opposite polarity signals traveling on them and are tightly timed to one-another



- **Differential signaling has several advantages**
  - Insensitive to ground connection quality between two ends of signal path
  - Data link maintains functionality with substantial attenuation in the channel
  - Supports very high data rates versus single-ended signal paths

**Serial Differential Signaling is the Signaling Protocol for Modern HSD Designs**

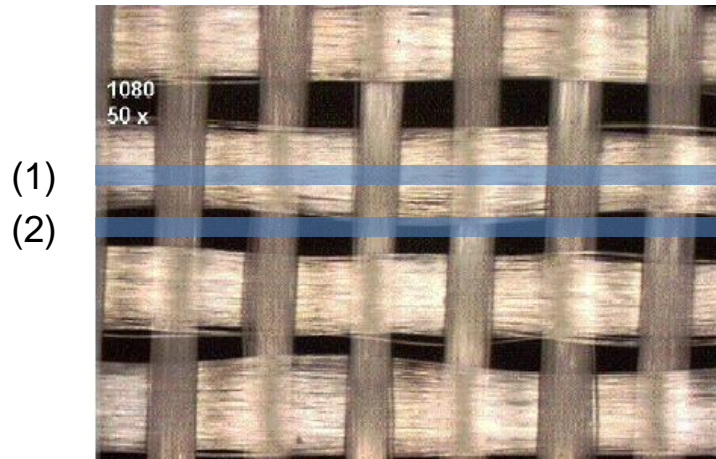
# **PCB Factors that limit HSD Performance**

# PCB Laminate Material Considerations

- **PCB laminates considered here consist of one or more plies of resin-impregnated glass cloth sandwiched between two copper foils**
- **The High-speed Digital performance of the laminate & resulting PCB depends on the quality of**
  - The resin
  - The copper foil
  - The weave of the glass

# PCB Dielectric Constant

- As a fiber/resin composite, PCB materials are inhomogeneous anisotropic dielectrics

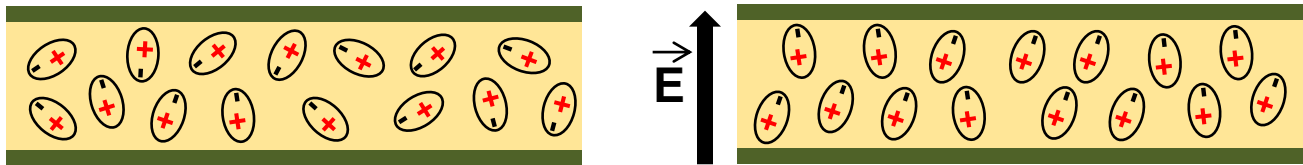


$$\epsilon_{\text{resin}} < \epsilon_{\text{fiber}}$$

- Propagation speed within material can vary depending on location of traces
  - Trace over fiber bundle (1) and trace over resin-rich area (2) see different effective dielectric constants
  - Differing propagation speeds creates timing skew & potential signaling errors

# PCB Material Dielectric Loss

- Dielectric materials have polarized molecules that move when subjected to the electric field of a digital signal



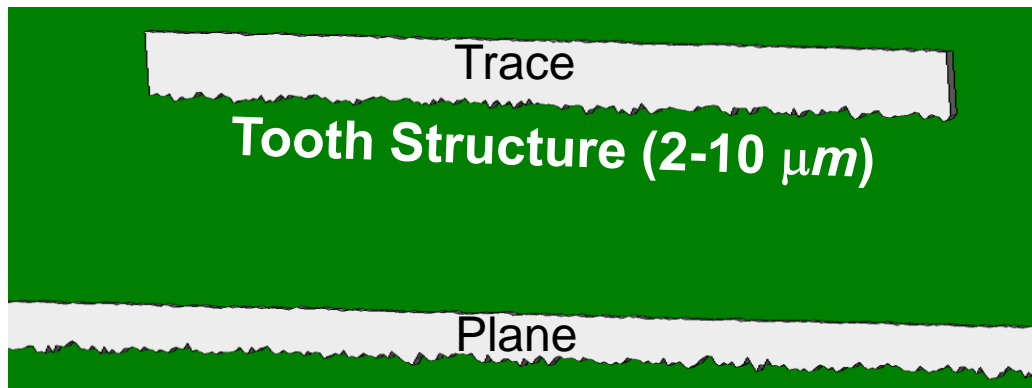
- This motion produces heat loss
- Loss results in signal attenuation that increases in direct proportion to signal frequency

# PCB Material Conduction Loss

- **The copper contributes to overall loss through the metal's resistive losses**
- **At high signal frequencies, the current in PCB copper is concentrated within a small depth near its surface (skin effect)**
- **Reduction in effective cross-sectional area increases the effective resistance**

# Conductor Surface Roughness

- Conductors on PCBs do not have perfectly smooth surfaces
- Rough copper improves peel strength of laminate
- Maximum peak-peak tooth size varies ~ 2-10 microns
- Surface roughness increases bulk copper resistance 10-50%
- Electrical impact of conductor roughness increases with increasing data rates

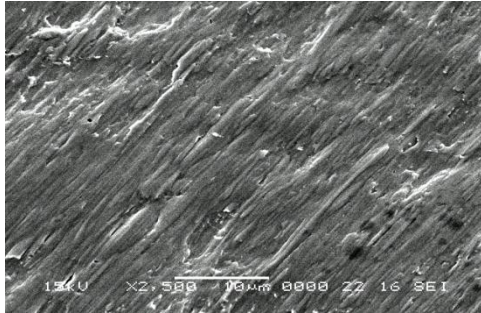


Frequency	Skin Depth (Copper)
50 Hz	9.3 mm
10 MHz	21 μm
100 MHz	6.6 μm
1 GHz	2.1 μm
10 GHz	0.66 μm

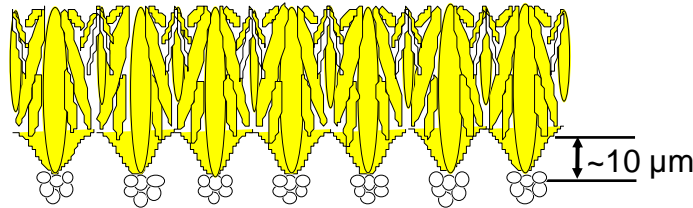


# Conductor Surface Roughness

## Resist side



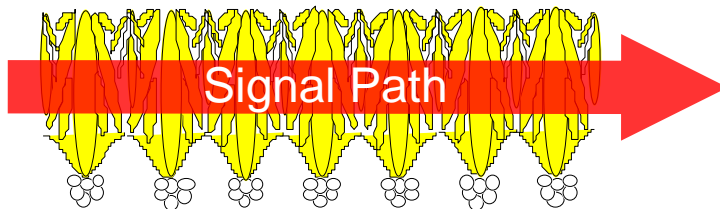
## Standard foil



## Bonding side

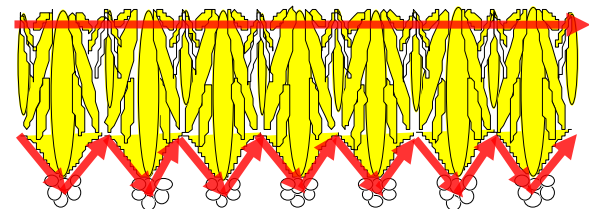


Frequency	Skin Depth
10 MHz	21 $\mu\text{m}$



The current is able to tunnel below the surface profile and through the bulk of the conductor

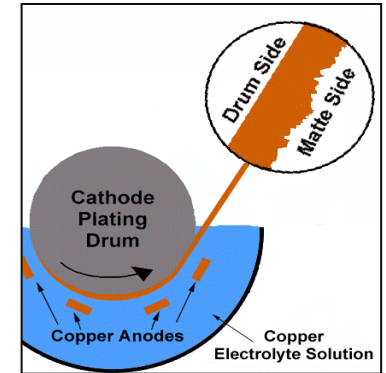
Frequency	Skin Depth
100 MHz	6.6 $\mu\text{m}$



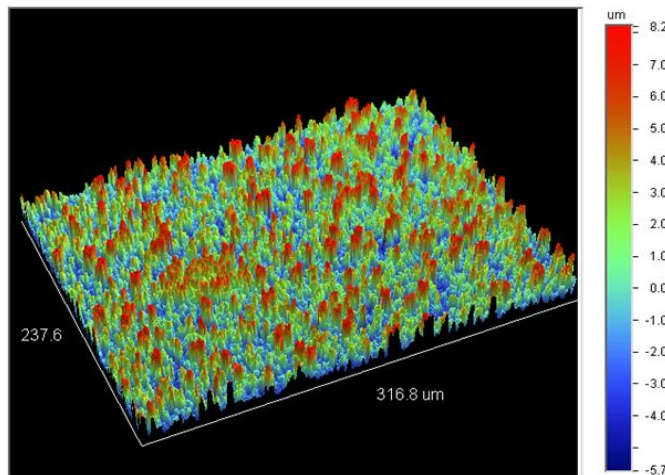
The current is forced to follow every peak and trough of the surface profile increasing path length and resistance

# Copper Foil Definitions

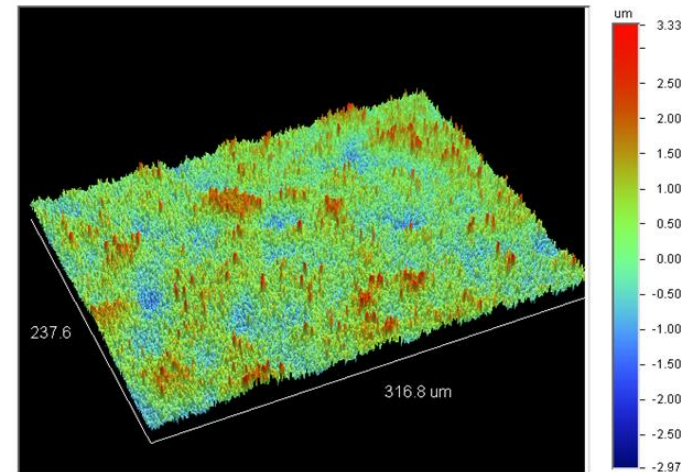
- **DSTF® (Drum Side Treated Foil):** Adhesion treatment is applied to shiny/drum side
- **RTF (Reverse Treated Foil):** Same as DSTF®
- **LP:** Low Profile Foil with Tooth 5.1-9.9 Microns
- **VLP:** Very Low Profile Foil with Tooth < 5 Microns
- **e-VLP/H-VLP:** Very Low Profile Foils
- **STD HTE (Standard Shiny Copper):** Adhesion treatment is applied to matte side



RTF:  $R_q=2.6 \text{ um}$ ,  $R_F=1.85$

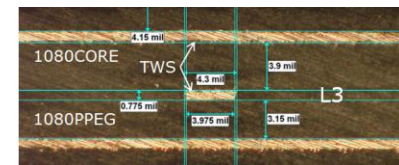
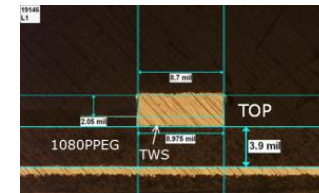
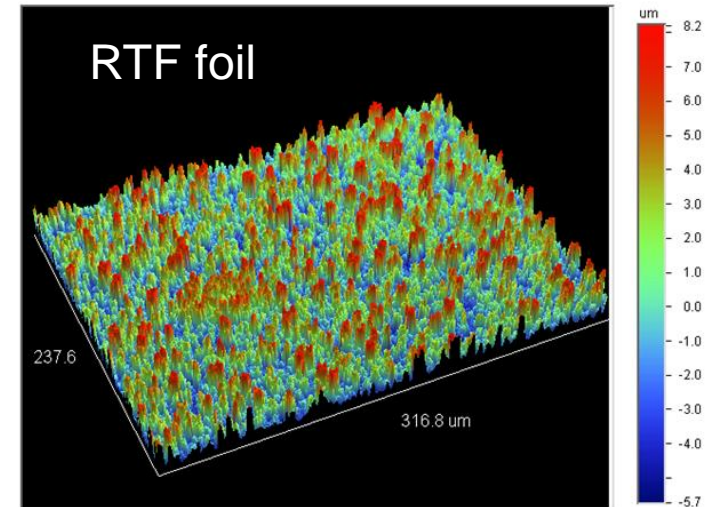


VLP:  $R_q=0.68 \text{ um}$ ,  $R_F=1.3$



# Surface Spikes Cause Increase in Capacitance

- Multiple spikes are about 10  $\mu\text{m}$  from top to bottom
- Electric field is singular on the spikes (similar to strip edges)
- Consistent for 2 line types
  - About 5% increase for MSL with one RTF surface
  - >10% increase for strip line with two RTF surfaces
- Consistent increase in group delay and decrease in characteristic impedance over very wide frequency band

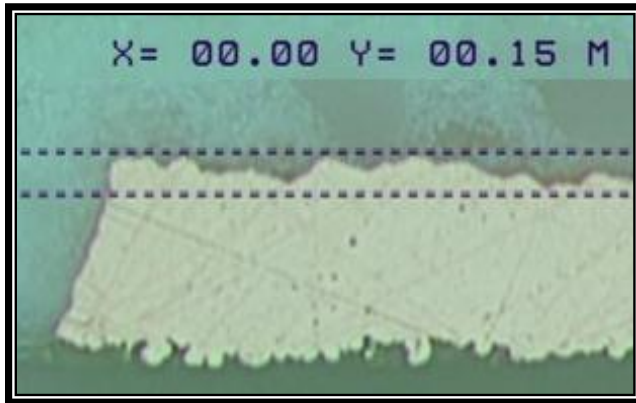


The effect was first noticed in *Deutsch, A. Huber, G.V. Kopcsay, B. J. Rubin, R. Hemedinger, D. Carey, W. Becker, T Winkel, B. Chamberlin, "Accuracy of Dielectric Constant Measurement Using the Full-Sheet-Resonance Technique IPC-T650 2.5.5.6" p. 311-314, ., IEEE Symposium on Electrical Performance of Electronic Packaging, 2002*

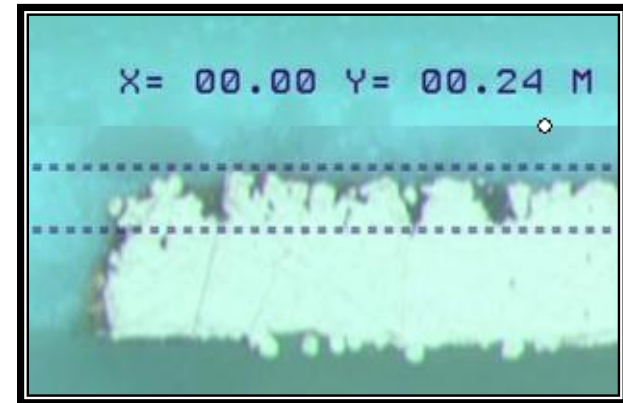


# Adhesion Promoter Effects

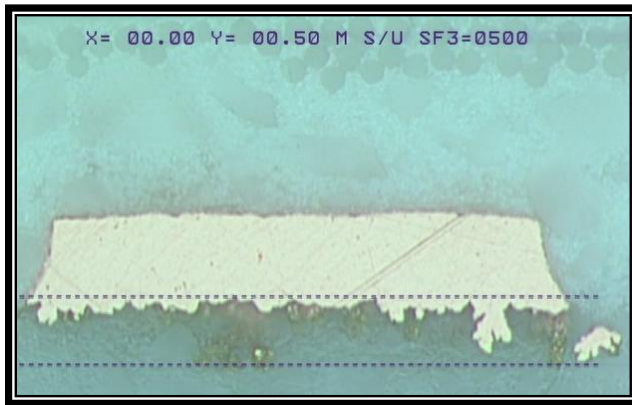
**RTF Foil**



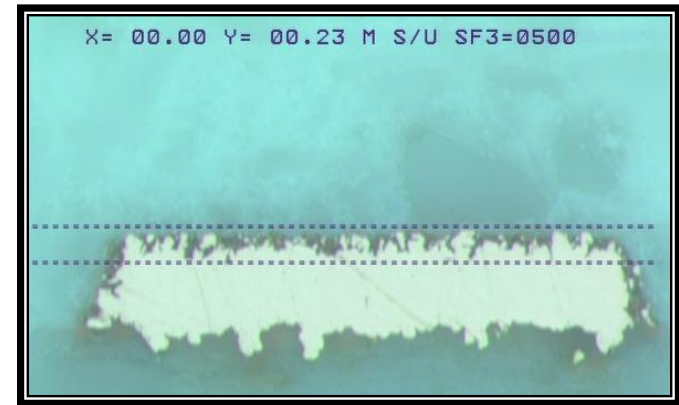
**RTF Foil + Adhesion Promoter**



**Shiny Foil**

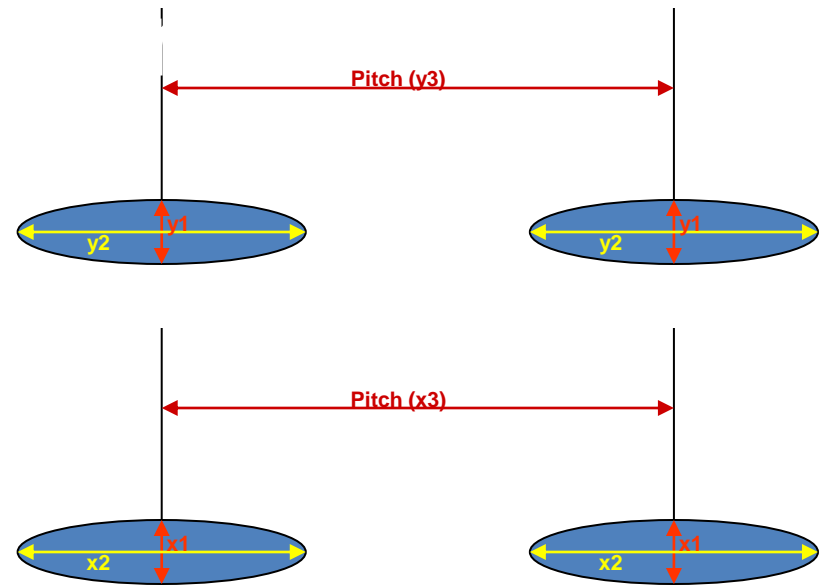
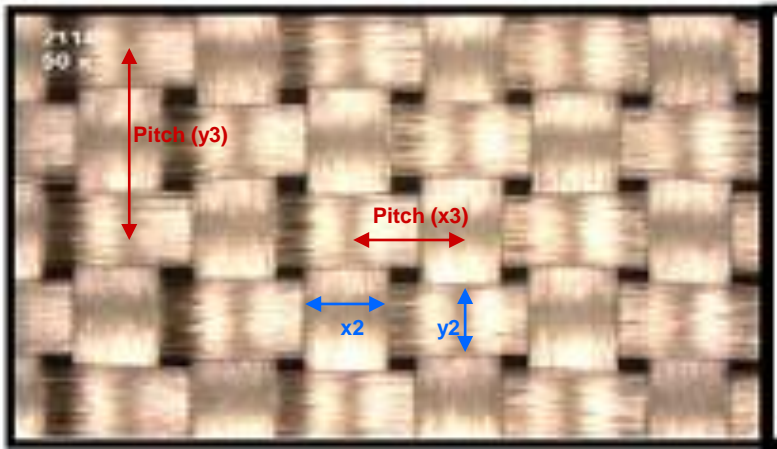


**Shiny Foil + Adhesion Promoter**



Courtesy of Viasystems

# Glass Fabric Definitions

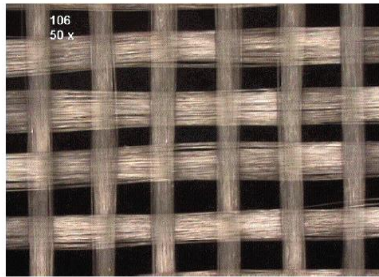


Glass type	X1	X2	X3	Y1	Y2	Y3
106	1.0	4.8	18.5	0.60	10.2	20.6
1067	0.82	8.85	14.3	0.78	12.4	13.7
1080	1.6	8.2	17	1.1	12.1	22.4
1086	1.44	10.8	16.6	1.0	14.7	17.1
2113 / 2313	2.4	10.5	17	1.0	15.3	18.2
3313	1.9	13.1	16.2	1.5	11	16.3
3070	1.7	12.7	14.8	1.7	12.6	14.2
2116	2.2	14.1	17.2	2.0	14.5	17.3
1652	2.4	15.3	17.5	2.9	15.9	18.8

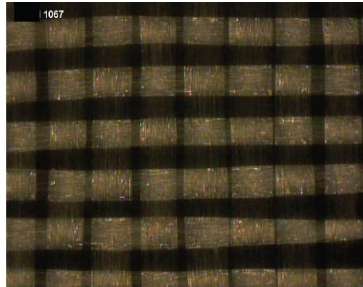
All Measurements in mls

# Fiber Weave Effect

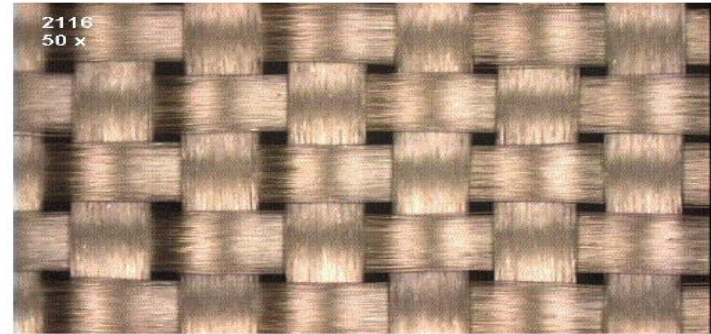
- PCBs materials are inhomogeneous dielectrics



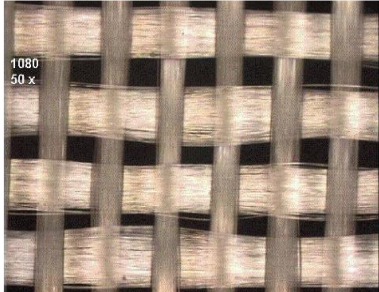
**106**  
106  
Warp and Fill count: 56 x 56 (ends/in)  
Thickness: 0.0015"/0.038mm



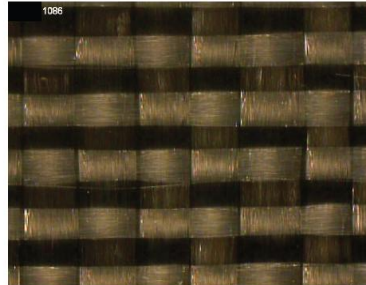
**1067**  
1067  
Warp & Fill Count: 70 x 70 (ends/in)  
Thickness: 0.0013"/0.032mm



**2116**  
2116  
Warp & Fill Count: 60 x 58 (ends/in)  
Thickness: 0.0038"/0.097mm



**1080**  
1080  
Warp & Fill Count: 60 x 47 (ends/in)  
Thickness: 0.0025"/0.064mm



**1086**  
1086  
Warp & Fill Count: 60 x 60 (ends/in)  
Thickness: 0.002"/0.050mm

$$\epsilon_{r_{composite}} = \epsilon_{r_{resin}} \times \text{Percentage Resin} + \epsilon_{r_{glass}} \times (1 - \text{Percentage Resin})$$

Inhomogeneous properties of PCB laminates lead to ***Fiber Weave Effects***

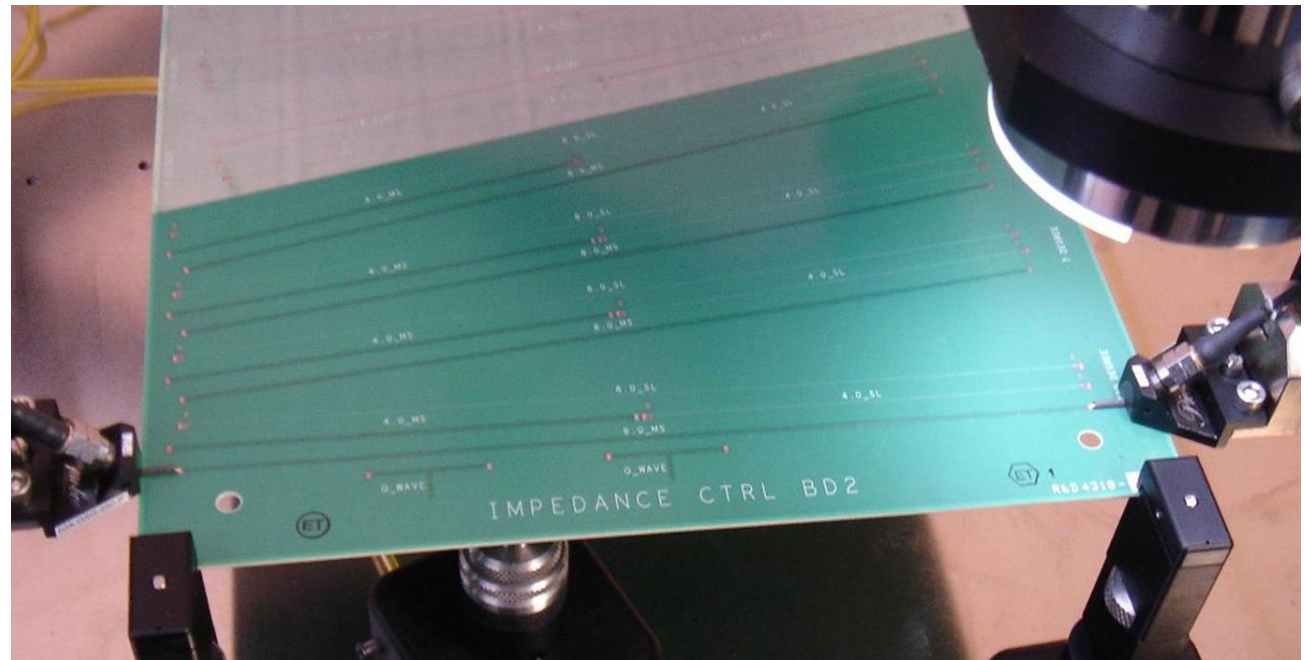


# Test board to Measure Fiber Weave Effects

- **8 layer stack-up with 2 microstrip layers (top and bottom) and 2 strip-line layers (L3, and L6)**
- **Microstrip Top:** RTF copper foil, 1080 prepreg, no solder mask
- **Strip L3:** RTF copper foil, laminate 1080 core and prepreg
- **Strip L6:** VLP copper foil, laminate 2116 core and prepreg
- **Microstrip Bottom:** VLP copper foil, laminate 2116 prepreg

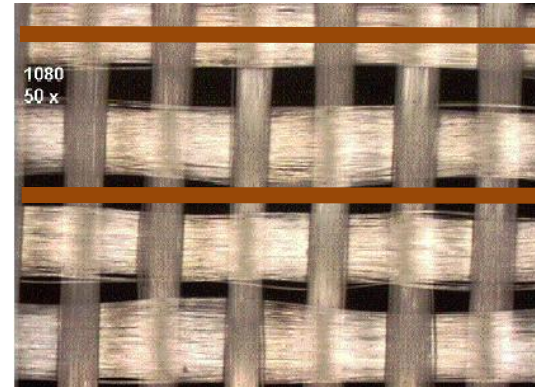
StackUp: LU=[mil], NL=8, T=37.525[mil]	
1	Signal: "TOP", T=2.75, Ins="Air", Cond="CondTop"
2	Medium: T=3.9, Ins="1080PPEG", DIE_002
3	Plane: "LAYER_2", Cond="COPPER", T=0.55, Ins="1080CORE"
4	Medium: T=3.9, Ins="1080CORE", DIE_004
5	Signal: "LAYER_3", T=0.775, Ins="1080PPEG", Cond="COPPER"
6	Medium: T=3.15, Ins="1080PPEG", DIE_006
7	Plane: "LAYER_4", Cond="COPPER", T=0.55, Ins="1080CORE"
8	Medium: T=2.5, Ins="1080CORE", DIE_008
9	Plane: "LAYER_5", Cond="COPPER", T=0.55, Ins="1080CORE"
10	Medium: T=5.05, Ins="2116PPEG", DIE_010
11	Signal: "LAYER_6", T=0.775, Ins="2116PPEG", Cond="COPPER"
12	Medium: T=4.9, Ins="2116CORE", DIE_012
13	Plane: "LAYER_7", Cond="COPPER", T=0.55, Ins="2116CORE"
14	Medium: T=5.3, Ins="2116PPEG", DIE_014
15	Signal: "BOTTOM", T=2.325, Ins="Air", Cond="COPPER"

Test structures: 4-inch and 8-inch line segment with transitions to probe pads



# Two Main Fiber Weave Effects

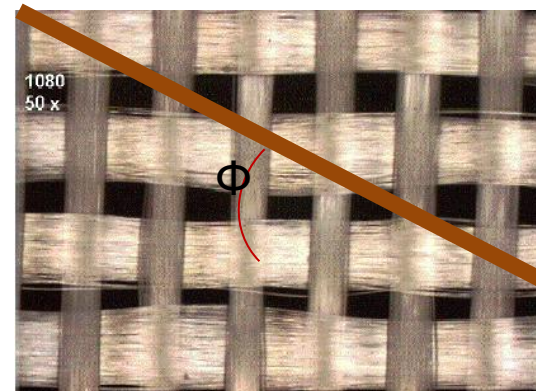
1. Effects due to location of trace with respect to fiber weave bundles



High  $E_r$ ;  
Low  $Z_o$

Low  $E_r$ ;  
High  $Z_o$

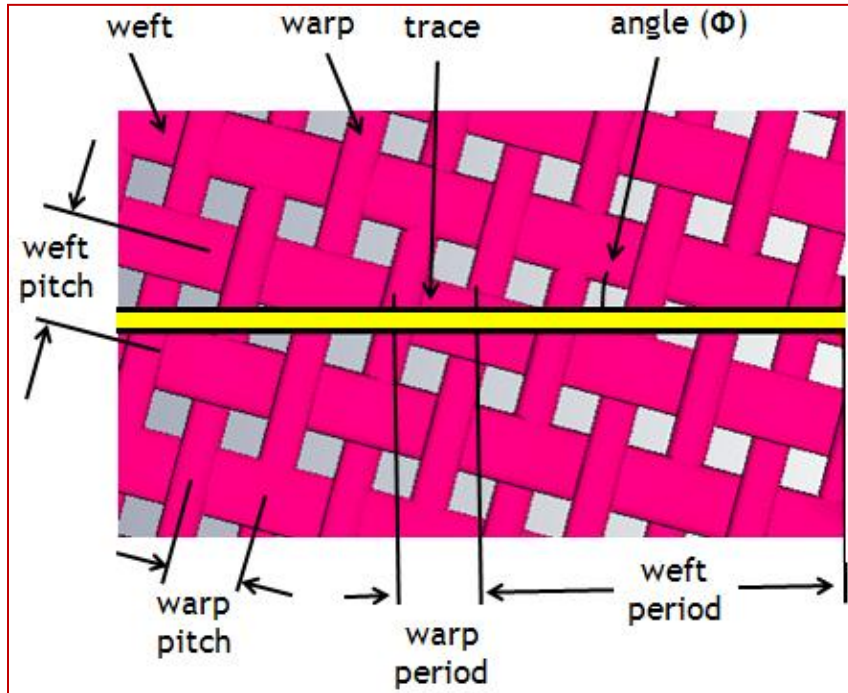
2. Effects due to periodic loading of trace by fiber weave bundles – resonance



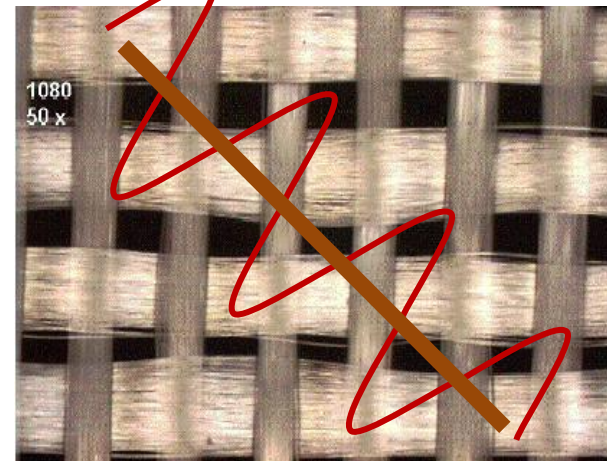


# Analytical Formulation of FWE

Arbitrary Angle:  $\Phi = 0^\circ > 45^\circ$



- Challenge is to find/define the spatial period
- Separate the Weft and Warp loading
- Warp loading is in pitch scale  $\rightarrow$  high frequencies  $\rightarrow$  neglected
- Weft loading occurs in a larger scale  $\rightarrow$  lower frequencies  $\rightarrow$  key role

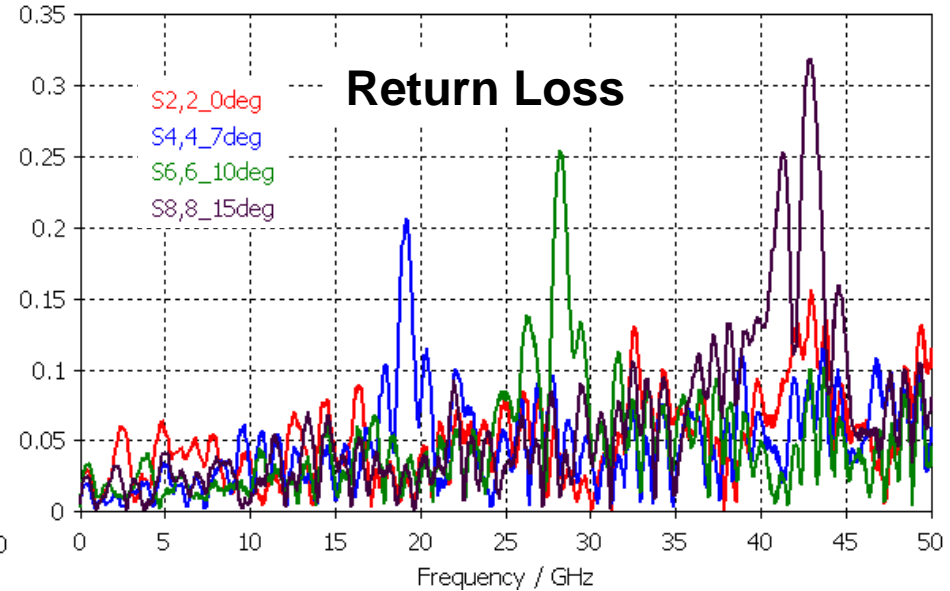
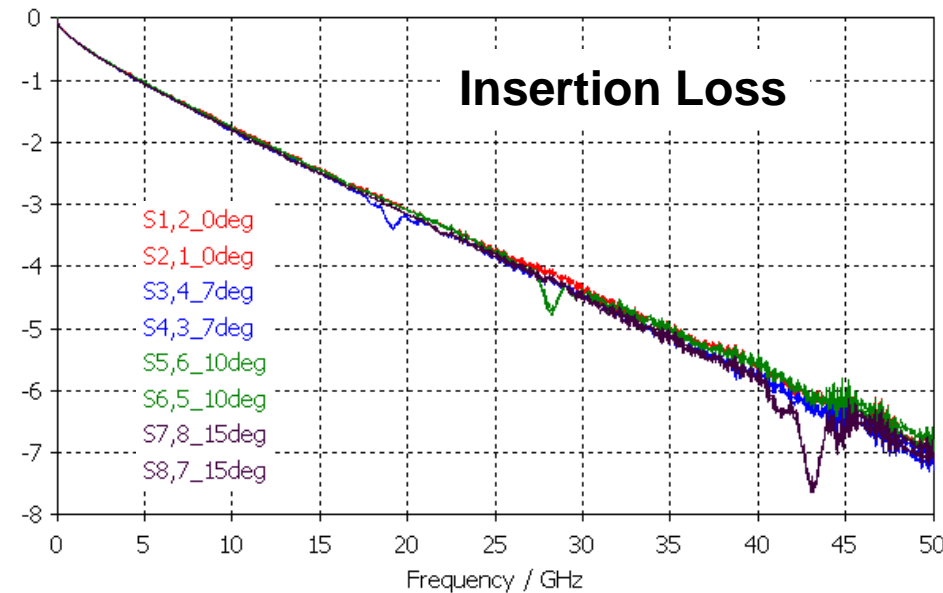


Weft spatial period is obtained from trigonometric expressions:

$$\text{weft period} = \sqrt{\text{pitch}^2 \left( \frac{1}{[\tan(\Phi)]^2} + 1 \right)} \quad \rightarrow \quad f_{res} = \frac{c}{2 \times \sqrt{\epsilon_{eff} \text{pitch}^2 \left( \frac{1}{[\tan(\Phi)]^2} + 1 \right)}}$$

# Fiber Weave Effect: Angle (1080)

## ■ Insertion and Return Loss, 4-inch traces

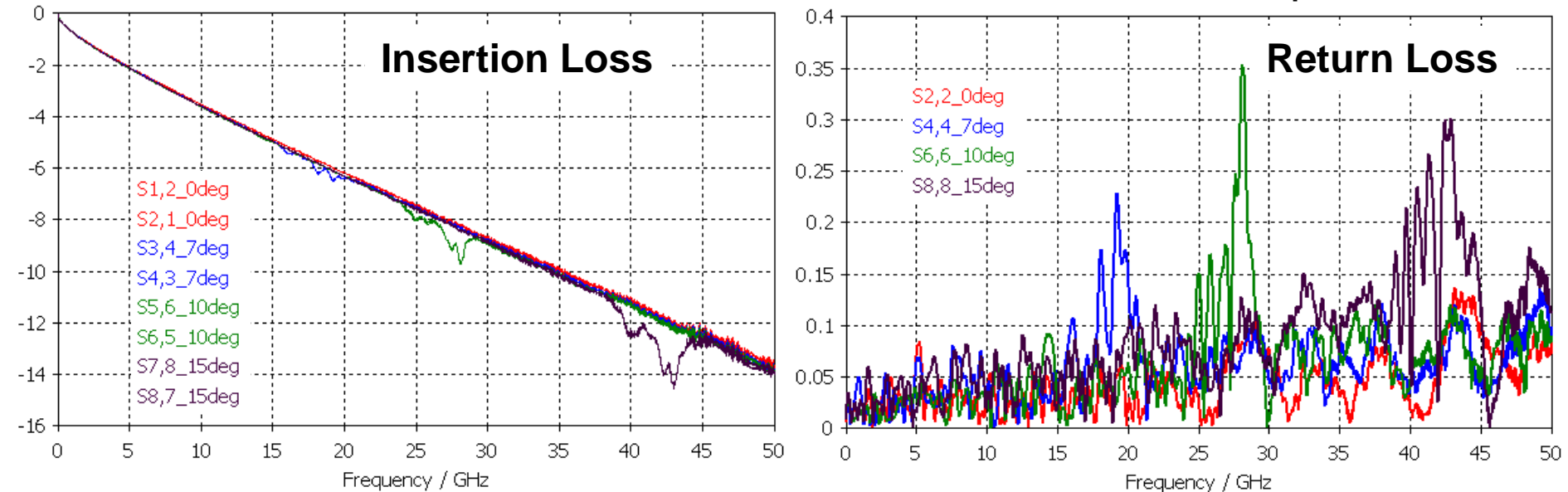


- Excellent agreement with analytical equation
- Strength of resonance increases with angle

Angle [Deg]	Equation 2 (GHz)	Measured (GHz)
7	19.6	19.17
10	26.76	28.2
15	41.39	42.86

# Fiber Weave Effect: Angle (1080)

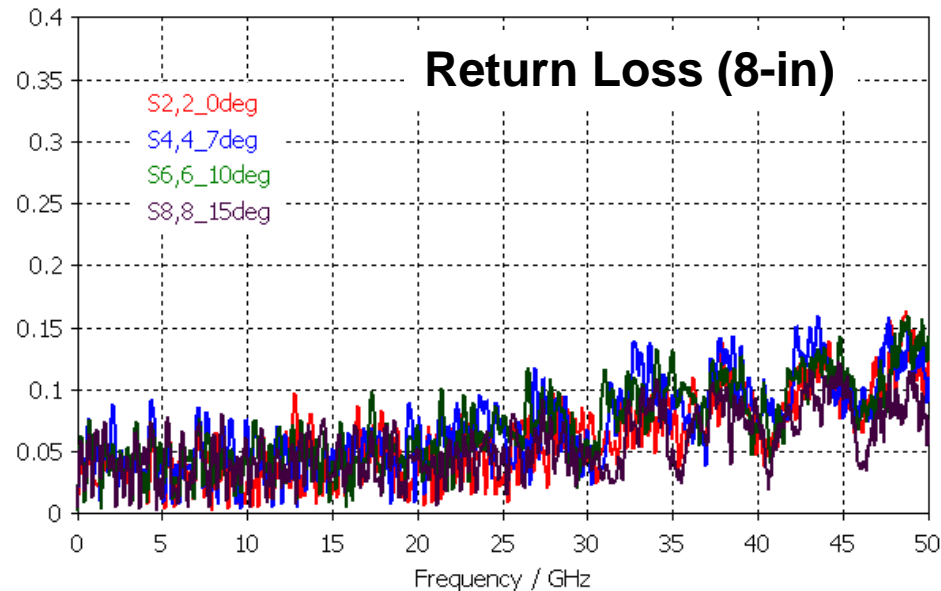
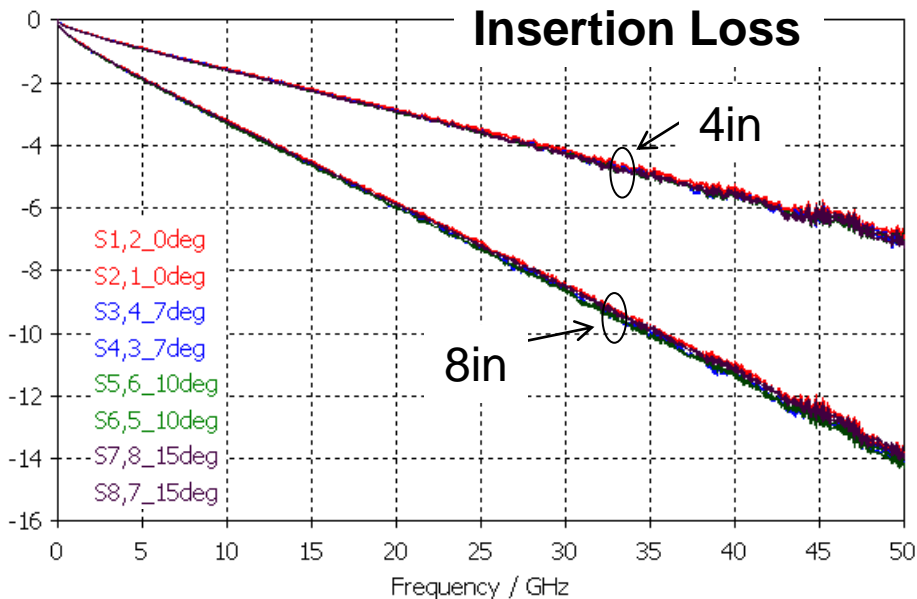
## ■ Insertion and Return Loss, 8-inch traces



- Excellent agreement with analytical equation
- Resonances “spread” over frequency due to fiber weave imperfections

# Fiber Weave Effect: Angle (2116)

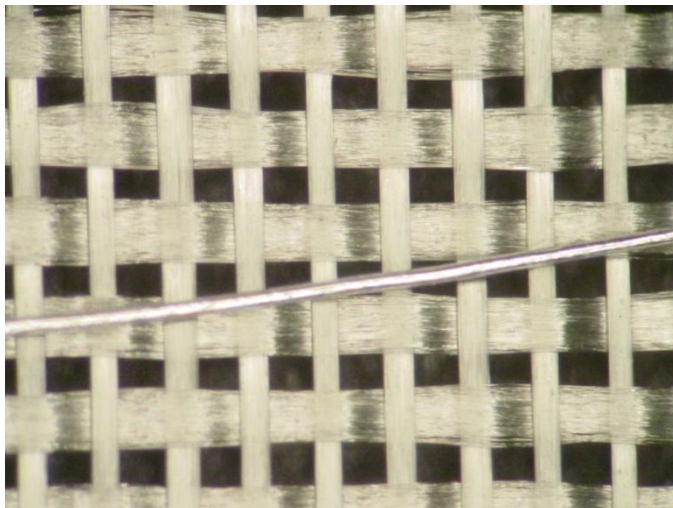
- Insertion and Return Loss, 4- and 8-inch traces



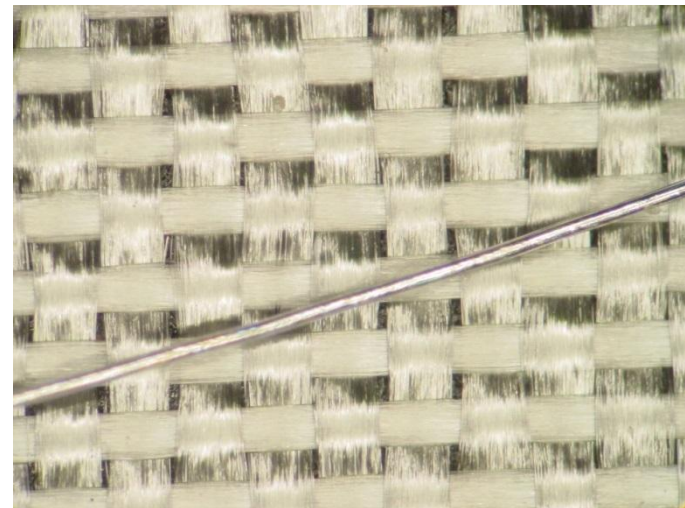
- No resonances were detected from measurement
- This is due to the denser and more homogeneous material

# Ways to Mitigate Fiber Weave Effects

- **Use more uniform glass such as 2116 or 3113 shown**
  - These styles have more uniform distributions of glass across the entire surface greatly reducing impedance variations
- **Use as wide a trace as practical for layout**
- **Route traces at an angle with respect to fiber warp/fill**
- **Use zig-zag routing**
- **Select materials having resin and fiber dielectric constants as close as possible to one another**



1080



3113



# **PCB Material Selection Process and Isola Product Solutions**

# PCB Material Selection

# Selecting the Right Material

- **Laminate material selection can not be condensed into a single page chart for easy selection**
- **High performance laminate material suppliers have a much better understanding of material performance**
- **Cost-to-performance evaluations must still be done by the system design team to ensure the lowest cost material that will do the job is selected**



# Isola High-speed Digital Comparison Data

Property	Units	IS415	FR408	FR408HR	FR408HRIS	I-Speed®	I-Speed®IS	GigaSync™	TerraGreen	I-Tera®MT	Tachyon
Tg C	°C	200	180	190	190	180 C	180 C	180	200	200	200
Td @ 5 % wt loss	°C	370	360	360	360	360	360	360	390	360	360
CTEz-axis ( 50 to 260 C )	%	2.80 %	3.50 %	2.80 %	2.80 %	2.70%	2.70%	2.70%	290%	2.80 %	2.90
CTEx-y axis pre-Tg	ppm/°C	13	13	13	13	13	13	13	13	12	12
CTEx-y axis post Tg	ppm/°C	14	14	14	14	14	14	14	14	13	13
T-260 ( TMA )	minutes	> 60	> 60	> 60	> 60	> 60	> 60	> 60	> 60	> 60	> 60
T-288 ( TMA )	minutes	> 20	> 20	> 30	> 30	> 60	> 60	> 60	> 60	> 60	> 60
Dk @ 2 GHz	-	3.72	3.67	3.66	3.39	3.6	3.30	4.15	3.44	3.30	3.00
Dk @ 5 GHz	-	3.71	3.66	3.65	3.38	3.58	3.28	4.15	3.44	3.30	3.00
Dk @ 10 GHz	-	3.71	3.65	3.64	3.37	3.57	3.27	4.15	3.44	3.30	3.00
Df @ 2 GHz	-	0.0134	0.0120	0.0090	0.0088	0.0060	0.0064	0.0053	0.0039	0.0036	0.0021
Df @ 5 GHz	-	0.0136	0.0127	0.0096	0.0094	0.0066	0.0066	0.0060	0.0039	0.0036	0.0021
Df @ 10 GHz	-	0.0136	0.0125	0.0094	0.0092	0.0071	0.0064	0.0066	0.0039	0.0036	0.0021
Typical Data Rates	Gbps	5	5	10	15	15	20	25	25	30	40
Electrical Strength	volts/mil	1100	1400	1700	1700	1700	1700	1700	1200	1200	1100
Peel Strength RTF H oz foil	lb/in	6.5	6.5	6.5	6.5	6.5	6.5	6.5	4.0	4.0	5
Peel Strength - after Thermal Stress	lb/in	7.0	7.0	5.5	5.5	5.5	5.5	5.5	4.0	4.0	6.0
Flammability	-	V-0	V-0	V-0	V-0	V-0	V-0	V-0	V-0	V-0	V-0
Moisture Absorption	%	0.15	0.15	0.061	0.061	0.06	0.06	0.061	TBD	0.016	0.01
Slash Sheets IPC 4101	Rev C	/21 /24 /26 /28 /121 / 124 / 129	/21 ' /24 /121 / 124	/21 /24 /121 /124 /129	/21 /24 /121 /124 /129	/21 /24 /121 /124 /129	/21 /24 /121 /124 /129	/21 /24 /121 /124 /129	TBD TBD	IPC 4103 /17	IPC 4103 /17
ZBC 2000 *		Yes	Yes	Yes	Yes	No	No	No	No	No	No

DSTF, DSRFoil, DSRFoil, GETEK, I-Fill, I-Speed, I-Tera, IsoDesign, Isola, IsoStack, Norplex, Polyclad, RCC, Lo-Flo and TURBO are registered trademarks of Isola USA Corp. in the U.S.A. and other countries. The Isola logo is a trademark of Isola USA Corp. in the U.S.A. and other countries. All other trademarks mentioned herein are property of their respective companies. Copyright © 2013 Isola Group, S.à.r.l. All rights reserved.

# Isola HSD Process Comparison Data

Product Description	Post Oxide Drying (Bake) (1)	Full Cure In Press	Heat Rates Deg. C/Min. (Deg. F /Min.)	Critical Range Deg. C (Deg. F)	Cool Rate (2) Deg. C/Min (Deg. F/Min)	Pressure (psi)	Drilling Recommendations (3)	Desmear Recommendations
IS415	110°C 2 hours	130 min >191°C (375°F)	3.5-5°C/min (6.3-9°F/min)	100-150°C (210-300°F)	Cool until <140°C <2.5°C/min (<4.5°F/min) (280°F)	275-375 Product Configuration Dependent	Tip Speed 120 SMM (400 SFM) Chip Load Moderate <50 um/rev (<2mils/rev)	Plasma Etch plus Chemical Desmear Do not use NMP
FR408	110°C 1-1.5 hours	95 min >191°C (375°F)	2.2-4.5°C/min (4-8°F/min)	80-135°C (175-275°F)	Cool until <140°C <2.5°C/min (4.5°F/min) (280°F)	250-350 Product Configuration Dependent	Tip Speed 120 SMM (400 SFM) Chip Load Moderate <50 um/rev (<2mils/rev)	Preferred: Plasma Etch plus 2 Pass Chemical Desmear Do not Use NMP
FR408HR	110°C 2 hours	130 min >191°C (375°F)	3.5-5°C/min (6.3-9°F/min)	100-150°C (210-300°F)	Cool until <140°C <2.5°C/min (4.5°F/min) (280°F)	275-375 Product Configuration Dependent	Tip Speed 120 SMM (400 SFM) Chip Load Moderate <50 um/rev (<2mils/rev)	Plasma Etch plus Chemical Desmear Do not use NMP
I-Speed	110°C 2 hours	130 min >191°C (375°F)	3.5-5°C/min (6.3-9°F/min)	100-150°C (210-300°F)	Cool until <140°C <2.5°C/min (<4.5°F/min) (280°F)	275-375 Product Configuration Dependent	Tip Speed 120 SMM (400 SFM) Chip Load Moderate <50 um/rev (<2mils/rev)	Plasma Etch plus Chemical Desmear Do not use NMP
GigaSync	110°C 2 hours	130 min >191°C (375°F)	3.5-5°C/min (6.3-9°F/min)	100-150°C (210-300°F)	Cool until <140°C <2.5°C/min (4.5°F/min) (280°F)	275-400 Product Configuration Dependent	Tip Speed 120 SMM (400 SFM) Chip Load Moderate <50 um/rev (<2mils/rev)	Plasma Etch plus Chemical Desmear Do not use NMP
I-Tera	Not Required	70 min >200°C (390°F)	2.5-4.5°C/min (4.5-8°F/min)	100-150°C (210-300°F)	Cool until <140°C <2.5°C/min (<4.5°F/min) (280°F)	300-400 Product Configuration Dependent	Tip Speed 120 SMM (400 SFM) Chip Load Moderate <50 um/rev (<2mils/rev)	Similar to high Tg FR4 Chemical desmear works well as does a light plasma
Tachyon	Not Required	70 min >200°C (390°F)	2.5-4.5°C/min (4.5-8°F/min)	100-150°C (210-300°F)	Cool until <140°C <2.5°C/min (<4.5°F/min) (280°F)	300-400 Product Configuration Dependent	Tip Speed 120 SMM (400 SFM) Chip Load Moderate <50 um/rev (<2mils/rev)	Similar to high Tg FR4 Chemical desmear works well as does a light plasma
Terra Green	Not Required	60 min >190°C (375°F)	3.5-5°C/min (6.3-9°F/min)	110-150°C (230-300°F)	Cool until <140°C <2.5°C/min (<4.5°F/min) (280°F)	375-425 Product Configuration Dependent	Tip Speed 120 SMM (400 SFM) Chip Load Moderate <50 um/rev (<2mils/rev)	Similar to high Tg FR4 Chemical desmear works well as does a light plasma

# Key Laminate Performance Indicators

## ■ Dielectric Constant (Dk)

- Matching material performance numbers is important. A small difference in this value between materials can impact impedance, line widths, and thus losses significant
- Consider construction options that allow you to find a drop in and match impedance

## ■ Dissipation Factor (Df)

- Values vary dramatically by resin content, resin type, frequency, and test method
- It is important to thoroughly understand the methods used to derive the numbers
- Compare Df to Df at equal test conditions and resin contents when looking at a suppliers data sheets

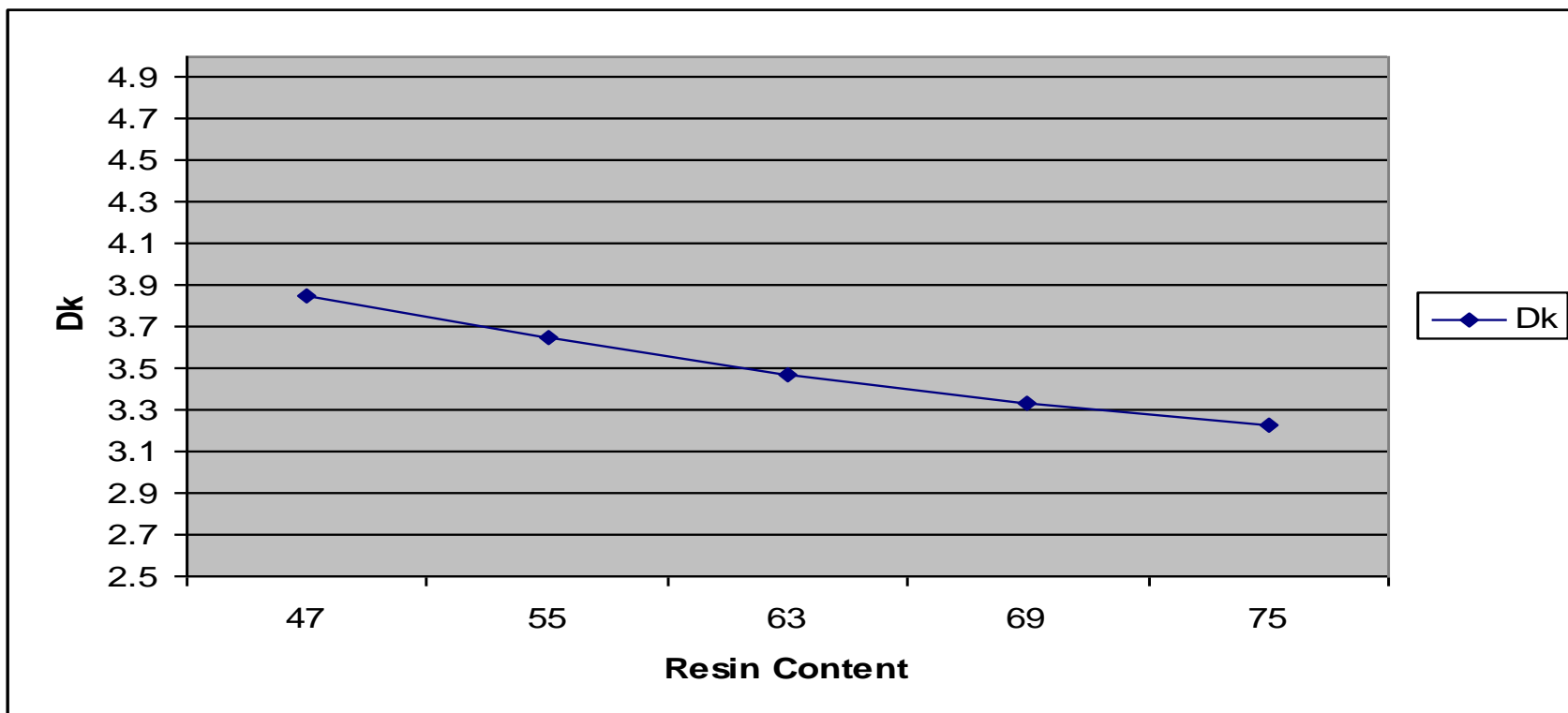
## ■ Copper Type

- Low profile copper provides better results than standard profile copper
- RTF or DSTF type foils offer significant improvements in loss characteristics. VLP foils are being used as well for better impedance

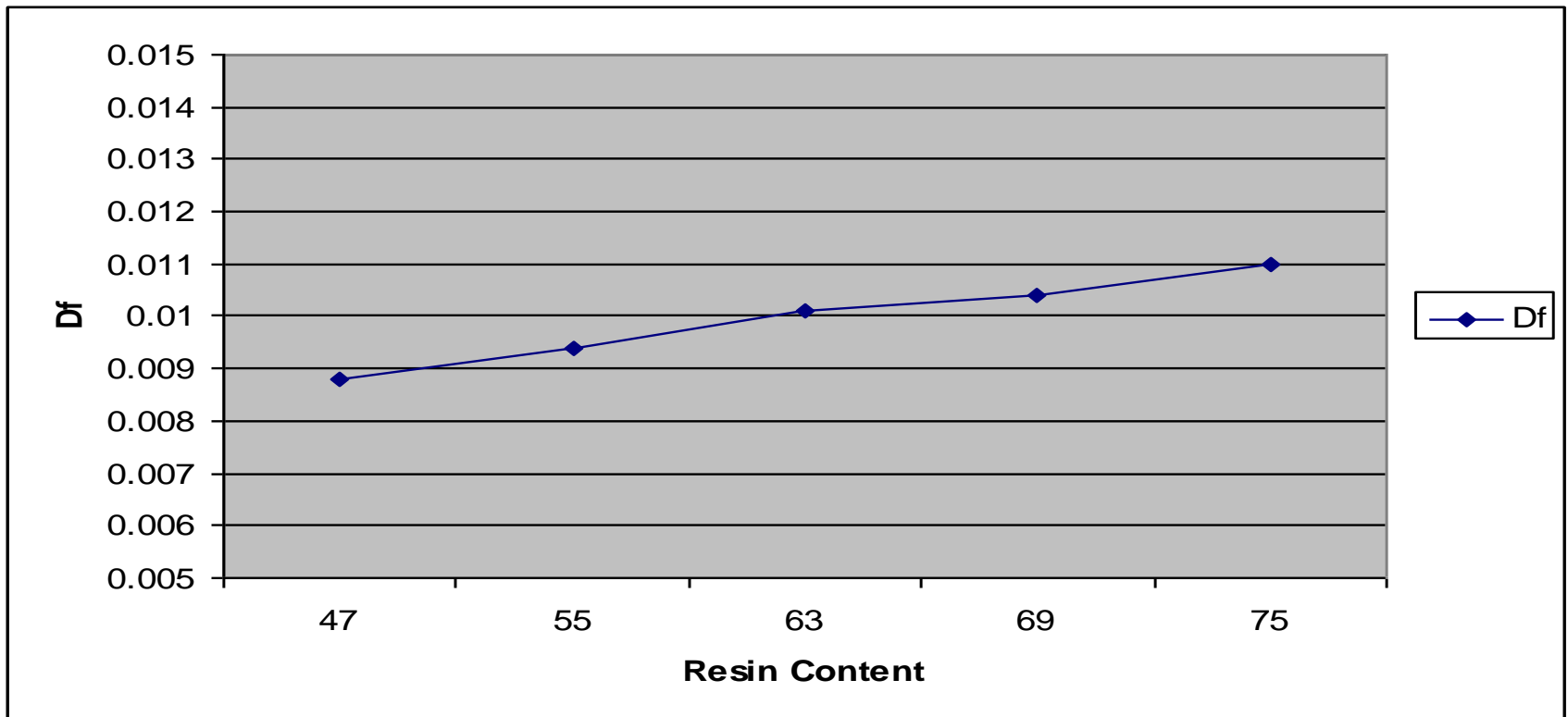
# Data Sheet Laminate Properties

- Laminate properties need to be fully tested across a range of resin contents, frequencies, constructions, using appropriate test methods
- Dk and Df values at 1 MHz and 1 GHz alone do not provide sufficient data for designers for High-speed Digital applications
- Laminate data sheets provide single points of information for Dk and Df based on a single resin content (usually in the 50% RC range).
- A range of data is essential for design work. The next slide shows the change in Dk and Df over the resin % range at 5 GHz

# FR408HR Dk vs Resin %



# FR408HR Df vs Resin %



# Electrical Test Methods

Methods	Specification	Sample		Frequency Range
		Thickness	Size	
Two Fluid Cell	IPC 2.5.5.3	20 to 250 mils	3.2" x 3.2"	1 MHz
Parallel Plate	IPC 2.5.5.9	20 to 60 mils	2" x 2"	100 MHz to 1.2 GHz
IPC Stripline	IPC 2.5.5.5	60 mils	2" x 2.75"	10 GHz
Bereskin Stripline	-	20 - 62 mils	4" x 1.125	2 - 15 GHz
Split Post Cavity	IPC 2.5.5.13	30 mils *	2" x 2.75"	1 GHz - 35 GHz**
All Test Methods are run using samples with no copper				
* The sample thickness for the Split Post Cavity Test Method is dependent on the testing frequency				
** Isola currently tests SPC at 3, 5 , 7 and 10 GHz				

- Different Test Methods will give varying results on the same resin systems
- Sample thickness and preparation are critical. Stacking of thin cores is not recommended. Air entrapment between samples will result in incorrect data
- When comparing data sheets the test methods need to be the same in order to compare Dk and Df values.

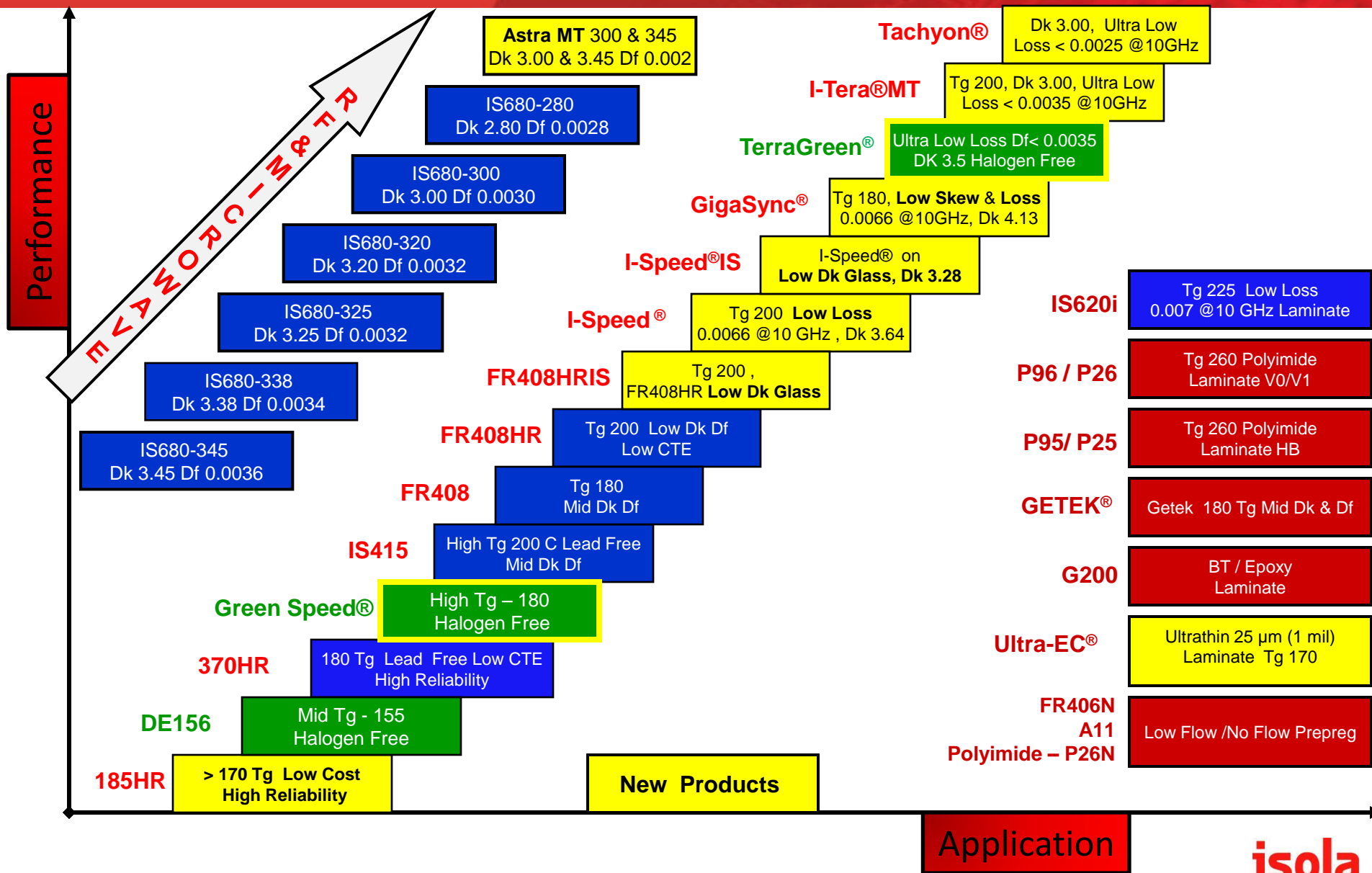
# Summary

- **Selecting a laminate material is a balancing act.**
  - **Simple substitution by core thickness is not advised**
  - **Use accurate data for modeling**
  - **Use simulation tools to understand changes in stack up and resulting material properties**
  - **Know your customers needs in detail**



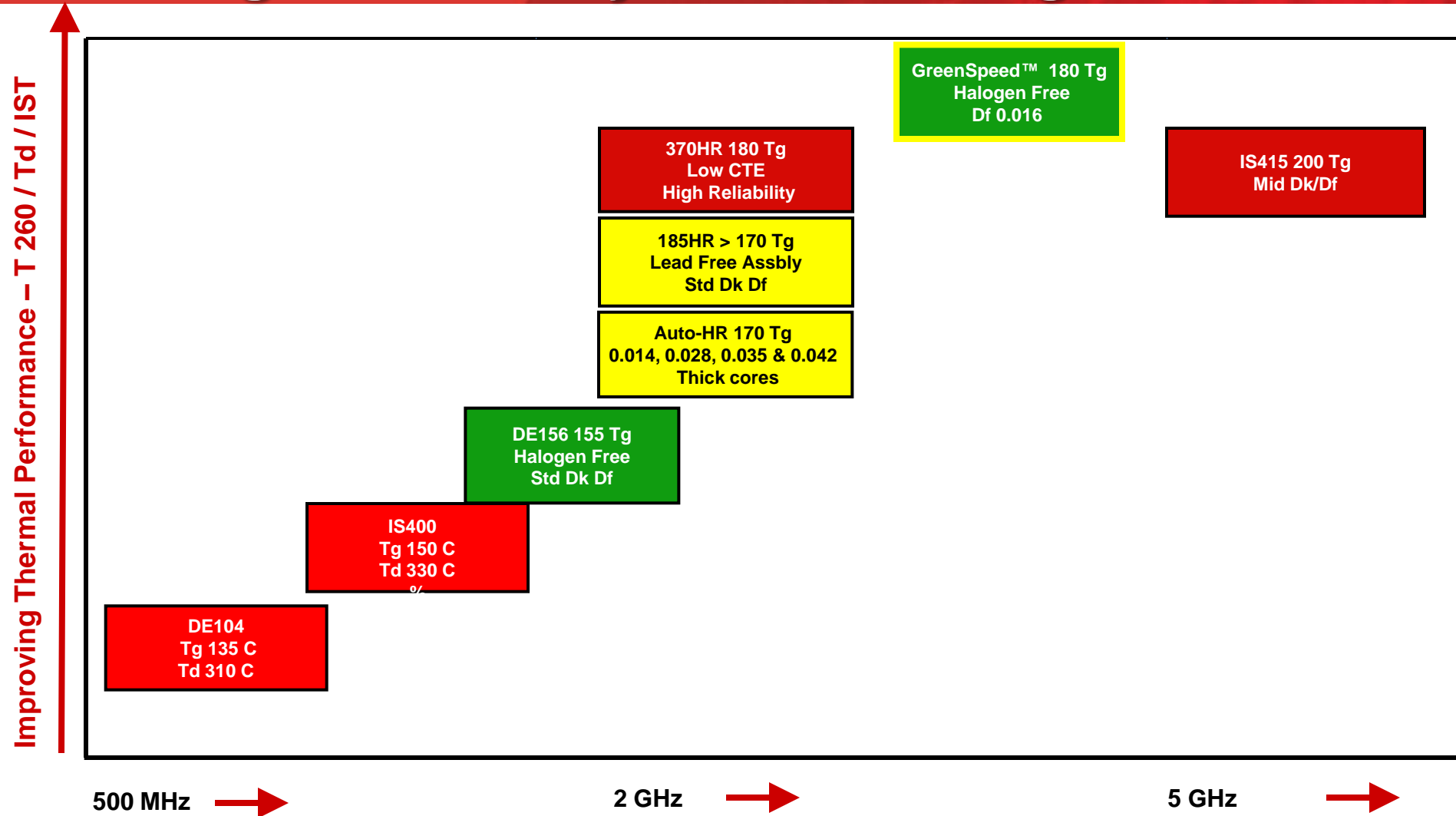
# Isola Product Solutions

# Isola Product Offering



# Isola Product Positioning

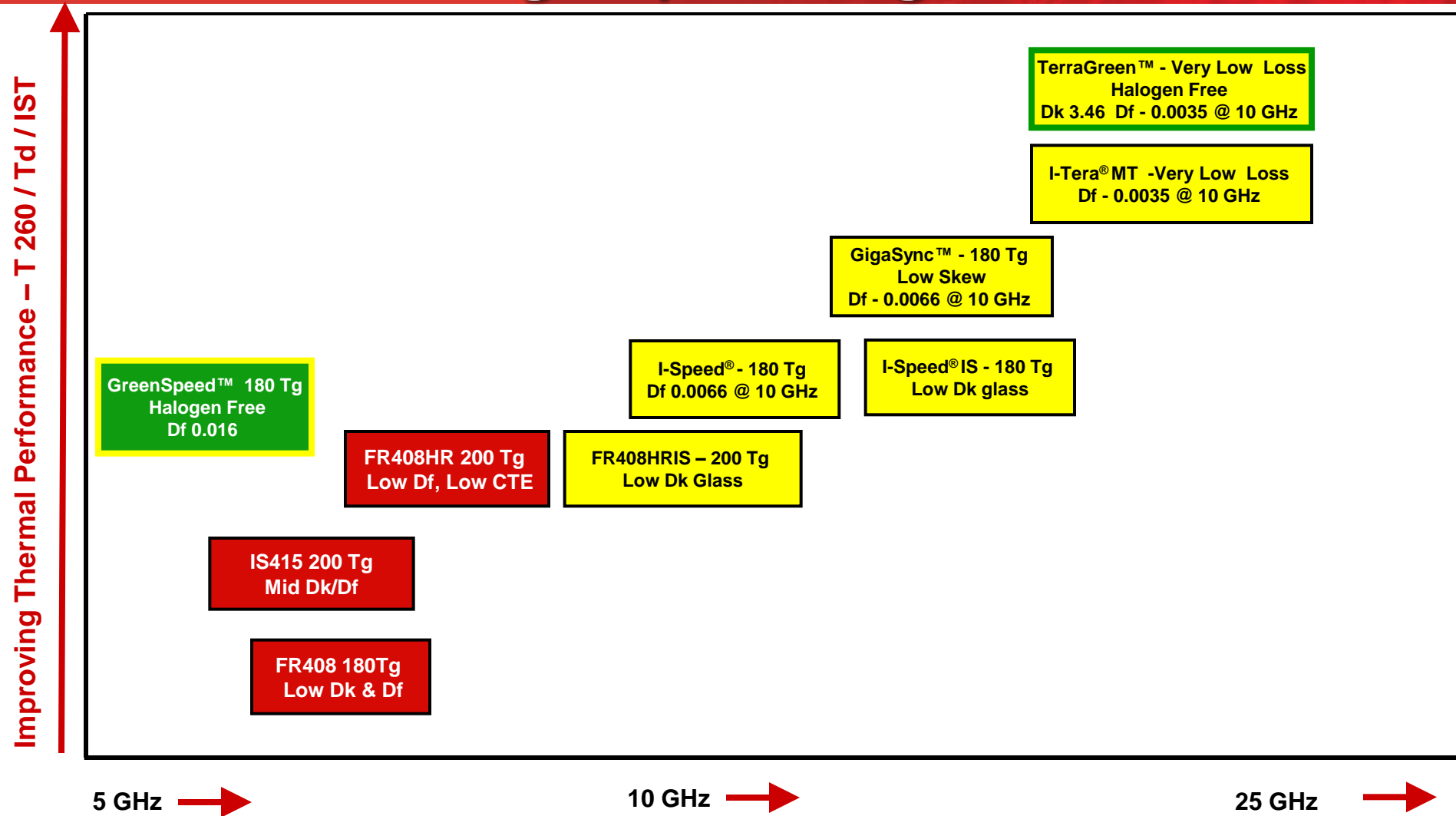
## High Reliability FR-4 & Halogen Free



Improving Electrical Performance – Lower Dk/Df – Higher Speed

# Isola Product Positioning

## High-speed Digital



Improving Electrical Performance - Lower Dk/Df - Higher Speed

# New HSD Product Offerings

- **I-Tera<sup>®</sup> MT**
- **TerraGreen<sup>®</sup>**
- **GigaSync<sup>®</sup>**
- **Tachyon<sup>®</sup>**

**I-Tera<sup>®</sup> MT**

# I-Tera<sup>®</sup> - MT

- Very low loss material for backplane, high data rate daughter cards, hybrid applications
- Uses standard E-glass
- Standard thicknesses available (nominal  $\pm 5\%$  for 0.020" and above)
- Full thin core offering from 0.0020 ( non ZBC ) to 0.018" for multilayer designs
- 0.020", 0.030" & 0.060" available for multilayer designs
- Square and MS spread glass weaves used - 1035, 1067, 1086, 1078
- Superior drilling performance –does not contain a ceramic filler
- Processing to date – plasma desmear not required
- No issues with ENIG in testing to date
- I-Tera has passed 10x 700 F re-work simulation testing.
- Compatible with Isola 185HR, 370HR and IS415 for hybrid constructions
- Prepreg can be stored at standard FR-4 conditions
- UL 94 V- 0
- UL MOT 130°C

# I-Tera<sup>®</sup> MT Typical Material Properties

Property	Units	I-Tera MT
Tg, (DSC)	C	200
Td, (TGA)	C	360
CTE - z-axis (50-260°C)	%	2.80
T-260 (TMA)	minutes	60
T-288 (TMA)	minutes	> 60
Dk - 2 GHz		3.00 - 3.45
Dk - 5 GHz		3.00 - 3.45
Dk - 10 GHz		3.00 - 3.45
Df - 2 GHz		0.0030 - 0.0035
Df - 5 GHz		0.0030 - 0.0035
Df - 10 GHz		0.0030 - 0.0035
Peels, 1 oz after thermal stress		5
Moisture Absorption	%	0.01
Flammability	-	94 V-0
UL recognition		non Ansi



**TerraGreen®**

# TerraGreen® Value Proposition

- Engineered for HSD applications that require halogen-free laminates
- Targeted for 12+ Gbps designs (backplanes, daughter cards, hybrid applications with Isola FR-4 materials)
- Supports 4G LTE base station applications, internet infrastructure, cloud computing & other markets
- Thicknesses from 0.002" to 0.018", 0.020", 0.030" & 0.060"
  - Spread glass options – 1035, 1067, 1086, 1078
  - VLP-2 copper = 2 micron copper
- Dk 3.46, Df 0.0039 @ 10 GHz
- UL 94 V-0
- UL approval in progress

# **TerraGreen® Processing Benefits**

- **No plasma required**
- **Enabler of low-cost hybrid constructions with Isola FR-4 materials**
- **Reduced drilling costs – better drilling and drill life due to no fillers**
- **Long shelf life**
- **Short press cycle (50% lower than competitive products)**

**GigaSync®**

# GigaSync®

- Engineered to eliminate skew issues in differential pairs on high data rate designs
- Targeted for 25+ Gb/s designs (backplanes and line cards) that require more bandwidth
- Optimized constructions to improve lead-free assembly performance
- Offers laminates and prepregs with engineered glass weaves to minimize micro-Dk effects of glass fabrics and to mitigate skew
  - 4.15 Dk on all cores and prepregs
  - 0.006 Df on all cores and prepregs
- Eliminates the need to rotate circuitry to the laminates
- UL approved in same family as FR408, IS415, FR408, FR408HR & I-Speed®

# GigaSync® Skew Data

## Skew in a Test PCB Fabricated with GigaSync Designed to Minimize Skew

Products	Vertical Skew (ps) 9" Fill			Horizontal Skew (ps) 14" Warp		
	Minimum	Maximum	Average	Minimum	Maximum	Average
IS415	0	8	5	30	123	88
FR408HR	1	8	5	3	43	20
FR408HR IS*	0	7	4.6	6	20	11.8
I-SPEED	3	10	4.5	1	59	18
I-SPEED IS*	1	4	1.3	5	12	7.5
I-TERA	1	12	6	1	13	9.5
I-TERA IS*	1	4	2.5	4	59	24.6
GigaSync	0	4	1.1	0	4	1.8

**Notes:**

1. \* IS Denotes Laminates with Low Dk Glass
2. 3313 Style E-Glass or 8313 Style Low Dk Glass used in all Builds
3. 9.5" Vertical Trace & 19.17" Horizontal Trace used for GigaSync

**This data was taken from five test PCBs made with the same artwork as those on the previous slide. Notice how much lower the skew is.**

**GigaSync is an enabler to get past the 100 Gbps barrier**

# GigaSync® Skew Data Vs Competition

## Test # 2 with Competitive Products

PCB #	VERTICAL SKEW (ps) 9" Fill			HORIZONTAL SKEW (ps) 14" Warp		
	Minimum	Maximum	Average	Minimum	Maximum	Average
MEG 4	1	2	1.4	1	28	14.8
MEG 6	0	4	2	2	37	8
I-SPEED	1	4	2	2	17	7
I-TERA	0	3	1.6	0	23	5.8
<b>GigaSync</b>	<b>0</b>	<b>4</b>	<b>1</b>	<b>0</b>	<b>4</b>	<b>2</b>

**GigaSync is an enabler to get past the 100 Gbps barrier**



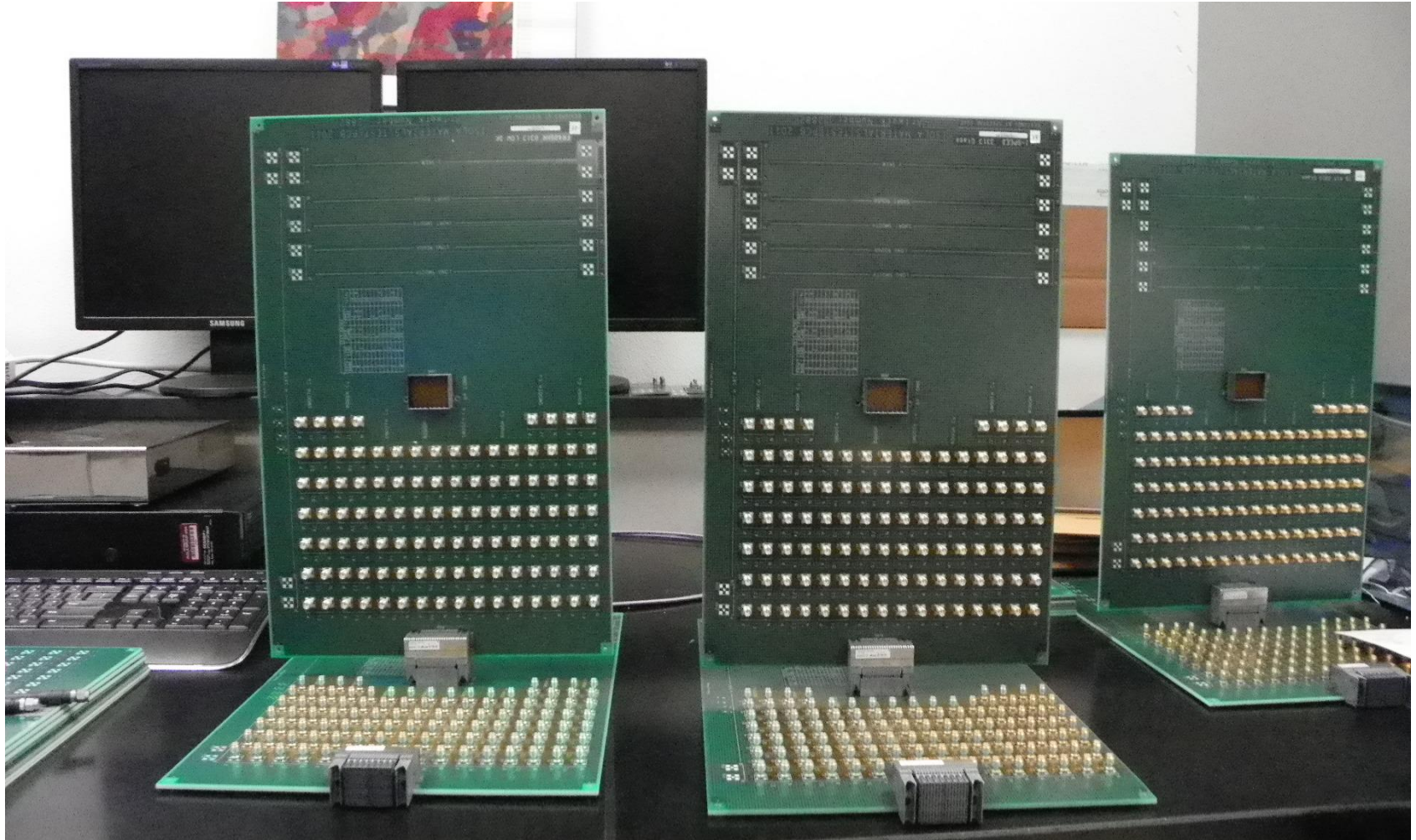
**Tachyon<sup>®</sup>**

# Tachyon®

- Engineered to improve insertion loss on the most demanding high-speed digital designs
- Targeted for 40+ Gb/s designs (backplanes and line cards) that require more bandwidth
- Optimized constructions to improve lead-free assembly performance
- Complete line of laminates and prepregs with spread glass weaves to minimize Dk effects of glass fabrics and to mitigate skew
- HDI-design friendly
- Can be used in hybrid builds as prepregs & laminates because of the low cure lamination cycle
- Dk 3.0, Df 0.002 at 10 GHz

# Signal Integrity Test Vehicle

# Isola Signal Integrity Test Vehicles



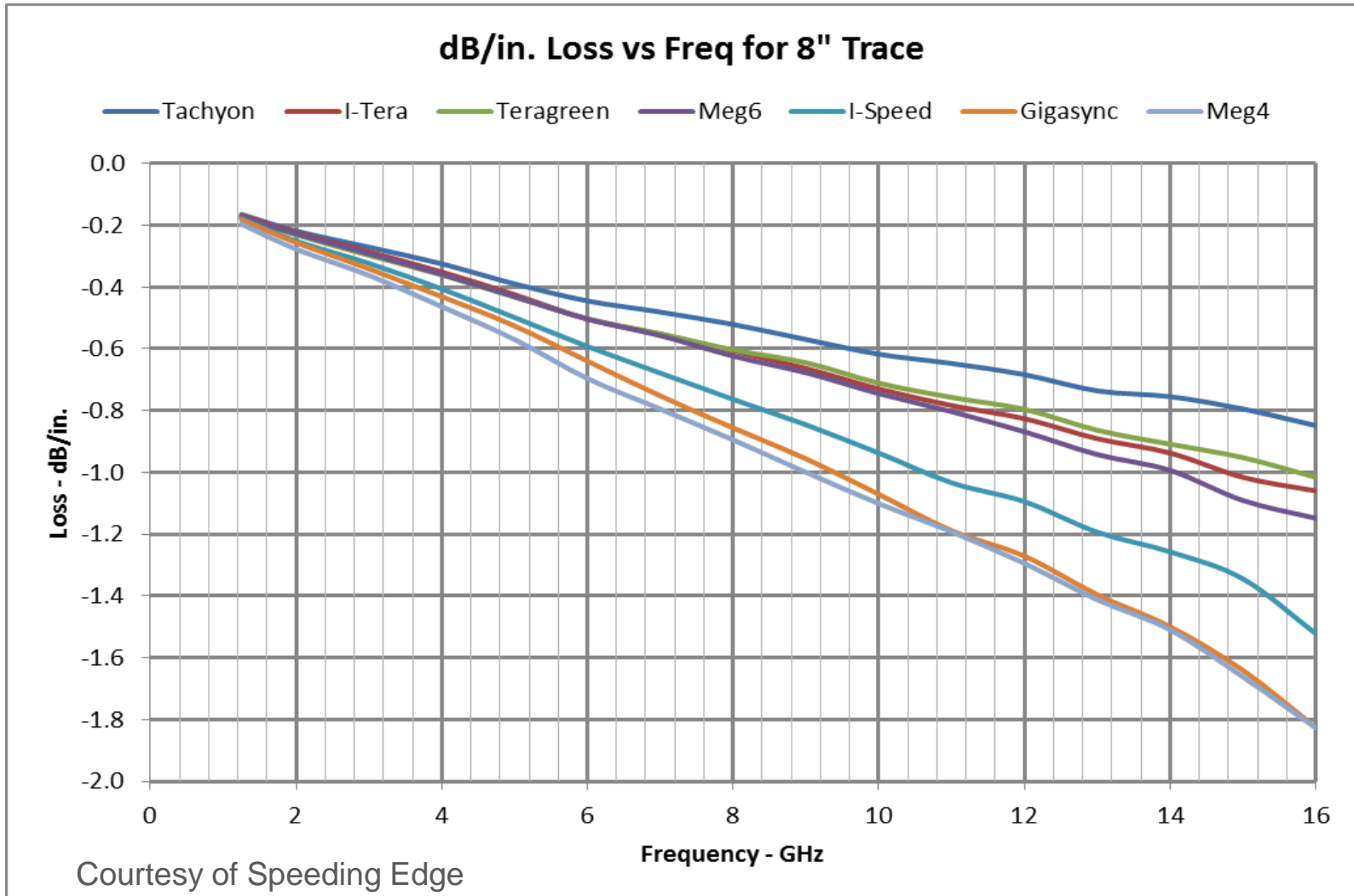
# Signal Integrity Test Vehicles

- **Differential pair lengths from 16" to 60" with a daughter card-backplane-daughter card configuration**
- **Reverse treat copper (RTF) and VLP-2 copper used in same board**
- **Measurements**
  - Differential skew
  - Loss tangent
  - Dielectric constant
  - Effect of copper roughness on overall loss
- **Amphenol Exceed connectors used**
- **Any combination of boards/different laminate material can be plugged together to represent classic backplane daughter card configurations**

# Measured Results

# Attenuation (dB/in) vs Frequency (GHz)

Measured results on 16 layer Lee Ritchey test vehicle





# Attenuation (dB/in) vs Frequency (GHz)

## Measured results on 16 layer Lee Ritchey test vehicle

GHz	Tachyon	I-Tera	Teragreen	Meg6	I-Speed	Gigasync	Meg4
1.25	-0.165	-0.169	-0.175	-0.173	-0.179	-0.183	-0.196
2.00	-0.219	-0.224	-0.231	-0.228	-0.251	-0.256	-0.278
3.00	-0.271	-0.286	-0.298	-0.293	-0.324	-0.341	-0.363
4.00	-0.325	-0.351	-0.361	-0.359	-0.406	-0.431	-0.464
5.00	-0.390	-0.425	-0.433	-0.431	-0.499	-0.526	-0.570
6.00	-0.445	-0.504	-0.503	-0.504	-0.593	-0.640	-0.696
7.00	-0.481	-0.553	-0.551	-0.558	-0.679	-0.753	-0.795
8.00	-0.521	-0.608	-0.604	-0.624	-0.764	-0.856	-0.895
9.00	-0.570	-0.664	-0.645	-0.678	-0.846	-0.956	-1.000
10.00	-0.618	-0.730	-0.711	-0.745	-0.938	-1.071	-1.101
11.00	-0.648	-0.784	-0.758	-0.804	-1.034	-1.189	-1.193
12.00	-0.684	-0.826	-0.796	-0.869	-1.095	-1.271	-1.295
13.00	-0.736	-0.891	-0.864	-0.943	-1.194	-1.396	-1.413
14.00	-0.755	-0.938	-0.909	-0.994	-1.258	-1.500	-1.510
15.00	-0.795	-1.016	-0.953	-1.091	-1.345	-1.641	-1.663
16.00	-0.849	-1.060	-1.016	-1.149	-1.523	-1.826	-1.828

Courtesy of Speeding Edge

# Isola HSD Product Offering Summary

Property	Units	IS415	FR408	FR408HR	FR408HRIS	I-Speed®	I-Speed®IS	GigaSync™	TerraGreen	I-Tera®MT	Tachyon
Tg C	°C	200	180	190	190	180 C	180 C	180	200	200	200
Td @ 5 % wt loss	°C	370	360	360	360	360	360	360	390	360	360
CTE z-axis ( 50 to 260 C )	%	2.80 %	3.50 %	2.80 %	2.80 %	2.70%	2.70%	2.70%	290%	2.80 %	2.90
T-260 ( TMA )	minutes	> 60	> 60	> 60	> 60	> 60	> 60	> 60	> 60	> 60	> 60
T-288 ( TMA )	minutes	> 20	> 20	> 30	> 30	> 60	> 60	> 60	> 60	> 60	> 60
Dk @ 2 GHz	-	3.72	3.67	3.66	3.39	3.6	3.30	4.15	3.44	3.30	3.00
Dk @ 5 GHz	-	3.71	3.66	3.65	3.38	3.58	3.28	4.15	3.44	3.30	3.00
Dk @ 10 GHz	-	3.71	3.65	3.64	3.37	3.57	3.27	4.15	3.44	3.30	3.00
Df @ 2 GHz	-	0.0134	0.0120	0.0090	0.0088	0.0060	0.0064	0.0053	0.0039	0.0036	0.0021
Df @ 5 GHz	-	0.0136	0.0127	0.0096	0.0094	0.0066	0.0066	0.0060	0.0039	0.0036	0.0021
Df @ 10 GHz	-	0.0136	0.0125	0.0094	0.0092	0.0071	0.0064	0.0066	0.0039	0.0036	0.0021
Typical Data Rates	Gbps	5	5	10	15	15	20	25	25	30	40
Electrical Strength	volts/mil	1100	1400	1700	1700	1700	1700	1700	1200	1200	1100
Peel Strength RTF H oz foil	lb/in	6.5	6.5	6.5	6.5	6.5	6.5	6.5	4.0	4.0	5
Peel Strength - after Thermal Stress	lb/in	7.0	7.0	5.5	5.5	5.5	5.5	5.5	4.0	4.0	6.0
Flammability	-	V-0	V-0	V-0	V-0	V-0	V-0	V-0	V-0	V-0	V-0
Moisture Absorption	%	0.15	0.15	0.061	0.061	0.06	0.06	0.061	TBD	0.016	0.01
Slash Sheets IPC 4101	Rev C	/21 /24 /26 /28 /121 / 124 / 129	/21 ' /24 /121 / 124	/21 /24 /121 /124 /129	/21 /24 /121 /124 /129	/21 /24 /121 /124 /129	/21 /24 /121 /124 /129	/21 /24 /121 /124 /129	TBD TBD	IPC 4103 /17	IPC 4103 /17
ZBC 2000 *		Yes	Yes	Yes	Yes	No	No	No	No	No	No

Test data on core material

Dk Df data by Bereskin Stripline Test Method

Data Rates are listed as those used on current production boards using a particular Isola product.

\* ZBC 2000 is licensed from Sanmina SCI

# Summary

# Summary

- **Printed Circuit Boards (PCBs) for High-speed Digital (HSD) applications**
- **PCB factors that limit High-speed Digital performance**
- **PCB material selection process and Isola product solutions**

# Contact Information

**Mike Miller**

**mike.miller@isola-group.com**

DSTF, DSRFoil, DSRFoil, GETEK, I-Fill, I-Speed, I-Tera, IsoDesign, Isola, IsoStack, Norplex, Polyclad, RCC, Lo-Flo and TURBO are registered trademarks of Isola USA Corp. in the U.S.A. and other countries. The Isola logo is a trademark of Isola USA Corp. in the U.S.A. and other countries. All other trademarks mentioned herein are property of their respective companies. Copyright © 2013 Isola Group, S.à.r.l. All rights reserved.