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0.200mm / 0.0079" (5 holes)
0.254mm / 0.0100" (39 holes)
0.400mm / 0.0157" (15 holes)
0.508mm / 0.0200" (90 holes)
1.000mm / 0.0394" (9 holes)
1.020mm / 0.0402" (40 holes)
1.067mm / 0.0420" (21 holes)
1.800mm / 0.0709" (2 holes) (not plated)
2.500mm / 0.0984" (4 holes) (not plated)
3.400mm / 0.1339" (8 holes) (not plated)
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NOTES: UNLESS OTHERWISE SPECIFIED.

STANDARDS:

 A. FABRINITE PCB IN ACCORDANCE WITH THE CURRENT REVISION OF IPC-6012, CLASS 2.
 B. INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH THE CURRENT REVISION OF ASME Y14.5M.
 C. DO NOT SCALE DRAWING.

MATERIAL:
 A. FRA Tg 180 C OR EQUIVALENT.
 B. EQUIVALENT MATERIAL SHALL BE ROHS COMPLIANT, HALOGEN FREE AND APPROVED BY YOURCO.
 C. THICKNESS OF INDIVIDUAL COPPER CLAD SHEETS SHALL BE IN AS DEFINED IN STACK-UP. SEE DETAIL D.

. FLAINESS: A. BOW AND TWIST OF ASSEMBLY SUB-PANEL OR SINGULATED PWB SHALL NOT EXCEED .025 MM PER MM. B. TEST IN ACCORDANCE WITH THE CURRENT REVISION OF IPC-TM-650 2.4.22

4. ETCH GEOMETRY:

A. MEASURE WIDTH FROM THE BASE OF THE METALLIZATION.
B. MINIMUM LINE WIDTH: 0.nn MM OUTER, 0.nn MM INNER LAYERS.
C. FINISHED LINE WIDTH AND TERMINAL AREA SHALL NOT DEVIATE FROM THE 1-TO-1 MASTER PATTERN IMAGE BY MORE THAN +/- 0.025 MM OR 20%, WHICHEVER IS LESS.

SURFACE FINISH: (SELECT APPROPRIATE FINISH(ES))
A. ENEPIG PLATING IN ACCORDANCE WITH CURRENT REVISION OF IPC4556. EXPOSED METAL SHALL HAVE 118–236 MICRO INCHES ELECTROLESS NICKEL, 2–6 MICRO INCHES ELECTROLESS PALLADIUM, AND 1.2MICRO INCHES GOLD.
B. ENIG PLATING PER CURRENT REVISION OF IPC-4552. EXPOSED METAL SHALL HAVE 118–236 MICRO INCHES ELECTROLESS NICKEL AND 2–5 MICRO INCHES GOLD.

6. DESTRUCTIVE TESTING: A. MICRO SECTION SAMPLE AND REPORT SHALL BE PROVIDED TO YourCo DESIGN ENGINEERING. B. SOLDER SAMPLE PROCESSED THROUGH LEAD—FREE SOLDERING SHALL BE INCLUDED WITH EACH SHIPMENT. C. X—OUT PANELS MAY BE USED FOR SOLDER SAMPLE.

7. HOLES:
A. PLATING IN HOLES SHALL BE CONTINUOUS ELECTROLYTIC COPPER WITH 0.025 MM MINIMUM BARREL THICKNESS.
B. MINIMUM FINISHED HOLE SIZE: 0.nn MM
C. HOLE SIZE MEASURED AFTER PLATING.
D. SEE ORILL CHART FOR FINISHED HOLE
E. ALL HOLES SHALL BE LOCATED WITHIN 0.08 MM OF TRUE POSITION AS SUPPLIED IN CAD DATA.

8. SOLDERMASK:
A. SOLDERMASK OVER BARE COPPER (SMOBC) ON PRIMARY AND SECONDARY SIDES USING SUPPLIED ARTWORK IN ACCORDANCE WITH CURRENT REVISION OF IPC-SM-940 TYPE B.
B. COLOR: MATTE GREEN
C. LIQUID PHOTO-IMAGEABLE (LPI) 0.001 MM TO 0.002 MM THICKNESS, HALOGEN FREE
D. NO BLEED-OUT ALLOWED OVER EXPOSED SMD PADS.
E. NO EXPOSED TRACES.

9. SILKSCREEN:
A SILKSCREEN PRIMARY AND SECONDARY SIDE WITH WHITE EPOXY, NON-CONDUCTIVE, NON-NUTRIENT INK.
B. ANY UNSPECIFIED STROKE WIDTH SHALL BE 0.13 MM
C. CLIP SILKSCREEN AWAY FROM ANY EXPOSED METAL.
D. VENDOR DATE CODE, LOGO, UL AND ANY ADDITIONAL MARKING TO BE LOCATED ON THE SECONDARY SIDE.
E. BAG AND TAG ACCEPTABLE FOR PMBS THAT ARE TOO SMALL FOR MARKING.

11. NON-DESTRUCTIVE EVALUATION:
A. ALL PWBS SHALL PASS 100% ELECTRICAL TEST USING SUPPLIED IPC-356 NETLIST IN ACCORDANCE WITH CURRENT REVISION OF IPC-9252. CLASS 2.
B. CERTIFICATE OF CONFORMANCE SHALL BE SUPPLIED WITH EACH SHIPMENT.

12. X-QUITS:
A. X-QUI BOARDS THAT DO NOT MEET ALL SPECIFICATIONS USING PERMANENT MARKING ON BOTH SIDES OF THE AFFECTED PCB.
B. PANELS THAT DO NOT HAVE ANY X-QUITS SHALL BE PACKAGED TOGETHER.
C. PANELS THAT HAVE NOT FEWER X-QUITS SHALL BE PACKAGED SEPARATE FROM NON-X-QUIT PANELS.
D. PANELS WITH MORE THAN n X-QUITS SHALL BE REJECTED.

13. PACKAGING REQUIREMENTS:
A. PWBS SHALL BE PACKAGED IN VACUUM SEALED INNER CONTAINERS.
B. OUTER CONTAINERS SHALL BE SUFFICIENT TO PREVENT DAMAGE DURING SHIPPING AND HANDLING.

14. IMPEDANCE (ALL TOLERANCES +/- 10%)
A. ALL 0.nn MM WIDE TRACES ON OUTER LAYERS SHALL BE 50 OHMS.
B. ALL 0.nn MM WIDE TRACES ON OUTER LAYERS SHALL BE 90 OHMS.
C. ALL 0.nn MM WIDE/0.nn MM SPACE PAIRS ON INNER LAYERS SHALL BE 90 OHMS.
D. VENDOR MAY ADJUST DESIGN GEOMETRIES UP TO +/-20% TO ACHIEVE TARGET IMPEDANCE. ADJUSTMENTS BEYOND 20% OF LINE WIDTH, SPACING OR DIELECTRIC THICKNEAY ADJUST DESIGN EAPPROVAL FROM YOUTE DENISHERING.

Layer Name	Туре	Material	Thickness (mm)	Color	Epsilon R	Loss Tangent
F.Silkscreen	Top Silk Screen	Not specified	0 mm	Not specified	1	0
F.Paste	Top Solder Paste		0 mm		1	0
F.Mask	Top Solder Mask	Not specified	0.01 mm	Not specified	3.3	0
F.Cu	copper		0.035 mm		1	0
Dielectric	core	FR4	0.508 mm	Not specified	4.5	0.02
In1.Cu	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.508 mm	Not specified	4.5	0.02
In2.Cu	copper		0.035 mm		1	0
Dielectric	core	FR4	0.508 mm	Not specified	4.5	0.02
B.Cu	copper		0.035 mm		1	0
B.Mask	Bottom Solder Mask	Not specified	0.01 mm	Not specified	3.3	0
B.Paste	Bottom Solder Paste		0 mm		1	0
B.Silkscreen	Bottom Silk Screen	Not specified	0 mm	Not specified	1	0



File: PI-Power-Board.kicad_pcb

Title:

Size: B KiCad E.D.A. kicad-cli 7.0.10-7.0.10~ubuntu22.04.1 ld: 1/1