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CAN FLEXIBLE DATA-RATE IP CORE

PRODUCT BRIEF

Overview

CAN Flexible Data-Rate IP Core connects functionality of CAN 2.0, CAN FD 1.0 and ISO CAN FD specification in single light-weight IP Core. It is soft-core IP Core written in VHDL with only standard IEEE libraries needed. The main target of usage are FPGA applications and the core is available as RTL. It is optimized for inference of native hardware blocks such as SRAM memories and multipliers in DSP blocks. Generic settings achieve a high level of flexibility before synthesis. It is posible to balance the core between high amount of features and small size.

The IP Core is accessed as memory mapped peripheria via Avalon bus. Easy manipulation with the core is achieved by using hardware buffers for CAN frames. One FIFO like RX buffer is available and two TX buffers are available. Timestamps can be captured for various events on the CAN bus. Additionally transmission of CAN frames can be triggered by external timestamp. Asynchronous access is supported via rich interrupt settings. Three Bit filters and one Range filter is available on received frames.

The design is fully tested at RTL level as well as in real hardware with Altera Cyclone IV FPGA series. The automated test-framework in TCL is available within the core and it provides an easy way of reproducing unit test, feature covering tests and real bus simulation.

Features

- CAN 2.0, CAN FD 1.0 and ISO CAN FD
- RTL VHDL (synthesis), TCL (testing)
- Pre-synthesis configurable features
- Avalon memory bus
- Timestamping and transmission at given time
- Optional event and error logging
- Fault confinement state manipulation
- Transceiver delay measurement
- Size 6 000 - 11 000 LUTs
- 2 000 - 12 000 SRAM memory bits
- Synchronization output with time quantum
- Variety of interrupt sources
- Filtering of received frame
- Listen-only mode, Self-test mode, Acknowledge forbidden mode
- Up to 14 Mbit in “Data” bit-rate (with 100 Mhz Core clock)
- Driver in C available