Summary

Name	Offset	Length	Description
alsaqr_periph_padframe_periphs_config.A_00_CFG	0x0	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_00_MUX_SEL	0x4	4	Pad signal port multiplex selection for pad a_00. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_01_CFG	0x8	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_01_MUX_SEL	0xc	4	Pad signal port multiplex selection for pad a_01. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_02_CFG	0x10	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_02_MUX_SEL	0x14	4	Pad signal port multiplex selection for pad a_02. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_03_CFG	0x18	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_03_MUX_SEL	0x1c	4	Pad signal port multiplex selection for pad a_03. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_04_CFG	0x20	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_04_MUX_SEL	0x24	4	Pad signal port multiplex selection for pad a_04. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_05_CFG	0x28	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_05_MUX_SEL	0x2c	4	Pad signal port multiplex selection for pad a_05. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_06_CFG	0x30	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_06_MUX_SEL	0x34	4	Pad signal port multiplex selection for pad a_06. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_07_CFG	0x38	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_07_MUX_SEL	0x3c	4	Pad signal port multiplex selection for pad a_07. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_08_CFG	0x40	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_08_MUX_SEL	0x44	4	Pad signal port multiplex selection for pad a_08. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_09_CFG	0x48	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_09_MUX_SEL	0x4c	4	Pad signal port multiplex selection for pad a_09. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_10_CFG	0x50	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_10_MUX_SEL	0x54	4	Pad signal port multiplex selection for pad a_10. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_11_CFG	0x58	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_11_MUX_SEL	0x5c	4	Pad signal port multiplex selection for pad a_11. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_12_CFG	0x60	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_12_MUX_SEL	0x64	4	Pad signal port multiplex selection for pad a_12. The programmed value defines which port

Name	Offset	Length	Description
alsaqr_periph_padframe_periphs_config.A_13_CFG	0x68	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_13_MUX_SEL	0x6c	4	Pad signal port multiplex selection for pad a_13. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_14_CFG	0x70	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_14_MUX_SEL	0x74	4	Pad signal port multiplex selection for pad a_14. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_15_CFG	0x78	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_15_MUX_SEL	0x7c	4	Pad signal port multiplex selection for pad a_15. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_16_CFG	0x80	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_16_MUX_SEL	0x84	4	Pad signal port multiplex selection for pad a_16. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_17_CFG	0x88	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_17_MUX_SEL	0x8c	4	Pad signal port multiplex selection for pad a_17. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_18_CFG	0x90	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_18_MUX_SEL	0x94	4	Pad signal port multiplex selection for pad a_18. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_19_CFG	0x98	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_19_MUX_SEL	0x9c	4	Pad signal port multiplex selection for pad a_19. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_20_CFG	0xa0	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_20_MUX_SEL	0xa4	4	Pad signal port multiplex selection for pad a_20. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_21_CFG	0xa8	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_21_MUX_SEL	0xac	4	Pad signal port multiplex selection for pad a_21. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_22_CFG	0xb0	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_22_MUX_SEL	0xb4	4	Pad signal port multiplex selection for pad a_22. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_23_CFG	0xb8	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_23_MUX_SEL	0xbc	4	Pad signal port multiplex selection for pad a_23. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_24_CFG	0xc0	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_24_MUX_SEL	0xc4	4	Pad signal port multiplex selection for pad a_24. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_25_CFG	0xc8	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_25_MUX_SEL	0xcc	4	Pad signal port multiplex selection for pad a_25. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_26_CFG	0xd0	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_26_MUX_SEL	0xd4	4	Pad signal port multiplex selection for pad a_26. The programmed value defines which port

Name	Offset	Length	Description
alsaqr_periph_padframe_periphs_config.A_27_CFG	0xd8	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_27_MUX_SEL	0xdc	4	Pad signal port multiplex selection for pad a_27. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_28_CFG	0xe0	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_28_MUX_SEL	0xe4	4	Pad signal port multiplex selection for pad a_28. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.A_29_CFG	0xe8	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.A_29_MUX_SEL	0xec	4	Pad signal port multiplex selection for pad a_29. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_00_CFG	0xf0	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_00_MUX_SEL	0xf4	4	Pad signal port multiplex selection for pad b_00. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_01_CFG	0xf8	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_01_MUX_SEL	0xfc	4	Pad signal port multiplex selection for pad b_01. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_02_CFG	0x100	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_02_MUX_SEL	0x104	4	Pad signal port multiplex selection for pad b_02. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_03_CFG	0x108	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_03_MUX_SEL	0x10c	4	Pad signal port multiplex selection for pad b_03. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_04_CFG	0x110	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_04_MUX_SEL	0x114	4	Pad signal port multiplex selection for pad b_04. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_05_CFG	0x118	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_05_MUX_SEL	0x11c	4	Pad signal port multiplex selection for pad b_05. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_06_CFG	0x120	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_06_MUX_SEL	0x124	4	Pad signal port multiplex selection for pad b_06. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_07_CFG	0x128	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_07_MUX_SEL	0x12c	4	Pad signal port multiplex selection for pad b_07. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_08_CFG	0x130	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_08_MUX_SEL	0x134	4	Pad signal port multiplex selection for pad b_08. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_09_CFG	0x138	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_09_MUX_SEL	0x13c	4	Pad signal port multiplex selection for pad b_09. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_10_CFG	0x140	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_10_MUX_SEL			Pad signal port multiplex selection for pad b_10. The

Name	Offset	Length	Description
	0x144	4	programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_11_CFG	0x148	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_11_MUX_SEL	0x14c	4	Pad signal port multiplex selection for pad b_11. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_12_CFG	0x150	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_12_MUX_SEL	0x154	4	Pad signal port multiplex selection for pad b_12. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_13_CFG	0x158	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_13_MUX_SEL	0x15c	4	Pad signal port multiplex selection for pad b_13. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_14_CFG	0x160	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_14_MUX_SEL	0x164	4	Pad signal port multiplex selection for pad b_14. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_15_CFG	0x168	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_15_MUX_SEL	0x16c	4	Pad signal port multiplex selection for pad b_15. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_16_CFG	0x170	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_16_MUX_SEL	0x174	4	Pad signal port multiplex selection for pad b_16. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_17_CFG	0x178	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_17_MUX_SEL	0x17c	4	Pad signal port multiplex selection for pad b_17. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_18_CFG	0x180	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_18_MUX_SEL	0x184	4	Pad signal port multiplex selection for pad b_18. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_19_CFG	0x188	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_19_MUX_SEL	0x18c	4	Pad signal port multiplex selection for pad b_19. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_20_CFG	0x190	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_20_MUX_SEL	0x194	4	Pad signal port multiplex selection for pad b_20. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_21_CFG	0x198	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_21_MUX_SEL	0x19c	4	Pad signal port multiplex selection for pad b_21. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_22_CFG	0x1a0	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_22_MUX_SEL	0x1a4	4	Pad signal port multiplex selection for pad b_22. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_23_CFG	0x1a8	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_23_MUX_SEL	0x1ac	4	Pad signal port multiplex selection for pad b_23. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_24_CFG	0x1b0	4	Pad signal configuration.

Name	Offset	Length	Description
alsaqr_periph_padframe_periphs_config.B_24_MUX_SEL	0x1b4	4	Pad signal port multiplex selection for pad b_24. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_25_CFG	0x1b8	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_25_MUX_SEL	0x1bc	4	Pad signal port multiplex selection for pad b_25. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_26_CFG	0x1c0	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_26_MUX_SEL	0x1c4	4	Pad signal port multiplex selection for pad b_26. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_27_CFG	0x1c8	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_27_MUX_SEL	0x1cc	4	Pad signal port multiplex selection for pad b_27. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_28_CFG	0x1d0	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_28_MUX_SEL	0x1d4	4	Pad signal port multiplex selection for pad b_28. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_29_CFG	0x1d8	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_29_MUX_SEL	0x1dc	4	Pad signal port multiplex selection for pad b_29. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_30_CFG	0x1e0	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_30_MUX_SEL	0x1e4	4	Pad signal port multiplex selection for pad b_30. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_31_CFG	0x1e8	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_31_MUX_SEL	0x1ec	4	Pad signal port multiplex selection for pad b_31. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_32_CFG	0x1f0	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_32_MUX_SEL	0x1f4	4	Pad signal port multiplex selection for pad b_32. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_33_CFG	0x1f8	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_33_MUX_SEL	0x1fc	4	Pad signal port multiplex selection for pad b_33. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_34_CFG	0x200	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_34_MUX_SEL	0x204	4	Pad signal port multiplex selection for pad b_34. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_35_CFG	0x208	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_35_MUX_SEL	0x20c	4	Pad signal port multiplex selection for pad b_35. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_36_CFG	0x210	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_36_MUX_SEL	0x214	4	Pad signal port multiplex selection for pad b_36. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_37_CFG	0x218	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_37_MUX_SEL	0x21c	4	Pad signal port multiplex selection for pad b_37. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_38_CFG	0x220	4	Pad signal configuration.

Name	Offset	Length	Description
alsaqr_periph_padframe_periphs_config.B_38_MUX_SEL	0x224	4	Pad signal port multiplex selection for pad b_38. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_39_CFG	0x228	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_39_MUX_SEL	0x22c	4	Pad signal port multiplex selection for pad b_39. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_40_CFG	0x230	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_40_MUX_SEL	0x234	4	Pad signal port multiplex selection for pad b_40. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_41_CFG	0x238	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_41_MUX_SEL	0x23c	4	Pad signal port multiplex selection for pad b_41. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_42_CFG	0x240	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_42_MUX_SEL	0x244	4	Pad signal port multiplex selection for pad b_42. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_43_CFG	0x248	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_43_MUX_SEL	0x24c	4	Pad signal port multiplex selection for pad b_43. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_44_CFG	0x250	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_44_MUX_SEL	0x254	4	Pad signal port multiplex selection for pad b_44. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_45_CFG	0x258	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_45_MUX_SEL	0x25c	4	Pad signal port multiplex selection for pad b_45. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_46_CFG	0x260	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_46_MUX_SEL	0x264	4	Pad signal port multiplex selection for pad b_46. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.B_47_CFG	0x268	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.B_47_MUX_SEL	0x26c	4	Pad signal port multiplex selection for pad b_47. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.OT_SPI_00_CFG	0x270	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.OT_SPI_00_MUX_SEL	0x274	4	Pad signal port multiplex selection for pad ot_spi_00. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.OT_SPI_01_CFG	0x278	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.OT_SPI_01_MUX_SEL	0x27c	4	Pad signal port multiplex selection for pad ot_spi_01. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.OT_SPI_02_CFG	0x280	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.OT_SPI_02_MUX_SEL	0x284	4	Pad signal port multiplex selection for pad ot_spi_02. The programmed value defines which port
alsaqr_periph_padframe_periphs_config.OT_SPI_03_CFG	0x288	4	Pad signal configuration.
alsaqr_periph_padframe_periphs_config.OT_SPI_03_MUX_SEL	0x28c	4	Pad signal port multiplex selection for pad ot_spi_03. The programmed value defines which port

A_00_CFG

Pad signal configuration.

- Offset: `0x0`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_00_MUX_SEL

Pad signal port multiplex selection for pad a_00. The programmed value defines which port is connected to the pad.

- Offset: `0x4`
- Reset default: `0x0`
- Reset mask: `0x3`

Fields


```
{"reg": [{"name": "A_00_MUX_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:2			Reserved
1:0	rw	0x0	A_00_MUX_SEL

A_00_MUX_SEL . A_00_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_can0_can_tx	Connect port can_tx from port group can0 to this pad.
0x2	port_gpio_b_gpio0	Connect port gpio0 from port group gpio_b to this pad.
0x3	port_uart_core_uart_tx	Connect port uart_tx from port group uart_core to this pad.

A_01_CFG

Pad signal configuration.

- Offset: `0x8`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_01_MUX_SEL

Pad signal port multiplex selection for pad a_01. The programmed value defines which port is connected to the pad.

- Offset: `0xc`
- Reset default: `0x0`
- Reset mask: `0x3`

Fields


```
{"reg": [{"name": "A_01_MUX_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:2			Reserved
1:0	rw	0x0	A_01_MUX_SEL

A_01_MUX_SEL . A_01_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_can0_can_rx	Connect port can_rx from port group can0 to this pad.
0x2	port_gpio_b_gpio1	Connect port gpio1 from port group gpio_b to this pad.
0x3	port_uart_core_uart_rx	Connect port uart_rx from port group uart_core to this pad.

A_02_CFG

Pad signal configuration.

- Offset: `0x10`

- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_02_MUX_SEL

Pad signal port multiplex selection for pad a_02. The programmed value defines which port is connected to the pad.

- Offset: `0x14`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_02_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_02_MUX_SEL

A_02_MUX_SEL . A_02_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_can1_can_tx	Connect port can_tx from port group can1 to this pad.
0x2	port_gpio_b_gpio2	Connect port gpio2 from port group gpio_b to this pad.
0x3	port_qspi_linux_qspi_sck	Connect port qspi_sck from port group qspi_linux to this pad.
0x4	port_sdio0_sdio_data0	Connect port sdio_data0 from port group sdio0 to this pad.

Other values are reserved.

A_03_CFG

Pad signal configuration.

- Offset: `0x18`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_03_MUX_SEL

Pad signal port multiplex selection for pad a_03. The programmed value defines which port is connected to the pad.

- Offset: `0x1c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_03_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_03_MUX_SEL

A_03_MUX_SEL . A_03_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_can1_can_rx	Connect port can_rx from port group can1 to this pad.
0x2	port_gpio_b_gpio3	Connect port gpio3 from port group gpio_b to this pad.
0x3	port_qspi_linux_qspi_csn	Connect port qspi_csn from port group qspi_linux to this pad.
0x4	port_sdio0_sdio_data1	Connect port sdio_data1 from port group sdio0 to this pad.

Other values are reserved.

A_04_CFG

Pad signal configuration.

- Offset: `0x20`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_04_MUX_SEL

Pad signal port multiplex selection for pad a_04. The programmed value defines which port is connected to the pad.

- Offset: `0x24`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_04_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_04_MUX_SEL

A_04_MUX_SEL . A_04_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_fll_soc_clk_soc	Connect port clk_soc from port group fll_soc to this pad.
0x2	port_gpio_b_gpio4	Connect port gpio4 from port group gpio_b to this pad.
0x3	port_qspi_linux_qspi_sd0	Connect port qspi_sd0 from port group qspi_linux to this pad.
0x4	port_sdio0_sdio_data2	Connect port sdio_data2 from port group sdio0 to this pad.

Other values are reserved.

A_05_CFG

Pad signal configuration.

- Offset: `0x28`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_05_MUX_SEL

Pad signal port multiplex selection for pad a_05. The programmed value defines which port is connected to the pad.

- Offset: `0x2c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields

{"reg": [{"name": "A_05_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_05_MUX_SEL

A_05_MUX_SEL . A_05_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio5	Connect port gpio5 from port group gpio_b to this pad.
0x2	port_qspi_linux_qspi_sd1	Connect port qspi_sd1 from port group qspi_linux to this pad.
0x3	port_sdio0_sdio_data3	Connect port sdio_data3 from port group sdio0 to this pad.
0x4	port_usart1_uart_tx	Connect port uart_tx from port group usart1 to this pad.

Other values are reserved.

A_06_CFG

Pad signal configuration.

- Offset: `0x30`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_06_MUX_SEL

Pad signal port multiplex selection for pad a_06. The programmed value defines which port is connected to the pad.

- Offset: `0x34`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_06_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_06_MUX_SEL

A_06_MUX_SEL . A_06_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio6	Connect port gpio6 from port group gpio_b to this pad.
0x2	port_qspi_linux_qspi_sd2	Connect port qspi_sd2 from port group qspi_linux to this pad.
0x3	port_sdio0_sdio_clk	Connect port sdio_clk from port group sdio0 to this pad.
0x4	port_usart1_uart_rx	Connect port uart_rx from port group usart1 to this pad.

Other values are reserved.

A_07_CFG

Pad signal configuration.

- Offset: `0x38`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_07_MUX_SEL

Pad signal port multiplex selection for pad a_07. The programmed value defines which port is connected to the pad.

- Offset: `0x3c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_07_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_07_MUX_SEL

A_07_MUX_SEL . A_07_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio7	Connect port gpio7 from port group gpio_b to this pad.
0x2	port_qspi_linux_qspi_sd3	Connect port qspi_sd3 from port group qspi_linux to this pad.
0x3	port_sdio0_sdio_cmd	Connect port sdio_cmd from port group sdio0 to this pad.
0x4	port_usart1_uart_rts	Connect port uart_rts from port group usart1 to this pad.

Other values are reserved.

A_08_CFG

Pad signal configuration.

- Offset: `0x40`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_08_MUX_SEL

Pad signal port multiplex selection for pad a_08. The programmed value defines which port is connected to the pad.

- Offset: `0x44`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_08_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_08_MUX_SEL

A_08_MUX_SEL . A_08_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio8	Connect port gpio8 from port group gpio_b to this pad.
0x2	port_i2c0_i2c_scl	Connect port i2c_scl from port group i2c0 to this pad.
0x3	port_pwm0_pwm0	Connect port pwm0 from port group pwm0 to this pad.
0x4	port_usart1_uart_cts	Connect port uart_cts from port group usart1 to this pad.

Other values are reserved.

A_09_CFG

Pad signal configuration.

- Offset: `0x48`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_09_MUX_SEL

Pad signal port multiplex selection for pad a_09. The programmed value defines which port is connected to the pad.

- Offset: `0x4c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_09_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_09_MUX_SEL

A_09_MUX_SEL . A_09_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio9	Connect port gpio9 from port group gpio_b to this pad.
0x2	port_i2c0_i2c_sda	Connect port i2c_sda from port group i2c0 to this pad.
0x3	port_pwm0_pwm1	Connect port pwm1 from port group pwm0 to this pad.
0x4	port_sdio1_sdio_data0	Connect port sdio_data0 from port group sdio1 to this pad.

Other values are reserved.

A_10_CFG

Pad signal configuration.

- Offset: `0x50`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_10_MUX_SEL

Pad signal port multiplex selection for pad a_10. The programmed value defines which port is connected to the pad.

- Offset: `0x54`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_10_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_10_MUX_SEL

A_10_MUX_SEL . A_10_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio10	Connect port gpio10 from port group gpio_b to this pad.
0x2	port_pwm0_pwm0	Connect port pwm0 from port group pwm0 to this pad.
0x3	port_pwm0_pwm2	Connect port pwm2 from port group pwm0 to this pad.
0x4	port_sdio1_sdio_data1	Connect port sdio_data1 from port group sdio1 to this pad.

Other values are reserved.

A_11_CFG

Pad signal configuration.

- Offset: `0x58`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_11_MUX_SEL

Pad signal port multiplex selection for pad a_11. The programmed value defines which port is connected to the pad.

- Offset: `0x5c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_11_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_11_MUX_SEL

A_11_MUX_SEL . A_11_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio11	Connect port gpio11 from port group gpio_b to this pad.
0x2	port_pwm0_pwm1	Connect port pwm1 from port group pwm0 to this pad.
0x3	port_pwm0_pwm3	Connect port pwm3 from port group pwm0 to this pad.
0x4	port_sdio1_sdio_data2	Connect port sdio_data2 from port group sdio1 to this pad.

Other values are reserved.

A_12_CFG

Pad signal configuration.

- Offset: `0x60`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_12_MUX_SEL

Pad signal port multiplex selection for pad a_12. The programmed value defines which port is connected to the pad.

- Offset: `0x64`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_12_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_12_MUX_SEL

A_12_MUX_SEL . A_12_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio12	Connect port gpio12 from port group gpio_b to this pad.
0x2	port_i2c0_i2c_scl	Connect port i2c_scl from port group i2c0 to this pad.
0x3	port_pwm0_pwm2	Connect port pwm2 from port group pwm0 to this pad.
0x4	port_sdio1_sdio_data3	Connect port sdio_data3 from port group sdio1 to this pad.

Other values are reserved.

A_13_CFG

Pad signal configuration.

- Offset: `0x68`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_13_MUX_SEL

Pad signal port multiplex selection for pad a_13. The programmed value defines which port is connected to the pad.

- Offset: `0x6c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields

{"reg": [{"name": "A_13_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_13_MUX_SEL

A_13_MUX_SEL . A_13_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio13	Connect port gpio13 from port group gpio_b to this pad.
0x2	port_i2c0_i2c_sda	Connect port i2c_sda from port group i2c0 to this pad.
0x3	port_pwm0_pwm3	Connect port pwm3 from port group pwm0 to this pad.
0x4	port_sdio1_sdio_clk	Connect port sdio_clk from port group sdio1 to this pad.

Other values are reserved.

A_14_CFG

Pad signal configuration.

- Offset: `0x70`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_14_MUX_SEL

Pad signal port multiplex selection for pad a_14. The programmed value defines which port is connected to the pad.

- Offset: `0x74`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_14_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_14_MUX_SEL

A_14_MUX_SEL . A_14_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio14	Connect port gpio14 from port group gpio_b to this pad.
0x2	port_sdio1_sdio_cmd	Connect port sdio_cmd from port group sdio1 to this pad.
0x3	port_spi0_spi_sck	Connect port spi_sck from port group spi0 to this pad.
0x4	port_uart2_uart_tx	Connect port uart_tx from port group uart2 to this pad.

Other values are reserved.

A_15_CFG

Pad signal configuration.

- Offset: `0x78`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_15_MUX_SEL

Pad signal port multiplex selection for pad a_15. The programmed value defines which port is connected to the pad.

- Offset: `0x7c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_15_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_15_MUX_SEL

A_15_MUX_SEL . A_15_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_eth_eth_rst	Connect port eth_rst from port group eth to this pad.
0x2	port_gpio_b_gpio15	Connect port gpio15 from port group gpio_b to this pad.
0x3	port_spi0_spi_cs0	Connect port spi_cs0 from port group spi0 to this pad.
0x4	port_uart2_uart_rx	Connect port uart_rx from port group uart2 to this pad.

Other values are reserved.

A_16_CFG

Pad signal configuration.

- Offset: `0x80`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_16_MUX_SEL

Pad signal port multiplex selection for pad a_16. The programmed value defines which port is connected to the pad.

- Offset: `0x84`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_16_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_16_MUX_SEL

A_16_MUX_SEL . A_16_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_eth_eth_rxck	Connect port eth_rxck from port group eth to this pad.
0x2	port_gpio_b_gpio16	Connect port gpio16 from port group gpio_b to this pad.
0x3	port_i2c5_i2c_scl	Connect port i2c_scl from port group i2c5 to this pad.
0x4	port_spi0_spi_miso	Connect port spi_miso from port group spi0 to this pad.

Other values are reserved.

A_17_CFG

Pad signal configuration.

- Offset: `0x88`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_17_MUX_SEL

Pad signal port multiplex selection for pad a_17. The programmed value defines which port is connected to the pad.

- Offset: `0x8c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_17_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_17_MUX_SEL

A_17_MUX_SEL . A_17_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_eth_eth_rxctl	Connect port eth_rxctl from port group eth to this pad.
0x2	port_gpio_b_gpio17	Connect port gpio17 from port group gpio_b to this pad.
0x3	port_i2c5_i2c_sda	Connect port i2c_sda from port group i2c5 to this pad.
0x4	port_spi0_spi_mosi	Connect port spi_mosi from port group spi0 to this pad.

Other values are reserved.

A_18_CFG

Pad signal configuration.

- Offset: `0x90`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_18_MUX_SEL

Pad signal port multiplex selection for pad a_18. The programmed value defines which port is connected to the pad.

- Offset: `0x94`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_18_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_18_MUX_SEL

A_18_MUX_SEL . A_18_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam0_cam_pclk	Connect port cam_pclk from port group cam0 to this pad.
0x2	port_eth_eth_rxd0	Connect port eth_rxd0 from port group eth to this pad.
0x3	port_gpio_b_gpio18	Connect port gpio18 from port group gpio_b to this pad.
0x4	port_spi2_spi_sck	Connect port spi_sck from port group spi2 to this pad.

Other values are reserved.

A_19_CFG

Pad signal configuration.

- Offset: `0x98`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_19_MUX_SEL

Pad signal port multiplex selection for pad a_19. The programmed value defines which port is connected to the pad.

- Offset: `0x9c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_19_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_19_MUX_SEL

A_19_MUX_SEL . A_19_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam0_cam_vsync	Connect port cam_vsync from port group cam0 to this pad.
0x2	port_eth_eth_rxd1	Connect port eth_rxd1 from port group eth to this pad.
0x3	port_gpio_b_gpio19	Connect port gpio19 from port group gpio_b to this pad.
0x4	port_spi2_spi_cs0	Connect port spi_cs0 from port group spi2 to this pad.

Other values are reserved.

A_20_CFG

Pad signal configuration.

- Offset: `0xa0`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_20_MUX_SEL

Pad signal port multiplex selection for pad a_20. The programmed value defines which port is connected to the pad.

- Offset: `0xa4`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_20_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_20_MUX_SEL

A_20_MUX_SEL . A_20_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam0_cam_hsync	Connect port cam_hsync from port group cam0 to this pad.
0x2	port_eth_eth_rxd2	Connect port eth_rxd2 from port group eth to this pad.
0x3	port_gpio_b_gpio20	Connect port gpio20 from port group gpio_b to this pad.
0x4	port_spi2_spi_miso	Connect port spi_miso from port group spi2 to this pad.

Other values are reserved.

A_21_CFG

Pad signal configuration.

- Offset: `0xa8`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_21_MUX_SEL

Pad signal port multiplex selection for pad a_21. The programmed value defines which port is connected to the pad.

- Offset: `0xac`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_21_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_21_MUX_SEL

A_21_MUX_SEL . A_21_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam0_cam_data0_i	Connect port cam_data0_i from port group cam0 to this pad.
0x2	port_eth_eth_rxd3	Connect port eth_rxd3 from port group eth to this pad.
0x3	port_gpio_b_gpio21	Connect port gpio21 from port group gpio_b to this pad.
0x4	port_spi2_spi_mosi	Connect port spi_mosi from port group spi2 to this pad.

Other values are reserved.

A_22_CFG

Pad signal configuration.

- Offset: `0xb0`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_22_MUX_SEL

Pad signal port multiplex selection for pad a_22. The programmed value defines which port is connected to the pad.

- Offset: `0xb4`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_22_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_22_MUX_SEL

A_22_MUX_SEL . A_22_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam0_cam_data1_i	Connect port cam_data1_i from port group cam0 to this pad.
0x2	port_eth_eth_txck	Connect port eth_txck from port group eth to this pad.
0x3	port_gpio_b_gpio22	Connect port gpio22 from port group gpio_b to this pad.
0x4	port_spi3_spi_sck	Connect port spi_sck from port group spi3 to this pad.

Other values are reserved.

A_23_CFG

Pad signal configuration.

- Offset: `0xb8`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_23_MUX_SEL

Pad signal port multiplex selection for pad a_23. The programmed value defines which port is connected to the pad.

- Offset: `0xbc`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_23_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_23_MUX_SEL

A_23_MUX_SEL . A_23_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam0_cam_data2_i	Connect port cam_data2_i from port group cam0 to this pad.
0x2	port_eth_eth_txctl	Connect port eth_txctl from port group eth to this pad.
0x3	port_gpio_b_gpio23	Connect port gpio23 from port group gpio_b to this pad.
0x4	port_spi3_spi_cs0	Connect port spi_cs0 from port group spi3 to this pad.

Other values are reserved.

A_24_CFG

Pad signal configuration.

- Offset: `0xc0`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_24_MUX_SEL

Pad signal port multiplex selection for pad a_24. The programmed value defines which port is connected to the pad.

- Offset: `0xc4`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_24_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_24_MUX_SEL

A_24_MUX_SEL . A_24_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam0_cam_data3_i	Connect port cam_data3_i from port group cam0 to this pad.
0x2	port_eth_eth_txd0	Connect port eth_txd0 from port group eth to this pad.
0x3	port_gpio_b_gpio24	Connect port gpio24 from port group gpio_b to this pad.
0x4	port_spi3_spi_miso	Connect port spi_miso from port group spi3 to this pad.

Other values are reserved.

A_25_CFG

Pad signal configuration.

- Offset: `0xc8`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_25_MUX_SEL

Pad signal port multiplex selection for pad a_25. The programmed value defines which port is connected to the pad.

- Offset: `0xcc`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_25_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_25_MUX_SEL

A_25_MUX_SEL . A_25_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam0_cam_data4_i	Connect port cam_data4_i from port group cam0 to this pad.
0x2	port_eth_eth_txd1	Connect port eth_txd1 from port group eth to this pad.
0x3	port_gpio_b_gpio25	Connect port gpio25 from port group gpio_b to this pad.
0x4	port_spi3_spi_mosi	Connect port spi_mosi from port group spi3 to this pad.

Other values are reserved.

A_26_CFG

Pad signal configuration.

- Offset: `0xd0`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_26_MUX_SEL

Pad signal port multiplex selection for pad a_26. The programmed value defines which port is connected to the pad.

- Offset: `0xd4`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_26_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_26_MUX_SEL

A_26_MUX_SEL . A_26_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam0_cam_data5_i	Connect port cam_data5_i from port group cam0 to this pad.
0x2	port_eth_eth_txd2	Connect port eth_txd2 from port group eth to this pad.
0x3	port_gpio_b_gpio26	Connect port gpio26 from port group gpio_b to this pad.
0x4	port_uart0_uart_tx	Connect port uart_tx from port group uart0 to this pad.

Other values are reserved.

A_27_CFG

Pad signal configuration.

- Offset: `0xd8`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_27_MUX_SEL

Pad signal port multiplex selection for pad a_27. The programmed value defines which port is connected to the pad.

- Offset: `0xdc`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_27_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_27_MUX_SEL

A_27_MUX_SEL . A_27_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam0_cam_data6_i	Connect port cam_data6_i from port group cam0 to this pad.
0x2	port_eth_eth_txd3	Connect port eth_txd3 from port group eth to this pad.
0x3	port_gpio_b_gpio27	Connect port gpio27 from port group gpio_b to this pad.
0x4	port_uart0_uart_rx	Connect port uart_rx from port group uart0 to this pad.

Other values are reserved.

A_28_CFG

Pad signal configuration.

- Offset: `0xe0`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_28_MUX_SEL

Pad signal port multiplex selection for pad a_28. The programmed value defines which port is connected to the pad.

- Offset: `0xe4`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_28_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_28_MUX_SEL

A_28_MUX_SEL . A_28_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam0_cam_data7_i	Connect port cam_data7_i from port group cam0 to this pad.
0x2	port_eth_eth_mdio	Connect port eth_mdio from port group eth to this pad.
0x3	port_gpio_b_gpio28	Connect port gpio28 from port group gpio_b to this pad.
0x4	port_i2c1_i2c_scl	Connect port i2c_scl from port group i2c1 to this pad.

Other values are reserved.

A_29_CFG

Pad signal configuration.

- Offset: `0xe8`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

A_29_MUX_SEL

Pad signal port multiplex selection for pad a_29. The programmed value defines which port is connected to the pad.

- Offset: `0xec`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "A_29_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	A_29_MUX_SEL

A_29_MUX_SEL . A_29_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_eth_eth_mdc	Connect port eth_mdc from port group eth to this pad.
0x2	port_fll_soc_clk_soc	Connect port clk_soc from port group fll_soc to this pad.
0x3	port_gpio_b_gpio29	Connect port gpio29 from port group gpio_b to this pad.

Value	Name	Description
0x4	port_i2c1_i2c_sda	Connect port i2c_sda from port group i2c1 to this pad.

Other values are reserved.

B_00_CFG

Pad signal configuration.

- Offset: `0xf0`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_00_MUX_SEL

Pad signal port multiplex selection for pad b_00. The programmed value defines which port is connected to the pad.

- Offset: `0xf4`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_00_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_00_MUX_SEL

B_00_MUX_SEL . B_00_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio0	Connect port gpio0 from port group gpio_b to this pad.
0x2	port_sdio1_sdio_data0	Connect port sdio_data0 from port group sdio1 to this pad.
0x3	port_uart0_uart_tx	Connect port uart_tx from port group uart0 to this pad.

Value	Name	Description
0x1	port_usart0_uart_tx	Connect port uart_tx from port group usart0 to this pad.

Other values are reserved.

B_01_CFG

Pad signal configuration.

- Offset: `0xf8`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_01_MUX_SEL

Pad signal port multiplex selection for pad b_01. The programmed value defines which port is connected to the pad.

- Offset: `0xfc`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_01_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_01_MUX_SEL

B_01_MUX_SEL . B_01_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio1	Connect port gpio1 from port group gpio_b to this pad.
0x2	port_sdio1_sdio_data1	Connect port sdio_data1 from port group sdio1 to this pad.

Value	Name	Description
0x3	port_uart0_uart_rx	Connect port uart_rx from port group uart0 to this pad.
0x4	port_usart0_uart_rx	Connect port uart_rx from port group usart0 to this pad.

Other values are reserved.

B_02_CFG

Pad signal configuration.

- Offset: `0x100`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_02_MUX_SEL

Pad signal port multiplex selection for pad b_02. The programmed value defines which port is connected to the pad.

- Offset: `0x104`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_02_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_02_MUX_SEL

B_02_MUX_SEL . B_02_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio2	Connect port gpio2 from port group gpio_b to this pad.
0x2	port_i2c1_i2c_scl	Connect port i2c_scl from port group i2c1 to this pad.

Value	Name	Description
0x3	port_sdio1_sdio_data2	Connect port sdio_data2 from port group sdio1 to this pad.
0x4	port_usart0_uart_rts	Connect port uart_rts from port group usart0 to this pad.

Other values are reserved.

B_03_CFG

Pad signal configuration.

- Offset: `0x108`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_03_MUX_SEL

Pad signal port multiplex selection for pad b_03. The programmed value defines which port is connected to the pad.

- Offset: `0x10c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_03_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_03_MUX_SEL

B_03_MUX_SEL . B_03_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio3	Connect port gpio3 from port group gpio_b to this pad.
0x2	port_i2c1_i2c_sda	Connect port i2c_sda from port group i2c1 to this pad.

Value	Name	Description
0x3	port_sdio1_sdio_data3	Connect port sdio_data3 from port group sdio1 to this pad.
0x4	port_usart0_uart_cts	Connect port uart_cts from port group usart0 to this pad.

Other values are reserved.

B_04_CFG

Pad signal configuration.

- Offset: `0x110`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_04_MUX_SEL

Pad signal port multiplex selection for pad b_04. The programmed value defines which port is connected to the pad.

- Offset: `0x114`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_04_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_04_MUX_SEL

B_04_MUX_SEL . B_04_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio4	Connect port gpio4 from port group gpio_b to this pad.

Value	Name	Description
0x2	port_sdio1_sdio_clk	Connect port sdio_clk from port group sdio1 to this pad.
0x3	port_spi4_spi_sck	Connect port spi_sck from port group spi4 to this pad.
0x4	port_spi5_spi_sck	Connect port spi_sck from port group spi5 to this pad.

Other values are reserved.

B_05_CFG

Pad signal configuration.

- Offset: `0x118`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_05_MUX_SEL

Pad signal port multiplex selection for pad b_05. The programmed value defines which port is connected to the pad.

- Offset: `0x11c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_05_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_05_MUX_SEL

B_05_MUX_SEL . B_05_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio5	Connect port gpio5 from port group gpio_b to this pad.

Value	Name	Description
0x2	port_sdio1_sdio_cmd	Connect port sdio_cmd from port group sdio1 to this pad.
0x3	port_spi4_spi_cs0	Connect port spi_cs0 from port group spi4 to this pad.
0x4	port_spi5_spi_cs0	Connect port spi_cs0 from port group spi5 to this pad.

Other values are reserved.

B_06_CFG

Pad signal configuration.

- Offset: `0x120`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_06_MUX_SEL

Pad signal port multiplex selection for pad b_06. The programmed value defines which port is connected to the pad.

- Offset: `0x124`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_06_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_06_MUX_SEL

B_06_MUX_SEL . B_06_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.

Value	Name	Description
0x1	port_gpio_b_gpio6	Connect port gpio6 from port group gpio_b to this pad.
0x2	port_spi0_spi_sck	Connect port spi_sck from port group spi0 to this pad.
0x3	port_spi4_spi_miso	Connect port spi_miso from port group spi4 to this pad.
0x4	port_spi5_spi_miso	Connect port spi_miso from port group spi5 to this pad.

Other values are reserved.

B_07_CFG

Pad signal configuration.

- Offset: `0x128`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_07_MUX_SEL

Pad signal port multiplex selection for pad b_07. The programmed value defines which port is connected to the pad.

- Offset: `0x12c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_07_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_07_MUX_SEL

B_07_MUX_SEL . B_07_MUX_SEL

Value	Name	Description

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio7	Connect port gpio7 from port group gpio_b to this pad.
0x2	port_spi0_spi_cs0	Connect port spi_cs0 from port group spi0 to this pad.
0x3	port_spi4_spi_mosi	Connect port spi_mosi from port group spi4 to this pad.
0x4	port_spi5_spi_mosi	Connect port spi_mosi from port group spi5 to this pad.

Other values are reserved.

B_08_CFG

Pad signal configuration.

- Offset: `0x130`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_08_MUX_SEL

Pad signal port multiplex selection for pad b_08. The programmed value defines which port is connected to the pad.

- Offset: `0x134`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_08_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_08_MUX_SEL

B_08_MUX_SEL . B_08_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio8	Connect port gpio8 from port group gpio_b to this pad.
0x2	port_i2c2_i2c_scl	Connect port i2c_scl from port group i2c2 to this pad.
0x3	port_i2c3_i2c_scl	Connect port i2c_scl from port group i2c3 to this pad.
0x4	port_spi0_spi_miso	Connect port spi_miso from port group spi0 to this pad.

Other values are reserved.

B_09_CFG

Pad signal configuration.

- Offset: `0x138`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_09_MUX_SEL

Pad signal port multiplex selection for pad b_09. The programmed value defines which port is connected to the pad.

- Offset: `0x13c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_09_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_09_MUX_SEL

B_09_MUX_SEL . B_09_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio9	Connect port gpio9 from port group gpio_b to this pad.
0x2	port_i2c2_i2c_sda	Connect port i2c_sda from port group i2c2 to this pad.
0x3	port_i2c3_i2c_sda	Connect port i2c_sda from port group i2c3 to this pad.
0x4	port_spi0_spi_mosi	Connect port spi_mosi from port group spi0 to this pad.

Other values are reserved.

B_10_CFG

Pad signal configuration.

- Offset: `0x140`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_10_MUX_SEL

Pad signal port multiplex selection for pad b_10. The programmed value defines which port is connected to the pad.

- Offset: `0x144`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_10_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_10_MUX_SEL

B_10_MUX_SEL . B_10_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio10	Connect port gpio10 from port group gpio_b to this pad.
0x2	port_spi6_spi_sck	Connect port spi_sck from port group spi6 to this pad.
0x3	port_spi7_spi_sck	Connect port spi_sck from port group spi7 to this pad.
0x4	port_usart0_uart_tx	Connect port uart_tx from port group usart0 to this pad.

Other values are reserved.

B_11_CFG

Pad signal configuration.

- Offset: `0x148`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_11_MUX_SEL

Pad signal port multiplex selection for pad b_11. The programmed value defines which port is connected to the pad.

- Offset: `0x14c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_11_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_11_MUX_SEL

Bits	Type	Reset	Name

B_11_MUX_SEL . B_11_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio11	Connect port gpio11 from port group gpio_b to this pad.
0x2	port_spi6_spi_cs0	Connect port spi_cs0 from port group spi6 to this pad.
0x3	port_spi7_spi_miso	Connect port spi_miso from port group spi7 to this pad.
0x4	port_usart0_uart_rx	Connect port uart_rx from port group usart0 to this pad.

Other values are reserved.

B_12_CFG

Pad signal configuration.

- Offset: `0x150`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_12_MUX_SEL

Pad signal port multiplex selection for pad b_12. The programmed value defines which port is connected to the pad.

- Offset: `0x154`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_12_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name

Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_12_MUX_SEL

B_12_MUX_SEL . B_12_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio12	Connect port gpio12 from port group gpio_b to this pad.
0x2	port_spi6_spi_miso	Connect port spi_miso from port group spi6 to this pad.
0x3	port_spi7_spi_mosi	Connect port spi_mosi from port group spi7 to this pad.
0x4	port_usart0_uart_rts	Connect port uart_rts from port group usart0 to this pad.

Other values are reserved.

B_13_CFG

Pad signal configuration.

- Offset: `0x158`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_13_MUX_SEL

Pad signal port multiplex selection for pad b_13. The programmed value defines which port is connected to the pad.

- Offset: `0x15c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_13_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```

Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_13_MUX_SEL

B_13_MUX_SEL . B_13_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio13	Connect port gpio13 from port group gpio_b to this pad.
0x2	port_spi6_spi_mosi	Connect port spi_mosi from port group spi6 to this pad.
0x3	port_spi7_spi_cs0	Connect port spi_cs0 from port group spi7 to this pad.
0x4	port_usart0_uart_cts	Connect port uart_cts from port group usart0 to this pad.

Other values are reserved.

B_14_CFG

Pad signal configuration.

- Offset: `0x160`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_14_MUX_SEL

Pad signal port multiplex selection for pad b_14. The programmed value defines which port is connected to the pad.

- Offset: `0x164`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields

{"reg": [{"name": "B_14_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_14_MUX_SEL

B_14_MUX_SEL . B_14_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio14	Connect port gpio14 from port group gpio_b to this pad.
0x2	port_spi4_spi_sck	Connect port spi_sck from port group spi4 to this pad.
0x3	port_spi7_spi_cs1	Connect port spi_cs1 from port group spi7 to this pad.
0x4	port_usart2_uart_tx	Connect port uart_tx from port group usart2 to this pad.

Other values are reserved.

B_15_CFG

Pad signal configuration.

- Offset: `0x168`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_15_MUX_SEL

Pad signal port multiplex selection for pad b_15. The programmed value defines which port is connected to the pad.

- Offset: `0x16c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields

{"reg": [{"name": "B_15_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_15_MUX_SEL

B_15_MUX_SEL . B_15_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio15	Connect port gpio15 from port group gpio_b to this pad.
0x2	port_i2c4_i2c_scl	Connect port i2c_scl from port group i2c4 to this pad.
0x3	port_spi4_spi_cs0	Connect port spi_cs0 from port group spi4 to this pad.
0x4	port_usart2_uart_rx	Connect port uart_rx from port group usart2 to this pad.

Other values are reserved.

B_16_CFG

Pad signal configuration.

- Offset: `0x170`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_16_MUX_SEL

Pad signal port multiplex selection for pad b_16. The programmed value defines which port is connected to the pad.

- Offset: `0x174`
- Reset default: `0x0`

- Reset mask: `0x7`

Fields

{"reg": [{"name": "B_16_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_16_MUX_SEL

B_16_MUX_SEL . B_16_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio16	Connect port gpio16 from port group gpio_b to this pad.
0x2	port_i2c4_i2c_sda	Connect port i2c_sda from port group i2c4 to this pad.
0x3	port_spi4_spi_miso	Connect port spi_miso from port group spi4 to this pad.
0x4	port_usart2_uart_rts	Connect port uart_rts from port group usart2 to this pad.

Other values are reserved.

B_17_CFG

Pad signal configuration.

- Offset: `0x178`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_17_MUX_SEL

Pad signal port multiplex selection for pad b_17. The programmed value defines which port is connected to the pad.

- Offset: `0x17c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_17_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_17_MUX_SEL

B_17_MUX_SEL . B_17_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio17	Connect port gpio17 from port group gpio_b to this pad.
0x2	port_spi4_spi_mosi	Connect port spi_mosi from port group spi4 to this pad.
0x3	port_uart1_uart_tx	Connect port uart_tx from port group uart1 to this pad.
0x4	port_usart2_uart_cts	Connect port uart_cts from port group usart2 to this pad.

Other values are reserved.

B_18_CFG

Pad signal configuration.

- Offset: `0x180`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_18_MUX_SEL

Pad signal port multiplex selection for pad b_18. The programmed value defines which port is connected to the pad.

- Offset: `0x184`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields

{"reg": [{"name": "B_18_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_18_MUX_SEL

B_18_MUX_SEL . B_18_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio18	Connect port gpio18 from port group gpio_b to this pad.
0x2	port_spi2_spi_sck	Connect port spi_sck from port group spi2 to this pad.
0x3	port_uart1_uart_rx	Connect port uart_rx from port group uart1 to this pad.
0x4	port_usart3_uart_tx	Connect port uart_tx from port group usart3 to this pad.

Other values are reserved.

B_19_CFG

Pad signal configuration.

- Offset: `0x188`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_19_MUX_SEL

Pad signal port multiplex selection for pad b_19. The programmed value defines which port is connected to the pad.

- Offset: `0x18c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_19_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_19_MUX_SEL

B_19_MUX_SEL . B_19_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio19	Connect port gpio19 from port group gpio_b to this pad.
0x2	port_spi2_spi_cs0	Connect port spi_cs0 from port group spi2 to this pad.
0x3	port_usart1_uart_tx	Connect port uart_tx from port group usart1 to this pad.
0x4	port_usart3_uart_rx	Connect port uart_rx from port group usart3 to this pad.

Other values are reserved.

B_20_CFG

Pad signal configuration.

- Offset: `0x190`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_20_MUX_SEL

Pad signal port multiplex selection for pad b_20. The programmed value defines which port is connected to the pad.

- Offset: `0x194`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_20_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_20_MUX_SEL

B_20_MUX_SEL . B_20_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio20	Connect port gpio20 from port group gpio_b to this pad.
0x2	port_spi2_spi_miso	Connect port spi_miso from port group spi2 to this pad.
0x3	port_usart1_uart_rx	Connect port uart_rx from port group usart1 to this pad.
0x4	port_usart3_uart_rts	Connect port uart_rts from port group usart3 to this pad.

Other values are reserved.

B_21_CFG

Pad signal configuration.

- Offset: `0x198`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX

Bits	Type	Reset	Name	driver Description

B_21_MUX_SEL

Pad signal port multiplex selection for pad b_21. The programmed value defines which port is connected to the pad.

- Offset: `0x19c`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_21_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_21_MUX_SEL

B_21_MUX_SEL . B_21_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio21	Connect port gpio21 from port group gpio_b to this pad.
0x2	port_spi2_spi_mosi	Connect port spi_mosi from port group spi2 to this pad.
0x3	port_usart1_uart_rts	Connect port uart_rts from port group usart1 to this pad.
0x4	port_usart3_uart_cts	Connect port uart_cts from port group usart3 to this pad.

Other values are reserved.

B_22_CFG

Pad signal configuration.

- Offset: `0x1a0`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength

Bits	Type	Reset	Name	Description
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_22_MUX_SEL

Pad signal port multiplex selection for pad b_22. The programmed value defines which port is connected to the pad.

- Offset: `0x1a4`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_22_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_22_MUX_SEL

B_22_MUX_SEL . B_22_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_gpio_b_gpio22	Connect port gpio22 from port group gpio_b to this pad.
0x2	port_spi3_spi_sck	Connect port spi_sck from port group spi3 to this pad.
0x3	port_spi8_spi_sck	Connect port spi_sck from port group spi8 to this pad.
0x4	port_usart1_uart_cts	Connect port uart_cts from port group usart1 to this pad.

Other values are reserved.

B_23_CFG

Pad signal configuration.

- Offset: `0x1a8`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low

Bits	Type	Reset	Name	Description
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_23_MUX_SEL

Pad signal port multiplex selection for pad b_23. The programmed value defines which port is connected to the pad.

- Offset: `0x1ac`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_23_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_23_MUX_SEL

B_23_MUX_SEL . B_23_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_eth_eth_rst	Connect port eth_rst from port group eth to this pad.
0x2	port_gpio_b_gpio23	Connect port gpio23 from port group gpio_b to this pad.
0x3	port_spi3_spi_cs0	Connect port spi_cs0 from port group spi3 to this pad.
0x4	port_spi8_spi_cs0	Connect port spi_cs0 from port group spi8 to this pad.

Other values are reserved.

B_24_CFG

Pad signal configuration.

- Offset: `0x1b0`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low

Bits	Type	Reset	Name	Description
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_24_MUX_SEL

Pad signal port multiplex selection for pad b_24. The programmed value defines which port is connected to the pad.

- Offset: `0x1b4`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_24_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_24_MUX_SEL

B_24_MUX_SEL . B_24_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_eth_eth_rxck	Connect port eth_rxck from port group eth to this pad.
0x2	port_gpio_b_gpio24	Connect port gpio24 from port group gpio_b to this pad.
0x3	port_spi3_spi_miso	Connect port spi_miso from port group spi3 to this pad.
0x4	port_spi8_spi_miso	Connect port spi_miso from port group spi8 to this pad.

Other values are reserved.

B_25_CFG

Pad signal configuration.

- Offset: `0x1b8`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low

Bits	Type	Reset	Name	Description
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_25_MUX_SEL

Pad signal port multiplex selection for pad b_25. The programmed value defines which port is connected to the pad.

- Offset: `0x1bc`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_25_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_25_MUX_SEL

B_25_MUX_SEL . B_25_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_eth_eth_rxctl	Connect port eth_rxctl from port group eth to this pad.
0x2	port_gpio_b_gpio25	Connect port gpio25 from port group gpio_b to this pad.
0x3	port_spi3_spi_mosi	Connect port spi_mosi from port group spi3 to this pad.
0x4	port_spi8_spi_mosi	Connect port spi_mosi from port group spi8 to this pad.

Other values are reserved.

B_26_CFG

Pad signal configuration.

- Offset: `0x1c0`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable

Bits	Type	Reset	Name	Description
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_26_MUX_SEL

Pad signal port multiplex selection for pad b_26. The programmed value defines which port is connected to the pad.

- Offset: `0x1c4`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_26_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_26_MUX_SEL

B_26_MUX_SEL . B_26_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_eth_eth_rxd0	Connect port eth_rxd0 from port group eth to this pad.
0x2	port_gpio_b_gpio26	Connect port gpio26 from port group gpio_b to this pad.
0x3	port_spi1_spi_sck	Connect port spi_sck from port group spi1 to this pad.
0x4	port_spi9_spi_sck	Connect port spi_sck from port group spi9 to this pad.

Other values are reserved.

B_27_CFG

Pad signal configuration.

- Offset: `0x1c8`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable

Bits	Type	Reset	Name	Description
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_27_MUX_SEL

Pad signal port multiplex selection for pad b_27. The programmed value defines which port is connected to the pad.

- Offset: `0x1cc`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_27_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_27_MUX_SEL

B_27_MUX_SEL . B_27_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_eth_eth_rxd1	Connect port eth_rxd1 from port group eth to this pad.
0x2	port_gpio_b_gpio27	Connect port gpio27 from port group gpio_b to this pad.
0x3	port_spi1_spi_cs0	Connect port spi_cs0 from port group spi1 to this pad.
0x4	port_spi9_spi_cs0	Connect port spi_cs0 from port group spi9 to this pad.

Other values are reserved.

B_28_CFG

Pad signal configuration.

- Offset: `0x1d0`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved

Bits	Type	Reset	Name	Description
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_28_MUX_SEL

Pad signal port multiplex selection for pad b_28. The programmed value defines which port is connected to the pad.

- Offset: `0x1d4`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_28_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_28_MUX_SEL

B_28_MUX_SEL . B_28_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_eth_eth_rxd2	Connect port eth_rxd2 from port group eth to this pad.
0x2	port_gpio_b_gpio28	Connect port gpio28 from port group gpio_b to this pad.
0x3	port_spi1_spi_miso	Connect port spi_miso from port group spi1 to this pad.
0x4	port_spi9_spi_miso	Connect port spi_miso from port group spi9 to this pad.

Other values are reserved.

B_29_CFG

Pad signal configuration.

- Offset: `0x1d8`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_29_MUX_SEL

Pad signal port multiplex selection for pad b_29. The programmed value defines which port is connected to the pad.

- Offset: `0x1dc`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_29_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_29_MUX_SEL

B_29_MUX_SEL . B_29_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_eth_eth_rxd3	Connect port eth_rxd3 from port group eth to this pad.
0x2	port_gpio_b_gpio29	Connect port gpio29 from port group gpio_b to this pad.
0x3	port_spi1_spi_mosi	Connect port spi_mosi from port group spi1 to this pad.
0x4	port_spi9_spi_mosi	Connect port spi_mosi from port group spi9 to this pad.

Other values are reserved.

B_30_CFG

Pad signal configuration.

- Offset: `0x1e0`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_30_MUX_SEL

Pad signal port multiplex selection for pad b_30. The programmed value defines which port is connected to the pad.

- Offset: `0x1e4`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields


```
{"reg": [{"name": "B_30_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '
```


Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_30_MUX_SEL

B_30_MUX_SEL . B_30_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_can1_can_tx	Connect port can_tx from port group can1 to this pad.
0x2	port_eth_eth_txck	Connect port eth_txck from port group eth to this pad.
0x3	port_gpio_b_gpio30	Connect port gpio30 from port group gpio_b to this pad.
0x4	port_spi10_spi_sck	Connect port spi_sck from port group spi10 to this pad.

Other values are reserved.

B_31_CFG

Pad signal configuration.

- Offset: `0x1e8`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_31_MUX_SEL

Pad signal port multiplex selection for pad b_31. The programmed value defines which port is connected to the pad.

- Offset: `0x1ec`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields

{"reg": [{"name": "B_31_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_31_MUX_SEL

B_31_MUX_SEL . B_31_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_can1_can_rx	Connect port can_rx from port group can1 to this pad.
0x2	port_eth_eth_txctl	Connect port eth_txctl from port group eth to this pad.
0x3	port_gpio_b_gpio31	Connect port gpio31 from port group gpio_b to this pad.
0x4	port_spi10_spi_cs0	Connect port spi_cs0 from port group spi10 to this pad.

Other values are reserved.

B_32_CFG

Pad signal configuration.

- Offset: `0x1f0`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_32_MUX_SEL

Pad signal port multiplex selection for pad b_32. The programmed value defines which port is connected to the pad.

- Offset: `0x1f4`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields

{"reg": [{"name": "B_32_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_32_MUX_SEL

B_32_MUX_SEL . B_32_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_eth_eth_txd0	Connect port eth_txd0 from port group eth to this pad.
0x2	port_gpio_b_gpio32	Connect port gpio32 from port group gpio_b to this pad.
0x3	port_pwm1_pwm0	Connect port pwm0 from port group pwm1 to this pad.
0x4	port_spi10_spi_miso	Connect port spi_miso from port group spi10 to this pad.

Other values are reserved.

B_33_CFG

Pad signal configuration.

- Offset: `0x1f8`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_33_MUX_SEL

Pad signal port multiplex selection for pad b_33. The programmed value defines which port is connected to the pad.

- Offset: `0x1fc`
- Reset default: `0x0`
- Reset mask: `0x7`

Fields

{"reg": [{"name": "B_33_MUX_SEL", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:3			Reserved
2:0	rw	0x0	B_33_MUX_SEL

B_33_MUX_SEL . B_33_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_eth_eth_txd1	Connect port eth_txd1 from port group eth to this pad.
0x2	port_gpio_b_gpio33	Connect port gpio33 from port group gpio_b to this pad.
0x3	port_pwm1_pwm1	Connect port pwm1 from port group pwm1 to this pad.
0x4	port_spi10_spi_mosi	Connect port spi_mosi from port group spi10 to this pad.

Other values are reserved.

B_34_CFG

Pad signal configuration.

- Offset: `0x200`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_34_MUX_SEL

Pad signal port multiplex selection for pad b_34. The programmed value defines which port is connected to the pad.

- Offset: `0x204`
- Reset default: `0x0`
- Reset mask: `0x3`

Fields

{"reg": [{"name": "B_34_MUX_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:2			Reserved
1:0	rw	0x0	B_34_MUX_SEL

B_34_MUX_SEL . B_34_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_eth_eth_txd2	Connect port eth_txd2 from port group eth to this pad.
0x2	port_gpio_b_gpio34	Connect port gpio34 from port group gpio_b to this pad.
0x3	port_pwm1_pwm2	Connect port pwm2 from port group pwm1 to this pad.

B_35_CFG

Pad signal configuration.

- Offset: `0x208`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_35_MUX_SEL

Pad signal port multiplex selection for pad b_35. The programmed value defines which port is connected to the pad.

- Offset: `0x20c`
- Reset default: `0x0`
- Reset mask: `0x3`

Fields

{"reg": [{"name": "B_35_MUX_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:2			Reserved
1:0	rw	0x0	B_35_MUX_SEL

B_35_MUX_SEL . B_35_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_eth_eth_txd3	Connect port eth_txd3 from port group eth to this pad.
0x2	port_gpio_b_gpio35	Connect port gpio35 from port group gpio_b to this pad.
0x3	port_pwm1_pwm3	Connect port pwm3 from port group pwm1 to this pad.

B_36_CFG

Pad signal configuration.

- Offset: `0x210`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_36_MUX_SEL

Pad signal port multiplex selection for pad b_36. The programmed value defines which port is connected to the pad.

- Offset: `0x214`
- Reset default: `0x0`
- Reset mask: `0x3`

Fields

{"reg": [{"name": "B_36_MUX_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:2			Reserved
1:0	rw	0x0	B_36_MUX_SEL

B_36_MUX_SEL . B_36_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam1_cam_pclk	Connect port cam_pclk from port group cam1 to this pad.
0x2	port_eth_eth_mdio	Connect port eth_mdio from port group eth to this pad.
0x3	port_gpio_b_gpio36	Connect port gpio36 from port group gpio_b to this pad.

B_37_CFG

Pad signal configuration.

- Offset: `0x218`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_37_MUX_SEL

Pad signal port multiplex selection for pad b_37. The programmed value defines which port is connected to the pad.

- Offset: `0x21c`
- Reset default: `0x0`
- Reset mask: `0x3`

Fields

{"reg": [{"name": "B_37_MUX_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:2			Reserved
1:0	rw	0x0	B_37_MUX_SEL

B_37_MUX_SEL . B_37_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam1_cam_vsync	Connect port cam_vsync from port group cam1 to this pad.
0x2	port_eth_eth_mdc	Connect port eth_mdc from port group eth to this pad.
0x3	port_gpio_b_gpio37	Connect port gpio37 from port group gpio_b to this pad.

B_38_CFG

Pad signal configuration.

- Offset: `0x220`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_38_MUX_SEL

Pad signal port multiplex selection for pad b_38. The programmed value defines which port is connected to the pad.

- Offset: `0x224`
- Reset default: `0x0`
- Reset mask: `0x3`

Fields

{"reg": [{"name": "B_38_MUX_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:2			Reserved
1:0	rw	0x0	B_38_MUX_SEL

B_38_MUX_SEL . B_38_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam1_cam_hsync	Connect port cam_hsync from port group cam1 to this pad.
0x2	port_gpio_b_gpio38	Connect port gpio38 from port group gpio_b to this pad.
0x3	port_spi10_spi_sck	Connect port spi_sck from port group spi10 to this pad.

B_39_CFG

Pad signal configuration.

- Offset: `0x228`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_39_MUX_SEL

Pad signal port multiplex selection for pad b_39. The programmed value defines which port is connected to the pad.

- Offset: `0x22c`
- Reset default: `0x0`
- Reset mask: `0x3`

Fields

{"reg": [{"name": "B_39_MUX_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:2			Reserved
1:0	rw	0x0	B_39_MUX_SEL

B_39_MUX_SEL . B_39_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam1_cam_data0_i	Connect port cam_data0_i from port group cam1 to this pad.
0x2	port_gpio_b_gpio39	Connect port gpio39 from port group gpio_b to this pad.
0x3	port_spi10_spi_cs0	Connect port spi_cs0 from port group spi10 to this pad.

B_40_CFG

Pad signal configuration.

- Offset: `0x230`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_40_MUX_SEL

Pad signal port multiplex selection for pad b_40. The programmed value defines which port is connected to the pad.

- Offset: `0x234`
- Reset default: `0x0`
- Reset mask: `0x3`

Fields

{"reg": [{"name": "B_40_MUX_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:2			Reserved
1:0	rw	0x0	B_40_MUX_SEL

B_40_MUX_SEL . B_40_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam1_cam_data1_i	Connect port cam_data1_i from port group cam1 to this pad.
0x2	port_gpio_b_gpio40	Connect port gpio40 from port group gpio_b to this pad.
0x3	port_spi10_spi_miso	Connect port spi_miso from port group spi10 to this pad.

B_41_CFG

Pad signal configuration.

- Offset: `0x238`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_41_MUX_SEL

Pad signal port multiplex selection for pad b_41. The programmed value defines which port is connected to the pad.

- Offset: `0x23c`
- Reset default: `0x0`
- Reset mask: `0x3`

Fields

{"reg": [{"name": "B_41_MUX_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:2			Reserved
1:0	rw	0x0	B_41_MUX_SEL

B_41_MUX_SEL . B_41_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam1_cam_data2_i	Connect port cam_data2_i from port group cam1 to this pad.
0x2	port_gpio_b_gpio41	Connect port gpio41 from port group gpio_b to this pad.
0x3	port_spi10_spi_mosi	Connect port spi_mosi from port group spi10 to this pad.

B_42_CFG

Pad signal configuration.

- Offset: `0x240`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_42_MUX_SEL

Pad signal port multiplex selection for pad b_42. The programmed value defines which port is connected to the pad.

- Offset: `0x244`
- Reset default: `0x0`
- Reset mask: `0x3`

Fields

{"reg": [{"name": "B_42_MUX_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:2			Reserved
1:0	rw	0x0	B_42_MUX_SEL

B_42_MUX_SEL . B_42_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam1_cam_data3_i	Connect port cam_data3_i from port group cam1 to this pad.
0x2	port_can0_can_tx	Connect port can_tx from port group can0 to this pad.
0x3	port_gpio_b_gpio42	Connect port gpio42 from port group gpio_b to this pad.

B_43_CFG

Pad signal configuration.

- Offset: `0x248`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_43_MUX_SEL

Pad signal port multiplex selection for pad b_43. The programmed value defines which port is connected to the pad.

- Offset: `0x24c`
- Reset default: `0x0`
- Reset mask: `0x3`

Fields

{"reg": [{"name": "B_43_MUX_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:2			Reserved
1:0	rw	0x0	B_43_MUX_SEL

B_43_MUX_SEL . B_43_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam1_cam_data4_i	Connect port cam_data4_i from port group cam1 to this pad.
0x2	port_can0_can_rx	Connect port can_rx from port group can0 to this pad.
0x3	port_gpio_b_gpio43	Connect port gpio43 from port group gpio_b to this pad.

B_44_CFG

Pad signal configuration.

- Offset: `0x250`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_44_MUX_SEL

Pad signal port multiplex selection for pad b_44. The programmed value defines which port is connected to the pad.

- Offset: `0x254`
- Reset default: `0x0`
- Reset mask: `0x3`

Fields

{"reg": [{"name": "B_44_MUX_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:2			Reserved
1:0	rw	0x0	B_44_MUX_SEL

B_44_MUX_SEL . B_44_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam1_cam_data5_i	Connect port cam_data5_i from port group cam1 to this pad.
0x2	port_gpio_b_gpio44	Connect port gpio44 from port group gpio_b to this pad.
0x3	port_pwm1_pwm0	Connect port pwm0 from port group pwm1 to this pad.

B_45_CFG

Pad signal configuration.

- Offset: `0x258`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_45_MUX_SEL

Pad signal port multiplex selection for pad b_45. The programmed value defines which port is connected to the pad.

- Offset: `0x25c`
- Reset default: `0x0`
- Reset mask: `0x3`

Fields

{"reg": [{"name": "B_45_MUX_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:2			Reserved
1:0	rw	0x0	B_45_MUX_SEL

B_45_MUX_SEL . B_45_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam1_cam_data6_i	Connect port cam_data6_i from port group cam1 to this pad.
0x2	port_gpio_b_gpio45	Connect port gpio45 from port group gpio_b to this pad.
0x3	port_pwm1_pwm1	Connect port pwm1 from port group pwm1 to this pad.

B_46_CFG

Pad signal configuration.

- Offset: `0x260`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_46_MUX_SEL

Pad signal port multiplex selection for pad b_46. The programmed value defines which port is connected to the pad.

- Offset: `0x264`
- Reset default: `0x0`
- Reset mask: `0x3`

Fields

{"reg": [{"name": "B_46_MUX_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:2			Reserved
1:0	rw	0x0	B_46_MUX_SEL

B_46_MUX_SEL . B_46_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_cam1_cam_data7_i	Connect port cam_data7_i from port group cam1 to this pad.
0x2	port_gpio_b_gpio46	Connect port gpio46 from port group gpio_b to this pad.
0x3	port_pwm1_pwm2	Connect port pwm2 from port group pwm1 to this pad.

B_47_CFG

Pad signal configuration.

- Offset: `0x268`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

B_47_MUX_SEL

Pad signal port multiplex selection for pad b_47. The programmed value defines which port is connected to the pad.

- Offset: `0x26c`
- Reset default: `0x0`
- Reset mask: `0x3`

Fields

{"reg": [{"name": "B_47_MUX_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "config": {"lanes": 1, "fontsize": 10, '

Bits	Type	Reset	Name
31:2			Reserved
1:0	rw	0x0	B_47_MUX_SEL

B_47_MUX_SEL . B_47_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_fll_cva6_clk_cva6	Connect port clk_cva6 from port group fll_cva6 to this pad.
0x2	port_gpio_b_gpio47	Connect port gpio47 from port group gpio_b to this pad.
0x3	port_pwm1_pwm3	Connect port pwm3 from port group pwm1 to this pad.

OT_SPI_00_CFG

Pad signal configuration.

- Offset: `0x270`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

OT_SPI_00_MUX_SEL

Pad signal port multiplex selection for pad ot_spi_00. The programmed value defines which port is connected to the pad.

- Offset: `0x274`
- Reset default: `0x0`
- Reset mask: `0x1`

Fields

{"reg": [{"name": "OT_SPI_00_MUX_SEL", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "config": {"lanes": 1, "fontsize":

Bits	Type	Reset	Name
31:1			Reserved
0	rw	0x0	OT_SPI_00_MUX_SEL

OT_SPI_00_MUX_SEL . OT_SPI_00_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_spi_ot_spi_sck	Connect port spi_sck from port group spi_ot to this pad.

OT_SPI_01_CFG

Pad signal configuration.

- Offset: `0x278`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields

{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},

Bits	Type	Reset	Name	Description

Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

OT_SPI_01_MUX_SEL

Pad signal port multiplex selection for pad ot_spi_01. The programmed value defines which port is connected to the pad.

- Offset: `0x27c`
- Reset default: `0x0`
- Reset mask: `0x1`

Fields


```
{"reg": [{"name": "OT_SPI_01_MUX_SEL", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "config": {"lanes": 1, "fontsize":
```


Bits	Type	Reset	Name
31:1			Reserved
0	rw	0x0	OT_SPI_01_MUX_SEL

OT_SPI_01_MUX_SEL . OT_SPI_01_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_spi_ot_spi_csn	Connect port spi_csn from port group spi_ot to this pad.

OT_SPI_02_CFG

Pad signal configuration.

- Offset: `0x280`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	

Bits	Type	Reset	Name	Description
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

OT_SPI_02_MUX_SEL

Pad signal port multiplex selection for pad ot_spi_02. The programmed value defines which port is connected to the pad.

- Offset: `0x284`
- Reset default: `0x0`
- Reset mask: `0x1`

Fields


```
{"reg": [{"name": "OT_SPI_02_MUX_SEL", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "config": {"lanes": 1, "fontsize":
```


Bits	Type	Reset	Name
31:1			Reserved
0	rw	0x0	OT_SPI_02_MUX_SEL

OT_SPI_02_MUX_SEL . OT_SPI_02_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_spi_ot_spi_sd0	Connect port spi_sd0 from port group spi_ot to this pad.

OT_SPI_03_CFG

Pad signal configuration.

- Offset: `0x288`
- Reset default: `0x18`
- Reset mask: `0x7f`

Fields


```
{"reg": [{"name": "chip2pad", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "drv", "bits": 2, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:7				Reserved
6	rw	0x0	smt	Schmit trigger enable
5	rw	0x0	slw	
4	rw	0x1	puen	Pull-Up enable signal, active low
3	rw	0x1	oen	Output enable signal, active low
2:1	rw	0x0	drv	Driving strength

Bits	Type	Reset	Name	Description
0	rw	0x0	chip2pad	The signal that connects to the pads TX driver

OT_SPI_03_MUX_SEL

Pad signal port multiplex selection for pad ot_spi_03. The programmed value defines which port is connected to the pad.

- Offset: `0x28c`
- Reset default: `0x0`
- Reset mask: `0x1`

Fields


```
{"reg": [{"name": "OT_SPI_03_MUX_SEL", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "config": {"lanes": 1, "fontsize":
```


Bits	Type	Reset	Name
31:1			Reserved
0	rw	0x0	OT_SPI_03_MUX_SEL

OT_SPI_03_MUX_SEL . OT_SPI_03_MUX_SEL

Value	Name	Description
0x0	register	Connects the Pad to the internal configuration register.
0x1	port_spi_ot_spi_sd1	Connect port spi_sd1 from port group spi_ot to this pad.