

# READ ME for I3C Free license Slave HDL Software (RTL)

To go with Free licensed sources from NXP

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## Revision history

| Revision | Date     | Description                                    | Author |
|----------|----------|--|--------|
| 1.0      | 10/17/16 | Updated to free license form from BSD license. | NXP    |

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## 1. Introduction

This free licensed distribution contains a Verilog implementation of a MIPI® I3C™ Slave, implementing all required and a set of optional features.

This distribution does not come with the MIPI I3C specification nor any details copied from it. If you are not a member of the MIPI Alliance, and you wish to use I3C, you are strongly encouraged to join MIPI Alliance.

Please see <http://mipi.org/join-mipi>

The I3C specification is available to all MIPI members, as are all other MIPI specifications, including ones using I3C for advanced functionality (e.g. Touch interfaces).

If joining the MIPI Alliance as an Adopter is not possible/feasible for you and your company/organization, MIPI Alliance can be contacted via <http://mipi.org/contact-mipi>, where you can express your interest, ask questions, and/or provide feedback.

### 1.1 License Details

The HDL software (RTL) is provided with a free license, but not an “open source” license due to the requirements of confidentiality from MIPI.org. You must agree to the confidentiality terms if you are not a MIPI member; if you are a MIPI member, then you have already agreed to this as part of your membership with MIPI.

You must read and agree to the NXP free license. Which license depends on your relationship to MIPI Alliance (ie. <http://mipi.org>).

If you are a MIPI member, then:

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If you are unsure, then check the list in: <http://mipi.org/member-directory>

You may join MIPI Alliance by going to: <http://mipi.org/join-mipi>

### 1.2 License rights

The free license allows you to use and optionally modify the HDL software (RTL) without providing it back. You may not openly distribute it or publish it in source form, modified or not, due to issues of confidentiality. If any sources are modified, the original copyright notice and license notice must be preserved.

The sources may be compiled into forms such as for simulation, FPGA, or Silicon chip. Those forms may be distributed in normal ways, as they do not risk confidentiality issues.

### 1.3 Building for FPGA, Simulation, or Silicon

To use this IP, there are 3 documents provided:

- i3c\_peripheral\_slave\_uarch.pdf, which is the micro-architectural spec, covering the parameters for configuration, clocking and reset, CDC handling, ports, and layers.
- i3c\_programmers\_model.pdf, which covers the APB Memory Mapped register interface.
- i3c\_autonomous\_slave.pdf, which is for non-processor uses; this provides built-in registers to support natural use in combination with a device state machine (e.g. sensor event collection mechanism).

Note that not all features are available in the free version.

### 1.4 Use of more advanced features and Master

The free licensed sources allow for the most common uses of a MIPI I3C Slave. This may be sufficient for your uses, including for experimentation, evaluation, FPGA projects, etc. It is possible to purchase support or full commercial versions from Silvaco: <http://www.silvaco.com/products/IP/i3c.html>

This includes 2 basic options:

1. Purchase of commercial support of the free version. A so-called ‘Freemium’ license.
2. Purchase of a standard IP licensed versions of this IP with additional features and options including

Master, DDR, Time Control, etc., along with configuration tools, technical support and verification suites.

## 2. Overview of HDL Software

As shown in Figure 1, the RTL is divided into layers and modules within each layer. A design may use all 3 layers or a subset. The top layer is appropriate for direct use by a processor (e.g. MCU or DSP). Additionally, a state machine type design may use the Autonomous slave form, which uses the bottom layer and then binds a generated Autonomous register set on it, as shown in Figure 2. The modularity allows ease in use as well as incorporating it into a device as appropriate to its capabilities. Finally, it allows for easier control of clock gating and other power saving techniques.

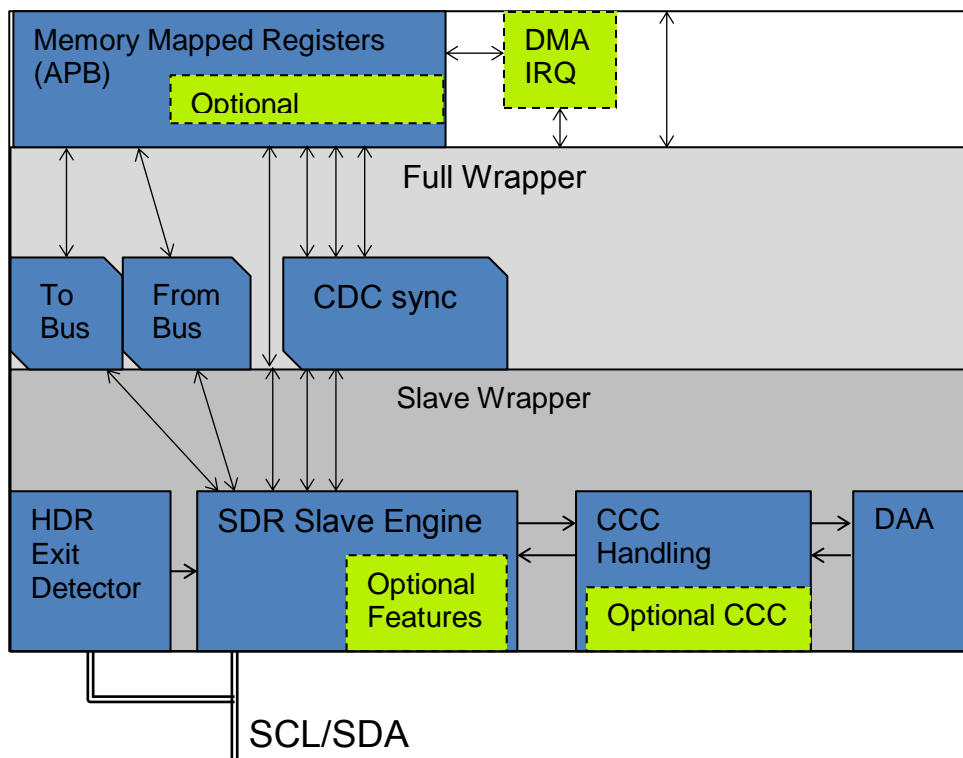


Figure 1 - Shows block layout of the RTL (HDR-DDR and Time control not shown).

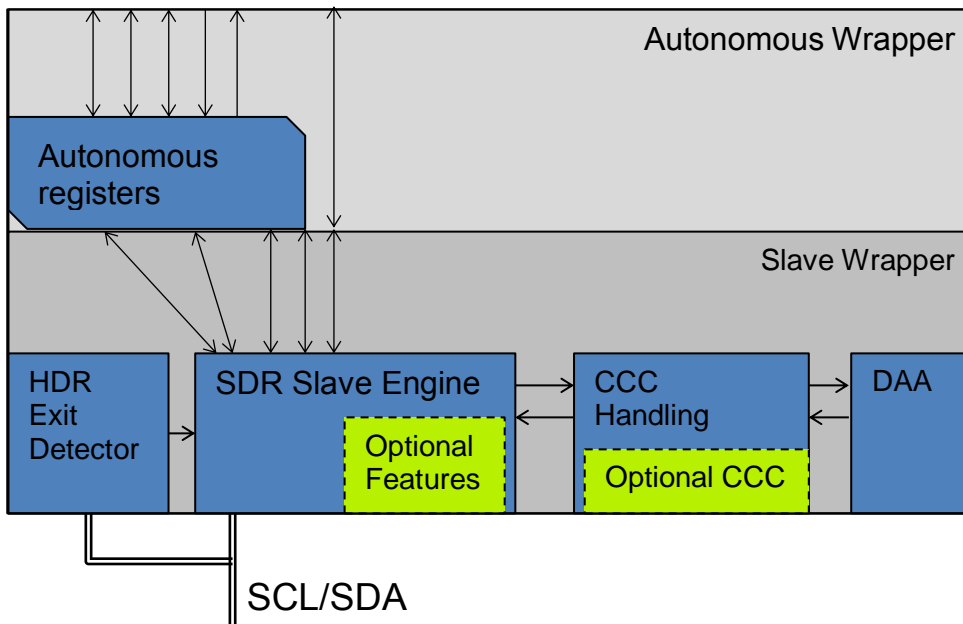


Figure 2 - Showing Autonomous Slave with generated registers

## 2.1 Documents to consult

The whole block is defined in detail in the accompanying specifications of **i3c\_peripheral\_slave\_uarch.pdf**, which outlines the parameters for configuration, the clocking and reset, how CDC is used, the signal lists for each layer, and more details on some features.

Additionally there are 2 other documents based on intended use:

- **i3c\_autonomous\_slave.pdf** details the autonomous slave, including how it works, how to configure it, and the port list.
- **i3c\_peripheral\_slave\_programmers\_model.pdf** explains the memory mapped registers, including which are available based on which parameters are selected. This is used for the basic checkout verification vectors provided.
- **i3c\_peripheral\_slave\_uarch.pdf**, which is the micro-architectural spec, covering the parameters for configuration, clocking and reset, CDC handling, ports, and layers. This can be used to integrate the design into your system.