# READ ME for I3C Free license Slave HDL Software (RTL)

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### Revision history

| Revision | Date | Description | Author |
|---|---|---|---|
| 1.1 | 12/11/18 | BSD License form to correspond to I3C Basic v1.0 release by MIPI (see notes). | NXP |
| 1.0 | 10/17/16 | Updated to free license form from BSD license. | NXP |

## Contents

# 1. Introduction

This free licensed distribution contains a Verilog implementation of a MIPI® I3C℠ Slave, implementing all required and a set of optional features. It matches the I3C Basic v1.0 feature set when configured down to that specification precisely.

This distribution does not come with the MIPI I3C specification nor any details copied from it. If you are not a member of the MIPI Alliance, and you wish to use I3C, you may download the MIPI I3C Basic specification to go with this source: https://mipi.org/specifications/i3c-sensor-specification?utm_source=MIPI+Alliance&utm_campaign=005db6649e-mipi-releases-I3C-Basic&utm_medium=email&utm_term=0_4ee96ff6dc-005db6649e-160669653
If you are a MIPI member, you may download either the MIPI I3C or I3C Basic specification, as you see fit.

If you are not a member, you are encouraged to join MIPI Alliance. Please see http://mipi.org/join-mipi
The I3C specification is available to all MIPI members, as are all other MIPI specifications, including ones using I3C for advanced functionality (e.g. Touch interfaces). Joining MIPI allows you and your company to contribute to specifications as well as access the whole library of MIPI specifications.

## 1.1 License Details

The HDL software (RTL) is provided with a BSD Open-source free license. The full BSD 3-line License is used, along with some notes from NXP related to this being RTL (HW) and not Software.

NOTE: No license under any third-party patent is granted or implied.
It is the responsibility of the licensee to obtain any required third-party patent licenses.

Note on terms used above:
1. Software and HDL software are used interchangeably.
2. Binary includes FPGA, simulation, and physical forms such as Silicon chips.
3. Clause 2 allows for such notice on a Web page or other electronic form not part of a distribution.

The original BSD source is available from:
https://github.com/NXPmicro/i3c-slave-design

## 1.2 License rights

The BSD free license allows you to use and optionally modify the HDL software (RTL) without providing it back. If any sources are modified, the original copyright notice and license notice must be preserved.
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NOTE: this file has been modified by MyCompany. The original sources may be obtained from NXP.

The sources may be compiled into forms such as for simulation, FPGA, or Silicon chip. Those forms may be distributed in normal ways, per the BSD license.

## 1.3 Building for FPGA, Simulation, or Silicon

To use this IP, there are 3 documents provided:

- i3c_peripheral_slave_uarch.pdf, which is the micro-architectural spec, covering the parameters for configuration, clocking and reset, CDC handling, ports, and layers.
- i3c_programmers_model.pdf, which covers the APB Memory Mapped register interface.
- i3c_autonomous_slave.pdf, which is for non-processor uses; this provides built-in registers to support natural use in combination with a device state machine (e.g. sensor event collection mechanism).

Note that not all features are available in the free version.

### 1.4 Use of more advanced features and Master

The free licensed sources allow for the most common uses of a MIPI I3C Slave, including what is in MIPI I3C Basic. This may be sufficient for your uses, including for experimentation, evaluation, FPGA projects, Silicon chips, etc. It is possible to purchase support or full commercial versions from Silvaco:
http://www.silvaco.com/products/IP/i3c.html
This includes 2 basic options:

1. Purchase of commercial support of the free version. A so-called 'Freemium' license.
2. Purchase of a standard IP licensed versions of this IP with additional features and options including Master, DDR, Time Control, etc., along with configuration tools, technical support and verification suites.

## 2. Overview of HDL Software (both APB and Autonomous forms)

As shown in Figure 1, the RTL is divided into layers and modules within each layer. A design may be use all 3 layers or a subset. The APB bus top layer is appropriate for direct use by a processor (e.g. MCU or DSP). Additionally, a state machine type design may use the Autonomous slave form, which uses the bottom layer and then binds a generated Autonomous register set on it, as shown in Figure 2. The modularity allows ease in use as well as incorporating it into a device as appropriate to its capabilities. Finally, it allows for easier control of clock gating and other power saving techniques.

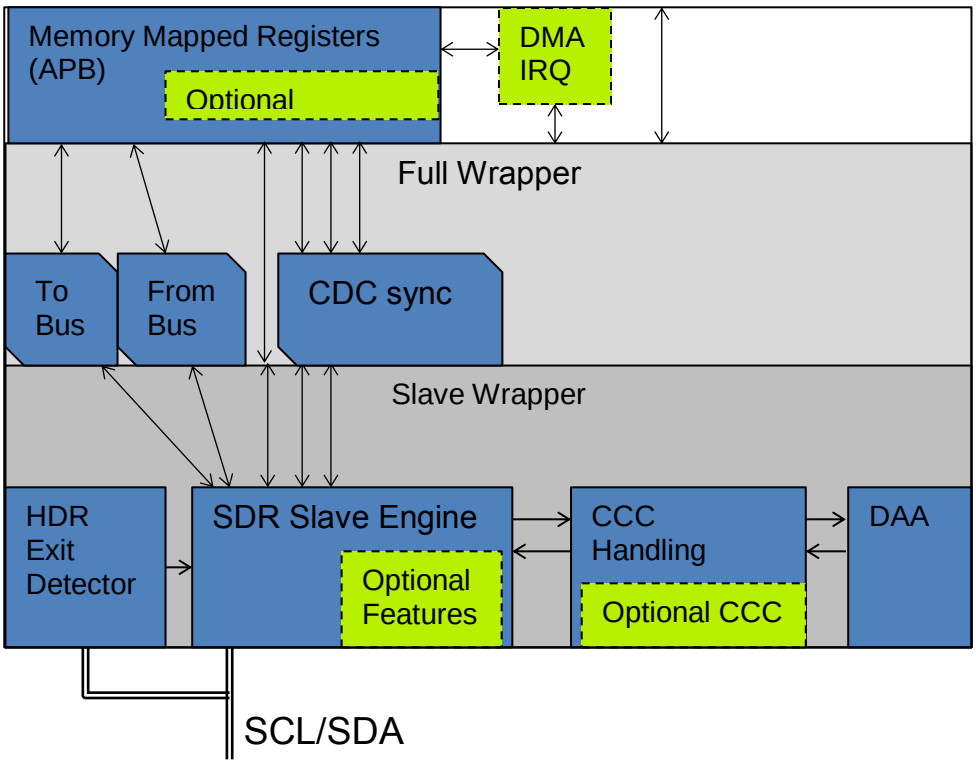


**Figure 1 - Shows block layout of the RTL (HDR-DDR and Time control not shown).**

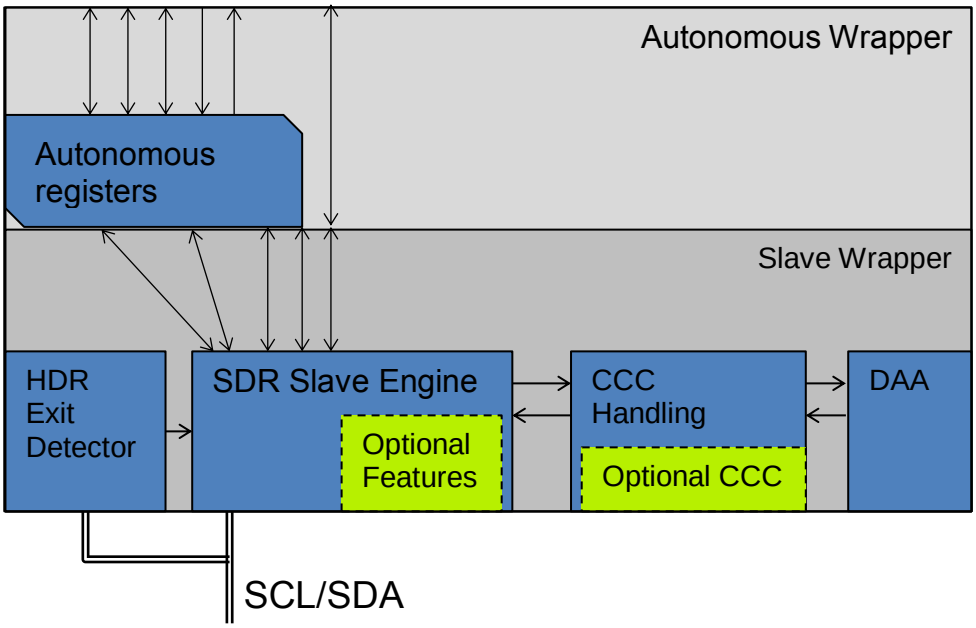


**Figure 2 - Showing Autonomous Slave with generated registers**

## 2.1 Documents to consult

The whole block is defined in detail in the accompanying specifications of **i3c_peripheral_slave_uarch.pdf**, which outlines the parameters for configuration, the clocking and reset, how CDC is used, the signal lists for each layer, and more details on some features.
Additionally there are 2 other documents based on intended use:

- **i3c_autonomous_slave.pdf** details the autonomous slave, including how it works, how to configure it, and the port list. Note that the distribution includes an RTL checker and display mechanism to show what your parameters mean.
- **i3c_peripheral_slave_programmers_model.pdf** explains the APB memory mapped registers, including which are available based on which parameters are selected.
- **i3c_peripheral_slave_uarch.pdf**, which is the micro-architectural spec, covering the parameters for configuration, clocking and reset, CDC handling, ports, and layers. This can be used to integrate the design into your system.