XXIV IMEKO World Congress "Think Metrology"
August 26 – 29, 2024, Hamburg, Germany

IMPROVING THE ACCURACY OF DIGITAL-TO-ANALOGUE CONVERTERS

Jonathan Sæthre Ege[1], Bikash Adhikari[2], Ahmad Faza[2], Trond Ytterdal[1], Arnfinn A. Eielsen[2,]*

[1]Norwegian University of Science and Technology, O. S. Bragstads Plass 2B, 7034 Trondheim, Trøndelag, Norway,
{jonathan.s.ege, trond.ytterdal}@ntnu.no
[2]University of Stavanger, Kjell Arholms gate 41, 4021 Stavanger, Rogaland, Norway,
{bikash.adhikari, ahmad.faza, arnfinn.a.eielsen}@uis.no

Abstract – The precision of digital-to-analogue converters (DACs) is principally limited by static errors in the output voltage or current levels, known as element mismatch. This paper evaluates five error mitigation methods on a set of candidate integrated circuit (IC) designs. The aim is to find a combination of a realistic and implementable IC design and a linearisation method that can yield a minimum of 18 effective number of bits (ENOB) at a 100 kHz bandwidth, well above the current state-of-the-art of semiconductor-based DACs, which currently is 17 ENOB at a 10 kHz bandwidth. It is demonstrated that three out of five methods provide performance improvements, with noise-shaping with digital calibration approaching the desired target.

Keywords: digital-to-analogue conversion; linearisation; dithering; simulation; current-steering; open-source

1. INTRODUCTION

The performance of digital-to-analogue converters (DACs) is principally limited by static errors in the output voltage or current levels which are known as element mismatch and quantified by the integral non-linearity (INL). These errors fundamentally limit the achievable accuracy and resolution in high-precision applications as they result in harmonic distortion, as well as gain and offset error. These errors can be compensated for using various linearisation methods. Summarily these are physical level calibration, dynamic element matching, noise-shaping with digital calibration, large periodic high-frequency dithering, and large stochastic high-pass noise dithering [1].

At lower frequencies, the static INL characteristic dominates, and it has been experimentally demonstrated that by using physical calibration, noise-shaping with digital calibration, and large periodic high-frequency dithering that it is possible to improve the performance of an off-the-shelf DAC to yield in excess of 17 effective number of bits (ENOB) at a bandwidth of 10 kHz [1]. This should be compared to the best baseline measurements of 15 ENOB for a standard off-the-shelf precision Nyquist-rate DAC and 16 ENOB for an audio DAC featuring noise-shaping in combination with dynamic element matching [2]. Audio DACs are targeted to provide good performance in the audible frequency range and perform poorly for general-purpose signal reproduction in other frequency ranges.

Increasing the bandwidth causes additional dynamic deleterious effects to come into play, mainly the slew-rate limitation [3]. There is a general divide between commercially available slow precision DACs and fast communications DACs. Precision DACs offer small INL and low noise but are slew-rate limited, whereas communications DACs feature significantly larger INL and noise, but with a much less severe slew-rate limit. With the available linearisation methods it has currently not been experimentally possible to leverage the improved slew-rate limit in communications DACs to yield an improved ENOB. This is mainly due to the significantly increased INL, but also due to the large sensitivity to environmental variables, such as temperature, making it difficult to model with accuracy. As a result, a tailor-made integrated circuit (IC) is being designed, in order to maximise the performance gain achievable using linearisation methods, and ultimately be able to yield a minimum of 18 ENOB at a 100 kHz bandwidth.

An evaluation of five available, real-time implementable linearisation methods applied to four proposed IC DAC designs is presented. One set of ICs have been implemented using the open-source SkyWater CMOS technology which is available to be simulated in a number of freely available SPICE compatible circuit simulators. Another set of ICs were implemented in a proprietary CMOS technology, available for simulation in the commercially available Spectre circuit simulator. The transistor modeling available in both cases typically provides good correspondence to the response of the final, fabricated IC. The simulation results demonstrate that three of the five methods can provide significant improvements in the resolution and accuracy and that it is possible to achieve the desired performance with reasonable assumptions on the ability to measure INL and achievable noise and distortion in the reconstruction filter. Improved DAC performance will find a wide range of applications including general metrology, dynamic measurements of voltage and current, precision mechatronics and machining, lithography, and optics.

2. NOISE AND DISTORTIONS IN DACS

Noise and distortion in digital-to-analogue conversion result from factors such as repeated spectra, quantisation, element mismatch, thermal noise, and semiconductor noise [3]. Repeated spectra occur due to converting a time-sampled signal to continuous time, as the signal spectrum below the Nyquist frequency (half the sampling rate) repeats at higher frequencies. Higher-order repetitions are typically attenuated

by the low-pass effect of the commonly used zero-order hold interpolation implemented by most DAC topologies, as well as low-pass reconstruction filters. Quantisation maps a large set of values into a smaller set, discarding some values and introducing a signal-dependent error. Element mismatch causes the output levels of the DAC to deviate from ideal levels, resulting in a static error known as integral non-linearity (INL), causing harmonic and inter-modulation distortion. INL is static in the sense that it measures the deviation from a linear, or straight-line, response. In many DACs, the INL can vary significantly with environmental variables, most notably temperature and ageing. Circuit components, such as resistors, capacitors, and transistors, contribute mainly to thermal noise and semiconductor noise. Component level noise can be reduced by using low-noise components (e.g. lower value resistors or larger area transistors) and averaging, i.e. summing several channels and low-pass filtering.

2.1. Uniform quantisation

Let w be the input signal then the quantisation operation $\mathbf{Q}$ on the input signal can be expressed analytically in terms of the quantiser step-size δ as

$$\mathbf{Q}(w) := \delta \left\lfloor \frac{w}{\delta} + \frac{1}{2} \right\rfloor \tag{1}$$

where $\lfloor . \rfloor$ denotes the floor operation. The quantised data is typically represented using binary encoding. For a word-size $\mathcal{B}$, a DAC has $2^{\mathcal{B}}$ quantisation levels. Let Δ represent the full-scale output range of the DAC. Then, the step size δ, commonly referred to as the least significant bit (LSB), is defined as $\delta = \Delta/(2^{\mathcal{B}} - 1)$.

Let $y = \mathbf{Q}(w)$ represent the output signal after the quantisation operation. Then the quantisation error is defined as

$$q(w) = \mathbf{Q}(w) - w = y - w. \tag{2}$$

The quantisation error has a maximum magnitude of $1/2$ LSB and is periodic in w with a period of 1 LSB. From (2) it can be seen that the error q is a deterministic function of the input w. The classical model of quantisation assumes that it can be modelled as an additive, uniformly distributed, white noise signal, independent of w [4]. This approximation holds well for large frequency-rich signals but poorly for small signals with few frequency components.

2.2. Non-linear quantiser

Practical DACs exhibit element mismatch, causing the actual levels to deviate from the ideal, equidistant levels of the uniform quantiser. This static deviation is commonly known as integral non-linearity (INL). Let $y = \delta\ell$ and $\tilde{y}$ be the ideal and actual outputs of the DAC, respectively. Then the INL at the level ℓ is represented as

$$\mathrm{INL}(\ell) := \frac{\tilde{y}(\ell) - \delta\ell}{\delta}. \tag{3}$$

The INL is the principal source of distortion in DACs, and most linearisation methods developed for data converters aim at mitigating the effect of this static non-linearity.

3. LINEARISATION METHODS

In this Section, we provide brief descriptions of the various linearisation methods used. Detailed discussions on physical calibration, noise-shaping with digital calibration, dynamic element matching, and periodic and stochastic dithering methods and implementations can be found in [1].

3.1. Physical level calibration (PHYSCAL)

The element mismatch in the DAC, can be corrected by adjusting or trimming the output voltage or current levels; physically calibrating each level to reduce the mismatch. This can be done in a number of ways, but one straightforward solution is to use a secondary DAC with a small gain to produce the correction voltages or currents. The output levels $\tilde{y}$ can be measured on the DAC output while the ideal levels are the scaled input codes $\delta\ell$. The implementation of the physical level calibration is shown in Fig. 1. It operates by summing the output of the main DAC and a secondary DAC. The output range of the secondary DAC is scaled to a minimum of the maximum INL of the primary DAC, and the correction levels are stored in a lookup table (LUT). Using the LUT, the secondary DAC can drive the error corresponding to each level towards zero in the summing stage [5, 6].

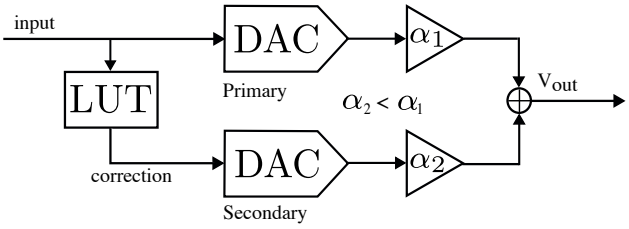

Fig. 1. Physical calibration using a secondary DAC where α_1 and α_2 are primary and secondary channel gains, respectively.

3.2. Noise shaping with digital calibration (NSDCAL)

Noise-shaping quantisers, or $\Delta\Sigma$-modulation, can effectively reduce the quantisation error due to uniform, or ideal, quantisation by shifting quantisation error to higher frequencies through oversampling and feedback. Typically the feedback filter is designed to generate a transfer-function equivalent to a high-pass filter for the quantisation error to the output. Subsequently a reconstruction filter is then used to attenuate the frequency-shaped quantisation error. The noise-shaping method employs an open-loop observer which means that any INL will cause the mismatch error to propagate to the output without attenuation, if the observer is the uniform quantiser. Digital calibration [7, 8] is a method where the uniform quantiser in the observer is replaced by measured output levels. The mismatch error is then more accurately estimated and can be attenuated by the feedback action. A block diagram illustrating a noise-shaping quantiser is depicted in Fig. 2.

3.3. Dynamic element matching (DEM)

By using more than one DAC channel, it is possible to introduce redundancy in how the output levels are generated. That means there are several combinations of output elements that can produce the same output level. Dynamic element matching leverages redundancy in the output elements to mitigate the effects of the element mismatch in the DACs. By scrambling the usage pattern of the elements, DEM causes the error resulting from the mismatches to be pseudo-random noise that is uncorrelated with the input sequence instead of

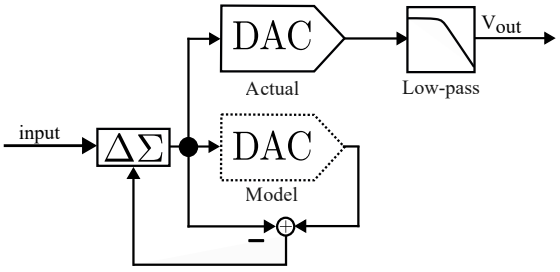

Fig. 2. Noise-shaping with digital calibration.

nonlinear distortion [9, 10]. A diagram illustrating the implementation of DEM with two channels and channel gain $\alpha = 1/2$ for averaging is shown in Fig. 3. Here, redundancy is introduced by using separate DACs, hence a DEM method for fully-segmented DACs (each DAC can only produce unique values) is required [11].

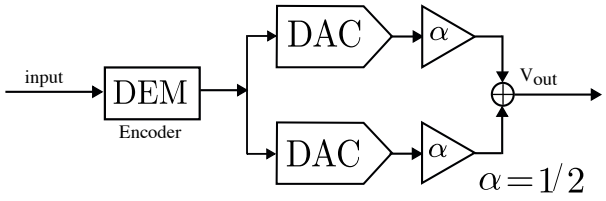

Fig. 3. Dynamic element matching with two DACs.

3.4. *Dithering*

The dithering technique intentionally introduces noise to the DAC input to mitigate effects due quantisation, element mismatch and some dynamic effects, such as glitches. The dither signal is a stochastic or periodic signal, and when applied to the input of a non-linear element (e.g. **Q** in (1)) it can be used to control the statistical properties when averaging [12, 13]. Non-subtractive dithering and subsequent filtering (averaging) is illustrated in Fig. 4. It is a low-cost feedforward method known to have a smoothing effect over the non-linear behaviour of the element. It has been shown to mitigate the effect of static non-linearities such as quantisation error [13] as well as element mismatch [14]. It can also reduce the effect of dynamic non-linearities [15, 16], and has been shown to work well for mitigating DAC glitches [17–19]. There are multiple ways of generating a dither signal with desired amplitude and spectral distribution characteristics, summarised in the following two Subsections.

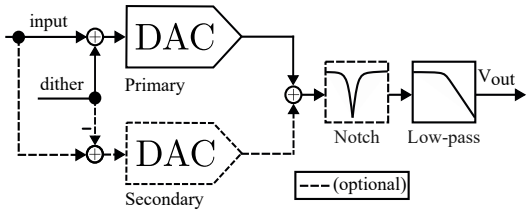

Fig. 4. Dithering with an optional DAC for canceling dither.

Periodic high-frequency dithering (PHFD)

By adding a high-frequency periodic dither signal, the desired signal traverses several voltage or current levels of the

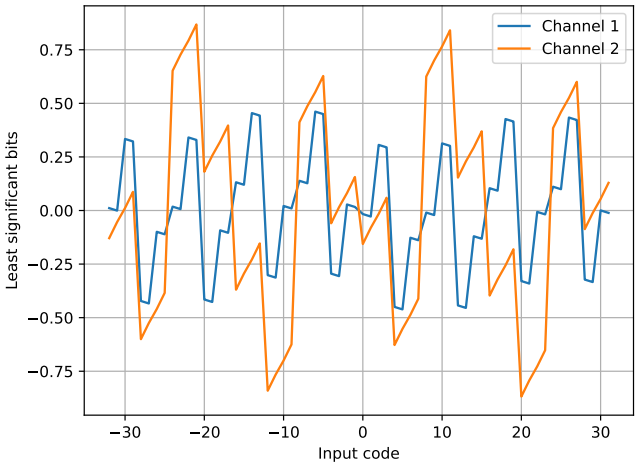

Fig. 5. INL for 6-bit DAC implemented in SkyWater.

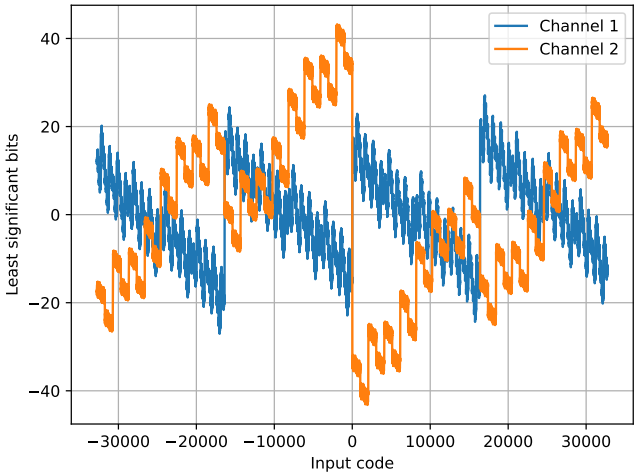

Fig. 6. INL for 16-bit DAC implemented in SkyWater.

DACs, effectively averaging out the mismatches [14]. As the high-frequency dither is undesired in the signal, various methods can be employed to attenuate it. Ideally, adding two identical signals with opposite polarity should cancel out the signal in the output. However, in practice, there will always be a residual signal that can be effectively attenuated by filtering the output using a notch filter and a low-pass filter.

Stochastic high-pass dithering (SHPD)

Stochastic high-pass dithering also reduces the effect of element mismatch by averaging out the mismatch. Unlike periodic high-frequency dithering, stochastic high-pass dithering achieves this smoothing through a random selection of voltage or current levels. It has been demonstrated that employing dither with a high-pass power spectral density decreases distortion resulting from element mismatch [1, 20]. Subsequently, a low-pass reconstruction filter can be employed to attenuate the undesirable high-frequency dither noise in the output.

4. DAC DESIGNS

Two different 130 nm CMOS technologies have been used. The first of the technologies used is a proprietary tech-

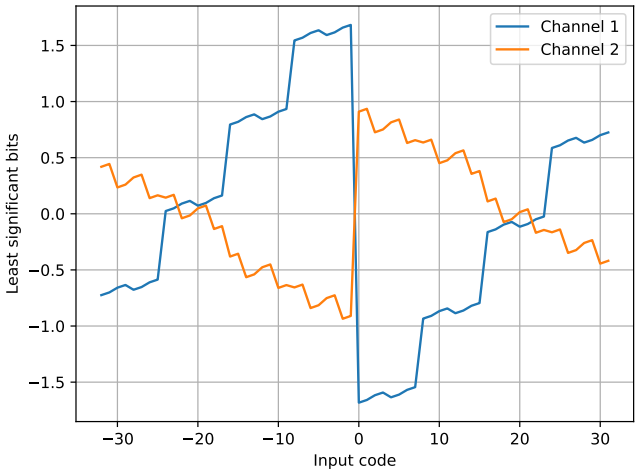

Fig. 7. INL for 6-bit DAC implemented in proprietary technology.

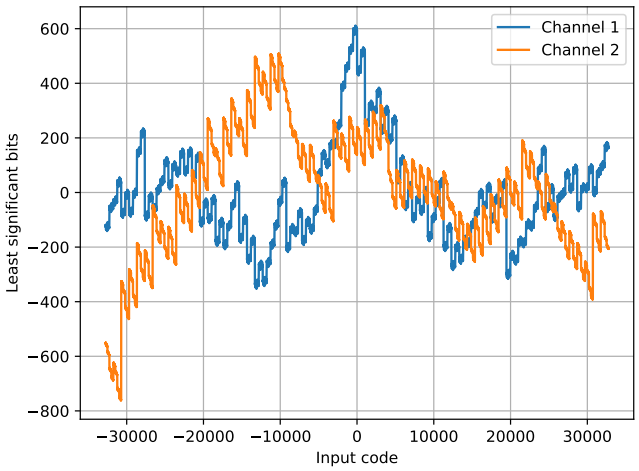

Fig. 8. INL for 16-bit DAC implemented in proprietary technology.

nology and is simulated in Cadence Spectre. The second technology is the open source technology, SkyWater 130 nm [21], and is simulated in Ngspice.

One 6-bit and one 16-bit DAC have been designed in each of the technologies. The DACs designed in SkyWater and the 6-bit DAC designed using proprietary technology are binary-weighted. While the 16-bit proprietary technology DAC is a hybrid DAC. This means that the 6 most significant bits of this DAC are unary-weighted (or thermometer-weighted), and the remaining 10 least significant bits are binary-weighted. All the DACs use the same current-steering topology, and have differential outputs. The current-steering topology was chosen because it is suitable for high-speed applications [22–25], attempting to minimise dynamic effects, increasing the slew-rate limit, which prevents the use of methods that cause high-frequency switching of elements. The proprietary technology DACs were designed for a 20 mA maximum output current. The SkyWater DACs were designed with the same transistor sizes, not aiming for specific current levels. Using the randomisation feature in SPICE, two instances of each of the SkyWater DACs were generated. The INL of these instances are shown in Fig. 5 for the 6-bit case and in Fig. 6 for the 16-bit case. Similarly, randomised instances were generated in Spectre for the proprietary technology DACs, and the

Tab. 1. Minimum and maximum output of the different DACs.

DAC	Proprietary		SkyWater	
	6-bit	16-bit	6-bit	16-bit
Minimum	-19.92 mA	-20.02 mA	-80.04 uV	-80.23 mV
Maximum	19.92 mA	20.02 mA	79.90 uV	80.24 mV

INL corresponding to the 6-bit and 16-bit DACs are show in Figs. 7 and 8.

The DAC designs consist only of the DAC cores which are made up of a number of P-channel Metal-Oxide Semiconductor (PMOS) unit cells. The design used for the unit cells is shown in Figure 9. It consists of three PMOS transistors, M0, M1, and M2. The unit size of the PMOS transistors are the same within a given DAC. The SkyWater DACs uses the same unit size for the PMOS transistors, while the proprietary DACs do not use the same unit sizes. Each unit cell is either scaled in a binary or unary fashion by varying the multiplier of the transistors. The multiplier of a transistors describes how many transistors are placed in parallel with each other. B1 is the voltage used to bias transistor M0 across all unit cells, driving M0 to generate the current I_{UC}. D0 and $\overline{D0}$ are the digital input signals used to control M1 and M2; which are used as switches. M1 and M2 are used to steer I_{UC} to either OP or ON; which are the positive and negative outputs of the DAC, respectively.

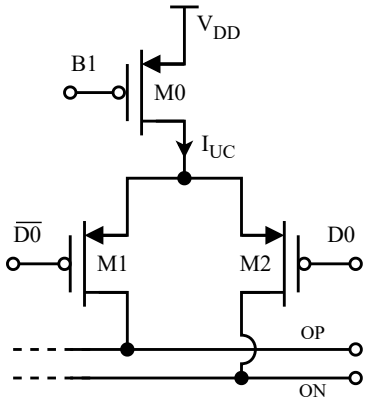

Fig. 9. Current-steering DAC PMOS unit cell.

4.1. Simulation settings

Some of the linearisation methods require two DACs of the same type. To emulate fabrication mismatch, different DAC instances based on the same design were generated using different Monte Carlo mismatch seeds. Throughout all simulations, a 999 Hz sinusoidal carrier is used and the implemented reconstruction filter is a 3rd-order Butterworth low-pass filter with a 100 kHz cut-off frequency.

The positive and negative outputs of the proprietary technology DACs have each been connected directly to ground. The positive and negative output of the SkyWater DACs have each been connected to 0.02 Ω resistors. The maximum and minimum output of each DAC is given in Tab. 1.

Tabs. 2 and 3 summarise the specific settings used for the PHFD and SHPD, respectively. The data-rate of the DAC is

specified in the rate row. The dither row specifies the dither frequency used. $F_{c_{hf}}$ is the corner frequency of the high-pass filter used to limit the frequency content of the applied stochastic dither. The scale row specifies the scaling of the dither, relative to the full scale of the DAC.

Tab. 2. Simulation settings for PHFD.

DAC	Proprietary		SkyWater			
	6-bit	16-bit	6-bit	16-bit	6-bit	16-bit
Rate	65.47 MHz	65.47 MHz	32.7 MHz	32.7 MHz	1.02 MHz	1.02 MHz
Dither	5.0 MHz	3.0 MHz	1 MHz	1 MHz	250 kHz	250 kHz
Scale	50 %	90 %	50 %	50 %	50 %	50 %

Tab. 3. Simulation settings for SHPD.

DAC	Proprietary		SkyWater			
	6-bit	16-bit	6-bit	16-bit	6-bit	16-bit
Rate	65.47 MHz	65.47 MHz	32.7 MHz	32.7 MHz	1.02 MHz	1.02 MHz
$F_{c_{hf}}$	200 kHz	200 kHz	200 kHz	200 kHz	200 kHz	200 kHz
Scale	80 %	90 %	50 %	50 %	50 %	50 %

5. RESULTS AND DISCUSSIONS

The primary performance indicator for DACs is the signal-to-noise-and-distortion ratio (SINAD), or alternatively, the effective number of bits (ENOB) [26]. SINAD is defined as the ratio of the standard deviations of the input signal and all other components, SINAD $= 20\log_{10}(\sigma_s/\sigma_t)$ where σ_s is the standard deviation of the input signal and σ_t accounts for all unwanted components in the output signal. The ENOB can be obtained from the SINAD using the expression ENOB $= (\text{SINAD} - 1.76)/6.02$.

ENOB performance results for the linearisation methods are provided in Tabs. 4, 5, 6, 7, 8 and 9. and Figs. 10, 11, 12, 13, 14 and 15 show the performances relative to their corresponding baselines. The simulation results indicate a strong correlation between the static modelling and the dynamic modelling provided by SPICE and Spectre. The designs are fast, and the dynamic effects are negligible. Although all the designs exhibit very large INL, the results demonstrate that compensation is still feasible. In a practical implementation, it is desirable for the INL to be insensitive to environmental variables to ensure accurate level measurements.

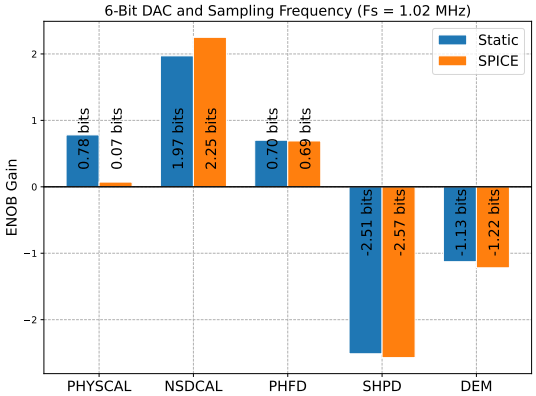

Fig. 10. ENOB gains for using different linearisation methods with 6-bit SkyWater DAC at 1.02 MHz sampling frequency.

Tab. 4. ENOB performance summary of simulation results for the 6-bit SkyWater DAC in SPICE at 1.02 MHz sampling rate.

	Method	Model	Scale	Word	Rate	ENOB
(a)	Baseline	Static	100%	6 bit	1.02 MS/s	6.051 bit
(b)	PHYSCAL	Static	100%	6 bit	1.02 MS/s	6.832 bit
(c)	NSDCAL	Static	99%	6 bit	1.02 MS/s	8.022 bit
(d)	PHFD	Static	50%	6 bit	1.02 MS/s	6.752 bit
(e)	SHPD	Static	50%	6 bit	1.02 MS/s	3.538 bit
(f)	DEM	Static	100%	6 bit	1.02 MS/s	4.924 bit
(g)	Baseline	SPICE	100%	6 bit	1.02 MS/s	6.093 bit
(h)	PHYSCAL	SPICE	100%	6 bit	1.02 MS/s	6.164 bit
(i)	NSDCAL	SPICE	99%	6 bit	1.02 MS/s	8.343 bit
(j)	PHFD	SPICE	50%	6 bit	1.02 MS/s	6.783 bit
(k)	SHPD	SPICE	50%	6 bit	1.02 MS/s	3.522 bit
(l)	DEM	SPICE	100%	6 bit	1.02 MS/s	4.874 bit

Tab. 5. ENOB performance summary of simulation results for the 6-bit SkyWater DAC in SPICE at 32.7 MHz sampling rate.

	Method	Model	Scale	Word	Rate	ENOB
(a)	Baseline	Static	100%	6 bit	32.7 MS/s	6.389 bit
(b)	PHYSCAL	Static	100%	6 bit	32.7 MS/s	8.206 bit
(c)	NSDCAL	Static	99%	6 bit	32.7 MS/s	16.476 bit
(d)	PHFD	Static	50%	6 bit	32.7 MS/s	8.828 bit
(e)	SHPD	Static	50%	6 bit	32.7 MS/s	7.461 bit
(f)	DEM	Static	100%	6 bit	32.7 MS/s	7.393 bit
(g)	Baseline	SPICE	100%	6 bit	32.7 MS/s	6.379 bit
(h)	PHYSCAL	SPICE	100%	6 bit	32.7 MS/s	6.483 bit
(i)	NSDCAL	SPICE	99%	6 bit	32.7 MS/s	11.206 bit
(j)	PHFD	SPICE	50%	6 bit	32.7 MS/s	8.847 bit
(k)	SHPD	SPICE	50%	6 bit	32.7 MS/s	7.502 bit
(l)	DEM	SPICE	100%	6 bit	32.7 MS/s	7.401 bit

Tab. 6. ENOB summary of simulation performance results for the 16-bit SkyWater DAC in SPICE at 1.02 MHz sampling rate.

	Method	Model	Scale	Word	Rate	ENOB
(a)	Baseline	Static	100%	16 bit	1.02 MS/s	11.121 bit
(b)	PHYSCAL	Static	100%	16 bit	1.02 MS/s	16.487 bit
(c)	NSDCAL	Static	99%	16 bit	1.02 MS/s	14.416 bit
(d)	PHFD	Static	50%	16 bit	1.02 MS/s	11.283 bit
(e)	SHPD	Static	50%	16 bit	1.02 MS/s	10.75 bit
(f)	DEM	Static	100%	16 bit	1.02 MS/s	8.645 bit
(g)	Baseline	SPICE	100%	16 bit	1.02 MS/s	11.111 bit
(h)	PHYSCAL	SPICE	100%	16 bit	1.02 MS/s	15.189 bit
(i)	NSDCAL	SPICE	99%	16 bit	1.02 MS/s	14.249 bit
(j)	PHFD	SPICE	50%	16 bit	1.02 MS/s	11.173 bit
(k)	SHPD	SPICE	50%	16 bit	1.02 MS/s	10.672 bit
(l)	DEM	SPICE	100%	16 bit	1.02 MS/s	8.640 bit

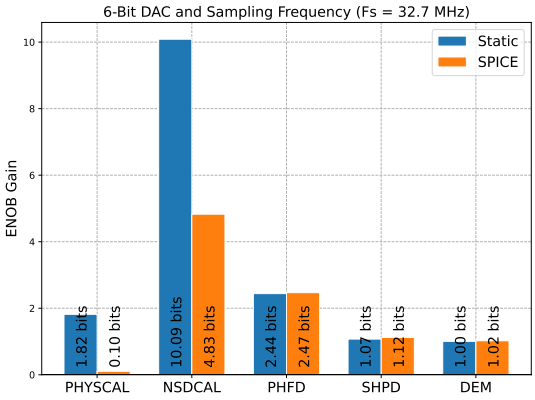

Fig. 11. ENOB gains for using various linearisation methods with 6-bit SkyWater DAC at 32.7 MHz sampling frequency.

Physical level calibration (PHYSCAL) leads to a notable improvement in the ENOB. This method requires two DACs, two gain stages, and a summing stage. In terms of computational complexity, the method is lightweight, only requir-

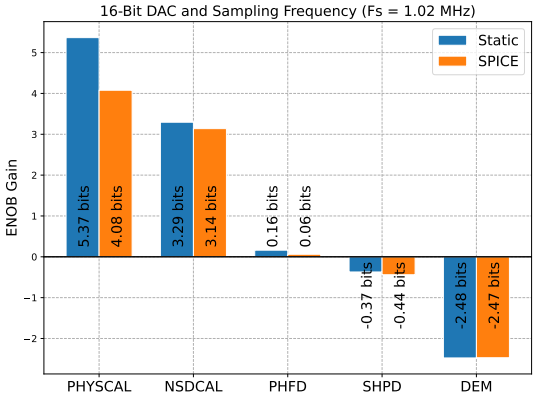

Fig. 12. ENOB gains for using different linearisation methods with 16-bit SkyWater DAC at 1.02 MHz sampling frequency.

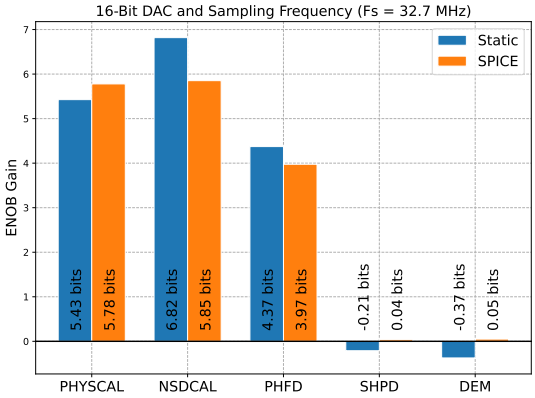

Fig. 13. ENOB gains for using different linearisation methods with 16-bit SkyWater DAC at 32.7 MHz sampling frequency.

Tab. 7. ENOB performance summary of simulation results for the 16-bit SkyWater DAC in SPICE at 32.7 MHz sampling rate.

	Method	Model	Scale	Word	Rate	ENOB
(a)	Baseline	Static	100%	16 bit	32.7 MS/s	11.514 bit
(b)	PHYSCAL	Static	100%	16 bit	32.7 MS/s	16.940 bit
(c)	NSDCAL	Static	99%	16 bit	32.7 MS/s	18.332 bit
(d)	PHFD	Static	50%	16 bit	32.7 MS/s	15.886 bit
(e)	SHPD	Static	50%	16 bit	32.7 MS/s	11.303 bit
(f)	DEM	Static	100%	16 bit	32.7 MS/s	11.141 bit
(g)	Baseline	SPICE	100%	16 bit	32.7 MS/s	11.134 bit
(h)	PHYSCAL	SPICE	100%	16 bit	32.7 MS/s	16.913 bit
(i)	NSDCAL	SPICE	99%	16 bit	32.7 MS/s	16.986 bit
(j)	PHFD	SPICE	50%	16 bit	32.7 MS/s	15.109 bit
(k)	SHPD	SPICE	50%	16 bit	32.7 MS/s	11.172 bit
(l)	DEM	SPICE	100%	16 bit	32.7 MS/s	11.184 bit

Tab. 8. ENOB summary of simulation performance results for the 6-bit proprietary DAC in Spectre at 65.47 MHz sampling rate.

	Method	Model	Scale	Word	Rate	ENOB
(a)	Baseline	Static	100%	6 bit	65.47 MS/s	4.452 bit
(b)	PHYSCAL	Static	100%	6 bit	65.47 MS/s	8.544 bit
(c)	NSDCAL	Static	99%	6 bit	65.47 MS/s	16.700 bit
(d)	PHFD	Static	50%	6 bit	65.47 MS/s	9.224 bit
(e)	SHPD	Static	20%	6 bit	65.47 MS/s	6.575 bit
(f)	DEM	Static	100%	6 bit	65.47 MS/s	8.057 bit
(g)	Baseline	SPECTRE	100%	6 bit	65.47 MS/s	5.37 bit
(h)	PHYSCAL	SPECTRE	100%	6 bit	65.47 MS/s	5.64 bit
(i)	NSDCAL	SPECTRE	99%	6 bit	65.47 MS/s	5.44 bit
(j)	PHFD	SPECTRE	50%	6 bit	65.47 MS/s	9.19 bit
(k)	SHPD	SPECTRE	20%	6 bit	65.47 MS/s	5.91 bit
(l)	DEM	SPECTRE	100%	6 bit	65.47 MS/s	8.14 bit

Tab. 9. ENOB summary of simulation performance results for the 16-bit proprietary DAC in Spectre at 65.47 MHz sampling rate.

	Method	Model	Scale	Word	Rate	ENOB
(a)	Baseline	Static	100%	16 bit	65.47 MS/s	6.997 bit
(b)	PHYSCAL	Static	100%	16 bit	65.47 MS/s	12.61 bit
(c)	NSDCAL	Static	99%	16 bit	65.47 MS/s	18.647 bit
(d)	PHFD	Static	10%	16 bit	65.47 MS/s	9.928 bit
(e)	SHPD	Static	10%	16 bit	65.47 MS/s	7.799 bit
(f)	DEM	Static	100%	16 bit	65.47 MS/s	9.216 bit
(g)	Baseline	SPECTRE	100%	16 bit	65.47 MS/s	5.98 bit
(h)	PHYSCAL	SPECTRE	100%	16 bit	65.47 MS/s	5.86 bit
(i)	NSDCAL	SPECTRE	99%	16 bit	65.47 MS/s	5.90 bit
(j)	PHFD	SPECTRE	10%	16 bit	65.47 MS/s	4.66 bit
(k)	SHPD	SPECTRE	10%	16 bit	65.47 MS/s	5.22 bit
(l)	DEM	SPECTRE	100%	16 bit	65.47 MS/s	6.25 bit

ing the implementation of a look-up table of integer values. However, a major drawback of this method is the necessity to measure the levels of both channels and any errors in the measured levels directly result in degraded performance. The method also does not benefit from higher sampling rates.

Similar to PHYSCAL, NSDCAL significantly improves the ENOB and provides the best performance overall. This method requires only one DAC but relies on adequate low-pass filtering of the output. The computational complexity of the method is moderate, requiring a look-up table of floating-point numbers, as well as the implementation of a second-order infinite impulse response (IIR) filter. As with PHYSCAL, the main drawback is that the INL must be measured. This method benefits greatly from higher sampling rates, as more of the error power can be shifted to higher frequencies. For higher oversampling rates the frequency of element switching can become quite high, incurring a performance penalty due to dynamic effects.

Periodic high-frequency dithering (PHFD) also improves the ENOB significantly. The method requires only the generation of a triangle-wave signal, making it the simplest method in terms of computational complexity. It also provides the best robustness with respect to changes in DAC response due to e.g. environmental variables, as this method does not rely on modelling and accurate level measurements, and consistently smooths the INL, even if it changes over time. However, it reduces the usable output range of the DAC, increasing the relative noise floor. This issue can be mitigated by averaging several channels if multiple DACs are available. Additionally, this method benefits from higher sampling rates, especially with smaller word sizes, as it effectively converts time resolution into value resolution.

Stochastic high-pass dither (SHPD) did not improve the ENOB. It does impact the harmonic distortion, but not as much as PHFD. This is likely due to the shape of the probability density function, being Gaussian, which then provides less smoothing of the INL compared to the uniform distribution of the triangular wave. This, combined with the difficulty of providing sufficient, practical attenuation of the dither noise at low frequency leads to poor performance. For the SPICE and Spectre simulations there is likely some effect due to the rapid switching between elements from the high-pass dither signal, which causes noise increase due to slew-rate limitations and glitches. This method requires only one DAC but needs sufficient low-pass filtering on the output. In the simulations, two DACs were used to approximately cancel the dither. The computational complexity is higher compared to

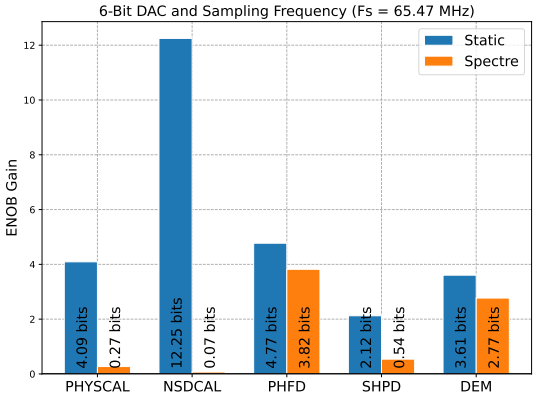

Fig. 14. ENOB gains for using various linearisation methods with 6-bit proprietary DAC at 65.47 MHz sampling frequency.

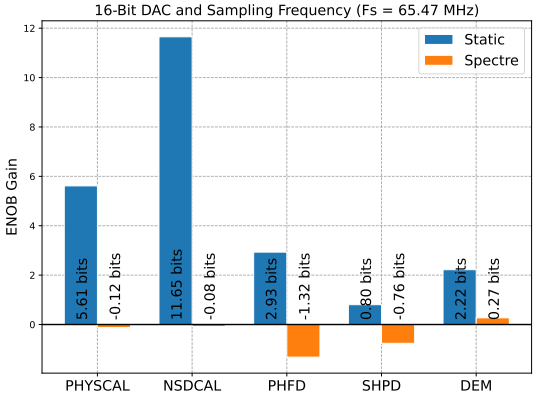

Fig. 15. ENOB gains for using various linearisation methods with 16-bit proprietary DAC at 65.47 MHz sampling frequency.

the large periodic high-frequency dither method, as it requires an infinite impulse response (IIR) filter and a random number generator. Improvement in the noise floor can be achieved by averaging several channels if multiple DACs are available.

The dynamic element matching (DEM) methods also performed very poorly and did not provide improvements in ENOB. Similarly to SHPD, the harmonic distortion was reduced, indicating that method was effective in reducing the effect of INL. The method [11] requires discrete uniform probability densities for the switching sequences, for which spectral shaping is not readily available. Hence the spectral distribution for the switching sequences used were white, and subsequently the error spectrum was white, meaning it was not attenuated well by the reconstruction filter, with a large amount of noise in the baseband. Although the main advantage of DEM is that it does not require knowledge of the INL to compensate for it, this method is considerably more computationally intensive compared to the other methods presented. As with the case of SHPD there is likely some deleterious effects from dynamic non-linearities due to the rapid switching between elements.

6. CONCLUSIONS

This paper investigates five different methods for mitigating the effects of non-linearity caused by element mismatch in digital-to-analogue converters. Simulation results demonstrate that three out of the five methods provided performance improvements in different settings: physical-level calibration, noise-shaping with digital calibration, and periodic high-frequency dithering. The two methods that did not perform well were dynamic element matching and stochastic high-pass noise dithering. Noise-shaping with digital calibration requires the least custom hardware but relies on accurate measurements of the non-linearity. Periodic high-frequency dithering does not require any knowledge of the non-linearity and is least sensitive to operating conditions but may require two or more channels and additional filtering to suppress the dither signal and to compensate for the increased noise floor due to reduced effective range. It was demonstrated that noise-shaping with digital calibration can approach the desired target of 18 ENOB at 100 kHz, with the assumption that accurate level measurements can be obtained. In order to reach the target, the most salient parameters to improve are the integral non-linearity and the sampling rate.

FUNDING STATEMENT

This work was supported by the Research Council of Norway, project FRIPRO 313716.

REFERENCES

[1] A. A. Eielsen and A. J. Fleming, "Existing methods for improving the accuracy of digital-to-analog converters," *Review of Scientific Instruments*, vol. 88, no. 9, p. 094702, 2017.

[2] ——, "Experimental assessment of dynamic digital-to-analog converter performance for applications in precision mechatronic systems," in *Proc. Australian Control Conference*, 2016, pp. 329–334.

[3] M. J. Pelgrom, *Analog-to-Digital Conversion*. Springer, 2013.

[4] W. R. Bennett, "Spectra of quantized signals," *The Bell System Technical Journal*, vol. 27, no. 3, pp. 446–472, 1948.

[5] J. Goes, J. Franca, N. Paulino, J. Grilo, and G. Temes, "High-linearity calibration of low-resolution digital-to-analog converters," in *Proc. IEEE International Symposium on Circuits and Systems*, vol. 5, 1994, pp. 345–348.

[6] J. V. Kane, "Double Precision Bidirectional Self-Calibrating Analog to Digital Converter," *Review of Scientific Instruments*, vol. 36, no. 7, pp. 1062–1063, 1965.

[7] T. Cataltepe, A. R. Kramer, L. E. Larson, G. C. Temes, and R. H. Walden, "Digitally corrected multi-bit ΣΔ data converters," in *Proc. IEEE International Symposium on Circuits and Systems,*, vol. 1, 1989, pp. 647–650.

[8] M. Frey and H. A. Loeliger, "On the Static Resolution of Digitally Corrected Analog-to-Digital and Digital-to-Analog Converters With Low-Precision Components," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 1, pp. 229–237, 2007.

[9] I. Galton and P. Carbone, "A rigorous error analysis of D/A conversion with dynamic element matching," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 42, no. 12, pp. 763–772, 1995.

[10] I. Galton, "Why dynamic-element-matching dacs work," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 2, pp. 69–74, 2010.

[11] K. L. Chan, N. Rakuljic, and I. Galton, "Segmented Dynamic Element Matching for High-Resolution Digital-to-

Analog Conversion," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 11, pp. 3383–3392, 2008.

[12] G. Zames and N. Shneydor, "Dither in nonlinear systems," *IEEE Transactions on Automatic Control*, vol. 21, no. 5, pp. 660–667, 1976.

[13] R. Wannamaker, S. Lipshitz, J. Vanderkooy, and J. Wright, "A theory of nonsubtractive dither," *IEEE Transactions on Signal Processing*, vol. 48, no. 2, pp. 499–516, 2000.

[14] A. A. Eielsen and A. J. Fleming, "Improving digital-to-analog converter linearity by large high-frequency dithering," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 6, pp. 1409–1420, 2017.

[15] C. A. Desoer and S. M. Shahruz, "Stability of dithered nonlinear systems with backlash or hysteresis," *International Journal of Control*, vol. 43, no. 4, pp. 1045–1060, 1986.

[16] B. Armstrong-Hélouvry, P. Dupont, and C. C. De Wit, "A survey of models, analysis tools and compensation methods for the control of machines with friction," *Automatica*, vol. 30, no. 7, pp. 1083–1138, 1994.

[17] A. A. Eielsen, J. Leth, A. J. Fleming, A. G. Wills, and B. Ninness, "Large-amplitude dithering mitigates glitches in digital-to-analogue converters," *IEEE Transactions on Signal Processing*, vol. 68, pp. 1950–1963, 2020.

[18] A. Faza, J. Leth, and A. A. Eielsen, "Mitigating non-linear DAC glitches using dither in closed-loop nano-positioning applications," in *Proc. American Control Conference*, 2023, pp. 685–691.

[19] ——, "Criterion for sufficiently large dither amplitude to mitigate non-linear glitches," in *Proc. IEEE Conference on Control Technology and Applications*, 2023, pp. 970–977.

[20] S. A. Leyonhjelm, M. Faulkner, and P. Nilsson, "An efficient implementation of bandlimited dithering," *Wireless Personal Communications*, vol. 8, no. 1, pp. 31–36, 1998.

[21] SkyWater Open Source PDK. Accessed 2024-05-30. [Online]. Available: https://github.com/google/skywater-pdk/

[22] Y. Tang, J. Briaire, K. Doris, R. van Veldhoven, P. C. W. van Beek, H. J. A. Hegt, and A. H. M. van Roermund, "A 14 bit 200 MS/s DAC With SFDR $>$78 dBc, IM3 $<$ -83 dBc and NSD $<$-163 dBm/Hz Across the Whole Nyquist Band Enabled by Dynamic-Mismatch Mapping," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 6, pp. 1371–1381, 2011.

[23] D. Gruber, M. Clara, R. S. Pérez, Y.-S. Wang, C. Duller, G. Rauter, P. Torta, G. Knoblinger, and K. Azadet, "A 12-b 16-GS/s RF-Sampling Capacitive DAC for Multi-Band Soft Radio Base-Station Applications With On-Chip Transmission-Line Matching Network in 16-nm FinFET," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 12, pp. 3655–3667, 2021.

[24] S. M. Taleie, T. Copani, B. Bakkaloglu, and S. Kiaei, "A Linear Σ–Δ Digital IF to RF DAC Transmitter With Embedded Mixer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 5, pp. 1059–1068, 2008.

[25] E. Roverato, M. Kosunen, K. Cornelissens, S. Vatti, P. Stynen, K. Bertrand, T. Korhonen, H. Samsom, P. Vandenameele, and J. Ryynänen, "All-Digital LTE SAW-Less Transmitter With DSP-Based Programming of RX-Band Noise," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3434–3445, 2017.

[26] W. Kester, Ed., *Data Conversion Handbook*. Elsevier, 2005.