

ECEN 4623/5623 RT Embedded Systems

Lecture 1 – Introduction
Part-4 – Terminology Guide

- **Actuator** - electro-mechanical device which converts analog or digital electrical inputs into mechanical energy interacting with the physical world.
- **ADC** - Analog to Digital Converter, encodes analog signals into digital values.
- **Aperiodic** – lacking a distinguishable frequency or period, having irregular occurrence. Faults and processing exceptions in real-time systems are aperiodic due to unpredictability of when or how often they might occur.
- **API** - Application Programmer's Interface, provides function call interface to lower level software and/or hardware functionality.
- **Anytime Algorithm** - Anytime algorithms generate the best answer given available information that has been processed since service request up to a deadline for response. The answer generated by the algorithm is an approximation of the correct answer at the deadline.
- **Application Executive** - Also known as a *Cyclic Executive*, a main loop program that calls functions on a periodic sub-rate of the main loop period.
- **Asynchronous** - An event or stimulus that occurs at any point in time rather than at known predictable points in time - e.g. an external interrupt may occur at any time and will immediately change the thread of execution on a *CPU*.
- **Asynchronous Logic** - Digital logic that is not globally clocked, but rather changes state based on edge triggering in a combinational logic circuit or edge triggered by multiple independent clocks.
- **Atomic Operation** - A non-interruptable CPU instruction - i.e any instruction that can be fetched and completed before the CPU can be interrupted.
- **Autonomic** - a network of organized, "smart" computing components that give us what we need, when we need it, without a conscious mental or even physical effort - this new view of computing will necessitate changing the industry's focus on processing speed and storage to one of developing distributed networks that are largely self-managing, self-diagnostic, and transparent to the user - IBM

- **Bandwidth** - data transfer per unit time, e.g. bytes/second.
- **BDM** - Background Debug Mode, a variant of *JTAG* that allows data and instructions to be clocked into and out of a 10-pin interface to a processor.
- **Best Effort** - scheduling policy that does not guarantee any particular response time for a service request, but attempts to make progress on all such requests and maximize total throughput.
- **Binary Semaphore** - a *semaphore* that has only 2 states: full and empty; a take on an empty binary *semaphore* will *block* the calling *thread* and a take on a full binary *semaphore* will change the state to empty; a give on an empty binary *semaphore* will change the state to full and a give on a full *semaphore* has no effect.
- **Black-Box Test** - a set of test vectors and driver that operate only on the functional interface of a subsystem or system with no knowledge of the internal workings or execution paths in the case of software.
- **Block Transfer** - transfer of data (typically contiguous, but may be a *scatter/gather list*) that includes multiple memory words/bytes on a bus with automatic addressing of each element in the block - rather than addressing and performing a full bus cycle to transfer each word.

- **Blocking** - when a *thread* of execution has been *dispatched* on the CPU for execution, but it needs some other resource such as memory access, an I/O interface, or some other external condition to be true such that it must give up the CPU and wait, the *thread* is said to be blocked.
- **Block-Oriented Driver** - A software I/O device interface which enables memory blocks to be transferred to and from the I/O device - rather than one memory word at a time.
- **Boot Code** - Software that is the very first to execute after a processor is reset and hardware sets the *PC (program counter)* to an initial address for execution - boot normally completes after initializing fundamental resources such as memory, cache, memory mapped devices, installing interrupt vector handlers, initializing basic critical I/O devices and disabling others, ... finally loading a higher level program or *RTOS kernel image* and then jumping to its entry point.

- **Bottom Half (BH)** - Software interfacing to I/O device hardware which services interrupts related to the device, provides basic configuration and control, monitors status, and buffers I/O data - the *Top Half* makes a Bottom Half usable for application software. Note that Linux normally defines the BH and TH opposite of the definition provided here.
- **BSP** - Board Support Package, the *boot* code and basic I/O interface initialization code needed by an *RTOS* to *boot* and cycle on an embedded system board.
- **BSS** - uninitialized global C program data - because the data is not initialized, this data need not take up space in non-volatile memory, but must be allocated a data segment in working main memory.
- **Bt878** - Brooktree Video/Audio encoder which can digitize an NTSC input
- **Burst Transfer** - A bus transaction which involves an initial address cycle followed by many data read/write cycles terminated by the *bus master* (similar to *Block Transfer*, but of unlimited length).

- **Bus** - a parallel interface for reading/writing data words from/to addresses and includes: digital data lines, address lines, and control lines - note that address and data lines may be multiplexed rather than separate lines.
- **Bus Master** - a device which can initiate bus cycles to address a target device and then read/write data to the target device which supplies data or receives data.
- **Bus Analyzer** - a passive device which snoops on a bus to capture a record of all bus cycles - typically acts like a specialized *logic analyzer* and can be setup to trigger and start collecting a bus cycle trace when a particular address, data, or control bit pattern is active on the bus.
- **Byte-Oriented Driver** - a device interface which provides the ability to read/write single words/bytes to and from the I/O device one at a time.
- **C (in RMA)** - the execution time required by a service to provide a response not including any time spent blocking (only time where the CPU was in fact being used to compute a response output).

- **Cache** - high speed access memory which typically can be read or written in a single CPU cycle, but due to high cost per storable word, is used as an efficient copy of a much larger main memory device - hardware functionality is typically included to aid with cache memory management including maintenance of cache/memory coherency, mapping of main memory addresses to cache lines (*Direct Mapped, Set Associative, Fully Associative*), and loading/write-back of data between cache and main memory.
- **Cache Coherency** - a cached copy of data at a given address will be different than the data at the same address in main memory after a cached write to this address - when this happens the cache control hardware/software must restore agreement between the data in cache and main memory sometime before data would otherwise be corrupted. Two main policies are used to maintain coherency - *write-back* and *write-through* - however, when memory addresses are cached and also used for DMA or other types of I/O, special care must also be taken by application code to ensure that data is not corrupted by intelligently performing write-backs and re-loads of cache lines as needed.

- **Cache Hit** - when a read or write is performed by an application on data cached at the address accessed/updated, then this is said to be a cache hit.
- **Cache Miss** - when a read or write is performed by an application on data that is not presently in cache and therefore the CPU must first load the data at the address being accessed/modified, this is said to be a cache miss.
- **Cache Line Eviction** - a system event where data that is written back to memory, freeing up a cache line.
- **Cache Line Invalidation** - a system event where a cache line is marked, typically with a status bit called “dirty”, which indicates that the cache line must be reloaded from memory before data is read from it.
- **Cache Line Locking** - Many caches have control features allowing a program to lock a particular address into a line of cache preventing this line from being replaced when other addresses are loaded (makes most sense for *set associative* caches rather than direct mapped) - cache line size varies, but is often 16-64 bytes.

- **Cache Line Pre-fetch** - Many caches have a feature allowing a program to request the cache to load a cache line despite the fact that the associated address has not been accessed yet - the idea is that this address will eventually be accessed in the future and rather than stalling the *CPU pipeline* at the time it is accessed, intelligent applications can plan ahead.
- **Cache Miss Penalty** - The number of CPU core cycles that the CPU pipeline must be stalled when a cache line must be loaded after a cache miss in order for a thread of execution to continue.
- **Call-back** - a programming technique where a pointer to a function is passed to a different function (registered) so that the function which obtains this pointer can call the function passed to it by reference later on - a technique commonly used in user interfaces so that an event such as a mouse click can be handled generically by code which however will call any number of user application callbacks when the mouse click event is detected.

- **Canonical Service** - A coding style template used for a real-time service provided by an *RTOS task* or *thread*. This style may vary, but at a minimum includes a main loop which executes as long as the service is “in service” and has a code section which either polls for input or *synchronously* or *asynchronously* waits for a service request.
- **Ceiling** - The ceiling is a mathematical operation that can be performed on a real number (floating point) - the ceiling(n) is the closest integer whole number greater than or equal to n - e.g. ceiling(1.1) = 2. (note that floor(1.0) = ceiling(1.0) assuming that the significance is 1, which is the the typical definition of floor and ceiling unless otherwise noted).
- **CFD** - Control Flow Diagram, a diagram used in Structured Analysis/Design which indicates where control signals in the system originate, where they terminate and how they change the flow of data and/or the processing of data in a *DFD*. (Note that a CFD is typically a subset of a DFD which shows both data flow and control flow).

- **Chaining Interrupt Service Routine**- A chaining *ISR* is an *ISR* which calls more than one handler for the very same interrupt source and priority - a technique often used in software when a hardware interrupt line is shared by multiple devices. (Note that most *chaining ISRs* also perform *ISR polling*).
- **Check-Stop** - When an error condition on a CPU that can not be handled and further execution by the CPU is considered either dangerous or impossible, then the CPU hardware may enter a state known as check-stop where it ceases to fetch and execute instructions and can only leave this state via a reset - e.g. a detectable memory error that can not be corrected normally causes the CPU to enter check-stop.
- **Circuit Switched I/O** - an I/O channel that is dedicated to one and only one data source and sink - often the channel may be point-to-point, but may be switched before the circuit is established.
- **Cirrus Crystal 4281** - an audio encoder/decoder used in ECEN 4623/5623.
- **CLI** - Command Line Interface, a simple ASCII terminal type interface that can operate over serial or any other byte-stream I/O interface to provide the ability to command a device and obtain basic status information.
- **Closed-Loop (Feedback) Control System** – A control system which compensates for disturbances by measuring the output response, feeding the measurement back, and comparing the response to the input at a summing junction. Any difference between the output and measured response is driven to zero by actuators which drive the plant to make corrections.

- **CODEC** - Coder/decoder - a device that converts analog signals to digital to be read by a computer or transmitted over a network, and converts the digital signals back to analog. Sound cards and video cards use this kind of codec. Also, compression/decompression - a two-step process used on very large multimedia files. Files are compressed for storage and then expanded to their original size in order to play them back on the computer.
- **Completion Test** - This *necessary and sufficient* scheduling *feasibility test* is based upon the Sha, Lehoczky, and Ding theorem - documented in the Briand and Roy reference book used in ECEN 4623/5623.
- **Computational Complexity** - the mathematical magnitude of operations required to successfully execute a given algorithm - e.g. searching a data set can take N operations for N items linearly searched or $\log(N)$ operations for a balanced tree search of N items, or even constant C operations for N items with a perfect hashing function.
- **Context Switch** - When a CPU is multiplexed (shared) by more than one *thread* of execution and the scheduler provides *preemption*, when the scheduler does preempt a thread in order to *dispatch* another, it must save state information associated with the currently executing thread (e.g. register values including *PC*) so that this *thread* can later be *dispatched* again to restore its thread of execution without a state error. The process of preempting a running task in response to an interrupt or kernel event followed by dispatch of a new task is a Context Switch. In some scenarios a thread will exit, suspend or enter a delayed or pending state and will yield the CPU which will be followed by a dispatch of another thread from the ready queue – this is also considered a context switch despite the lack of a priority preemption of an executing thread.

- **Context Switch Overhead** - the number of machine code instructions (and clock cycles) that an RTOS scheduler must execute to perform a *context switch*.
- **Continuous Media** - I/O stream that requires isochronal delivery of data between a source and sink - e.g. video stream, audio stream, and possibly a telemetry stream.
- **Control Flow** - A control flow is a *CFD* unidirectional association between two processes and/or external entities that indicates an asynchronous mechanism used to control a process or data source/sink.
- **Control Plane** - the bus or network transport and memory buffer path for control flow in an architecture which strictly separates data and control. Control data and commands are processed to determine data flow parameters, context, and sequencing in the separated *data plane*.
- **Cooperative Scheduling** – A method for scheduling threads of execution through the threads themselves which make calls to transfer from one thread execution context to another rather than relying upon a centralized scheduler.
- **Coverage Criteria** - when unit tests and/or system tests are completed on software, coverage criteria define the completeness of the testing by specifying the percentage of execution paths, statements, conditions, and decisions that must be covered.
- **Control System** – A system consisting of subsystems and processes (plants) assembled for the purpose of controlling the outputs of the process.
- **CPI** - Clocks Per Instruction, a measure of CPU efficiency with the ideal that a CPU pipeline should have a CPI of 1.0 or less if the pipeline can retire an instruction every clock - if the pipeline is also *superscalar* such that multiple instruction pipelines may execute, then this type of *microparallelism* can theoretically yield a CPI less than 1.0.

- **CPU** - Central Processing Unit, a processor core providing arithmetic and logic operations, possibly floating point arithmetic, and basic register and memory operations.
- **CPU Bound** - When an application program is unable to execute any faster due to the clock rate of the CPU and the CPI.
- **CPU Pipeline** - The use of micro-parallelism in the CPU core to provide a stage of instruction processing every clock such that once the parallel pipeline is started, an instruction is completed every clock - stages typically include: fetch, decode, execution, and write-back as a minimum. The key to pipelining is that it is possible for the pipeline to fetch, decode, execute, and write-back all at the same time for 4 instructions at various stages - each instruction will actually take multiple cycles to complete, but in the aggregate one instruction is completed every clock. (Note that pipelines may also be superscalar such that whole pipelines may be run in parallel as well).

- **Critical Instant** - This assumption made by Liu and Layland when they formalized fixed priority RM describes a worst-case scenario where all services in a system would be released simultaneously.
- **Critical Section** - When two independent threads of execution share a resource, such as a shared memory location, the section of code which accesses and possibly updates this shared resource in each thread is called a critical section - to ensure correctness, both threads will employ a synchronization mechanism such as a *mutex semaphore* to protect the critical section.
- **Critical Time Zone** – A time interval in RM theory which extends from the last release of an interfering service to the end of the larger period containing it.
- **Cross Compiler** - A compiler which can generate code for a target processor which may be different than the host system that it runs on.
- **Cross Debugger** - A debugger which can single step through code executing on a target processor different than the host system the debugger interface is running on - most often this works with a host debugger which communicates with and controls a target agent debugger.

- **CSMA/CD** - Carrier Sense Multi-Access / Collision Detection, a protocol used in ethernet to detect when a node is already transmitting on the shared link and to back off and attempt to use the network later.
- **Cycle-Based Profiling** - profiling code executing on a processor by periodically saving off the current PC in a trace buffer - most often implemented by an interrupt generating counter that counts cycles and can be programmed to raise an interrupt every N cycles - the ISR associated can then service the interrupt and save off the PC each time into a trace buffer.
- **Cyclic Executive** – a control structure to explicitly interleave execution of more than one periodic process on a single CPU. The Cyclic Executive is often implemented as a main loop with an invariant loop body known as the cyclic schedule. The basic concept may be extended to include asynchronous interrupt service routines to select one of several loop invariants based upon even data, often called Main+ISR. In Main+ISR several loop invariant bodies selected by input data can provide different modes or rates of function execution - e.g. a high, medium, and low frequency executive.

- **D (in RMA)** - The service deadline relative to request for service.
- **DAC** - Digital to Analog Conversion, most often used to provide analog output to an actuator from a digital I/O interface - e.g. a motor or speaker.
- **Data Flow Diagram** - Data Flow Diagram, a diagram used in Structured Analysis/Design which indicates where data in the system originates, where terminate and how it is processed in between. (Note that a DFD typically includes a *CFD* and therefore shows both data flow and control flow).
- **Data Plane** – the bus or network transport and memory buffer path for data flow, most often DMA transfer blocks, in an architecture which strictly separates data and control. Payload data passes through the system untouched or minimally modified according to commands and context for the flow maintained in the separated *control plane*.
- **Data Segment** - a memory region reserved for global variables and constants in a C program thread - most often each thread has its own data segment. (Note, most programs include a Stack, Data, and Text segment as a minimum).
- **Datagram Transport** - transmission of packets on a link such that errors in transmission can be detected, but are not automatically corrected nor is there automatic retransmission of lost data - furthermore, there is no concept of a connection (real or virtual) such that multiple messages are unrelated and if fragmented will not be reordered or reassembled automatically.

- **DDR** - Double Data Rate, a bus data encoding technique where read or write data is transferred on both edges of a reference clock rather than just one (rising edge and falling edge) - this doubles the data rate.
- **Dead Reckoning** - a technique used in robotics and vehicle navigation whereby a direction or motion or rotation is selected and executed at a constant rate for a calculated period of time in order to produce a desired amount of translation or rotation to reach a target - e.g. a vehicle might be pointed north and drive at 5 feet per second for 1 hour in order to get to a target city due north of a starting point south of this target. The major disadvantage of dead reckoning is that there is no mid-course correction possible and overshoot and undershoot are also likely.
- **Deadline** - a time relative to a request for service when the service must be completed to realize full utility of the service.
- **Deadline Driven Scheduling** – Dynamic preemptive priority assignment scheduling using policies such as Earliest Deadline First or Least-Laxity First. As presented by Liu and Layland, this is EDF scheduling, however since its introduction, a number of different policies have been proposed in addition to EDF.
- **Deadline Monotonic** - a real-time theory directly related to RM, but with a policy such that shortest deadline receives highest priority (rather than shortest period) and a feasibility test based on deadlines rather than periods.

- **Deadlock** - a multi-thread condition where 2 or more threads of execution are waiting on resources held by another and the graph of wait-for associations is circular - e.g. if A is waiting on resource R1 to produce resource R2; and B is waiting on resource R2 to produce resource R1 - this is a deadlock.
- **Decoder** - a digital device which takes a bit-encoded input and produces an analog actuator output - e.g. audio playback decoder which drives a speaker - hardware or software that translates an encoded signal back to its original form.
- **Delayed Task** - the state of a VxWorks task which has been programmed arbitrarily to yield the CPU for a period of time before replacing itself back on the ready queue - e.g. taskDelay is called and task enters DELAYED state.
- **Deterministic** – causal events that are fixed in form, position, and character apriori; in real-time systems this describes services that provide invariant responses with no irregularity in timing of response, execution or behavior.
- **DFD** - Data Flow Diagram, a diagram used in Structured Analysis/Design which indicates where data in the system originates, how it is processed, and where it terminates (from data source to data sink).
- **Digital Control** - feedback control where the control law is driven by discrete periodic sensor samples and based upon a Z-transform (rather than a Laplace transform in analog control).

- **Direct-Mapped Cache** - a *cache* memory which has cache lines directly mapped to main memory locations such that a given main memory address can be loaded into one and only one cache line, yet a set/range of main memory locations may be loaded into that particular line.
- **Dispatch** - when an RTOS scheduler selects a thread ready to run, restores state associated with the thread, and transfers execution control back to the thread's last PC if it was preempted earlier (or to its entry point if the thread is ready to run for the first time).
- **DMA** - Direct Memory Access, a hardware state machine independent of the CPU core which is able to transfer data in or out of memory without directly executing core instructions, thus allowing the core to continue execution while regions of memory are copied, updated by an I/O device, or read out to an I/O device.

- **DOF** - Degree of Freedom, a rotational or translational dimension which a mechanical device can move in - e.g. a typical robotic arm has 5 rotating joints: base, shoulder, elbow, wrist, and gripper - the robot is therefore said to have 5 degrees of freedom.
- **Double-Buffering** - a technique often used in continuous media applications to allow for data acquisition into one buffer while another is being read-out and processed - when the acquisition buffer is full, the buffer pointers are swapped such that the newly acquired data is processed and the already processed buffer can now be used for acquisition.
- **Driver** - a driver is software composed of code which interfaces to a hardware device and provides buffering, control, and status and which also interfaces to RTOS threads/applications and provides controlled access to the hardware device for I/O.
- **DSP** - Digital Signal Processing, a specialized embedded processor core which includes parallel mixed analog and digital processing for typical signal processing functions - e.g. for a Fourier transform.
- **Dude** - Etymology: origin unknown
 - 1 : a man extremely fastidious in dress and manner : DANDY
 - 2 : a city dweller unfamiliar with life on the range; especially : an Easterner in the West – webster.com

- **Dynamic Linking** - a technique where *P/C* software compiled into an object file format such as *ELF* can be loaded and linked into existing software on an RTOS platform on the fly after the RTOS has already been booted and is up and running.
- **Dynamic Priority** - when thread or interrupt processing priorities are changed during run time by code, they are said to be dynamic.
- **Earliest Deadline First** - a dynamic priority scheme for scheduling where services are assigned priority dynamically every time the ready queue is updated, with highest priority given to the service with the earliest impending deadline - the scheme requires not only dynamic priority, but *preemption* to work.
- **ECC** - Error Correction Circuitry, a digital circuit which automatically corrects an SBE using an error detection and correction encoding such as the Hamming code - normally the data read out of memory is corrected before the final value is placed in the read buffer, but not necessarily also corrected in main memory - a *write-back* may be required to correct the actual memory location.

- **EDAC** - Error Detection and Correction, an information encoding scheme which not only allows for detection of errors, but correction of those errors - e.g. the Hamming code.
- **EEPROM** - Electrically Erasable Programmable Read Only Memory, a non-volatile memory device which can be erased and re-written in circuit if so desired.
- **EFSM** - Extended Finite State Machine, a formal method based upon state machines which extends the basic state transition on I/O to include side effects on transitions such as global data update and data processing.
- **ELF** - Executable and Linking Format, an object file format which includes significant annotation and is PIC such that these files can be dynamically loaded and linked and such that they can serve for supporting debug and trace analysis to map addresses back to source code.
- **Embedded System** - a digital and analog computer system which provides a specific set of services, driven by sensor inputs, and producing sensor outputs to provide services - e.g. digital control in an anti-lock braking system or call switching and billing management for a telecommunications main trunk (Note that the scale of the services provided and of the hardware itself does not matter).

- **Encoder** - a circuit which takes analog signal inputs and using an ADC converts them to digital and bit encodes them - e.g. an audio recorder which takes analog microphone input and encodes the input signal into 255 different tones - a sensor or transducer for converting rotary motion or position to a series of electronic pulses.
- **Entry Point** - an address in a *text segment* which is the first instruction in a function and serves as the starting point for a thread such that a scheduler can simply set the *PC* to this address in order to start execution of this thread.
- **EPROM** - Erasable Programmable Read Only Memory, a non-volatile memory device which typically can be erased by a UV light source and electrically re-programmed, but not in circuit, rather by pulling the device from a socket, exposing it to UV and then placing it in an external programmer.
- **Event-Based Profiling** - a profiling technique where the PC is saved into a trace buffer whenever events of a specific type exceed a threshold - e.g. when data cache misses exceed N misses, the PC is saved into a trace buffer.

- **Exception (NMI)** - an exception is normally a non-maskable interrupt because it signifies a serious error condition which must be handled before any program should continue execution - e.g. a bus error.
- **Execution Jitter** - when a service is dispatched and the number of cycles and/or instructions required to complete the service varies on each release, this service is said to have execution jitter.
- **Extended Finite State Machine** - an FSM (Finite State Machine) with more features than just states and I/O transitions so that the Von Neumann architecture and general programs may be modeled formally - e.g. on a state transition a procedural function may be called and or global memory updated.
- **External Fragmentation** - when blocks of a resource such as memory are allowed to be arbitrarily sized, small sections of the resource between used sections may evolve from successive allocations and frees such that significant resource exists, but is unusable unless allocations are moved to provide larger contiguous free spaces from small many non-contiguous spaces. (fragmentation outside of blocks).

- **FCFS** - First Come, First Served, the policy often used by an RTOS when services/threads are at the same priority level - i.e. the first service ready is the first one dispatched.
- **Feasibility Test** - An algorithmic or formulaic operation that takes a set of services and their *RM* characteristics and will provide a binary output indicating whether this service set can be scheduled given resources available and resources required by the service set.
- **FEC** - Forward Error Correction, an EDAC method provided in-line such that bit errors are handled at the link layer - e.g. Reed Solomon encoding (in contrast to EDAC memory).
- **Feedback** - a signal used in control systems which provides sensor inputs to compute the difference between desired and actual plant state such that a control law can drive the plant to a desired target control point.

- **FIFO** - First In, First Out, a policy for queues (e.g. a dispatch queue) where the first element queued is always the first element de-queued.
- **Firmware** - the first code to execute on a processor and therefore must initially execute out of an *NV-RAM* device, although it may load itself into memory and continue execution to complete a boot process before an RTOS is initialized and run. Less specifically, firmware is usually thought of as any software that directly interfaces to hardware to make the hardware usable by higher levels of software. A firmware engineer is typically a software engineer that has a good understanding of hardware or vice versa – the original background of a firmware engineer may be hardware or software design and the idea of straddling both worlds; integrating and co-designing SW/HW is appealing to this iconoclast.
- **Fixed Priority Scheduling** - a scheduling policy whereby threads on the ready queue are dispatched in priority order and the priority of any given thread is not modified over time.
- **Flash Memory** - a non-volatile memory technology that can be erased and re-programmed in circuit like EEPROM, but has much higher density for a given cost.
- **Floor** - The floor is a mathematical operation that can be performed on a real number (floating point) - the floor(n) is the closest integer whole number less than or equal to n - e.g. floor(1.1) = 1. (note that floor(1.0) = ceiling(1.0) assuming that the significance is 1, which is the the typical definition of floor and ceiling unless otherwise noted).

- **Flow Control** - signals between a data transmitter and receiver used to indicate buffer capabilities on each side so that a transmitter does not overdrive a receiver resulting in data loss when the receiver is unable to buffer incoming data.
- **Form Factor** - the physical dimensions of an electronic device that may be independent of the electrical characteristics - e.g. the PCI bus electrical specification and protocol is implemented as compact PCI, stackable PC/104+, and PMC (PCI Mezzanine).
- **FPGA** - Field Programmable Gate Array, an array of generic transistors which can be programmed once or on power-up to provide combinational logic and state machines for digital processing.
- **Fixed Priority Scheduling** - a scheduling policy whereby threads on the ready queue are dispatched in priority order and the priority of any given thread is not modified over time (except by the application itself).

- **Fully Associative Cache** - A *cache* which allows main memory addresses to be loaded to any cache line - this is the ideal cache since replacement is not constrained at all, but associative memory is complex and expensive - by comparison a *direct mapped cache* is completely constrained and a *set associative* is a compromise.
- **Gather Read List** - A list of not necessarily contiguous addresses in memory that are to be read into a contiguous buffer - e.g. a host memory may have multiple blocks in memory scattered through memory space that are to be read by an I/O device which will gather all these blocks into a single contiguous buffer before an I/O operation.
- **Geek** - a carnival performer whose act usually includes biting the head off a live chicken or snake; or more recently, a person often of an intellectual bent who is disapproved of by others.
- **GPIO** - General Purpose I/O - digital inputs and outputs at TTL logic levels which can be used as a generic interface to digital devices such as LEDs.

- **Hacker** - a person who is inexperienced or unskilled at a particular activity: an expert at programming and solving problems with a computer : a person who illegally gains access to and sometimes tampers with information in a computer system – webster.com
- **Hamming Code** - A bit encoding used to detect and correct *SBEs* (single bit errors) and to detect *MBEs* (multi-bit errors) for memory devices which may be subject to *SEUs*.
- **Hard Real-Time** - A service or set of services which are required to meet their deadlines relative to request frequency - if such deadlines are missed, there is not only no utility in continuing the service, but in fact the consequences to the system are considered fatal or critical.
- **Harmonic** - When the relative periods of services are all common multiples of each other - this characteristic can yield cases where the CPU resource can be deterministically scheduled to full utility. For example, T1=2, T2=5, T3=10 has a base frequency of 1/10th Hz and has the harmonic sequence of 1x, 2x, 5x for the base frequency.
- **Harvard Architecture** - a core CPU architecture which splits the memory hierarchy into separate instruction and data streams - typically including an L1 instruction cache which is independent of an L1 data cache.

- **Heap** - A memory space used for dynamic buffer management and/or dynamic allocation of memory as requested by an application - heap space is memory outside the data, text, and stack segments and is most often reserved by the boot or RTOS during initialization.
- **High Availability** - A system which guarantees that it will be ready to provide services with a quantifiable reliability - e.g. a system is said to provide 5 9's availability if it is ready to provide service upon request 99.999% of a given year (I.e. is only unavailable for a total of about 5 minutes per year). Note that HA systems can crash, but they can't be out of service very long if they do.
- **High Reliability** - A system which has been designed to have a very low probability of failure to provide services - typically measures such as redundancy, cross strapping, and fail safe modes are designed in to ensure that critical services have an extremely low likelihood of failure.

- **Host** - Desktop development computing system used in *IDE* for cross compilation, cross debugging, connection to the target agent, trace tools and any number of other tools that connect to a target server on the host to communicate with *target agent* software resident on the embedded system.
- **H-Reset** - Hardware Reset, either from a power-on reset state transition or from assertion of an external signal to drive a hardware reset.
- **HSTL** - High Speed Transceiver Logic, a 0.0-1.5v logic level standard used for high speed single-ended digital I/O, most often for memory I/O (speeds of 180 Mhz and greater).
- **HWIC** - Hardware In Circuit, a concept whereby debug and trace tools have hardware probes in circuit with a CPU by interfacing to signals coming from the CPU/SoC ASIC to the rest of the system board for the purpose of snoop tracing and/or control - e.g. JTAG debug emulator, Vision ICE Event Trace, RISCWatch trace port probe, and CodeTEST Universal trace probe.

- **ICE** - In Circuit Emulator, a debug and trace device which monitors all I/O pins on a CPU/SoC ASIC and provides memory trace, external interrupt trace, JTAG, I/O pin trace, and emulates the state of the system including all registers, cache, and addressing to aid in firmware development and board verification.
- **IDE** - Integrated Development Environment, a software development system which for an embedded system includes a cross and native compiler, cross and native debugger, and many target tools interfaced through a host-based target server and a target-based target agent.
- **Importance** - in real-time systems theory services with low priority based upon *RM* policy may still be critical to system operation - they are important despite being low priority.

- **Interference** - when a higher priority thread preempts a lower one in a fixed priority preemptive system the time that the CPU is unavailable to lower priority threads is referred to as interference time.
- **Internal Fragmentation** - When a resource such as memory is made available in minimum sized blocks, this can help reduce *external fragmentation*, but when a user of the resource requires less than a full block, this causes internal fragmentation.
- **Interrupt** – A hardware signal assertion into the CPU core from an IO device to indicate that an event has occurred such as data available on an input interface (e.g. a sensor sample or DMA transfer has been completed).
- **Interrupt Handler** - during the normal CPU pipeline processing (fetch, decode, execute, write-back) an external device may assert a signal input or an internal sub-block may also assert a signal input to the CPU core which causes it to asynchronously branch to an interrupt vector (a memory location) where basic code called the handler acknowledges and services the hardware and then calls application *ISRs*.
- **Interrupt Latency** - the delay between assertion of an interrupt signal by a device and the time at which the PC is vectored to an interrupt handler is known as the interrupt latency.

- **Interrupt Vector** - an address in memory where the CPU sets the PC after an interrupt signal is asserted, causing the CPU to asynchronously branch to this location and to execute the instruction there - normally a CPU will have a number of interrupt inputs (e.g. x86 IRQ0-15) and each signal asserted causes the CPU to vector to a different address such that different handlers can be associated with each interrupt signal.
- **Interval Timer** - a double-buffered state machine in a CPU core which allows software to set a value in a register that is loaded into a separate count-down register which asserts an interrupt at zero (or perhaps all F's if it counts up) and automatically is reloaded with the interval register value to repeat the process over and over - this hardware can therefore be used for basic timer services in an RTOS.
- **IO Bound** - a condition where an application does not have sufficient I/O bandwidth to meet throughput goals or real-time deadlines.

- **ISA Legacy Interrupt** - Industry Standard Architecture Legacy Interrupt, specifically refers to x86 architecture IRQ0-15 which have been part of the x86 architecture from the beginning (8086) and support a number of well-known PC devices and services such as booting from a hard drive.
- **Isochronal** - uniform in time, having equal duration, recurring at regular intervals; literally the same in time, which in real-time systems means that a service is required to produce a response at a precise time relative to a service request - not too early and not too late. This is important to continuous media applications and digital control which are sensitive to *jitter*. Most often isochronal services hold a response computed ahead of deadline that is delivered to an interface within a narrow band around the optimal time. For data transport, isochronal channels provide guaranteed bandwidth and latency characteristics so that the transmission of continuous media is provided with a constant bit, byte, or frame rate per unit time.
- **ISR** - Interrupt Service Routine, the application level of an interrupt handler which is often a call-back function registered with an RTOS that installs the *interrupt handler* at an *interrupt vector*.

- **Jiffy** - a term to describe the tick of a hardware interval timer – often the smallest unit of time that the OS can track - e.g. on x86 architecture the standard interval timer ticks about every 0.45 microseconds, but the Linux OS typically loads an interval timer count to generate interrupts such that it can control processes on a 10 millisecond software tick.
- **Jitter** - when latency and/or timing of an operation or process changes with each iteration, this is jitter - i.e. when latency/timing is not constant. Jitter as a term can be used to describe many different types of operations or processes - e.g. execution jitter, period jitter, response jitter.
- **JTAG** - Joint Test Applications Group, an IEEE committee that standardized the concept of boundary scan and the *TAP* (Test Access Port), which is used to verify integration of ASICS in a system (boundary scan), but is now also typically used in firmware development to control and single step a CPU by loading data and commands through the *TAP* with JTAG. JTAG includes the following signals: TDI (Test Data In), TDO (Test Data Out), TRST (Test Reset), Clock, Test Mode Set.

- **Keep-alive** - an indication from a thread/process/task on a system that it is functioning normally or perhaps similar indication from a subsystem in a larger system - the keep-alive is most often a simple ID and count indicating that the subsystem/thread/process/task is advancing through its service loop - often referred to as a heartbeat as well.
- **Kernel** - the software in an RTOS which directly controls all critical resources such as CPU, memory, and device I/O - the kernel is typically interfaced to by applications through an *API* or *device driver*.
- **Kernel Image** - the binary machine code text segment, data segment, stack, and BSS used for the RTOS kernel software.
- **Kernel Instrumentation** - tools like Windview or LTT which provide active tracing of C code and/or RTOS events require that code, often specifically kernel code, be instrumented with trace instructions that provide efficient update of a trace buffer with a trace token to track progress of the code and to mark events for later timeline analysis.

- **L1 Cache** - Level 1 Cache, a high-speed memory integrated on-chip with a CPU core - on the same ASIC for data access that can most often be completed in a single clock.
- **L2 Cache** - Level 2 Cache, a high speed memory off-chip which can be accessed in several clocks.
- **Latch-Up** - a non recoverable bit error due to permanent transistor logic damage to a memory device or register.
- **Latency** - delay in an operation or process due to physical limitations such as electronic propagation delay, the speed of light, the number of clock cycles required to execute instructions, or time to modify a physical memory device.
- **Laxity** - Laxity = (Time-to-Deadline - Time-to-Completion), but the time to the completion of a service can be difficult to determine, so most often an estimate of the Time-to-Completion is used which is derived from (WCET - Computation-Time-So-Far).
- **Layered Driver** - a layered driver includes a *Top Half* and *Bottom Half* - the *Top Half* provides an interface to application code wishing to use a hardware resource and the *Bottom Half* provides an interface to a hardware device.

- **LCM** - Least Common Multiple, the LCM is the smallest number which is also multiple of 2 different numbers - e.g. given $x=3$, $y=5$, the $\text{LCM}(x,y)=15$. This concept is key to periodic service analysis in real-time theory because it is necessary to diagram service times over the LCM of all periods in order to fully analyze timing demands upon a resource. Note that the LCM for numbers that are prime can be very large compared to harmonic numbers.
- **Least Laxity First (LLF)** - a dynamic priority policy where services on the ready queue are assigned higher priority if their laxity is the least (where laxity is the time difference between their deadline and remaining computation time) - this requires the scheduler to know all outstanding service request times, their deadlines, the current time, remaining computation time for all services, and to re-assign priorities to all services on every preemption. Estimating remaining computation time for each service can be difficult and typically requires a worst-case approximation.
- **LED** - Light Emitting Diode, a device typically used to provide visual I/O and status for an embedded system.
- **Lehoczky, Sha, and Ding Theorem (a.k.a Theorem 2)** - If a set of services can be scheduled over the period of the longest period service after a *critical instant*, then the system is feasible (i.e. is guaranteed not to miss a deadline in the future).

- **Limit Sensor** - a sensor which detects when hardware has reached a physical limit - e.g. when a robotic arm has driven a joint through full rotation after which continued motor drive will break the joint.
- **Linking (Dynamic or Static)** - Linking is the process by which an executable image is assigned addresses for all function entry points, all global variables, and all constants which may be referenced by other software modules - these addresses can be statically assigned once and for all at a pre-determined offset in physical memory (static linking) or may be position independent such that only relative addresses are assigned until the module is loaded, at which time physical addresses are derived from the relative (dynamic linking).
- **Live-lock** - related to deadlock, this situation arises when a circular wait for resources evolves and an attempt to break the deadlock is made by having each requester drop their requests and then re-request them - if the requests are well synchronized, then the system may cycle between deadlock and dropping requests over and over.

- **Logic Analyzer** - a hardware, firmware, software analysis tool that provides generic acquisition of digitally clocked signals (or arbitrary digital signals which are clocked by the analyzer internally).
- **LSP** - Linux Support Package, an embedded Linux term, much like a BSP, which refers to code required to boot Linux on a given architecture and platform - e.g. the PowerPC 750 LSP.
- **LTT** – Linux Trace Toolkit – a tool that traces events in the Linux kernel, encodes them, and stores a trace of event codes in memory. The event trace can be loaded later into a tool for timing analysis.
- **LVDS** - Low Voltage Differential Serial, an electrical standard for transmission of high-rate serial signals on wire pairs that carry differential signals to encode data.

- **Main+ISR** - this is essentially the same software architecture as a *Cyclic Executive*, however, Main+ISR may be much simpler in that it normally has just one main loop and a small number of ISRs compared to a *Cyclic Executive* which may have multiple loops operating at different frequencies.
- **MBE** - Multi-bit Error, a condition when more than one bit in a word is in error - typically this can not be corrected.
- **Memory Hierarchy** - the whole memory system design from the fastest and typically smallest devices to the slowest and typically largest devices - e.g. L1/L2 cache, main memory, and flash.
- **Memory Mapped I/O** - I/O devices which can be read or written can be mapped into the address space of a processor allowing software to simply update an address in order to write to the device or read an address to read from the device - the device must respond to the addressing by the CPU, i.e. decode it and then read/write data on a bus which both the device and CPU interface with.

- **Memory Protection** - an *MMU* feature which allows address ranges on page boundaries (a minimum size memory block) to be specified as read-only - if an update to such a range is attempted, the *MMU* will assert an *NMI* exception.
- **Message Queue** - an RTOS software mechanism which abstracts shared memory data into atomic enqueue and dequeue operations on a buffer controlled by the RTOS and known only to applications by an ID, accessible to them only through RTOS message queue operations. Operations are atomic with respect to threads only (not interrupts), and so most often only a message queue send is allowed in interrupt context - never a message queue receive.
- **Message Sequence Chart** - a diagramming method used in the Specification and Design Language (SDL) as well as UML (Universal Modeling Language) which shows threads of execution and all messages (or function call interfaces) which associate the threads in a protocol.

- **Micro-code** - machine code which executes on a state machine internal to a processor or on a simple state machine device that is independent of the main execution pipeline - e.g. the Bt878 RISC processor executes code fetched from the x86 processor's memory over the PCI bus - this code is micro-code from the viewpoint of the x86 system.
- **Micro-parallelism** - parallel processing inside the CPU core.
- **MMU** - Memory Management Unit, a block in most CPU cores which provides virtual to physical address mapping, address range checking, and can protect read-only address ranges from unintentional update.
- **Module Loading** - when an *ELF* module is transferred to an embedded target and dynamically linked into the kernel and other application code on the fly.
- **MTD** - Mapping to Device, a term used to describe Bottom Half code used in a flash file system driver.

- **Multi-access Network** - a network such as ethernet where more than one device can use the physical and link layer of the network, thus requiring a CSMA/CD protocol for shared use.
- **Multi-tasking** - when a CPU is shared and multiplexed by a scheduler in order that multiple threads with state information may execute on a single CPU or may be mapped onto a set of CPUs dynamically. Tasks include state information that goes beyond the minimal requirements of register state, stack, and PC for a thread - e.g. task variables, a task error indicator, name, and many other elements of a VxWorks *TCB*.
- **Multi-threaded** - when a CPU is shared and multiplexed by a scheduler with the minimal management of execution state for each thread of execution (register state, stack, and PC).

- **Mutex Semaphore** - a specialized semaphore (compared to a binary semaphore) which is specifically used to protect critical sections of code for multi-thread safety - this semaphore is used to guarantee mutually exclusive access to a shared resource such that only one thread may access a common resource at a time - with shared memory this prevents data corruption that could be caused by multiple readers/writers - e.g. if a writer has partially updated a shared data structure, is preempted/interrupted, and then a reader accessed the partially updated data, the data may be completely inconsistent.
- **Nand Flash** - a flash memory device which is normally erased to all F's and writes are bit-wise masked in with an and operation.
- **NCD SCAM Chip** - a pre-burned Microchip PIC which includes code to generate PWM signals for hobby servos (2 channels) based upon an RS-232 command.

- **Necessary and Sufficient** - a feasibility test in real-time theory which will pass all service sets that can be scheduled and will never fail a set that can be scheduled (more precise than a sufficient test which may falsely reject some service sets, but will never falsely ok a service set than can not be safely scheduled).
- **Nerd** – may be based on a creature portrayed in *If I Ran the Zoo* by Dr. Seuss: an unstylish, unattractive, or socially inept person; one slavishly devoted to intellectualism or academics to the point of their own detriment.
- **Nesting** - when a construct is used inside the same sort of construct - one inside the other - e.g. if a critical section encloses another critical section the critical sections are said to be nested.
- **Non-Blocking** - when a request for a resource can not be met immediately, the RTOS can either block the calling thread until it is available or return it an error code indicating why the request can not be met and letting the thread go on - the latter is non-blocking.
- **Non-Preemptive** – when all threads run to completion without interruption by other requests for service or the scheduler during execution.
- **Nor Flash** a flash memory device which is normally erased to all 0's and writes are bit-wise masked in with an or operation.

- **NTSC** - National Television Systems Council, the standard for analog color television transmission with 640x480 pixels.
- **NVRAM** - Non-Volatile Random Access Memory, memory which persistently holds data whether or not a system is powered or not - e.g. a battery backed-up *DRAM*, a *Flash memory* device, *EEPROM*, or *EPROM*.
- **Object Code** - machine code annotated with symbol information (variable and function names and addresses) and information to support debugging (source file names and locations).
- **OCD** - On-Chip Debugging, a type of JTAG front end that allows a typical line debugger to single step code through the JTAG protocol.
- **OnCE** - On-Chip Emulation, a type of JTAG front end that allows for not only debug through JTAG, but additional control such as register viewing and setting.

- **Offloading** - the concept of taking a software service and re-allocating it to a hardware implementation on a parallel processing unit in order to free the main CPU of loading - e.g. a network interface card may perform functions basic to TCP/IP such as checksums in order to offload those operations from the host CPU.
- **On-line Admission** - when a system can run a feasibility test while currently providing other services in order to determine whether new services can safely be added to the current safe set.
- **On-Off Control** - the use of relays to turn on and off motors to control a mechanical device.
- **Optical Navigation** - using computer vision images of a scene to determine ranges to targets and to plan paths to navigate to a target using only video data.
- **Optimal Policy** - a fixed priority assignment policy which will successfully schedule any set of services which can be scheduled by any other fixed priority policy.

- **Over-run Policy** - how a system handles a service which attempts to continue execution beyond its advertised deadline - e.g. the scheduler could terminate the service.
- **Packet Switched** - a network protocol which allows links to be shared by multiple datagram or virtual circuit protocols and routes packets between end-points based upon their header information.
- **PC (program counter)** - The Program Counter is normally a register used by a CPU to track the current or next address of main memory which contains a machine instruction to execute. (Note that a trace of the PC over time provides the definition of the *thread of execution* until a *context switch* occurs, if it does at all).
- **PCI** - Peripheral Component Interconnect, a standard defined by the PCI Special Interest Group to provide CPU, memory, and IO device interconnection for data transport.
- **PCI Bus Probing** - A process that allows a BIOS or OS software to find all PCI devices and functions on a given PCI bus using configuration space registers.

- **PCI Configuration Space** - A well known port address on x86 architecture where a PCI bus master can read/write registers in order to find other PCI devices and their functions and configure them as far as memory mapping and interrupts as a minimum.
- **PCI Interrupt Routing** - PCI interrupts A-D can be routed onto x86 legacy interrupts IRQ0-15 in order to allow PCI devices to interrupt an x86 core.
- **PCI-Express** - previously known as 3GIO, this standard is a scalable differential serial bus architecture for 2.5 Gbps main-board interconnection and peripheral connection.
- **Peak-Up** - a computer vision algorithm which finds a bright spot or the center of an object by segmenting an image and finding the centroid of a target within the image.
- **Pending Task** - a VxWorks task state which indicates the task is blocking on a resource not presently available.
- **Period Jitter** - when the period of a service request is not constant.
- **Period Transform** - a real-time theory adjustment to service characteristics to simplify analysis or to elevate importance of a service whereby the service period is assumed to be shorter than it really is.

- **Pessimistic Assumption** - RM is full of assumptions that are worst case and therefore make it a very safe form of analysis, but also may lead to excessive resource margin in order to guarantee deadlines - e.g. WCET.
- **PID Controller** – Proportional-Integral-Derivative Controller, a controller that sets outputs proportional to error, integrates sensor inputs to find for example velocity from acceleration, and also uses derivatives such as velocity from position measurements in order to control a system and obtain a target operational state - e.g. a cruise control provides acceleration proportional to the difference between current and target speed and integrates to determine when the target will be achieved and when to decelerate.
- **Pipeline Hazard** - A condition in a CPU pipeline that forces it to stall - e.g. a cache miss.
- **Pipeline Stall** - when a CPU pipeline must stop until a resource is made available.
- **PIT** – See Programmable Interval Timer.

- **Pixel** - A picture element - an array of picture elements forms an NxM image where each pixel encodes the XY position, brightness and RGB color mix for the picture element in the image.
- **Point-to-Point** - a network topology which connects nodes one-to-one.
- **Polling** - when status is checked periodically (synchronously) by a looping construct.
- **Polling Interrupt Service Routine** - an *ISR* which must determine the source of an interrupt by reading status registers when a hardware interrupt is shared by multiple devices (note that most polling *ISRs* also provide *ISR chaining*).
- **Position Independent Code** - code which is base address independent such that it can be mapped in at any base address and all other entry points, jumps, and memory locations are set relative to the dynamically determined base address.

- **POSIX** - Portable Operating Systems Interface, a standard for operating system mechanisms and APIs. POSIX includes a number of sub-standards such as 1003.1b which covers basic real-time mechanisms.
- **Power-on Reset** - a CPU state after initial power-on, which most often causes the CPU to branch to a known address and perform basic operations like resetting the memory controller, bus, and other basic interfaces.
- **Preemption** - when the current thread executing on a CPU is placed back on the ready queue by the scheduler and state information saved so that a different thread can be allocated the CPU.
- **Predictable Response** – compared to *deterministic* response, predictable means that the response behavior is bounded and characterized by a statistical distribution of response times rather than having an invariant response time.
- **Priority** - an encoding which controls the order of dispatch for threads by a scheduler when more than one is ready to use the CPU resource.
- **Priority Ceiling** - a priority is defined that is the highest priority a thread can have that may lock a resource, this priority level is stored as the resource's priority ceiling - a thread which has locked the resource is given priority as high as the highest priority thread blocking on the resource up to the ceiling value - i.e. the thread holding the resource always has a priority higher than or equal to all threads waiting to obtain the resource, but amplification is limited to the ceiling value. When the priority amplification is limited to the highest priority of threads involved in the mutex access to a shared resource it is a “least locker” protocol – when the amplification is simply set to the highest priority in the system, it is a “ceiling” protocol.

- **Priority Inheritance** - See Briand and Roy p. 66 - If a thread is holding a resource and another thread of higher priority is blocking on the same resource, the thread holding the resource inherits the blocked threads priority for the duration of the *critical section*. There is no limit on the priority level that may be inherited.
- **Priority Inversion (Unbounded)** - whenever a thread is unable to obtain the CPU and a thread of lower priority is holding it, this is called priority inversion. The condition is most often caused by a secondary resource needed by a thread such as a shared memory critical section - in a simple two thread case, if a lower priority thread is in a critical section, then a higher priority thread experiences priority inversion for the duration of the critical section, however, if the low priority thread suffers interference from a medium priority thread, the high priority thread could potentially be blocked for an indeterminate amount of time, an unbounded priority inversion.

- **Priority Preemptive Run-to-Completion** - A scheduling mechanism which dispatches any thread ready to run based on priority as soon as the set of ready threads is updated (preemptive) and allows a dispatched thread to run indefinitely unless another higher priority thread is added to the ready set (via an interrupt or a call to the RTOS by the currently running thread). One danger of this type of system is that a high priority non-terminating thread will take over the CPU resource completely. **Priority Queue** - A mechanism for implementing a first-in-first-out policy, but with N levels of priority such that all items at the highest priority level are dequeued first first-in-first-out before all items at the next lower priority level.
- **Process** - a thread of execution with stack, register state, and PC state along with significant additional software state such as copies of all I/O descriptors (much more than a task TCB for example) including a protected memory data segment (protected from writes by other processes).
- **Programmed IO** - a technique where software reads and writes each word to and from a device interface involving the CPU in each and every transfer.
- **Programmable Interval Timer (PIT)** – A CPU core timer that can be loaded with a value to count down with a known decrement period so that when it reaches zero an interrupt is asserted and the counter optionally reset automatically. In some cases it may count up to 0xFFFF_FFFF.
- **Protocol Stack** - a layered driver which includes data processing between the *Bottom Half* and *Top Half* layers - each layer can be separated and has a distinct interface - e.g. TCP/IP.

- **Pure Function** – a function coded so that it only uses stack (no global data at al), depends only in input parameters, and calls only other pure functions is a pure function and is also *thread safe*.
- **PWM** - Pulse Width Modulation, a technique to control a motor or other normally analog device by creating a pulse train of digital TTL output to simulate an analog output.
- **Quality of Service** - definition of service levels based upon guarantees of resource availability for each service - e.g. processor capacity can be reserved for each service in advance (say 10%) and the system guarantees that this capacity will be available within in a worst case period of time, however may not guarantee all services will meet their deadlines.
- **RAS** – Reliability, Availability, Serviceability
- **Rate Monotonic** - a hard real-time theory for fixed priority preemptive run-to-completion systems where priority is assigned according to service request period (higher priority for shorter period) and where feasibility of a set of services can be determined by the RM least upper bound or an iterative test such as the completion test.
- **Reachability Space** - The points in space where a robotic device can place and end effector - e.g. places in space where a robotic arm can grapple an object.
- **Ready** - the VxWorks task state where a task is ready to running and waiting only on the CPU to be granted by the scheduler.
- **Ready Queue** – a FIFO queue of VxWorks tasks that are ready to execute on the CPU.

- **Real-Time (System)** – an event driven system (sensors provide input through *ADCs*) for which services provide computation to produce a response (output to actuators interfaced with *DACs*) before a deadline relative to the request for service. A hard real-time system must never miss a deadline, but a soft or best effort system may be allowed to miss occasional deadlines.
- **Real-Time Clock** - a hardware clock circuit which maintains an absolute date and time (e.g. Gregorian or Julian date), often employing a battery-backed clock circuit and/or a method to synchronize with an external time source such as Universal Coordinated Time.
- **Real-Time Correctness** - a real-time service must produce functionally correct outputs and also provide the outputs prior to a relative deadline to be real-time correct.
- **RTOS** – Real-Time Operating System, a scheduling and resource management framework for implementation of software services that must provide responses to requests prior to well defined deadlines.
- **Re-boot** - when a system is commanded or as a part of a recovery mode re-enters the boot code entry point causing re-initialization of memory, I/O interfaces, and re-start of all services.

- **Recovery** - a key feature of a high availability system, this is the mechanism by which a system which is experiencing system failures restarts those services. A system may need to start a recovery process for a number of reasons - e.g. deadlock, priority inversion, livelock, resource exhaustion. Often recovery is achieved by the hardware *watch dog* which reboots the system.
- **Reentrant Function** – a reentrant function must be designed so that it can be called from multiple execution contexts (threads) and still provide correct results. A reentrant function must either allocate unique copies of global data for each execution context (VxWorks task variables), provide mutex protection for global data, or avoid the use of global data completely as a *pure function*.
- **Regression Test** - re-running a test to verify that features previously verified still work after bug fixes or feature addition - intended to prevent unintentional interactions between software modifications that might introduce new problems.
- **Relay** - a mechanical or solid state device which provides a simple switch - e.g. double pole double throw or single pole single throw – normally open, latching, or normally closed when not energized.
- **Reliable Transport** - a data transport protocol on a network which includes error detection/correction, retransmission and supports diverse routing such that overall data is delivered if at all possible.
- **Resource Arbiter** - a sub-system which implements a resource grant policy - e.g. a bus arbiter coordinates bus grants for bus requests from multiple masters and targets.

- **Response Time** - the latency between a request for service (typically by an ISR) and the generation of a response output.
- **Ring Buffer** - a data structure which provides multiple serially reusable buffers - most often used to buffer incoming data from a device interface before it can be processed - likewise for output data before it can be transmitted.
- **RISC** - Reduced Instruction Set Computer.
- **RM**- Rate Montonic, the basic theory formulated by Liu and Layland for fixed priority multiplexing of a single CPU that is intended to provide multiple services over time.
- **RMA** - Rate Monotonic Analysis, the process of analyzing the C , T , and D characteristics of a set of *services* to be executed on a CPU and determination of priorities according to *RM policy* and *feasibility* according to a *sufficient* or better yet, *necessary and sufficient* test.

- **RM Least Upper Bound (a.k.a. Theorem One)** – This bound derived from the critical time zone for a set of services released at a critical states that the sum of the service resource requirements must be less than $m(2^{1/m}-1)$ where m is the number of services in the set.
- **RM policy** - services with shorter period are assigned higher priority.
- **ROM Based** - a boot or kernel image which is PIC and initially runs out of a non-volatile device, but tests and initializes memory and then copies itself to working memory and continues execution there.
- **ROM Resident** - a boot or kernel image that executes out of non-volatile memory and sets up a data and stack segment in working memory, but the text segment remains always in the non-volatile memory.
- **Round Robin** - a best effort scheme with preemptive time-slicing where the scheduler assigns threads a slice in a fair fashion where all ready threads are given a slice of CPU and put back on the end of the queue if needed.
- **Sanity Monitor (Software)** - a service which periodically resets the hardware watchdog timer and also monitors keep-alive messages from other critical services in the system - if a critical service fails to post a keep-alive, then the sanity monitor provides error handling and attempts to recover that service - if the sanity monitor itself fails to function, then the hardware watchdog timer will time out and the whole system will reboot and start a system level recovery process.

- **SBE** - Single Bit Error, when an SEU causes a bit flip or other form of unintended bit flip occurs in a memory word.
- **Scatter Write List** - A list of not necessarily contiguous addresses in memory that are to be written from a contiguous buffer - e.g. a host memory may have multiple blocks in memory scattered through memory space that are updated by an I/O device which contains all of the data to be updated in a single contiguous buffer.
- **Scheduler** – A kernel service loop which monitors the Ready Queue and will preempt and dispatch a task in place of the currently running task according to priorities, providing a context switch. The scheduler is executed as a result of making a kernel API call from task and interrupt contexts and also executes in a polling mode when there are not other tasks to execute.
- **Scheduling Point** - a necessary and sufficient test based upon the Sha, Lehoczky, and Ding theorem which determines whether all services can be scheduled within the longest period.
- **SDRAM** - Synchronous Dynamic Random Access Memory.

- **Semaphore** - an RTOS mechanism which can be used for synchronization of otherwise asynchronous tasks in order to coordinate resource usage such as shared memory, or to simply indicate a condition such as data is available on an interface.
- **Semaphore Take** - a semaphore operation which allows a thread to check and see if a resource is available - if not, the RTOS can either block the calling thread until it is, or simply return an error code.
- **Semaphore Give** - a semaphore operation which allows a thread to indicate that a resource is available - if another thread is blocking on this resource, then this will un-block that thread.
- **Sensor** - a transducer device which indicates physical status of a system or the environment in which it operates with an electrical signal to encode the system/environment characteristic it is designed to measure - e.g. a thermistor, a position encoder, limit switch, stress/strain gauge, pressure transducer, ...

- **Service** - a specific computation provided for inputs which produces required output in order to meet a system requirement. Real-time systems include *periodic* or *sporadic* services that are requested on a *periodic* or *sporadic* basis triggered by externally sensed events.
- **Service Release** - when an external event sensed by an embedded system indicates a request for service, the thread which provides the service is released - e.g. an *ISR* can do a semaphore give to indicate sensor data is available for processing.
- **Set Associative Cache** - A *cache* which allows main memory addresses to be loaded in N different cache lines - a set associative cache is said to be N ways, where each way is a different cache line which the same address data may be loaded - e.g. 32 way set associative cache.
- **SEU** - Single Event Upset, a phenomena where a memory bit is flipped due to an environmental influence such as electromagnetic radiation. The bit's original value may be restored if the SEU can be detected and corrected by a system monitoring technique.

- **Shared Interrupt** - when an interrupt can be asserted by multiple devices, it is shared and requires the interrupt handler to poll status - i.e. the handler must read the status of every device that may have asserted the interrupt to figure out which device in fact did.
- **Shared Memory** - when more than one thread on a single CPU or on multiple CPUs can access the same memory locations, this memory is shared, and shared memory must be protected by a synchronization mechanism if reads and writes are allowed.
- **Signal (Software)** - a software signal is often also called a software interrupt and in fact functions much like a hardware interrupt does but at the scheduler/thread level - when a signal is thrown by one thread to another, the throw call causes the RTOS to potentially dispatch the catching thread's handler instead of the code it is currently executing after the catch kernel code is executed - so, a signal can be used to asynchronously interrupt a running thread.
- **Signal Block Diagram** - a systems design method used in SDL (Specification and Description Language) where hardware and software elements can be modeled as blocks with signal list inputs and outputs - inside the blocks at a lower level, all signals are ultimately consumed or generated by *EFSMs*.

- **Signal Catch** - when a signal is received by a thread by the RTOS scheduler on behalf of the thread - the catch modifies the catching thread's state such that the PC, registers, and stack are saved and when the thread is dispatched next, the scheduler dispatches the threads registered signal handler rather than where it was last preempted.
- **Signal Throw** - when a thread wants to asynchronously interrupt the normal flow of execution of another thread, it can call an RTOS mechanism to throw a signal to the other thread instructing the RTOS to dispatch the other thread's signal handler rather than it's last context.
- **Slack Time** - on a real-time system, when no real-time services are requesting CPU time (I.e. waiting on the ready queue or actively running), this unused CPU time is called slack time and often can be used for non real-time best effort processing. Slack time is often created by service releases where the actual execution time taken is much shorter than WCET due to *execution jitter*.
- **SoC** - System On-a-Chip, an ASIC which includes one or more CPU cores, a bus, and I/O interfaces such that it essentially places devices previously on a board in earlier products on a single ASIC.

- **Soft Real-Time** - when a service can occasionally miss a deadline and over-run it or terminate and drop a service release without system failure, these services are considered soft - e.g. a video encoder compression and transport service might occasionally drop a frame when compression takes too long - as long as the video stream is not critical and an occasional drop-out is acceptable w.r.t. system requirements, this service can be considered a soft real-time service.
- **Software Profiling** - periodically tracing the cycle count and the current PC or actively tracing it by instrumenting all function entry and exit points to save cycle count to a trace buffer allows for determination of where most of the execution time is spent and how many cycles basic blocks of code such as functions requires - this type of tracing provides a profile of the software. Profiles can be at a function level, basic code block level (bounded by branches) or at a C statement level - overhead is higher for lower level profiling.
- **Software Sanity** - software is said to be sane when embedded services check in with a sanity monitor by posting a keep-alive - the sanity monitor itself is known to be sane (functioning correctly) if it resets the hardware watchdog timer.
- **Sporadic** – an event that occurs occasionally, singly, or in scattered instances, infrequently, without a deterministic period, but not aperiodic.

- **SRAM** - Static Random Access Memory.
- **S-Reset** - Soft Reset, a reset state for a CPU which can be commanded by an application program.
- **Stack Segment** - a segment of memory allocated for a thread which provides buffer space for function arguments and local variables - each application thread, the kernel thread, ISRs, and signal handlers typically all have their own stack space for the purpose of parameter passing and local variable instantiation.
- **State Machine** - a formal design notation which includes a start state, state transitions driven by inputs made while in a specific state, and outputs on transitions.
- **Static Priority Stereo Vision** - the use of two cameras separated by a known constant distance to judge distances to objects of unknown physical dimensions through the use of triangulation.
- **Stress Testing** - test vectors which are designed to stress the system by going beyond the requirements-based specification for limits - e.g. commanding at high rate, exposure to high voltage ESD, shock testing, and thermal cycling.

- **Superscalar** - A *CPU pipeline* feature that employs parallel hardware within a single CPU core to allow for 2 or more instructions to be fetched, executed and retired concurrently. Note that this feature of a *CPU pipeline* can yield a *CPI* less than 1.0 for the CPU core.
- **Suspended Task** - a VxWorks task state entered when an exception (NMI) is generated by a task - the RTOS handles the exception and suspends the task to protect the system. The suspend state can also be entered explicitly through the taskSuspend API call in VxWorks.
- **SWIC** - Software In Circuit, a technique where software instrumentation is used to trace execution - e.g. logging messages to a file from an application.
- **Switch-Hook** - a VxWorks call-back mechanism where the kernel calls a user function on each and every context switch.
- **Symbol Table** - an array of function and global variable names and addresses where they are stored in their text and data segments respectively.
- **Synchronous** - An event or stimulus that occurs at a specific point in time relative to other events in the system rather than at any time - e.g. a thread of execution can perform a *semaphore take* to synchronize with an *ISR* - the ISR will execute asynchronously, but the processing provided by the thread performing the semaphore take will be *synchronous* since it is known that this processing will only be provided after the *semaphore take* AND the *semaphore give* performed by the *ISR*.

- **Synchronous Bus** - a bus that has clocked address, data, and control cycles.
- **Syndrome** - the encoded bits in an error detection and correction scheme which indicate SBE or MBE and contain the coded bit position that can be used to complement an errant bit for correction of SBEs.
- **System Lifecycle** - the process of turning an embedded system concept into a working maintained system. The steps potentially include: concept, requirements, high-level design, detailed design, implementation of units and subsystems, unit/subsystem test, integration, system test, acceptance testing, fielding, maintenance, and unit/system regression testing.
- **System Test** - end-to-end and feature tests performed after the units and subsystems in a larger system have been unit tested and are integrated for the first time.
- **T (in RMA)** - the period of a service request type. In many cases this will be based upon the worst case frequency of the event(s) that cause a service to be released.
- **Target** - the embedded computing system including the processor complex and all I/O devices.
- **Target Agent** - an embedded service which provides development, debug, and performance analysis features such as cross debugging, code loading and linking, and RTOS event traces.

- **Target Server** - a service on the host development system which provides an interface to host tools and translates user inputs into target agent commands and target agent responses into application data.
- **Task** - a thread with normal thread state including stack, registers, PC, but also including signal handlers, task variables, task ID and name, priority, entry point, and a number of state and inter-task communication data contained in a TCB.
- **Task Spinning** - when a task loops where it is expected to block and wait for a resource before proceeding.
- **Task Wedging** - when a task blocks on a resource indefinitely or is suspended or fails to loop and post a keep-alive periodically.
- **TCB** - Task Control Block, the data structure associated with a VxWorks task which contains all task data in addition to task stack and context.
- **Text Segment (Code Segment)** - a segment of memory used for storing the machine code associated with an application, kernel image, or boot image.
- **TFTP** - Trivial File Transfer Protocol, a simplified FTP (File Transfer Protocol) which allows a client to download files from one known directory in a file system.

- **Thread (of execution)** - a thread is simply the trace of a CPU's *PC* over time not including *context switch* code execution by an *RTOS*. State information may or may not be associated with a thread of execution, but the value of the *PC* before a context switch is the minimum state that must be maintained on a system which includes *preemption*.
- **Thread Safe** – code is thread safe only if it functions as expected when executed simultaneously by multiple threads. A function that is designed to be *reentrant* or a *pure function* is thread safe.
- **Throughput** - an aggregate measure of speed and efficiency for a device - e.g. for a processor the measure is MIPS (Millions of Instructions Per Second) and for an I/O device the measure would be Mbps or Gbps (Mega bits/sec or Giga bits/sec).
- **Tick** - a counter which counts interval timer interrupts and is used by an *RTOS* for basic timer services - e.g. to provide the minimum resolution for timeouts on blocking calls (the *RTOS* will unblock a call made with a timeout specified within tick accuracy).
- **Timeout** - when making a blocking call, in order to avoid “wedging”, where a thread is blocked indefinitely, it is most often advisable to specify a timeout for any blocking call at which time the thread will be asynchronously awoken and will continue execution - this can be done by setting a timer that is set up to throw a signal to a timeout handler prior to making a blocking call if the API does not directly support a timeout option.

- **Timer Services** - an interrupt handler set up by the RTOS which counts ticks on each interval timer interrupt and signals any threads that have reached a timeout threshold.
- **Time-slice** - a unit of CPU called a quantum which can be allocated to a thread in a preemptable best effort system - in these systems timer services often makes a call into the scheduler on each system tick in order to provide quantum preemption - so, the tick, a quantum, and timeout resolution are typically all the same - e.g. Linux/Unix scheduling.
- **Top Half (TH)** - the interface presented to calling threads/tasks/processes by a driver. The Top Half includes thread control features such as blocking (using a semTake most often) and policy such as how many threads it will allow to read/write a device at once. Note that Linux normally defines the BH and TH opposite of the definition provided here.
- **Trace** - a linear buffer with records that include time (cycle count) and state information for a processor core and/or application code.
- **TTL** - Transistor to Transistor Logic - traditional 5v digital logic levels. Also, Time-To-Live - A counter in a datagram that is decremented on each node-to-node hop such that the packet is discarded when TTL=0; this prevents a packet from hopping around the network indefinitely and creating a problem.

- **Unbounded** - when a condition can persist for a non-deterministic amount of time - e.g. unbounded priority inversion where the set of middle level priority interference tasks may cause the inversion to persist for an arbitrary time.
- **Unit Test** - a test designed to validate and verify a software and/or hardware unit that is a building block for a larger system in isolation.
- **Utility Curve** - an XY graph which shows time on the X axis between a service release and relative deadline and shows utility or damage caused to the system caused by service response generation.
- **Virtual Timer** - a timer which is not directly supported by a hardware interval timer, but rather is a software tick counter that can generate a signal after the passing of N software ticks.
- **VoIP** - Voice over IP, a protocol for transporting voice duplex audio over the Internet protocol.
- **Watchdog Timer** - a hardware based interval timer which counts down (or up) and when it reaches zero (or all F's) it generates an *H-reset* signal causing the system to re-boot - critical software services are expected to post keep-alives to a system sanity monitor which normally in turn resets the watchdog timer before it expires. If the software loses sanity, i.e. the sanity monitor fails to reset the watchdog timer (e.g. if a deadlock were to occur), then the idea is that the system will be able to recover by re-booting.

- **WCET** - Worst Case Execution Time, the longest number of CPU cycles required by a service release ever observed and/or theoretically possible given the hardware architecture and algorithm for data processing used.
- **Wear Leveling** - a flash file system method to ensure that maximum capacity and operational longevity is maintained in a flash device which hosts a filesystem - since flash is divided into sectors, with each sector having a maximum expected number of erase/write cycles, this method attempts to keep erase counts for all sectors approximately the same so no one sector wears out early.
- **White-Box Test** - a set of test vectors which drive specific execution paths in a software unit by design so that the software unit test meets specific path, statement, condition, and/or decision coverage criteria - such tests require intimate knowledge of the software unit such as API return codes, error conditions, and I/O ranges.
- **Worst-Case Response Time** – The sum of WCET, Input-Latency, Dispatch Latency, Interference, and Output Latency for a Service Release.
- **Write-Back** - when a processor updates memory from registers or cache.
- **Write-Through** - when a processor maintains cache/memory coherency by always writing cache and the corresponding memory location on all writes to locations which are cached.
- **Yield** – when a thread of execution gives up the CPU resource voluntarily through a system API call – e.g. in VxWorks pause(). Yields may include transition from executing to pending, delayed, or suspended states. Note: In a priority preemption, a thread will transition from executing to ready.