Note:

-In embedded system we use memory mapped.

-Every device (GPIO)range of addresses (base address + offset).

-any peripheral >>> (hardware circuit + registers).

TRM >> technical reference manual has specs inside it.

Specs has:

-Section memory mapped >> has the start and the end of addressed of each peripheral.

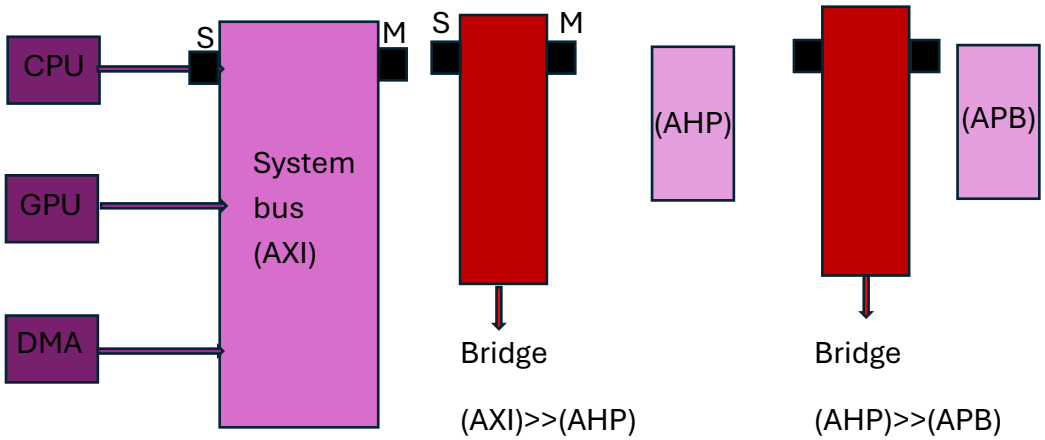
GPIO >>BASE
>>END

-Every register in the peripheral has the base address and an offset.

EX: GPIO

-DR >> 0X0+BASE
-ODR >>0X4+BASE
-IR >>0X8+BASE

Bus bridges:



Hardware port:

Has two types

1-**master**: initiate transaction (R/W)>> add + data +size

2-**slave.**

AMBA (the arm advanced MC bus architecture):

We want the Reusability to be high, so we make standard AMBA

Bus >> latency and BW

Clock tree:

c/k >> 80M >>>>40M>>20M

-If the clock is greater than the frequency of the buses and CPU the system fails.

-We can't work on the max frequency of all the buses as the power increases with the increase of frequency.

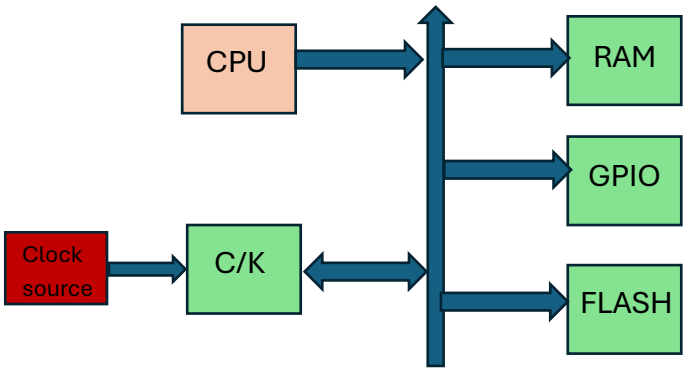
-**In MC:**

Most of them have: -power management unit. -clock management unit.

General topology of the clock architecture (system clock):

Note:

the clock must be master for the other peripheral as it allows to open the clock or not and at the same time it is a slave for CPU.



External clock:

-RC/CHIP >> one pin.

-CRYSTAL >>two pin.