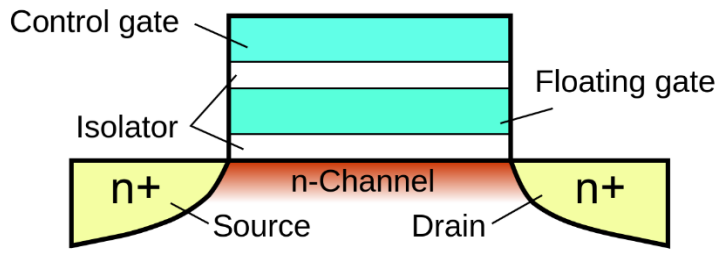
❖ Nonvolatile memory (ROM):

-Program memory (the code on it).

-Access time in rom is greater than in ram.

-Rom based on FGM (floating gate mosfet).



The floating gate has two states:

1-**programing state:** means there is a negative charge (make the bit equal 0).

2-**erasing state:** means there is no charge (positive charge) (make the bit equal 1).

- **Note:**
  -The charge in the floating gate is stuck until we apply high voltage on the drain.

  -Rom is read only memory for microprocessor.

Types of rom:

a-mask programable rom:

-Once you apply a code you can't modify it if there is bug in runtime.

-the factory already applies the code in it.

-OTP>>one time program.

Ex: bios chip.

b-PROM (programable ROM)

-OTP, consists of fuses, the user apply the code in it.

c-EPROM (erasable programable rom):

-erasable by ultraviolet.

Adv: erasable, nonvolatile

Dis: affected by noise and radiation(corruption).

❖ Hybrid memory:

-Take the adv of RAM (read and write) and the adv of ROM (nonvolatile).

Types:

a-EEPROM (electrical erasable programable rom):

-erase by electricity.

-Endurance (can write and erase up to):100000

-Byte access.

-high cost per bit.

Types

1-internal (inside the MCU).

2-external (connected through communication protocols).

b-flash:

-block access (sector by sector) number of bytes

- Endurance (can write and erase up to):10000

-low cost per bit.

c-NVRAM:

(SRAM +battery) or (SRAM +EEROM +battery).

❖ Cache memory (SRAM):

CPU<< >> cache << >> RAM.

-The cache has levels.

-every cache has a controller in it.

Cache coherence: if any of the cache change variable in ram it will tell the other caches.

Register files >>> cache memory >>> RAM >>> HDD.

Hit ratio:

Number of hits divided by the total (hit + miss).

FPU (floating point unit):

Can be inside the microprocessor or outside.

MPU (memory protection unit):

-put between cache and ram.

-Divide the RAM to ranges based on the operating system.

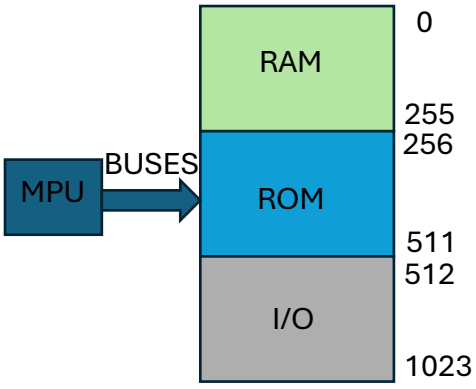
MMU (memory management unit)

❖ Architecture:

1-VON-NEUMEN:

-One memory system.

-We can't talk to ROM and RAM at the same time.

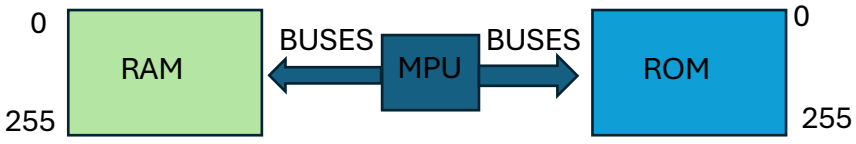


2-harvard:

-We can talk to ROM and RAM at the same time.

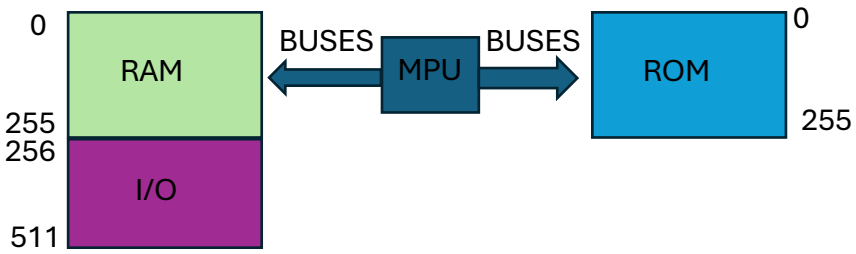
-But how do we know if we talk to RAM, or we talk to ROM??

By software for RAM (load/store), ROM(R/W)

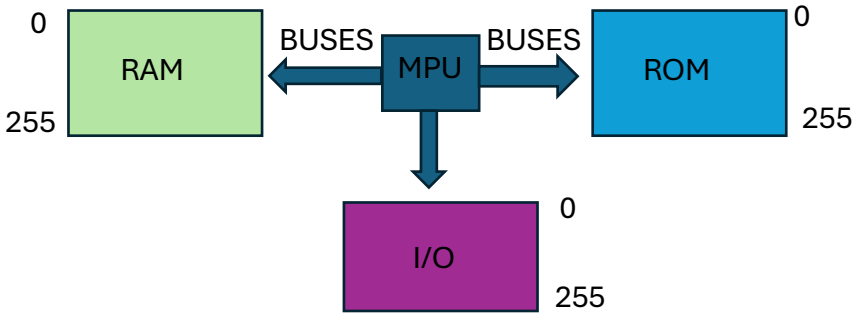


I/O on Harvard:

1- the I/O are connected with RAM or ROM by memory mapped.



2-the I/O are connected with MPU by port mapped.



- **Note:**

-VON-NEUMEN is used in PC, but Harvard used it in MC.

-VON-NEUMEN can't support pipelining, but Harvard does.

-CISC can't support pipelining, but RISC does.

MIPS: million instructions (assembly INST) per second.

❖ Clock systems:

1-electrical:

RC-OSCILLATER.

2-mechanical:

-Material has electrical power as an input and output square wave.

Has two types: a-ceramic resonator. b-crystal oscillator.

	RC	ceramic resonator	crystal oscillator
▪ Cost	low	medium	high
▪ Accuracy	low	medium	high
▪ Settling T	high	medium	low
▪ Noise IMM			
a-Temp	low	high	high
b-EMI	low	high	high
c-VIBR	high	low	low