Cairo University
Faculty of Engineering
Computer Engineering

Computer Architecture
Lab 3

You are required to build the following:

- A register file which contains **7 registers**, each register has **12-bits widths**.

  The register file has:

  - **2**-read addresses and **2**-write address.
  - **2**-read ports and **2**-write port.
  - write enables and reset signal.

  (What is the size of address bus? What is the size of data bus?)
- Use the given registers (DFF) to create the register files.
- Create testbench to do the following:
  - **Reset** all registers, set all read addresses to zero.
  - **Read** Reg(0) on port 0, **Read** Reg(1) on port 1, **Write** 0x0F0 to Reg(0), **Write** 0xAAA to Reg(3).
  - **Read** Reg(4) on port 0, **Read** Reg(3) on port 1, **Write** 0x123 to Reg(6), **Write** 0xCCC to Reg(1).
  - **Read** Reg(1) on port 0, **Read** Reg(6) on port 1, **Write** 0x456 to Reg(4), **Don't write** on the 2nd port.
  - **Read** Reg(6) on port 0, **Read** Reg(0) on port 1, **Don't write** on the 1st port, **Write** 0x789 to Reg(1).
  - **Read** Reg(1) on port 0, **Read** Reg(2) on port 1, **Don't write** anything.
  - **Read** Reg(3) on port 0, **Read** Reg(4) on port 1, **Don't write** anything.

Assignment:

- Create the same register file using memory arrays instead of DFFs.
- Test your new register file using the same testbench.
- Use Quartus to generate RTL view for both designs to compare them.

Expected Output:

CYCLE#	Read Port 0	Read Port 1
1	**000**	**000**
2	**0F0**	**000**
3	**000**	**AAA**
4	**CCC**	**123**
5	**123**	**0F0**
6	**789**	**000**
7	**AAA**	**456**