**Snippets for the implemented**

Welcome | Uart_packet.sv U | Testbench.sv U | run.do U

Assigment4 > Testbench.sv

```
module uart_tb(uart_if.TEST interface_test);
    import enum_pkg::*;
    import uart_packet::*;

    functionsImp func_imp;
    covergroup_class cg_inst;
    bit [9:0] actual_queue[$];
    bit [9:0] expected_value[$];

    initial begin
        func_imp = new();
        cg_inst  = new();

        do begin
            @(negedge interface_test.tx_busy);
            generate_stimulus(func_imp);
            drivestim(func_imp);
            collect_output(func_imp);
            golden_model(expected_value);
            check_output(actual_queue, expected_value);
        end while (cg_inst.cg.get_coverage() < 100);

        $display("Coverage Reached 100");
        $stop;
    end

    function automatic void generate_stimulus(ref functionsImp f);
        assert (f.randomize()) else begin
            $display("Randomization failed!");
            $stop;
        end
    endfunction

    task automatic drivestim(ref functionsImp f);
        @(negedge interface_test.clk);
        interface_test.data_in     = f.data_in;
        interface_test.parity_en   = f.parity_en;
```

Welcome | Uart_packet.sv U | Testbench.sv U | run.do U

Assigment4 > Testbench.sv

```
module uart_tb(uart_if.TEST interface_test);
    task automatic drivestim(ref functionsImp f);
        interface_test.even_parity = f.even_parity;
        interface_test.tx_start    = 1;
        @(negedge interface_test.clk);
        interface_test.tx_start    = 0;

        cg_inst.sample(f);
    endtask

    function automatic void golden_model(ref bit [9:0] expected_value[$]);
        expected_value.delete();
        expected_value.push_back(0); // Start bit
        for (int j = 0; j < 8; j++) begin
            expected_value.push_back(interface_test.data_in[j]);
        end
        if (interface_test.parity_en) begin
            bit par_value = (interface_test.even_parity) ? ~(^interface_test.data_in) : (^interface_test.data_in);
            expected_value.push_back(par_value);
        end
        expected_value.push_back(1); // Stop bit
    endfunction

    task automatic collect_output(ref functionsImp f);
        logic [10:0] collected;
        int i;
        int bits_to_collect = f.parity_en ? 11 : 10;

        @(posedge interface_test.clk);
        for (i = 0; i < bits_to_collect; i++) begin
            @(negedge interface_test.clk);
            collected[i] = interface_test.tx;
        end
        if (!f.parity_en) collected[10] = 1;
        actual_queue.push_back(collected);
    endtask
```

Welcome | Uart_packet.sv U | Testbench.sv U | run.do U

Assigment4 > Testbench.sv

```
module uart_tb(uart_if.TEST interface_test);
    task automatic collect_output(ref functionsImp f);
        for (i = 0; i < bits_to_collect; i++) begin
            @(negedge interface_test.clk);
            collected[i] = interface_test.tx;
        end
        if (!f.parity_en) collected[10] = 1;
        actual_queue.push_back(collected);
    endtask

    function automatic void check_output(ref bit [9:0] actual_queue[$], ref bit [9:0] expected_value[$]);
        if (actual_queue.size() != expected_value.size()) begin
            $display("Mismatch in size: Actual = %0d, Expected = %0d", actual_queue.size(), expected_value.size());
            return;
        end
        for (int i = 0; i < actual_queue.size(); i++) begin
            if (actual_queue[i] !== expected_value[i]) begin
                $display("Mismatch at index %0d: Actual = %b, Expected = %b", i, actual_queue[i], expected_value[i]);
                return;
            end
        end
        $display("UART frame matched expected output.");
    endfunction
endmodule
```

## Snippets for functional coverage report

Coverage Report by instance with details

```
================================================================================
===============
=== Instance: /top/tb_if_inst
=== Design Unit: work.uart_if
================================================================================
===============
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         30         4        26    13.33%
```

```
================================Toggle
Details================================

Toggle Coverage for instance /top/tb_if_inst --

                                  Node      1H->0L      0L->1H  "Coverage"
                                 --------------------------------------
                            data_in[0-7]          0           0        0.00
                             even_parity          0           0        0.00
                               parity_en          0           0        0.00
                                   rst_n          0           1       50.00
                                      tx          0           0        0.00
                                tx_busy           0           0        0.00
                                tx_start          1           0       50.00

Total Node Count     =        15
Toggled Node Count   =         1
Untoggled Node Count =        14

Toggle Coverage      =     13.33% (4 of 30 bins)

================================================================================
===============
=== Instance: /top/uart_top
=== Design Unit: work.uart_tx
================================================================================
===============
Branch Coverage:
    Enabled Coverage             Bins      Hits    Misses  Coverage
    ----------------             ----      ----    ------  --------
    Branches                       16         4        12    25.00%

================================Branch
Details================================

Branch Coverage for instance /top/uart_top

    Line         Item                    Count     Source
    ----         ----                    -----     ------
  File uart_tx.sv
-----------------------------------IF Branch-----------------------------------
    15                                       4     Count coming in to IF
    15              1                        3
    22              1                        1
Branch totals: 2 hits of 2 branches = 100.00%

---------------------------------CASE Branch-----------------------------------
    23                                       1     Count coming in to CASE
    24              1                        1
    35              1                    ***0***
    39              1                    ***0***
    50              1                    ***0***
    54              1                    ***0***
                                         ***0***     All False Count
Branch totals: 1 hit of 6 branches = 16.66%

-----------------------------------IF Branch-----------------------------------
```

```
   27                                1     Count coming in to IF
   27            1                ***0***
                                    1     All False Count
Branch totals: 1 hit of 2 branches = 50.00%

------------------------------------IF Branch------------------------------------
   30                               ***0***     Count coming in to IF
   30            1                  ***0***
   30            2                  ***0***
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
   43                               ***0***     Count coming in to IF
   43            1                  ***0***
                                   ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
   44                               ***0***     Count coming in to IF
   44            1                  ***0***
   46            1                  ***0***
Branch totals: 0 hits of 2 branches = 0.00%


Condition Coverage:
   Enabled Coverage            Bins   Covered    Misses  Coverage
   ----------------            ----      ----    ------  --------
   Conditions                     1         0         1     0.00%

================================Condition
Details================================

Condition Coverage for instance /top/uart_top --

  File uart_tx.sv
----------------Focused Condition View-------------------
Line       43 Item    1  (bit_cnt == 7)
Condition totals: 0 of 1 input term covered = 0.00%

     Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  ----------------------  --------------
  (bit_cnt == 7)        N  No hits                 Hit '_0' and '_1'

    Rows:       Hits  FEC Target           Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (bit_cnt == 7)_0      -
  Row   2:    ***0***  (bit_cnt == 7)_1      -


Expression Coverage:
   Enabled Coverage            Bins   Covered    Misses  Coverage
   ----------------            ----      ----    ------  --------
   Expressions                    3         0         3     0.00%

================================Expression
Details================================
```

Expression Coverage for instance /top/uart_top --

File uart_tx.sv
----------Focused Expression View (Bimodal)----------
Line 30 Item 1 (even_parity? ~^data_in: ^data_in)
Expression totals: 0 of 3 input terms covered = 0.00%

| Input Term | Covered | Reason for no coverage | Hint |
|---|---|---|---|
| even_parity | N | No hits | Hit '_0' and '_1' for different outputs |
| ~^data_in | N | No hits | Hit '_0' and '_1' for different outputs |
| ^data_in | N | No hits | Hit '_0' and '_1' for different outputs |

| Rows: | Hits(->0) | Hits(->1) | FEC Target | Non-masking condition(s) |
|---|---|---|---|---|
| Row 1: | 0 | 0 | even_parity_0 | - |
| Row 2: | 0 | 0 | even_parity_1 | - |
| Row 3: | 0 | 0 | ~^data_in_0 | even_parity |
| Row 4: | 0 | 0 | ~^data_in_1 | even_parity |
| Row 5: | 0 | 0 | ^data_in_0 | ~even_parity |
| Row 6: | 0 | 0 | ^data_in_1 | ~even_parity |

FSM Coverage:

| Enabled Coverage | Bins | Hits | Misses | Coverage |
|---|---|---|---|---|
| FSM States | 5 | 1 | 4 | 20.00% |
| FSM Transitions | 9 | 0 | 9 | 0.00% |

==========FSM Details==========

FSM Coverage for instance /top/uart_top --

FSM_ID: state
Current State Object : state
---
State Value MapInfo :
---

| Line | State Name | Value |
|---|---|---|
| 24 | IDLE | 0 |
| 35 | START | 1 |
| 39 | DATA | 2 |
| 54 | STOP | 4 |
| 50 | PARITY | 3 |

Covered States :
---

| State | Hit_count |
|---|---|
| IDLE | 3 |

Uncovered States :
---

| State |
|---|
| START |

DATA
STOP
PARITY

Uncovered Transitions :

---

| Line | Trans_ID | Transition |
|---|---|---|
| 32 | 0 | IDLE -> START |
| 37 | 1 | START -> DATA |
| 16 | 2 | START -> IDLE |
| 47 | 3 | DATA -> STOP |
| 45 | 4 | DATA -> PARITY |
| 16 | 5 | DATA -> IDLE |
| 56 | 6 | STOP -> IDLE |
| 52 | 7 | PARITY -> STOP |
| 16 | 8 | PARITY -> IDLE |

| Summary | Bins | Hits | Misses | Coverage |
|---|---|---|---|---|
| FSM States | 5 | 1 | 4 | 20.00% |
| FSM Transitions | 9 | 0 | 9 | 0.00% |

Statement Coverage:

| Enabled Coverage | Bins | Hits | Misses | Coverage |
|---|---|---|---|---|
| Statements | 25 | 9 | 16 | 36.00% |

==========Statement Details==========

Statement Coverage for instance /top/uart_top --

| Line | Item | Count | Source |
|---|---|---|---|
| File uart_tx.sv | | | |
| 14 | 1 | 4 | |
| 16 | 1 | 3 | |
| 17 | 1 | 3 | |
| 18 | 1 | 3 | |
| 19 | 1 | 3 | |
| 20 | 1 | 3 | |
| 21 | 1 | 3 | |
| 25 | 1 | 1 | |
| 26 | 1 | 1 | |
| 28 | 1 | ***0*** | |
| 29 | 1 | ***0*** | |
| 30 | 1 | ***0*** | |
| 31 | 1 | ***0*** | |
| 32 | 1 | ***0*** | |
| 36 | 1 | ***0*** | |
| 37 | 1 | ***0*** | |
| 40 | 1 | ***0*** | |
| 41 | 1 | ***0*** | |
| 42 | 1 | ***0*** | |
| 45 | 1 | ***0*** | |
| 47 | 1 | ***0*** | |
| 51 | 1 | ***0*** | |

```
   52             1                ***0***
   55             1                ***0***
   56             1                ***0***
Toggle Coverage:
   Enabled Coverage            Bins      Hits    Misses  Coverage
   ----------------            ----      ----    ------  --------
   Toggles                       32         0        32     0.00%

================================Toggle
Details================================

Toggle Coverage for instance /top/uart_top --

                                    Node      1H->0L      0L->1H  "Coverage"
                                    ----------------------------------------
                                bit_cnt[0-3]          0           0        0.00
                                  parity_bit          0           0        0.00
                               shift_reg[0-7]           0           0        0.00
                                  state[0-2]           0           0        0.00

Total Node Count     =         16
Toggled Node Count   =          0
Untoggled Node Count =         16

Toggle Coverage      =       0.00% (0 of 32 bins)

=================================================================
===============
=== Instance: /top/uart_tb_top
=== Design Unit: work.uart_tb
=================================================================
===============

Assertion Coverage:
   Assertions                    1         1         0   100.00%
----------------------------------------------------------------
Name                File(Line)                Failure      Pass
                                                Count        Count
----------------------------------------------------------------
/top/uart_tb_top/generate_stimulus/immed__28
                  testbench.sv(28)                    0         1
Branch Coverage:
   Enabled Coverage            Bins      Hits    Misses  Coverage
   ----------------            ----      ----    ------  --------
   Branches                      12         4         8    33.33%

================================Branch
Details================================

Branch Coverage for instance /top/uart_tb_top

   Line         Item                    Count     Source
   ----         ----                    -----     ------
  File testbench.sv
------------------------------------IF Branch------------------------------------
   52                                      1     Count coming in to IF
   52             1                ***0***
```

```
                                    1     All False Count
Branch totals: 1 hit of 2 branches = 50.00%

------------------------------------IF Branch------------------------------------
   53                              ***0***     Count coming in to IF
   53            1                  ***0***
   53            2                  ***0***
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
   62                                 1     Count coming in to IF
   62            1                  ***0***
   62            2                    1
Branch totals: 1 hit of 2 branches = 50.00%

------------------------------------IF Branch------------------------------------
   69                                 1     Count coming in to IF
   69            1                    1
                                   ***0***     All False Count
Branch totals: 1 hit of 2 branches = 50.00%

------------------------------------IF Branch------------------------------------
   74                                 1     Count coming in to IF
   74            1                    1
                                   ***0***     All False Count
Branch totals: 1 hit of 2 branches = 50.00%

------------------------------------IF Branch------------------------------------
   79                              ***0***     Count coming in to IF
   79            1                  ***0***
                                   ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%


Condition Coverage:
   Enabled Coverage            Bins   Covered    Misses  Coverage
   ----------------            ----      ----    ------  --------
   Conditions                     3         0         3     0.00%

================================Condition
Details================================

Condition Coverage for instance /top/uart_tb_top --

  File testbench.sv
----------------Focused Condition View-------------------
Line       21 Item    1  (get_coverage(#dummy_covered_bins#,#dummy_total_bins#) <
100)
Condition totals: 0 of 1 input term covered = 0.00%

                                        Input Term   Covered  Reason for no coverage   Hint
                                       -----------  --------  ----------------------  --------------
  (get_coverage(#dummy_covered_bins#,#dummy_total_bins#) < 100)         N  '_0' not
hit             Hit '_0'

    Rows:       Hits  FEC Target                                        Non-masking
condition(s)
```

```
 ---------  ---------  --------------------                                    ------------------------
  Row   1:    ***0***  (get_coverage(#dummy_covered_bins#,#dummy_total_bins#) <
100)_0  -
  Row   2:          1  (get_coverage(#dummy_covered_bins#,#dummy_total_bins#) <
100)_1  -

----------------Focused Condition View-------------------
Line       74 Item    1  (size(actual_queue) != size(expected_value))
Condition totals: 0 of 1 input term covered = 0.00%

                            Input Term   Covered  Reason for no coverage   Hint
                           -----------  --------  ----------------------  --------------
  (size(actual_queue) != size(expected_value))         N  '_0' not hit            Hit '_0'

    Rows:       Hits  FEC Target                              Non-masking condition(s)
 ---------  ---------  --------------------                   ------------------------
  Row   1:    ***0***  (size(actual_queue) != size(expected_value))_0  -
  Row   2:          1  (size(actual_queue) != size(expected_value))_1  -

----------------Focused Condition View-------------------
Line       79 Item    1  (actual_queue[i] !== expected_value[i])
Condition totals: 0 of 1 input term covered = 0.00%

                          Input Term   Covered  Reason for no coverage   Hint
                         -----------  --------  ----------------------  --------------
  (actual_queue[i] !== expected_value[i])         N  No hits                 Hit '_0' and '_1'

    Rows:       Hits  FEC Target                              Non-masking condition(s)
 ---------  ---------  --------------------                   ------------------------
  Row   1:    ***0***  (actual_queue[i] !== expected_value[i])_0  -
  Row   2:    ***0***  (actual_queue[i] !== expected_value[i])_1  -


Expression Coverage:
    Enabled Coverage            Bins   Covered    Misses  Coverage
    ----------------            ----     ----    ------  --------
    Expressions                    3        0         3     0.00%

================================Expression
Details================================

Expression Coverage for instance /top/uart_tb_top --

  File testbench.sv
-----------Focused Expression View (Bimodal)------------
Line       53 Item    1  (even_parity? ~^data_in: ^data_in)
Expression totals: 0 of 3 input terms covered = 0.00%

     Input Term   Covered  Reason for no coverage                Hint
    -----------  --------  ------------------------------------  --------------
    even_parity         N  No hits                          Hit '_0' and '_1' for different outputs
      ~^data_in         N  No hits                          Hit '_0' and '_1' for different outputs
       ^data_in         N  No hits                          Hit '_0' and '_1' for different outputs

    Rows:   Hits(->0)   Hits(->1)  FEC Target           Non-masking condition(s)

---------  ----------  ----------  --------------------  ------------------------
```

| | | | | | |
|---|---|---|---|---|---|
| Row | 1: | 0 | 0 | even_parity_0 | - |
| Row | 2: | 0 | 0 | even_parity_1 | - |
| Row | 3: | 0 | 0 | ~^data_in_0 | even_parity |
| Row | 4: | 0 | 0 | ~^data_in_1 | even_parity |
| Row | 5: | 0 | 0 | ^data_in_0 | ~even_parity |
| Row | 6: | 0 | 0 | ^data_in_1 | ~even_parity |

Statement Coverage:

| Enabled Coverage | Bins | Hits | Misses | Coverage |
|---|---|---|---|---|
| Statements | 42 | 33 | 9 | 78.57% |

==========Statement Details==========

Statement Coverage for instance /top/uart_tb_top --

| Line | Item | Count | Source |
|---|---|---|---|
| File testbench.sv | | | |
| 11 | 1 | 1 | |
| 12 | 1 | 1 | |
| 14 | 1 | 1 | |
| 15 | 1 | 2 | |
| 16 | 1 | 1 | |
| 17 | 1 | 1 | |
| 18 | 1 | 1 | |
| 19 | 1 | 1 | |
| 20 | 1 | 1 | |
| 23 | 1 | ***0*** | |
| 24 | 1 | ***0*** | |
| 35 | 1 | 1 | |
| 36 | 1 | 1 | |
| 37 | 1 | 1 | |
| 38 | 1 | 1 | |
| 39 | 1 | 1 | |
| 40 | 1 | 1 | |
| 41 | 1 | 1 | |
| 43 | 1 | 1 | |
| 47 | 1 | 1 | |
| 48 | 1 | 1 | |
| 49 | 1 | 1 | |
| 49 | 2 | 8 | |
| 50 | 1 | 8 | |
| 53 | 1 | ***0*** | |
| 54 | 1 | ***0*** | |
| 56 | 1 | 1 | |
| 62 | 1 | 1 | |
| 64 | 1 | 1 | |
| 65 | 1 | 1 | |
| 65 | 2 | 10 | |
| 66 | 1 | 10 | |
| 67 | 1 | 10 | |
| 69 | 1 | 1 | |
| 70 | 1 | 1 | |
| 75 | 1 | 1 | |

```
   76            1                    1
   78            1                ***0***
   78            2                ***0***
   80            1                ***0***
   81            1                ***0***
   84            1                ***0***

================================================================
===============
=== Instance: /top
=== Design Unit: work.top
================================================================
===============
Statement Coverage:
   Enabled Coverage            Bins      Hits    Misses  Coverage
   ----------------            ----      ----    ------  --------
   Statements                    9         9         0   100.00%

================================Statement
Details================================

Statement Coverage for instance /top --

   Line         Item                   Count     Source
   ----         ----                   -----     ------
  File top.sv
   4             1                 11646398
   4             2                 11646397
   11            1                        1
   12            1                        1
   12            2                 116463971
   12            3                 116463970
   16            1                        1
   17            1                        1
   17            2                        1
Toggle Coverage:
   Enabled Coverage            Bins      Hits    Misses  Coverage
   ----------------            ----      ----    ------  --------
   Toggles                       4         3         1    75.00%

================================Toggle
Details================================

Toggle Coverage for instance /top --

                                  Node      1H->0L      0L->1H  "Coverage"
                                  ----------------------------------------
                                  rst_n          0           1       50.00

Total Node Count     =         2
Toggled Node Count   =         1
Untoggled Node Count =         1

Toggle Coverage      =      75.00% (3 of 4 bins)

================================================================
===============
```

```
=== Instance: /uart_packet
=== Design Unit: work.uart_packet
================================================================================
===============

Covergroup Coverage:
    Covergroups                 1        na        na    20.07%
        Coverpoints/Crosses     5        na        na        na
            Covergroup Bins   266         3       263     1.12%
--------------------------------------------------------------------------------------------------------------
Covergroup                                    Metric       Goal       Bins    Status

--------------------------------------------------------------------------------------------------------------
 TYPE /uart_packet/covergroup_class/cg                20.07%        100          -
Uncovered
    covered/total bins:                                  3        266          -
    missing/total bins:                                263        266          -
    % Hit:                                          1.12%        100          -
    Coverpoint cp1                                  0.39%        100          -    Uncovered
        covered/total bins:                              1        256          -
        missing/total bins:                            255        256          -
        % Hit:                                      0.39%        100          -
        bin all_values[0]                                0          1          -    ZERO
        bin all_values[1]                                0          1          -    ZERO
        bin all_values[2]                                0          1          -    ZERO
        bin all_values[3]                                0          1          -    ZERO
        bin all_values[4]                                0          1          -    ZERO
        bin all_values[5]                                0          1          -    ZERO
        bin all_values[6]                                0          1          -    ZERO
        bin all_values[7]                                0          1          -    ZERO
        bin all_values[8]                                0          1          -    ZERO
        bin all_values[9]                                0          1          -    ZERO
        bin all_values[10]                               0          1          -    ZERO
        bin all_values[11]                               0          1          -    ZERO
        bin all_values[12]                               0          1          -    ZERO
        bin all_values[13]                               0          1          -    ZERO
        bin all_values[14]                               0          1          -    ZERO
        bin all_values[15]                               0          1          -    ZERO
        bin all_values[16]                               0          1          -    ZERO
        bin all_values[17]                               0          1          -    ZERO
        bin all_values[18]                               0          1          -    ZERO
        bin all_values[19]                               0          1          -    ZERO
        bin all_values[20]                               0          1          -    ZERO
        bin all_values[21]                               0          1          -    ZERO
        bin all_values[22]                               0          1          -    ZERO
        bin all_values[23]                               0          1          -    ZERO
        bin all_values[24]                               0          1          -    ZERO
        bin all_values[25]                               0          1          -    ZERO
        bin all_values[26]                               0          1          -    ZERO
        bin all_values[27]                               0          1          -    ZERO
        bin all_values[28]                               0          1          -    ZERO
        bin all_values[29]                               0          1          -    ZERO
        bin all_values[30]                               0          1          -    ZERO
        bin all_values[31]                               0          1          -    ZERO
        bin all_values[32]                               0          1          -    ZERO
        bin all_values[33]                               0          1          -    ZERO
        bin all_values[34]                               0          1          -    ZERO
```

| | | | | |
|---|---|---|---|---|
| bin all_values[35] | 0 | 1 | - | ZERO |
| bin all_values[36] | 0 | 1 | - | ZERO |
| bin all_values[37] | 0 | 1 | - | ZERO |
| bin all_values[38] | 0 | 1 | - | ZERO |
| bin all_values[39] | 0 | 1 | - | ZERO |
| bin all_values[40] | 0 | 1 | - | ZERO |
| bin all_values[41] | 0 | 1 | - | ZERO |
| bin all_values[42] | 0 | 1 | - | ZERO |
| bin all_values[43] | 0 | 1 | - | ZERO |
| bin all_values[44] | 0 | 1 | - | ZERO |
| bin all_values[45] | 0 | 1 | - | ZERO |
| bin all_values[46] | 0 | 1 | - | ZERO |
| bin all_values[47] | 0 | 1 | - | ZERO |
| bin all_values[48] | 0 | 1 | - | ZERO |
| bin all_values[49] | 0 | 1 | - | ZERO |
| bin all_values[50] | 0 | 1 | - | ZERO |
| bin all_values[51] | 0 | 1 | - | ZERO |
| bin all_values[52] | 0 | 1 | - | ZERO |
| bin all_values[53] | 0 | 1 | - | ZERO |
| bin all_values[54] | 0 | 1 | - | ZERO |
| bin all_values[55] | 0 | 1 | - | ZERO |
| bin all_values[56] | 0 | 1 | - | ZERO |
| bin all_values[57] | 0 | 1 | - | ZERO |
| bin all_values[58] | 0 | 1 | - | ZERO |
| bin all_values[59] | 0 | 1 | - | ZERO |
| bin all_values[60] | 0 | 1 | - | ZERO |
| bin all_values[61] | 0 | 1 | - | ZERO |
| bin all_values[62] | 0 | 1 | - | ZERO |
| bin all_values[63] | 0 | 1 | - | ZERO |
| bin all_values[64] | 0 | 1 | - | ZERO |
| bin all_values[65] | 0 | 1 | - | ZERO |
| bin all_values[66] | 0 | 1 | - | ZERO |
| bin all_values[67] | 0 | 1 | - | ZERO |
| bin all_values[68] | 0 | 1 | - | ZERO |
| bin all_values[69] | 0 | 1 | - | ZERO |
| bin all_values[70] | 0 | 1 | - | ZERO |
| bin all_values[71] | 0 | 1 | - | ZERO |
| bin all_values[72] | 0 | 1 | - | ZERO |
| bin all_values[73] | 0 | 1 | - | ZERO |
| bin all_values[74] | 0 | 1 | - | ZERO |
| bin all_values[75] | 0 | 1 | - | ZERO |
| bin all_values[76] | 0 | 1 | - | ZERO |
| bin all_values[77] | 0 | 1 | - | ZERO |
| bin all_values[78] | 0 | 1 | - | ZERO |
| bin all_values[79] | 0 | 1 | - | ZERO |
| bin all_values[80] | 0 | 1 | - | ZERO |
| bin all_values[81] | 0 | 1 | - | ZERO |
| bin all_values[82] | 0 | 1 | - | ZERO |
| bin all_values[83] | 0 | 1 | - | ZERO |
| bin all_values[84] | 0 | 1 | - | ZERO |
| bin all_values[85] | 0 | 1 | - | ZERO |
| bin all_values[86] | 0 | 1 | - | ZERO |
| bin all_values[87] | 0 | 1 | - | ZERO |
| bin all_values[88] | 0 | 1 | - | ZERO |
| bin all_values[89] | 0 | 1 | - | ZERO |
| bin all_values[90] | 0 | 1 | - | ZERO |
| bin all_values[91] | 0 | 1 | - | ZERO |

| | | | | |
|---|---|---|---|---|
| bin all_values[92] | 0 | 1 | - | ZERO |
| bin all_values[93] | 0 | 1 | - | ZERO |
| bin all_values[94] | 0 | 1 | - | ZERO |
| bin all_values[95] | 0 | 1 | - | ZERO |
| bin all_values[96] | 0 | 1 | - | ZERO |
| bin all_values[97] | 0 | 1 | - | ZERO |
| bin all_values[98] | 0 | 1 | - | ZERO |
| bin all_values[99] | 0 | 1 | - | ZERO |
| bin all_values[100] | 0 | 1 | - | ZERO |
| bin all_values[101] | 0 | 1 | - | ZERO |
| bin all_values[102] | 0 | 1 | - | ZERO |
| bin all_values[103] | 0 | 1 | - | ZERO |
| bin all_values[104] | 0 | 1 | - | ZERO |
| bin all_values[105] | 0 | 1 | - | ZERO |
| bin all_values[106] | 0 | 1 | - | ZERO |
| bin all_values[107] | 0 | 1 | - | ZERO |
| bin all_values[108] | 1 | 1 | - | Covered |
| bin all_values[109] | 0 | 1 | - | ZERO |
| bin all_values[110] | 0 | 1 | - | ZERO |
| bin all_values[111] | 0 | 1 | - | ZERO |
| bin all_values[112] | 0 | 1 | - | ZERO |
| bin all_values[113] | 0 | 1 | - | ZERO |
| bin all_values[114] | 0 | 1 | - | ZERO |
| bin all_values[115] | 0 | 1 | - | ZERO |
| bin all_values[116] | 0 | 1 | - | ZERO |
| bin all_values[117] | 0 | 1 | - | ZERO |
| bin all_values[118] | 0 | 1 | - | ZERO |
| bin all_values[119] | 0 | 1 | - | ZERO |
| bin all_values[120] | 0 | 1 | - | ZERO |
| bin all_values[121] | 0 | 1 | - | ZERO |
| bin all_values[122] | 0 | 1 | - | ZERO |
| bin all_values[123] | 0 | 1 | - | ZERO |
| bin all_values[124] | 0 | 1 | - | ZERO |
| bin all_values[125] | 0 | 1 | - | ZERO |
| bin all_values[126] | 0 | 1 | - | ZERO |
| bin all_values[127] | 0 | 1 | - | ZERO |
| bin all_values[128] | 0 | 1 | - | ZERO |
| bin all_values[129] | 0 | 1 | - | ZERO |
| bin all_values[130] | 0 | 1 | - | ZERO |
| bin all_values[131] | 0 | 1 | - | ZERO |
| bin all_values[132] | 0 | 1 | - | ZERO |
| bin all_values[133] | 0 | 1 | - | ZERO |
| bin all_values[134] | 0 | 1 | - | ZERO |
| bin all_values[135] | 0 | 1 | - | ZERO |
| bin all_values[136] | 0 | 1 | - | ZERO |
| bin all_values[137] | 0 | 1 | - | ZERO |
| bin all_values[138] | 0 | 1 | - | ZERO |
| bin all_values[139] | 0 | 1 | - | ZERO |
| bin all_values[140] | 0 | 1 | - | ZERO |
| bin all_values[141] | 0 | 1 | - | ZERO |
| bin all_values[142] | 0 | 1 | - | ZERO |
| bin all_values[143] | 0 | 1 | - | ZERO |
| bin all_values[144] | 0 | 1 | - | ZERO |
| bin all_values[145] | 0 | 1 | - | ZERO |
| bin all_values[146] | 0 | 1 | - | ZERO |
| bin all_values[147] | 0 | 1 | - | ZERO |
| bin all_values[148] | 0 | 1 | - | ZERO |

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|---|---|---|---|---|
| bin all_values[149] | 0 | 1 | - | ZERO |
| bin all_values[150] | 0 | 1 | - | ZERO |
| bin all_values[151] | 0 | 1 | - | ZERO |
| bin all_values[152] | 0 | 1 | - | ZERO |
| bin all_values[153] | 0 | 1 | - | ZERO |
| bin all_values[154] | 0 | 1 | - | ZERO |
| bin all_values[155] | 0 | 1 | - | ZERO |
| bin all_values[156] | 0 | 1 | - | ZERO |
| bin all_values[157] | 0 | 1 | - | ZERO |
| bin all_values[158] | 0 | 1 | - | ZERO |
| bin all_values[159] | 0 | 1 | - | ZERO |
| bin all_values[160] | 0 | 1 | - | ZERO |
| bin all_values[161] | 0 | 1 | - | ZERO |
| bin all_values[162] | 0 | 1 | - | ZERO |
| bin all_values[163] | 0 | 1 | - | ZERO |
| bin all_values[164] | 0 | 1 | - | ZERO |
| bin all_values[165] | 0 | 1 | - | ZERO |
| bin all_values[166] | 0 | 1 | - | ZERO |
| bin all_values[167] | 0 | 1 | - | ZERO |
| bin all_values[168] | 0 | 1 | - | ZERO |
| bin all_values[169] | 0 | 1 | - | ZERO |
| bin all_values[170] | 0 | 1 | - | ZERO |
| bin all_values[171] | 0 | 1 | - | ZERO |
| bin all_values[172] | 0 | 1 | - | ZERO |
| bin all_values[173] | 0 | 1 | - | ZERO |
| bin all_values[174] | 0 | 1 | - | ZERO |
| bin all_values[175] | 0 | 1 | - | ZERO |
| bin all_values[176] | 0 | 1 | - | ZERO |
| bin all_values[177] | 0 | 1 | - | ZERO |
| bin all_values[178] | 0 | 1 | - | ZERO |
| bin all_values[179] | 0 | 1 | - | ZERO |
| bin all_values[180] | 0 | 1 | - | ZERO |
| bin all_values[181] | 0 | 1 | - | ZERO |
| bin all_values[182] | 0 | 1 | - | ZERO |
| bin all_values[183] | 0 | 1 | - | ZERO |
| bin all_values[184] | 0 | 1 | - | ZERO |
| bin all_values[185] | 0 | 1 | - | ZERO |
| bin all_values[186] | 0 | 1 | - | ZERO |
| bin all_values[187] | 0 | 1 | - | ZERO |
| bin all_values[188] | 0 | 1 | - | ZERO |
| bin all_values[189] | 0 | 1 | - | ZERO |
| bin all_values[190] | 0 | 1 | - | ZERO |
| bin all_values[191] | 0 | 1 | - | ZERO |
| bin all_values[192] | 0 | 1 | - | ZERO |
| bin all_values[193] | 0 | 1 | - | ZERO |
| bin all_values[194] | 0 | 1 | - | ZERO |
| bin all_values[195] | 0 | 1 | - | ZERO |
| bin all_values[196] | 0 | 1 | - | ZERO |
| bin all_values[197] | 0 | 1 | - | ZERO |
| bin all_values[198] | 0 | 1 | - | ZERO |
| bin all_values[199] | 0 | 1 | - | ZERO |
| bin all_values[200] | 0 | 1 | - | ZERO |
| bin all_values[201] | 0 | 1 | - | ZERO |
| bin all_values[202] | 0 | 1 | - | ZERO |
| bin all_values[203] | 0 | 1 | - | ZERO |
| bin all_values[204] | 0 | 1 | - | ZERO |
| bin all_values[205] | 0 | 1 | - | ZERO |

| | | | | |
|---|---|---|---|---|
| bin all_values[206] | 0 | 1 | - | ZERO |
| bin all_values[207] | 0 | 1 | - | ZERO |
| bin all_values[208] | 0 | 1 | - | ZERO |
| bin all_values[209] | 0 | 1 | - | ZERO |
| bin all_values[210] | 0 | 1 | - | ZERO |
| bin all_values[211] | 0 | 1 | - | ZERO |
| bin all_values[212] | 0 | 1 | - | ZERO |
| bin all_values[213] | 0 | 1 | - | ZERO |
| bin all_values[214] | 0 | 1 | - | ZERO |
| bin all_values[215] | 0 | 1 | - | ZERO |
| bin all_values[216] | 0 | 1 | - | ZERO |
| bin all_values[217] | 0 | 1 | - | ZERO |
| bin all_values[218] | 0 | 1 | - | ZERO |
| bin all_values[219] | 0 | 1 | - | ZERO |
| bin all_values[220] | 0 | 1 | - | ZERO |
| bin all_values[221] | 0 | 1 | - | ZERO |
| bin all_values[222] | 0 | 1 | - | ZERO |
| bin all_values[223] | 0 | 1 | - | ZERO |
| bin all_values[224] | 0 | 1 | - | ZERO |
| bin all_values[225] | 0 | 1 | - | ZERO |
| bin all_values[226] | 0 | 1 | - | ZERO |
| bin all_values[227] | 0 | 1 | - | ZERO |
| bin all_values[228] | 0 | 1 | - | ZERO |
| bin all_values[229] | 0 | 1 | - | ZERO |
| bin all_values[230] | 0 | 1 | - | ZERO |
| bin all_values[231] | 0 | 1 | - | ZERO |
| bin all_values[232] | 0 | 1 | - | ZERO |
| bin all_values[233] | 0 | 1 | - | ZERO |
| bin all_values[234] | 0 | 1 | - | ZERO |
| bin all_values[235] | 0 | 1 | - | ZERO |
| bin all_values[236] | 0 | 1 | - | ZERO |
| bin all_values[237] | 0 | 1 | - | ZERO |
| bin all_values[238] | 0 | 1 | - | ZERO |
| bin all_values[239] | 0 | 1 | - | ZERO |
| bin all_values[240] | 0 | 1 | - | ZERO |
| bin all_values[241] | 0 | 1 | - | ZERO |
| bin all_values[242] | 0 | 1 | - | ZERO |
| bin all_values[243] | 0 | 1 | - | ZERO |
| bin all_values[244] | 0 | 1 | - | ZERO |
| bin all_values[245] | 0 | 1 | - | ZERO |
| bin all_values[246] | 0 | 1 | - | ZERO |
| bin all_values[247] | 0 | 1 | - | ZERO |
| bin all_values[248] | 0 | 1 | - | ZERO |
| bin all_values[249] | 0 | 1 | - | ZERO |
| bin all_values[250] | 0 | 1 | - | ZERO |
| bin all_values[251] | 0 | 1 | - | ZERO |
| bin all_values[252] | 0 | 1 | - | ZERO |
| bin all_values[253] | 0 | 1 | - | ZERO |
| bin all_values[254] | 0 | 1 | - | ZERO |
| bin all_values[255] | 0 | 1 | - | ZERO |
| Coverpoint cp2 | 0.00% | 100 | - | ZERO |
| covered/total bins: | 0 | 4 | - | |
| missing/total bins: | 4 | 4 | - | |
| % Hit: | 0.00% | 100 | - | |
| bin allones | 0 | 1 | - | ZERO |
| bin allzeros | 0 | 1 | - | ZERO |
| bin up_pattern | 0 | 1 | - | ZERO |

```
    bin down_pattern                    0         1         -    ZERO
  Coverpoint cp3                      50.00%      100         -    Uncovered
    covered/total bins:                   1         2         -
    missing/total bins:                   1         2         -
    % Hit:                           50.00%       100         -
    bin reset                             0         1         -    ZERO
    bin not_reset                         1         1         -    Covered
  Coverpoint cp4                      50.00%      100         -    Uncovered
    covered/total bins:                   1         2         -
    missing/total bins:                   1         2         -
    % Hit:                           50.00%       100         -
    bin start                             0         1         -    ZERO
    bin not_start                         1         1         -    Covered
  Coverpoint cp5                       0.00%      100         -    ZERO
    covered/total bins:                   0         2         -
    missing/total bins:                   2         2         -
    % Hit:                            0.00%       100         -
    bin parity_even_enabled               0         1         -    ZERO
    bin parity_odd_enabled                0         1         -    ZERO
Statement Coverage:
  Enabled Coverage            Bins      Hits    Misses  Coverage
  ----------------            ----      ----    ------  --------
  Statements                     7         7         0   100.00%

================================Statement
Details================================

Statement Coverage for instance /uart_packet --

  Line        Item                   Count     Source
  ----        ----                   -----     ------
File uart_packet.sv
  76            1                        1
  77            1                        1
  78            1                        1
  79            1                        1
  80            1                        1
  81            1                        1
  84            1                        1

COVERGROUP COVERAGE:
----------------------------------------------------------------------------------------------------------
Covergroup                                  Metric       Goal       Bins    Status

----------------------------------------------------------------------------------------------------------
 TYPE /uart_packet/covergroup_class/cg                 20.07%        100         -
Uncovered
  covered/total bins:                       3        266         -
  missing/total bins:                     263        266         -
  % Hit:                                1.12%        100         -
  Coverpoint cp1                        0.39%        100         -    Uncovered
    covered/total bins:                     1        256         -
    missing/total bins:                   255        256         -
    % Hit:                              0.39%        100         -
    bin all_values[0]                       0          1         -    ZERO
    bin all_values[1]                       0          1         -    ZERO
    bin all_values[2]                       0          1         -    ZERO
```

| | | | | |
|---|---|---|---|---|
| bin all_values[3] | 0 | 1 | - | ZERO |
| bin all_values[4] | 0 | 1 | - | ZERO |
| bin all_values[5] | 0 | 1 | - | ZERO |
| bin all_values[6] | 0 | 1 | - | ZERO |
| bin all_values[7] | 0 | 1 | - | ZERO |
| bin all_values[8] | 0 | 1 | - | ZERO |
| bin all_values[9] | 0 | 1 | - | ZERO |
| bin all_values[10] | 0 | 1 | - | ZERO |
| bin all_values[11] | 0 | 1 | - | ZERO |
| bin all_values[12] | 0 | 1 | - | ZERO |
| bin all_values[13] | 0 | 1 | - | ZERO |
| bin all_values[14] | 0 | 1 | - | ZERO |
| bin all_values[15] | 0 | 1 | - | ZERO |
| bin all_values[16] | 0 | 1 | - | ZERO |
| bin all_values[17] | 0 | 1 | - | ZERO |
| bin all_values[18] | 0 | 1 | - | ZERO |
| bin all_values[19] | 0 | 1 | - | ZERO |
| bin all_values[20] | 0 | 1 | - | ZERO |
| bin all_values[21] | 0 | 1 | - | ZERO |
| bin all_values[22] | 0 | 1 | - | ZERO |
| bin all_values[23] | 0 | 1 | - | ZERO |
| bin all_values[24] | 0 | 1 | - | ZERO |
| bin all_values[25] | 0 | 1 | - | ZERO |
| bin all_values[26] | 0 | 1 | - | ZERO |
| bin all_values[27] | 0 | 1 | - | ZERO |
| bin all_values[28] | 0 | 1 | - | ZERO |
| bin all_values[29] | 0 | 1 | - | ZERO |
| bin all_values[30] | 0 | 1 | - | ZERO |
| bin all_values[31] | 0 | 1 | - | ZERO |
| bin all_values[32] | 0 | 1 | - | ZERO |
| bin all_values[33] | 0 | 1 | - | ZERO |
| bin all_values[34] | 0 | 1 | - | ZERO |
| bin all_values[35] | 0 | 1 | - | ZERO |
| bin all_values[36] | 0 | 1 | - | ZERO |
| bin all_values[37] | 0 | 1 | - | ZERO |
| bin all_values[38] | 0 | 1 | - | ZERO |
| bin all_values[39] | 0 | 1 | - | ZERO |
| bin all_values[40] | 0 | 1 | - | ZERO |
| bin all_values[41] | 0 | 1 | - | ZERO |
| bin all_values[42] | 0 | 1 | - | ZERO |
| bin all_values[43] | 0 | 1 | - | ZERO |
| bin all_values[44] | 0 | 1 | - | ZERO |
| bin all_values[45] | 0 | 1 | - | ZERO |
| bin all_values[46] | 0 | 1 | - | ZERO |
| bin all_values[47] | 0 | 1 | - | ZERO |
| bin all_values[48] | 0 | 1 | - | ZERO |
| bin all_values[49] | 0 | 1 | - | ZERO |
| bin all_values[50] | 0 | 1 | - | ZERO |
| bin all_values[51] | 0 | 1 | - | ZERO |
| bin all_values[52] | 0 | 1 | - | ZERO |
| bin all_values[53] | 0 | 1 | - | ZERO |
| bin all_values[54] | 0 | 1 | - | ZERO |
| bin all_values[55] | 0 | 1 | - | ZERO |
| bin all_values[56] | 0 | 1 | - | ZERO |
| bin all_values[57] | 0 | 1 | - | ZERO |
| bin all_values[58] | 0 | 1 | - | ZERO |
| bin all_values[59] | 0 | 1 | - | ZERO |

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|---|---|---|---|---|
| bin all_values[60] | 0 | 1 | - | ZERO |
| bin all_values[61] | 0 | 1 | - | ZERO |
| bin all_values[62] | 0 | 1 | - | ZERO |
| bin all_values[63] | 0 | 1 | - | ZERO |
| bin all_values[64] | 0 | 1 | - | ZERO |
| bin all_values[65] | 0 | 1 | - | ZERO |
| bin all_values[66] | 0 | 1 | - | ZERO |
| bin all_values[67] | 0 | 1 | - | ZERO |
| bin all_values[68] | 0 | 1 | - | ZERO |
| bin all_values[69] | 0 | 1 | - | ZERO |
| bin all_values[70] | 0 | 1 | - | ZERO |
| bin all_values[71] | 0 | 1 | - | ZERO |
| bin all_values[72] | 0 | 1 | - | ZERO |
| bin all_values[73] | 0 | 1 | - | ZERO |
| bin all_values[74] | 0 | 1 | - | ZERO |
| bin all_values[75] | 0 | 1 | - | ZERO |
| bin all_values[76] | 0 | 1 | - | ZERO |
| bin all_values[77] | 0 | 1 | - | ZERO |
| bin all_values[78] | 0 | 1 | - | ZERO |
| bin all_values[79] | 0 | 1 | - | ZERO |
| bin all_values[80] | 0 | 1 | - | ZERO |
| bin all_values[81] | 0 | 1 | - | ZERO |
| bin all_values[82] | 0 | 1 | - | ZERO |
| bin all_values[83] | 0 | 1 | - | ZERO |
| bin all_values[84] | 0 | 1 | - | ZERO |
| bin all_values[85] | 0 | 1 | - | ZERO |
| bin all_values[86] | 0 | 1 | - | ZERO |
| bin all_values[87] | 0 | 1 | - | ZERO |
| bin all_values[88] | 0 | 1 | - | ZERO |
| bin all_values[89] | 0 | 1 | - | ZERO |
| bin all_values[90] | 0 | 1 | - | ZERO |
| bin all_values[91] | 0 | 1 | - | ZERO |
| bin all_values[92] | 0 | 1 | - | ZERO |
| bin all_values[93] | 0 | 1 | - | ZERO |
| bin all_values[94] | 0 | 1 | - | ZERO |
| bin all_values[95] | 0 | 1 | - | ZERO |
| bin all_values[96] | 0 | 1 | - | ZERO |
| bin all_values[97] | 0 | 1 | - | ZERO |
| bin all_values[98] | 0 | 1 | - | ZERO |
| bin all_values[99] | 0 | 1 | - | ZERO |
| bin all_values[100] | 0 | 1 | - | ZERO |
| bin all_values[101] | 0 | 1 | - | ZERO |
| bin all_values[102] | 0 | 1 | - | ZERO |
| bin all_values[103] | 0 | 1 | - | ZERO |
| bin all_values[104] | 0 | 1 | - | ZERO |
| bin all_values[105] | 0 | 1 | - | ZERO |
| bin all_values[106] | 0 | 1 | - | ZERO |
| bin all_values[107] | 0 | 1 | - | ZERO |
| bin all_values[108] | 1 | 1 | - | Covered |
| bin all_values[109] | 0 | 1 | - | ZERO |
| bin all_values[110] | 0 | 1 | - | ZERO |
| bin all_values[111] | 0 | 1 | - | ZERO |
| bin all_values[112] | 0 | 1 | - | ZERO |
| bin all_values[113] | 0 | 1 | - | ZERO |
| bin all_values[114] | 0 | 1 | - | ZERO |
| bin all_values[115] | 0 | 1 | - | ZERO |
| bin all_values[116] | 0 | 1 | - | ZERO |

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|---|---|---|---|---|
| bin all_values[117] | 0 | 1 | - | ZERO |
| bin all_values[118] | 0 | 1 | - | ZERO |
| bin all_values[119] | 0 | 1 | - | ZERO |
| bin all_values[120] | 0 | 1 | - | ZERO |
| bin all_values[121] | 0 | 1 | - | ZERO |
| bin all_values[122] | 0 | 1 | - | ZERO |
| bin all_values[123] | 0 | 1 | - | ZERO |
| bin all_values[124] | 0 | 1 | - | ZERO |
| bin all_values[125] | 0 | 1 | - | ZERO |
| bin all_values[126] | 0 | 1 | - | ZERO |
| bin all_values[127] | 0 | 1 | - | ZERO |
| bin all_values[128] | 0 | 1 | - | ZERO |
| bin all_values[129] | 0 | 1 | - | ZERO |
| bin all_values[130] | 0 | 1 | - | ZERO |
| bin all_values[131] | 0 | 1 | - | ZERO |
| bin all_values[132] | 0 | 1 | - | ZERO |
| bin all_values[133] | 0 | 1 | - | ZERO |
| bin all_values[134] | 0 | 1 | - | ZERO |
| bin all_values[135] | 0 | 1 | - | ZERO |
| bin all_values[136] | 0 | 1 | - | ZERO |
| bin all_values[137] | 0 | 1 | - | ZERO |
| bin all_values[138] | 0 | 1 | - | ZERO |
| bin all_values[139] | 0 | 1 | - | ZERO |
| bin all_values[140] | 0 | 1 | - | ZERO |
| bin all_values[141] | 0 | 1 | - | ZERO |
| bin all_values[142] | 0 | 1 | - | ZERO |
| bin all_values[143] | 0 | 1 | - | ZERO |
| bin all_values[144] | 0 | 1 | - | ZERO |
| bin all_values[145] | 0 | 1 | - | ZERO |
| bin all_values[146] | 0 | 1 | - | ZERO |
| bin all_values[147] | 0 | 1 | - | ZERO |
| bin all_values[148] | 0 | 1 | - | ZERO |
| bin all_values[149] | 0 | 1 | - | ZERO |
| bin all_values[150] | 0 | 1 | - | ZERO |
| bin all_values[151] | 0 | 1 | - | ZERO |
| bin all_values[152] | 0 | 1 | - | ZERO |
| bin all_values[153] | 0 | 1 | - | ZERO |
| bin all_values[154] | 0 | 1 | - | ZERO |
| bin all_values[155] | 0 | 1 | - | ZERO |
| bin all_values[156] | 0 | 1 | - | ZERO |
| bin all_values[157] | 0 | 1 | - | ZERO |
| bin all_values[158] | 0 | 1 | - | ZERO |
| bin all_values[159] | 0 | 1 | - | ZERO |
| bin all_values[160] | 0 | 1 | - | ZERO |
| bin all_values[161] | 0 | 1 | - | ZERO |
| bin all_values[162] | 0 | 1 | - | ZERO |
| bin all_values[163] | 0 | 1 | - | ZERO |
| bin all_values[164] | 0 | 1 | - | ZERO |
| bin all_values[165] | 0 | 1 | - | ZERO |
| bin all_values[166] | 0 | 1 | - | ZERO |
| bin all_values[167] | 0 | 1 | - | ZERO |
| bin all_values[168] | 0 | 1 | - | ZERO |
| bin all_values[169] | 0 | 1 | - | ZERO |
| bin all_values[170] | 0 | 1 | - | ZERO |
| bin all_values[171] | 0 | 1 | - | ZERO |
| bin all_values[172] | 0 | 1 | - | ZERO |
| bin all_values[173] | 0 | 1 | - | ZERO |

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|---|---|---|---|---|
| bin all_values[174] | 0 | 1 | - | ZERO |
| bin all_values[175] | 0 | 1 | - | ZERO |
| bin all_values[176] | 0 | 1 | - | ZERO |
| bin all_values[177] | 0 | 1 | - | ZERO |
| bin all_values[178] | 0 | 1 | - | ZERO |
| bin all_values[179] | 0 | 1 | - | ZERO |
| bin all_values[180] | 0 | 1 | - | ZERO |
| bin all_values[181] | 0 | 1 | - | ZERO |
| bin all_values[182] | 0 | 1 | - | ZERO |
| bin all_values[183] | 0 | 1 | - | ZERO |
| bin all_values[184] | 0 | 1 | - | ZERO |
| bin all_values[185] | 0 | 1 | - | ZERO |
| bin all_values[186] | 0 | 1 | - | ZERO |
| bin all_values[187] | 0 | 1 | - | ZERO |
| bin all_values[188] | 0 | 1 | - | ZERO |
| bin all_values[189] | 0 | 1 | - | ZERO |
| bin all_values[190] | 0 | 1 | - | ZERO |
| bin all_values[191] | 0 | 1 | - | ZERO |
| bin all_values[192] | 0 | 1 | - | ZERO |
| bin all_values[193] | 0 | 1 | - | ZERO |
| bin all_values[194] | 0 | 1 | - | ZERO |
| bin all_values[195] | 0 | 1 | - | ZERO |
| bin all_values[196] | 0 | 1 | - | ZERO |
| bin all_values[197] | 0 | 1 | - | ZERO |
| bin all_values[198] | 0 | 1 | - | ZERO |
| bin all_values[199] | 0 | 1 | - | ZERO |
| bin all_values[200] | 0 | 1 | - | ZERO |
| bin all_values[201] | 0 | 1 | - | ZERO |
| bin all_values[202] | 0 | 1 | - | ZERO |
| bin all_values[203] | 0 | 1 | - | ZERO |
| bin all_values[204] | 0 | 1 | - | ZERO |
| bin all_values[205] | 0 | 1 | - | ZERO |
| bin all_values[206] | 0 | 1 | - | ZERO |
| bin all_values[207] | 0 | 1 | - | ZERO |
| bin all_values[208] | 0 | 1 | - | ZERO |
| bin all_values[209] | 0 | 1 | - | ZERO |
| bin all_values[210] | 0 | 1 | - | ZERO |
| bin all_values[211] | 0 | 1 | - | ZERO |
| bin all_values[212] | 0 | 1 | - | ZERO |
| bin all_values[213] | 0 | 1 | - | ZERO |
| bin all_values[214] | 0 | 1 | - | ZERO |
| bin all_values[215] | 0 | 1 | - | ZERO |
| bin all_values[216] | 0 | 1 | - | ZERO |
| bin all_values[217] | 0 | 1 | - | ZERO |
| bin all_values[218] | 0 | 1 | - | ZERO |
| bin all_values[219] | 0 | 1 | - | ZERO |
| bin all_values[220] | 0 | 1 | - | ZERO |
| bin all_values[221] | 0 | 1 | - | ZERO |
| bin all_values[222] | 0 | 1 | - | ZERO |
| bin all_values[223] | 0 | 1 | - | ZERO |
| bin all_values[224] | 0 | 1 | - | ZERO |
| bin all_values[225] | 0 | 1 | - | ZERO |
| bin all_values[226] | 0 | 1 | - | ZERO |
| bin all_values[227] | 0 | 1 | - | ZERO |
| bin all_values[228] | 0 | 1 | - | ZERO |
| bin all_values[229] | 0 | 1 | - | ZERO |
| bin all_values[230] | 0 | 1 | - | ZERO |

| | | | | |
|---|---|---|---|---|
| bin all_values[231] | 0 | 1 | - | ZERO |
| bin all_values[232] | 0 | 1 | - | ZERO |
| bin all_values[233] | 0 | 1 | - | ZERO |
| bin all_values[234] | 0 | 1 | - | ZERO |
| bin all_values[235] | 0 | 1 | - | ZERO |
| bin all_values[236] | 0 | 1 | - | ZERO |
| bin all_values[237] | 0 | 1 | - | ZERO |
| bin all_values[238] | 0 | 1 | - | ZERO |
| bin all_values[239] | 0 | 1 | - | ZERO |
| bin all_values[240] | 0 | 1 | - | ZERO |
| bin all_values[241] | 0 | 1 | - | ZERO |
| bin all_values[242] | 0 | 1 | - | ZERO |
| bin all_values[243] | 0 | 1 | - | ZERO |
| bin all_values[244] | 0 | 1 | - | ZERO |
| bin all_values[245] | 0 | 1 | - | ZERO |
| bin all_values[246] | 0 | 1 | - | ZERO |
| bin all_values[247] | 0 | 1 | - | ZERO |
| bin all_values[248] | 0 | 1 | - | ZERO |
| bin all_values[249] | 0 | 1 | - | ZERO |
| bin all_values[250] | 0 | 1 | - | ZERO |
| bin all_values[251] | 0 | 1 | - | ZERO |
| bin all_values[252] | 0 | 1 | - | ZERO |
| bin all_values[253] | 0 | 1 | - | ZERO |
| bin all_values[254] | 0 | 1 | - | ZERO |
| bin all_values[255] | 0 | 1 | - | ZERO |
| Coverpoint cp2 | 0.00% | 100 | - | ZERO |
| covered/total bins: | 0 | 4 | - | |
| missing/total bins: | 4 | 4 | - | |
| % Hit: | 0.00% | 100 | - | |
| bin allones | 0 | 1 | - | ZERO |
| bin allzeros | 0 | 1 | - | ZERO |
| bin up_pattern | 0 | 1 | - | ZERO |
| bin down_pattern | 0 | 1 | - | ZERO |
| Coverpoint cp3 | 50.00% | 100 | - | Uncovered |
| covered/total bins: | 1 | 2 | - | |
| missing/total bins: | 1 | 2 | - | |
| % Hit: | 50.00% | 100 | - | |
| bin reset | 0 | 1 | - | ZERO |
| bin not_reset | 1 | 1 | - | Covered |
| Coverpoint cp4 | 50.00% | 100 | - | Uncovered |
| covered/total bins: | 1 | 2 | - | |
| missing/total bins: | 1 | 2 | - | |
| % Hit: | 50.00% | 100 | - | |
| bin start | 0 | 1 | - | ZERO |
| bin not_start | 1 | 1 | - | Covered |
| Coverpoint cp5 | 0.00% | 100 | - | ZERO |
| covered/total bins: | 0 | 2 | - | |
| missing/total bins: | 2 | 2 | - | |
| % Hit: | 0.00% | 100 | - | |
| bin parity_even_enabled | 0 | 1 | - | ZERO |
| bin parity_odd_enabled | 0 | 1 | - | ZERO |

TOTAL COVERGROUP COVERAGE: 20.07%  COVERGROUP TYPES: 1

ASSERTION RESULTS:

| Name | File(Line) | Failure | Pass |
|---|---|---|---|

| | Count | Count |
|---|---|---|
| /top/uart_tb_top/generate_stimulus/immed__28 | | |
| testbench.sv(28) | 0 | 1 |

Total Coverage By Instance (filtered view): 27.68%

## RUN.DO FILE