

AO3401A

30V P-Channel MOSFET

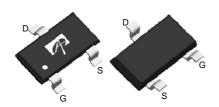
General Description

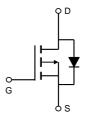
The AO3401A uses advanced trench technology to provide excellent $R_{\text{DS}(\text{ON})}$, low gate charge and operation gate voltages as low as 2.5V. This device is suitable for use as a load switch or other general applications.

Product Summary



SOT23
Top View Bottom View





Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		V _{DS}	-30	V	
Gate-Source Voltage		V _{GS}	±12	V	
Continuous Drain	T _A =25℃	1	-4		
Current	T _A =70℃	'D	-3.2	A	
Pulsed Drain Current Č		I _{DM}	-27		
	T _A =25℃	P _D	1.4	W	
Power Dissipation ^B	T _A =70℃	' D	0.9	VV	
Junction and Storage Temperature Range		T _J , T _{STG}	-55 to 150	C	

Thermal Characteristics									
Parameter	Symbol	Тур	Max	Units					
Maximum Junction-to-Ambient A	t ≤ 10s	$R_{\theta JA}$	70	90	℃/W				
Maximum Junction-to-Ambient AD	Steady-State	$\kappa_{\theta JA}$	100	125	€/M				
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	63	80	℃/W				



Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Тур	Max	Units	
STATIC P	ARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-30			V	
I _{DSS}	Zero Gate Voltage Drain Current	V_{DS} =-30V, V_{GS} =0V			-1	^	
		T _J =55℃			-5	μΑ	
I _{GSS}	Gate-Body leakage current	V_{DS} =0V, V_{GS} = ±12V			±100	nA	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS} I_{D}=-250\mu A$	-0.5	-0.9	-1.3	V	
I _{D(ON)}	On state drain current	V_{GS} =-10V, V_{DS} =-5V	-27			Α	
	Static Drain-Source On-Resistance	V_{GS} =-10V, I_D =-4.0A		41	50	50 mΩ	
		T _J =125℃		62	75	11122	
		V_{GS} =-4.5V, I_{D} =-3.5A		47	60	mΩ	
		V_{GS} =-2.5V, I_{D} =-2.5A		60	85	mΩ	
g FS	Forward Transconductance	V_{DS} =-5V, I_{D} =-4.0A		17		S	
V_{SD}	Diode Forward Voltage	I _S =-1A,V _{GS} =0V		-0.7	-1	V	
I _S	Maximum Body-Diode Continuous Current				-2	Α	
DYNAMIC	PARAMETERS						
C _{iss}	Input Capacitance			645		pF	
C _{oss}	Output Capacitance	V_{GS} =0V, V_{DS} =-15V, f=1MHz		80		pF	
C_{rss}	Reverse Transfer Capacitance			55		pF	
R_g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	4	7.8	12	Ω	
SWITCHIN	NG PARAMETERS						
Q _g (10V)	Total Gate Charge			14		nC	
Q _g (4.5V)	Total Gate Charge	V _{GS} =-10V, V _{DS} =-15V, I _D =-4.0A		7		nC	
Q_{gs}	Gate Source Charge	v _{GS} =-10v, v _{DS} =-15v, i _D =-4.0A		1.5		nC	
Q_{gd}	Gate Drain Charge] [2.5		nC	
t _{D(on)}	Turn-On DelayTime			6.5		ns	
t _r	Turn-On Rise Time	V_{GS} =-10V, V_{DS} =-15V, R_L =3.75 Ω ,		3.5		ns	
t _{D(off)}	Turn-Off DelayTime	$R_{GEN}=3\Omega$		41		ns	
t _f	Turn-Off Fall Time]		9		ns	
t _{rr}	Body Diode Reverse Recovery Time	I _F =-4.0A, dI/dt=100A/μs		11		ns	
Q_{rr}	Body Diode Reverse Recovery Charge	I _F =-4.0A, dI/dt=100A/μs		3.5		nC	

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

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B. The power dissipation P_D is based on $T_{J(MAX)}$ =150°C, using \leqslant 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150$ °C. Ratings are based on low frequency and duty cycles to keep initial $T_J=25$ °C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μ s pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse ratin g.



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

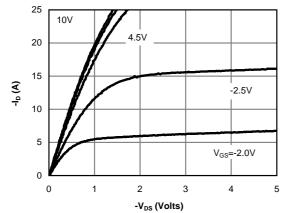


Fig 1: On-Region Characteristics (Note E)

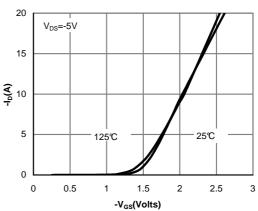


Figure 2: Transfer Characteristics (Note E)

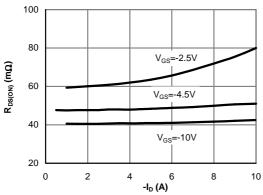


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

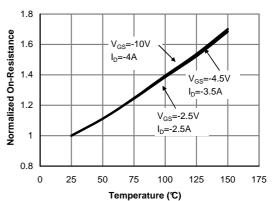


Figure 4: On-Resistance vs. Junction Temperature (Note E)

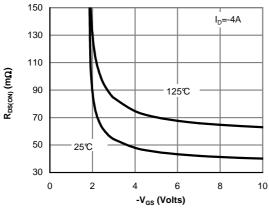


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

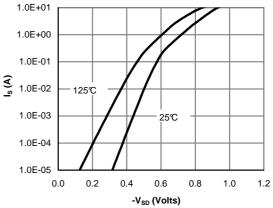


Figure 6: Body-Diode Characteristics (Note E)



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

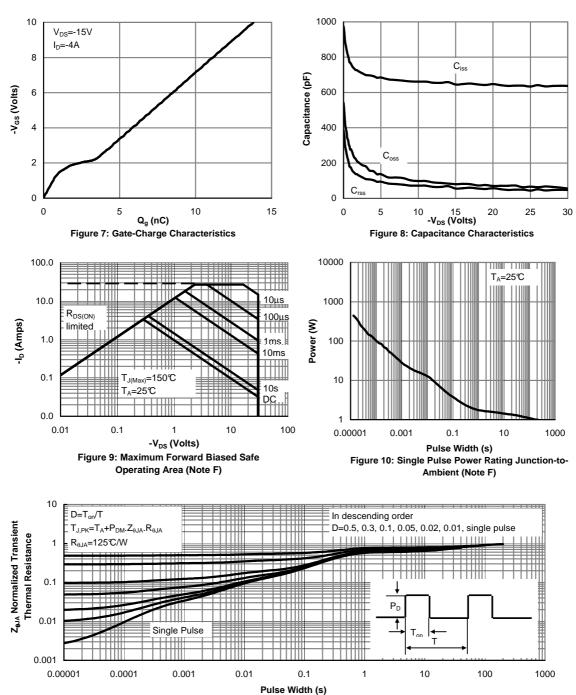
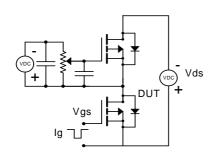
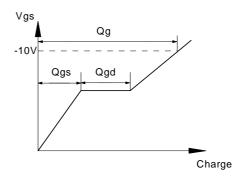


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

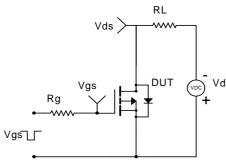


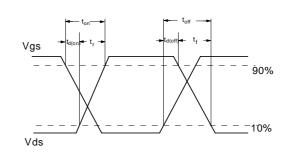
Gate Charge Test Circuit & Waveform



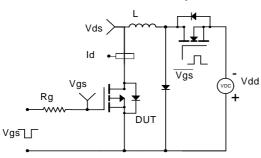


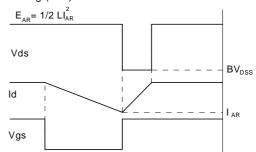
Resistive Switching Test Circuit & Waveforms





Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms

