DESIGN, OPERATION AND CONTROL OF 3 LEVEL NPC CONVERTER AS RECTIFIER WITH DQO MODEL PI CONTROL WITH SPWM OPERATION

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1. Introduction

Rectification is the term used to describe the conversion of alternating current (AC) into direct current (DC). When actively controlled switches are used to carry out the ac-dc conversion, synchronous rectification is used. Using controlled switches rather than diodes has several benefits, including an increase in system efficiency. Therefore, synchronous rectifiers—also known as active rectifiers—are utilized in a variety of applications, such as dc motor drives, power conversion and home appliances. With an emphasis on industrial and high-power applications, a three-phase rectifier circuit is frequently used as a dc power source for medium and high-voltage level power transmission systems.

Multilevel power converters are widely recognized for their benefits in all kinds of power conversion systems. Multilevel converters are widely used in medium and high-power applications in the industry due to their benefits such as bidirectional power flow, a rise in output voltage magnitude, resilience, etc.

One of the most popular multilevel topologies is the neutral-point-clamped (NPC) converter. The fundamental working principle of the NPC converter in rectifier applications is to maintain the total dc-link voltage constant at a chosen reference value without incorporating a supply voltage. Typically, a feedback control loop is implemented to do this. However, the converter must also manage the three -phase system's instantaneous powers in order to maintain nearly sinusoidal ac current waveforms and regulate the power factor.

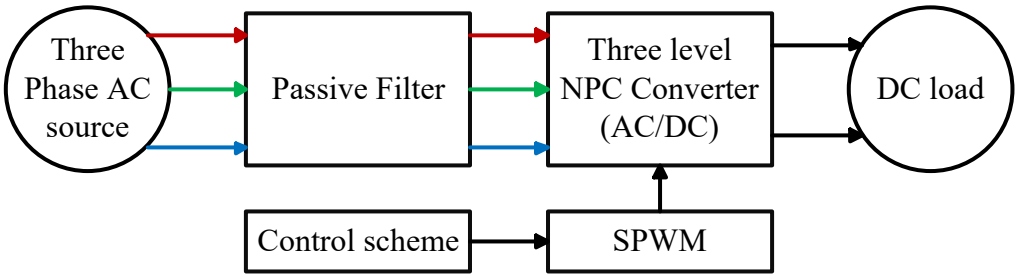

Fig. 1: General block diagram

2. Objective of this project

In this project, the 3-level Neutral Point Clamped converter is operated as in rectification mode while using the SPWM technique to provide switching to all the switches. The main goals which we have to achieve in this work are:

- To maintain a constant DC voltage across load.

- Control action is in dq0-frame.
- Input current harmonics reduction.
- Power factor correction.

3. Origin of the NPC converter

In the late 1960s, a cascaded H-bridge converter, also known as an H-bridge converter with series connections, introduced the multilevel scaled waveform idea. After a decade, the diode-based clamped converter was introduced in the late 1970s. As it was developed, the diode-based converter concept grew into the 3-level NPC converter we know today, and it can be considered the first true multilevel power converter for medium high voltage applications.

Diode clamped inverter is the mostly used multilevel converter structure where diodes are used to clamp the dc bus voltage to achieve steps in the output voltage.

In multilevel converter, the diode based clamped inverter, which uses diodes as a clamping devices to clamp the dc bus voltage in order to achieve the desired steps in the output voltage, is the mostly used. The circuit for a 3-level 4-level inverter using a diode clamp is shown in Fig. 2.

The diodes D_{1a} and D_{2a} represent the primary distinction between the two-level inverter and the three-level inverter. These two components reduce the switch voltage to half the dc-bus voltage. With an N level diode clamped inverter, the voltage across each capacitor is typically $\frac{V_{dc}}{n-1}$ at steady state. The ratings of the clamping devices vary even though each active switching device is only required to block $\frac{V_{dc}}{n-1}$. To offer various voltage levels, the diode-clamped inverter's phases are coupled to a number of capacitors. By incorporating additional capacitors, the original innovation claimed that the concept could be stretched to a number of level.

The implementation of the diode-clamped inverter is limited to the third level due to problems with the voltage balancing of capacitor. The 3-level inverter is currently widely employed in real applications as a result of recent advancements in industry. Despite the fact that three-level inverters for 480V are readily accessible, medium-voltage applications still predominate. In general, two (N-1) switching devices, (N-1) * (N-2) clamping diodes, and (N-1) dc link capacitors are needed for each leg of a N level diode clamped inverter.

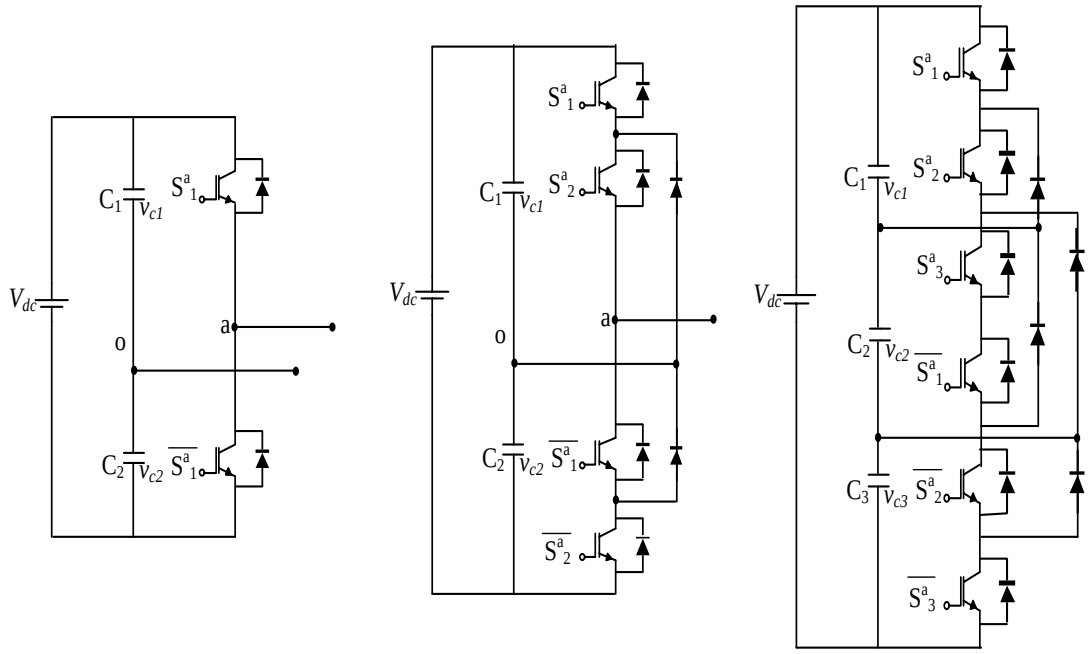

Fig. 2: Structural topology of the different levels diode-clamped inverter (2,3 and 4 level).

4. Three-Level NPC converter

Fig.3 depicts the main circuit of the NPC-PWM inverter. Here (Sa1, Sa4), (Sb1, Sb4), (Sc1 Sc4) are the primary transistors operating as switches, and (Sa2, Sa3), (Sb2, Sb3), (Sc2, Sc3) are secondary transistors to vary the output potentials to the neutral point (o) potential, with the help of diodes. All standard PWM methods may be used with this inverter. But in the following, we will simply look at one technique.: the SPWM technique based on two carriers level shifted signals. Auxiliarytransistors (Sa3, Sa2) are driven complementary to the primary transistors (Sa1, Sa4), respectively. The respective waveforms for a conventional inverter are shown in Fig. 4(b). Comparing Fig. 4(a) with Fig. 4(b).

1) Output terminal potentials of the conventional PWM inverter vary between $(+E/2)$ and $(-E/2)$, but those of the NPC-PWM inverter vary between $(+E/2)$ and (0) or $(+E/2)$ and (0).

2) The NPC-PWM inverter's terminal voltage waveform has a lower harmonic content than a traditional inverter.

When power is flowing from the grid side to the converter, this circuit acts as a rectifier and converts 3-phase AC voltage into DC and then charges the DC-link capacitor and supplies the load. When the power flows in the reverse direction, the converter will operate as an inverter, thus discharging the capacitor and taking power from the load.

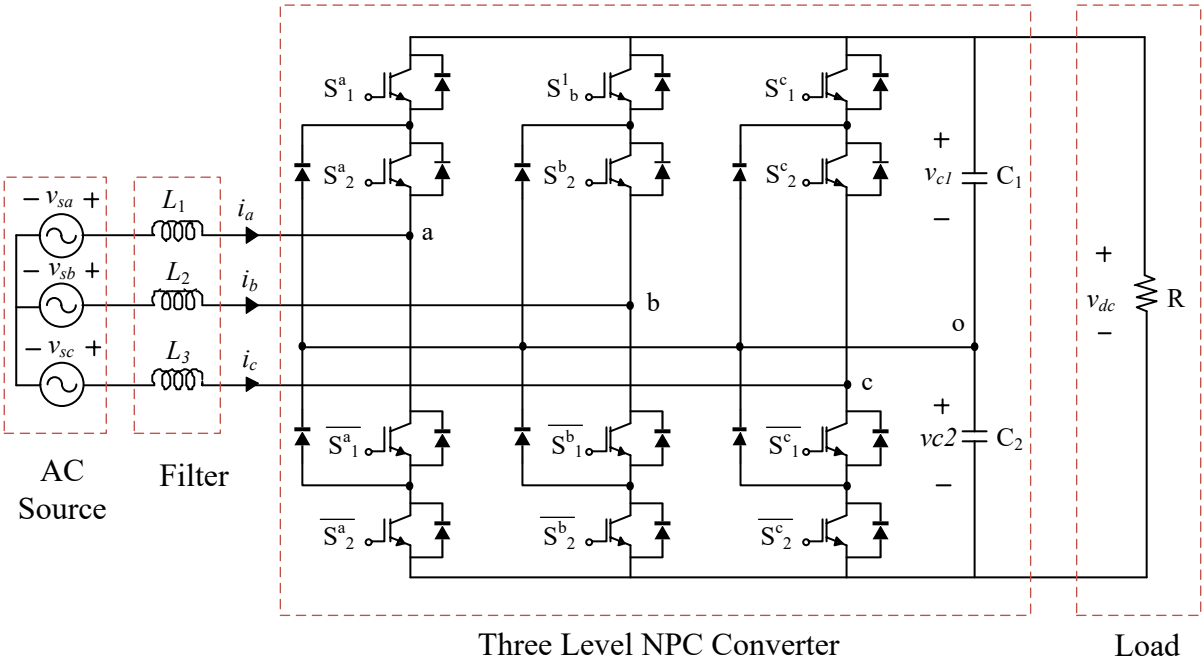

Fig. 3: 3 level NPC converter as rectifier

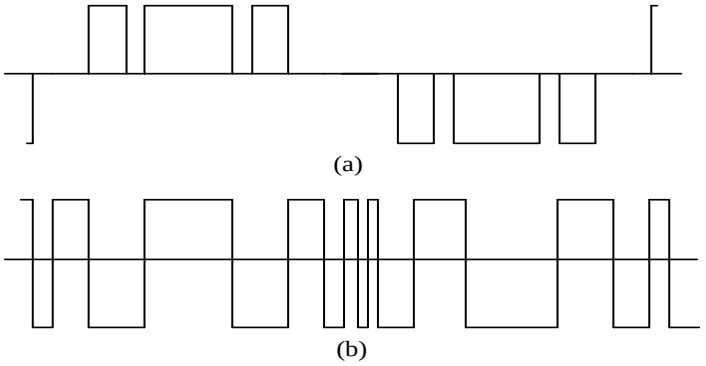

Fig. 4: (a) 3-level NPC inverter output, (b) 2-level inverter output.

One major advantage of such a converter is the bi-directionality of power flow and the skill to control the reactive power of the Grid. For satisfactory operation of the converter, the output voltage must be maintained at 1.5 times higher than the peak of the input line voltage.

4.1 Modes of Operation

- Operation mode 1: In this mode of operation, the phase a terminal voltage will be $V_{a0} = \frac{V_{dc}}{2}$ (assuming that $V_{c1} = V_{c2}$)and the filter inductor voltage will be equal to $V_L = v_{an} - \frac{V_{dc}}{2} < 0$ (voltage drop across the resistor is neglected). So the current (i) through the line will start reducing. In this mode of operation, the current (i) will may charge or discharge the dc bus capacitor C_1 if the ac system voltage V_a is positive or negative half cycles of the input voltage, respectively.

- Operation mode 2: In this mode of operation, the phase a terminal voltage $V_{a0} = 0$ (assuming that $V_{c1} = V_{c2}$) and the filter inductor voltage will be equal to $V_L = v_a$ (voltage drop across the resistor is neglected). So the line current I_a rises or decreases during the positive or negative cycles of the input supply voltage, respectively. In this mode of operation,line current I_a will not charge or discharge the dc bus capacitors.
- Operation mode 3: In this mode of operation, the phase a terminal voltage $V_{a0} = -\frac{V_{dc}}{2}$. The filter inductor voltage will be $V_L = v_a - \frac{V_{dc}}{2} > 0$ (voltage drop across the resistor is neglected). So the current (i) through line increases. The current (i) will charge or discharge the dc bus capacitor C_2 if the ac system voltage V_a is positive or negative half cycles of the supply voltage, respectively.

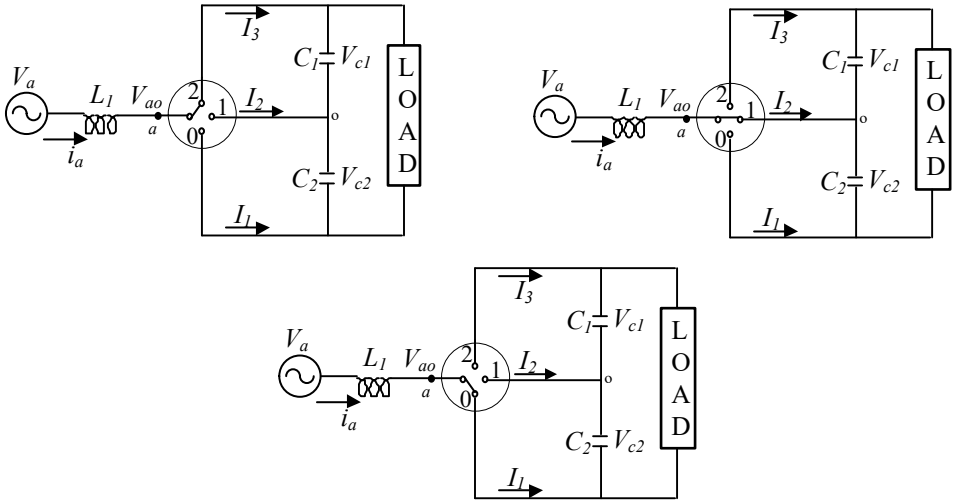

Fig. 5: (a) Operation mode 1, (b) Operation mode 2, and (c) Operation mode 3

5. Level shift SPWM Technique

5.1 Block diagram of control technique

Block diagram of phase PWM generation scheme and the control signal waveform along with the triangular waveform are given below:

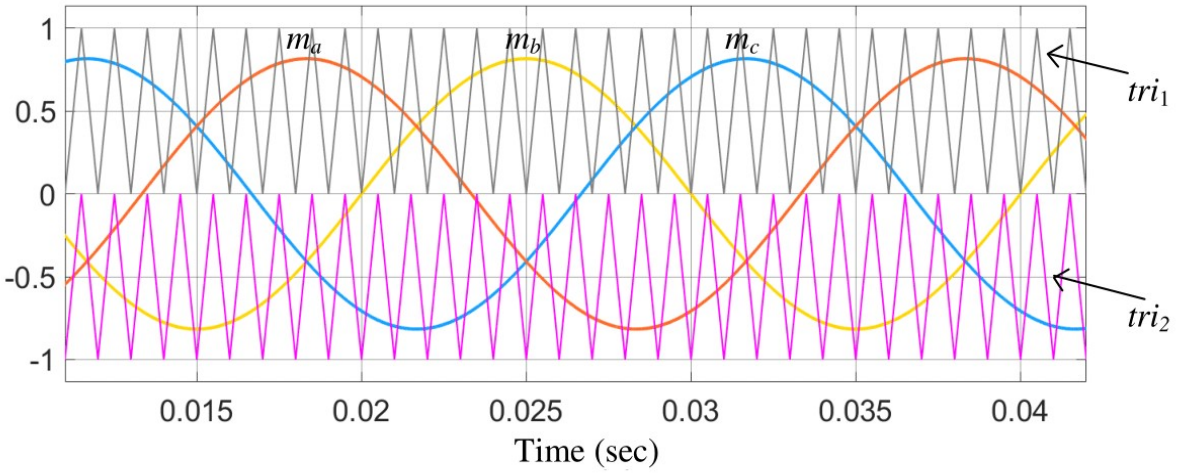

Fig. 6: Control technique of 3-level NPC converter.

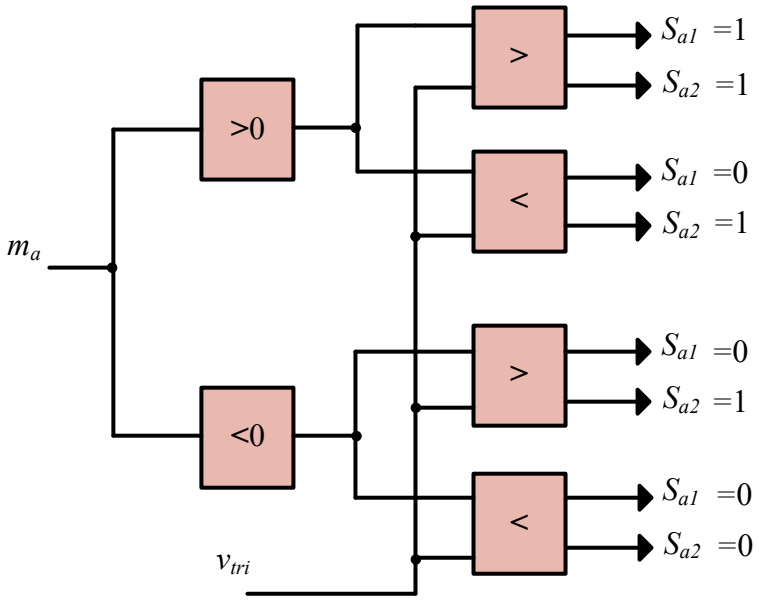

Fig. 7: Block Diagram for A phase PWM generation.

It will be necessary to use N - 1 carriers if an N-level inverter is used. The peak-to-peak amplitude Ac and frequency w of the carriers are identical. The carrier set's zero references are positioned in the center. The modulating signal is a sinusoid with amplitude Am and frequency f. Each carrier is compared against the modulating signal at every time.

If the modulating sinusoidal is larger than the triangle carrier and smaller than the triangular in the first and second halves of the fundamental period, respectively, each comparison yields a result of 1 or 0, as illustrated in Fig. 6. The findings are summed to determine the voltage level needed at the inverter's output terminal.

6. Grid Synchronization

Single-phase grid-connected converters' internal oscillators must be tuned to the oscillator dynamics imposed by the grid in order to achieve grid synchronization. This is done by accurately detecting the characteristics of the grid voltage. The amplitude and phase-angle of the fundamental frequency component of the grid voltage are often the primary characteristics of interest when integrating renewable energy sources into the grid utilizing power converters.

The implementation of other features, such as power conditioning, resonance damping, or grid impedance detection, in the grid-connected power converter of distributed generators, however, might also make the identification of other harmonic components interesting. As a result, grid synchronization techniques are comparable to the harmonic detection techniques used in power systems and may be divided into two primary categories, namely the frequency-domain and the time-domain detection approaches.

The frequency-domain detection techniques often rely on a discrete Fourier analysis implementation. The following will briefly discuss the Fourier series, the discrete Fourier transform (DFT), and the recursive discrete Fourier transform (RDFT) as potential grid synchronization methods in single-phase systems. By definition, frequency analysis presupposes that the processed signal's fundamental frequency has a known and constant value. The basic grid frequency should be an integer multiple of the signal processor's sampling frequency. The time-domain detection techniques rely on some sort of adaptive loop that enables a built-in oscillator to follow the signal's important component. The phase-locked loop (PLL) is the synchronization technique that is most frequently utilized in engineering applications.

6.1 Phased Locked Loop (PLL)

A phase-locked loop (PLL) is a closed-loop system in which a feedback loop is used to regulate an internal oscillator to maintain the timing of an external periodic signal. The PLL's guiding principle is ideal for a grid-connected power converter since it should operate in unison with the grid. In order to provide an internal signal that is amplitude and phase-coherent and is utilized by various control system blocks, it should phase-lock its internal oscillator to a certain grid power signal. Based on silicon-controlled rectifiers, the first grid-connected power converters were developed. These power converters had a limited amount of control and synchronized with the grid when the grid voltage crossed zero.

Figure 8 depicts a phase-locked loop's (PLL) fundamental structure. There are three main building

blocks in it.

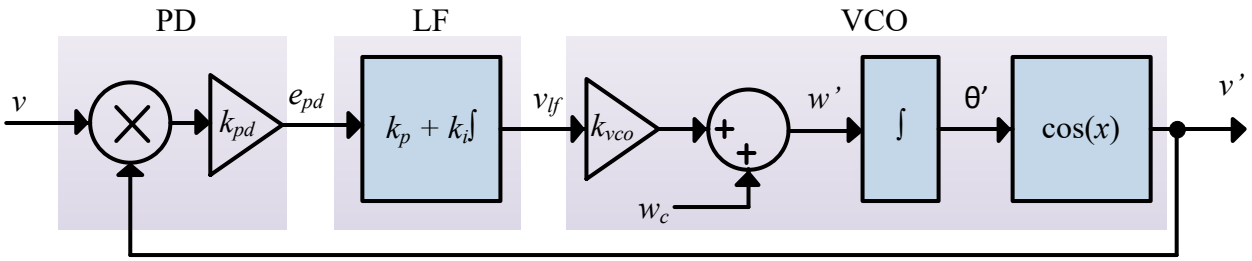

Fig. 8: Basic PLL architecture.

- The phase detector (PD) block produces an output signal proportionate to the phase difference between the signal coming from the PLL's internal oscillator, v1, and the input signal, v. High-frequency AC components may also be present, depending on the kind of PD, along with the DC phase-angle difference signal.
- In order to reduce the high-frequency AC components from the PD output, the loop filter (LF) block exhibits a low-pass filtering characteristic. Usually, a first-order low-pass filter or a PI controller make up this block.
- The VCO, or voltage-controlled oscillator, based on the input voltage supplied by the LF, this block produces an AC signal at its output that has a frequency shift relative to a specified center frequency, wc.

7. DQ0 Control

The DQ0 control of three-level NPC converter will help to change voltage/current at the load side with the help of instantaneous active and reactive power theory. To understand it, we require to take a look over the transformations required in DQ0 control.

7.1 DQ0 Transformation

Two orthogonal dq axes that are positioned at the $\theta = \omega t$ angular point on the plane and rotate at a frequency of ω , are the foundation of the synchronous reference frame, also referred to as the dq reference frame. In three-phase systems, this formulation is very helpful for controlling the active and reactive power components.

The following expression is the transformation matrix needed to convert a voltage vector from the abc stationary reference frame to the dq0 synchronous reference frame:

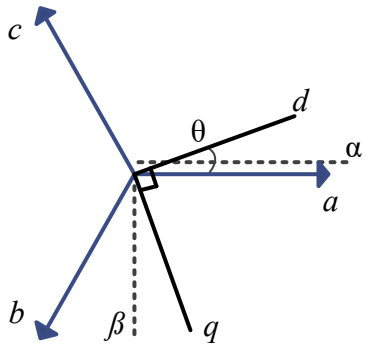

Fig. 9: Graphical representation of the dq0 reference frame.

$$\begin{bmatrix} v_d \\ v_q \\ v_o \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} cos(\theta) & cos(\theta - \frac{2\pi}{3}) & cos(\theta + \frac{2\pi}{3}) \\ -sin(\theta) & -sin(\theta - \frac{2\pi}{3}) & -sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{1}$$

7.2 Power in DQ0 Quantitites

The power equation in dq0 frame will help to identify the current required to fulfill the power estimate. For a balanced system the active instantaneous power (p_{dq}) and reactive instantaneous power (q_{dq}) is given as:

$$p_{dq} = \frac{3}{2}(v_d i_d + v_q i_q) \tag{2}$$

$$q_{dq} = \frac{3}{2}(v_q i_d - v_d i_q) \tag{3}$$

7.3 Open Loop Control in DQ0 frame

By identifying the current required to meet the estimated power, modulation indexes are generated. The modulation index is then converted back to abc frame and compared with the level-shifted carrier wave. This generated the required PWM for the switches.

This dq0 control technique has been illustrated in Fig. 10

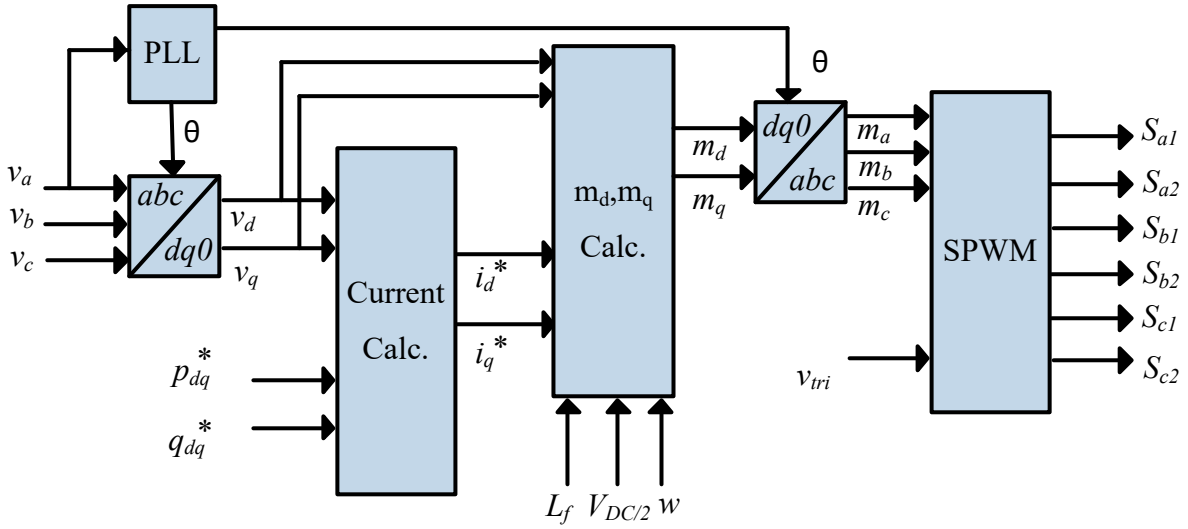

Fig. 10: Open Loop Control of Three-Level NPC in DQ0 frame.

8. Filter Design

A passive filter element is made up of a pair of capacitors and inductors that have been set to resonate over a certain frequency range or over a range of frequencies. Passive filters are used in power systems to reduce voltage distortion in sensitive areas of the system and suppress harmonic currents.

Different impedance values are shown at the resonant frequency by passive filters in order to function. When a filter is linked in series, the harmonic frequency that has to be blocked should encounter a high impedance. It is possible to link filters in a series design, although parallel connections are more typical. A shunt design like this sends harmonic currents to the ground while also producing reactive power that may be utilised to adjust the power factor. As a result, fundamental frequency capacitance is a design requirement for passive shunt filters.. For this converter, only a single inductor is used as an input filter.

$$L = \frac{V_{DC}/2}{4hf_s} \tag{4}$$

Here h represents the current ripple allowed at the grid side. And f_s represents the switching frequency on which the converter is operated. With the help of this equation, inductor values come out to be around 400 mH, which is a very big size inductor. Therefore to reduce the size frequency can be increased to 20 kHz. The inductor value is now changed to 20 mH.

9. DC Capacitor Design

The rating of Dc side capacitor is given by equation (5).

$$C >= \frac{T_r \Delta P_{LMAX}}{2 V_o \Delta V_o} \tag{5}$$

where T_r is the delays introduced by filtering of the dc-voltage and current control. ΔV_o is tolerable dc voltage variation. ΔP_{LMAX} is the maximum known variation of the power on DC side. and V_o is the DC voltage.

10. State space model of NPC converter:

The converter's state space model is a mathematical representation that aims to construct a linear system to interact with linear controllers using Matlab/Simulink. To achieve more ability to control either transient or steady-state response and the capability to study and change the overall system's performance under different loads. Some important aspects of the state space model are:

- The operation equation for each component of the exact model has been derived from its operation principle to create the average model.
- State space model is useful for the full control of both linear and nonlinear systems. In the case of a nonlinear system, some assumptions are considered for linearization.
- In this state space model of the converter, we use the D-Q transformation.
- The switches are assumed to be ideal with zero losses for analysis.
- The converter's load must be symmetrical and balanced. In the D-Q frame, the line currents and load voltages have zero components, which are denoted by iy0 = 0 and vy0, = 0, respectively.
- The switching frequency is substantially higher than the line frequency. For the purposes of using the moving average operator, this assumption is important.

Distinct state variables, including the DC link and the dynamics of the load, are present: two output voltages, two-line currents, and two DC link capacitor voltages. Additionally, it is fascinating to examine a variety of output characteristics, including output voltage, line current, neutral point voltage of the DC-link, etc.

10.1 Large signal model

$$\begin{bmatrix} \dot{i_{Yd}} \\ \dot{v_{Yd}} \\ \dot{i_{Yq}} \\ \dot{v_{Yq}} \\ \dot{v_p} \\ \dot{v_n} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L} & \omega_r & 0 & \frac{d_{pd}}{L} & \frac{d_{nd}}{L} \\ 0 & \frac{-1}{L} & \omega_r & 0 & \frac{d_{pd}}{L} & \frac{d_{nd}}{L} \\ 0 & \frac{-1}{L} & \omega_r & 0 & \frac{d_{pd}}{L} & \frac{d_{nd}}{L} \\ 0 & \frac{-1}{L} & \omega_r & 0 & \frac{d_{pd}}{L} & \frac{d_{nd}}{L} \\ 0 & \frac{-1}{L} & \omega_r & 0 & \frac{d_{pd}}{L} & \frac{d_{nd}}{L} \\ 0 & \frac{-1}{L} & \omega_r & 0 & \frac{d_{pd}}{L} & \frac{d_{nd}}{L} \end{bmatrix} \begin{bmatrix} i_{Yd} \\ v_{Yd} \\ i_{Yq} \\ v_{Yq} \\ v_p \\ v_n \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ \frac{-1}{C_1} \\ \frac{-1}{C_2} \end{bmatrix} i_{DC} \tag{6}$$

$$\begin{bmatrix} i_0 \\ i_{Yd} \\ i_{Yq} \\ v_{pn} \\ v_{No} \end{bmatrix} = \begin{bmatrix} -(d_{pd} + dnd) & 0 & -(d_{pq} + dnq) & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 0 & \frac{d_{p0}}{\sqrt{3}} & \frac{d_{n0}}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} i_{Yd} \\ v_{Yd} \\ i_{Yq} \\ v_{Yq} \\ v_p \\ v_n \end{bmatrix} \tag{7}$$

The following notation is for the different quantities used in the above matrices:

- d_{kl} are the duty cycles (by considering moving average and D-Q transformation to S_{ij}, in (1), $k = p, n$, $I = d, q, 0$.
- I_{yd} and i_{yq} are the line currents in D-Q components form.
- V_{yd} and V_{yq} are the load voltages,
- W_r is the angular frequency of the line.
- V_{pn} and $V_N o$ are DC-link voltage and load-neutral voltage, respectively.

Equation (1) shows the description of the state space model of the system. These equations are formulated using the Kirchhoff Voltage Law and Kirchoff current law, respectively, on the DC side and AC-side. Equations (1) and (2) gives a common description of a state space model-based system including a three level neutral point clamped (NPC) converter. For this description, the control variables are given in terms of the duty ratios like dpd, dnd, ..., dpo , dno which are expressed in D-Q components.

10.2 Small signal model

The general state-space expression of the model is given in equation (4) and it is processed using perturbation and linearization. Introducing the steady-state values the general expression for the

small-signal model is given by following model:

$$\hat{S}\begin{bmatrix} \hat{i_{Yd}} \\ \hat{v_{Yd}} \\ \hat{i_{Yq}} \\ \hat{v_{Yq}} \\ \hat{v_p} \\ \hat{v_n} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L} & \omega_r & 0 & \frac{D_{pd}}{L} & \frac{D_{nd}}{L} \\ \frac{1}{C} & \frac{-1}{RC} & 0 & \omega - r & 0 & 0 \\ \omega - r & 0 & 0 & \frac{1}{C} & \frac{d_{pd}}{L} & \frac{d_{nd}}{L} \\ 0 & \frac{-1}{L} & \omega & 0 & \frac{d_{pd}}{L} & \frac{d_{nd}}{L} \\ 0 & \frac{-1}{L} & \omega & 0 & \frac{d_{pd}}{L} & \frac{d_{nd}}{L} \\ 0 & \frac{-1}{L} & \omega & 0 & \frac{d_{pd}}{L} & \frac{d_{nd}}{L} \end{bmatrix} \begin{bmatrix} \hat{i_{Yd}} \\ \hat{v_{Yd}} \\ \hat{i_{Yq}} \\ \hat{v_{Yq}} \\ \hat{v_p} \\ \hat{v_n} \end{bmatrix} + \begin{bmatrix} \frac{V_p}{L} & \frac{V_n}{L} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{V_p}{L} & \frac{V_n}{L} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{-I_{Yd}}{C_{dc}} & 0 & \frac{-I_{Yq}}{C_{dc}} & 0 & 0 & 0 \\ 0 & \frac{-I_{Yd}}{C_{dc}} & 0 & \frac{-I_{Yq}}{C_{dc}} & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{d}_{pd} \\ \hat{d}_{nd} \\ \hat{d}_{pq} \\ \hat{d}_{nq} \\ \hat{d}_{p0} \\ \hat{d}_{n0} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ \frac{1}{Cdc} \\ \frac{-1}{Cdc} \end{bmatrix} \hat{i}_{DC} \tag{8}$$

Where,

- I_{dc} is the DC-link current.
- V_{pn}, V_p, V_n are DC-link voltages.
- D_{pd}, d_{nd}, d_{pq}, d_{nq}, d_{p0}, d_{n0} are different duty ratios in terms of D-Q components.
- V_{abc}I (I = d, q, 0) are output voltages in terms of D-Q components.
- R, L, C are the resistance, inductance, and capacitance, respectively.
- C_{dc} is the DC-link capacitor.

$$\hat{S}\begin{bmatrix} \hat{i_o} \\ \hat{i_{Yd}} \\ \hat{i_{Yq}} \\ \hat{v_{pn}} \\ \hat{v_{No}} \end{bmatrix} = \begin{bmatrix} -(D_{pd} + D_{nd}) & 0 & -(D_{pq} + D_{nq}) & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 0 & \frac{D_{p0}}{\sqrt{3}} & \frac{D_{n0}}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} \hat{i_{Yd}} \\ \hat{v_{Yd}} \\ \hat{i_{Yq}} \\ \hat{v_{Yq}} \\ \hat{v_p} \\ \hat{v_n} \end{bmatrix} +$$

$$\begin{bmatrix} -I_{Yd} & -I_{Yd} & -I_{Yq} & -I_{Yq} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{V_p}{\sqrt{3}} & \frac{V_n}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} \hat{d_{pd}} \\ \hat{d_{nd}} \\ \hat{d_{pq}} \\ \hat{d_{nq}} \\ \hat{d_{p0}} \\ \hat{d_{n0}} \end{bmatrix} \tag{9}$$

Equation (3) shows the perturbed state-space model and equation(4) shows the perturbed output

equation.

11. Open loop Simulation of 3-level NPC converter

Simulation of open loop 3-level NPC converter as a rectifier is done using Simulink.

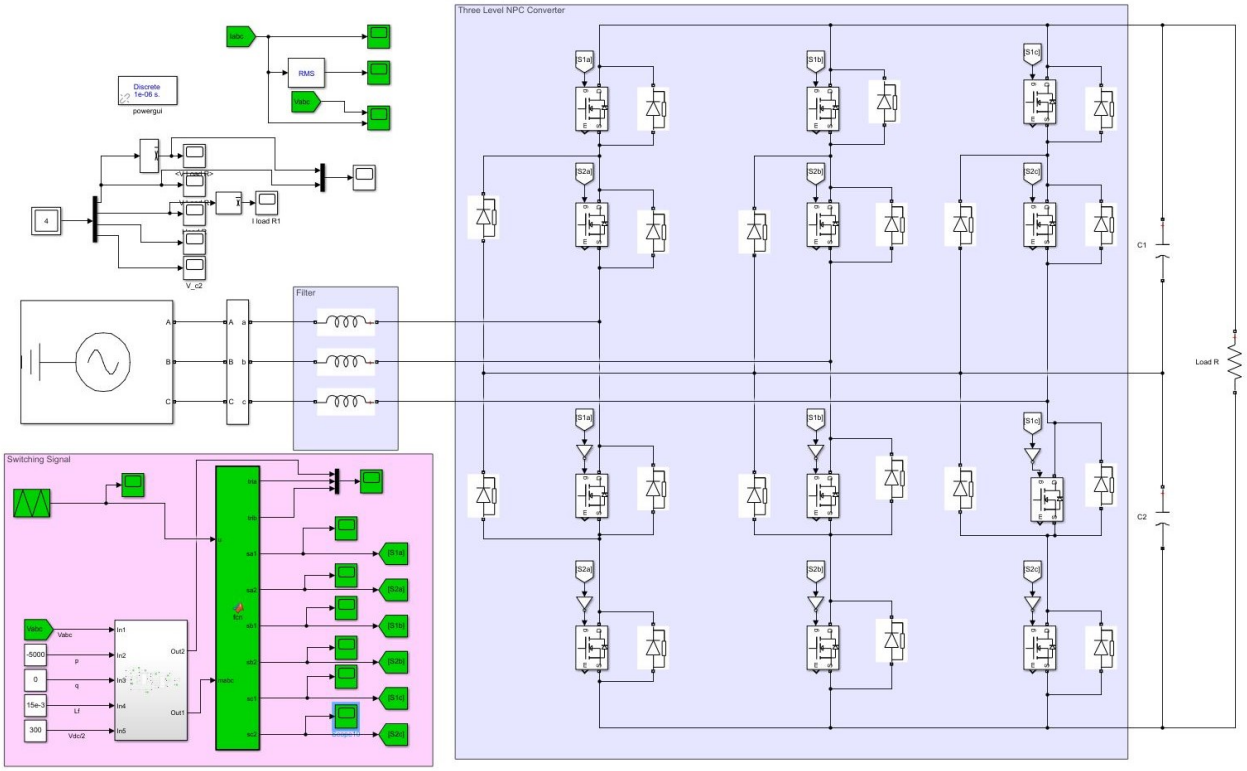

Fig. 11: Open loop simulation

- Line to line input source voltage (V_{ab}) = 415 V.
- Power transferred to Load Resistance P = 5000W.
- With the help of the design parameters discussed earlier, all parameters are calculated.
- Filter Inductance L_f = 15 mH.
- Half DC-dink capacitance C = 12 μF.
- Switching frequency f = 15kHz.
- Load Resistance = R = 72Ω.
- fixed time step = 1e-6.

11.1 Open loop Simulated Waveforms

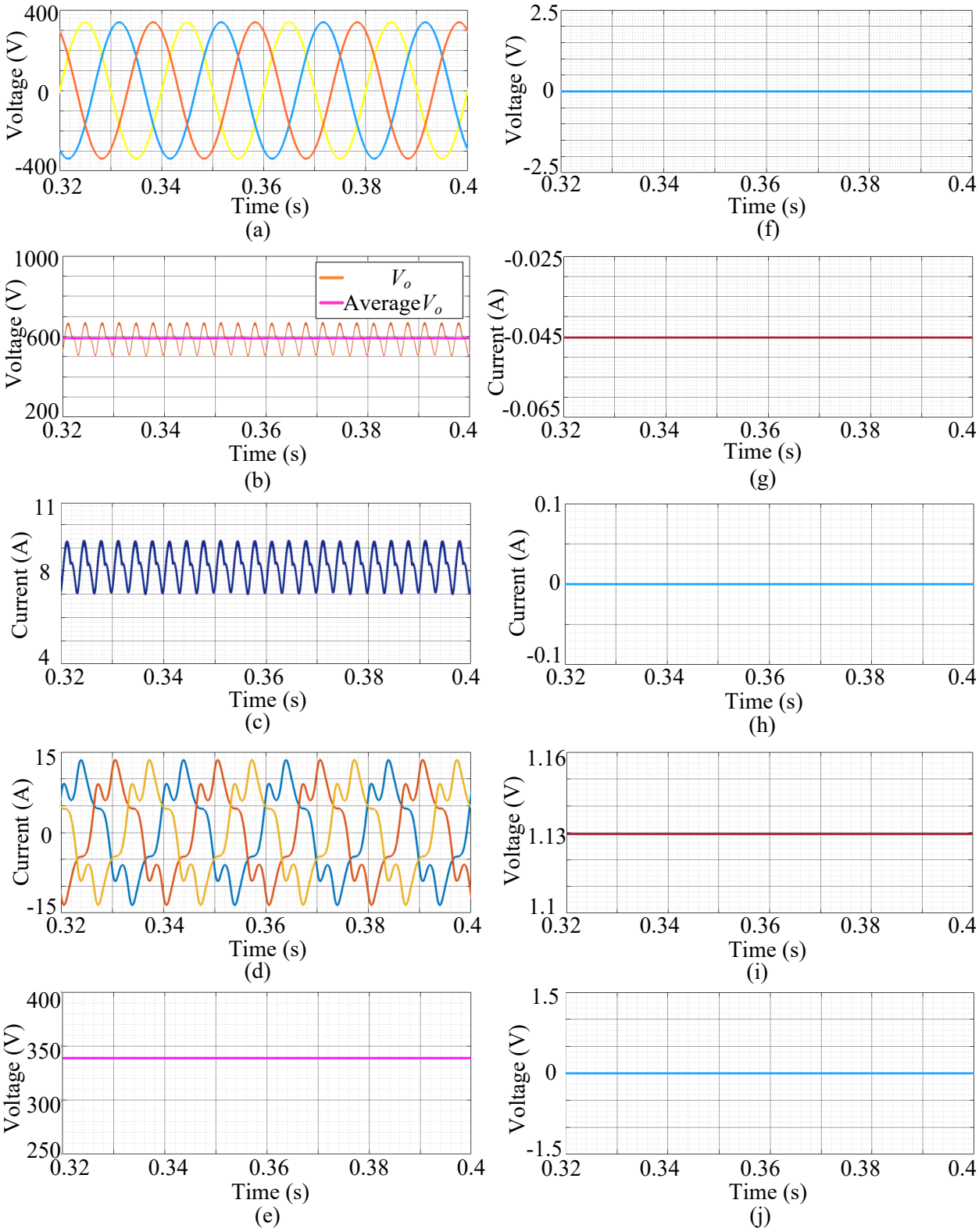

Fig. 12: (a) Supply Voltage, (b) Load Voltage, (c) Load Current, (d) Supply Current, (e) v_d, (f) v_q, (g) i_d, (h) i_q, (i) $m-d$, (j) m_q.

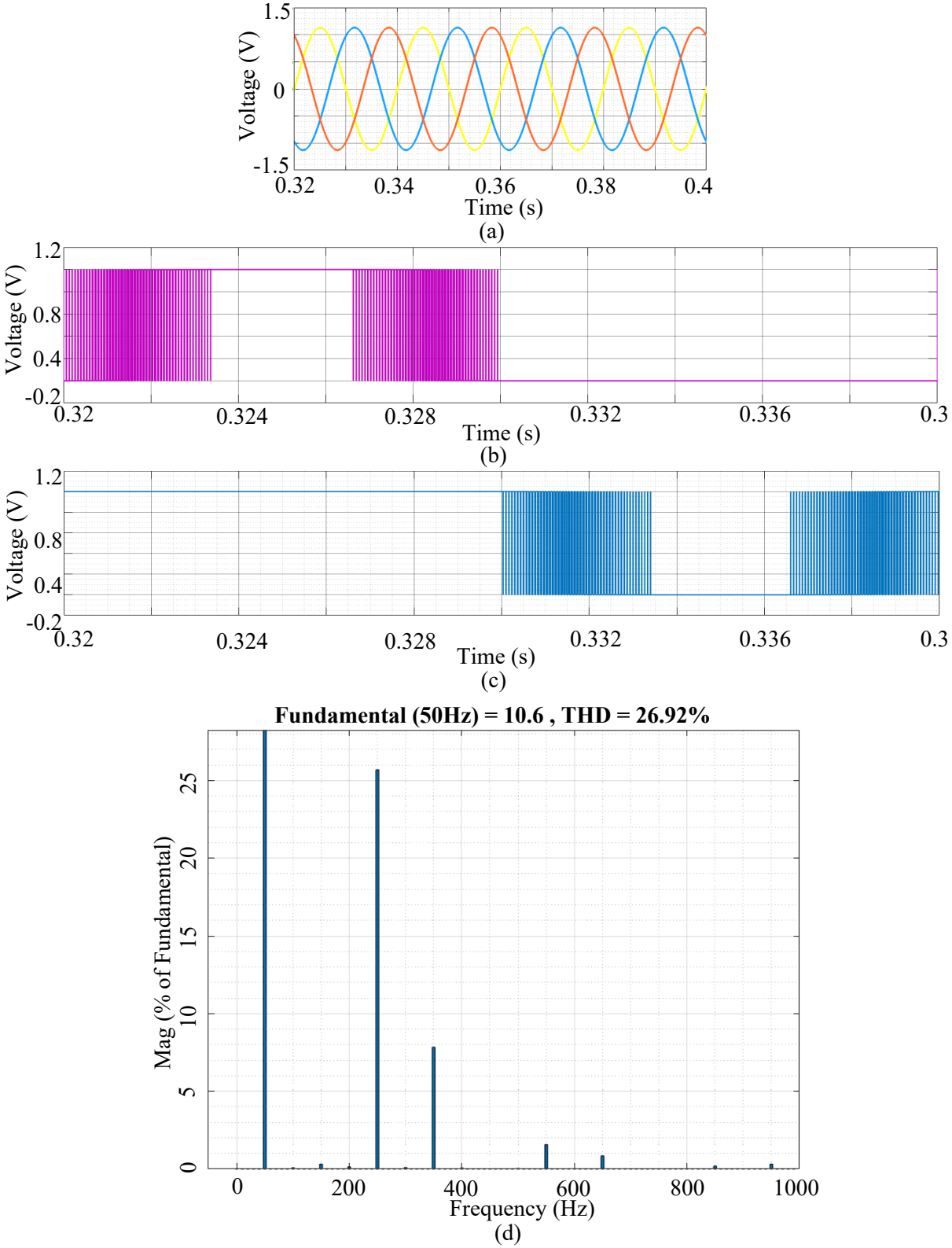

Fig. 13: (a) m_{abc}, (b) S_{a1}, (c) S_{a2}, (d) FFT analysis of supply current i_a.

- Now in order to control voltage, improve current quality and power factor, we will analyse circuit in close loop control.

12. Closed Loop Control in DQ0 frame

To control voltage and improve input current quality, closed-loop control is implemented. The block diagram of closed-loop control of three-level NPC is shown in Fig. 14. Outer loop contains of load voltage and reference load voltage compared and passed through the PI controller to produce i_d^* (reference current d component). The reference current's q component (i_q^*) is taken as zero as the reactive power transferred is zero. The error signal thus obtained by subtracting actual dq current components with reference ones is passed through the PI controller to obtain modulation signals.

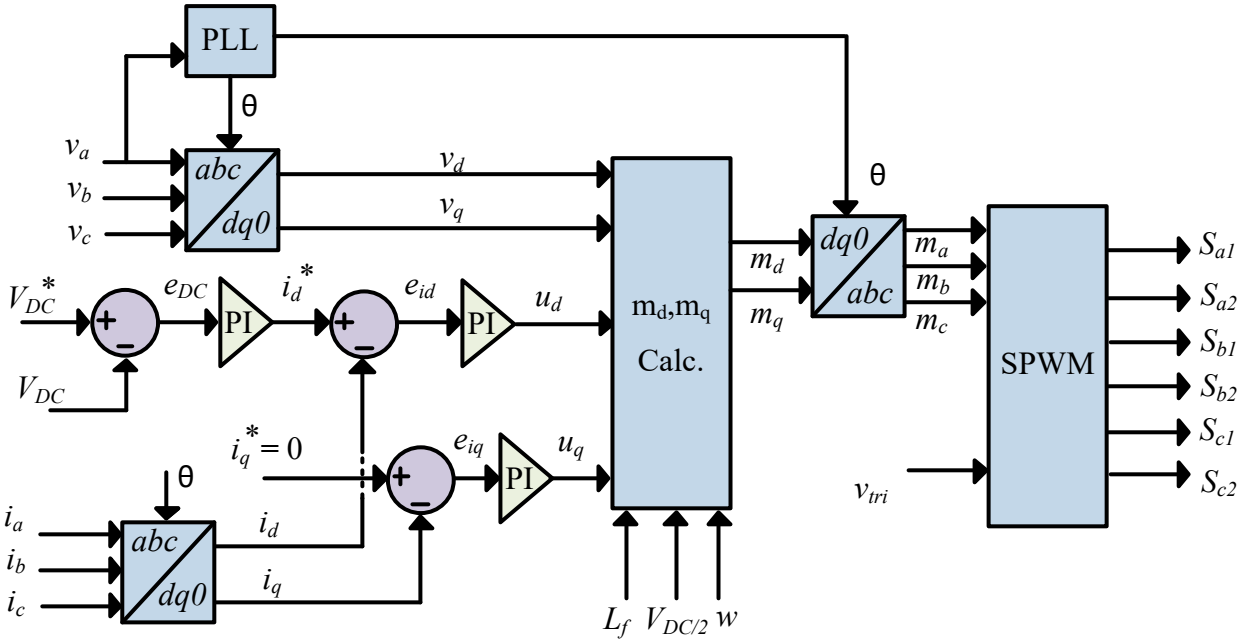

Fig. 14: Closed Loop Control of Three-Level NPC in DQ0 frame.

The equations for calculation of m_d and m_q are shown in equation (10). Both u_d and u_q contain coupling terms; i.e., i_d is found to be in the m_d equation, and i_q is found to be in the m_q equation. Therefore decoupling has to be done in order to produce m_d and m_q.

$$\begin{bmatrix} m_d \\ m_q \end{bmatrix} = \frac{1}{V_{DC}} \begin{bmatrix} 1 & 0 & 0 & \omega L_f \\ 0 & 1 & -\omega L_f & 0 \end{bmatrix} \begin{bmatrix} v_d \\ v_q \\ i_d \\ i_q \end{bmatrix} + \begin{bmatrix} u_d \\ u_q \end{bmatrix} \tag{10}$$

12.1 Close loop Simulated Waveforms

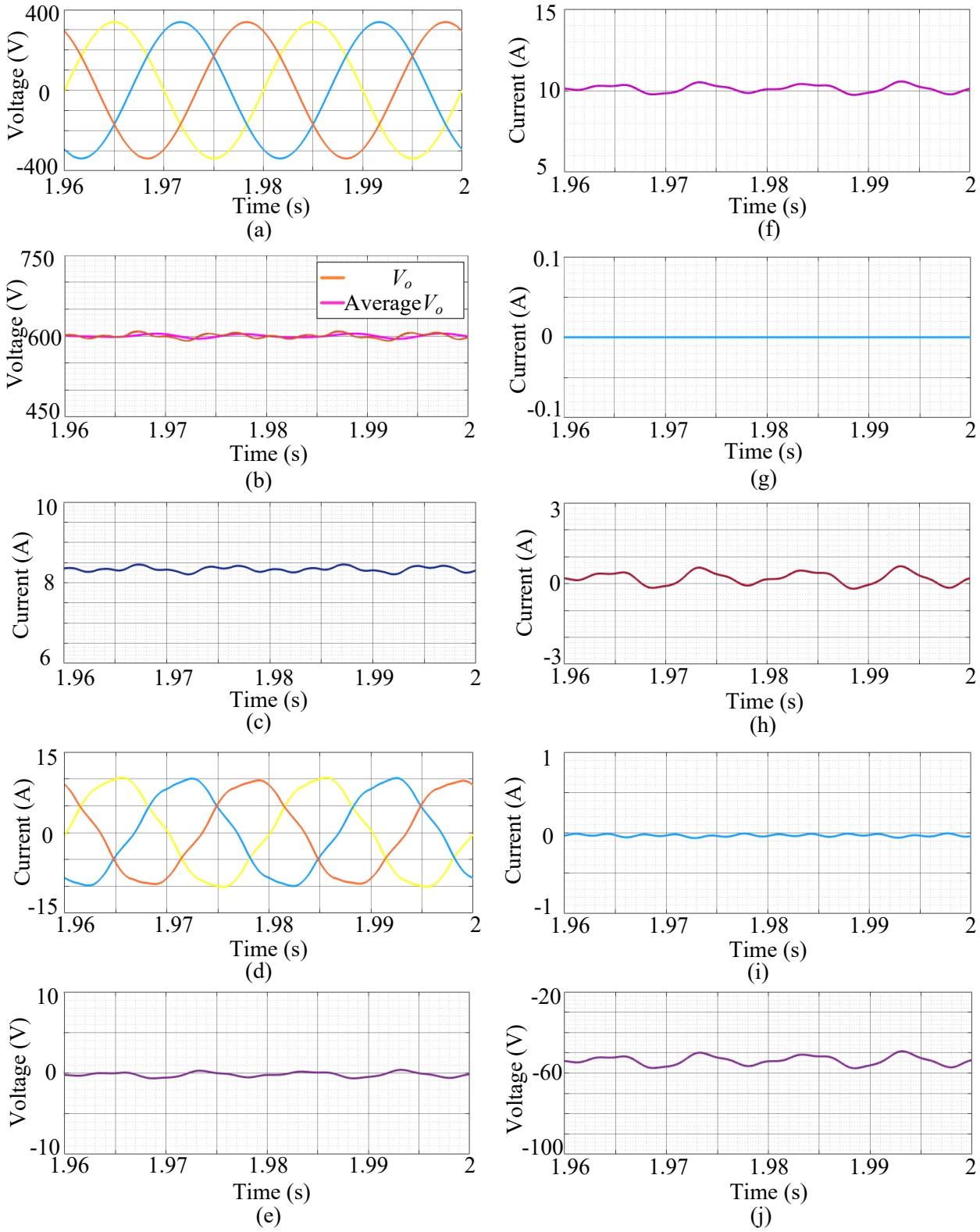

Fig. 15: (a) Supply Voltage, (b) Load Voltage, (c) Load Current, (d) Supply Current, (e) $e_{v_{DC}}$, (f) i_d^*, (g) i_q^*, (h) e_{i_d}, (i) e_{i_q}, (j) u_d.

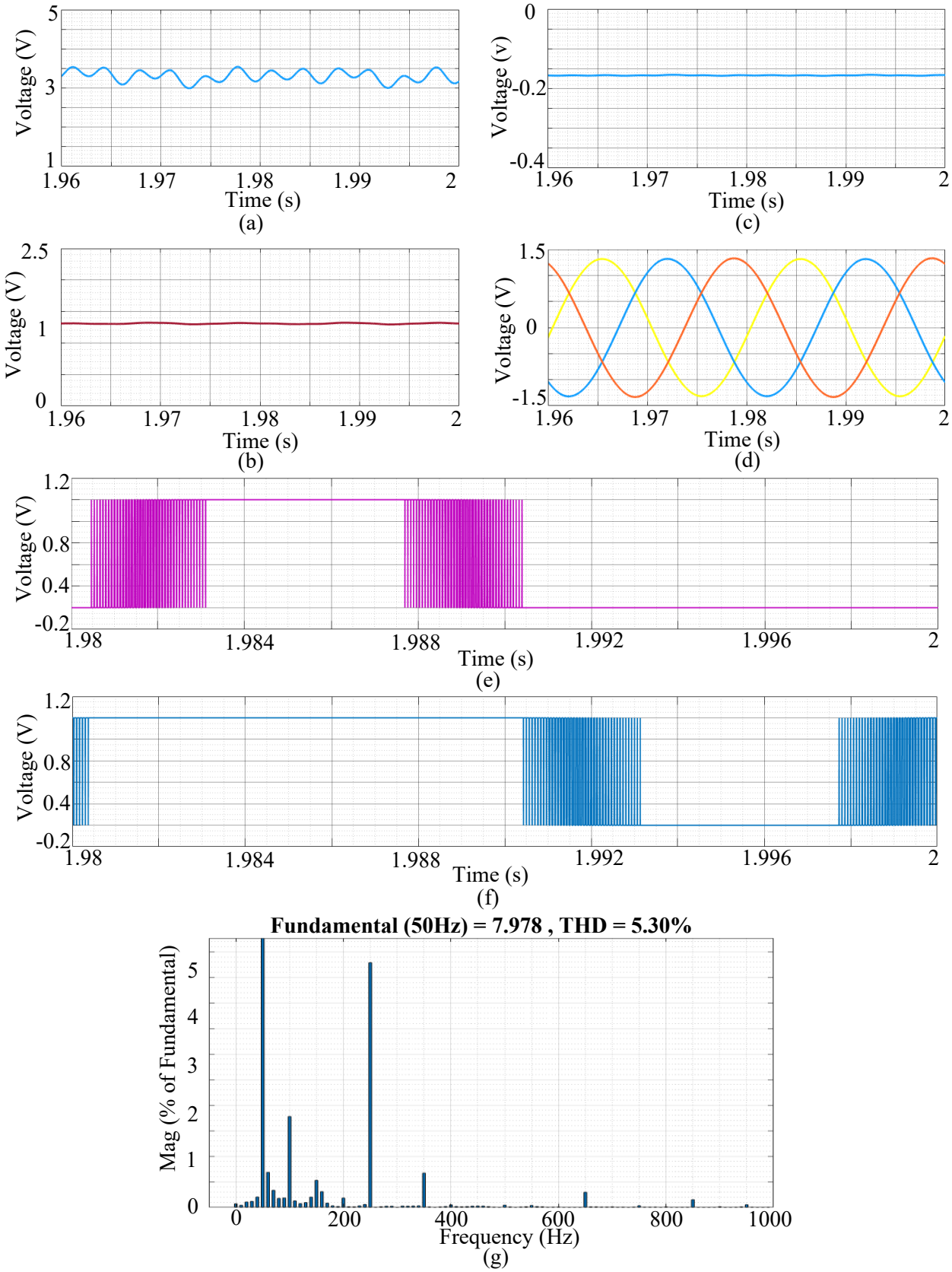

Fig. 16: (a) u_q, (b) m_d, (c) m_q, (d) m_{abc}, (e) S_{a1}, (f) S_{a2}, (g) FFT analysis of supply current i_a.

13. References

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