1.

a. Define half adder.

Ans: A form of combinational logic circuit known as the Half Adder adds two 1-bit binary digits.

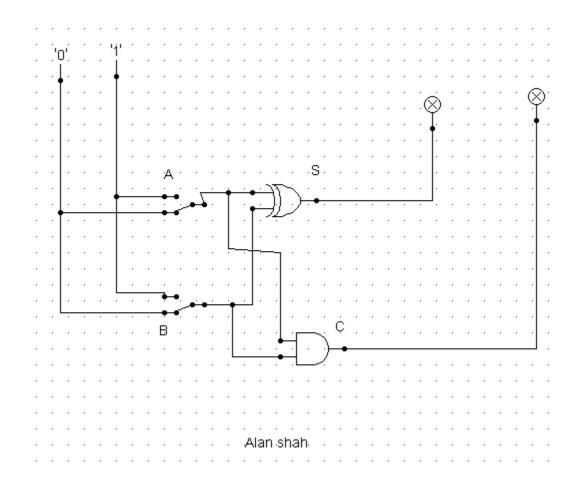
b. Draw a truth table for the sum and carry of half adder.

		J	
A	В	С	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

c. Write the sop expression from the truth table.

Ans:
$$S = x'y + xy'$$
, $C = xy$

d. Draw the circuit using logsim.



2.

a	Draw the ti	ruth table	for the	outputs	of the	full adder
а.	Diaw uic u	uui tabic	ioi tiic	Outputs	or the	rum auuci.

A	В	C-IN	S	C-OUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

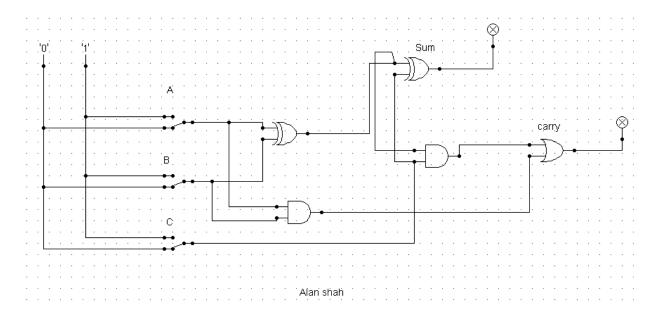
b. Write the corresponding sop expression for sum and carry of full adder and simplify the expression

Ans:

$$SUM = (A XOR B) XOR Cin = (A \oplus B) \oplus Cin$$

$$CARRY-OUT = A \ AND \ B \ OR \ Cin(A \ XOR \ B) = A.B + Cin(A \ \bigoplus \ B)$$

c. Draw a full adder using two half adders and an OR gate.



3. Using the three stages of design, construct the circuits for the following input /output values. Here A, B, and C are the inputs whereas D, E, F, G, H

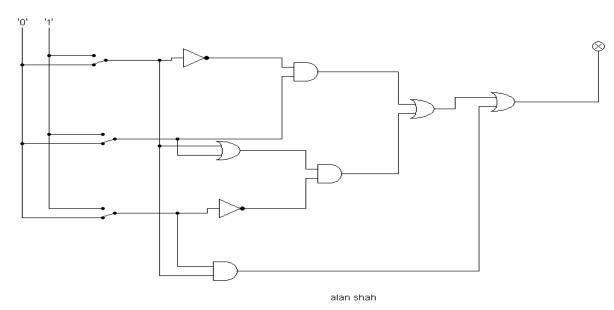
and I are the outputs. *Note: Draw a circuit diagram using logsim* corresponding to the simplified expression of outputs D, E, F, G, H, and I.

Α	В	С	D	E	F	G	Н	I
0	0	0	1	0	1	0	1	1
0	0	1	1	0	1	1	0	1
0	1	0	1	0	1	1	1	1
1	0	0	1	0	0	1	0	1
1	1	1	1	1	1	1	1	1
1	1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	1	0
0	1	1	0	0	0	1	1	1

Ans:

$$= A'B'(C'+C) + B(A'C'+AC') + AC(B+B') + AB'C'$$

$$=A'B+C'(B+A)AC$$

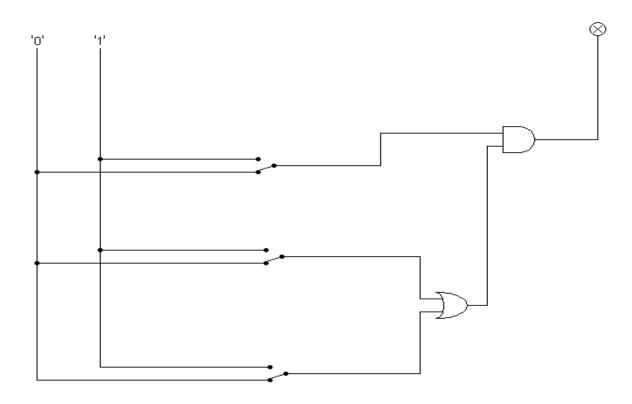


$$E = ABC + ABC' + AB'C$$

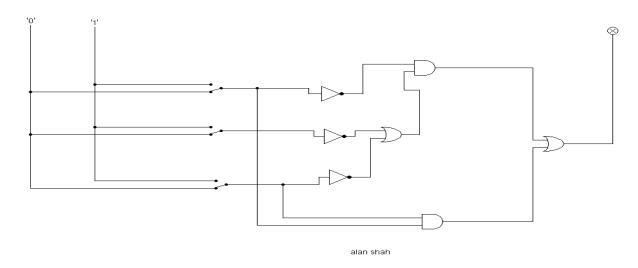
$$=AB(C+C')+AB'C$$

$$=A(B+B'C)$$

$$=A(B+C)$$



$$=A'(B'+C')+AC$$



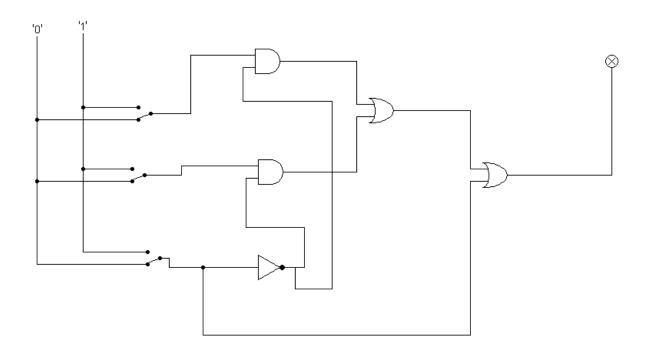
G=A'B'C+A'BC'+AB'C'+ABC+ABC'+AB'C+A'BC

$$=A'C(B'+B)+BC'(A'+A)+AC(B'+B)+AB'C'$$

$$=C(A'+A)+C'(B+AB')$$

$$=C+C'(B+A)$$

$$=C+C'B+AC'$$

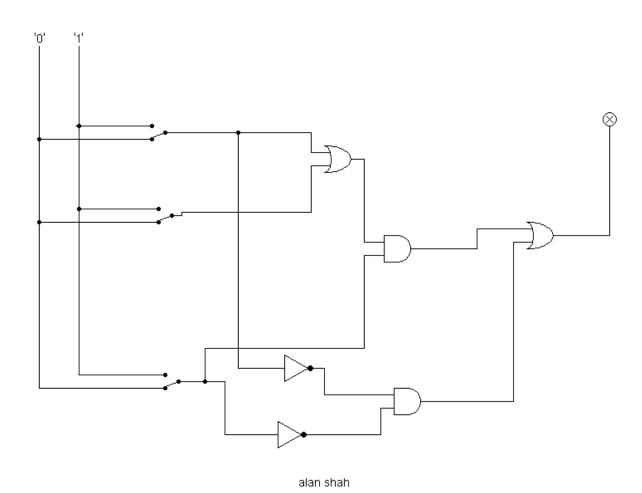


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$$=AC(B'+B)+A'C'(B'+B)+A'BC$$

$$=C(A'B+A)+A'C'$$

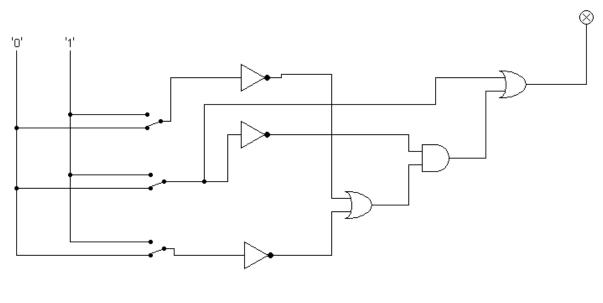
$$=C(A+B)+A'C'$$



I=A'B'C'+A'B'C+A'BC'+AB'C'+ABC+ABC'+A'BC

$$=B'C'(A'+A)+AB(C'+C)+A'B(C'+C)+A'B'C$$

$$=B(A+A')+B'(A'C+C')$$



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