GDAŃSK UNIVERSITY OF TECHNOLOGY

Subject card

| | | | |
|---|---|---|---|
| Subject name and code | Digital Technology - laboratory, PG_00047557 | | |
| Field of study | Automatic Control, Cybernetics and Robotics | | |
| Date of commencement of studies | October 2020 | Academic year of realisation of subject | 2020/2021 |
| Education level | first-cycle studies | Subject group | Obligatory subject group in the field of study |
| Mode of study | Full-time studies | Mode of delivery | at the university |
| Year of study | 1 | Language of instruction | Polish |
| Semester of study | 2 | ECTS credits | 4.0 |
| Learning profile | general academic profile | Assessment form | assessment |
| Conducting unit | Department of Automatic Control -> Faculty of Electronics, Telecommunications and Informatics | | |
| Name and surname of lecturer (lecturers) | Subject supervisor | dr inż. Marcin Pazio | |
| | Teachers | dr inż. Marcin Pazio<br>dr inż. Stefan Sieklicki<br>dr inż. Tomasz Merta<br>mgr inż. Marlena Gruba<br>dr inż. Stanisław Raczyński<br>mgr inż. Michał Drożdziel<br>mgr inż. Dawid Łukwiński<br>mgr inż. Karol Szymański<br>dr inż. Jarosław Magiera | |

Lesson types and methods of instruction

| Lesson type | Lecture | Tutorial | Laboratory | Project | Seminar | SUM |
|---|---|---|---|---|---|---|
| Number of study hours | 0.0 | 0.0 | 30.0 | 0.0 | 0.0 | 30 |

E-learning hours included: 0.0

Adresy na platformie eNauczanie:

Learning activity and number of study hours

| Learning activity | Participation in didactic classes included in study plan | Participation in consultation hours | Self-study | SUM |
|---|---|---|---|---|
| Number of study hours | 30 | 4.0 | 66.0 | 100 |

Subject objectives

The class of logic students acquire knowledge of:

- The mathematical systems used to describe iterative combination and sequence combination

- Introduction to binary, binary, Boolean algebra arytmetyka's logical functions

- Basic concepts, systems, systems iterative

- Synthesis of sequential iterative and sequence

- Synthesis of synchronous and asynchronous sequential Circuits

- memory

**Learning outcomes**

| Course outcome | Subject outcome | Method of verification |
|---|---|---|
| [K6_U06] can analyse the operation of components, circuits and systems related to the field of study, measure their parameters and examine technical specifications | Student after lab classes. The TC can design, according to the specified specification, and perform typical digital systems a simple device, object, system or process, using appropriately selected methods, techniques, tools and materials, using standards and Engineering standards, using technology-specific technologies and using the experience gained in an environment of professional engineering activities | [SU1] Assessment of task fulfilment |
| [K6_U03] can design, according to required specifications, and make a simple device, facility, system or carry out a process, specific to the field of study, using suitable methods, techniques, tools and materials, following engineering standards and norms, applying technologies specific to the field of study and experience gained in the professional engineering environment | Student after lab classes. The TC can design, according to the specified specification, and perform typical digital systems a simple device, object, system or process, using appropriately selected methods, techniques, tools and materials, using standards and Engineering standards, using technology-specific technologies and using the experience gained in an environment of professional engineering activities | [SU4] Assessment of ability to use methods and tools |

**Subject contents**

. TTL and CMOS gates testing 2. Designing, assembling and testing iterative circuits 3. Designing and assembling digital timing circuits 4. Designing synchronous sequential circuits 5. Assembling and testing synchronous sequential circuits 6. Designing counter modules 7. Assembling and testing counter modules 8. Designing, assembling and testing register modules 9. Designing asynchronous sequential circuits 10. Assembling and testing asynchronous sequential circuits 11. Microprogramming: coding data interchange between digital modules 12. Microprogramming: implementing the code from ex.11 13. Prototyping digital circuits: designing various projects 14. Assembling projects from ex.13 15. Prototyping: testing projects from ex.14

**Prerequisites and co-requisites**

No requirements

**Assessment methods and criteria**

| Subject passing criteria | Passing threshold | Percentage of the final grade |
|---|---|---|
| Realization of task | 50.0% | 50.0% |
| activity / presence | 50.0% | 50.0% |

**Recommended reading**

| | |
|---|---|
| Basic literature | R. F. Tinder, Engineering Digital Design J. D. Daniels, Digital Design from Zero to One Texas Instruments, Digital Design Seminar M. Barski, W. Jędruch, Digital Circuits W. Majewski, Logical Circuits Zieliński C .: Fundamentals of Digital Circuit Design, Wydawnictwo Naukowe PWN, Warsaw 2003 |
| Supplementary literature | Logical circuits Zieliński C .: Fundamentals of digital circuits design, Wydawnictwo Naukowe PWN, Warsaw 2003<br><br>logic circuits Stefan Sieklicki - script from the subject of Logical Circuits |
| eResources addresses | |

**Example issues/ example questions/ tasks being completed**

- Carry out the operation (10101)2 x (101) 2) the result reported in the decimal system,

- The function f(d,c,b,a)= Π (0, 3, 5, 8, 12, 14, (2,11,13)) achieved using a a multiplexer 4/1 and NAND Gates.

-Provide a table of trigger JK and D ,

- Design the table in a logical network to build the NAND Gate

- Design the synchronous presence or within binary digits given in the series in the number of ones is an even number other than zero, which should be indicated by setting the output in=1 for exactly one clock cycle.

Enter in the solution:

1. Graf and a table to access/exit created based on graph tables and minimum
2. function triggers excitations for pursuing more bits of triggers JK
3. minimum output
4. function schematic diagram

| | |
|---|---|
| Work placement | Not applicable |