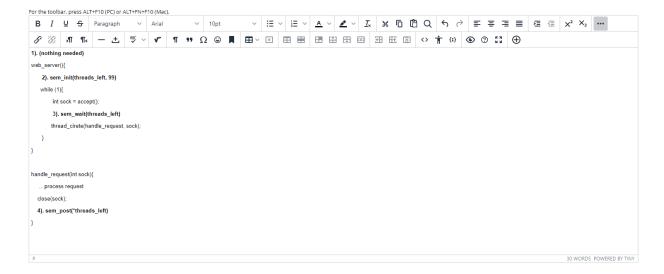


Here is an example of a web server using multi-threading. It creates a new thread to serve every request. Suppose you like to limit the resource consumption by allowing no more than 100 active threads simultaneously, how do you complete the code to realize this limit? (Hint: use semaphore(s). pseudo code is enough.)



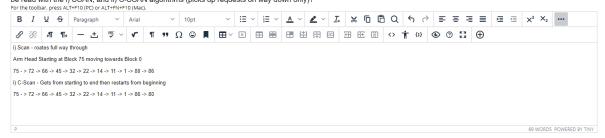
QUESTION 6 10 points 🗸 Saved

Consider that requests to read the following set of logical block numbers are enqueued to be served from a disk that has 100 logical blocks laid out sequentially from block 0 to block 90

{1, 22, 14, 72, 86, 32, 11, 66, 45, 80}

Assume that the seek time in moving the disk arm head from logical block i to block j is proportional to |i - j|.

Given that the arm head is currently positioned at block 75 and is in the midst of moving in the direction towards block 0, what is the sequence in which the enqueued blocks will be read with the i) SCAN, and ii) C-SCAN algorithms (picks up requests on way down only)?



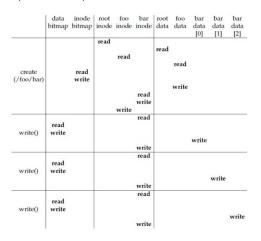
QUESTION 7

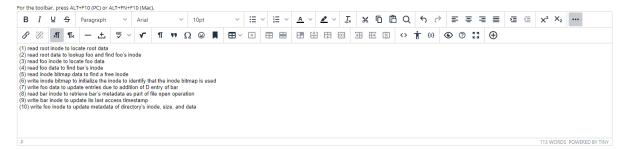
Consider a UNIX-style inode with 10 direct pointers, one single-indirect pointer, and one double-indirect pointer only. Assume that the block size is 8K bytes, and the size of a pointer is 4 bytes.

- a. What is the largest file size that can be indexed in this system?
- b. How many blocks (including indirect blocks) are needed to address a file of size 100 bytes, 10K bytes and 4G bytes?

QUESTION 8 10 points Served

Explain the first 10 steps in the timeline below for file write.



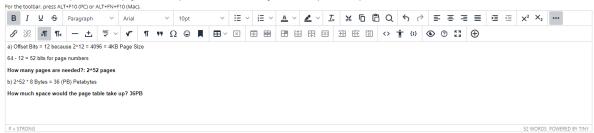


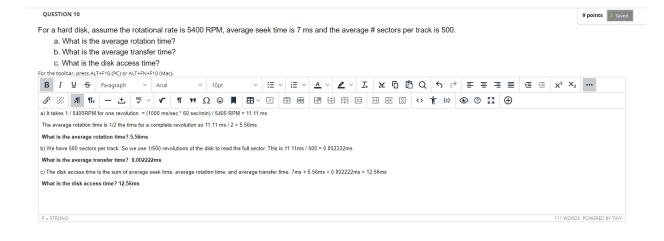
QUESTION 9 10 points Saved

Assume a single-level page table system with 4KB page size, 64-bit address and 8-byte PTE.

a. How many pages are needed?

b. How much space would the page table take up? Hint: think about how big the address space is; use power-of-two math.





15 points 🛷 Saved

Consider a processor with 16-bit address space and 4KB page size. Page Table is at 0x2000 and each PET is 4 bytes. Given a page table as follows,

VPN:0	0x0	
	0x0	1
PageTable	0x1	Ī
	0x9	Ī
	0x7	Ī
	0x8	
	0	
	:	1
VPN:15	0	Ī

QUESTION 11

Assume the CPU is about to execute the following instructions starting at virtual address 0x3000

0x3000: load 0x5320, %eax 0x3004: load 0x4004, %ebx 0x3008: mul %ecx, %eax, %ebx

- a. Assuming no TLB, how many memory accesses are needed? What are the physical addresses to be accessed?
- b. Assuming a TLB with no valid entry is in use at the beginning of the execution, how many memory accesses are needed?

a)

If the is 12 bits (because 4KB = 2\*12 bytes)

If the is 15 bits (because 4KB = 2\*12 bytes)

If the is 15 bits (because 4KB = 2\*12 bytes)

If the is 15 bits (because 4KB = 2\*12 bytes)

If the is 15 bits (because 4KB = 2\*12 bytes)

If the is 15 bits (because 4KB = 2\*12 bytes)

If the is 15 bits (because 4KB = 2\*12 bytes)

If the is 12 bits (because 4KB = 2\*12 bytes)

If the istal references this is 10 references

If the total references this is 10 references

If the istal references this is 10 references

If the total references this is 5 references.