Lab 4: Code Conversion

ECE218-L01

Alan Biju Palayil

TA: Muyu Yang

Lab Date: 1 Mar 21

Due Date: 8 Mar 21

Introduction

Purpose

Create an encoder that converts Natural-BCD code to Excess-3 BCD and a decoder that goes from Excess-3 to Natural BCD

Scope

Observe the output of the circuit to confirm whether the encoder and decoder convert code correctly.

Theory

Theoretical Basis

Many complex digital systems handle many different types of coding languages, so it is important that these systems are able to translate code into a language it is programmed to understand. To do this these systems need decoders to make the input understandable to the system and encoders to make the output understandable to whatever language is needed. This lab introduces this concept, which can be very complex, by having us create a circuit that converts Natural-BCD to Excess-3 BCD, a very simple conversion.

Preliminary Work

To prepare for this lab a circuit was designed, shown in Experimental Procedure section, using preset values for both the encoder and the decoder. The values were used to create Boolean expressions which were used to create the circuit diagrams.

Encoder Truth Table

Decimal	Natural BCD			Excess-3 BCD		
	A_2	A_1	A_0	Y_2	Y_1	Y_0
0	0	0	0	0	1	1
1	0	0	1	1	0	0
2	0	1	0	1	0	1
3	0	1	1	1	1	0
4	1	0	0	1	1	1
5	1	0	1	0	0	0
6	1	1	0	0	0	1
7	1	1	1	0	1	0

$$Y_2 = ((A_2A_1'A_0')' * (A_2'A_1)' * (A_2'A_0)')'$$

$$Y_1 = ((A_1'A_0')' * (A_1A_0)')'$$

$$Y_0 = A_0'$$

Decoder Truth Table

Decimal	Excess-3 BCD			Natural BCD		
	A_2	A_1	A_0	Y_2	Y_1	Y_0
0	0	1	1	0	0	0
1	1	0	0	0	0	1
2	0	0	1	0	1	0
3	1	1	0	0	1	1
4	1	1	1	1	0	0
5	0	0	0	1	0	1
6	1	0	1	1	1	0
7	0	1	0	1	1	1

$$Y_2 = ((A_2'A_1')' * (A_2'A_0')' * (A_2A_1A_0)')'$$

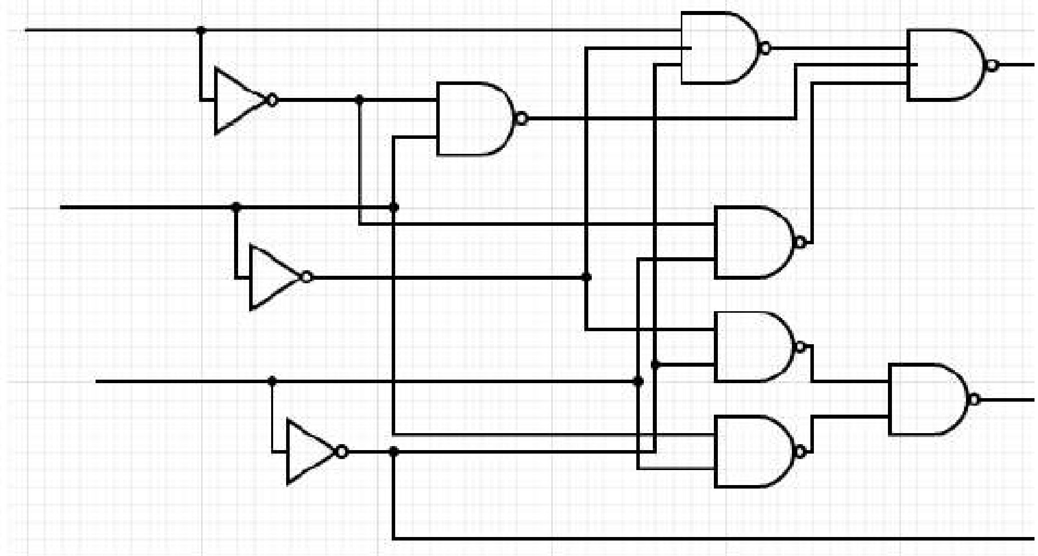
$$Y_1 = ((A_1'A_0)' * (A_1A_0')')'$$

$$Y_0 = A_0'$$

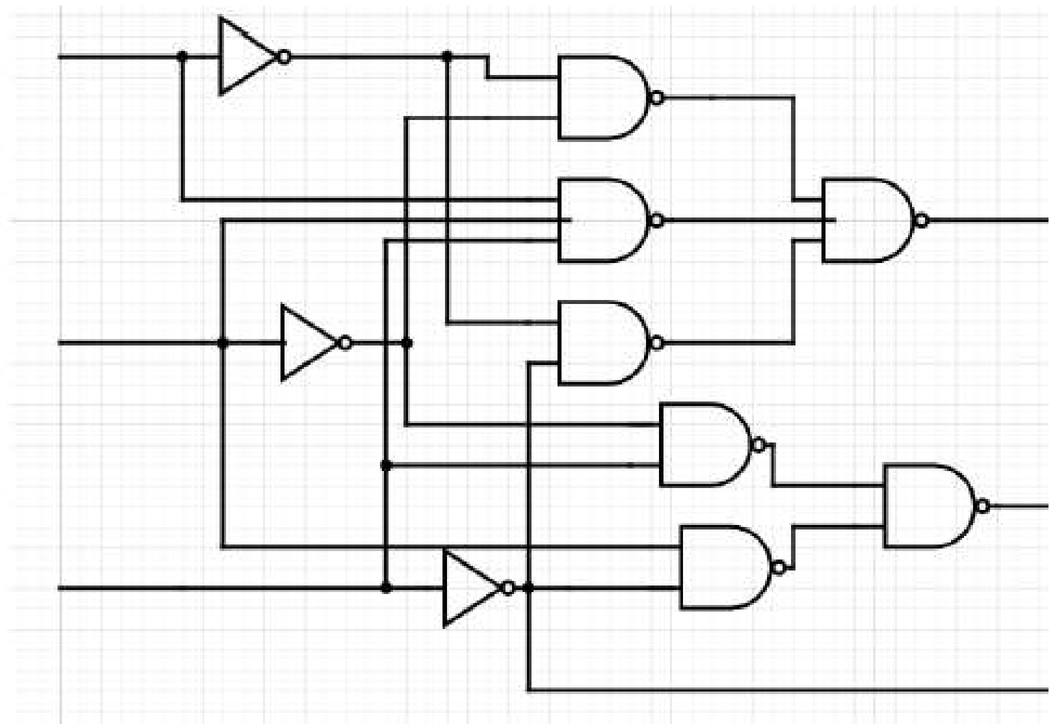
Experimental Procedure

Schematics (Circuit Diagram)

For the diagrams, the from top to bottom the inputs and outputs are A_2, A_1, A_0, and Y_2, Y_1, Y_0.



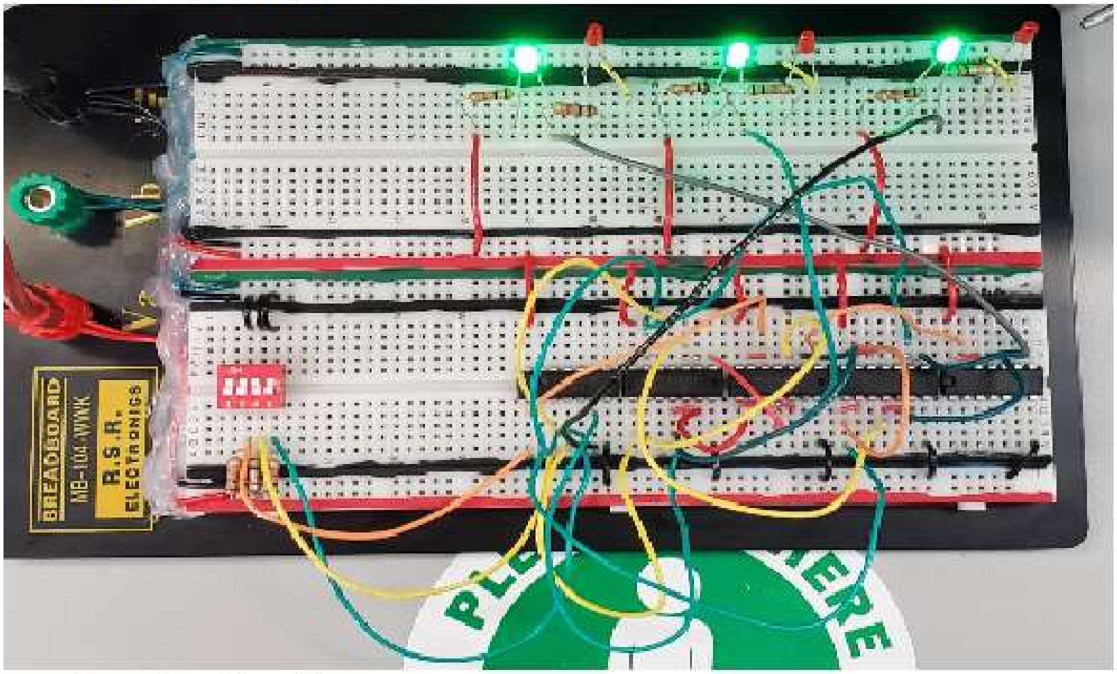
Encoder Diagram



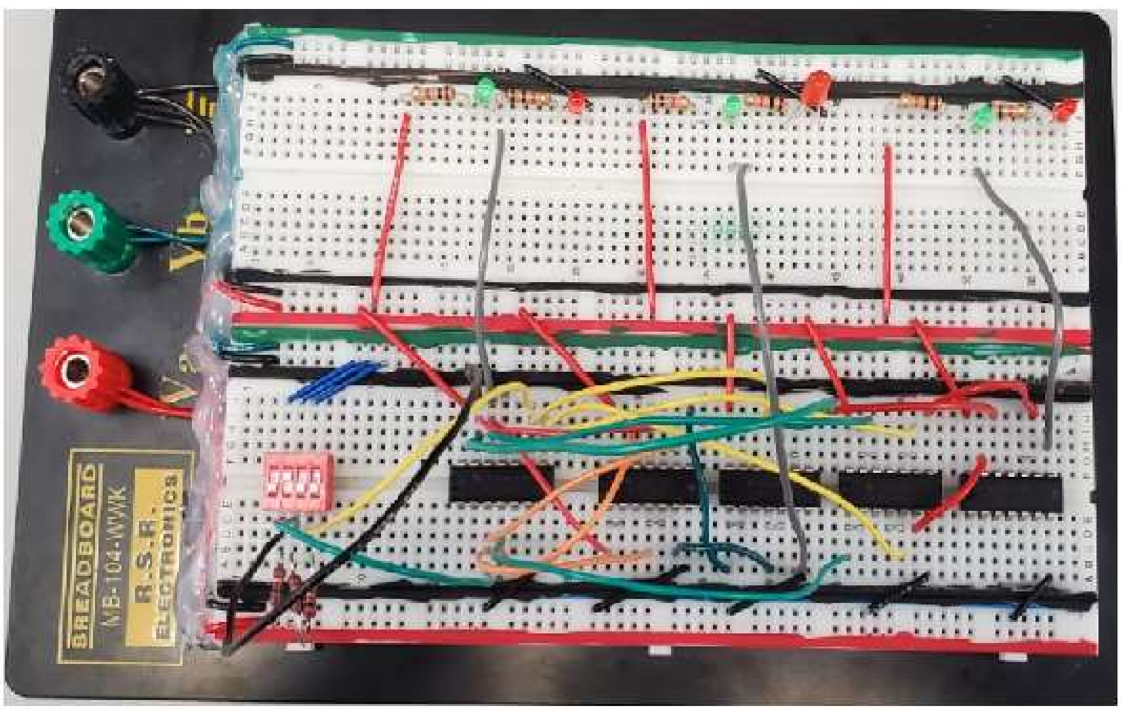
Decoder Diagram

Breadboard

Encoder Circuit:



Decoder Circuit:



Equipment

- Copper wire
- SN74LS04N Hex Inverter
- SN74LS32N Quad 2-Input OR Gate
- SN74LS20N Dual 4-Input NAND Gate
- 1KΩ±5% Resistor
- Red and green LEDs

Procedure

1. Set up breadboard depicted in Encoder Diagram on breadboard.
2. Set desktop voltage source to 5V and connect to breadboard.
3. Test and demonstrate the output to TA.
4. Repeat steps 1-3 with the Decoder Diagram.

Result

Despite the LEDs being switched on the breadboard the colors have the same meaning with red being LOW, or zero, and green being HIGH, or 1.

Encoder Data table

A_2	A_1	A_0	Y_2	Y_1	Y_0
0	0	0	RED	GREEN	GREEN
0	0	1	GREEN	RED	RED
0	1	0	GREEN	RED	GREEN
0	1	1	GREEN	GREEN	RED
1	0	0	GREEN	GREEN	GREEN
1	0	1	RED	RED	RED
1	1	0	RED	RED	GREEN
1	1	1	RED	GREEN	RED

Decoder Data table

A_2	A_1	A_0	Y_2	Y_1	Y_0
0	0	0	GREEN	RED	GREEN
0	0	1	GREEN	GREEN	RED
0	1	0	GREEN	GREEN	GREEN
0	1	1	RED	RED	RED
1	0	0	RED	RED	GREEN
1	0	1	RED	GREEN	RED
1	1	0	RED	GREEN	GREEN
1	1	1	GREEN	RED	RED

Interpretation

The results were a success with both the encoder and the decoder working as intended, correctly converting Natural-BCD code into Excess-3 BCD and vice versa.

Conclusion

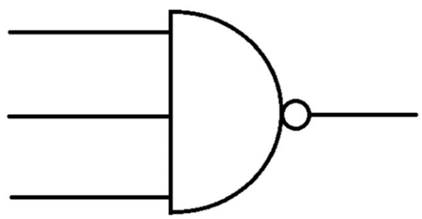
We can conclude that it is possible to encode Natural-BCD into Excess-3 BCD and to decode Excess-3 BCD back into Natural-BCD.

Post-Lab Questions

1. Draw the schematic of a simple logic function that returns 1 if the input is from 0 to 7, and 0 otherwise.

Decimal	Input			Output
D	A_2	A_1	A_0	Y
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0

$Y=(A_2A_1A_0)'$



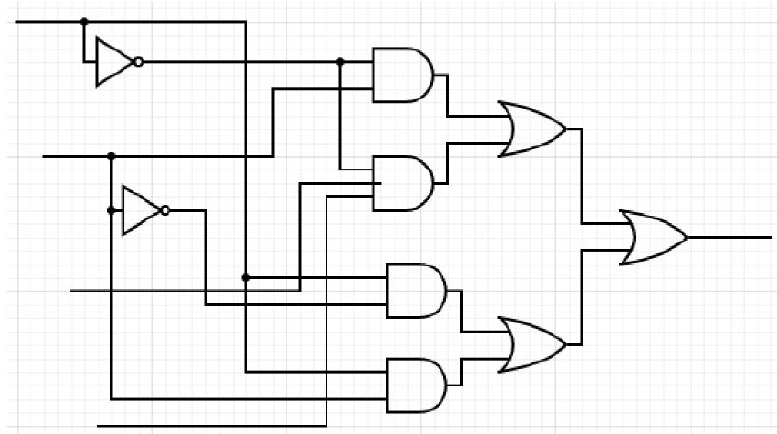
2. Draw the schematic of a simple logic function that returns 1 if the input is from 3 to 10, and 0 otherwise.

Decimal	Input				Output
D	A_3	A_2	A_1	A_0	Y
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	1
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	0

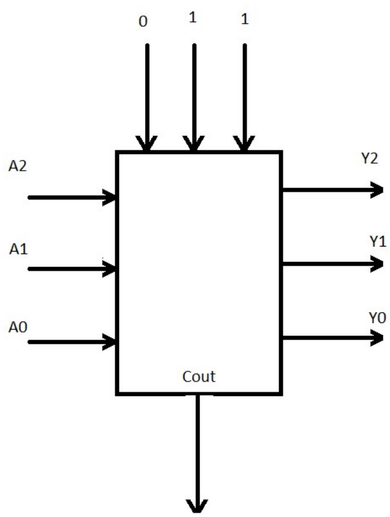
A_3A_2/A_1A_0	00	01	11	10
00	0	0	1	0
01	1	1	1	1
11	0	0	0	0
10	1	1	0	1

$Y = A_3'A_2 + A_3'A_1A_0 + A_3A_2'A_1 + A_3A_1$

The inputs from top to bottom are A_3, A_2, A_1, A_0.



3. Using a 3-bits adder, draw the schematic of the Excess-3 BCD encoder



4. Using a 3-bits adder, draw the schematic of the Excess-3 BCD decoder