

# ECE 218 Digital Systems

## Lab Final Exam

2021 Spring  
Electrical and Computer Engineering Department  
Illinois Institute of Technology

<b>Fall Name</b>	<b>First Name</b>	<b>Last Name</b>
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- This examination is an open book and open note exam.
- Discussion and Cell phones are not allowed.
- You will have 150 mins to complete this exam individually (8:10am — 10:40am).
- Part 1 (Written Test: Question 1 - 4) will be collected around 10:30am.
- Part 2 (Experiment Test: Question 5) need to be demonstrated to TA before 10:40am.
- Write your name and CWID on this page and on the top of each successive pages.
- Good Luck!

**Design a 3-bit Gray code counter with enable input EN, using D Flip-Flops and combinational logic gates. When EN is logic H, the counter should go through the counting sequence of a Gray code; When EN is logic L, the counter stays in the current state.**

Question 1: Draw the state diagram. (20 points)

Question 2: Draw the state transition table. (20 points)

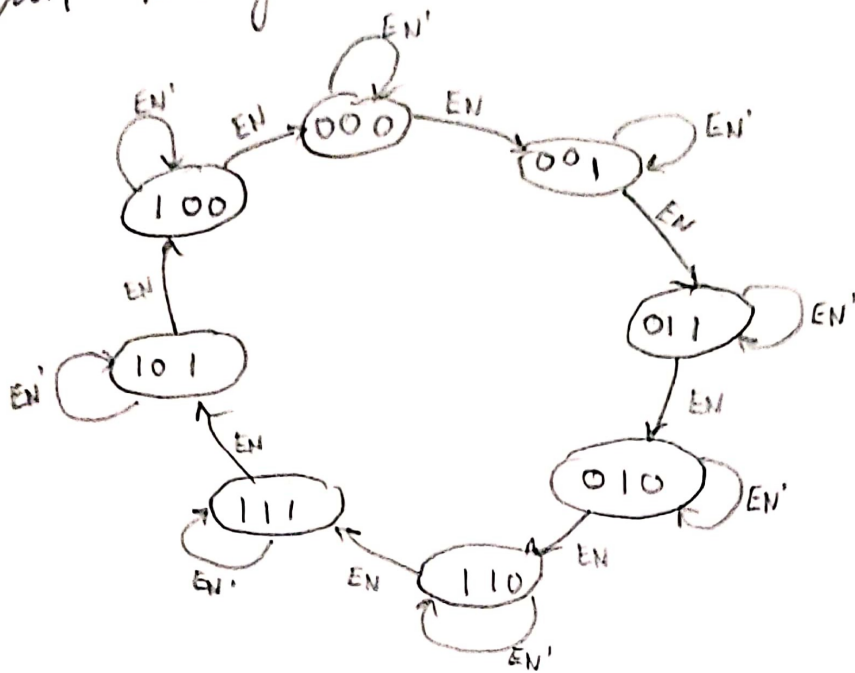
Question 3: Derive the equations for output literals  $D_A$ ,  $D_B$ , and  $D_C$  in terms of input literals EN,  $Q_A$ ,  $Q_B$ , and  $Q_C$  using K-map. (20 points)

Question 4: Design the 3-bit Gray code counter with enable using D flop-flops and combinational logic gates. Draw the schematic. (20 points)

Question 5: Realize the 3-bit Gray code counter with enable on the breadboard. Input EN controlled by a switch in an input circuit. Outputs  $D_A$ ,  $D_B$ , and  $D_C$  connects to three output circuits and show the results with LEDs. (20 points)

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Q.1)



State Diagram

Q.2)

Present State $Q_A Q_B Q_C$	Next State						D Flip-Flop			$\Sigma$		
	EN=1			EN=0			EN=1				EN=0	
	$q_A$	$q_B$	$q_C$	$q_A$	$q_B$	$q_C$	$D_A$	$D_B$	$D_C$	$D_A$	$D_B$	$D_C$
0 0 0	0	0	1	0	0	0	0	0	1	0	0	0
0 0 1	0	1	1	0	0	1	0	1	1	0	0	1
0 1 1	0	1	0	0	1	1	0	1	0	0	1	1
0 1 0	1	1	0	0	1	0	1	1	0	0	1	0
1 1 0	1	1	1	1	1	0	1	1	1	1	1	0
1 1 1	1	0	1	1	1	1	1	0	1	1	1	1
1 0 1	1	0	0	1	0	1	1	0	0	1	0	1
1 0 0	0	0	0	1	0	0	0	0	0	1	0	0

Transition Table

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Q.3)

$D_A$

$q_A q_B \backslash q_A E_n$	00	01	11	10
00	0	0	0	0
01	0	1	0	0
11	1	1	1	1
10	1	0	1	1

$$D_A = Q_B Q_C E_n + Q_A E_n + Q_A Q_C$$

$D_C$

$q_A q_B \backslash q_A E_n$	00	01	11	10
00	0	1	1	1
01	0	0	0	1
11	0	1	1	1
10	0	0	0	1

$$D_C = Q_B Q_C E_n + Q_A Q_C E_n + Q_C E_n$$

$D_B$

$q_A q_B \backslash q_A E_n$	00	01	11	10
00	0	0	1	0
01	1	1	1	1
11	1	1	0	1
10	0	0	0	0

$$D_B = Q_B E_n + Q_B Q_C + Q_A Q_C E_n$$



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Q4)

