Lab 6: Serial Adder

ECE218-L01

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Due Date: 12 Apr 21

Introduction

Purpose

Introduce the concept of shift registers and their parallel-to-serial and serial-to-parallel uses by designing and implementing a serial adder.

Scope

Observe the output of the circuit to confirm the functionality of the adder on 4 LEDs.

Theory

Theoretical Basis

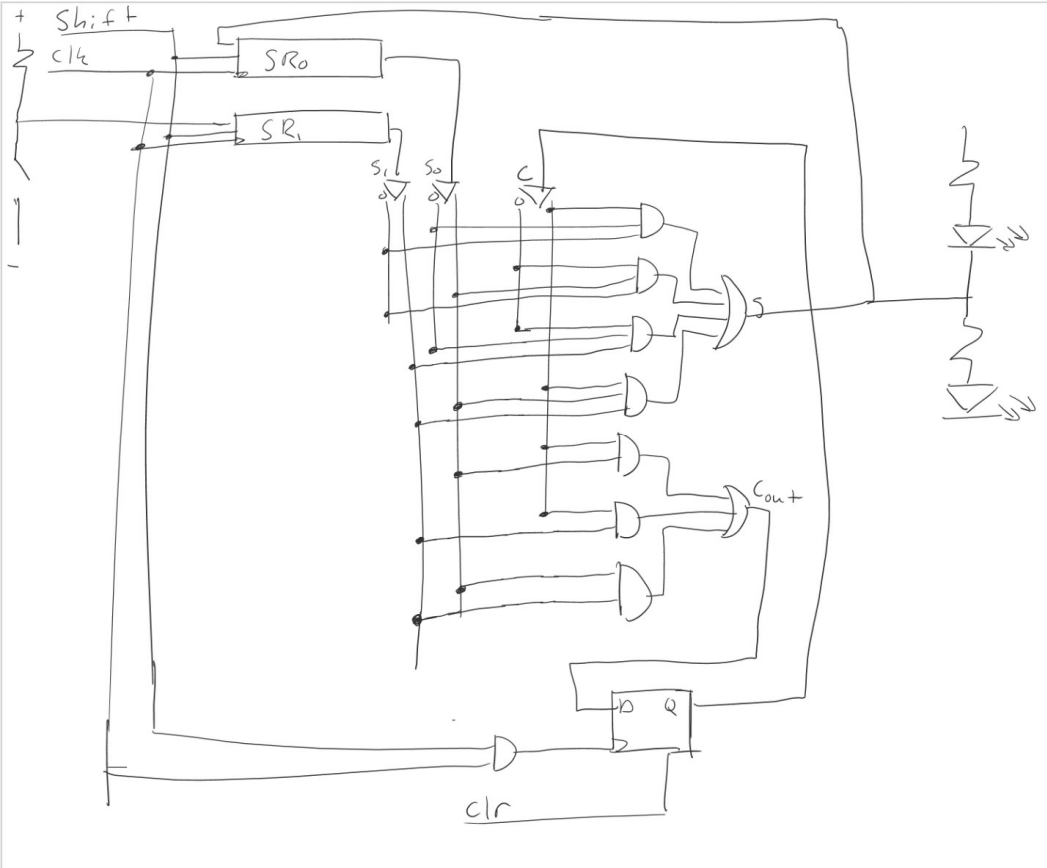
Shift registers are used to store and transmit data in a serial or parallel fashion. A serial shift register takes one bit at a time and shifts it down to store more data, a parallel shift register takes several bits at a time and can shift them to clear space and move data. For this lab we will use serial shift registers to store our data and shift it one bit at a time into our adder circuit.

Preliminary Work

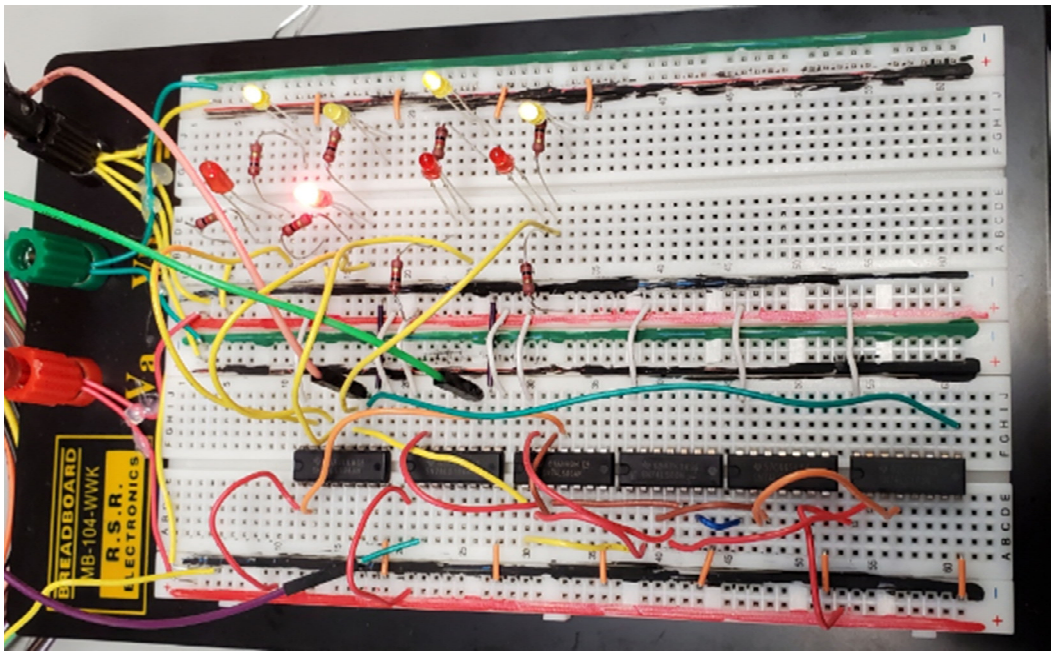
To prepare for this lab a circuit diagram was created, and a breadboard layout was designed which can be seen in the experimental procedure section. The actions needed to operate the adder were also laid out:

a) Set clear to high to begin use of flip-flops and shift registers.
b) Turn on waveform generator set to four cycles on trigger and input first number using switch starting with least significant bit.
c) Repeat step c for the second number.
d) Turn switches off and trigger waveform generator again, observe LEDs.

Experimental Procedure



Circuit diagram, the actual circuit used a simplified version of this layout.



The lab circuit was constructed in the second lab but was not performed in front of the TA.

Equipment:

- Copper wire
- 2 SN74LS175 Quad D Flip-Flops
- 2 SN75LS194 4-Bit Bidirectional Universal Shift Registers
- SN74LS32 Quad OR Gate
- SN75LS86 Quad XOR Gate
- 1kΩ±5% resistors
- Green and Red LEDs

Procedure

1. Build circuit shown in circuit diagram.
2. Set signal generator to:
    a. Pulse
    b. HI Level = 5V
    c. Low Level = 0V
    d. High-Z output
    e. Pulse width = 1s
    f. Duty cycle = 50%
    g. Turn on burst with 1 pulse per trigger
3. Test circuit using values in data table.
4. Demonstrate operation to TA

Results

Input A	Input B	Output
0111	0001	1000
0111	1000	1111
0110	0101	1011
1000	0001	1001
1000	1110	0110
0011	0010	0101

Interpretation

The circuit were a success with the adder outputting the correct value for each test case.

Conclusion

We can conclude that it is possible to construct a functioning full adder using universal shift registers.

Post-Lab Questions 1.