

Pre-lab Report 4

ECE 218- L01

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Preliminary Assignment

Excess-3 BCD Encoder

Decimal	Natural BCD			Excess-3 BCD		
	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>
0	0	0	0	0	1	1
1	0	0	1	1	0	0
2	0	1	0	1	0	1
3	0	1	1	1	1	0
4	1	0	0	1	1	1
5	1	0	1	X	X	X
6	1	1	0	X	X	X
7	1	1	1	X	X	X

A <sub>2</sub> /A <sub>1</sub> A <sub>0</sub>	00	01	11	10
0	0	1	1	1
1	1	X	X	X

$$Y_2 = A_2A_0' + A_2'A_0 + A_1$$

A <sub>2</sub> /A <sub>1</sub> A <sub>0</sub>	00	01	11	10
0	1	0	1	0
1	1	X	X	X

$$Y_1 = A_1'A_0' + A_1A_0$$

A <sub>2</sub> /A <sub>1</sub> A <sub>0</sub>	00	01	11	10
0	1	0	0	1
1	1	X	X	X

$$Y_0 = A_0'$$

Natural BCD			Intermediary Functions					Excess-3 BCD		
A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	A <sub>0</sub> '	A <sub>1</sub> 'A <sub>0</sub> '	A <sub>1</sub> A <sub>0</sub>	A <sub>2</sub> A <sub>0</sub> '	A <sub>2</sub> 'A <sub>0</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>
0	0	0	1	1	0	0	0	0	1	1
0	0	1	0	0	0	0	1	1	0	0
0	1	0	1	0	0	0	0	0	0	1
0	1	1	0	0	1	0	1	1	1	0
1	0	0	1	1	0	1	0	1	1	1
1	0	1	0	0	0	0	0	0	0	0
1	1	0	1	0	0	1	0	1	0	1
1	1	1	0	0	1	0	0	0	1	0

Excess-3 BCD Decoder

Decimal	Excess-3 BCD			Natural BCD		
	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>
0	0	1	1	0	0	0
1	1	0	0	0	0	1
2	0	0	1	0	1	0
3	1	1	0	0	1	1
4	1	1	1	1	0	0
5	0	0	0	1	0	1
6	1	0	1	1	1	0
7	0	1	0	1	1	1

A <sub>2</sub> /A <sub>1</sub> A <sub>0</sub>	00	01	11	10
0	1	0	0	1
1	0	1	1	0

$$Y_2 = A_2A_0 + A_2'A_0'$$

A <sub>2</sub> /A <sub>1</sub> A <sub>0</sub>	00	01	11	10
0	0	1	0	1
1	0	1	0	1

$$Y_1 = A_1'A_0 + A_1A_0'$$

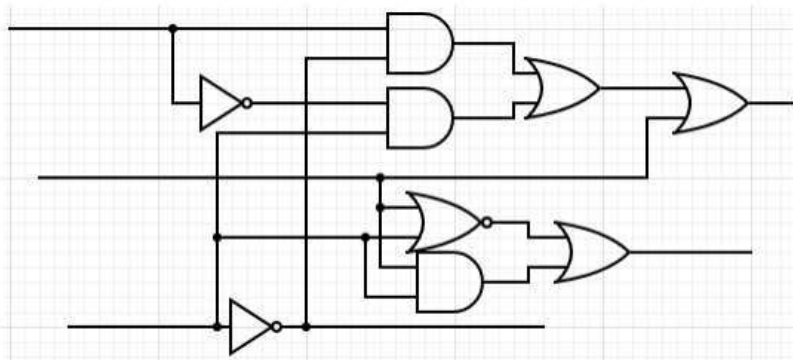
A <sub>2</sub> /A <sub>1</sub> A <sub>0</sub>	00	01	11	10
0	1	0	0	1
1	1	0	0	1

$$Y_0 = A_0'$$

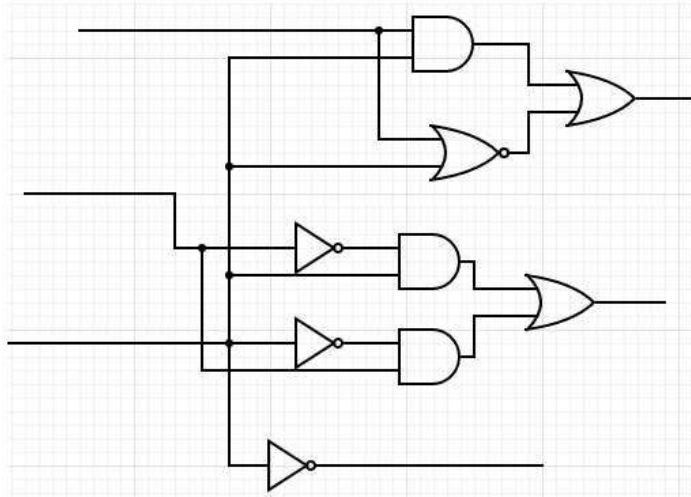
Excess-3			Intermediary				BCD		
A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	A <sub>2</sub> A <sub>1</sub> A <sub>0</sub>	A <sub>1</sub> 'A <sub>0</sub>	A <sub>1</sub> A <sub>0</sub> '	A <sub>0</sub> '	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>
0	1	1	0	0	0	0	0	0	0
1	0	0	0	0	0	1	0	0	1
1	0	1	0	1	0	0	0	1	0
1	1	0	0	0	1	1	0	1	1
1	1	1	1	0	0	0	1	0	0

## Schematics

Inputs and outputs from top to bottom are A<sub>2</sub>, A<sub>1</sub>, A<sub>0</sub> and Y<sub>2</sub>, Y<sub>1</sub>, Y<sub>0</sub>, respectively.



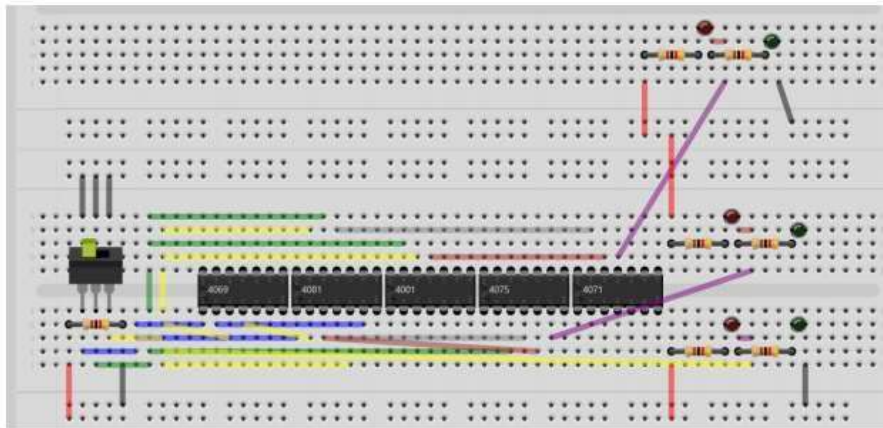
Encoder Circuit



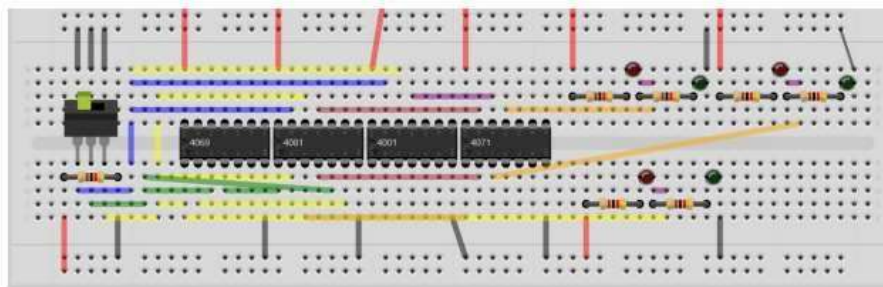
Decoder Circuit

### Breadboard Layout

I have color coded my inputs  $A_2$ ,  $A_1$ , and  $A_0$  with blue, green, and yellow, respectively. The 4069 chip is an inverter, the 4081 is a 2-input AND gate, the 4001 is a 2-input NOR gate, the 4075 is a 3-input OR gate, and the 4071 is a 2-input OR gate.



Encoder Breadboard



Decoder Breadboard

## Data Table

### Encoder

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	LED 1 (Y <sub>2</sub> )	LED 2 (Y <sub>1</sub> )	LED 3 (Y <sub>0</sub> )
LOW	LOW	LOW			
LOW	LOW	HIGH			
LOW	HIGH	LOW			
LOW	HIGH	HIGH			
HIGH	LOW	LOW			
HIGH	LOW	HIGH			
HIGH	HIGH	LOW			
HIGH	HIGH	HIGH			

### Decoder

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	LED 1 (Y <sub>2</sub> )	LED 2 (Y <sub>1</sub> )	LED 3 (Y <sub>0</sub> )
LOW	LOW	LOW			
LOW	LOW	HIGH			
LOW	HIGH	LOW			
LOW	HIGH	HIGH			
HIGH	LOW	LOW			
HIGH	LOW	HIGH			
HIGH	HIGH	LOW			
HIGH	HIGH	HIGH			