Lab 4: Memory Design Using Static RAM

ECE 441-02, Thursday Lab (L02)

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Acknowledgement: I acknowledge all the work (including figures and code) belong to me and/or persons who are referenced:

Signature: *Neil Dhote*

Purpose:

The purpose of this lab is to familiarize the student with the following topics: MC68000's Asynchronous Bus Control Signals, Static RAM, Open Collector Devices, SANPER-1 ELU's Block Select Lines.

Background:

The following material should be reviewed by student:

- MC68000 Asynchronous Bus Interface
- SRAM Devices
- Open Collector Devices
- SANPER-1 ELU's Block Select Lines
- SANPER-1 User's Manual

Equipment:

- SANPER-1 ELU
- PC with TUTOR Software
- Easy68K Software
- Wires
- Breadboard
- MCM2114 Static Random Access Memory Chip
- 74LS00 NAND Chip
- 74LS02 NOR Chip
- 74LS04 Inverter Chip
- 74LS05 Open Collector Inverter Chip
- 74LS74 D Flip-Flop Chip
- 74LS138 Decoder Chip
- Power Supply Unit
- Multimeter
- Mixed Signal Oscilloscope

Procedure:

Refer to Lab Manual for detailed Procedure

Results and Analysis:

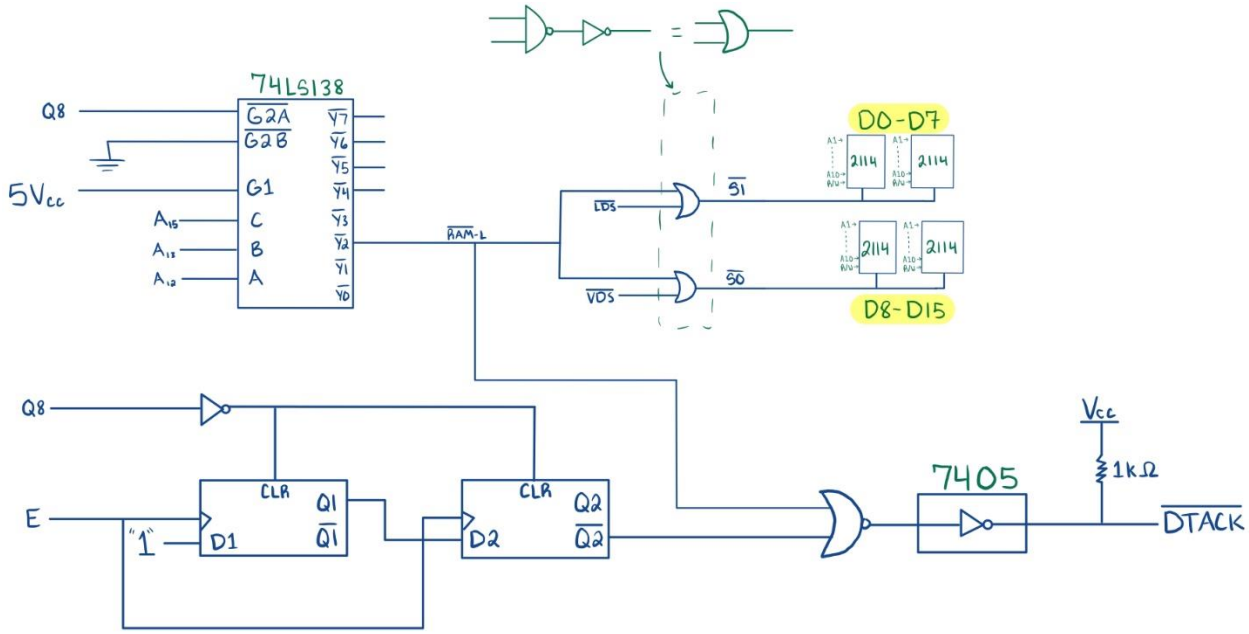
```
TUTOR 1.3 > MM 82000
1E15 00082000 1E14
BUS TRAP ERROR
PC=000093C6 SR=2709=.S7.N..C US=7BFF797B SS=00000782
D0=00382030 D1=05EE4D4D D2=3E142000 D3=00000000
D4=00000030 D5=00000000 D6=00000001 D7=000001FF
A0=000080B6 A1=00008354 A2=00000414 A3=00000554
A4=00082000 A5=00000540 A6=0000054A A7=00000782
----------0093C6 2007 MOVE.L D7,D0
TUTOR 1.3 > MM 82000
1E15 00082000 1E14
BUS TRAP ERROR
PC=000093C6 SR=2709=.S7.N..C US=7BFF797B SS=00000782
D0=00382030 D1=05EE4D4D D2=3E142000 D3=00000000
D4=00000030 D5=00000000 D6=00000001 D7=000001FF
A0=000080B6 A1=00008354 A2=00000414 A3=00000554
A4=00082000 A5=00000540 A6=0000054A A7=00000782
----------0093C6 2007 MOVE.L D7,D0
TUTOR 1.3 > MM 82000
082000 00 ff
ERROR
TUTOR 1.3 > MM $82000
082000 00 ?FF
082001 07 ?.
TUTOR 1.3 > MM $82000
082000 FF ?
082001 07 ?56
082002 00 ?.
TUTOR 1.3 > BT 82000 827FE
PHYSICAL ADDRESS=00082000 000827FE
FAILED AT 082160 WROTE=FFFF READ=FFDF
TUTOR 1.3 > BT 82000 827FE
PHYSICAL ADDRESS=00082000 000827FE
FAILED AT 0820E0 WROTE=FFFF READ=FF5F
TUTOR 1.3 > MM 82160
082160 FF ?67
082161 FF ?56
082162 FF ?.
TUTOR 1.3 > MM 82160
082160 67 ?
082161 56 ?
082162 FF ?
```

```
082163 FF ?.
TUTOR 1.3 > LO1
S021000036384B50524F472020203230435245415445442042592045415359363 84B6D
S11509004D454D4F525920544553542050415353454 4C8
S12310002A7C000820002C7C000827FE1AFC00AABDCD66F82A7C000820000C1500AA660082
S1231020002E1AFC0055BDCD66F02A7C000820000C1500556600004A1AFC00AABDCD66F09F
S12310404BF809004DF809124EF9000010AC2C7C00002000200D1E3C00E74E4E1CFC0020D3
S12310601CFC00411CFC00411CFC002010151E3C00E94E4E2A7C000020004EF9000010ACB5
S12310802C7C00002000200D1E3C00E74E4E1CFC00201CFC00351CFC00351CFC002010154B
S11D10A01E3C00E94E4E2A7C000020001E3C00F34E4E1E3C00E44E4EFFFFCC
S10510B8FFFF34
S804001000EB
TUTOR 1.3 > G $1000
PHYSICAL ADDRESS=00001000
MEMORY TEST PASSED
TUTOR 1.3 >

WHAT
TUTOR 1.3 > G 1000
PHYSICAL ADDRESS=00001000
082000 55 D5
TUTOR 1.3 > G 1000
PHYSICAL ADDRESS=00001000
MEMORY TEST PASSED
```

Discussion Questions:

1) Schematic Diagram of Hardware Design:



2) Fully commented listing of the memory test program:

```
ORG     $900

MSGPAS:     DC.B    'MEMORY TEST PASSED'
MSGENP:     DC.B

    ORG     $1000

START:

    MOVE.L  #$82000,A5 ; limits of memory
    MOVE.L  #$827FE,A6

FILL_AA:

    MOVE.B  #$AA,(A5)+ ; AA to memory
    CMPA.L  A5,A6 ; see if reached memory limit
    BNE     FILL_AA ; loop if not
    MOVE.L  #$82000,A5

CHECK_AA:

    CMP.B   #$AA,(A5) ; see if memory contents = AA
    BNE     NOT_AA
```

```
    MOVE.B  #$55,(A5)+ ; set memory to 55
    CMP.L   A5,A6 ; see if reached memory limit
    BNE     CHECK_AA
    MOVE.L  #$82000,A5

CHECK_55:

    CMP.B   #$55,(A5) ; see if memory contents = 55
    BNE     NOT_55
    MOVE.B  #$AA,(A5)+ ; set memory to AA
    CMPA.L  A5,A6
    BNE     CHECK_55
    LEA     MSGPAS,A5 ; load string into A5
    LEA     MSGENP,A6 ; load into A6
    JMP     OUTPUT ; if successful, output string

NOT_AA:

    MOVE.L  #$2000,A6 ; load into A6
    MOVE.L  A5,D0
    MOVE.B  #231,D7 ; covert 6 hex digits to ASCII
    TRAP    #14
    MOVE.B  #$20,(A6)+ ; ASCII for space
    MOVE.B  #$41,(A6)+ ; ASCII for A
    MOVE.B  #$41,(A6)+ ; ASCII for A
    MOVE.B  #$20,(A6)+ ; ASCII for space
    MOVE.B  (A5),D0
    MOVE.B  #233,D7 ; convert 2 hex digits to ASCII
    TRAP    #14
    MOVE.L  #$2000,A5
    JMP     OUTPUT ; jump to the output that has string ' AA '

NOT_55:

    MOVE.L  #$2000,A6
    MOVE.L  A5,D0
    MOVE.B  #231,D7 ; covert 6 hex digits to ASCII
    TRAP    #14
    MOVE.B  #$20,(A6)+ ; ASCII for space
    MOVE.B  #$35,(A6)+ ; ASCII for 5
    MOVE.B  #$35,(A6)+ ; ASCII for 5
    MOVE.B  #$20,(A6)+ ; ASCII for space
    MOVE.B  (A5),D0
    MOVE.B  #233,D7
    TRAP    #14
    MOVE.L  #$2000,A5
```

```
OUTPUT:

    MOVE.B  #243,D7 ; output String
    TRAP    #14
    MOVE.B  #228,D7 ; return control to TUTOR
    TRAP    #14

    SIMHALT             ; halt simulator

    END    START
```

3) Discuss which address range you chose for the memory bank and elaborate on the reasons for your selection.

I chose the memory address range of $82000-$827FF because it was available and not being used by any other devices and the range could also accommodate the RAM chips.

4) Discuss the reasons for implementing memory tests. What conditions are you actually testing the hardware for?

Memory tests ensure that the memory works properly. Different edge timing cases could affect results by causing errors in reading and writing to the memory. Some examples of tests that could be used are storing the correct data, memory being able to retain data, being able to read the data correctly, and obtaining DTACK.

5) Suggest some other bit patterns that could in used in a memory test program, and explain the reasons for your selections.

Other bit patterns that could be used in a memory test program are $00FF and$FF00, which would allow the upper and lower data byte reads and writes to be tested as well.

6) List the advantages and disadvantages of using Static RAMs over other types of memory devices such as EPROMS, Dynamic RAMs, etc.

The advantage of Static RAM is that it does not require a periodic refresh to retain data. A disadvantage is that is volatile, which means that data will be lost when it loses power. Dynamic RAM, by contrast, uses capacitors to store each bit and is also volatile. EPROMs allow the retention of data when power is lost since it is a form of non-volatile memory but is read-only and wouldn't be able to handle writing to it, at least not as easily as with Static RAM.