Lab 5: Input Output Design and Interrupt Handling

ECE 441-02, Thursday Lab (L02)

Alan Palayil

TA: Xinrui

Lab Date: 04-14-2022

Due Date: 05-01-2022

Purpose:

The purpose of this experiment is to introduce the user to the concepts of memory mapped I/O and interrupts.

Background:

The following material should be reviewed by student:

- Memory-Mapped I/O
- Interrupts
- SANPER-1 User's Manual

Equipment:

- SANPER-1 ELU
- PC with TUTOR Software
- Easy68K Software
- 2x SN74LS373N Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops
- 2x MAN74 7 Segment Displays
- 1x 76RSB08 8-Positions DIP Switch
- 8x 1kΩ Pull-Up Resistors
- 1x SN74LS04 Hex Inverter
- 1x SN74LS05 Hex Inverter with Open Collector Outputs
- SN74LS02 NOR Gate
- SN74LS00 NAND Gate

Procedure:

Refer to Lab Manual for detailed Procedure

Results and Analysis:

TUTOR 1.3 > LO1
S021000036384B50524F472020203230435245415445442042592045415359363 84B6D
S123200042844285428722 7C0006E0007A01181112841E04040700996700002C44FC00000F
S1232020C90513C40006E000223C0000C3504EB90000203660DC0C81000000006F00000605
S1112040538160F24E752E3C000000E44E4EBB
S804002000DB
TUTOR 1.3 > MM 6E000
06E000 25 ?.
TUTOR 1.3 > MM 7C

```
00007C 00 ?
00007D 00 ?
00007E 20 ?.
TUTOR 1.3 >
UT E TRAP ERROR
PC=84D82700 SR=0000=..0..... US=7FFF7FFF SS=00000750
D0=0000012E D1=00000000 D2=61000120 D3=00000000
D4=00000099 D5=00000001 D6=00000001 D7=000000E4
A0=00010040 A1=0006E000 A2=00000754 A3=0000054A
A4=0000007E A5=00000540 A6=00000540 A7=7FFF7FFF
4CD5 84D82700 4CD4
BUS TRAP ERROR
PC=0000896A SR=2704=.S7..Z.. US=7FFF7FFF SS=00000782
D0=7F467F46 D1=00000000 D2=61007FFF D3=00000053
D4=00000099 D5=00000001 D6=00000008 D7=61000141
A0=00000750 A1=7FFF7FFF A2=00000414 A3=00000428
A4=84D82700 A5=00000540 A6=00000554 A7=00000782
----------00896A 61003108 BSR.L $00BA74
TUTOR 1.3 > MM 6E000
06E000 25 ?
06E001 FF ?
06E002 21 ?
06E003 FF ?
06E004 21 ?
06E005 FF ?
06E006 21 ?
06E007 FF ?
06E008 21 ?
06E009 FF ?
06E00A 21 ?
06E00B FF ?
06E00C 21 ?.
TUTOR 1.3 > LO1
S021000036384B50524F472020203230435245415445442042592045415359363 84B6D
S123200042844285428722 7C0006E0007A01181112841E04040700996700002C44FC00000F
S1232020C90513C40006E000223C0000C3504EB90000203660DC0C81000000006F00000605
S1092040538160F24E75AD
S804002000DB
TUTOR 1.3 > G 2000
PHYSICAL ADDRESS=00002000
UT E TRAP ERROR
PC=84D82700 SR=0000=..0..... US=7FFF7FFF SS=0000077E
D0=7F467F46 D1=00000000 D2=61007FFF D3=00000053
D4=00000099 D5=00000001 D6=00000008 D7=000000E4
```

A0=00000750 A1=0006E000 A2=00000414 A3=00000428
A4=84D82700 A5=00000540 A6=00000554 A7=7FFF7FFF
4CD5 84D82700 4CD4
BUS TRAP ERROR

PC=0000896A SR=2704=.S7..Z.. US=7FFF7FFF SS=00000782
D0=7F467F46 D1=00000000 D2=61007FFF D3=00000053
D4=00000099 D5=00000001 D6=00000008 D7=61007F41
A0=0000077E A1=7FFF7FFF A2=00000414 A3=00000428
A4=84D82700 A5=00000540 A6=00000554 A7=00000782
----------00896A 61003108 BSR.L $00BA74

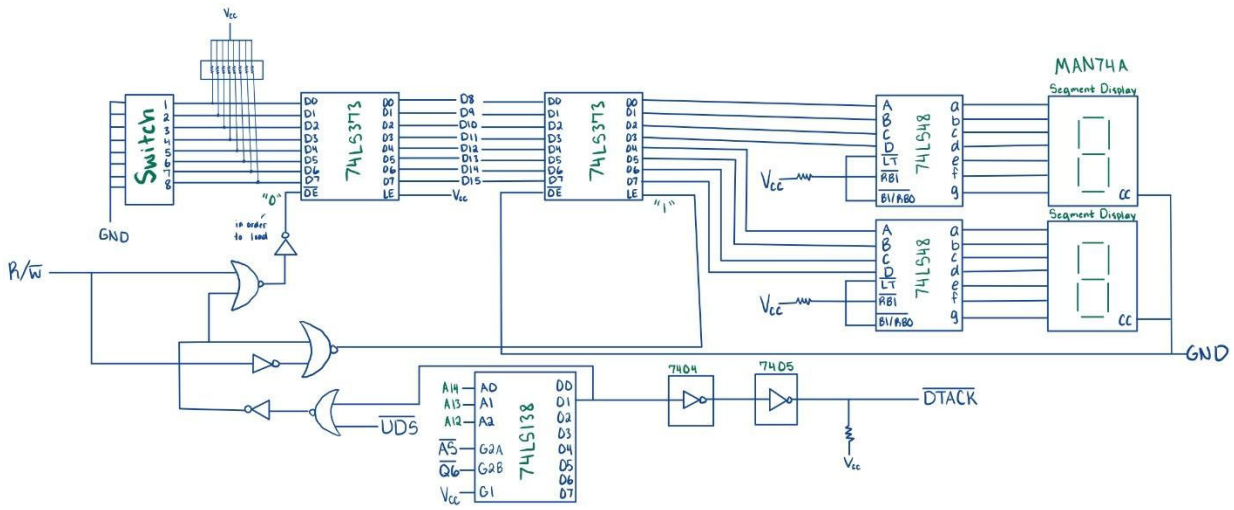
Discussion Questions:

1) A commented listing for the programs of Prelim #3.

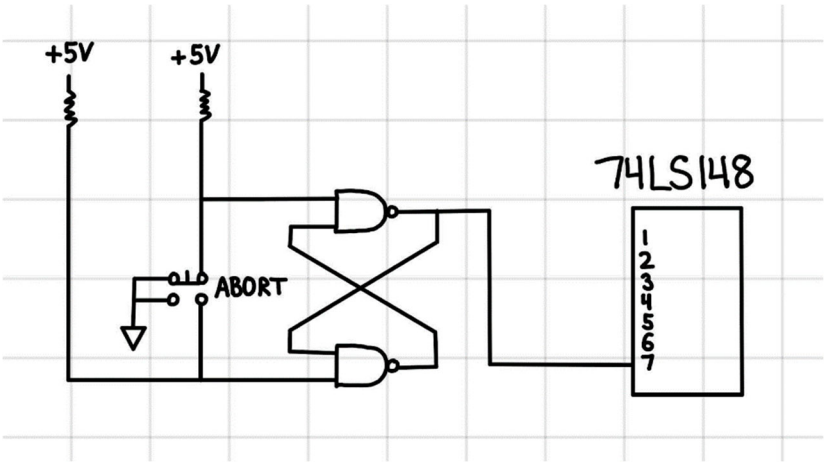
```
ORG    $2000

START:
    CLR.L   D4
    CLR.L   D5
    CLR.L   D7
    MOVE.L  #$06E000, A1
    MOVEQ   #$01, D5

    MOVE.B  (A1),D4
    MOVE.B  D4,(A1)

COUNTER:
    MOVE.B  D4, D7
    SUB.B   #$99, D7
    BEQ     DONE
    MOVE.W  #0, CCR
    ABCD    D5, D4

    MOVE.B  D4,$06E000

    MOVE.L  #50000, D1
    JSR     PAUSE

    BRA     COUNTER

PAUSE:
    CMPI.L  #0, D1
    BLE     PAUSERET
    SUBQ.L  #1, D1
```

```
    BRA     PAUSE

PAUSERET:
    RTS

DONE:
    MOVE.L  #228, D7
    TRAP    #14

    END     START
```

2) A schematic diagram of your hardware design for Prelim #1.



3) Review Chapter 7, "Hardware Description" of the Motorola Educational Computer Board User's Manual. Also, review Chapter 8 and examine Figure 8-3, Sheet 2 of 3 of the MC68000 Educational Computer Board Schematic Diagram and redraw only the ABORT switch circuitry. Describe in detail how this ABORT Switch circuitry operates.



4) The Exception Vector Table has vectors assigned for Uninitialized Interrupts and Spurious Interrupts. Discuss how each of these types of interrupts occurs. Discuss the significance and applications of each of these types of interrupts.

An Uninitialized Interrupt is generated when an external device is connected and hasn't been configured yet but generates an interrupt. By contrast, a Spurious Interrupt is generated when the CPU sends and interrupt acknowledge after receiving an interrupt acknowledge request but no device responds to it. The 68000 based peripherals are given the uninitialized vector $0F.

5) Discuss the differences between Auto Vectored and User Vectored interrupts. For how many of each type does the MC68000 allow?

Auto Vector Interrupts are used in conjunction with 8-bit peripherals since a vector cannot be provided during an IACK cycle. For a User Vectored Interrupt, it is used with peripherals that can provide these vector numbers. There are 7 Auto Vector Interrupts and 256 User Vector Interrupts.

6) Discuss the events that occur during an Interrupt Acknowledge (IACK) Bus Cycle.

During an IACK cycle, the peripheral first signals on its interrupt line and then the line is encoded. The microprocessor completes the current instruction and saves its state on the stack and then proceeds to check the interrupt mask level against the Status Register. If the level that needs to be serviced is higher than the current level, the interrupt would proceed with the service routine. If the level is less, then it will not do the service routine.