ECE 485/585 – Computer Organization and Design
Fall 2022

Project 1: Designing Multiplexers using Behavioral & Structural Models
Report Due: Friday, October 7th 2022, 11:59PM

IMPORTANT:	***You must sign and date below acknowledgment statement on the title page of your report.*** **Failing to do so, or any violation of this rule will result in an automatic failure for this course.**
Acknowledgment:	I acknowledge all works including figures, codes and writings belong to me and/or persons who are referenced. I understand if any similarity in the code, comments, customized program behavior, report writings and/or figures are found, both the helper (original work) and the requestor (duplicated/modified work) will be called for academic disciplinary action.

I. Introduction

The purpose of this Project 1 is to prepare you towards Project 2 and Project 3, which you will design and implement your own custom 32-bit RISC processor, a stripped-down MIPS processor. The goal of this project is to get familiar with the VHDL programming, as well as the simulation environment. In this project, you will design and implement an **eight-input multiplexer in both behavioral model and structural model using VHDL**.

II. Background

In class, we have discussed two different models that you could implement using VHDL; structural model and behavioral model (Refer to "[Lecture 2] Introduction to VHDL" and "Day 2 Lecture Video" from Blackboard for more detail). Also, you will need to verify your models by creating your own testbench. A testbench is used to verify and confirm your design by observing the output(s) of your circuit, based on your customized input(s). You may need to refer to the "VHDL References" section on the Blackboard and follow the tutorials before beginning this project.

III. Design and Implementation

1. Implement an eight-input multiplexer using behavioral model
2. Implement an eight-input multiplexer using structural model
3. Test both models using your own testbench.

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IV. Project Requirements

1. You are required to design and implement this project **individually**.
2. You are required to provide your original VHDL codes, as well as your testbench codes that you have used to verify your VHDL codes. **All codes should contain your original comments.**
3. You are required to provide simulation results by capturing the screen of the simulation output. Your simulation result must contain the input data used and corresponding output data. You must clearly state in all captured figures which input data used and corresponding output data.
4. You may use one of the following VHDL simulators for the course project:
    a. ModelSim on Endeavour (ECE Server) ~~or local~~
        ~~i. Local installation: https://tinyurl.com/modelsim-student-ed~~
    b. Xilinx Vivado on Endeavour (ECE Server) or local
        i. Local installation (WebPack): https://tinyurl.com/vivado2019
    c. Xilinx ISE (WebPack): https://tinyurl.com/xilinx-ise2018
5. **Your report should include the following sections:**
    a. Title Page with Acknowledgment (shown in Page 1 of this document) and your Signature
    b. Abstract of your report
    c. Introduction *(please remember, introduction and abstract aren't the same)*
    d. Background
        i. Description of a VHDL structural model
        ii. Description of a VHDL behavioral model
        iii. Description of a VHDL testbench
        iv. Description of your VHDL simulator and environment
        v. Anything else that you'd like to address in the background
    e. System Design
        i. Description of your eight-input multiplexer using structural model
        ii. Description of your eight-input multiplexer using behavioral model
        iii. Description of your VHDL testbench code
    f. Simulation Results and discussion
        i. Screenshots of your test cases
        ii. Descriptions of each screenshots
        iii. Discussion of any issues that you faced, any improvement could be made, etc.
    g. Conclusion
    h. List of references

   i. Appendix
      i. Entire Source Code of your project with comments
      ii. Entire Testbench Codes with comments that used to verify your design

6. Due date is **Friday, October 7th 2022 11:59PM**. *No late submission will be accepted*. You'll need to submit the following package in a single ZIP file to the Blackboard.
   a. Your Project Report
   b. Your VHDL Source Codes with your own comments
   c. Your VHDL Testbench Codes with your own comments
7. Refer to the tutorials uploaded on the Blackboard if you are not familiar with VHDL environment.