ECE 485/585 – Computer Organization and Design

Midterm Exam
Friday, October 14th 2022, 2:15PM – 4:45PM

Last Name					
First Name					
CWID					
Section (circle one)	01 (Mies Campus) / 02 (Online) / 03 (India Online)				
Total Score	Q1. /20	Q2. /20	Q3. /15	Q4. /40	Total /95

Exam Guide:

1. **Open books, open notes, and one regular/scientific calculator allowed.**
2. **Only your notes, calculator, pen, or pencil (with eraser) are allowed on your desk.**
3. **All smartphones/tablets/laptops must be turned off, place inside your bag and close it.**
4. You must place your bag at the front of the exam room. You may only pick up your bag when you complete your exam.
5. Please write your name on every page.
6. Do not tear off the exam paper in any circumstances. Any torn-off exam paper will not be graded. The re-stapled exam will not be graded also.
7. **Do not write your answer on the back pages. Back pages can be used as your scratch papers.**
8. Any attempts to look at or copy other people's exam papers will result in failure of this course and asked to leave the exam room immediately.
9. All answers must be readable. Any unreadable or unclear answers may not be graded correctly.

Name:_____

Question 1. (20 Points)

Answer the following questions on MIPS Instruction Set.

a) Show the minimal sequence of MIPS instruction for the following pseudocode segment:

```
A[15] = A[3] + B[2];
```

Assume that array A has a base address of C850 which is required to be loaded to register $t0 in your code and array B's base address value is stored in register $t5. For both arrays, *Assume each index size is 2 bytes*. Provide comments for each line of your MIPS instruction.

```
addi $t0, $zero, 0xC850
lw   $t1, 6($t0)   // A[3]
lw   $t2, 4($t5)   // B[2]
add  $t1, $t1, $t2
sw   $t1, 30($t0)  // A[15] ← Result
```

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b) Assume that Loop starts at memory location 0xDD00. Encode below ***beq and jump*** MIPS instruction into hexadecimal format. Use the reference shown on Pages 6 and 7, or MIPS Reference Data Green Card. *You MUST show your work for full points.*

```
0xDD00  Loop :   add  $s3, $t0, $t1
0xDD04           lw   $s1, 4($s3)
0xDD08           beq  $s0, $s1, Exit
0xDD0C           j    Loop
0xDD10  Exit:    …
```

target addr = $PC_{current} + 4 + (offset \times 4)$

$0xDD10 = 0xDD08 + 4 + (offset \times 4)$

$0xDD0C$

$4 = offset \times 4$

op	rs	rt	offset
000100	10000	10001	0000 0000 0000 0001

$0x12110$

target addr $= PC_{31:28} : (offset \times 4)$

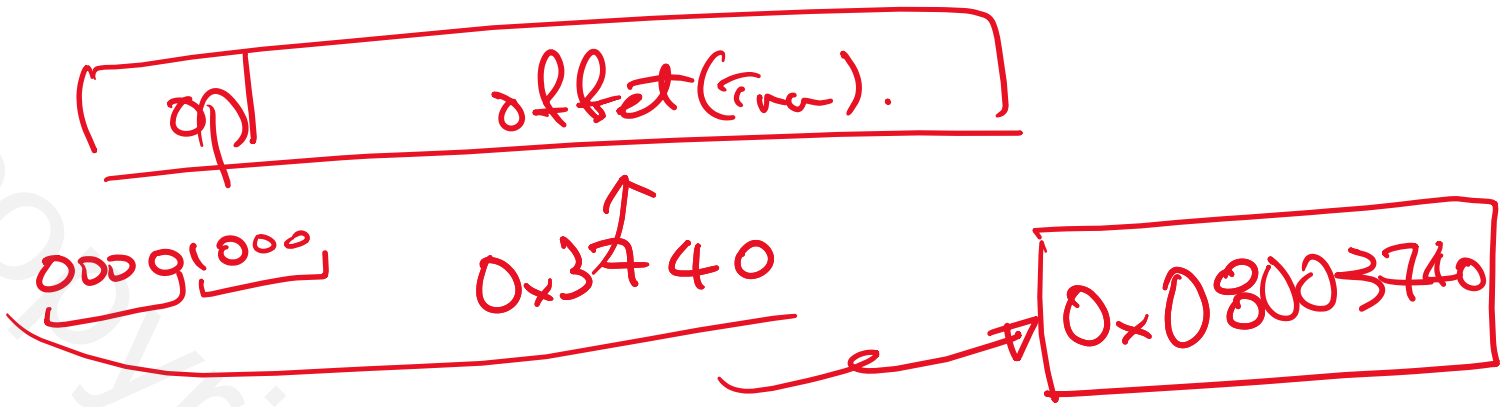
$0xDD00 = offset \ll 2$ $\quad \therefore offset = 0xDD00 \gg 2$

1101 1101 0000 0000

0011 0111 0100 0000

3 7 4 0

Name:_____



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Question 2. (20 Points)

You are trying to decide between two programs for a specific machine, where this machine supports four classes of instructions: A, B, C, and D - Class A takes 6 clock cycles, Class B takes 4 clock cycles, and Class C takes 15 clock cycles, Class D takes 8 clock cycles to execute.

Assume that there are two instruction sequences of the following:

Sequence 1:	250 Class A instructions, 50 Class B instructions
	150 Class C instructions, 100 Class D instructions
Sequence 2:	200 Class A instructions, 150 Class B instructions
	100 Class C instructions, 200 Class D instructions

a) Which instruction sequence executes the most instruction, and by how much?
b) Which instruction sequence is faster? By how much?
c) What is the overall CPI for each instruction sequence?
d) Determine the desired clock rate (in frequency) for each instruction sequence when the expected runtime would be 5µs.

a) S1 : 250 + 50 + 150 + 100 = 550 inst.
S2 : 200 + 150 + 100 + 200 = 650 inst.
+100 inst.

b) $\sum clockcycles_{S1} = (250\times6) + (50\times4) + (150\times15) + (100\times8)$
1500 200 2250 800
$IC \times CC$
$= 4750$ ←

$\sum clockcycles_{S2} = (200\times6) + (150\times4) + (100\times15) + (200\times8)$
1200 600 1500 1600
$= 4900$

$\frac{Perf_{S1}}{Perf_{S2}} = \frac{CPU\ time_{S2}}{CPU\ time_{S1}} = \frac{clockcycles_{S2}\times T_C}{clockcycles_{S1}\times T_C} = \frac{4900}{4750} \doteq 1.03$ ←
S1 faster than S2 by

Name:_____

c) $CPI_{avg\_S1} = \frac{4750}{550} \doteq 8.64$

$CPI_{avg\_S2} = \frac{4900}{650} \doteq 7.54$.

d) $CPU_{time_{S1}} = IC_{S1} \times CPI_{S1} \times T_{C_{S1}}$

$5\mu s = \sum IC_{S1} \times CPI_{S1} \times \frac{1}{f_{C_{S1}}}$

$\therefore f_{S1} = \frac{4750}{5 \times 10^{-6}}$

$= 950 \times 10^6 =$ 950MHz

$\therefore f_{S2} = \frac{4900}{5 \times 10^{-6}} = 980 \times 10^6$

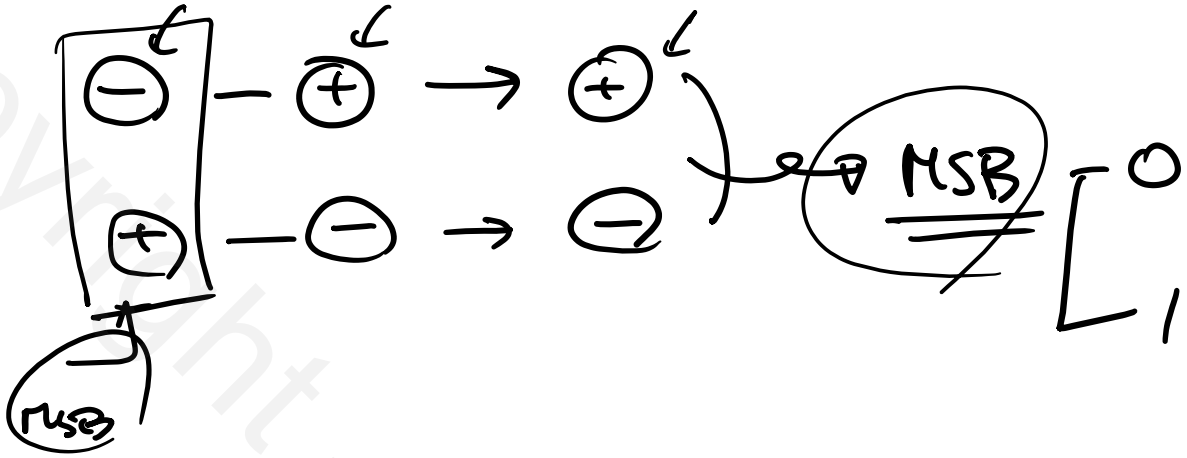
$=$ 980MHz

Name:_____

Question 3. (15 Points)

Answer the following questions in a short sentence:

a) When subtracting two signed numbers, explain how to detect an overflow of the result.



b) Explain why ALU prefers to use **beq** and **bne** instructions over **blt** or **bge**.

H/W limitation

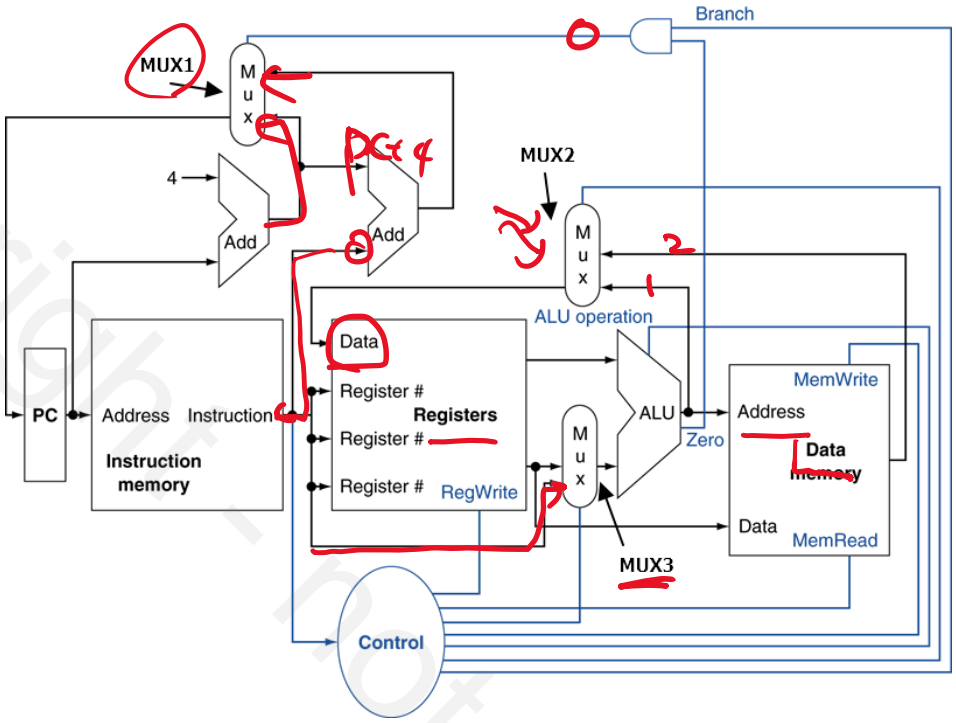
c) Explain how `jump` instruction is implemented in MIPS hardware.

take IR[25:0] → shift << 2 + fill 0s.
append PC[31:28]
→ JUMP addr Reg → MUX [PC+4, JUMP]

Name:_____

Question 4. (40 Points)

Below is the **single-cycle architecture** for MIPS instruction sets.



a) Describe each input and output of MUX1, MUX2, and MUX3 in RTL format.

i. MUX1

In1 : PC+4

In2 : PC+4+ Imm → Sign_ext(Imm16)<<2 or IR[15:0]<<2

Out : PC

ii. MUX2

In1 : R[rs]+R[rt] or R[rs] + Sign_ext(Imm16)

In2 : MEM[Addr] or MEM[R[rs] + Sign_ext(Imm16)]<<2

Out : MEM[R[rt]] or MEM[R[rd]]

lw

iii. MUX3

In1: R[rt] or Sign_ext(Imm16)

In2:

Out : ALU[___]

Name:_____

b) Explain how the Control Unit determines the value for each control signal of this architecture (*provide your answer in one sentence*)

IR[31:26]
opcode

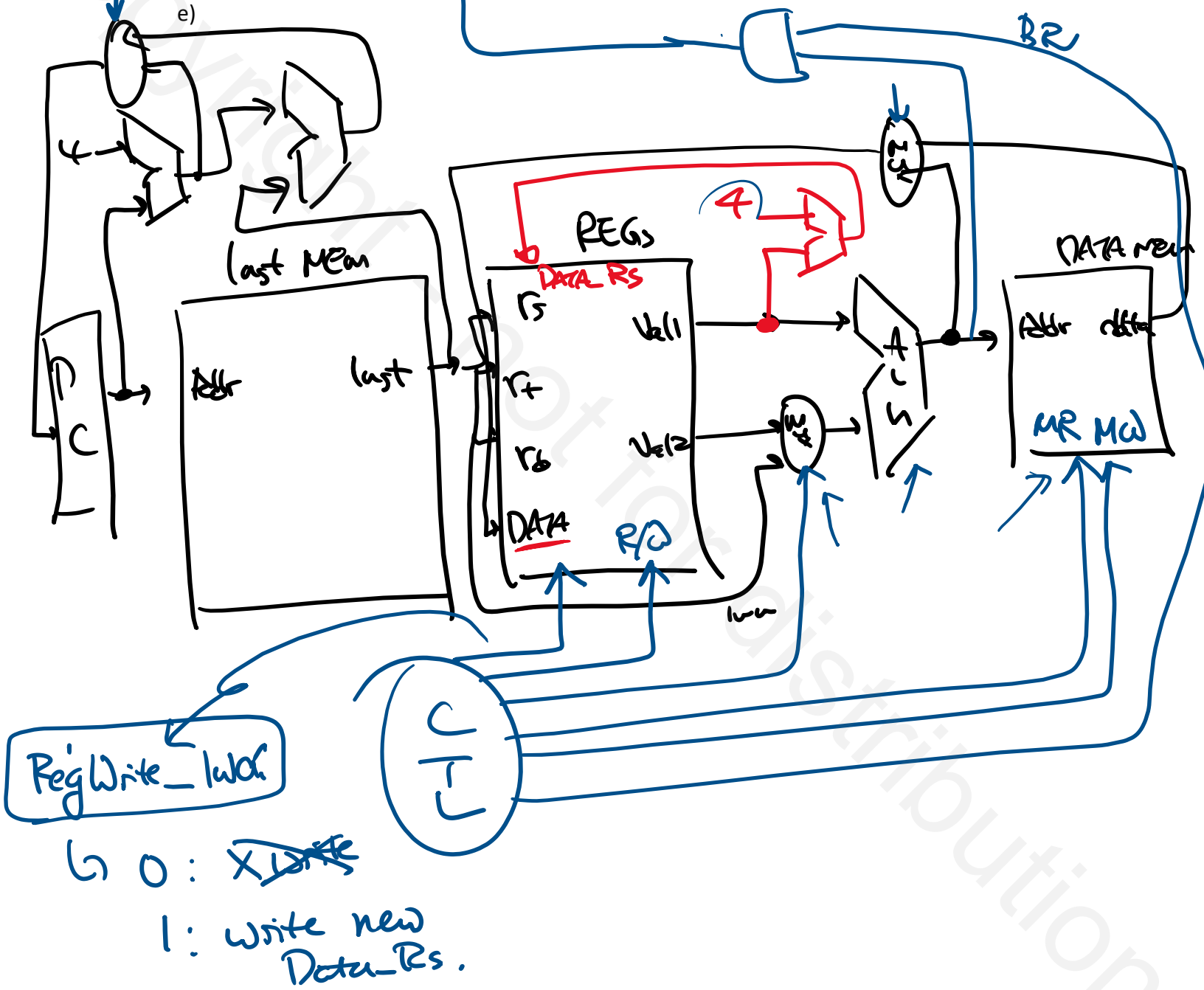
c) Provide each of the control signal values (1 bit) to execute *sw, lw, add, beq* instructions. Use X to indicate any "don't care" signals. (Discard ALU operation signal value)

Instruction	RegWrite	Zero	MemWrite	MemRead	Branch
sw	0	X	1	0	0
lw	1	X	0	1	0
add	1	X	0	0	0
beq	0	0 or 1	0	0	1

Name:_____

d) A new instruction called *lwai* (load word and increment) is introduced to this system. This new instruction will perform the same as *lw* (load word) instruction and additionally perform increment (+4) of the base address value automatically. Draw a new MIPS hardware design by modifying the given hardware (from Page 11) to support this instruction (in additional to other regular MIPS instructions). Add any necessary hardware parts, control signals, and datapath. **Provide your answer below.**

e)



Name:_____

Based on your answer from Question 4d), provide each of the control signal values (1 bit) to execute *lwai* instructions. Use X to indicate any "don't care" signals.
(Discard ALU operation signal value)

	RegWrite	Zero	MemWrite	MemRead	BR	RegWrite lwai
lwai	1	X	0	1	0	1