ECE 485/585 Computer Organization and Design

Syllabus Fall 2022

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Illinois Institute of Technology

Instructor Dr. Won-Jae Yi (wyi3@iit.edu)

Office Hours: TBD or by appointment in advance

Office Location: TBD or Meet online (Zoom link on Blackboard)

Teaching Mr. Tianyang Fang (<u>tfang3@hawk.iit.edu</u>)

Assistant Office Hours: TBD

Office Location: TBD

Class Time Fridays 2:15 PM – 4:55 PM

Class Location Section 01: John T. Rettaliata Engineering Center 104 (Auditorium)

Section 02 & 03: Zoom (recurring link available on Blackboard)

Prerequisites ECE 218 and ECE 242 or Consent of Instructor or Graduate Standing

This course covers basic concepts and state-of-the-art developments in computer

architecture: computer technology, performance measures, instruction set design, computer

arithmetic, controller and datapath design, memory systems, pipelining, array processing,

parallel processing, multiprocessing, abstract analysis models, input-output systems,

relationship between computer design and application requirements, and cost/performance

tradeoffs. Students will complete a project implementing a version of multiple-cycle

processor.

Class Website Illinois Tech Blackboard

Textbook

- Computer Organization and Design MIPS Edition: The Hardware/Software Interface 5th Edition, by David Patterson, John Hennessy; ISBN: 978-0-12-407726-3
- VHDL Simulator for Course Project (Choose one)
 - ECE Endeavour Server (Modelsim & Vivado)
 - Modelsim (Local): https://tinyurl.com/modelsim-student-ed
 - Xilinx Vivado (Local, WebPack): https://tinyurl.com/vivado2019
 - Xilinx ISE (Local, WebPack): https://tinyurl.com/xilinx-ise2018

Reference Books

- Readings in Computer Architecture, Edited by M.D. Hill, N.P. Jouppi, G.S.
 Sohi Morgan Kaufmann Publ., San Francisco, 2000.
- Computer Architecture and Organization, J.P. Hayes, McGraw Hill, 3rd Ed., 1998
- Computer Logic Design, M.M. Mano, Prentice-Hall, 1972
- Computer Hardware/Software Architecture, W. Toy and B. Zee, Prentice-Hall, 1986
- The Design of the UNIX Operating System, M.J. Bach, Prentice-Hall, 1986

Course Objective

- Understanding of current state of computer architecture and technology
- Understanding of computer design trends and upcoming computer architecture direction
- Use of VHDL in design and architecture of a computer system
- Design and tradeoffs of Instruction Sets
- Design of cache systems, main memory and storage systems
- Overall design of a typical computer system

Topics Covered

Computer architecture fundamentals, performance metrics, instruction set architectures, MIPS processors, computer arithmetic, processor data path, pipelining, control logic, data hazards, control hazards, exceptions, parallelism, memory hierarchy, cache design, virtual memory, parallel processors, GPUs, cloud computing, hardware security

Grading		ECE 485	ECE 585
	Homework	10%	10%
	Midterm Exam	30%	30%
	Final Exam	40%	40%
	Project(s)	20%	20%
		(Implementation)	(Implementation & Research Papers)
Homework	All sections need to submit their homework to the Blackboard.		
Policy	Late homework will not be accepted nor graded. Working together on homework is		
	encouraged, but copying assignments will call for disciplinary action. For the project,		
	you may be asked to work in groups.		
Exam Policy	Specific directions will be given before the exam dates. Makeup exams will not be given,		
	except for extraordinary reasons.		
	Final exam will be	comprehensive.	

Academic Honesty

It is your responsibility to be familiar with Illinois Tech Code of Academic Honesty: https://web.iit.edu/student-affairs/handbook/fine-print/code-academic-honesty Working together on the homework assignments are encouraged but copying assignments will call for disciplinary action. All submissions including exercises, programming assignments and exam papers must be your own.

If the above policy and/or any part of the Illinois Tech Code of Academic Honesty is violated in any similarity within the exercise answers, programming assignment codes, comments, customized program behavior, any writings and/or figures are found, both the helper (original source of work submission) and the requestor (duplicated/modified work submission) will be called for academic disciplinary action including zero score of the submission/exam **AND** degrading course letter grade by one.

If the above policy and/or any part of the Illinois Tech Code of Academic Honesty is violated in any similarity within the exam paper submissions, both the helper (original source of work submission) and the requestor (duplicated/modified work submission) will receive a failing grade E for this course, and will be notified to the student's advisor, department and the university.

ADA Statement

Reasonable accommodations according to American Disability Act (ADA) will be made for students with documented disabilities. In order to receive accommodations, students must obtain a letter of accommodation from the Center for Disability Resources and make an appoint to speak with as soon as possible. The Center for Disability Resources (CDR) is located in 3424 S. State St. Suite 1C3-2, (312) 567-5744 or disabilities@iit.edu

This Semester...

- All lectures will be in-person, livestreamed, recorded, and will be available to everyone.
 - No attendance will be taken during this semester.
 - **BUT!** It's your responsibility to follow the lecture, submit your work on time, take the exam on time, etc.