ECE 485/585 Project 2 Evaluation Form

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SECTIONS				SCORE
Abstract + Introduction (10)			10	10
Background & Design Descriptions (35)	Background		5	5
	Full-adder	1-bit RCA	5	5
		4-bit RCA	10	10
		32-bit RCA	10	10
	VHDL simulator & environment		5	5
Simulation Results (20)	Screenshots with descriptions		15	15
	Correctness of the result		5	5
Discussion (15)	Issues Faced, Improvements or others		15	15
Conclusion (10)			10	10
Reference (5)			5	5
Appendix (5)			5	5
TOTAL (100)				100+20=120

Comments: Excellent report, bonus applied for finishing the CLA design