ECE 485/585 Practice Problems 2

Problem 1. A certain computer has a CPU running at 500 MHz. A program running on this machine ends up executing 200 million instructions, of the following mix:

Type	CPI	Freq
A	4	20 %
B	3	30 %
C	1	40 %
D	2	10 %

a) What is the average CPI for this session?

Answer: (20% · 4) + (30% · 3) + (40% · 1) + (10% · 2) = 2.3

b) How much CPU time was used in this session?

Answer: 500 MHz implies 2 ns/cycle. So,

(200 x 106 instructions) · (2 ns/cycle) · (2.3 cycles/instruction) = 0.92 seconds

Problem 2.

a) How does the cache block size affect performance?

Answer. Increasing the block size increases performance up to a point, but performance decreases if the block size is too large.

b) List effect on the miss rate and performance if cache size is increased.

Answer. Increasing the cache size leads to a decrease in capacity misses, but may increase access time.

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Problem 3. Our cache has: 32-byte cache, 4-byte blocks and is 2-way set associative. The policies are: Write Back, LRU replacement.

Assume physical memory is as follows:

Address in hex	Address in decimal	Value
0x4	4	w
0x5	5	x
0x6	6	y
0x7	7	z
…	…	…
0x14	20	a
0x15	21	b
0x16	22	c
0x17	23	d
…	…	…
0x24	36	p
0x25	37	q
0x26	38	r
0x27	39	s
…	…	…

a) For the each of the following instructions, indicate whether it is a hit or miss.

`lb $t0, 21($0)`	**miss**
`lb $t0, 5($0)`	**miss**
`sb $t0, 22($0)`	**hit**
`lb $t0, 4($0)`	**hit**
`lb $t0, 37($0)`	**miss**

b) Fill in the following table to indicate what values are in the cache at the end of this sequence. Include values for data, tag, LRU bit, valid bit and the dirty bit.

Cache set (index)	Valid Bit	Dirty Bit	LRU Bit	Tag	Data
0	0	0			
	0	0			
1	1	0	0	0	wxyz
	1	0	1	2	pqrs
2	0	0			
	0	0			
3	0	0			
	0	0			

c) Finally, indicate any changes to the main memory.

Answer: Memory location 22 holds x.

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Problem 4.

a) Assume that you have a processor with the following specifications:
   i) Five pipeline stages as seen in the lecture notes (IF, ID, EX, MEM, WB)
   ii) Branch comparing done in the third stage
   iii) No forwarding implementation
   iv) Register write and register read cannot happen in the same clock cycle
   v) Multiple read/write possible with the memory in a clock cycle
   vi) Memory stage takes one cycle
   vii) Cannot fetch instruction until branch comparison is done
   viii) No out-of-order execution

Fill in the pipeline execution. (Use IF=Instruction Fetch, ID=Instruction Decode, EX=Execute, MEM=Memory Access, WB=Write Back)

CC / Inst.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
add $3, $3, $5	**IF**	**ID**	**EX**	**MEM**	**WB**												
sub $8, $3, $7		**IF**				**ID**	**EX**	**MEM**	**WB**								
bne $5, $5, exit						**IF**	**ID**	**EX**	**MEM**	**WB**							
lw $10, 4($11)									**IF**	**ID**	**EX**	**MEM**	**WB**				
add $12, $10, $11										**IF**				**ID**	**EX**	**MEM**	**WB**

b) How many clock cycles does it need to execute the above set of instructions?

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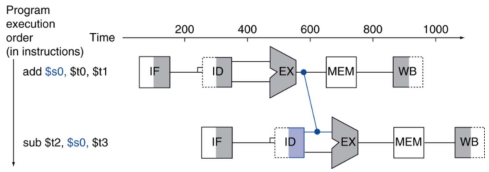
Problem 5. Consider executing the following code on the 5-stage (IF, ID, EX, MEM, WB) pipelined datapath. (Pipeline has forwarding and hazard detection units)

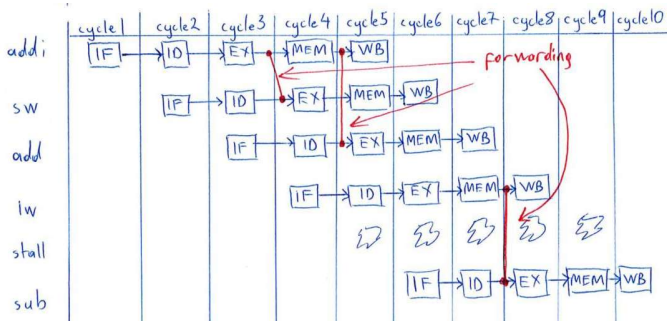
```
addi  $4,$3,8
sw    $3,28($4)
add   $3,$4,$2
lw    $4,44($2)
sub   $2,$4,$9
```

a) How many cycles will it take to execute this code?

10 clock cycles. 1 stall cycle due to lw←→sub data hazard

b) Draw a pipeline diagram (similar to the figure below) that shows the dependencies and how they are to be resolved.





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c) Compute the CPI of the pipeline for the given program. What would be the CPI if there were no forwarding logic?

10 cycles/5 instructions → CPI = 2

If no forwarding, then addi←→sw needs 2 stall cycles

lw ←→sub needs 2 stall cycles instead of 1

Thus, total = 13 cycles

$CPI_{no\_forwarding}$ = 13/5 = 2.6