

ECE586 MIDTERM,

Grade _____

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Examination Rules:

The original exam must be returned for grading.

Exam is open book and open notes. Calculator can be used. Students can use their digital documents on their laptops/tablets.

No smartphone use. No messaging.

Exam period is 75 minutes.

Exam time is on Monday, March 8th, 10:00am – 11:15am Chicago Time.

A Proctor must monitor the students during the entire examination period.

Both the students and Proctor must follow the above requirements and their signatures below will confirm that the above requirements have been fully followed.

Student Signature: _____



Proctor Signature: _____

Date and Time of Examination: _____

Student NAME: ALAN PALAYIL
 Student ID: A20447935

03/08/2023

ECE 586 – Midterm Exam

You may use class notes & textbook. Calculators are allowed. You need to answer all 3 questions.
 Duration: 75 min. Please read the questions carefully. Show all your work, answers must be explained.

Problem 1. (30 points)

Consider a 5-stage pipeline (Fetch, Decode, Execute, Memory, Writeback). Branch condition is checked in the Execute stage. Branch Target Address is calculated in the Decode stage.

- a) Given the following code, determine the pipeline behavior assuming no assists. Clearly state all your key assumptions and fill the table. Flush scheme is used when conditional branch is encountered.

(Branch is not taken)

Assume No data forwarding.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
DONE: LD R3,100(R4)	F	D	E	M	W															
SUBD R8, R3, R6			F	D	-	E	M	W												
AND R10, R6, R3				F	-	D	E	M	W											
SD R10, 0(R8)					-	F	D	-	E	M	W									
BNEZ R8, DONE					-		F	-	D	E	M	W								
DADD R11, R8, R6						-	-	F	D	E	M	W								

Flush mechanism

- b) What are the overall number of cycles in case **Hardware Forwarding** and a static branch predictor (not taken predicted) is used? Show your work. (Branch is not taken)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
DONE: LD R3,100(R4)	F	D	E	M	W	R ₃	F													
SUBD R8, R3, R6		-	F	D	E	M	W													
AND R10, R6, R3				F	D	E	M	W	R ₁₀											
SD R10, 0(R8)					F	D	E	M	W	R ₁₀										
BNEZ R8, DONE						F	D	E	M	W										
DADD R11, R8, R6							F	D	E	M	W	(predicted) (empty pipeline)								

∴ overall no. of cycles for completion = 11 + 4

= 15 //
If hardware forwarding and static branch prediction is used.

Problem 2. (40 points)

Apply Hardware Dynamic Scheduling to the code which computes the dot-product of two vectors.

```
START FLD    F1, 96(R1)
       FLD    F2, 96(R2)
       FADD.D F1, F2, F1
       FDIV.D F2, F2, F1
       FSD    192(R1), F2
       SUBI   R1, R1, 8
       SUBI   R2, R2, 16
       BNEZ   R1, Start
```

Consider a processor that supports hardware speculation for one branch. Assume that one instruction can be issued (single issue processor) to a reservation station each cycle, and that the instruction queue is always ready. Assume the following distribution of functional units (FU, which are not pipelined), execution latencies, and reservation stations (RS):

FU Type	Cycles in EX	Number of FUs	Number of Reservation stations
Integer ALU	1	2	5
FP Add/Sub	3	1	3
FP Divide	6	1	2
Load/Store	2	1	5

The first cycle of load/store execution performs effective address calculation; the second cycle is used to access memory. Assume that memory accesses always hit in cache and that branches are always predicted correctly. The re-order buffer has 56 entries, and only one instruction can be committed each cycle.

- a) (20 points) Determine the instruction schedule for **three iterations** by filling the table given. How many cycles does each loop iteration take?

Iteration	Instruction	Issues at	Executes at	Memory access	Writes CDB at	Commit	Comment
1	FLD F1, 96(R1)	1	2	3	4	5	
(+3)	1 FLD F2, 96(R2)	2	3	4	5	6	
(+6)	1 FADD F1, F2, F1	3	6	-	9	10	DP and Dependency
	1 FDIV F2, F2, F1	4	10	-	16	17	Fadd OP
	1 FSD 192(R1), F2	5	17	-	-	18	Wait for DIV result
	1 SUB1 R1, R1, 8	6	7	-	8	19	No Dependant
	1 SUB1 R2, R2, 16	7	8	-	10	20	CDB Conflict
	1 BNEZ R1, Start	8	9	-	-	21	
→	2 FLD F1, 96(R1)	9	10	11	12	22	
(+3)	2 FLD F2, 96(R2)	10	11	12	13	23	
(+6)	2 FADD F1, F2, F1	11	14	-	17	24	
	2 FDIV F2, F2, F1	12	18	-	24	25	
	2 FSD 192(R1), F2	13	25	-	-	26	
	2 SUB1 R1, R1, 8	14	15	-	16	27	
	2 SUB1 R2, R2, 16	15	16	-	18	28	
	2 BNEZ R1, Start	16	17	-	-	29	
→	3 FLD F1, 96(R1)	17	18	19	20	30	
(-3)	3 FLD F2, 96(R2)	18	19	20	21	31	
(+6)	3 FADD F1, F2, F1	19	22	-	25	32	
	3 FDIV F2, F2, F1	20	25	-	30	33	
	3 FSD 192(R1), F2	21	31	-	-	34	
	3 SUB1 R1, R1, 8	22	23	-	26	35	No dependant / CDB conflict
	3 SUB1 R2, R2, 16	23	24	-	27	36	
	3 BNEZ R1, Start	24	25	-	-	37	

INT ALU - 1
 FP Add/Sub - 3
 FP Div - 6
 Load/Store - 2

b) (20 points) What is the state of the reservation stations, re-order buffer, and register file when the first FDIV.D is ready to commit? Fill the following tables:

Re-order Buffer					
Entry No.	Busy	Instruction	State (Commit/ Write Result/ Execute)	Dest.	Value
1	No	FDP	Commit	F1	96(R1)
2	No	FLD	Commit	F2	96(R2)
3	No	FADD.D	Commit	F1	F2 + F1
4	YES	FDIV	Write Result	F2	F2/F1
5	YES	FSD	Issue	192(R1)	F2
6	YES	SUB	Write Result	R1	R1-8
7	YES	SUB	Write Result	R2	R2-16
8	YES	BNEZ	Write Result	R1	Start
9	YES	FLD	Write Result	F1	96(R1)
10	YES	FLD	Write Result	F2	96(R2)
11	YES	FADD.D	Execute	F1	F2 + F1
12	YES	FDIV	Issue	F2	F2/F1
13	YES	FSD	Write Result	192(R1)	F2
14	YES	SUB	Write Result	R1	R1-8
15	YES	SUB	Execute	R2	R2-16
16	YES	BNEZ	Issue	R1	Start
...					

Reservation Stations								
Name	Busy (Yes/No)	Op	Vj	Vk	Qj	Qk	Dest	Address
Int ALU1	No	SUB	R1	8			#6	
Int ALU2	No	SUB	R2	16			#7	
Int ALU3	Yes	BNE					#8	
Int ALU4	Yes	SUB	#6	8			#14	
Int ALU5	Yes	SUB	#7	16			#15	
FP Add1	No	ADD	#1	#2			#3	
FP Add2	Yes	ADD	#9	#10			#11	
FP Add3								
FP Div1	Yes	DIV	#2	#3			#4	
FP Div2	Yes	DIV	#10				#12	
Load1	No	LOAD	96+R1				#1	
Load2	No	LOAD	96+R2				#2	
Load3	No	FSD	192(R1)	F2			#3	
Load4	No	LOAD	96+#1				#9	
Load5	No	LOAD	96+#2				#10	

Register Status					
	R1	R2	R3	F1	F2
Re-order #	16	15	-	11	12
Busy (yes/no)	Yes	Yes	No	Yes	Yes

end of cycle at 16

Problem 3. (30 points)

A machine uses a **global (2,1) correlating branch predictor**. Consider a code segment that has three branches B1, B2 and B3. At one point in execution, all three branches have been repeatedly taken and all four prediction bits are set to the state **T** (see the state diagram). The initial predictor is (T,T) as circled (i.e. last two branches were taken)

A sequence of branch outcomes that occurs right after this point are given below, listed in the order that the branches are executed.

- a) What is the branch misprediction rate for this sequence? Fill the table (circle the predictor used and determine the predicted outcome) (20 points)

Assume four predictors are named as: Predictor (NT,NT) (if last two branches were Not Taken); Predictor (NT, T) (if last branch was taken and second to last one was Not Taken); Predictor (T,NT) (if previous branch was not taken and second to last one was taken) and Predictor (T,T) (if last two branches were taken).

Branch	Branch Sequence										
	B1	B2	B3	B2	B1	B3	B1	B3	B1	B2	B1
Predictor (NT,NT)	T	T	T	T	(T)	NT	T	T	T	T	T
Predictor (NT,T)	T	T	(T)	NT	NT	NT	NT	NT	NT	NT	(NT)
Predictor (T,NT)	T	(T)	T	(T)	NT	NT	NT	(NT)	T	(T)	T
Predictor (T,T)	(T)	NT	NT	NT	NT	NT	NT	NT	NT	NT	NT
Predicted Outcome	T	T	T	T	NT	NT	NT	NT	T	NT	T
Actual Outcome	NT	T	NT	NT	NT	T	NT	T	NT	T	T
New Prd. (NT,NT)	T	T	T	T	NT	T	T	T	T	T	T
New Prd. (NT,T)	T	T	NT	NT	NT	NT	NT	NT	NT	NT	T
New Prd. (T,NT)	T	T	T	NT	NT	NT	T	T	T	T	T
New Prd (T,T)	NT	NT	NT	NT	NT	NT	NT	NT	NT	NT	NT

$M \rightarrow \text{Miss}$ $M \quad H \quad M \quad \xrightarrow{M} \quad M \quad M \quad H \quad M \quad H \quad H \quad M$

$H \rightarrow \text{Hit}$ $\xrightarrow{\text{misses}} //$

- b) Repeat using a (1,1) correlating branch predictor (all predictors are initialized with "NT"). (10 points)

Branch	B1	B2	B3	B2	B1	B3	B1	B3	B1	B2	B1
Predictor 1 (T)	(NT)	NT	NT	NT	NT	NT	(NT)	NT	NT	NT	NT
Predictor 2 (NT)	NT	(NT)	T	(T)	(NT)	(NT)	T	(T)	T	(T)	T
Predicted Outcome	NT	NT	NT	T	NT	NT	NT	T	NT	T	NT
Actual Outcome	NT	T	NT	NT	(NT)	T	NT	T	NT	T	T
New Prd. 1 (T)	NT	NT	NT	NT	NT	NT	NT	NT	NT	NT	T
New Prd. 2 (NT)	NT	T	T	NT	NT	T	T	T	T	T	T
	H	M	H	M	H	M	H	H	H	H	M

4 misses