CS219 Assignment #6 **Fall 2023**

Purpose: Become familiar with the MIPS architecture instruction formats, Single-Cycle, Multiple-Cycle, Pipelining implementations

Points: 100

Reading/References: Chapter 4, Class Lecture / Lecture Notes

Assignment: Responses must be submitted in writing via the class web site. Must use ".pdf" format.

1) Answer the following Questions [20 pts]

Total Instruction Count = 100				
Program Sequence	**Type**	**Arith**	**Load**	**Store**
Program Sequence 1	**% of Instr.**	10	70	20
Program Sequence 2	**% of Instr.**	40	50	10

a) Which program will be executed first?
b) What is the ET of Program Sequence 1 using single-cycle implementation and multiple cycle implementation?
c) What is the ET of Program Sequence 2 using single-cycle implementation and multiple cycle implementation?

Unit/Stage	**IF**	**ID**	**IE**	**DM**	**WB**
nano seconds (ns)	4	1	3	4	1
Type	**Arith**	**Load**	**Store**	**Branch**	**Jump**
Latency in nanoseconds	9	13	12	8	4

Helpful Notes:
Single Cycle Implementation:

- Longest delay determines clock period.
  - Critical path: load instruction
  - Instruction memory → register file → ALU → data memory → register file
  - For example, if lw=13ns, sw=12ns, R-format=9ns, beq=8ns, j=4ns.
  - In Single cycle, it takes the longest instruct path, which is 13ns in this example.
  - So, ET for lw instruction is 13ns.
  - ET for sw instruction is 13ns.
  - ET for R-format instruction is 13ns.
  - ET for beq instruction is 13ns.
  - ET for j instruction is 13ns.

Multiple Cycle Implementation:

- Longest unit time determines clock period.
- Here unit time is individual time of IF, ID, IE, DM, WB.
- The unit times that takes maximum time among all should be selected as clock period.
- For example, if IF-4ns, ID-1ns, IE-3ns, DM-4ns, WB-1ns. So 4ns is the maximum time in this case, so clock period is 4ns.
- If lw is the instruction, then it requires 5 units, IF+ID+IE+DM+WB, as the clock period is 4ns in multiple cycle implementation, then it is 4ns*5(units for lw)=20ns (This is ET).
- If sw is the instruction, then it requires 4 units, IF+ID+IE+DM, as the clock period is 4ns in multiple cycle implementation, then it is 4ns*4(units for sw)=16ns (This is ET).
- If it is R-format instruction, then it requires 4 units, IF+ID+IE+WB, as the clock period is 4ns in multiple cycle implementation, then it is 4ns*4(units for R-format)=16ns (This is ET).
- If beq is the instruction, then it requires 3 units, IF+ID+IE as the clock period is 4ns in multiple cycle implementation, then it is 4ns*3(units for beq)=12ns (This is ET).
- If j is the instruction, then it requires 1 unit, IF, as the clock period is 4ns in multiple cycle implementation, then it is 4ns*1(units for j)=4ns (This is ET).

Note: For Q1, you must calculate the total ET for all the instructions of program1. For Single Cycle, you can simply multiply the IC with the ET of a single instruction. You must follow the similar methodology for Program Sequence 1 and Program Sequence 2.
For Multiple Cycle, you can calculate the ET for each category of instructions and then sum all the ETs. You must follow the similar methodology for Program Sequence 1 and Program Sequence 2.

2) The 5 stages of the processor have the following latencies: [30 pts, 6 pts each]

Processor	Fetch	Decode	Execute	Memory	Writeback
	350ns	50ns	250ns	800ns	50ns

Assume that when pipelining, each pipeline stage costs 20ns extra for the registers between pipeline stages.

Note: Consider lw instruction for part (a to c)
Throughput=Number of Instructions/ Execution Time
Instruction latency= ET/Number of instructions

a) Non-pipelined processor (Single-Cycle): How many clock cycles does it need? What is the clock cycle time(1 clock cycle time period) ? What is the ET? What is the throughput? What is the instruction latency?

b) Non-pipelined processor (Multi-cycle): How many clock cycles does it need? What is the clock cycle time(1 clock cycle time period) ? What is the ET? What is the throughput? What is the instruction latency? **(Note: You can't calculate the latency by simply knowing the number of instructions. You need the type of instruction as the number of units used varies with type of instruction)**

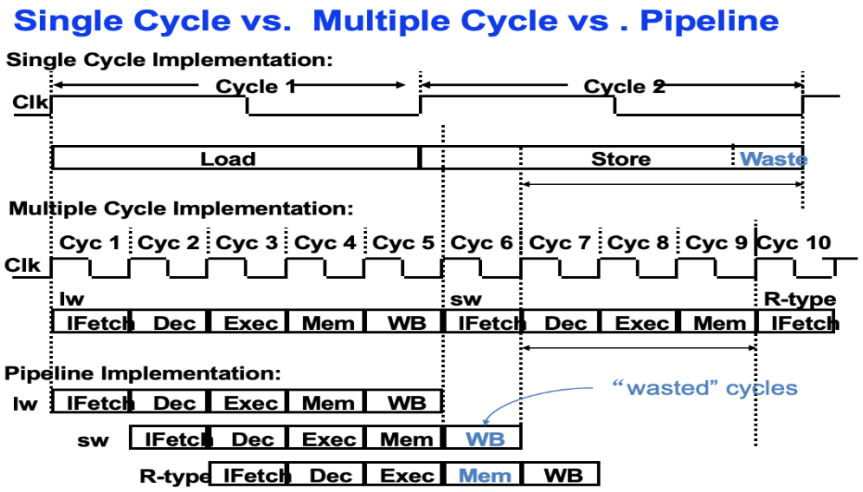
c) Pipelined processor: How many clock cycles does it need? What is the clock cycle time(1 clock cycle time period) ? What is the ET? What is the throughput? What is the instruction latency?

d) If the instruction count=5000, calculate part (a) and part (c); Calculate the speedup between single-cycle non-pipelined processor and Pipelined processor.

e) (pipelined processor only) If you could split one of the pipeline stages into 2 equal halves, which one would you choose? How many clock cycles does it need? What is the clock cycle time(1 clock cycle time period) ? What is the ET? What is the throughput? What is the instruction latency?

3) The 5 stages of the processor have the following number of cycles and instructions:[25 pts]

Unit/Stage	**IF**	**ID**	**IE**	**DM**	**WB**
nano seconds	250	150	300	700	150
Type	**Arith**	**Load**	**Store**	**Branch**	**Jump**
% of Instr.	35	40	15	5	5



Single-cycle: Clock cycle time is based on slowest instruction (Ex: lw)
Multi-cycle: CPU will break Datapath into sub-operations with the cycle time set by the longest sub-operation(logic unit). Now instructions only take the number of clock cycles they need to perform their sub-operations. (Excludes the unit that is not used for any instruction, ex: add- Data Memory is not used)
Pipelining: CPU will break Datapath into sub-operations with the cycle time set by the longest sub-operation. Does not exclude the unit that is not used for any instruction. It may be considered as waste time but the clock cycle time for each instruction is (number of units *clock cycle). However, the performance is attained, due to concurrency/overlapping of instructions. After the execution of 1st instruction, on every clock cycle, the next instruction will be executed.

i) Solve a to c, assuming Instruction Count= 10000

a) Non-pipelined processor (Single-Cycle): How many clock cycles does it take to complete the given instructions? What is the throughput? (8 pts)

b) Non-pipelined processor (Multi-cycle): How many clock cycles does it take to complete the given instructions? What is the throughput? (8 pts)

c) Pipelined processor: How many clock cycles does it take to complete the given instructions? What is the instruction latency? What is the throughput? (8 pts)

d) Compare the speed-up between the above processors (a, b , and c) and write observations (6 pts)

4) List the major types of pipeline hazards and explain each hazard in detail. [10 pts]

5) Explain RAW, WAR, and WAW hazards in detail. Give an example for each hazard. [15 pts, 5 pts each]