A Multichannel EEG Acquisition Scheme Based on Single Ended Amplifiers and Digital DRL

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***Abstract*—Single ended (SE) amplifiers allow implementing biopotential front-ends with a reduced number of parts, being well suited for preamplified electrodes or compact EEG headboxes. On the other hand, given that each channel has independent gain; mismatching between these gains results in poor common-mode rejection ratios (CMRRs) (about 30 dB considering 1% tolerance components). This work proposes a scheme for multichannel EEG acquisition systems based on SE amplifiers and a novel digital driven right leg (DDRL) circuit, which overcome the poor CMRR of the front-end stage providing a high common mode reduction at power line frequency (up to 80 dB). A functional prototype was built and tested showing the feasibility of the proposed technique. It provided EEG records with negligible power line interference, even in very aggressive EMI environments.**

***Index Terms*—Biopotential amplifier, biopotential front-end, common-mode rejection ratio (CMRR), driven right leg (DRL) circuit, multichannel EEG, power line interference.**

I. Introduction

EEG multichannel acquisition systems are widely used in medical practice and research, where up to 128 channels or even more are used [1], [2]. These multichannel EEG equipments usually acquire the signals using the monopolar topology, where every channel amplifies the voltage between each electrode and a reference electrode common to all them. This scheme allows the computation of any bipolar derivation between pairs of electrodes by subtracting the corresponding monopolar channels.

Despite state-of-art integrated solutions [3], [4] for specific applications, EEG instrumentation is still spread between active/pasive electrodes, headbox and a mainboard [5], [6]. The use of active electrodes is mainly addressed as an alternative to shielded cables, in order to avoid power line interference effects due to displacement currents coupled to the patient leads [7]. They also allow using dry electrodes, avoiding issues related to conductive gel or pastes [4].

Power line also interferes imposing a common mode (CM) voltage $V_{\rm CM}$ between the patient and the amplifier common (GND), as it is depicted in Fig. 1. In general, this voltage is of the order of tens of mV, but it can be up to 200 mV peak-to-peak [8], [9].

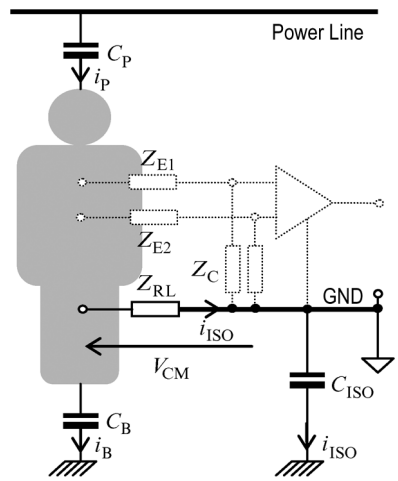

Fig. 1. Simple interference model. It illustrates how power line works as common mode generator.

Common mode interference $V_{\rm CM}$ affects the biopotential measurement by "mode transformation" to differential mode (DM) voltages. This occurs before the signal reaches the amplifier due to imbalances between the electrode's impedances $Z_{\rm E1}, Z_{\rm E2}$ ("potential divider effect") and also inside the amplifier itself, because of its limited common-mode rejection ratio $CMRR_{\rm A}$. The effect of electrode's impedances can be described by an equivalent $CMRR_{\rm PD}$ given by [8]

$$CMRR_{\rm PD} = \frac{Z_C}{\Delta Z_{\rm E}} \tag{1}$$

being $\Delta {\rm Z_E} = {\rm Z_{E1}} - {\rm Z_{E2}}$ the electrode impedance imbalance and $Z_{\rm C}$ the amplifier CM input impedance at power line frequency $f_{\rm PL}$ (50/60 Hz). Typical $CMRR_{\rm PD}$ values are between 80–90 dB for unshielded leads or active electrodes, and around 60 dB when shielded leads are used. The resulting input-referenced DM voltage is given by [10]

$$V_{\rm DM} = V_{\rm CM}\left(\frac{1}{CMRR_{\rm PD}} + \frac{1}{CMRR_A}\right). \tag{2}$$

The second factor in (2) can be regarded as an overall $CMRR_{\rm T}$: $(CMRR_{\rm T}^{-1} = CMRR_{\rm PD}^{-1} + CMRR_{\rm A}^{-1})$.

When differential front-ends are used, $CMRR_{\rm A}$ larger than 90 dB can be easily achieved [11] and interference in (2) is dominated by $CMRR_{\rm PD}$. The same does not occur when using

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TABLE I
COMPARATION OF CMRR BETWEEN EEG SYSTEMS

System	Single Ended (TLC2274)		Yazicioglu [3]		ADS1298 [25]	
Z_{IN}	10TΩ//8pf		1GΩ//8pf[c]		1GΩ//20pf	
$CMRR_A$	>**30dB**		>120dB		115dB	
	case I[a]	case II[a]	case I	case II	case I	case II
$CMRR_{PD}$[b]	92dB	66dB	**92dB**	**66dB**	**84dB**	**65dB**
$CMRR_T$	**30dB**	**30dB**	**92dB**	**66dB**	**84dB**	**65dB**
DRL's Gain to achieve CMRR=100dB	70dB	70dB	8dB	34dB	16dB	35dB

[a] case I: unshielded leads, driven shields or active electrodes.
case II: shielded leads; $C_{shield} = 150$ pF.
[b] $\Delta Z_E = 10$ kΩ.
[c] Input capacitance is not specified, 8 pf were taken as a typical value.

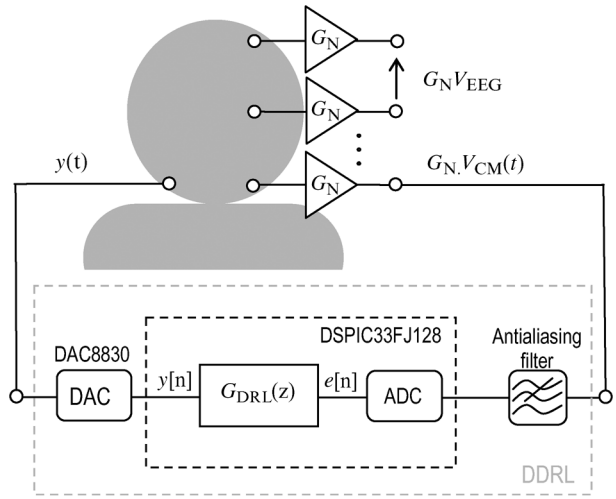

Fig. 2. Simplified diagram of the proposed scheme. It is based on SE amplifiers and a high gain digital DRL.

independent single ended (SE) amplifiers, as in active preamplified electrodes [12], [13], because differences between individual channel's gains yield to poor $CMRR_A$ values, as low as 30 dB. For two SE channels with unmatched gains G_1 and G_2, the $CMRR_A$ is given by [13], [14]

$$CMRR_A = \frac{\overline{G}}{\Delta G}; \quad \Delta G = G_1 - G_2; \quad \overline{G} = \frac{|G_1 + G_2|}{2}. \tag{3}$$

In summary, for differential front-ends (2) becomes

$$V_{DM}|_{DA} \approx V_{CM} \frac{1}{CMRR_{PD}} \tag{4}$$

with $CMRR_{PD}$ of around 80–90 dB, and for SE amplifiers it reduces to

$$V_{DM}|_{SE} \approx V_{CM} \frac{1}{CMRR_A} \tag{5}$$

with $CMRR_A$ as low as 30 dB.

As it was previously stated, V_{CM} can be up to 200 mV peak-to-peak [8]. So, a $CMRR_T$ of 100 dB is enough to reduce CM interference effects below the amplifier noise level, which is typically higher than 2–3 μV_{P-P}. Either for differential and SE front-ends, an additional common mode rejection is needed to achieve the required $CMRR_T$ as it is summarized in Table I. Some approaches work on correcting the imbalances in electrode impedances [15] to increase $CMRR_{PD}$, or in amplifier's gains matching [16] to improve $CMRR_A$. Nevertheless, these methods require many components and independent signal processing for each individual channel, becoming difficult to implement as the number of channels increases. Another ways to improve the power line interference rejection is by gain calibration or including notch filters at 50/60 Hz. These methods also need to be applied channel by channel and can lead to other problems as signal distortion or a poor rejection of non stationary interference [17], [18].

An effective technique to deal with CM interference is reducing directly V_{CM} (the source of interference), as the well known driven right leg (DRL) circuit does. This circuit, also called body potential driver (BPD) [19], [12], performs a negative feedback of the patient's CM voltage through the ground electrode. This closed-loop technique, widely used in biopotential acquisition systems, allows reducing V_{CM} by the open-loop gain factor G_{DRL} at the power line frequency f_{PL} (50/60 Hz) [8], [20]. Equation (2) becomes

$$V_{DM} \cong \frac{V_{CM}}{G_{DRL}} \left(\frac{1}{CMRR_{PD}} + \frac{1}{CMRR_A} \right) \tag{6}$$

and, expressed in dB units, the equivalent $CMRR_T$ increases in G_{DRL}.

In conclusion, to achieve an overall $CMRR_T$ of 100 dB, there is a trade-off between CM voltage rejection and CM voltage reduction. Usually, differential front-ends meet with high CM rejection, needing moderate or low CM reduction by the DRL circuit. In contrast, the proposed SE front-end, with low CM rejection, demands high G_{DRL} to reduce CM voltage. This is not a disadvantage, because with a single high gain DRL circuit it is possible to reduce the CM voltage for all SE channels.

Table I resumes the different factors that affects the $CMRR_T$ for three different EEG acquisition systems, two state-of-art differential SOICs [3], [21] and the proposed single ended solution. Two cases were analyzed: the most favorable for $CMRR_{PD}$, using active electrodes, unshielded leads or driven shields; and the least favorable, using shielded leads.

The table shows that even in the most favorable case, differential systems need some amount of CM feedback (DRL's gain) to completely neglect the CM interference.

II. PROPOSED SYSTEM

The proposed scheme is depicted in Fig. 2. It consists in an array of single ended amplifiers, similar to that presented in [19] with an improved DRL that provides more than 70 dB of CM reduction.

Although the scheme is explained using discrete components, the aim is to present the general structure and expose its feasibility without suggesting a particular implementation. Generally speaking the scheme can be realised as a single integrated IC.

A. The SE Amplifiers

The objective of the SE amplifiers array is to simplify the EEG front-end leading to a very simple circuit. It reduces to one SE amplifier per channel, being well suited for multichannel monopolar systems [12], preamplified electrodes [13], [16] or miniature wireless headboxes.

Each SE channel could be implemented with one operational amplifier (OA) and two resistors. A nominal gain $G_{\rm N}$ of 10 times is high enough to ensure that voltage noise is exclusively due to the front-end. So, subsequent stages do not contribute significantly to the overall noise. With this gain, SE amplifiers can work properly with DC electrode potentials up to ± 200 mV when powered by a 5 V single supply. With such gain, it is also possible the direct connection to high resolutions $\Sigma - \Delta$ ADCs which lead to input referenced noise voltages lower than 1 $\mu {\rm V}_{\rm RMS}$ for ${\rm BW} = 100$ Hz [22], [23]. Hence, additionally amplification stages are not needed [23] and the removal of DC component can be performed by software.

B. The Digital Driven Right Leg Circuit

The maximum allowable $G_{\rm DRL}$ value is limited by stability issues. A typical DRL circuit design provides a open loop gain of 30–50 dB at $f_{\rm PL}$ [8], [13], [20], [24], which is enough for differential front-ends, but not for SE front-ends, which require a $G_{\rm DRL}$ larger than 70 dB to fulfill the desired $CMRR_{\rm T}$ of 100 dB. Because of that, the proposed scheme includes the improved DRL presented in [25], which provides an ultra high gain $G_{\rm DRL}$ at $f_{\rm PL}$ but without jeopardizing circuit stability. This circuit [25], is an improvement of the classic DRL circuit, often implemented by an integrator with a $G_{\rm DRL}$ limited to 30–50 dB [8]. In order to achieve a higher gain at power line frequency, a high Q resonator at $f_{\rm PL}$ is introduced in parallel with the classical integrator, thus resulting the following $G_{\rm DRL}$ transfer function

$$G_{\rm DRL}(s) = \frac{1}{\tau_i {\rm s}} + K \frac{(2\pi f_{\rm PL})^2}{{\rm s}^2 + (2\pi f_{\rm PL}/Q){\rm s} + (2\pi f_{\rm PL})^2}. \quad (7)$$

The resonator transfer function $R({\rm s})$ (right term of (7)) will have to provide a high gain at power line frequency, while its contribution close to the cutoff frequency $f_{\rm C}$ must be negligible when compared to the integrator gain at this point (0 dB). In this way, $G_{\rm DRL}$ will present a high gain at $f_{\rm PL}$ whereas it behaves as the classic integrator for high frequencies (see Fig. 3). This is the key issue to keep the same phase margin (45 degrees) of the classical approach. In summary, the design conditions for $R({\rm s})$ are a huge gain at $f_{\rm PL}$ and a reduced gain (lower than unity) at $f_{\rm C}$

$$R({\rm j}2\pi f_{\rm PL}) = KQ > 70 \text{ dB};\ R({\rm j}2\pi f_{\rm C}) \approx K(f_{\rm PL}/f_{\rm C})^2 \ll 1. \quad (8)$$

Power line common mode voltage will be reduced by the open loop gain at $f_{\rm PL}$, i.e., by KQ. Then, selecting a high enough Q factor and an appropriate gain K, it is possible to choose the peak gain and the bandwidth ${\rm BW} = 2\pi f_{\rm PL}/Q$.

The implementation of that scheme requires a high Q circuit with a very precise central frequency f_0. This is difficult to achieve by analog circuits having in mind aging, tolerance and temperature sensibility of the electronics devices. Therefore, a fully digital implementation of the DRL, as in [25], was adopted (DDRL: Digital DRL). It was implemented in a 16-bit fixed point DSC, with a Q factor of 130 $({\rm BW} = 0.4$ Hz) and $K = 127$, fulfilling the conditions in (8) and providing a $G_{\rm DRL}$ gain of 84 dB at 50 Hz.

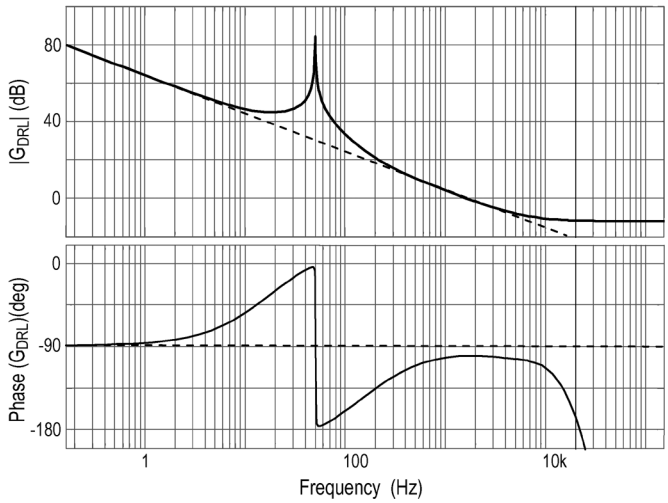

Fig. 3. Common mode amplifier transfer function for the classic approach (dashed line) and for the proposed scheme (solid line).

Fig. 3 shows the DDRL's frequency response including the antialiasing filter (at 7 kHz), and DAC (zero order hold) effects for a sampling rate of 40 kHz.

As Fig. 2 shows, the common mode voltage $V_{\rm CM}$ is taken from one of the SE channels, which is a usual practice in multichannel acquisition [19], [12]. This voltage is sampled using a 12 bit ADC embedded in the DSC. The voltage gain of 11 V/V allows a good use of ADC's dynamic range and in this way, all active channels are equal and anyone can acts for CM sense or biopotential measurement.

III. Experimental Tests

A functional prototype of the proposed EEG acquisition scheme was built to test its feasibility. The frequency response of the DDRL was experimentally verified and some EEG records were made to evaluate the proposed scheme working in a real EEG acquisition setup, where the measurement conditions were chosen to recreate an adverse EMI coupling scenario.

A. DDRL's Frequency Response

The frequency response of the DDRL was experimentally measured using a frequency variable sinusoidal generator working as CM voltage input $V_{\rm CM}$. Fig. 4 shows the experimental data, which shows a good agreement with the theoretical curve. It can be observed that the $G_{\rm DRL}$ gain (including $G_{\rm N}$) is about 74 dB at 50 Hz. This is a bit lower than the expected 84 dB due to resonator implementation in 16 bits fixed point precision; but higher enough to fulfill with the required 70 dB.

B. Real EEG Acquisition

The experimental setup used to acquire EEG signals is shown in Fig. 5. It permits to select the proposed DDRL or the classic

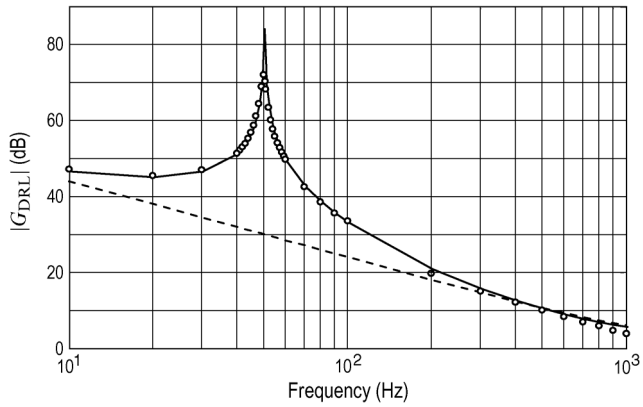

Fig. 4. Open loop DDRL frequency response including G_N. The designed frequency response is indicated in solid line and the experimental data with markers. The dashed line curve represents classical DRL frequency response.

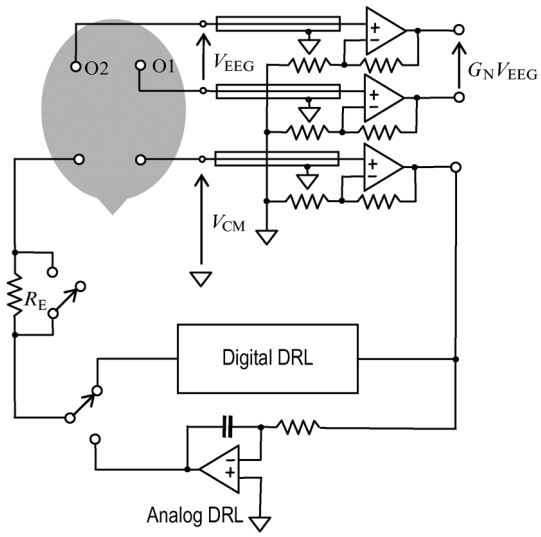

Fig. 5. Experimental setup for testing the proposed scheme in real EEG acquisition and to compare the DDRL against a typical analog DRL.

DRL circuit. Both DRL circuits were designed for the worst measurement condition, which means $f_C = 1.5$ kHz [20] and gains of 30 dB and 84 dB at power line frequency for the classic and digital DRL, respectively. If better conditions are assumed, i.e., $f_C = 15$ kHz, both DRL's gains can be increased in 20 dB. The setup also allows inserting a resistor $R_E = 100$ kΩ in series with the feedback electrode to recreate poor measurement conditions [26].

Real EEG signals were obtained from two SE channels and the difference between them was acquired by a biopotential acquisition system [27]. The gains of the used channels were: 10.873 V/V and 10.804 V/V respectively; which implies a $CMRR_A$ of about 44 dB.

In order to test the CM rejection of the proposed scheme, a condition of high CM interference was generated asking the subject to sit on a chair with his/her feet elevated from the floor and placing a power cord near him/her. In these conditions and without any DRL circuit, V_{CM} was about 70 $\mathrm{mV_{P-P}}$.

EEG signals were acquired from electrodes placed in locations O1-O2 of the standard 10–20 system [9]. During the test, the subject was asked to close and open his/her eyes, in order to observe the visual alpha rhythm. Several records were acquired alternatively with the DDRL and with the analog DRL. Two of these records, which are not simultaneous but correspond to the same session, are presented in Fig. 6. As can be seen in this figure, no power line interference can be observed when the DDRL is used, whereas it is evident for the classic DRL.

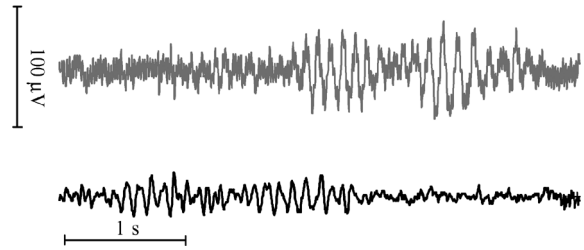

Fig. 6. EEG signals recorded using the classic DRL (gray curve) and with the DDRL (black curve).

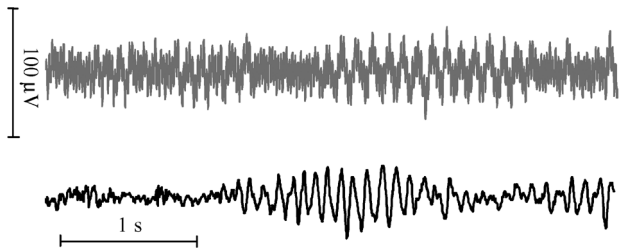

Fig. 7. EEG signals registered using the classic DRL (gray curve) and with the DDRL (black curve). A 100 kΩ resistor was placed in series with the feedback electrode to deteriorate interference rejection.

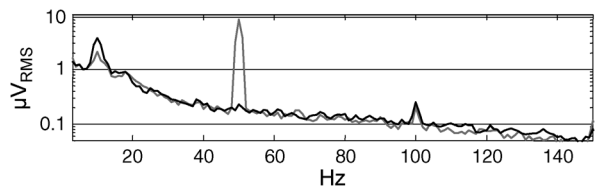

Fig. 8. Spectrum of EEG signals registered using the classic DRL (gray curve) and the DDRL (black curve). A 100 kΩ resistor was placed in series with the feedback electrode to deteriorate the interference rejection.

A second test was performed including an additional resistor $R_E = 100$ kΩ in series with the feedback electrode. Even in this poor measurement condition, power line interference is negligible when the DDRL is used but increases significantly for the classic DRL (Figs. 7 and 8).

IV. Conclusions

It is possible to use Single Ended amplifiers for EEG acquisition when combined with an ultra high gain DDRL circuit, thus leading to very simple front-ends. This is possible, even with the poor CM rejection of SE amplifiers, because the DDRL provides enough reduction of CM interfering voltage. The DDRL presents a gain of 74 dB at 50 Hz and no power line interference was observed in real EEG measurements; even in a very aggressive EMI environment. In the same conditions, the classic analog DRL led to non acceptable EMI levels (more than 25 $\mu\mathrm{V_{P-P}}$), requiring differential front-ends.

The advantages of the proposed scheme are more noticeable as the number of channels increases. The schemes based on differential front-ends require more complex amplifiers (balanced circuit design, more active components, etc.) and it is necessary to route the same reference signal to each channel. This calls for low noise buffers suitable to drive capacitive loads and a carefully designed PCB layout for the reference signal. A SE array instead, can refer each channel to the common (ground) or any other DC voltage. The only drawback is a more complex DRL, which vanishes as the number of SE channels increases.

The proposed front-end demands a reduced number of components and the involved DDRL digital processing requires a reduced number of resources, being well suited to be integrated in a monolithic circuit. The DDRL does not impose a high computational load and the DSP can also be used to perform other tasks such as acquisition, filtering and decimation.

Another advantages of having digital control of CM voltages is the possibility to measure electrode impedances [28], and the implementation of new methods for interference rejection, as those for capacitive electrodes, which needs a different G_{DRL} transfer function.

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