APPLICATION NOTE

Atmel AT02595: RF Design Schematic Checklist

Atmel MCU Wireless

Features

- Quick guide for schematic implementation
- Supported Atmel® Wireless chipset,
  - AT86RF212B
  - AT86RF231
  - AT86RF232
  - AT86RF233
  - ATmega128RFA1
  - ATmega64/128/256RFR2
  - ATmega644/1284/2564RFR2
- Reference design for interfacing,
  - Crystal
  - Balun/Filter
  - External Front End Module
  - Antenna
  - MAC ID chip
  - EEPROM
  - Serial Dataflash
  - Programming header
- Procedure for terminating and mapping pinouts
- Hardware consideration for controlling FEM and antenna diversity

Description

Scope of the application note is to guide customers in designing wireless products using Atmel Wireless chipsets, but limited to schematic design.

Targeted audience includes embedded product designers and hardware engineers.Document provides the checklist for various components along with design consideration guidelines.

Term SoC denotes either ATmega64/128/256RFR2 or ATmega644/1284/2564RFR2 chipsets throughout this document.

Table of Contents

1. Introduction

This application note shall guide schematic designers to understand the ecosystem of components required around Atmel Wireless chipsets. Checklist of components provided in the document consolidates the various design options possible with Atmel Wireless chipsets.

Atmel Wireless Evaluation kits [23] can be referred for evaluating RF performance of Atmel chipsets and most of the schematic design considerations covered in this application note is an excerpt from these evaluation boards.

1. Atmel AVR®2044: RCB128RFA1 - Hardware User Manual (www.atmel.com/images/doc8339.pdf)
2. Atmel AVR10004: RCB256RFR2 – Hardware User Manual (www.atmel.in/Images/Atmel-42081-RCB256RFR2-Hardware-User-Manual_Application-Note_AVR10004.pdf)
3. Atmel AVR2043: REB231ED - Hardware User manual (www.atmel.com/Images/doc8345.pdf)
4. Atmel AVR2092: REB232ED - Hardware User Manual (www.atmel.com/Images/doc8427.pdf)
5. Atmel AVR2162: REB233SMAD – Hardware User Manual (www.atmel.in/Images/doc42006.pdf)
6. Atmel AVR2080: REB231FE2 – Hardware User's Manual (www.atmel.in/Images/doc8479.pdf)

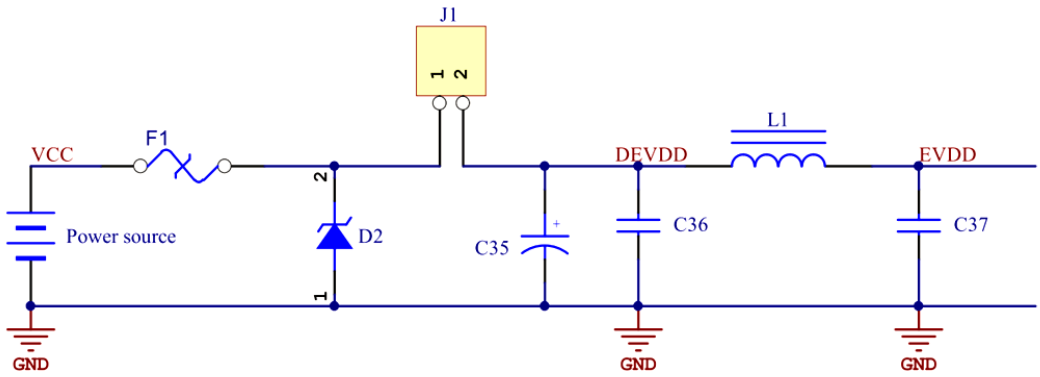
Schematic symbols and footprints for Atmel Wireless chipsets are available as Altium supported library in Atmel AVR2010: MCU Wireless - Altium Design Package [24].

2. Power and Ground

2.1 Power supply

Atmel wireless chipsets support supply voltage from 1.8V to 3.6V. Custom board can be powered either by an external power supply or battery. Figure 2-1 shows the basic power supply circuit containing current measurement jumper. Ammeter can be connected by removing the current measurement jumper (or 0 ohm resistor) for measuring current consumption of the module. Inductor (L1) acts as filter between analog (EVDD) and digital (DEVDD) power supply domains. Both analog and digital power supply domains are described in section 2.2 and 2.3 respectively.

Figure 2-1. Power supply



- **Power source: 1.8 to 3.6V**
- **F1 (optional)**
- **D2 (optional)**
- **L1: Ferrite bead (optional)**
- **J1: Current measurement jumper (optional)**
- **C35: 47µF (Electrolytic capacitor)**
- **C36: 100nF (Ceramic capacitor)**
- **C37:100nF (Ceramic capacitor)**

2.2 Analog supply pins (EVDD and AVDD)

Analog power domain has two types of supply pins namely EVDD and AVDD where,

- EVDD – Analog supply voltage pins of transceiver
- AVDD – Internal 1.8V Analog voltage regulator output.

Analog supply pin, EVDD should be connected to a decoupling capacitor (C2). Analog regulator pin, AVDD should be connected to a bypass capacitor (C1) to ensure stable operation, refer Figure 2-2. Every EVDD and AVDD pin on the chipset should have a decoupling and bypass capacitor respectively.

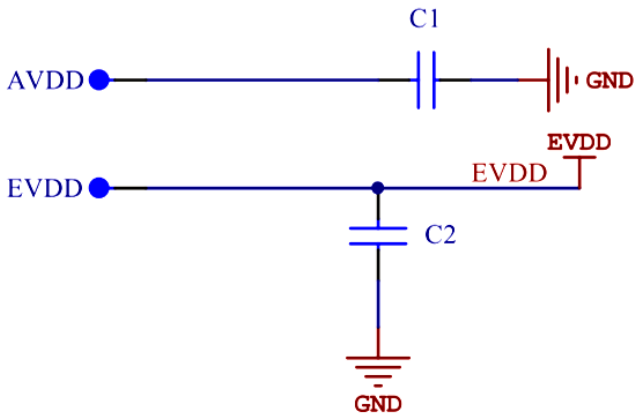
Caution: All decoupling and bypass capacitors should be placed as close as possible to the pins and it should have a low resistance and low inductance connection to ground for better performance.

Analog supply pinouts available on Atmel wireless chipsets are given in Table 2-1. Analog block settling times are tablulated in Table 2-2. For more details refer to corresponding device datasheet [1].

Table 2-1. Analog supply pinouts

S.No	Chipsets	EVDD	AVDD
1	AT86RF212B	Pin 28	Pin 29
2	AT86RF231	Pin 28	Pin 29
3	AT86RF232	Pin 28	Pin 29
4	AT86RF233	Pin 28	Pin 29
5	ATmega128RFA1	Pin 59	Pin 60
6	ATmega64/128/256RFR2	Pin 59	Pin 60
7	ATmega644/1284/2564RFR2	Pin 44	Pin 45

Figure 2-2. Connecting analog supply pins



- **C1: Ceramic capacitor, X5R, 16V (Refer Table 2-2 for typical value)**
- **C2: Ceramic capacitor, X5R, 16V (Refer Table 2-2 for typical value)**

Caution: Worst case C1 and C2 values can reach upto 10uF.

Table 2-2. Analog block settling time

S.No	Chipsets	C1 (µF)	C2 (µF)	AVREG, t_{TR18} or t_{AVREG} (µS)		TRX_OFF to PLL_ON, t_{TR4} (µS)	TRX_OFF to RX_ON, t_{TR6} (µS)
				Typical	Maximum	Typical	Typical
1	AT86RF212B	1	1	150	1500	170*	170*
2	AT86RF231	1	1	60	1000	110	110
3	AT86RF232	0.1	1	50	1000	80	80
4	AT86RF233	0.1	1	50	1000	80	80
5	ATmega128RFA1	1	1	60	1000	110	110
6	ATmega64/128/256RFR2	1	1	60	1000	110	110
7	ATmega644/1284/2564RFR2	1	1	60	1000	110	110

*TRX_OFF_AVDD_EN (register 0x0C, TRX_CTRL_2) is not set.

2.3 Analog ground pins (AVSS)

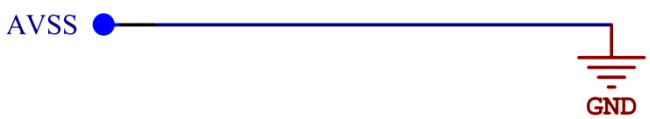
Analog ground pins are designated as AVSS and they provide ground reference for analog domain. Reference schematics for connecting analog ground pins are shown in Figure 2-3.

Analog ground pinouts available on Atmel wireless chipsets are given in Table 2-3.

Table 2-3. Analog ground pinouts

S.No	Chipsets	AVSS
1	AT86RF212B	Pin 3, 6, 27, 30, 31, 32 and Paddle
2	AT86RF231	Pin 3, 6, 27, 30, 31, 32 and Paddle
3	AT86RF232	Pin 1, 2, 3, 6, 27, 30, 31, 32 and paddle
4	AT86RF233	Pin 3, 6, 27, 30, 31, 32 and Paddle
5	ATmega128RFA1	Pin 7, 10, 58, 61 and Paddle
6	ATmega64/128/256RFR2	Pin 7, 10, 58, 61 and Paddle
7	ATmega644/1284/2564RFR2	Pin 5, 8, 43 and Paddle

Figure 2-3. Connecting analog ground pins



Caution: In this example we connected both Digital ground (DVSS) and Analog ground (AVSS) to the same ground plane, for providing solid continuous ground plane. Designer should find a better solution to isolate the digital noise from RF/Analog domain, if the board is affected by such interferences

2.4 Digital supply pins (DEVDD and DVDD)

Digital power domain has two types of supply pins namely DEVDD and DVDD where,

- DEVDD – Digital supply voltage pins of transceiver
- DVDD – Internal 1.8V digital voltage regulator output.

Digital supply pin, DEVDD should be connected to a decoupling capacitor (C4). Digital regulator pin, DVDD should be connected to a bypass capacitor (C3) to ensure stable operation, refer Figure 2-4. Every DEVDD and DVDD pin on the chipset should have a decoupling and bypass capacitor respectively.

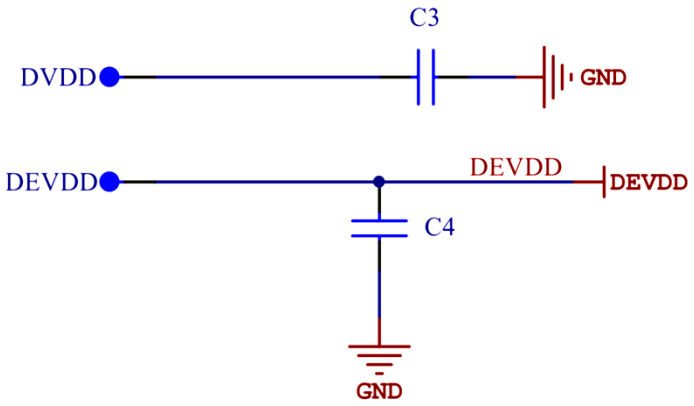
Caution: All decoupling and bypass capacitors should be placed as close as possible to the pins and it should have a low resistance and low inductance connection to ground for better performance.

Analog supply pinouts available on Atmel wireless chipsets are given in Table 2-4. Digital block settling times are tablulated in Table 2-5. For more details refer to corresponding device datasheet [1].

Table 2-4. Digital supply pinouts

S.No	Chipsets	DEVDD	DVDD
1	AT86RF212B	Pin 15	Pin 13 and 14
2	AT86RF231	Pin 15	Pin 13 and 14
3	AT86RF232	Pin 15	Pin 13 and 14
4	AT86RF233	Pin 15	Pin 13 and 14
5	ATmega128RFA1	Pin 23, 24, 44 and 54	Pin 21 and 22
6	ATmega64/128/256RFR2	Pin 23, 24, 44 and 54	Pin 21 and 22
7	ATmega644/1284/2564RFR2	Pin 16	Pin 15

Figure 2-4. Connecting digital supply pins



- **C3: Ceramic capacitor, X5R, 16V (Refer Table 2-5 for typical value)**
- **C4: Ceramic capacitor, X5R, 16V (Refer Table 2-5 for typical value)**

Note: Worst case C3 and C4 values can reach upto 10uF.

Table 2-5. Digital block settling time

S.No	Chipsets	C3 (µF)	C4 (µF)	DVREG, t_{TR17} or t_{DVREG} (µS)		P_ON to CLKM available, t_{TR1} (µS)		SLEEP to TRX_OFF, t_{TR2} (µS)	
				Typical	Maximum	Typical	Maximum	Typical	Maximum
1	AT86RF212B	1	1	150	1500	420	1000	390	1000
2	AT86RF231	1	1	60	1000	330	-	380	-
3	AT86RF232	0.1	1	50	1000	330	1000	210	1000
4	AT86RF233	0.1	1	50	1000	330	1000	210	1000
5	ATmega128RFA1	1	1	60	1000	-	-	240	-
6	ATmega64/128/256RFR2	1	1	60	1000	-	-	240	-
7	ATmega644/1284/2564RFR2	1	1	60	1000	-	-	240	-

2.5 Digital ground pins (DVSS)

Digital ground pins are designated as DVSS and they provide ground reference for digital domain. Reference schematics for connecting digital ground pins are shown in Figure 2-5.

Digital ground pinouts available on Atmel wireless chipsets are given in Table 2-6.

Table 2-6. Digital ground pinouts

S.No	Chipsets	DVSS
1	AT86RF212B	Pin 7, 12, 16, 18 and 21
2	AT86RF231	Pin 7, 12, 16, 18 and 21
3	AT86RF232	Pin 7, 12, 16, 18 and 21
4	AT86RF233	Pin 7, 12, 16, 18 and 21
5	ATmega128RFA1	Pin 20, 24, 35, 45 and 55
6	ATmega64/128/256RFR2	Pin 20, 24, 35, 45 and 55
7	ATmega644/1284/2564RFR2	Pin 14

Figure 2-5. Connecting digital ground pins

Caution: In this example we connected both Digital ground (DVSS) and Analog ground (AVSS) to the same ground plane, for providing solid continuous ground plane. Designer should find a better solution to isolate the digital noise from RF/Analog domain during layout design, if the board is affected by such interferences.

2.6 Reset

Reset pinouts available on Atmel wireless chipsets are given in Table 2-7. Reset pin of transceivers have to be controlled by the master MCU using GPIO pin, refer section 4 Transceiver to microcontroller interface for more details.

Table 2-7. Reset pinouts

S.No	Chipsets	RSTN	RSTON
1	AT86RF212B	Pin 8	-
2	AT86RF231	Pin 8	-
3	AT86RF232	Pin 8	-
4	AT86RF233	Pin 8	-
5	ATmega128RFA1	Pin 12	Pin 13
6	ATmega64/128/256RFR2	Pin 12	Pin 13
7	ATmega644/1284/2564RFR2	Pin 10	-

For ATmega64/128/256RFR2 and ATmega644/1284/2564RFR2 chipsets, refer to Figure 2-6 for connecting RSTN pin and Figure 2-7 for connecting RSTN to external reset switch. Reset switch SW1 circuitry is not mandatory but it will be useful in implementing hardware reset option.

Figure 2-6. Connecting RSTN pin of ATmega64/128/256RFR2 and ATmega644/1284/2564RFR2

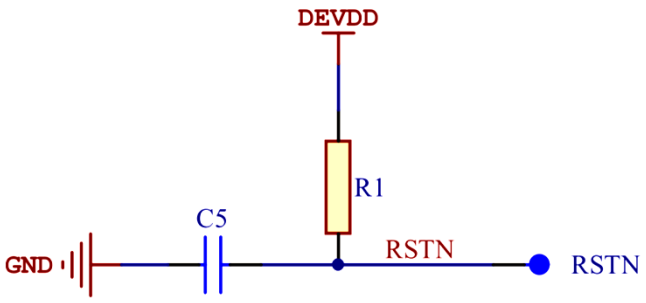
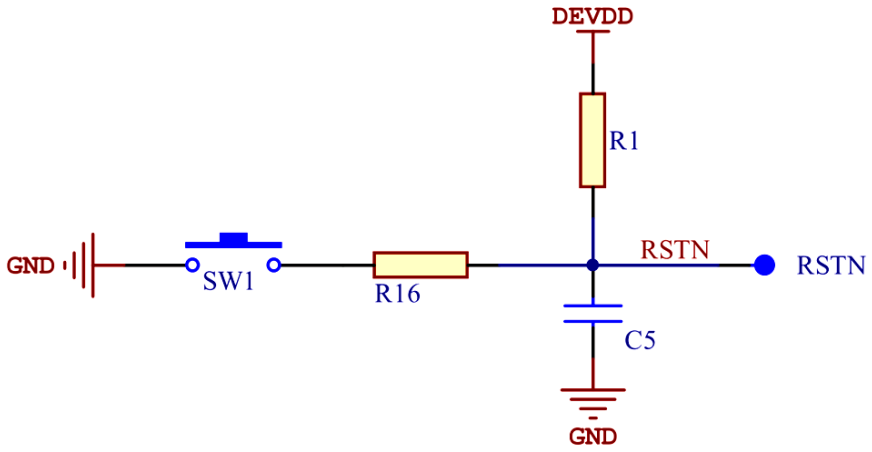


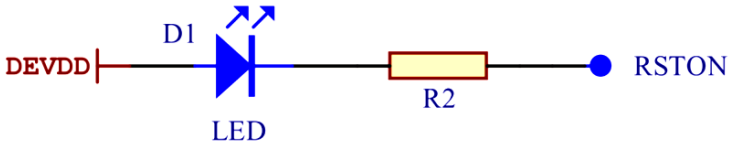
Figure 2-7. Connected external Reset switch for ATmega64/128/256RFR2 or ATmega644/1284/2564RFR2



- **R1: 10k ohm**
- **C5: 10pF (Ceramic capacitor) (optional)**
- **SW1: Press switch (optional)**
- **R16: 330 ohm (optional)**

Similarly LED indication on RSTON is optional, but this LED serves as the indication of whether the MCU is reset or not. As per the RSTON circuitry shown in Figure 2-8, LED D1 will glow if the MCU is in reset condition. Refer section 3.2 Pin Descriptions in SoC datasheet [2].

Figure 2-8. Connecting RSTON pin to LED



- **D1: LED (optional)**
- **R2: Current limiting resistor (optional)**

3. System clock and clock options

Various Clock options are available in Atmel chipsets are listed below,

- External 16MHz crystal serves as transceiver clock and also as system clock (in case of SoC)
- Internal 16MHz clock can only be used as system clock and not as transceiver clock (in case of SoC)
- External clock serves as transceiver clock and also as system clock (in case of SoC)
- External 32kHz crystal serves as RTC clock reference (in case of SoC)

16MHz crystal is usually used in Atmel wireless chipsets for producing accurate clock reference for the RF section, so that maximum deviation of carrier frequency meets the IEEE 802.15.4 standard requirement of +/-40 ppm. So it requires some efforts in choosing an apt crystal for their application. Atmel AVR2067: Crystal Characterization for AVR RF application note [3] provides easy selection guide for crystals. Using external 16MHz crystal in design adds to the BoM cost. Detailed description is given in section 3.1.

If the design is more concern on the cost, then external clock reference [3.2] option can be used as both system clock and transceiver clock instead of external 16MHz crystal, but this requires accurate external clock reference which should meet the IEEE 802.15.4 standard requirement of +/-40 ppm. Utilizing external clock option highly depends on the board design which should have the capability to source 16MHz clock.

Internal 16MHz oscillator can only be used as system clock and not as transceiver clock as it does not meet the require accuracy. Detailed description is available in the corresponding device datasheet [2].

External 32 kHz crystal is used to clock RTC module which is capable of running in Power Down of the SoC. For applications which sleeps and wakes periodically might require this 32 kHz crystal for counting the sleep period. Few applications might use other interrupt sources (like pin change interrupt, transceiver interrupt, etc) for waking the sleeping SoC, in such scenarios this 32 kHz crystal can be omitted. Detailed description is given in section 3.3.

3.1 16 MHz crystal (XTAL1 and XTAL2)

External 16MHz crystal is required for Atmel wireless chipsets, because RF frequency is derived from this 16MHz clock reference. So accuracy of external 16MHz crystal is important for proper RF operation refer Atmel AVR2067: Crystal Characterization for AVR RF application note [3].

16 MHz crystal (X1) along with two external load capacitors (C6 and C7) should be connected to XTAL1 and XTAL2 pins of the crystal oscillator circuitry as shown in Figure 3-1

Caution: To achieve the best accuracy and stability of the reference frequency, large parasitic capacitances should be avoided. Crystal lines should be routed as short as possible and not in proximity of digital I/O signals.

Board designers have the flexibility to tune the accuracy of crystal oscillator by varying the XTAL_TRIM register values.

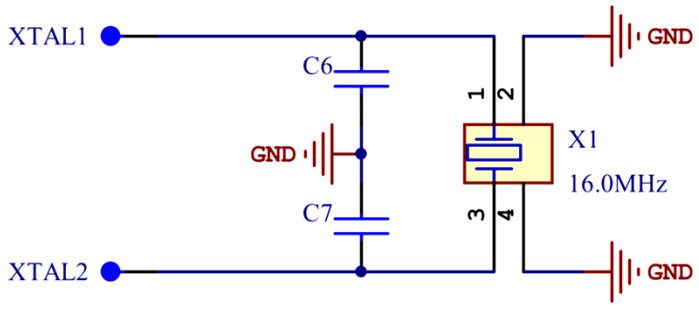
Note: XTAL_TRIM register is available in all Atmel wireless chipsets

16 MHz pinouts available on Atmel wireless chipsets are given in Table 3-1.

Table 3-1. XTAL pinouts

S.No	Chipsets	XTAL1	XTAL2
1	AT86RF212B	Pin 26	Pin 25
2	AT86RF231	Pin 26	Pin 25
3	AT86RF232	Pin 26	Pin 25
4	AT86RF233	Pin 26	Pin 25
5	ATmega128RFA1	Pin 56	Pin 57
6	ATmega64/128/256RFR2	Pin 56	Pin 57
7	ATmega644/1284/2564RFR2	Pin 41	Pin 42

Figure 3-1. Connecting external 16MHz crystal



- **X1: 16 MHz crystal**
- **C6: Load capacitor (Ceramic capacitor)**
- **C7: Load capacitor (Ceramic capacitor)**

Caution: C6 and C7 load capacitance values can vary from 8pF to 14pF. Load capacitor values vary depending on the crystal and board design

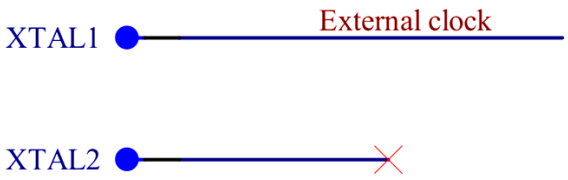
3.2 External clock reference

External clock pinouts available on Atmel wireless chipsets are given in Table 3-2. External clock input should be fed through XTAL1 as shown in Figure 3-2. When applying an external clock, it is required to avoid sudden changes in the applied clock frequency to ensure stable operation of the microcontroller unit (MCU). A variation in frequency of more than 2% from one clock cycle to the next can lead to unpredictable behavior. If changes of more than 2% are required, ensure that the MCU is kept in Reset during the changes.

Table 3-2. External clock pinouts

S.No	Chipsets	XTAL1	XTAL2	CLKI
1	AT86RF212B	Pin 26	Do not connect	-
2	AT86RF231	Pin 26	Do not connect	-
3	AT86RF232	Pin 26	Do not connect	-
4	AT86RF233	Pin 26	Do not connect	-
5	ATmega128RFA1	Do not connect	Do not connect	Pin 33
6	ATmega64/128/256RFR2	Do not connect	Do not connect	Pin 33
7	ATmega644/1284/2564RFR2	Do not connect	Do not connect	Pin 25

Figure 3-2. Connecting external 16MHz clock source



Caution: The oscillation peak-to-peak amplitude shall be between 100 mV and 500 mV, the optimum range is between 400 mV and 500 mV.

Warning: XTAL2 should not be wired.

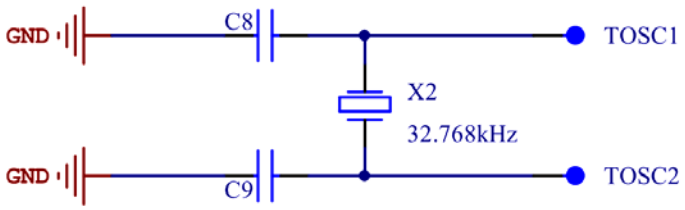
3.3 32.768 kHz crystal (TOSC1 and TOSC2)

32.768 kHz crystal clock can be as input to Timer/Counter2 running in asynchronous mode which is used as interrupt source for waking up from Power Save mode of SoC. For more details refer to section AVR Microcontroller Sleep Modes in SoC Datasheets [2]. 32.768 kHz pinouts available on Atmel SoC are given in Table 3-3. Refer Figure 3-3 for connecting the 32.768 kHz crystal with SoC, for more details on crystal selection refer to [3] [4].

Table 3-3. TOSC pinouts

S.No	Chipsets	TOSC1	TOSC2
1	ATmega128RFA1	Pin 17	Pin 18
2	ATmega64/128/256RFR2	Pin 17	Pin 18
3	ATmega644/1284/2564RFR2	Pin 12	Pin 13

Figure 3-3. Connecting external 32.768kHz crystal



- **X2: 32.768 kHz crystal**
- **C8: Load capacitor (Ceramic capacitor)**
- **C9: Load capacitor (Ceramic capacitor)**

4. Transceiver to Microcontroller interface

Atmel transceivers are true SPI-to-antenna solution, which can be controlled using an external Microcontroller like Atmel's AVR Microcontroller [5] or Atmel ARM based solution [6] and the interface diagram is given in Figure 4-2.

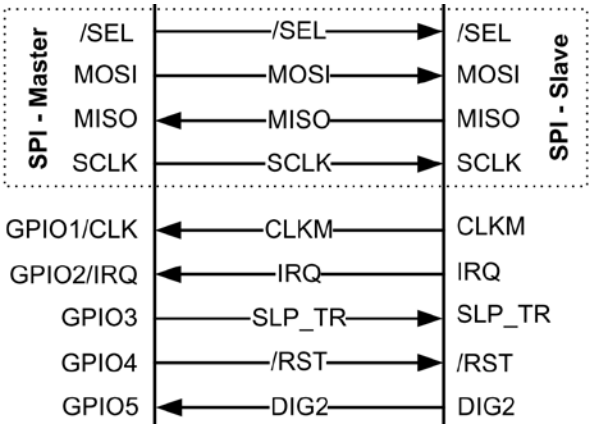
Microcontroller interface pinouts available on Atmel transceiver chipsets are given in Table 4-1.

Table 4-1. Microcontroller interface pinouts

S.No	Chipsets	/SEL	SCLK	MISO	MOSI	RSTN	SLP_TR	IRQ	DIG2	CLKM
1	AT86RF212B	Pin 23	Pin 19	Pin 20	Pin 22	Pin 8	Pin 11	Pin 24	Pin 10	Pin 17
2	AT86RF231	Pin 23	Pin 19	Pin 20	Pin 22	Pin 8	Pin 11	Pin 24	Pin 10	Pin 17
3	AT86RF232	Pin 23	Pin 19	Pin 20	Pin 22	Pin 8	Pin 11	Pin 24	Pin 10	Pin 17
4	AT86RF233	Pin 23	Pin 19	Pin 20	Pin 22	Pin 8	Pin 11	Pin 24	Pin 10	Pin 17
5	MCU	/SS	SCLK	MISO	MOSI	GPIO	GPIO	INT	TC*	External Clock source*

*Optional interface option

Figure 4-2. Interfacing MCU with Atmel transceivers



4.1 Filter for CLKM

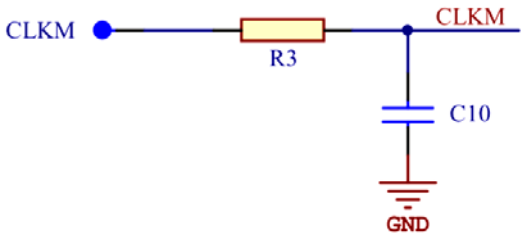
The generated reference clock signal can be fed to a microcontroller using pin 17 (CLKM). Transceiver's 16 MHz raw clock can be divided by an internal prescaler. Thus, clock frequencies of 16 MHz, 8 MHz, 4 MHz, 2 MHz, 1 MHz, 250 kHz, or 62.5 kHz can be supplied by pin CLKM. The CLKM frequency, update scheme, and pin driver strength is configurable using register 0x03 (TRX_CTRL_0) which can be used as,

- microcontroller clock source
- high precision timing reference
- MAC timer reference

Crosstalk from digital signals on the crystal pins or the RF pins can degrade the system performance. Therefore, a low pass filter (C10, R3) is placed close to the CLKM output pin to reduce the emission of CLKM signal harmonics as shown in Figure 4-3.

Caution: When using CLKM along with external Front End Module (FEM), there might be an amplification of CLKM signal by the external FEM due to coupling effects, so care should be taken while routing CLKM line. So it is recommended to run the microcontroller using the internal RC oscillator.

Figure 4-3. Filter for CLKM



- **C10: 2.2pF**
- **R3: 680 ohm**

Note: Designed for CLKM @1MHz

Caution: If CLKM is not used as microcontroller clock source then it has to be turned off in firmware during device initialization and low pass filer is not needed.

4.2 RX frame time stamping (DIG2)

DIG2 pin is used to determine the exact timing of an incoming frame and the reception of this frame can be signaled to the microcontroller via pin DIG2. The pin turns from L to H after a detection of a valid PHR. This function is enabled with register bit IRQ_2_EXT_EN (register 0x04) set. DIG2 pin could be connected to a timer capture unit of the microcontroller.

When enabled, DIG2 is set to DIG2 = H at the same time as IRQ_2 (RX_START), even if IRQ_2 is disabled.

Caution: If DIG2 pin is not used for RX Frame Time Stamping it can be configured for Antenna Diversity. If the application requires both RX Frame Time Stamping and Antenna Diversity features then refer the section 7.

5. Balun/Filter

Balun/Filter operates as a differential (balanced) to single-ended (unbalanced) converter connecting Atmel chipsets with antenna. The design might requires two DC blocking capacitors as shown in Figure 5-2,

- C11 on DC feed/GND pin (optional, refer Balun datasheet for more information)

- C12 on the unbalanced output pin (optional, refer Balun datasheet for more information)

For recommended Balun/Filters from Johanson Technologies refer to [7] and for Wurth refer to [8]. Balanced RF pinouts available on Atmel wireless chipsets are given in Table 5-1.

Table 5-1. Balanced RF pinouts

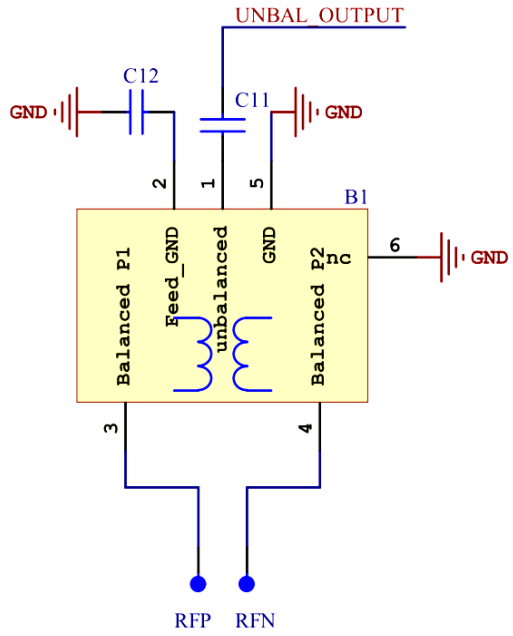
S.No	Chipsets	RFP	RFN	Recommended Wurth Balun Part Number	Recommended Johanson Balun/Filter Part number
1	AT86RF212B	Pin 4	Pin 5	-	0896FB15A0100(1)
2	AT86RF231	Pin 4	Pin 5	748421245	2450FB15L0001(2)
3	AT86RF232	Pin 4	Pin 5	748421245	2450BM15A0015(3)
4	AT86RF233	Pin 4	Pin 5	748421245	2450BM15A0015(3)
5	ATmega128RFA1	Pin 8	Pin 9	748421245	2450FB15L0001(2)
6	ATmega64/128/256RFR2	Pin 8	Pin 9	748421245	2450BM15A0015(3)
7	ATmega644/1284/2564RFR2	Pin 6	Pin 7	748421245	2450BM15A0015(3)

(1) Only C11 required

(2) Only C12 required

(3) Both C11 and C12 not required

Figure 5-2. Connecting RFP/RFN pins to Balun/Filter



- **B1: Balun**
- **C11: 22pF for 2.4GHz (100pF for Sub-GHz) (applicable for Johanson Balun only)**
- **C12: 22pF for 2.4GHz (100pF for Sub-GHz) (applicable for Johanson Balun only)**

Caution: It is always recommended to use COG/NPO grade capacitors for C11 and C12

6. External FEM control (DIG3 and DIG4)

External Front End Module (FEM) can be included in the design for improving the transmit power and receiver sensivity of the final product. FEM shall have features like transmit power amplifier (PA) with harmonic filtering, receive low noise amplifier (LNA) with optional bypass switch, transmit/receive (TR) switching and an antenna diversity switch.

Caution: Low pass filter/matching might be required at the antenna ports to reduce harmonic levels at these higher output powers. Refer section 8.

As the impact of removing balun while using external FEM is minimal, it is possible to reduce Bill of material by avoiding balun in design. Refer FAQ [9]

Warning: Some application requirement might required balun as well, so the designer has to decide on the need for using Balun in their designs

Note: The unused RFN or RFP pin have to be terminated to ground with a 50Ω resistor and DC block capacitor; refer section 9 for terminating unused pins.

For example we have considered SE2431L [10] as the external FEM, Table 6-1 provides the mapping of SE2431L's control lines with Atmel chipsets. And the reference schematic is shown in Figure 6-2.

Other FEM chips includes SE2438T [11], RC6505 [12], RC6575 [13], RC6555 [14] etc. Atmel AT03188: Performance Test EVK with External FEM [15] shall guide the user in adding support for external FEM in IEEE 802.15.4 MAC stack.

Please note that different FEM chips contain different control logics, so it is the scope of the designer to refer the FEM datasheet and map accordingly.

Table 6-1. Control lines for SE2431L, external FEM

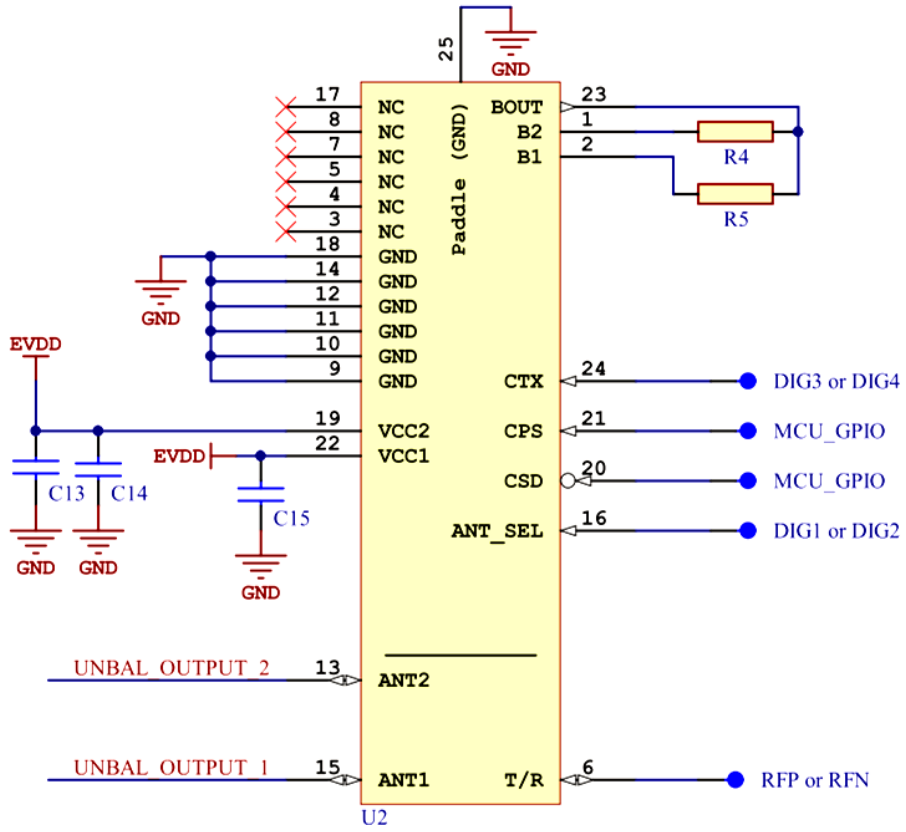
SE2431L	Atmel chipsets	Comments
Antenna1	-	Connected to external antenna 1, selection of antenna is based on ANT_SEL control logic
Antenna2	-	Connected to external antenna 2, selection of antenna is based on ANT_SEL control logic
T/R	RFP or RFN	RF input for Power Amplifier (PA) and RF output from Low Noise Amplifier (LNA)
ANT_SEL	DIG1 or DIG2	signal to control antenna switch
CSD	GPIO	Connect to GPIO signal to control SE2431L modes, refer [10]
CPS	GPIO	Connect to GPIO signal to control SE2431L modes, refer [10]
CTX	DIG3 or DIG4	Control signal for selecting TX or RX path

Note: Refer the datasheet of external FEM for more information on the different modes and corresponding logical states.

Note: AT86RF232 transceiver does not support RX/TX indicator feature for controlling external FEM

Note: Optional filter capacitors can be used on the Control signal lines to avoid signal coupling.

Figure 6-2. Connecting RFP/RFN pins to SE2431L, external FEM



- **U2: SE2431L, External Front End Module (FEM)**
- **C13: 22pF**
- **C14: 10pF**
- **C15: 10pF**
- **R4: 49.9 ohm**
- **R5: 1.5 kohm**

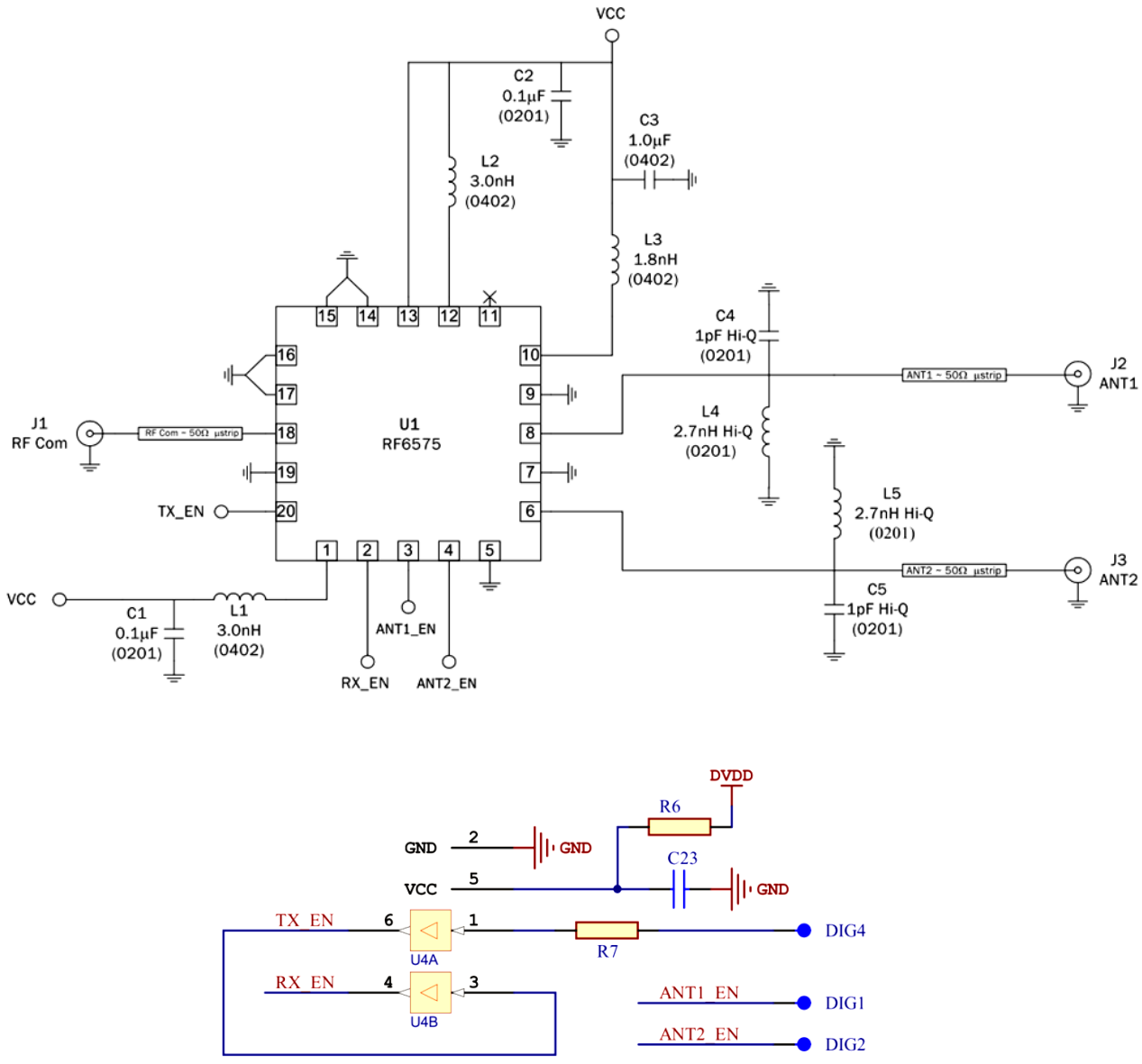
Special consideration is required for ATmega644/1284/2564RFR2 as the chips contains only DIG4 line multiplexed with JTAG TCK interface. For more details refer to the FAQ [16]. For example if custom board is based on ATmega644/1284/2564RFR2 and RFMD's RF6575 [13] as external FEM, then below schematic mapping Table 6-2 and Figure 6-3 might be required.

Table 6-2. Control lines for RF6575, external FEM

RF6575	Atmel chipsets	Comments
ANT1	-	Connected to external antenna 1, selection of antenna is based on ANT1_EN control logic
ANT2	-	Connected to external antenna 2, selection of antenna is based on ANT2_EN control logic
RF_COM	RFP or RFN	RF input for Power Amplifier (PA) and RF output from Low Noise Amplifier (LNA)
ANT1_EN	DIG1	signal to control antenna1 switch
ANT2_EN	DIG2	signal to control antenna2 switch

RF6575	Atmel chipsets	Comments
TX_EN	DIG3	Enable logic for PA and transmit switch
RX_EN	DIG4	Enable logic for LNA and receive switch

Figure 6-3. Connecting RFP/RFN pins to RF6575, external FEM



- **U4A/B: Dual inverter chip**
- **R6: 2.2 kohm**
- **R7: 2.2 kohm**
- **C23: 100nF**

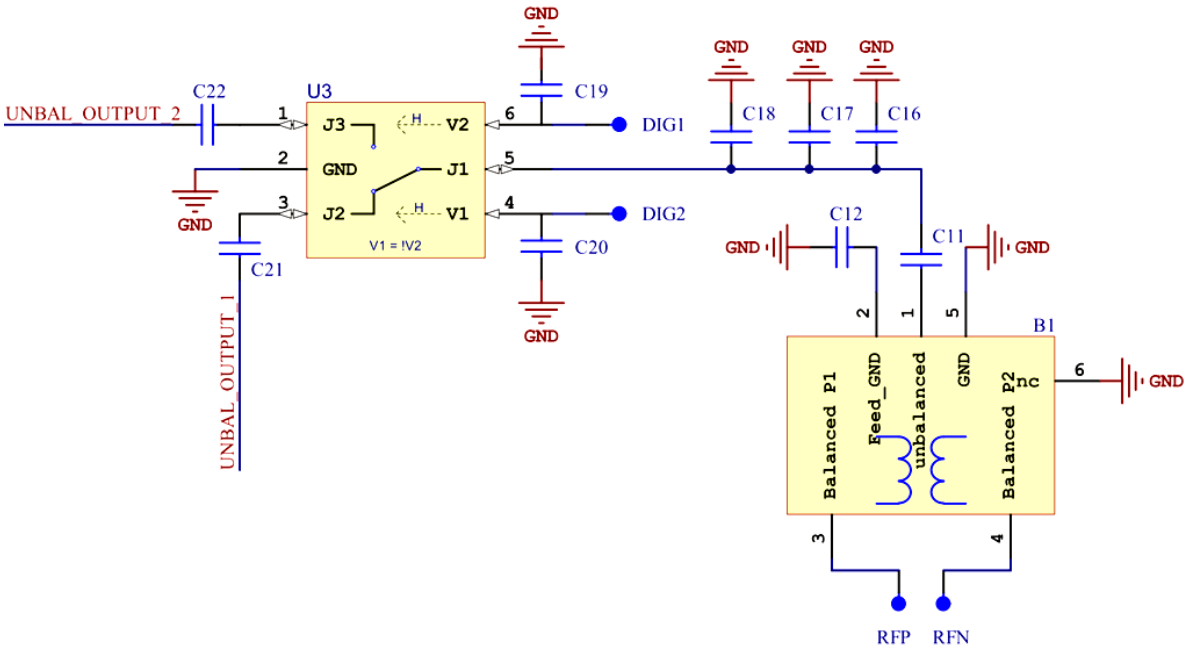
7. Antenna Diversity control (DIG1 and DIG2)

To improve the reliability of an RF link between network nodes Antenna Diversity can be applied to reduce effects of multipath propagation and fading. Antenna Diversity uses two antennas to select the most reliable RF signal path. This is done by the radio transceiver automatically using DIG1 and DIG2 lines during preamble field search without the need for microcontroller interaction. To ensure highly independent receive signals on both antennas, the antennas should be carefully separated from each other [17].

Transmission line should be impedance matched by using optional tuning capacitors [25]. The capacitance value and the position of the capacitor can be changed to tune the impedance of the system. To vary the capacitor position along the line, the tuning capacitor can be assembled to any one of C16, C17 or C18 footprints as shown in Figure 7-1. C21 and C22 capacitors block any DC voltage on RF lines.

Caution: RF switch, balun and filters are always associated with signal loss, so it is always recommended to refer the individual datasheets while taking design loss in account.

Figure 7-1. Connecting RF switch using DIG1 and DIG2



- **B1: Balun**
- **U3: RF switch**
- **C11, C12: 22pF for 2.4GHz (100pF for Sub-GHz) (applicable for Johanson Balun only)**
- **C16, C17, C18: Tuning capacitor for impedance control**
- **C19, C20, C21, C22: 22pF**

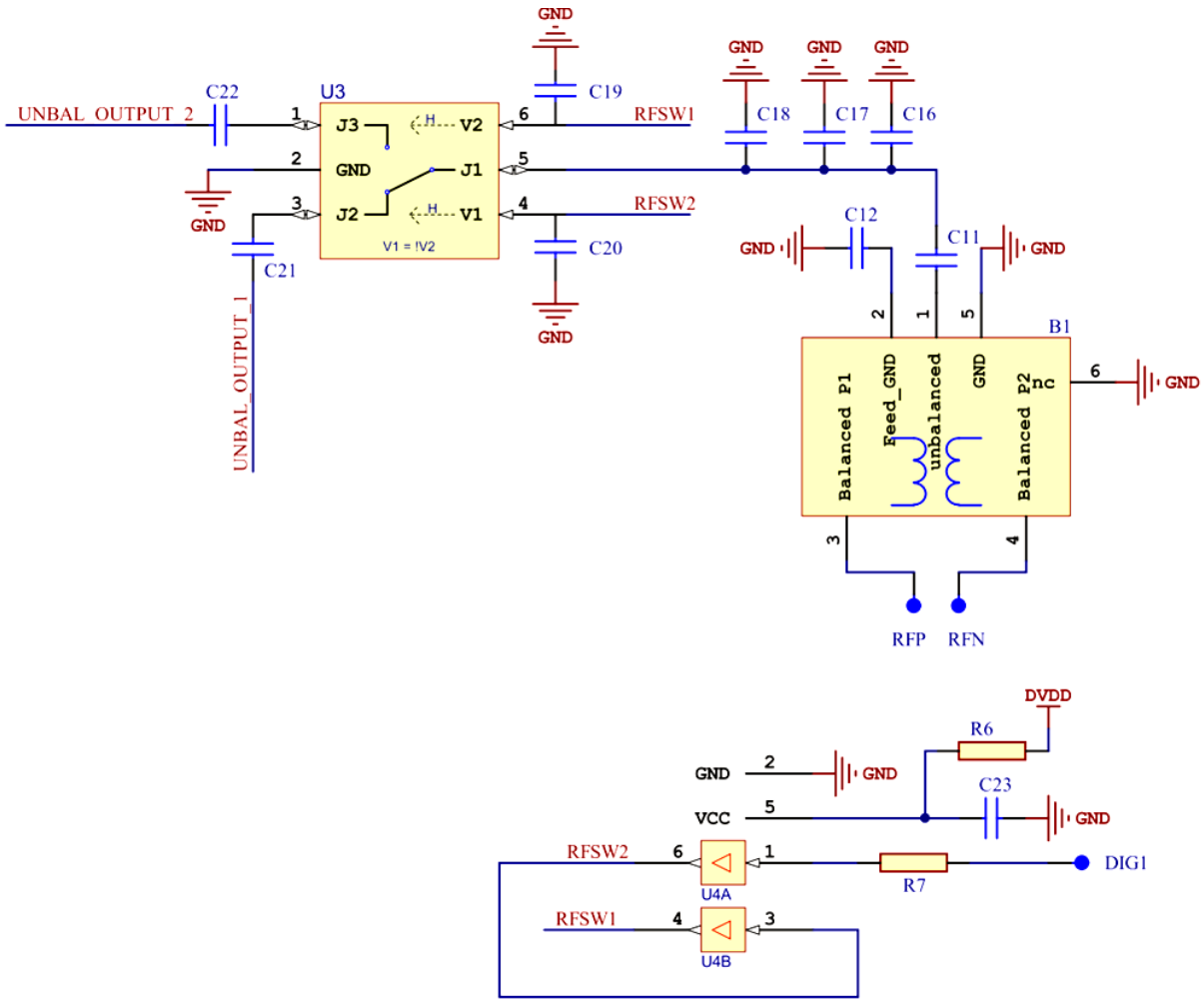
Caution: It is always recommended to use COG/NPO grade capacitors for C11, C12, C16, C17, C18, C21 and C22.

Caution: Typical tuning capacitor values are in between 0.5pF and 1pF if Johanson Balun is used.

Caution: Noise interfering on the DIG1 and DIG2 control pins may cause undesired modulation of the RF signal. So it is recommended to place C19 and C20 capacitors as close to RF switch to short any control line noise.

If the application requires DIG2 line for time stamping, then the antenna diversity differential logic has to be derived from DIG1 pin using an external dual inverter chip, refer Figure 7-2 for reference. Switching characterstics of inverter chip is important and minimum switching delay has to be considered. So DIG2 line can be made available for time stamping feature 4.3.

Figure 7-2. Connecting RF switch using DIG1



- **U4A/B: Dual inverter chip**
- **R6: 2.2 kohm**
- **R7: 2.2 kohm**
- **C23: 100nF**

Caution: Typical tuning capacitor values are in between 0.5pF and 1pF if Johanson Balun is used.

Caution: It is always recommended to use COG/NPO grade capacitors for C11, C12, C16, C17, C18, C21 and C22.

8. Antenna

The unbalanced output from balun or from external FEM needs to be connected with an antenna through a transmission line of impedance 50Ω. PCB trace in combination with tuning capacitors can be used for impedance matching. Under normal conditions only one capacitor is assembled at position C26, C27, C28 or C29. These four positions allow varying the position of the capacitor along the transmission line as shown in Figure 8-1. The capacitance value and the position of the capacitor can be changed to tune the system. Further Pi low pass filter (not mandatory) can be designed using C24-L1-C25 components for surpressing out of band harmonics.

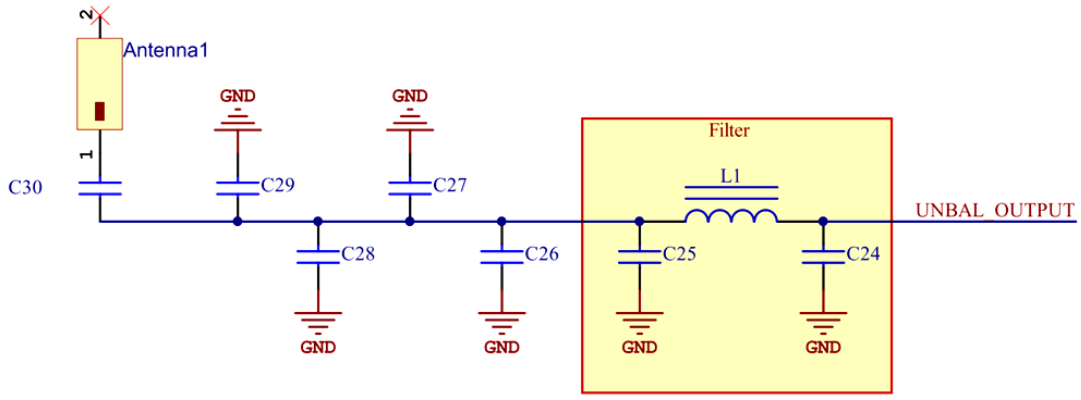
Note: Custom prototyping board can also have more than four capacitor mounting slots as well for tuning and it depends on the length of the transmission line.

First verify the line impedance is matched to 50Ω using network analyzer. During tuning best compromise between RX and TX performance has to be found.

Goal of tuning is achieve better link budget, so measurements like Receiver sensitivity, Transmitting power, EVM, spurious emissions and performance flatness over the whole frequency band are required for validating the design.

Capacitor C30 might be used for matching chip antenna's impedance with the transmission line [25] and [26].

Figure 8-1. Low pass filter and Impedance matching with an antenna



- **Antenna1 (chip antenna or PCB antenna or SMA Whip antenna)**
- **L1, C24, C25: Low pass filter (optional)**
- **C26, C27, C28, C29: Tuning capacitor for impedance control**
- **C30 (optional, values are based on antenna and board design)**

Caution: It is always recommended to use COG/NPO grade capacitors for C24, C25, C26, C27, C28, C29 and C30.

Caution: Typical tuning capacitor values are in between 0.5pF and 1pF if Johanson Balun is used (without Low pass filter).

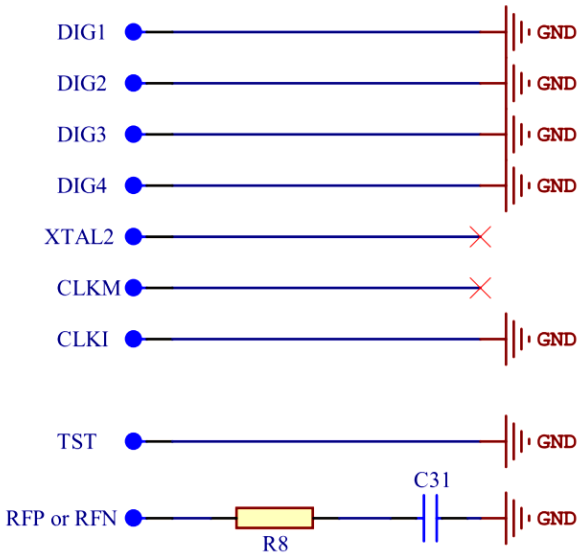
Caution: If low pass filter is used, then impedance matching should consider both tuning capacitors and filter components during RF design.

9. Terminating unused pins

Some of the pins on the chipset may not be used in the design; these pins have to be terminated properly as shown in Figure 9-1. TST pin is used for Parallel programming in ATmega64/128/256RFR2 and ATmega644/1284/2564RFR2 chipsets [2], if not used this pin have to be grounded.

If external reference clock (section 3.2) is not used in the design, then CLKI pin have to be grounded.

Figure 9-1. Terminating unused pins



- **R8: 51 ohm**
- **C31: 10pF (Ceramic capacitor)**

Caution: In this example we connected both Digital ground (DVSS) and Analog ground (AVSS) to the same ground plane, for providing solid continuous ground plane. Designer should find a better solution to isolate the digital noise from RF/Analog domain, if the board is affected by such interferences.

10. Programming interfaces

10.1 JTAG connectivity

The JTAG interface consists of a 4-wire Test Access Port (TAP) controller that is compliant with the IEEE 1149.1 standard. The IEEE standard was developed to provide an industry-standard way to efficiently test circuit board connectivity (Boundary Scan).

Atmel AVR devices have extended this functionality to include full Programming and On-Chip Debugging support. JTAG pinouts available on Atmel SoC are tabulated in Table 10-1.

Table 10-1. JTAG pinouts

S.No	Chipsets	TCK	TDO	TMS	TDI	RSTN
1	ATmega128RFA1	Pin 3	Pin 5	Pin 4	Pin 6	Pin 12
2	ATmega64/128/256RFR2	Pin 3	Pin 5	Pin 4	Pin 6	Pin 12
3	ATmega644/1284/2564RFR2	Pin 1	Pin 3	Pin 2	Pin 4	Pin 10

When external circuitry shares the JTAG debug lines on the target application, series resistors should be used to avoid driver contention, as shown in Figure 10-1. The value of the resistors should be chosen so that the external circuitry and the chip do not exceed their maximum ratings (i.e. sink or source too much current).

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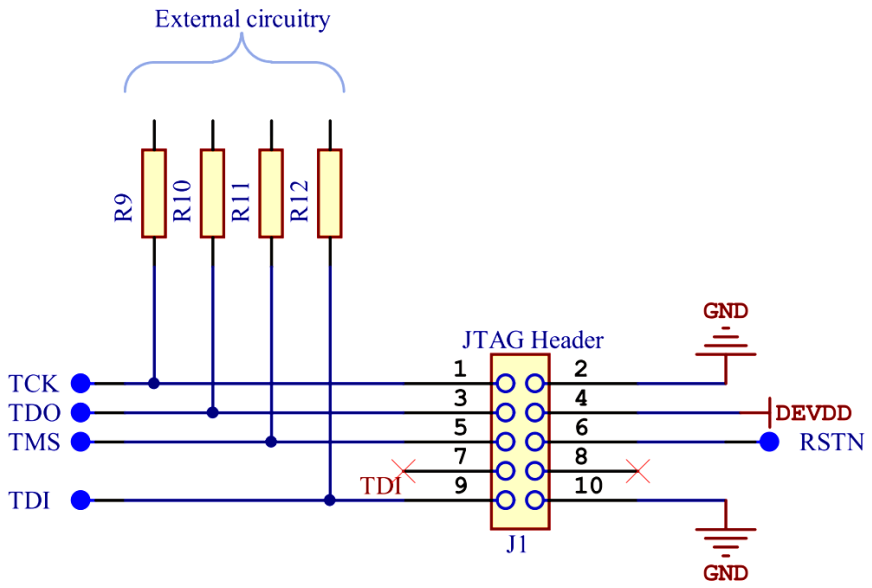
Figure 10-1. JTAG interface header



- **R9: 1kohm (optional)**
- **R10: 1kohm (optional)**
- **R11: 1kohm (optional)**
- **R12: 1kohm (optional)**

It is recommended to disconnect any analog filters on these lines (which should be on the 'outside' of the resistors) during a JTAG session, since these elements are discharged by the JTAG signals, possibly causing false logic levels influenced by the residual voltage in the capacitor.

If the filters cannot be disconnected, it is then recommended to apply target Vcc directly to the capacitor during a session to hold the voltage stable. Be sure to use a large enough resistor between the capacitor and the JTAG line when doing this [18].

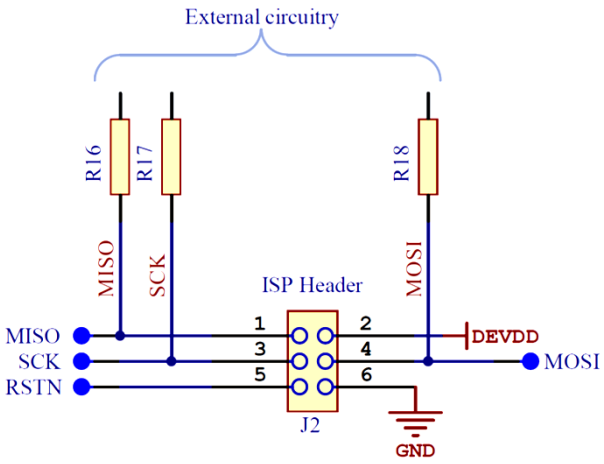
10.2 Serial Programming

Serial Programming bus can be used to download code into the Flash or EEPROM memories of SoC. The serial programming interface consists of pins SCK, PDI (input) and PDO (output) shown in Figure 10-2. If additional devices are connected to the ISP lines, series resistors have to added to protect the programmer from any device, that may try to drive the lines. Serial Programming pinouts available on Atmel SoC are given in Table 10-2.

Table 10-2. Serial Programming pinouts

S.No	Chipsets	PDO	PDI	SCK	RSTN
1	ATmega128RFA1	Pin 39	Pin 38	Pin 37	Pin 12
2	ATmega64/128/256RFR2	Pin 39	Pin 38	Pin 37	Pin 12
3	ATmega644/1284/2564RFR2	Pin 29	Pin 28	Pin 27	Pin 10

Figure 10-2. Serial Programming interface header



- **R16: 1kohm (optional)**
- **R17: 1kohm (optional)**
- **R18: 1kohm (optional)**

11. Interfacing MAC ID chip

Unique IEEE address for the products can be written into User Signature Row of SoC chipsets during production. Refer SoC datasheet for more information on procedure to read and write to User Signature Rows [2]. For designs which use microcontroller and transceiver combination, please refer individual microcontroller datasheets [5] to understand whether it supports User Signature Rows.

Alternate option is to use Atmel MAC ID chip (for example AT24MAC602) which contains a globally unique MAC or EUI address which can be used as Unique 64 bit IEEE MAC address for any IEEE 802.15.4 system.

This chip can be interfaced using I2C serial interface of Atmel chipsets and the I2C pinouts are given in Table 11-1. And example interfacing circuit is shown in Figure 11-2.

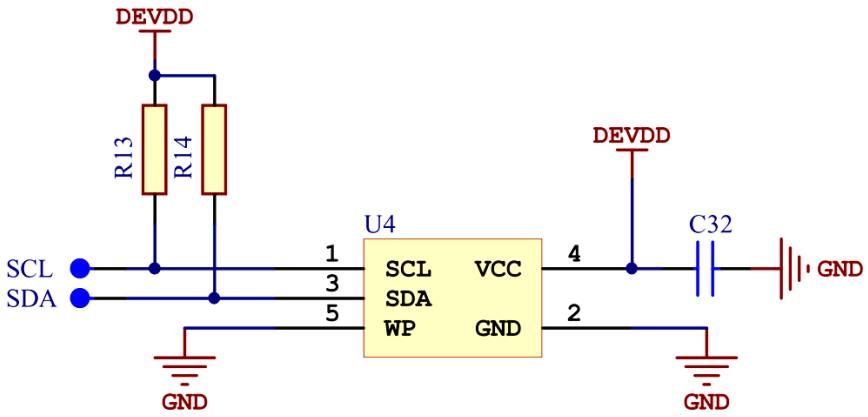
This chip also contains 2Kbit serial EEPROM, for more details refer to AT24MAC602 datasheet [19].

Table 11-1. I2C interface pinouts

S.No	Chipsets	SCL	SDA	WP
1	ATmega128RFA1	Pin 8	Pin 9	GPIO*
2	ATmega64/128/256RFR2	Pin 8	Pin 9	GPIO*
3	ATmega644/1284/2564RFR2	Pin 6	Pin 7	GPIO*

* Optional interface option

Figure 11-2. Interfacing external MAC ID chip



- **U4: AT24MAC602**
- **R13: 10kohm**
- **R14: 10kohm**
- **C32: 100nF (Ceramic capacitor)**

12. Interfacing EEPROM

If the application requires SPI based EEPROM, then it is also possible to store board related information or any application specific information. Pinouts and interface connections required for connecting external EEPROM is given in Table 12-1and Figure 12-2. For more details refer AT25010B datasheet [20].

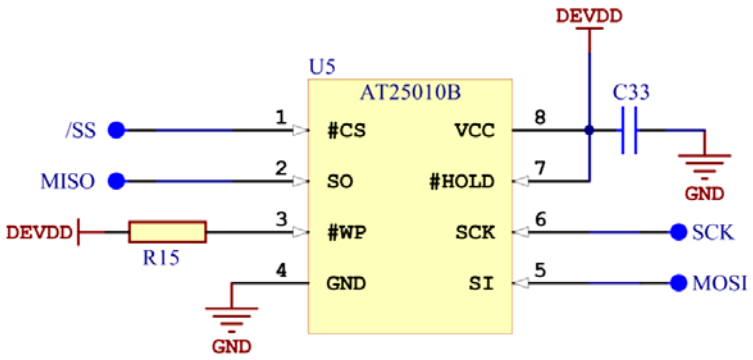
In the example ciruit we have pulled both #WP and #HOLD to DEVDD, if the application need control over these pins then it has to be connected to individual GPIO pins.

Table 12-1. EEPROM interface pinouts

S.No	Chipsets	/CS	SCK	SO	SI	/WP	/HOLD
1	ATmega128RFA1	/SS	SCK	MISO	MOSI	GPIO*	GPIO*
2	ATmega64/128/256RFR2	/SS	SCK	MISO	MOSI	GPIO*	GPIO*
3	ATmega644/1284/2564RFR2	/SS	SCK	MISO	MOSI	GPIO*	GPIO*

* Optional interface option

Figure 12-2. Interfacing external EEPROM



- **U5: AT25010B**
- **R15: 10k ohm**
- **C33: 100nF (Ceramic capacitor)**

13. Interfacing Serial Dataflash

Serial Dataflash will be required for some functionality like Over-the-Air Upgrade (OTAU) [22].Pinouts and interface connections required for connecting external Serial Dataflash is given in Table 13-1 and Figure 13-2. For more details refer AT45DB041D datasheet [21].

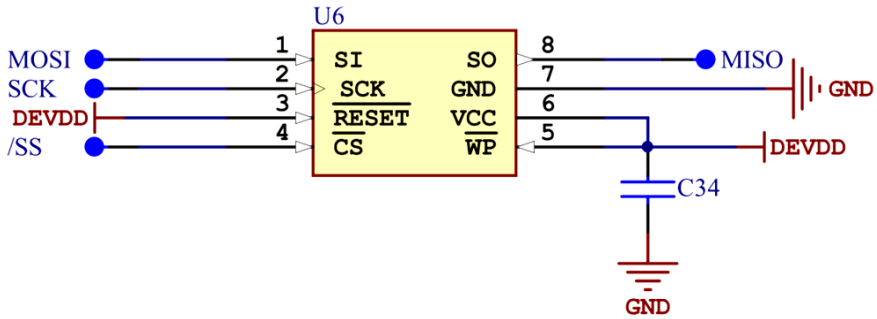
In the example ciruit we have pulled both #WP and #RESET to DEVDD, if the application need control over these pins then it has to be connected to individual GPIO pins. It is possible to interface more than one device on the same SPI bus. For example if the application requires both SPI based EEPROM and SPI based Serial Dataflash, then Chip select lines should be controlled accordingly.

Table 13-1. Serial Dataflash interface pinouts

S.No	Chipsets	/CS	SCK	SO	SI	/WP	/RESET
1	ATmega128RFA1	/SS	SCK	MISO	MOSI	GPIO*	GPIO*
2	ATmega64/128/256RFR2	/SS	SCK	MISO	MOSI	GPIO*	GPIO*
3	ATmega644/1284/2564RFR2	/SS	SCK	MISO	MOSI	GPIO*	GPIO*

* Optional interface option

Figure 13-2. Interfacing external Serial Dataflash



- **U6: AT45DB041D**
- **C34: 100nF (Ceramic capacitor)**

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15. Revision History

Doc. Rev.	Date	Comments
42157B	07/2013	Fixed footer issue
42157A	07/2013	Initial revision

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