LAB 3

Implement Lab 2 on
FPGA board

Due on 10/09/2018

05.00PM

Lab 3 – Up and Down Counter

- If last four digits of your N-number is "wxyz" then implement a counter counting from to 'wx' to 'yz' and a counter that counts from 'yz' to 'wx'
  - Use XDC/UCF files to map the counter design to FPGA board.
  - Generate bit file.
  - Program the FPGA and demonstrate the counter working.

Lab 3 – Up and Down counter

- For each design the DELIVERABLES are:
  - VHDL code (– Don'tinclude in the lab report in the zip).
    - Zip all the .vhd/UCF/XDC/.bit files as <netID>_Lab3_vhdl.zip
  - Submit a report as <netID>_Lab3_report.pdf which includes
    - Design block diagram.
    - Functional/Timing Simulation: Screen-shots of Isim/Modelsim wave window covering all counting steps.
    - Resource utilization.
    - Speed of the design.
    - Make a 4-5min demonstration of counter working on FPGA.

CAUTION – READ CAREFULLY

- **Important: We are using a Plagiarism checking service. Only one submission is available. You cannot resubmit/modify the report after submission. Please heed caution when submitting the report. Submit only the final version. Sending a modified report to TA/Professor is not allowed.**