AHD - LAB 4

FPGA implementation of simple function

and its inverse (loop)

Lab 4 – FPGA implementation of simple function and its inverse

- Perform timing simulation of the following given function and its inverse:
  - The design should accept 64 bit input (Din) and the initial A=Din[63 downto 32], B=Din[31 downto 0]

FUNCTION:

for i = 1 to 12 do

A = ((A xor B) <<< B) + S[2×i];
B = ((B xor A) <<< A) + S[2×i + 1];

INVERSE OF THE FUNCTION:

for i = 12 downto 1 do

B = ((B - S[2×i +1]) >>> A) xor A;
A = ((A - S[2×i]) >>> B) xor B;

'S' values are given in next slide

- You can use a clk signal and an asynchronous clear signal.

Lab 4 – FPGA implmentation of simple function and its inverse

The S values are:

S = [x"00000000", x"00000000", x"46F8E8C5", x"460C6085",
x"70F83B8A", x"284B8303", x"513E1454", x"F621ED22",
x"3125065D", x"11A83A5D", x"D427686B", x"713AD82D",
x"4B792F99", x"2799A4DD", x"A7901C49", x"DEDE871A",
x"36C03196", x"A7EFC249", x"61A78BB8", x"3B0A1D2B",
x"4DBFCA76", x"AE162167", x"30D76B0A", x"43192304",
x"F6CC1431", x"65046380"]

Lab 4– FPGA implementation of simple function and its inverse

- Design and implement the given function and its inverse
  - Simulate and analyze the designs.
  - Perform a timing simulation.
  - Calculate resource utilization and maximum speed.
  - Implement the design on an FPGA. Display the intermediate and final result on LEDs or 7-segment display.

Lab 4 – FPGA implementation of simple function and its inverse

- For each design, the DELIVERABLES are:
  - VHDL code and constraint file (Zip the files <netid>_<lab4>_vhdl.zip – Don't include in the lab report).
  - Submit Report (in pdf format <netID>_lab4_report.pdf):
    - **Test cases:** Test cases: 3 different values of "Din"
    - **Hand calculation** for one test vector(din). Just do it only for first three rounds. The hand calculation should be done for the test vectors that are used for functional simulation.
    - B**lock diagram**
    - Resource utilization: Report the utilization after synthesis and post-route phase.
    - Show a screen shot of your Isim/Modelsim window that verify the design output matches the test vectors you have generated by hand.
    - Report the critical path delay (minimum period), speed of operation-maximum clock frequency, and the latency (in number of clk cycles) of your design.
    - Explain how did you map the design logical ports to FPGA physical ports to provide inputs and display of the outputs.
    - Demo video of FPGA implementation - not more than 5 min.

CAUTION – READ CAREFULLY

Important: We are using a Plagiarism checking service. Only one submission is available. You cannot resubmit/modify the report after submission. Please heed caution when submitting the report. Submit only the final version. Sending a modified report to TA/Professor is not allowed.