LAB 2

Up and Down Counter

Due on 10/01/2018

10.00AM

Lab 2 – Up and Down Counter

- If last four digits of your N-number is "wxyz" then implement a counter counting from to 'wx' to 'yz' and a counter that counts from 'yz' to 'wx'
  - Draw and explain the block diagram of the counter designs.
  - Write a VHDL code and synthesize your design using Xilinx ISE/Vivado tools.
  - Perform functional and timing simulation using Modelsim/Isim tool.
  - Estimate speed of your design.
  - Calculate resource utilization.

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- For each design the DELIVERABLES are:
  - VHDL code (– Don't include in the lab report in the zip).
    - Zip all the .vhd files as <netID>_Lab2_vhdl.zip
  - Submit a report as <netID>_Lab2_report.pdf which includes
    - Design block diagram.
    - Functional/Timing Simulation: Screen-shots of Isim/Modelsim wave window covering all counting steps.
    - Resource utilization.
    - Speed of the design.
    - Make a 4-5min demonstration, capture the video, upload it to youtube and paste the link in the report.

CAUTION – READ CAREFULLY

- **Important: We are using a Plagiarism checking service. Only one submission is available. You cannot resubmit/modify the report after submission. Please heed caution when submitting the report. Submit only the final version. Sending a modified report to TA/Professor is not allowed.**