AHD - LAB #1

Left Rotate and Right Rotate

Demo Video due before 9/24/2018 (10 A.M)

Report due on 9/24/2018 (10 A.M)

Lab #1 – Left Rotate and Right Rotate Simulation

- Implement data dependent **32-bit left rotate** and **32-bit right rotate**
  - Simulate and verify your designs using Xilinx ISE/Vivado.
  - Perform functional and timing simulation (Modelsim/Isim).
  - Draw and explain the synthesized design.

Lab #1 – Left Rotate and Right Rotate Simulation

- For each design the DELIVERABLES are:
  - VHDL code (Zip the files – Don't include in the lab report in Zip).
    - Submit in assignment titled "Lab #1 "
  - Submit Report in PDF (separately from the VHDL code Zip file):
    - Test cases: 2 different values of "a." For each value of "a," simulate 2 different values of "b." At least one value of "b" should be greater than 32 (value).
    - Functional Simulation: Screen-shots of Isim/Modelsim wave window for all test cases.
    - Submit Block Diagram.
    - Hand calculation for the test cases that are used for the functional simulation.
  - Upload the demo video in Youtube→ (Set Privacy Settings to 'UNLISTED ")
  - https://support.google.com/youtube/answer/157177?hl=en
    - Place the link in report.

CAUTION – READ CAREFULLY

- **Important: We are using a Plagiarism checking service. Only one submission is available. You cannot resubmit/modify the report after submission. Please heed caution when submitting the report. Submit only the final version. Sending a modified report to TA/Professor is not allowed.**