**EL6463 ADV Hardware Design**

**Lab #2 – Up and Down Counter**

By

Name: xxxxx NetID: xxxx

# Date:2018/10/21

## 1. Theory and Block Diagram

In this lab, an 8-bit Up Counter and an 8-bit Down Counter were designed. A counter is a device which stores the number of times a particular event or process has occurred, often in relationship to a clock signal. The circuit is special type of shift register where the output of the last flipflop is feed back to the input of first flipflop. When the circuit is reset, except one of the flipflop output, all others are made zero. For n-flipflop counter has N different states. In this lab, N = 8. [1]

The circuit diagram for a 4-bit ring counter is shown below:

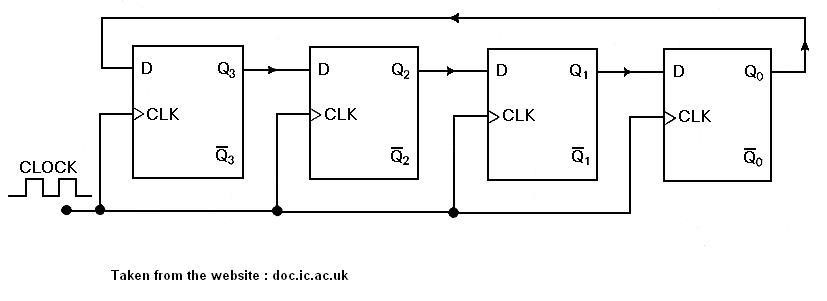
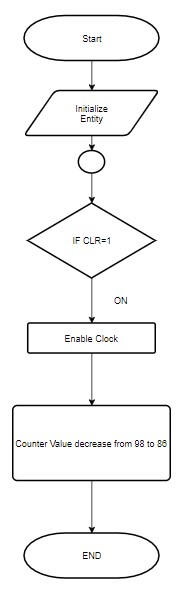
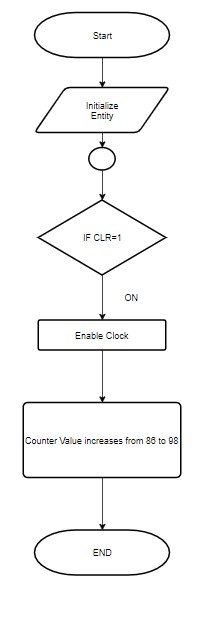


Figure 1. 4-bit counter

And the circuit diagram for an 8-bit counter contains 8 flipflop with the same structure.

In this lab, a counter has a 1-bit input and a 8-bit output, and an additional control signals. The flow charts were shown below:



**Figure 2. Flow chart for counter. Up (left), Down (Right)**

When the model start, all the value will be initialized, and when **clr** become 1, the clock will be enabled and the counter will begin to add or minus numbers.

Here because of two numbers I need to test are 98 and 86, they are both even numbers, a 2 will be added or minus for each clock enable in order to save processing time.

1. **Test Cases and Expected results:**

For Up Counter, 86 should be added to 98 steps by 2

For Down Counter, 98 should be decreased to 86 steps by 2.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 86 | 88 | 90 | 92 | 94 | 96 | 98 |
| 01010110 | 01011000 | 01011010 | 01011100 | 01011110 | 01100000 | 01100010 |

So, for Up Counter, the simulation result should show from left to right, and for Down Counter the simulation results should show from right to left.

1. **Simulation and Results The simulation results were shown below:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 86 | 88 | 90 | 92 | 94 | 96 | 98 |
| 01010110 | 01011000 | 01011010 | 01011100 | 01011110 | 01100000 | 01100010 |
|  | **Table 1. Up Counter results** | | | |  |  |
| 98 | 96 | 94 | 92 | 90 | 88 | 86 |
| 01100010 | 01100000 | 01011110 | 01011100 | 01011010 | 01011000 | 01010110 |

**Table 2. Down Counter results**

|  |  |  |
| --- | --- | --- |
|  | Synthesis Stage | Place and Route  Stage |
| LUT and FF pairs usage | 10 | 5 |
| IOB usage | 10(7%) | 10(7%) |
| RAM/DSP bl0cks used (if any) | N/A | N/A |

**Table 3. Up counter usage summary**

|  |  |  |
| --- | --- | --- |
|  | Synthesis Stage | Place and Route  Stage |
| LUT and FF pairs usage | 10 | 5 |
| IOB usage | 10(7%) | 10(7%) |
| RAM/DSP bl0cks used (if any) | N/A | N/A |

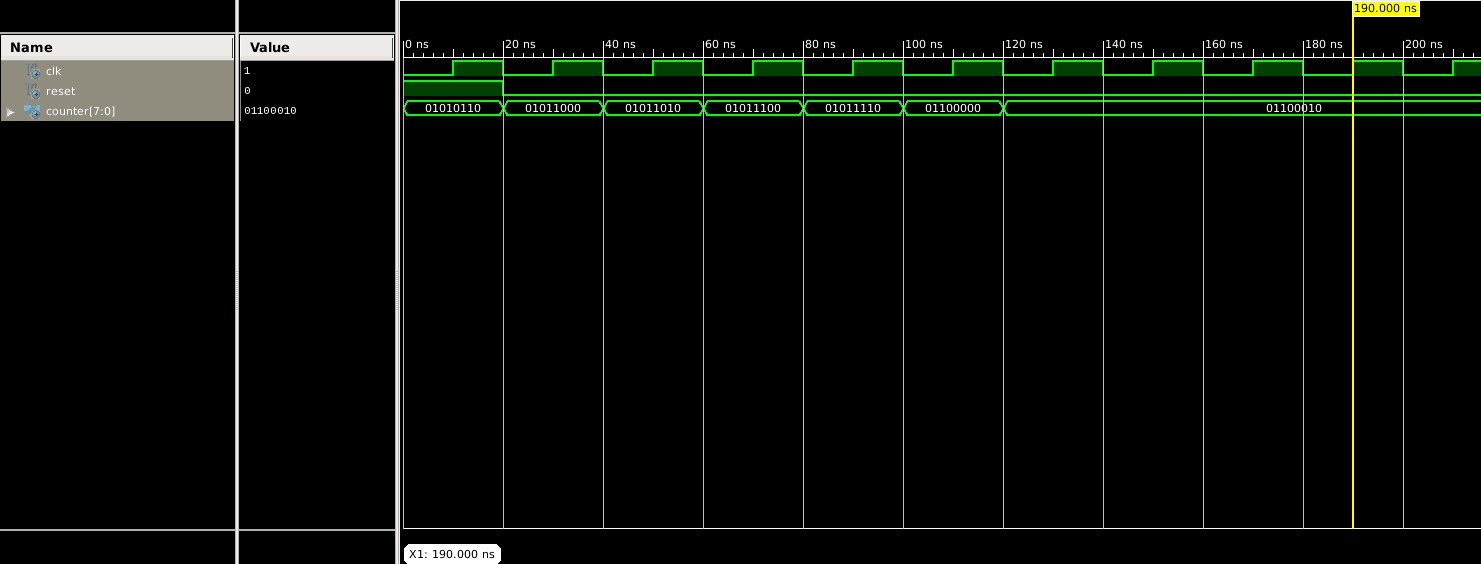
**Table 4. Down counter usage summary**

1. **Summary**

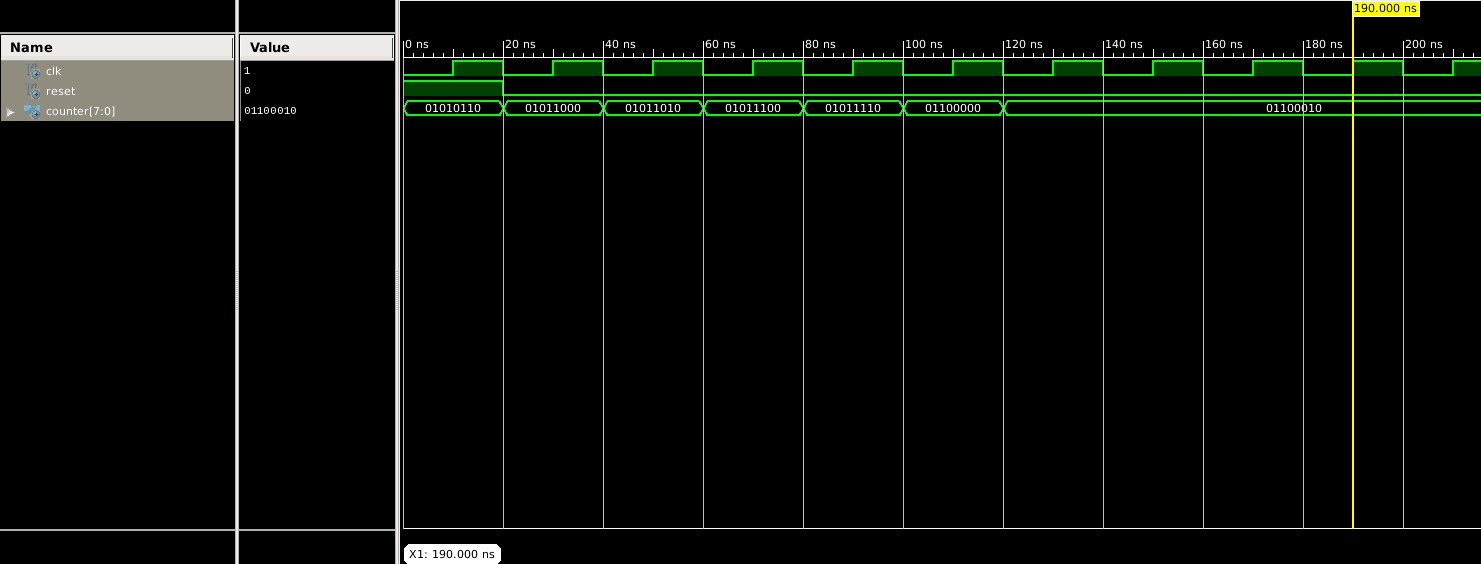
Based on the results, both up and down counter work well and because I don’t want the end value back to the initial value, I set the **i\_cnt** equal to the end value.

1. **Resources and Screen shot**

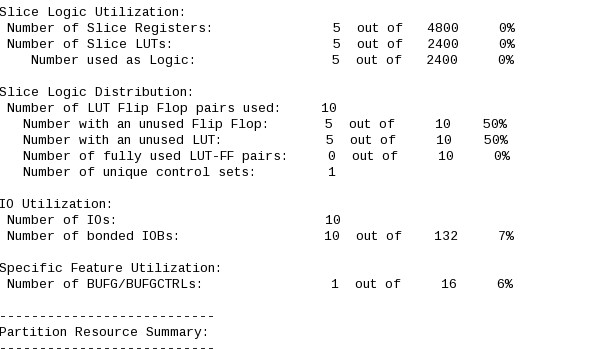
Function Simulation:

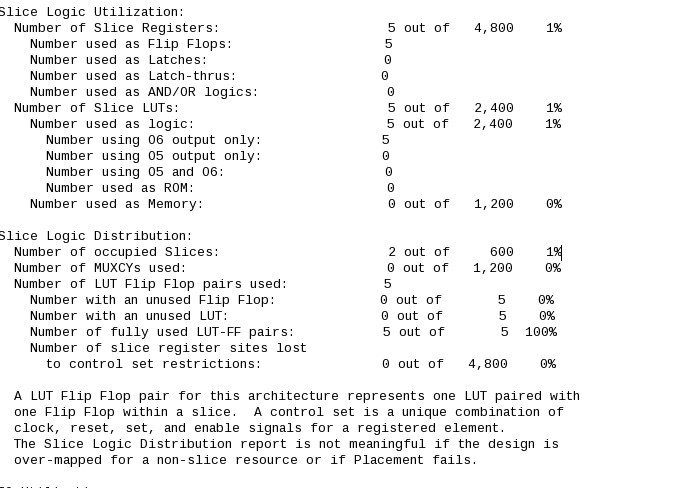


Timing Simulation:

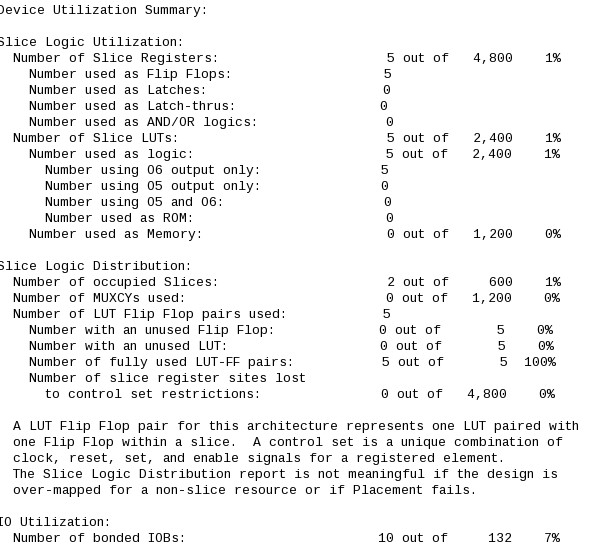
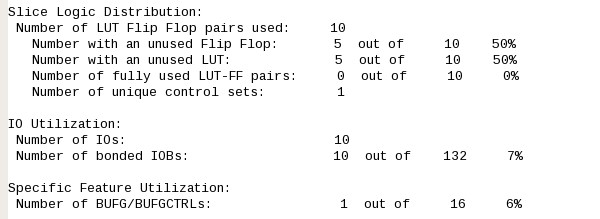
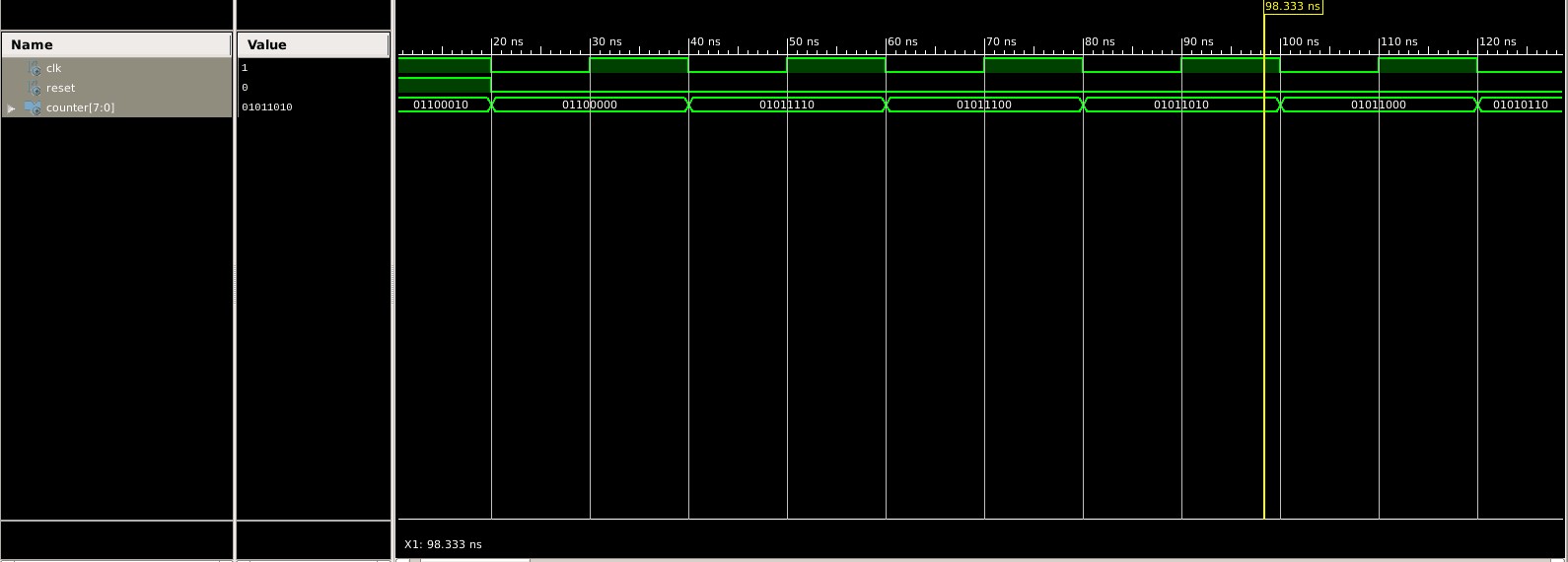


Resource Report:





Up Counter Simulation Results



Down Counter Simulation Value

1. **References and Notifications**

*[1] Vhdlguru.blogspot.com. (2018). Example: 4 bit Ring Counter with testbench. [online] Available at: http://vhdlguru.blogspot.com/2010/09/example-4-bit-ring-counter-with.html [Accessed 26 Sep. 2018]. [2]* *Karri, R. (2018). Advanced Hardware Design Lecture 2*

***The VHDL code files were zipped and submitted separately. All codes are based on Lecture 2 power point times. [2]***

## For video please click this link:xxxxxxx