浙江大学

本科实验报告

课程名称：	数字逻辑设计
姓　　名：	
学　　院：	竺可桢学院
专　　业：	混合班
指导教师：	董亚波
报告日期：	2025 年 3 月 28 日

浙江大学实验报告

课程名称：数字逻辑设计 实验类型：综合

实验项目名称：7 段数码管显示译码器设计与应用

学生姓名：__ 学号：___同组学生姓名：无

实验地点：紫金港东四 509 室 实验日期：2025 年 3 月 26 日

一、 实验目的

- 掌握七数码管显示原理
- 掌握七段码显示译码设计
- 进一步熟悉 Xilinx Vivado、Digital 环境及 SWORD 实验平台

二、操作方法与实验步骤

1. 原理图设计实现显示译码 MyMC14495 模块

实验原理为：

- 由 7+1 个 LED 构成的数字显示器件。
- 每个 LED 显示数字的一段，另一个为小数点。
- 逻辑表达式满足以下条件（可通过 K-Map 得出）：

$a= \bar{D}_3\bar{D}_2\bar{D}_1D_0+\bar{D}_3D_2\bar{D}_1\bar{D}_0+D_3\bar{D}_2D_1D_0+D_3D_2\bar{D}_1D_0$

$b= \bar{D}_3D_2\bar{D}_1D_0+D_2D_1\bar{D}_0+D_3D_2\bar{D}_0+D_3D_1D_0$

$c= \bar{D}_3\bar{D}_2D_1\bar{D}_0+D_3D_2\bar{D}_0+D_3D_2D_1$

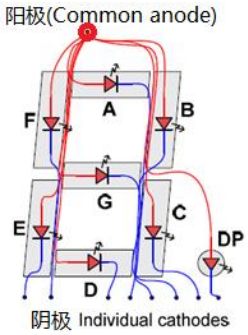
$d= \bar{D}_3\bar{D}_2\bar{D}_1D_0+\bar{D}_3D_2\bar{D}_1\bar{D}_0+D_2D_1D_0+D_3\bar{D}_2D_1\bar{D}_0$

$e= \bar{D}_3D_0+\bar{D}_3D_2\bar{D}_1+\bar{D}_2\bar{D}_1D_0$

$f= \bar{D}_3\bar{D}_2D_0+\bar{D}_3\bar{D}_2D_1+\bar{D}_3D_1D_0+D_3D_2\bar{D}_1D_0$

$g= \bar{D}_3\bar{D}_2\bar{D}_1+\bar{D}_3D_2D_1D_0+D_3D_2\bar{D}_1\bar{D}_0$

- 结构如图所示：



实验步骤如下：

- 在 Digital 中新建电路，名称用 MyMC14495。
- 原理图方式进行设计。
- 测试验证完成后导出 MyMC14495.v（可通过波形图等方式进行验证）。

2. 用 MyMC14495 模块实现数码管显示

实验要求：使用 MyMC14495 和开关，控制左上角 4 位数码管显示开关输入的数字，即把 Digital 上实现的测试功能在 Vivado 和实验板上实现。

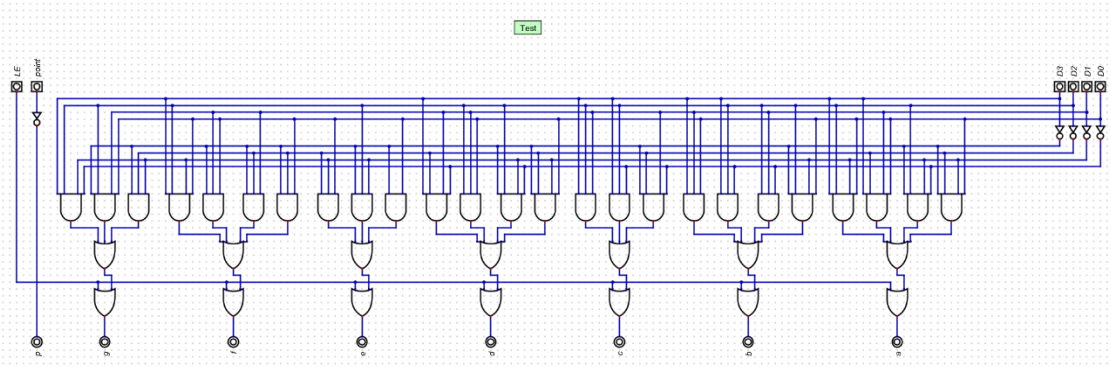
实验步骤如下：

- 在 Vivado 中新建工程 DispNumber_sch。
- 新建文件 DispNumber_sch.v。
- 添加 MyMC14495.v 到工程。
- 在 Vivado 上进行后续的仿真以及在实验板上验证。

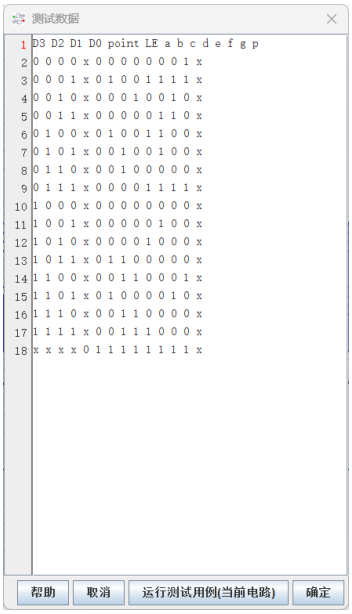
三、实验结果与分析

1. 原理图设计实现显示译码 MyMC14495 模块

按照真值表搭建的电路如图所示：



对该电路图进行正确性检验，结果如下（已加入预期结果）：

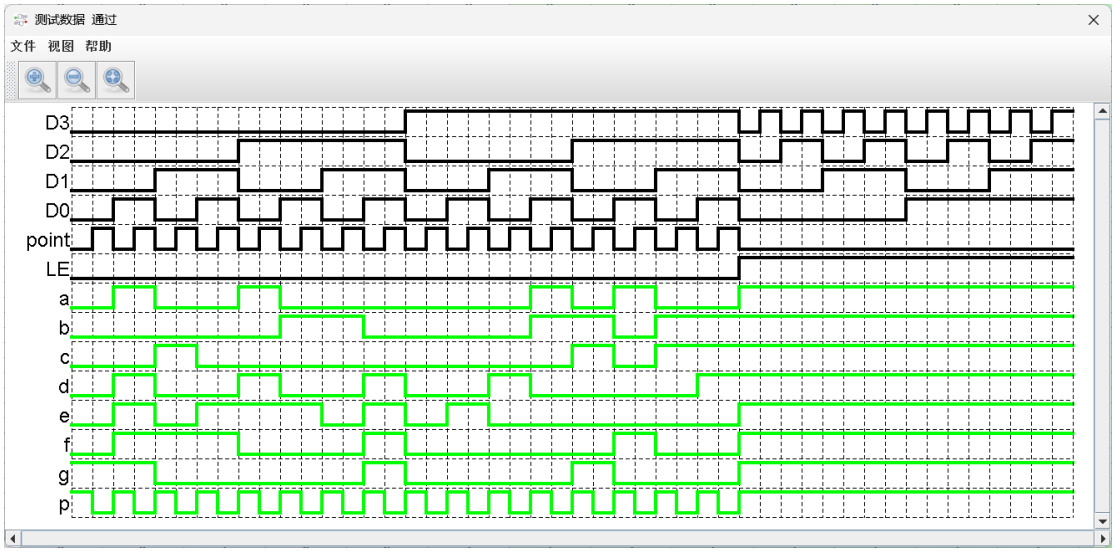


测试结果

文件 视图

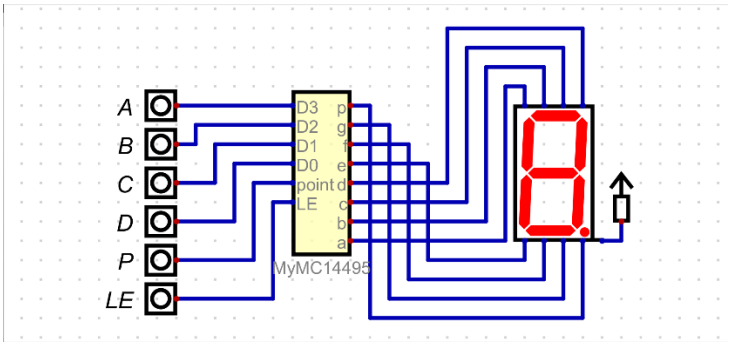
通过

	D3	D2	D1	D0	point	LE	a	b	c	d	e	f	g	p
L2;X=0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
L2;X=1	0	0	0	0	1	0	0	0	0	0	0	0	1	0
L3;X=0	0	0	0	1	0	0	1	0	0	1	1	1	1	1
L3;X=1	0	0	0	1	1	0	1	0	0	1	1	1	1	0
L4;X=0	0	0	1	0	0	0	0	0	1	0	0	1	0	1
L4;X=1	0	0	1	0	1	0	0	0	1	0	0	1	0	0
L5;X=0	0	0	1	1	0	0	0	0	0	0	1	1	0	1
L5;X=1	0	0	1	1	1	0	0	0	0	0	1	1	0	0
L6;X=0	0	1	0	0	0	0	1	0	0	1	1	0	0	1
L6;X=1	0	1	0	0	1	0	1	0	0	1	1	0	0	0
L7;X=0	0	1	0	1	0	0	0	1	0	0	1	0	0	1
L7;X=1	0	1	0	1	1	0	0	1	0	0	1	0	0	0
L8;X=0	0	1	1	0	0	0	0	1	0	0	0	0	0	1
L8;X=1	0	1	1	0	1	0	0	1	0	0	0	0	0	0
L9;X=0	0	1	1	1	0	0	0	0	0	1	1	1	1	1
L9;X=1	0	1	1	1	1	0	0	0	0	1	1	1	1	0
L10;X=0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
L10;X=1	1	0	0	0	1	0	0	0	0	0	0	0	0	0
L11;X=0	1	0	0	1	0	0	0	0	0	0	1	0	0	1
L11;X=1	1	0	0	1	1	0	0	0	0	0	1	0	0	0
L12;X=0	1	0	1	0	0	0	0	0	0	1	0	0	0	1
L12;X=1	1	0	1	0	1	0	0	0	0	1	0	0	0	0
L13;X=0	1	0	1	1	0	0	1	1	0	0	0	0	0	1
L13;X=1	1	0	1	1	1	0	1	1	0	0	0	0	0	0
L14;X=0	1	1	0	0	0	0	0	1	1	0	0	0	1	1
L14;X=1	1	1	0	0	1	0	0	1	1	0	0	0	1	0
L15;X=0	1	1	0	1	0	0	1	0	0	0	0	1	0	1
L15;X=1	1	1	0	1	1	0	1	0	0	0	0	1	0	0
L16;X=0	1	1	1	0	0	0	0	1	1	0	0	0	0	1
L16;X=1	1	1	1	0	1	0	0	1	1	0	0	0	0	0
L17;X=0	1	1	1	1	0	0	0	1	1	1	0	0	0	1
L17;X=1	1	1	1	1	1	0	0	1	1	1	0	0	0	0
L18;X=0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
L18;X=1	1	0	0	0	0	1	1	1	1	1	1	1	1	1
L18;X=2	0	1	0	0	0	1	1	1	1	1	1	1	1	1
L18;X=3	1	1	0	0	0	1	1	1	1	1	1	1	1	1
L18;X=4	0	0	1	0	0	1	1	1	1	1	1	1	1	1
L18;X=5	1	0	1	0	0	1	1	1	1	1	1	1	1	1
L18;X=6	0	1	1	0	0	1	1	1	1	1	1	1	1	1
L18;X=7	1	1	1	0	0	1	1	1	1	1	1	1	1	1
L18;X=8	0	0	0	1	0	1	1	1	1	1	1	1	1	1
L18;X=9	1	0	0	1	0	1	1	1	1	1	1	1	1	1
L18;X=10	0	1	0	1	0	1	1	1	1	1	1	1	1	1
L18;X=11	1	1	0	1	0	1	1	1	1	1	1	1	1	1
L18;X=12	0	0	1	1	0	1	1	1	1	1	1	1	1	1
L18;X=13	1	0	1	1	0	1	1	1	1	1	1	1	1	1
L18;X=14	0	1	1	1	0	1	1	1	1	1	1	1	1	1

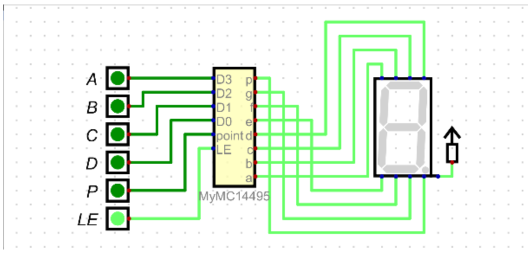


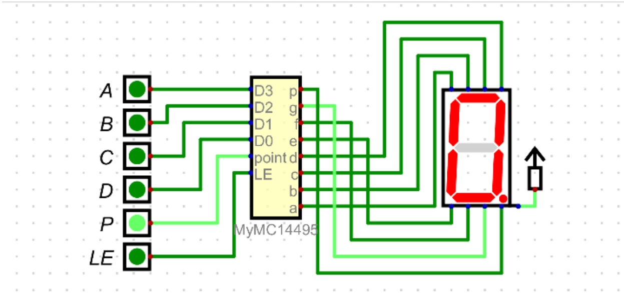
可以观察到这 48 组输出值均符合预期，即说明该电路无误。

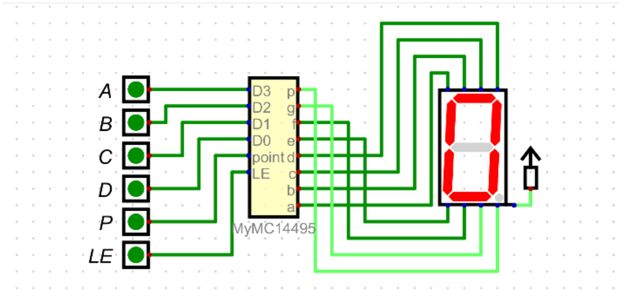
同时，也可以通过创建新的电路 MyMC14495_Test 进行验证，电路图如下：

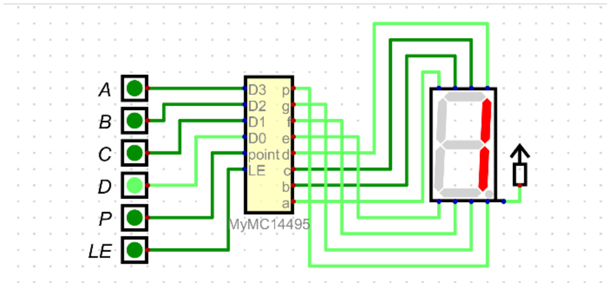


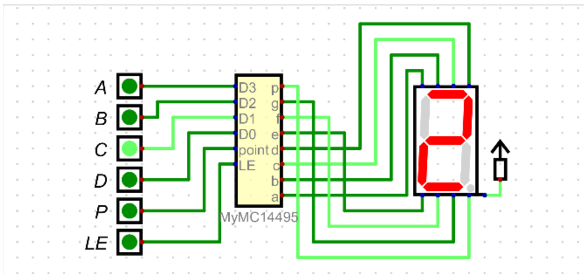
对其正确性进行进一步验证：

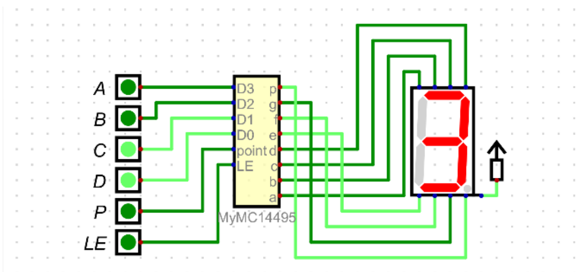


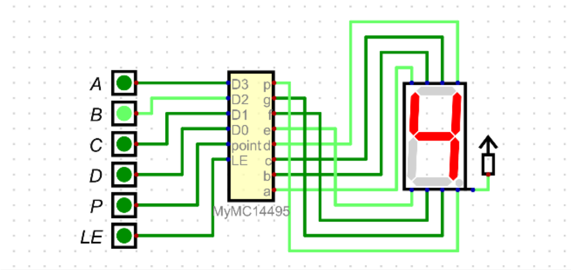











A
B
C
D
P
LE
D3
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D1
D0
point
LE
p
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f
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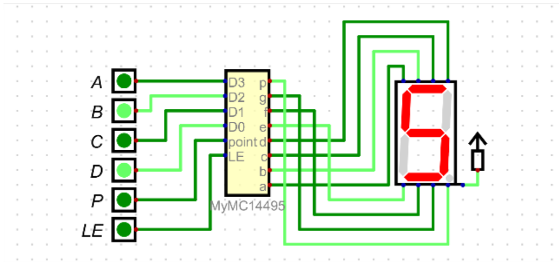
c
b
a
MyMC14495

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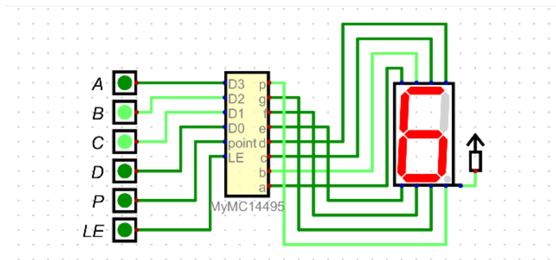
MyMC14495

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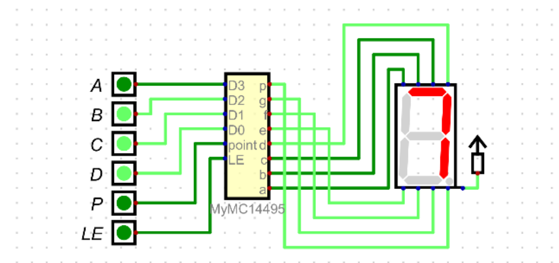
MyMC14495

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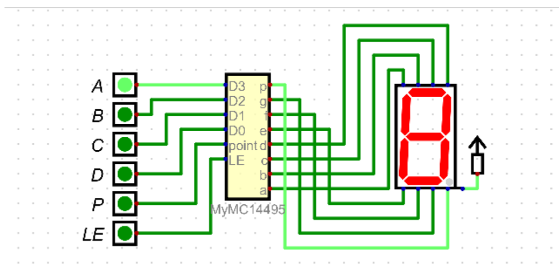
MyMC14495

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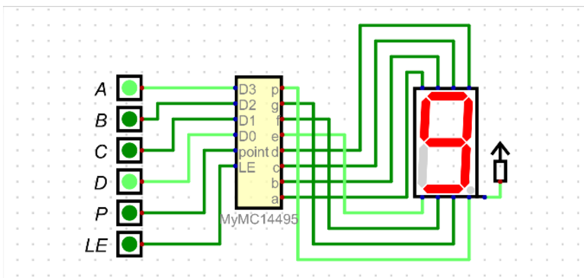
MyMC14495

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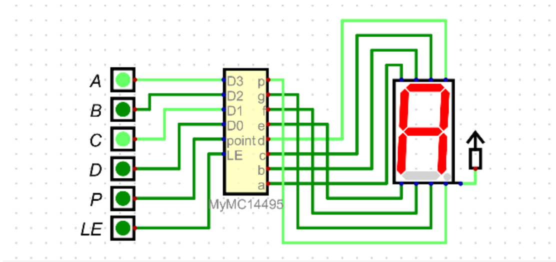
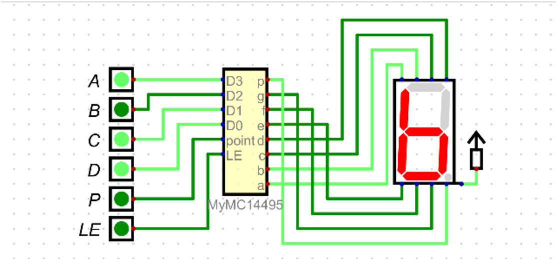
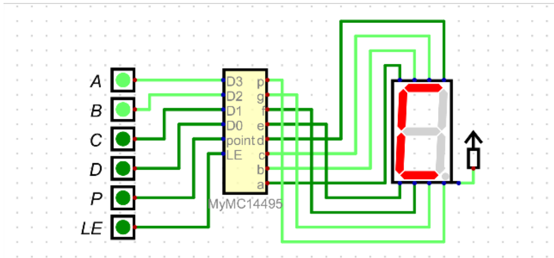
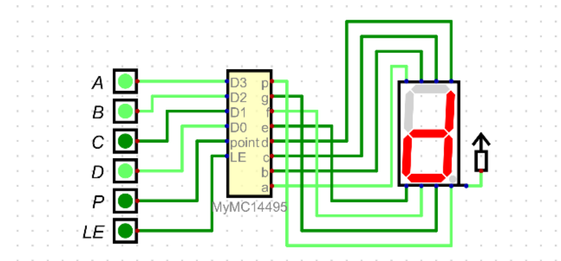
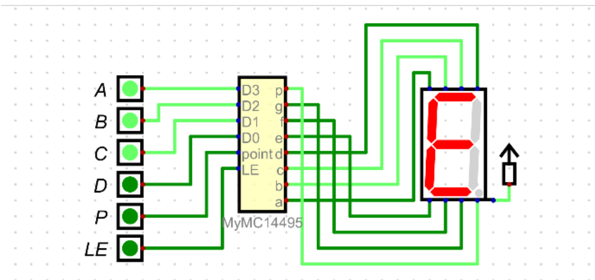
MyMC14495

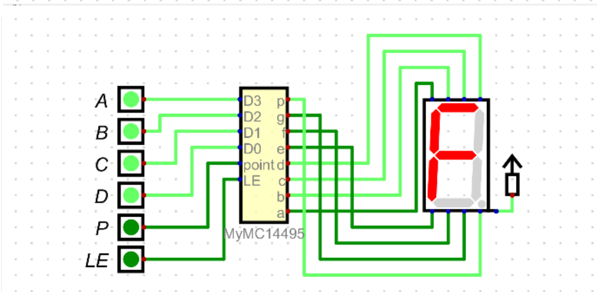












观察到这 19 张测试结构均符合预期，进一步证明该电路无误。

此时将 MyMC14495 电路图导出为 Verilog 代码：

```
/*
 * Generated by Digital. Don't modify this file!
 * Any changes will be lost if this file is regenerated.
 */

module MyMC14495 (
  input D3,
  input D2,
  input D1,
  input D0,
  input point,
  input LE,
  output p,
  output g,
  output f,
  output e,
  output d,
  output c,
  output b,
  output a
);
  wire s0;
  wire s1;
  wire s2;
  wire s3;
  assign s0 = ~ D3;
  assign s1 = ~ D2;
  assign s2 = ~ D1;
  assign s3 = ~ D0;
  assign p = ~ point;
  assign g = (((s2 & s1 & s0) | (D0 & D1 & D2 & s0) | (s3 & s2 & D2 &
D3)) | LE);
  assign f = (((D0 & s1 & s0) | (D1 & s1 & s0) | (D0 & D1 & s0) | (D0 &
s2 & D2 & D3)) | LE);
  assign e = (((D0 & s0) | (s2 & D2 & s0) | (D0 & s2 & s1)) | LE);
  assign d = (((D0 & s2 & s1 & s0) | (s3 & s2 & D2 & s0) | (D0 & D1 &
D2) | (s3 & D1 & s1 & D3)) | LE);
  assign c = (((s3 & D1 & s1 & s0) | (s3 & D2 & D3) | (D1 & D2 & D3)) |
LE);
  assign b = (((D0 & s2 & D2 & s0) | (s3 & D1 & D2) | (s3 & D2 & D3) |
(D0 & D1 & D3)) | LE);
  assign a = (((D0 & s2 & s1 & s0) | (s3 & s2 & D2 & s0) | (D0 & D1 & s1
& D3) | (D0 & s2 & D2 & D3)) | LE);
endmodule
```

2. 用 MyMC14495 模块实现数码管显示

根据任务要求，编写 DispNumber_sch.v,MyMC14495_testbench,约束文件：

DispNumber_sch.v：

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 2025/03/26 12:47:46
// Design Name:
// Module Name: DispNumber_sch
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module DispNumber_sch(
    input [15:0]SW,
    output [7:0]SEGMENT,
    output [3:0]AN
    );

    assign AN[3:0] = SW[7:4];
    MyMC14495 s0(.D3(SW[3]), .D2(SW[2]),  .D1(SW[1]), .D0(SW[0]),
                .point(SW[15]), .LE(SW[14]),
                .a(SEGMENT[0]),
                .b(SEGMENT[1]),
                .c(SEGMENT[2]),
                .d(SEGMENT[3]),
                .e(SEGMENT[4]),
                .f(SEGMENT[5]),
                .g(SEGMENT[6]),
                .p(SEGMENT[7]));
```

```
endmodule
```

MyMC14495_testbench.v:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
//////////
// Company:
// Engineer:
//
// Create Date: 2025/03/26 12:49:21
// Design Name:
// Module Name: MyMC14495_testbench
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
//////////


module MyMC14495_testbench();
  reg D3;
  reg D2;
  reg D1;
  reg D0;
  reg point;
  reg LE;
  wire p;
  wire g;
  wire f;
  wire e;
  wire d;
  wire c;
  wire b;
  wire a;
  MyMC14495 MyMC14495_UUT(
  .D3(D3),
  .D2(D2),
```

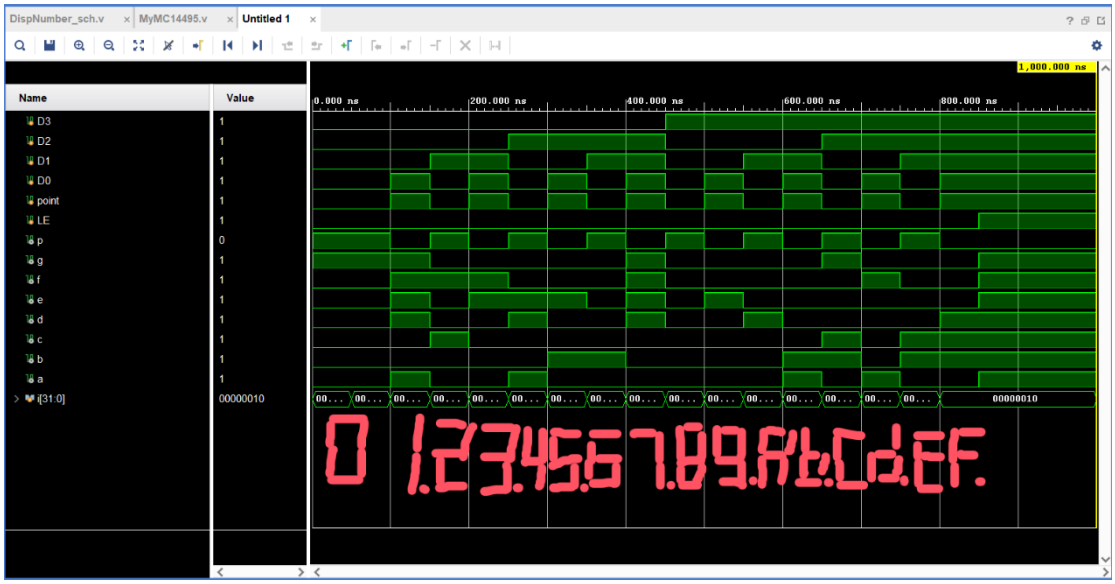
```
  .D1(D1),
  .D0(D0),
  .point(point),
  .LE(LE),
  .p(p),
  .g(g),
  .f(f),
  .e(e),
  .d(d),
  .c(c),
  .b(b),
  .a(a)
  );
integer i;
initial begin
  D3 = 0;
  D2 = 0;
  D1 = 0;
  D0 = 0;
  LE = 0;
  point = 0;
  for (i=0; i<=15;i=i+1) begin
    #50;
    {D3, D2, D1, D0}=i;
    point = i;
  end

  #50;
  LE = 1;
end
endmodule
```

约束文件：

```
set_property PACKAGE_PIN AA10 [get_ports {SW[0]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[0]}]
set_property PACKAGE_PIN AB10 [get_ports {SW[1]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[1]}]
set_property PACKAGE_PIN AA13 [get_ports {SW[2]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[2]}]
set_property PACKAGE_PIN AA12 [get_ports {SW[3]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[3]}]
set_property PACKAGE_PIN Y13 [get_ports {SW[4]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[4]}]
set_property PACKAGE_PIN Y12 [get_ports {SW[5]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[5]}]
set_property PACKAGE_PIN AD11 [get_ports {SW[6]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[6]}]
set_property PACKAGE_PIN AD10 [get_ports {SW[7]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[7]}]
set_property PACKAGE_PIN AE10 [get_ports {SW[8]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[8]}]
set_property PACKAGE_PIN AE12 [get_ports {SW[9]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[9]}]
set_property PACKAGE_PIN AF12 [get_ports {SW[10]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[10]}]
set_property PACKAGE_PIN AE8 [get_ports {SW[11]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[11]}]
set_property PACKAGE_PIN AF8 [get_ports {SW[12]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[12]}]
set_property PACKAGE_PIN AE13 [get_ports {SW[13]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[13]}]
set_property PACKAGE_PIN AF13 [get_ports {SW[14]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[14]}]
set_property PACKAGE_PIN AF10 [get_ports {SW[15]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[15]}]
```

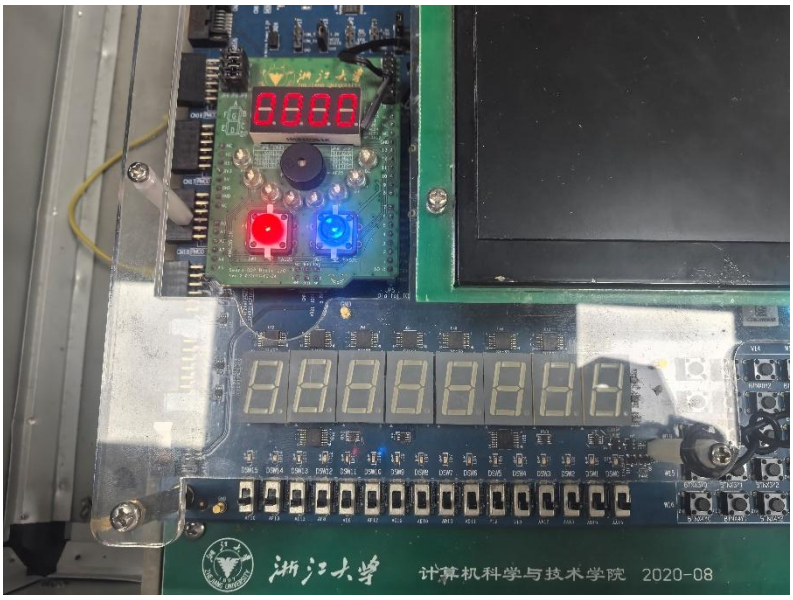
```
set_property PACKAGE_PIN AB22 [get_ports {SEGMENT[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {SEGMENT[0]}]
set_property PACKAGE_PIN AD24 [get_ports {SEGMENT[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {SEGMENT[1]}]
set_property PACKAGE_PIN AD23 [get_ports {SEGMENT[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {SEGMENT[2]}]
set_property PACKAGE_PIN Y21 [get_ports {SEGMENT[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {SEGMENT[3]}]
set_property PACKAGE_PIN W20 [get_ports {SEGMENT[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {SEGMENT[4]}]
set_property PACKAGE_PIN AC24 [get_ports {SEGMENT[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {SEGMENT[5]}]
set_property PACKAGE_PIN AC23 [get_ports {SEGMENT[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {SEGMENT[6]}]
set_property PACKAGE_PIN AA22 [get_ports {SEGMENT[7]}]
set_property IOSTANDARD LVCMOS33 [get_ports {SEGMENT[7]}]
set_property PACKAGE_PIN AD21 [get_ports {AN[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {AN[0]}]
set_property PACKAGE_PIN AC21 [get_ports {AN[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {AN[1]}]
set_property PACKAGE_PIN AB21 [get_ports {AN[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {AN[2]}]
set_property PACKAGE_PIN AC22 [get_ports {AN[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {AN[3]}]
```

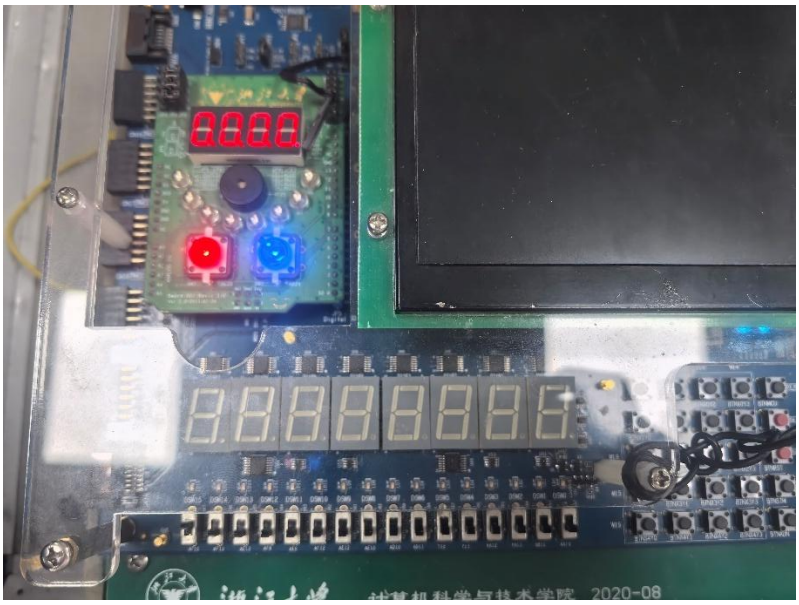
Vivado 平台上的仿真实验如下（已对结果进行标注）：

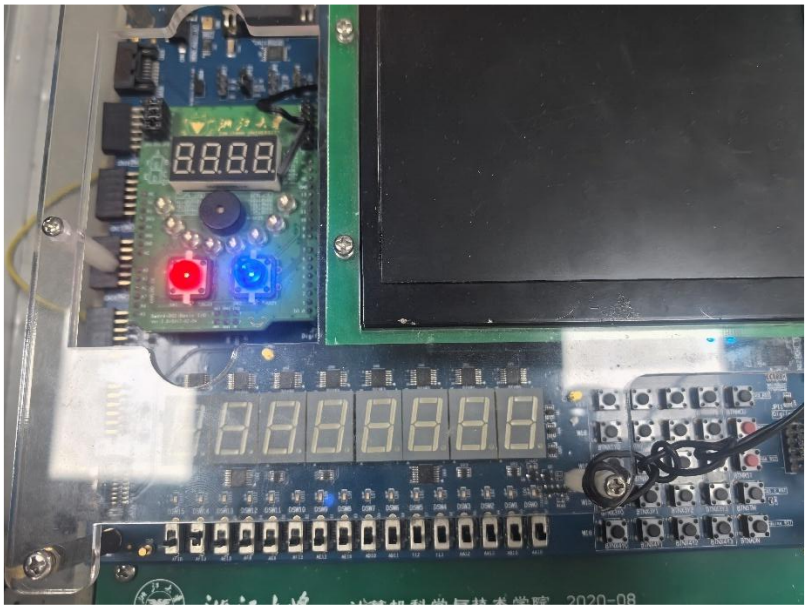


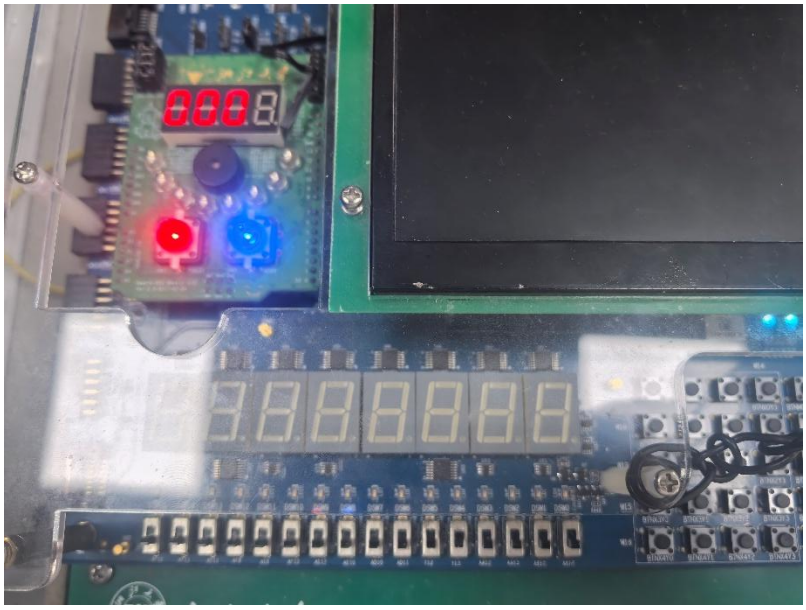
可以看到，仿真实验的结果与前两次 Digital 上验证的结果均一致。

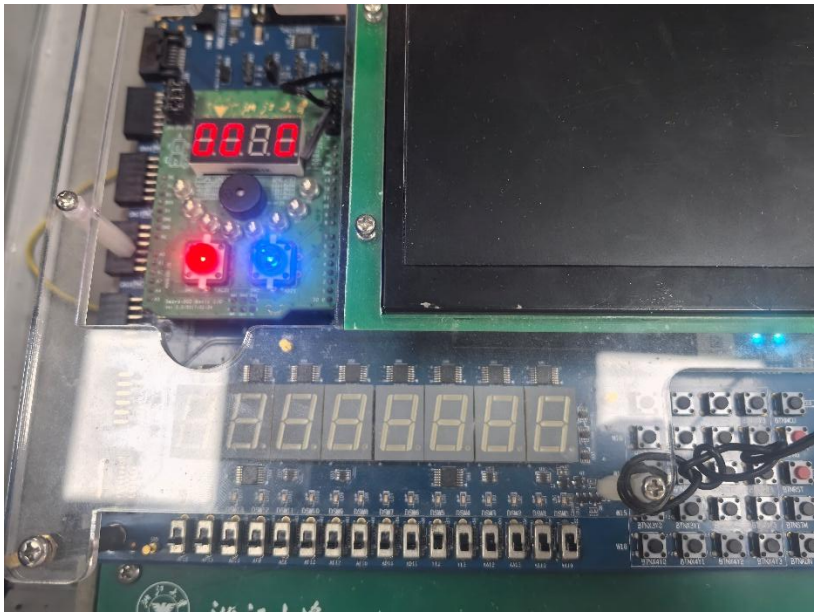
实验板上验证结果为：当 SW[15]闭合时，显示小数点；当 SW[14]闭合时，所有数字均熄灭；SW[4]~SW[7]中有开关闭合时，其对应的数字熄灭；SW[0]~SW[3]则对应控制从最低位至最高位，且结果与先前的实验均一致，实验照片如下：

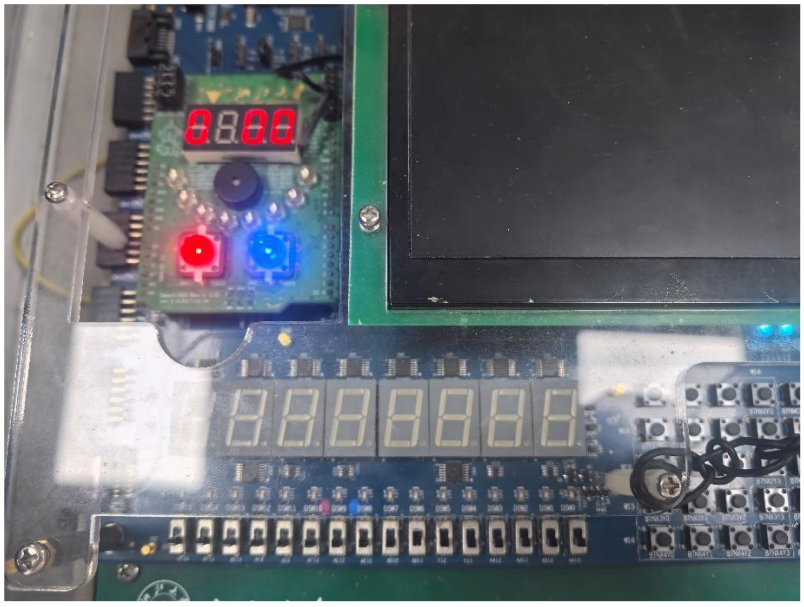

浙江大学
计算机科学与技术学院 2020-08

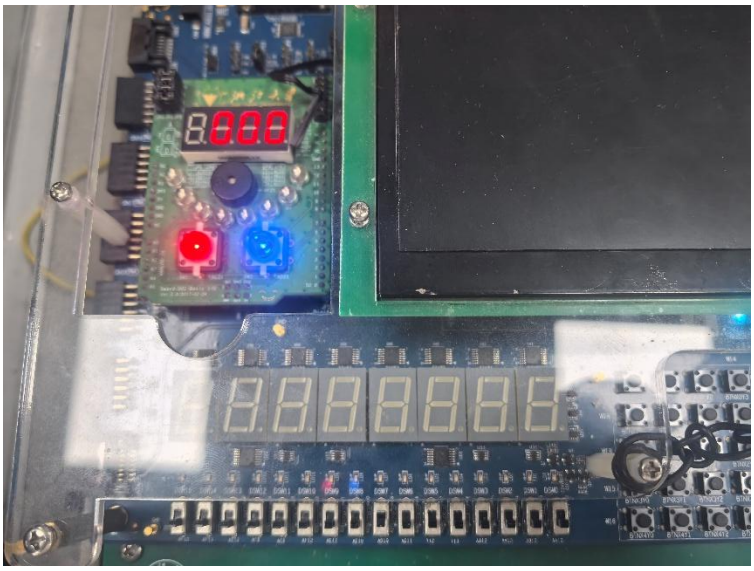

浙江大学
计算机科学与技术学院 2020-08

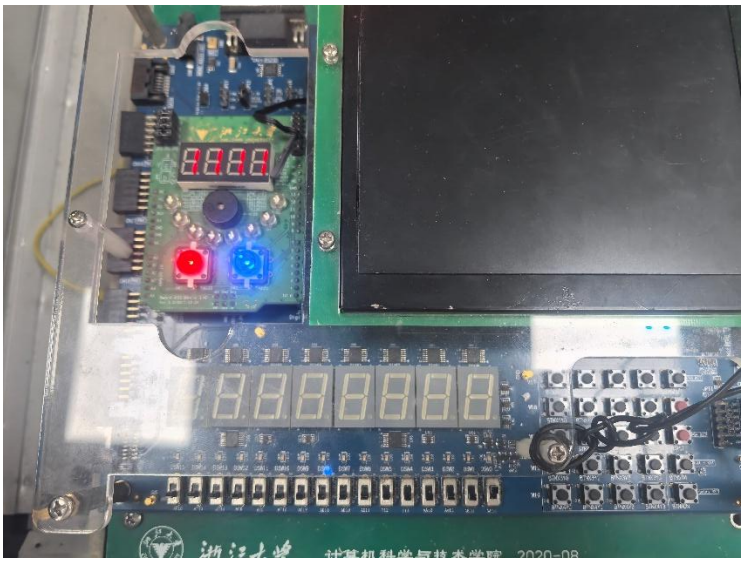

浙江大学
计算机科学与技术学院 2020-08

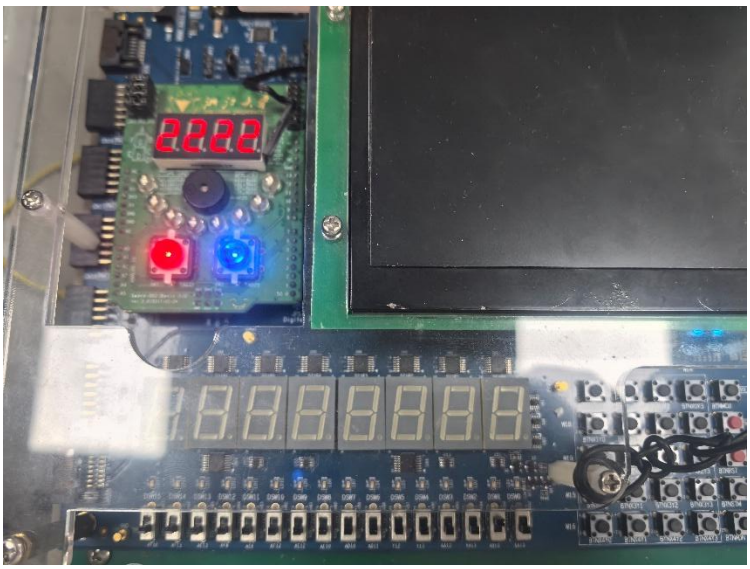


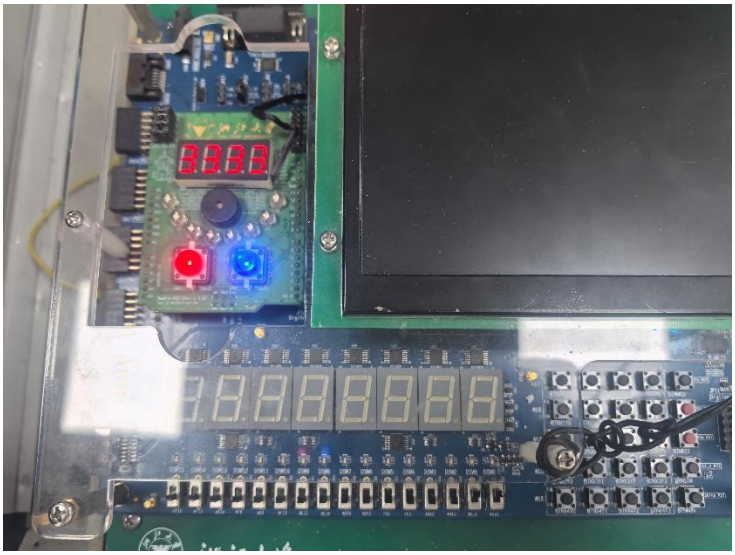


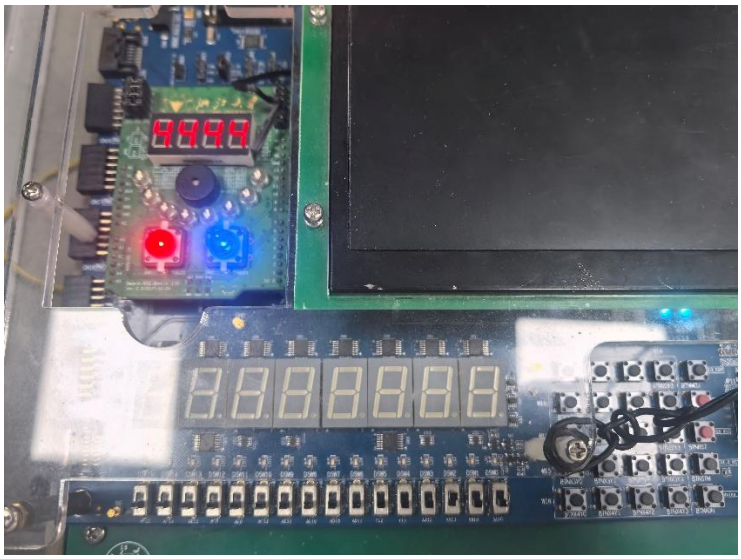


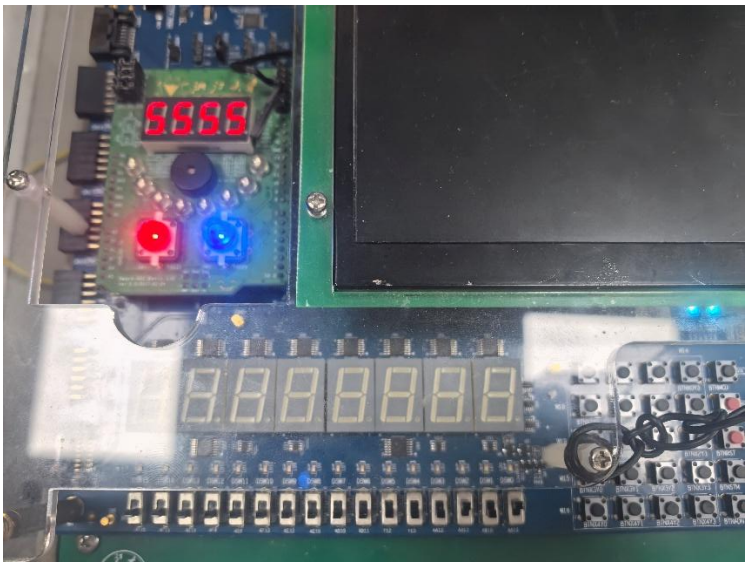


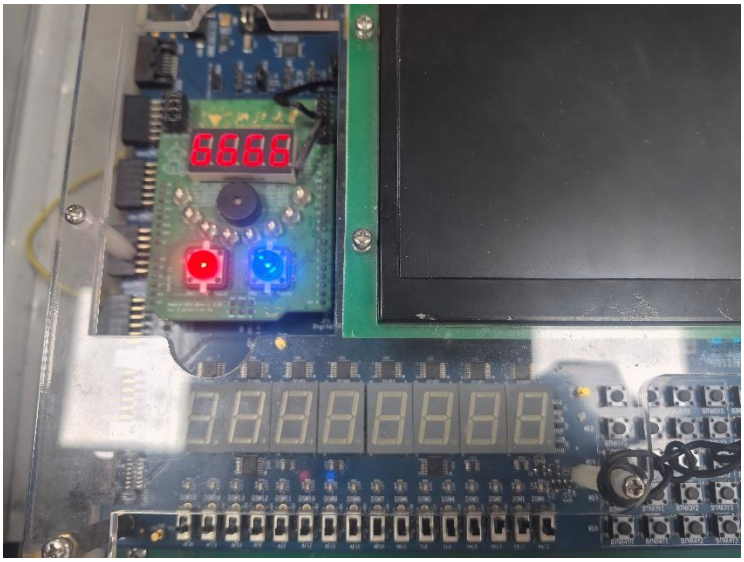


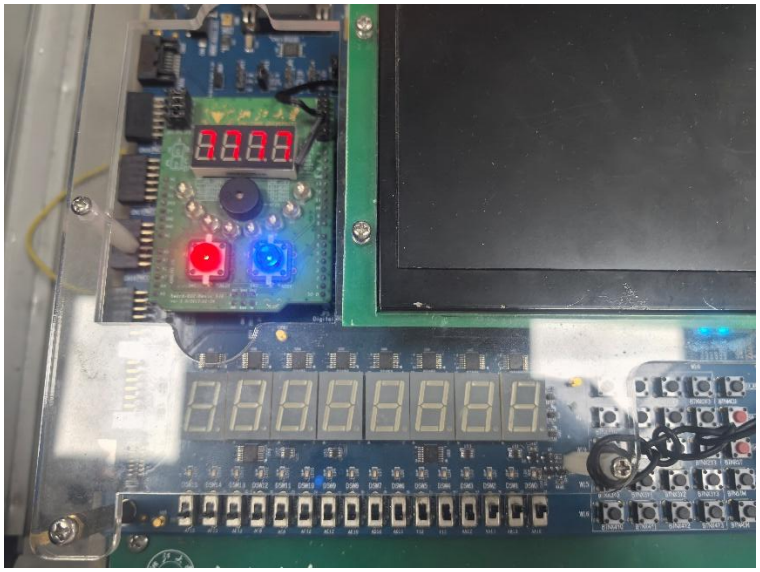


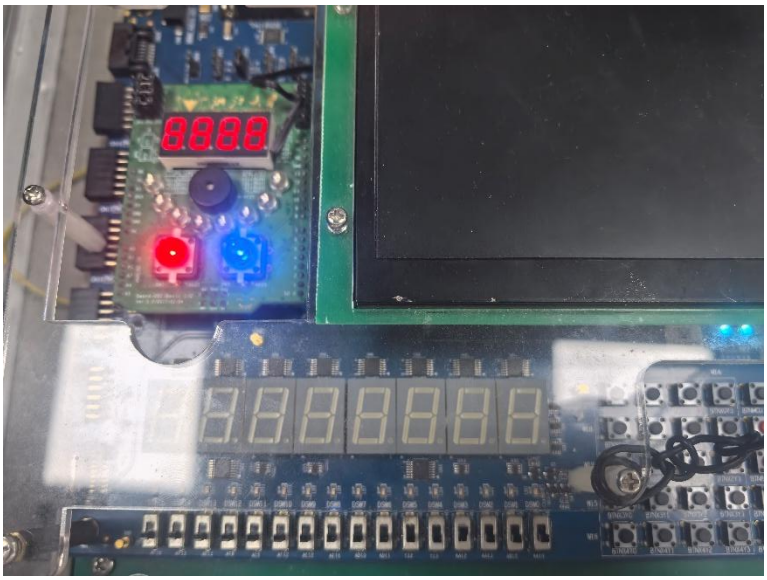


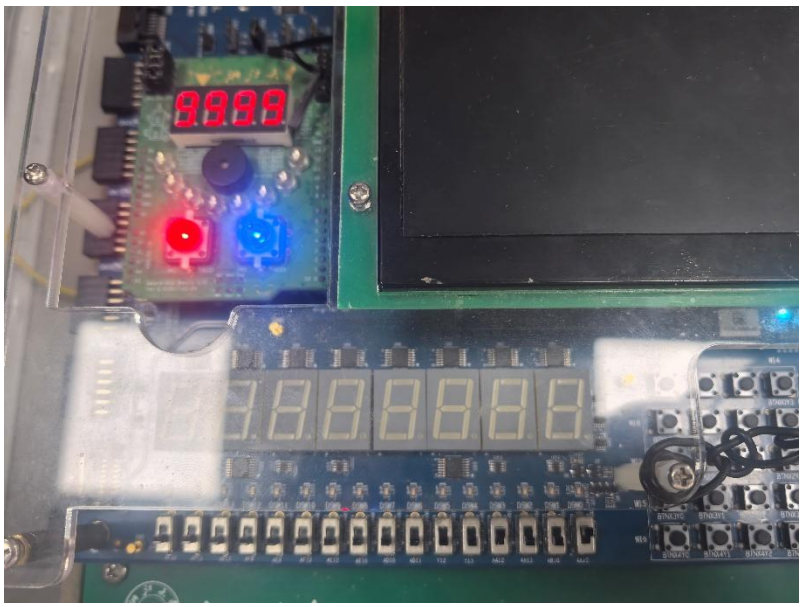








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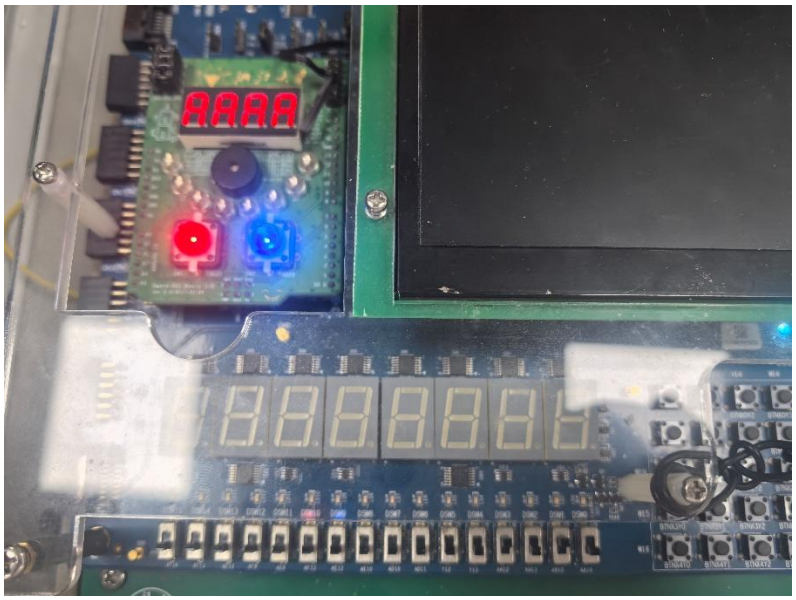
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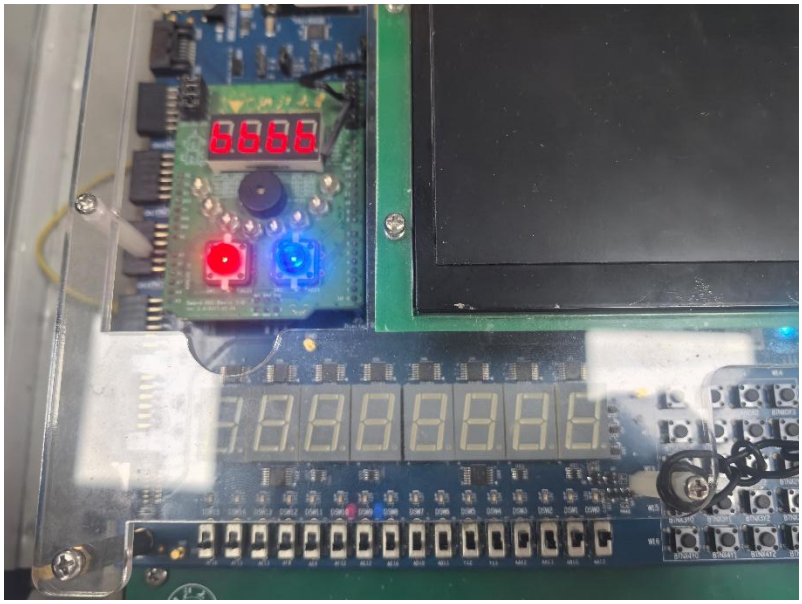
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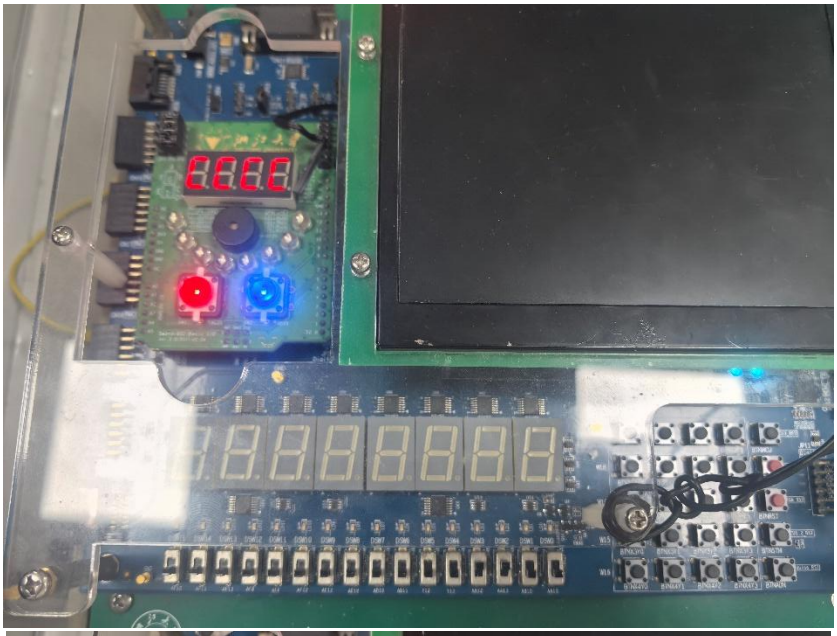

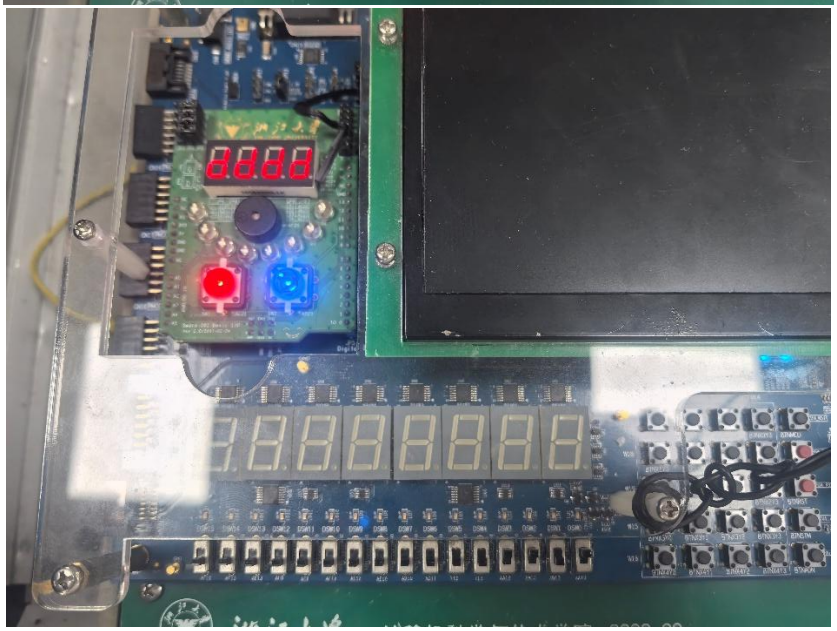

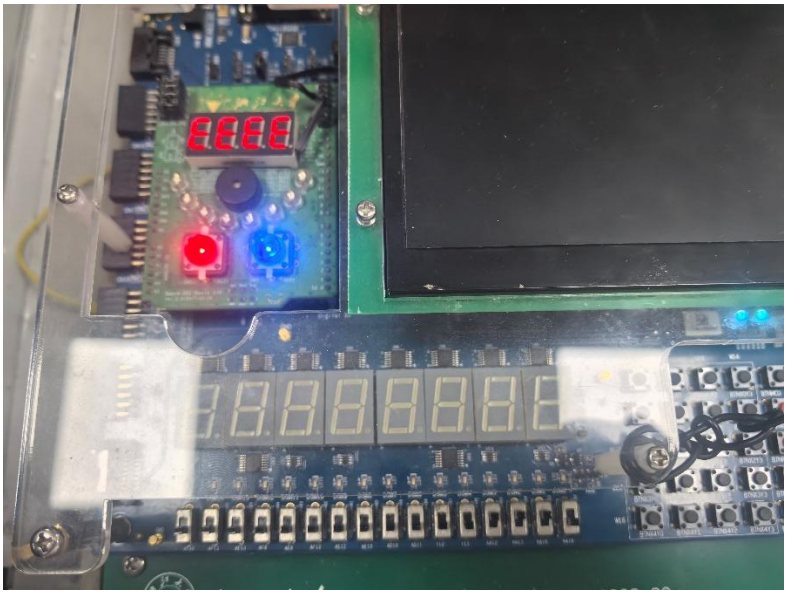

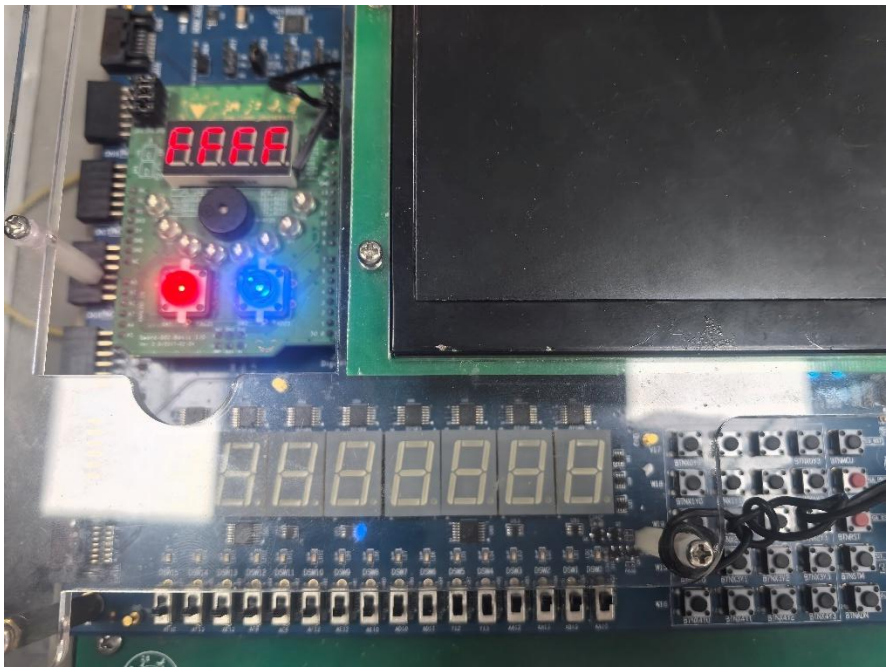

四、讨论、心得

通过这一次实验，我对 Digital 软件和 Vivado 平台的熟悉程度进一步加深，也学会了七段数码管电路的绘制，同时也对 verilog 以及约束文件的语法有了更加深刻的了解。