Lab 1: Software Installation

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I – Introduction

AMD's FPGA creation suite, Vivado, improves the process of how hardware and digital designers created their embedded projects. The suite is complete with standard integrated development features such as debugging, console, and timing analysis tools.

We were encouraged to gain familiarity and proficiency in the simplest functions within Vivado throughout this exercise and I documented the results.

II – Screenshots:

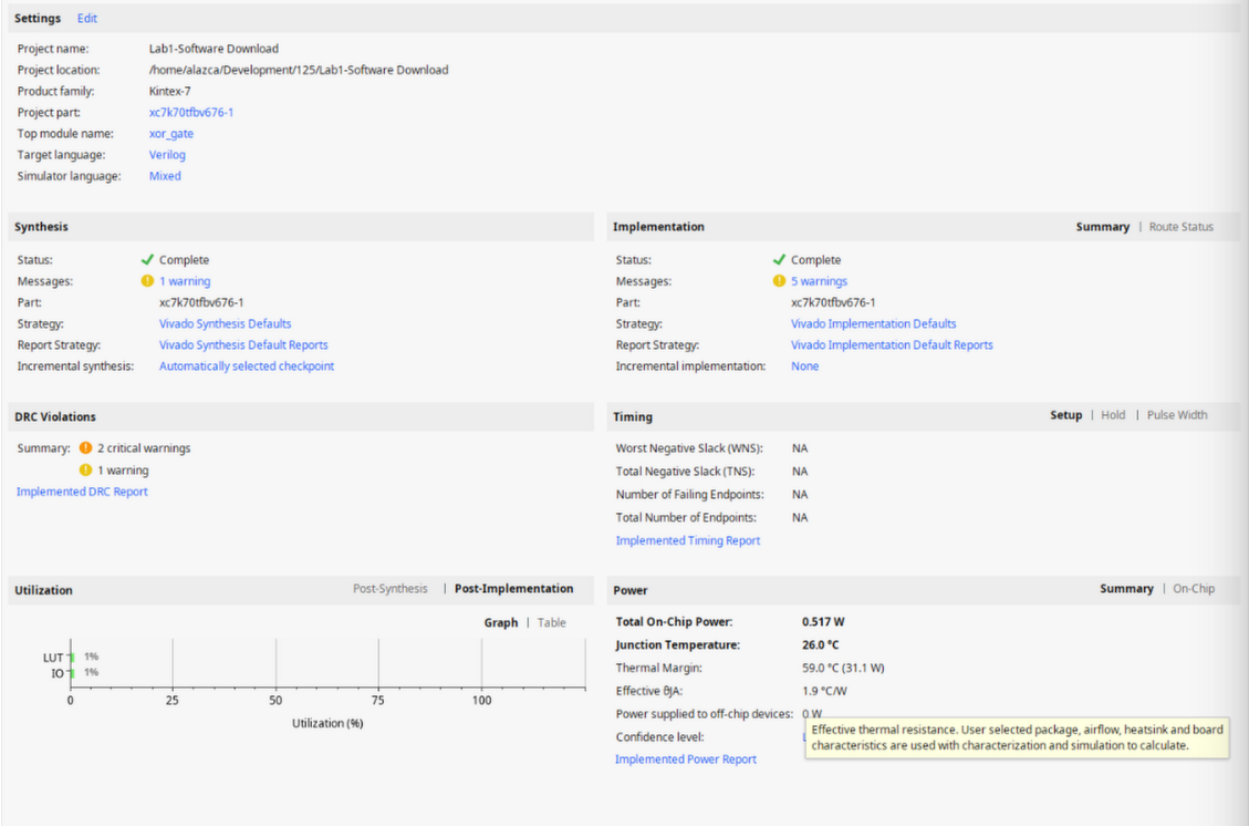


Figure 1: Screenshot of the completed synthesis and implementation summary.

```
// Gate level modeling
module xor_gate(c,a,b);
input a,b;
output c;
xor(c,a,b);
endmodule

// Data flow modeling
module xor_gate_bm(c,a,b);
input a,b;
output c;
assign x = (a & ~b) | (~a & b);
endmodule
```

Figure 2: Copy of the sample code provided, alongside the gate-level modeling of the XOR gate.

```
module xor_gatetb();
reg a,b;
wire c;
xor_gate xor_test(c,a,b);
initial
begin
#00 a = 0; b = 0;
#10 a = 0; b = 1;
#10 a = 1; b = 0;
#10 a = 1; b = 1;
end
initial
begin
$monitor($time, "a=%b,b=%b, c=%b", a,b,c);
end
endmodule
```

Figure 3: Copy of the testbench Verilog code.

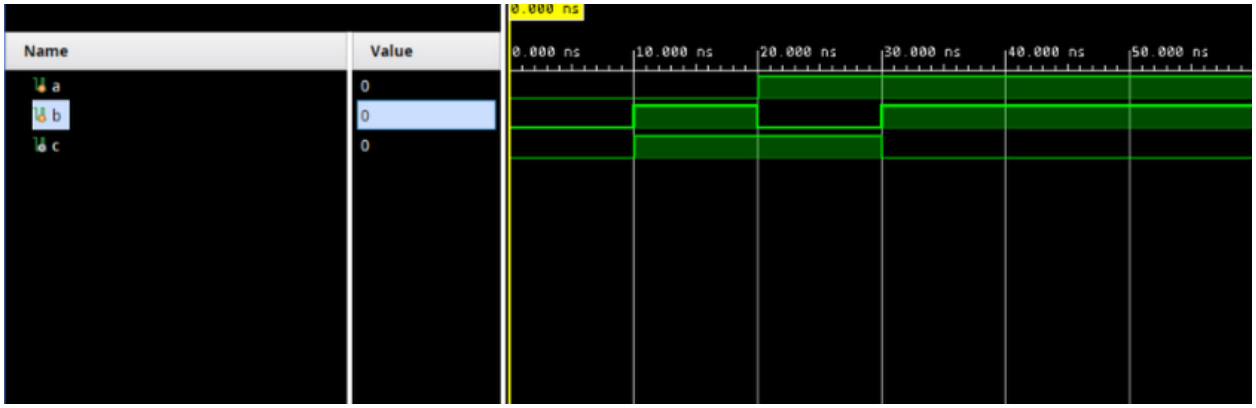


Figure 4: Sample of the output waveform. As can be observed, output C is high only when either A or B is 1 and low when A and B are the same value.

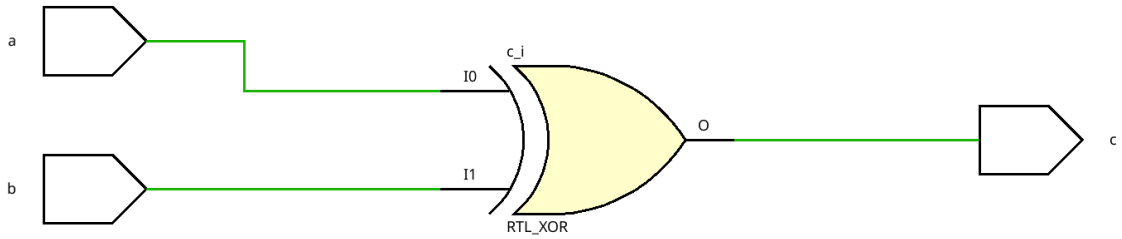


Figure 5: Schematic of the Xor gate.

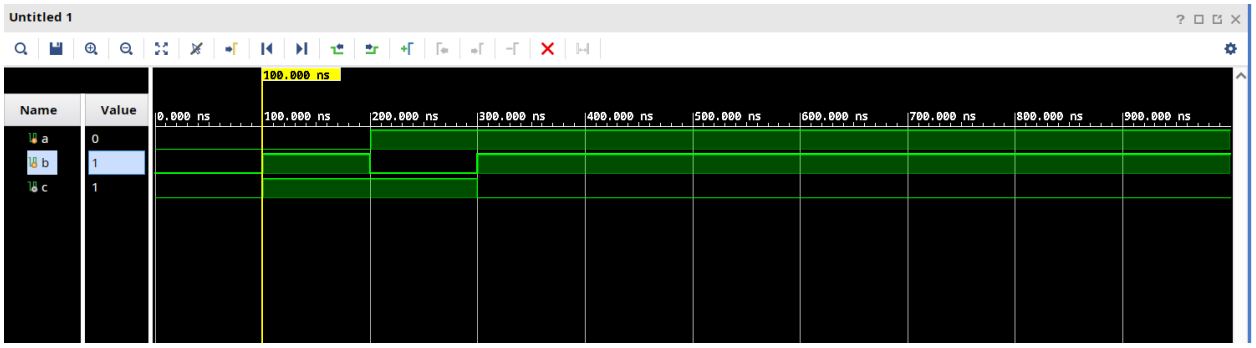
III – Verification Summary

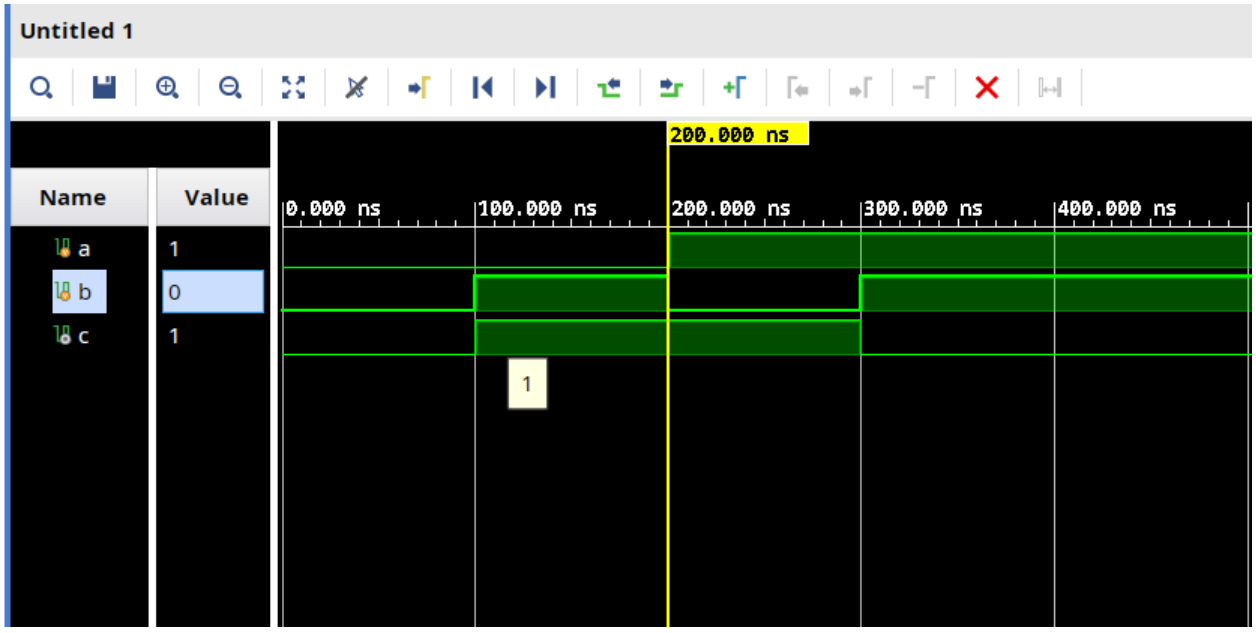
The intended waveform matches the testbench. Due to simplicity, I used 10ns for the testing. As indicated in **Figure 4**, output C is 1 at every instance of either A or B being 1 and is 0 for each instance A and B are the same value.

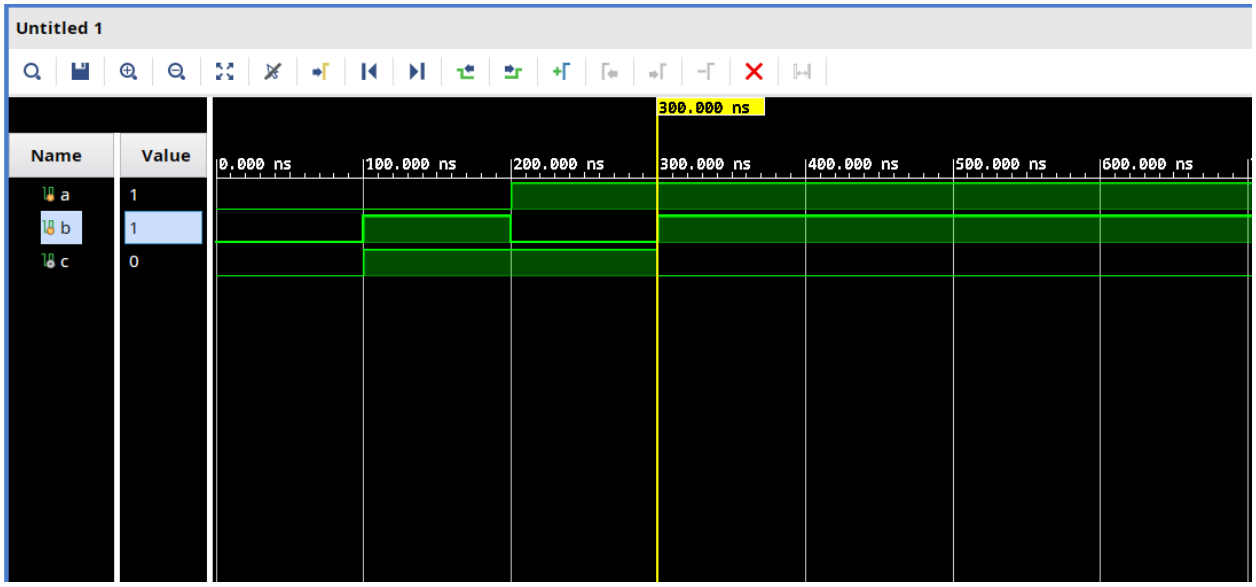
IV – Enclosures

See attached enclosures in zip file.

Screenshot of Waveforms:






Untitled 1
Name
Value
a
1
b
1
c
0
300.000 ns
0.000 ns
100.000 ns
200.000 ns
300.000 ns
400.000 ns
500.000 ns
600.000 ns