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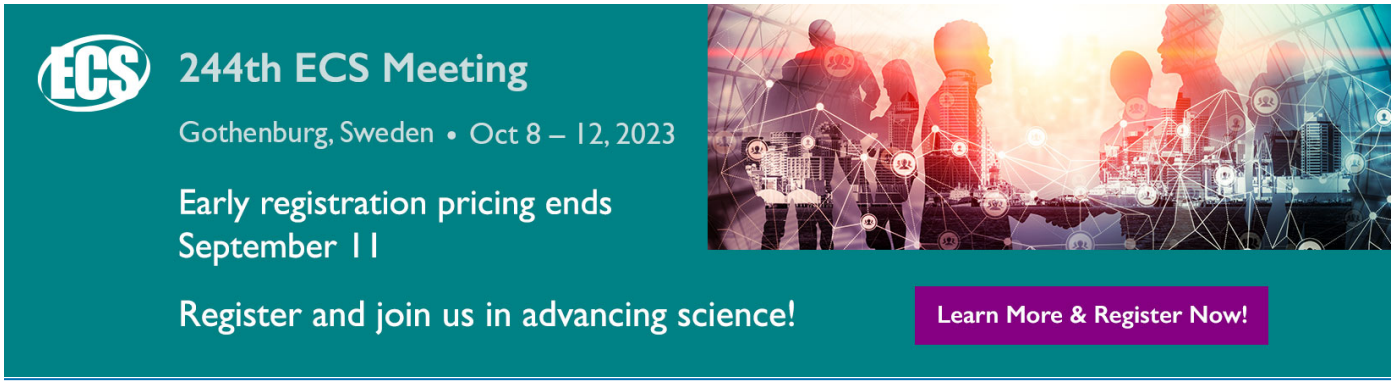

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The upgrade of the PreProcessor system of the ATLAS level-1 calorimeter trigger

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ABSTRACT: The ATLAS Level-1 Calorimeter Trigger is a pipelined system to identify high-p_T objects and to build energy sums within a fixed latency of $\sim 2\,\mu$s. It consists of a PreProcessor, which conditions and digitises analogue calorimeter signals, and two object-finding processors. The PreProcessor's tasks are implemented on a Multi-Chip Module, holding ADCs, time-adjustment and digital processing ASICs, and LVDS serialisers. A pin-compatible substitute, based on today's technology, like dual-channel ADCs and FPGAs, has been built to improve the BCID and pedestal subtraction algorithms. Test results with the first prototype are presented.

KEYWORDS: Digital signal processing (DSP); Trigger algorithms; Modular electronics; Digital electronic circuits

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1 Introduction

The Large Hadron Collider (LHC) is designed to collide bunches of protons at a centre-of-mass energy of 14 TeV and a luminosity of $10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. With bunches colliding every 25 ns at its centre, the ATLAS detector [1] produces ~ 1 PByte of raw data every second, while the event data recording is limited by technology and resources to ~ 300 MByte/s. The task of the ATLAS Trigger system is to reduce the event data rate from the input bunch-crossing rate of 40.08 MHz down to the more affordable storage rate of ~ 200 Hz, while efficiently selecting interesting physics events.

In order to achieve this, the ATLAS Trigger system is organised into three levels of successive event selection: Level-1 (L1), Level-2 (L2) and Event Filter (EF). The L1 trigger is entirely implemented in hardware, and it uses coarse granularity calorimeter data and dedicated muons chambers to reduce the 40 MHz bunch-crossing rate to about 75 kHz (upgradeable to 100 kHz). The L2 and EF triggers are software-based systems, running on large commercial computer farms, and have access to the full-granularity and full-precision calorimeter and muon detector data, as well as to the tracking data, to further reduce the event data rate down to the imposed storage limit.

The L1 trigger consists of three main subsystems: a Calorimeter Trigger (L1Calo), a Muon Trigger (L1Muon) and a Central Trigger Processor (CTP), which combines the results of the other two subsystems to reach a final L1 trigger decision with respect to each event.

The L1Calo [2] system is a hardware-based, pipelined system designed to identify high-p_T objects in the electromagnetic and hadronic calorimeters of the ATLAS detector. The system receives and processes 7168 pre-summed analogue signals from the entire ATLAS calorimetry, and provides results to the CTP within 2 μs after the proton-proton collision has occurred. The L1Calo system is itself composed of three subsystems: the PreProcessor (PPr), the Cluster Processor (CP) and the Jet/Energy-sum Processor (JEP) (see figure 1). The PreProcessor receives, conditions and digitises all the 7168 analogue signals, extracts a corresponding digital transverse energy (E_T) value from each pulse and identifies it with a specific bunch-crossing, and sends the results in parallel to the subsequent processors. The CP identifies isolated clusters of electrons, photons, taus and hadrons, while the JEP identifies jet objects and computes global sums of total and missing E_T, as well as

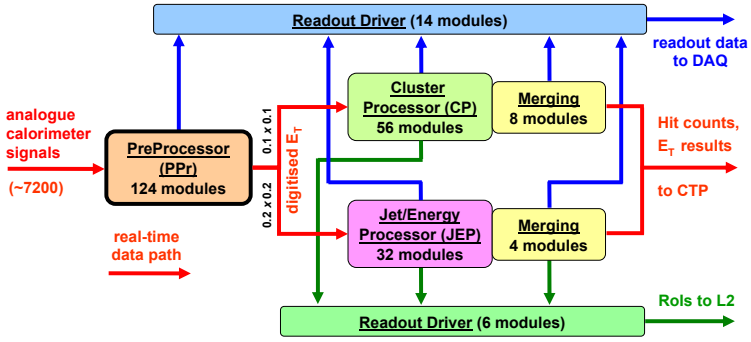

Figure 1. Schematic representation of the ATLAS Level-1 Calorimeter Trigger system.

the total E_T of the jet candidates. The results of these investigations are sent to the CTP in form of multiplicity of objects passing predefined thresholds for the final L1 trigger decision. If this is positive, then the L1Calo subsystems transmit event related data to the ATLAS Data Acquisition (DAQ) system, and Region-of-Interest (RoI) information to the L2 trigger, via dedicated Readout Driver (ROD) modules. The event data consists of digital E_T values and processing results, to allow the verification and the monitoring of the trigger operation, while the RoI includes the type and the location of the identified objects and the computed energy sums.

2 The PreProcessor system

The PreProcessor is a compact, highly modular system, consisting of 124 hardware-identical PreProcessor Modules (PPMs) which are organised into eight 9U VME crates. Each PPM is designed to process 64 input analogue signals, and carries 23 daughterboards and several programmable devices (see figure 2). The input analogue signals, also referred to as trigger-tower signals, correspond to E_T deposits in multiple calorimeter cells. They are formed by analogue summation in the front-end electronics of the calorimeters, and have amplitudes up to 2.5 V and a typical granularity of 0.1×0.1 in pseudorapidity (η) and azimuthal angle (ϕ) coordinates.

The trigger-tower signals are driven differentially from detector to the input of the PreProcessor, over long cables of variable length (30 m to 70 m). On the PPM, four 16-channel Analogue Input (PPrAnIn) daughterboards receive the differential signals, convert them to single-ended form, and re-scale them to match the 1 V digitisation window by applying a fixed gain factor and a programmable pedestal. The conditioned signals are then routed to 16 four-channel Multi-Chip Modules (PPrMCMs), which digitise the inputs, extract a corresponding E_T from each pulse and assign this value to a specific bunch-crossing. The digital E_T results are then serialised and sent in real-time as LVDS signals to the L1Calo processors, via an LVDS Cable Driver (LCD) daughtercard. In order to allow the verification of the L1 trigger decision and of the operation of the L1Calo subsystems, the PPMs provide real-time digital values related to the accepted event to the DAQ system. The event data is accumulated on the PPrMCMs, and transferred to the DAQ via a Field Programmable Gate Array (FPGA) device called the Readout Manager FPGA (ReM_FPGA). The configuration and control of the PPM is realised via a standard VME interface. The task to transfer data from the VME controller to all on-board programmable locations is assigned to a dedicated

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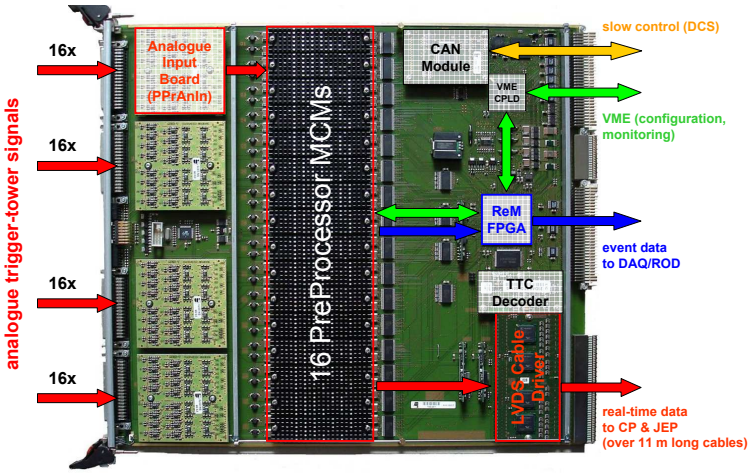

Figure 2. The PreProcessor Module.

Complex Programmable Logic Device (VME_CPLD) and to the same ReM_FPGA. Additionally, the ReM_FPGA has the task to collect and provide monitoring data to VME. This data is accumulated continuously on the PPrMCMs, and it consists of channel-wise and trigger independent energy rates and spectra.

2.1 The PreProcessor Multi-chip Module

The main signal processing is performed on the 16 PPrMCMs. Each PPrMCM carries nine unpackaged dies (see figure 3): four single-channel Analogue-to-Digital Converters (ADCs), one PHOS4 timing chip, one custom-built four-channel Application-Specific Integrated Circuit (PPrASIC), and three LVDS serialiser chips.

The ADCs digitise the input single-ended signals with 10-bit resolution at the LHC bunch-crossing frequency of 40.08 MHz. The four digitisation strobes are provided by the PHOS4 chip. The device allows to delay each strobe separately with respect to the LHC clock, in steps of 1 ns up to one LHC clock period (i.e. 25 ns), in order to sample the input signals at their maximum amplitude, and thus to improve the energy resolution. The resulting digital pulses are then sent to the PPrASIC which performs the main trigger-specific data processing:

- coarse synchronisation of pulses originating from the same collision, to compensate for the different time-of-flight of particles from the interaction point to the calorimeters, and for the different length of the signal paths from the calorimeters to the PreProcessor;
- measurement of signal E_T and identification of the corresponding bunch-crossing in time, by using FIR Filter and PeakFinder algorithms for pulses in linear range, and dedicated algorithms for saturated pulses;
- noise suppression, pedestal subtraction and fine-calibration of the extracted E_T values, by means of a Look-Up table (LUT);
- multiplexing of the E_T results from two trigger channels adjacent in ϕ into one serial stream, to better utilise the high-speed bandwidth to the CP system;

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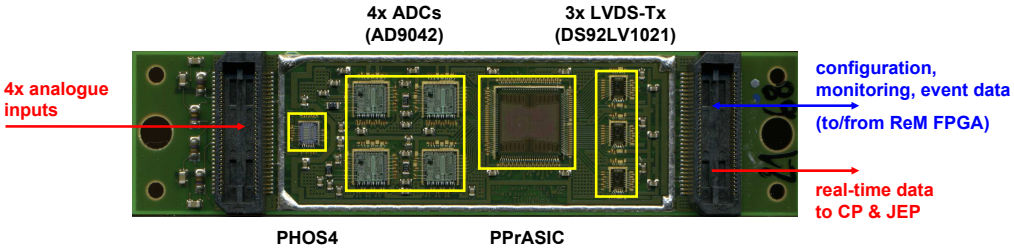

Figure 3. Front view of the PreProcessor Multi-Chip Module without glob-topping and heat-sink.

- pre-summing of the E_T results from all four trigger channels to form a 0.2×0.2 jet element, in order to reduce the number of links to the JEP system;
- providing of pipelined event data readout to document the L1 trigger decision;
- rate-metering and histogramming for trigger independent monitoring purposes.

The pre-processed E_T results are then routed to the LVDS serialisers, which send them to the CP and JEP systems at 480 Mbit/s. For configuration, readout and monitoring purposes, two custom, bi-directional and synchronous serial interfaces connect the PPrASIC with the ReM_FPGA.

The PPrMCM is a mini-printed circuit board ($2 \times 7\,\mathrm{cm}^2$) of which base is formed by a small four-layer FR4 substrate with layer-to-layer microvias. The nine unpackaged dies are wire-bonded to the substrate pads. In order to prevent corrosion as well as to damp mechanical vibrations, the dies and the wire bonds are covered with a glob-top material. Also, the area between the connectors is covered by a brass lid, to provide further protection and to act as a Faraday cage. The backside of the PPrMCM is completely covered by a black-anodized radiator, to remove the heat produced inside the area enclosed by the lid. The radiator can be observed in figure 2.

3 The new PPrMCM

The technological decisions for the PPrMCM were taken more than ten years ago. Given the compactness of the PPrMCM and the multitude and complexity of processing tasks assigned to the module, at that time it was not possible to use packaged, re-programmable components. The FPGAs were too large to match the size of the PPrMCM, the featured resources were insufficient for implementing all the processing algorithms, and the costs were prohibitive. Therefore, the usage of a small ASIC-die ($8.370 \times 8.375\,\mathrm{mm}^2$, $0.6\,\mu$m CMOS), was the appropriate solution.

The PPrMCMs are successfully used in the ATLAS experiment. However, in the view of the LHC upgrade plans, leading to increase in luminosity and pile-up, there is a need for the PreProcessor to improve significantly the capabilities and the performance of its current trigger algorithms, as well as to add new functionalities, e.g.:

- improved bunch-crossing identification (BCID) algorithm for saturated pulses, in order to handle analogue trigger-tower signals with a peaking time longer than 50 ns (see figure 4);
- improved noise filtering to maximise the energy resolution;

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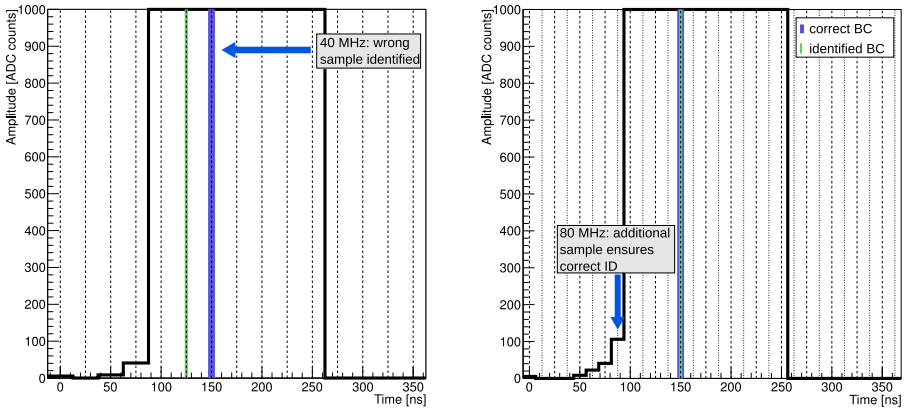

Figure 4. Simulation of the current (*left*) and improved (*right*) BCID algorithms for saturated pulses. The latter requires a sampling of the analogue input at 80 MHz.

- dynamic pedestal correction to handle the signal pile-up in the calorimeters at high LHC luminosities;
- separate fine-calibration for the E_T data sent to CP and JEP systems;
- double LVDS data rate output (960 Mbit/s) to the upgraded JEP to transmit 0.1×0.1 E_T information.

A rework of the PPrMCM in the same configuration, but with a re-designed PPrASIC that would include the new processing algorithms, is limited by several technical aspects, as described in [3]. For these reasons, a PPrMCM substitute, functionally, mechanically and electrically equivalent to the current module, has been built at Kirchhoff-Institute for Physics (KIP) Heidelberg, to profit from the technical progress of the last ten years and to enhance the flexibility of the digital processing.

3.1 Test results from a first prototype

The new PPrMCM carries the following main components (see figure 5):

- two dual-channel 105 MHz ADCs for compact, fast, low noise and low power digitisation;
- one Xilinx Spartan-6 FPGA as flexible, low-cost, configurable digital processing unit;
- one EEPROM device to store the configuration file of the FPGA;
- one Signal Generator electronics circuit to serve as on-board test facility.

The functionality of the first prototype for the new PPrMCM has been tested on the PPM in Heidelberg.

The ADCs have 10-bit resolution and they are operated at twice the LHC bunch-crossing frequency (i.e. 80.16 MHz), to ensure the same latency (i.e. 62.5 ns) of the digitisation process as in the current PPrMCM design. Digitisation of DC input shows noise distributions with a width below one ADC count for all four channels of the module (see figure 6). The fine-adjusted digitisation

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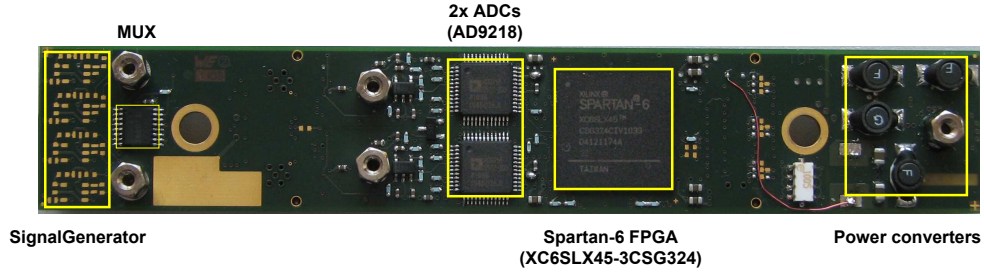

Figure 5. Rear view of the new PPrMCM. The EEPROM device and the interfacing connectors are mounted on the front side.

strobes are provided by the FPGA, which takes over the functionality of the PHOS4 chip. The strobes and the fine-time adjustment are implemented using high-speed output shift registers operated at 960 MHz. The method is used to perform a delay scan in 1.042 ns steps of an analogue signal produced by an waveform generator (see figure 7). The reproduction of the input is a good evidence for the successful implementation. The currently achieved resolution of 1.042 ns (24 delay steps) is slightly larger than the 1 ns resolution of the PHOS4 chip (25 steps), but it can be further improved, if necessary, to 0.96 ns (26 steps) by operating the shift registers to 1040 MHz. The method initially proposed in [3], based on the usage of the FPGA's Digital Clock Manager blocks, was dropped due to the large number of clocking resources required for implementation.

The FPGA, called Calorimeter Information Pre-processor (CALIPPR), implements also the trigger algorithms of the PPrASIC and the full functionality of the LVDS serialisers. The PPrASIC algorithms are driven by the LHC clock frequency, therefore the input 80 MHz digital streams from the ADCs are reduced to 40 MHz streams in CALIPPR, by discarding every second input 10-bit data. The serialisation and transmission in LVDS format is realised with high-speed shift registers operated at 480 MHz and differential output buffers. The data quality of the LVDS serialisation is shown on the left side of figure 8. Even double LVDS data rate, i.e. 960 Mbit/s, is produced and transmitted to the motherboard's periphery permitting the upgrade to 0.1×0.1 granularity for the JEP system (see figure 8, right). However, the transfer of these data streams over 11 m long cables to the JEP remains to be tested.

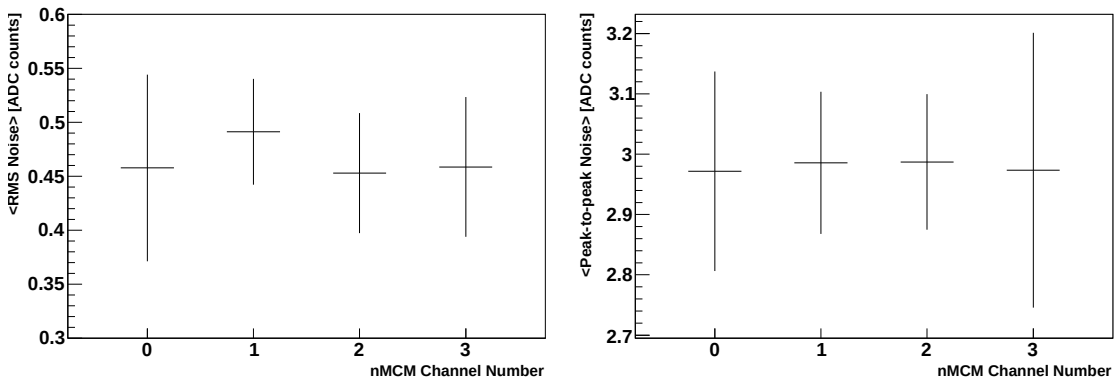

Figure 6. Measured RMS (*left*) and peak-to-peak (*right*) noise values per PPrMCM channel.

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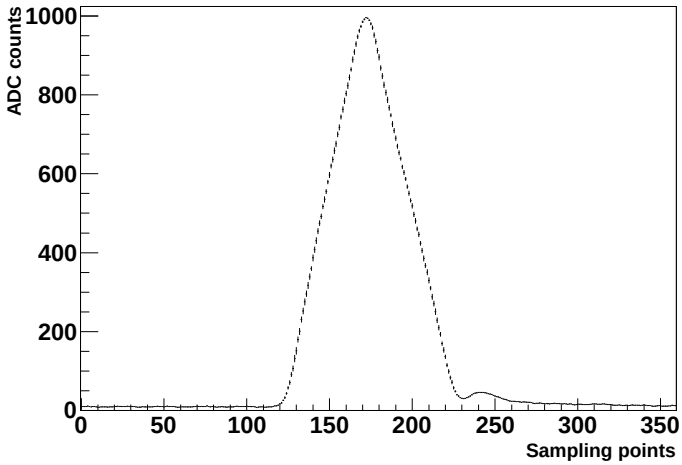

Figure 7. Fine-timing tests: reconstruction of an analogue pulse with 1.042 ns resolution.

The EEPROM serves as configuration loader at power-on for the FPGA. The configuration file is written to EEPROM from VME, via CALIPPR. Two methods are provided. The first one uses a JTAG chain implemented on the PPM, to transfer the data serially to the PPrMCMs. The second method is faster, allowing to transfer the data in parallel to all 16 PPrMCMs, via the ReM_FPGA. The EEPROM stores also, in addition to the configuration file, an unique, write protected, identification number for each PPrMCM.

The Signal Generator block provides the possibility to perform standalone tests avoiding complex external set-ups. The parameters of the generated analogue signals, e.g. amplitude, width or pedestal level, are controlled from the CALIPPR FPGA. A programmable multiplexing device is built on the PPrMCM to switch between calorimeter signals and generated pulses (see again figure 5).

An essential fact of "electrical compatibility" is the latency required by the new PPrMCM. A measurement shows that the new module is compatible with the current one (see figure 9).

The new PPrMCM is slightly longer than the current module (12 cm vs. 7 cm), but still fitting on the motherboard. The extension was mainly determined by the need for local power converters. On the current PPrMCM, only two voltages are needed to supply the active components, i.e. 5 V

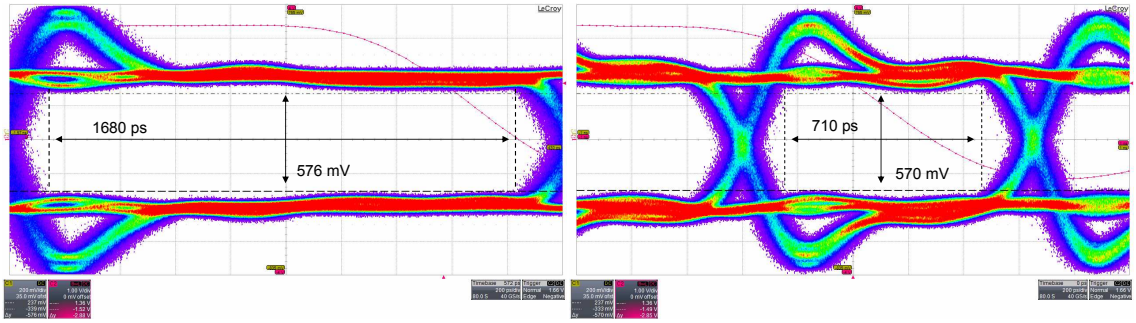

Figure 8. LVDS transmission tests at 480 Mbit/s (*left*) and 960 Mbit/s (*right*).

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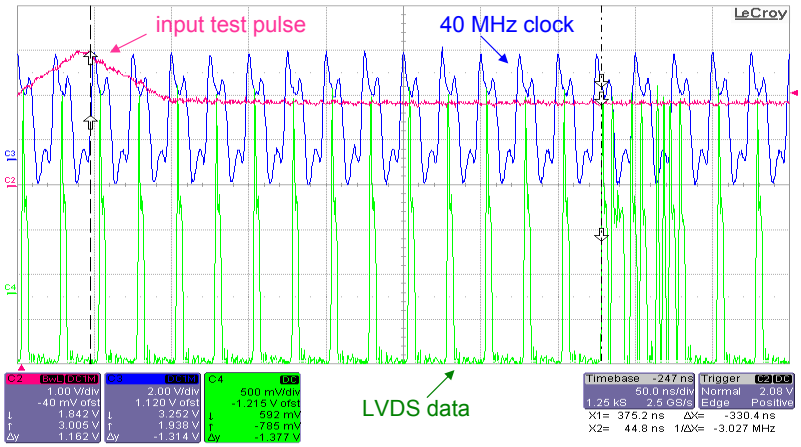

Figure 9. PPM latency measurements from the output of the AnIn board to the output of the PPM. The measured value is 330 ns (equivalent to 13 bunch-crossings), similar to that obtained with the current PPrMCM (i.e. 325 ns).

for the PPrASIC and 3.3 V for the ADCs, both being received from the power management of the motherboard. On the new PPrMCM, two additional voltages are required, 1.2 V for the FPGA core and 2.5 V for the LVDS output, which are derived from the 3.3 V via power converters.

The new PPrMCM will also be equipped with a heat-exchanging system. The foreseen implementation consist of a compressible film with very good thermal characteristics, to cover the central part of the PPrMCM where most of the active components are placed, and a black-anodized aluminium lid, which will cover the entire surface of the PPrMCM and serve as a heat-sink.

4 Conclusions

A first prototype of the new PPrMCM has been successfully tested. Full compatibility with existing PPrMCM in hardware and operational requirements has been shown. Some additional features (e.g. double LVDS data rate) were demonstrated as well. Hence, the flexible, new module is able to master the challenges presented by the highest luminosities at LHC.

Acknowledgments

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