Total No. of Questions : 8]

SEAT No. : [ ]

PC2836

[Total No. of Pages :2

[6352]-60

S.E. (I.T.)

LOGIC DESIGN & COMPUTER ORGANIZATION

(2019 Pattern) (Semester- III) (214442)

Time : 2½ Hours] ***[Max. Marks : 70***

Instructions to the candidates:

1) ***Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, and Q.7 or Q.8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Assume suitable data. If necessary.***

Q1) a) Convert JK-FF into T-FF. **[6]**

b) Compare combinational circuits and sequential circuits with example? **[6]**

c) Design MOD-96 using Asynchronous Decade Counter IC 7490 **[6]**

OR

Q2) a) Explain D-FF with Logic diagram, Symbol & Truth Table. **[6]**

b) Design 3-bit Asynchronous up Counter using JK-FF **[6]**

c) State the types of shift register with application of each. **[6]**

Q3) a) Explain components of CPU with Block Diagram? **[6]**

b) Write required micro operations and control signals for instruction ADD (R3) R1? **[6]**

c) Compare horizontal and vertical microinstruction format **[5]**

OR

Q4) a) Explain various types of Registers? State the function of Control and status Registers. **[6]**

b) Write in brief about multiple bus organization with suitable diagram? **[6]**

c) Compare Hardwired control unit with Micro Programmed control Unit? **[5]**

Q5) a) Differentiate between UMA and NUMA? **[6]**

b) What is meant by interrupt? Mention steps of interrupt handling procedure of microprocessor? **[6]**

c) What is mean by Multi-core architecture? Discuss its advantages? **[6]**

OR

Q6) a) What is mean by Addressing modes? Explain any two addressing modes with suitable example? **[6]**

b) Write a short note explaining instruction pipelining, its advantages and disadvantages? **[6]**

c) Describe Flynn's taxonomy for parallel computing? **[6]**

Q7) a) Write a short note on memory hierarchy? Write any four the characteristics of memory system **[8]**

b) Briefly describe different cache mapping techniques? **[9]**

OR

Q8) a) Explain DMA operation with help of suitable diagram? Compare Programmed I/O and Interrupt Driven I/O. **[8]**

b) What is mean by Cache Coherence? Explain cache coherence prolem in single processor systems? **[9]**