Total No. of Questions : 8]

SEAT No. : [ ]

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S.E. (Information Technology Engg.)

LDCO : LOGIC DESIGN & COMPUTER ORGANIZATION

(2019 Pattern) (Semester - III) (214442)

Time : 2½ Hours] ***[Max. Marks : 70***

Instructions to the candidates:

1) ***Answer Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***

Q1) a) Differentiate between Combinational circuit & Sequential circuits? **[6]**

b) Design flip flop conversion logic to convert J-K flip flop to T flip-flop? **[6]**

c) Design and draw MOD 96 Counter using IC 7490 & explain its operations? **[6]**

OR

Q2) a) Compare Asynchronous counters with Synchronous counters? **[6]**

b) Design flip flop conversion logic to convert S-R Flip Flop to a J-K Flip-Flop? **[6]**

c) Explain the working of 3-bit synchronous counter using J-K flip flop with suitable circuit diagram and state table? **[6]**

Q3) a) Describe with neat diagram Von Neumann Architecture of computer? **[6]**

b) Write a note on multiple bus hierarchies? **[5]**

c) Explain how system bus organization is used for communication between the major components of a computer with neat diagram? **[6]**

OR

P.T.O.

Q4) a) Describe with neat diagram Harvard Architecture of computer? **[6]**

b) Which are the types of ALU? Explain the operations of ALU by using various control signal? **[5]**

c) Explain the Control unit Implementation using Micro-programmed Implementation? **[6]**

Q5) a) Describe instructions with 0, 1, 2 or 3 addresses using suitable example. **[6]**

b) Differentiate between RISC & CISC Architecture. **[6]**

c) Define and explain with suitable diagram and example Instruction Pipelining Architecture of processor. **[6]**

OR

Q6) a) Describe cluster computer architecture with neat diagram. **[6]**

b) What is SMP? Draw suitable diagram of SMP & explain briefly. **[6]**

c) Explain interrupt handling process using IVT and ISR. **[6]**

Q7) a) Write short note on : **[8]**

i) EPROM

ii) EEPROM

b) What is cache coherency problem? Explain four different approaches to prevent cache coherence problem. **[9]**

OR

Q8) a) Explain cache memory operation using multilevel cache organization. **[8]**

b) Explain with neat diagram Signals used to Connect Memory to Processor. **[9]**