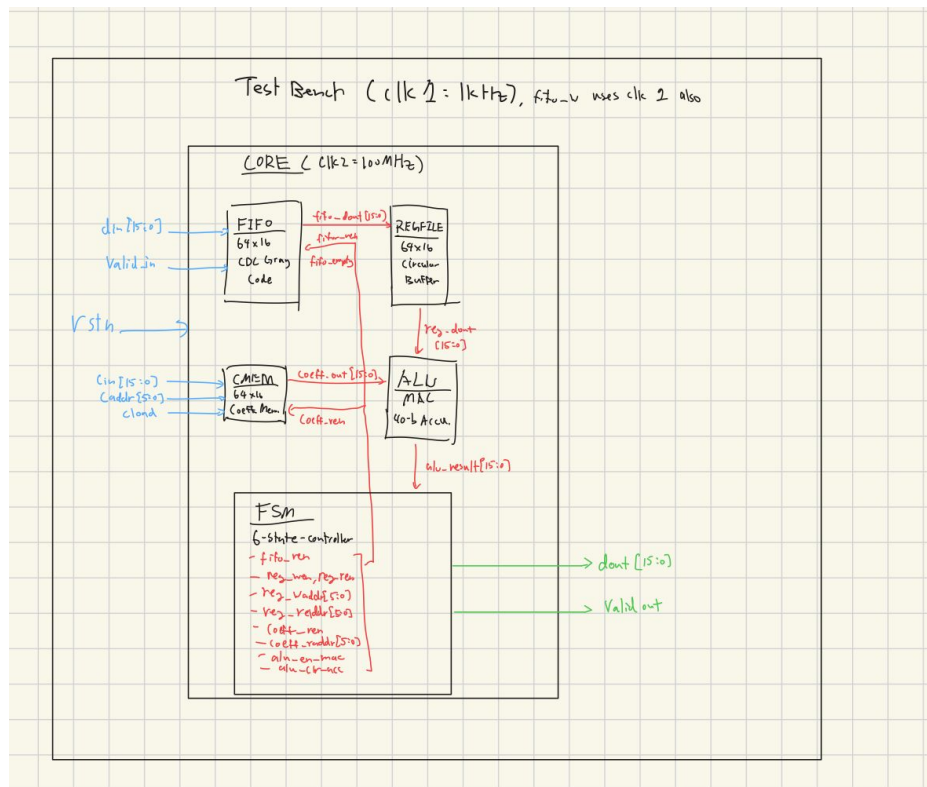# Design and Implementation of a 64-Tap 16-Bit FIR Filter with Dual-Clock Domain Crossing

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Top Level Architecture in Testbench

Input:
clk1 - Input sampling clock (10 kHz) clk2 - Processing clock (100 MHz)
rstn - Active-low async reset
din[15:0] - Input data samples (Q1.15 signed)
valid_in - Input data valid
cin[15:0] - Coefficient data (Q1.15 signed)
caddr[5:0] - Coefficient address (0-63)
cload - Coefficient load enable

Output:
dout[15:0] - Output data (Q7.9 signed)
valid_out - Output data valid

Internal (Simplified):
fifo_dout[15:0] - FIFO → REGFILE
coeff_out[15:0] - CMEM → ALU
coeff_raddr[5:0] - FSM → CMEM
reg_dout[15:0] - REGFILE → ALU
reg_raddr[5:0] - FSM → REGFILE
reg_waddr[5:0] - FSM → REGFILE
alu_result[15:0] - ALU → FSM

Methods and Results

Methods

- **Input:** Randomly generated 10,000 16-bit Q1.15 real-valued numbers
- **Coefficients:** Randomly generated 16-bit Q1.15 real-valued numbers
- **RTL coding from scratch:** Yes
- **Throughput:** Measured with PrimeTime using DC-generated SDF annotation
- **Maximum clock frequency:** Determined from PrimeTime timing analysis with DC-generated SDF annotation
- **Energy efficiency:** PrimeTime with DC-generated SDF and QuestaSim-generated VCD annotations
- **Area:** From Design Compiler synthesis report
- **Accuracy:** NRMSE compared to MATLAB results in 32-bit floating-point numbers

Results

- **Throughput:** 10 kS/s
- **Maximum clock frequency:** 100 MHz
- **Energy efficiency:** 338.4 pJ/sample (0.034 mW/MHz)
- **Area:** 0.0466 mm² (46,551 μm²)
- **Accuracy NRMSE:**
  - Worst case: 0.012%
  - Average: 0.003%