Albert Wang

aw3741@columbia.edu | albert-wang1010.github.io | linkedin.com/in/albert-wang1

Education

Columbia University Aug. 2024 – May 2026
B.S. Electrical Engineering | GPA: 3.81/4.0 | Dean's List 2024, 2025 *New York, NY*

Bates College Aug. 2021 – May 2026
B.A. Physics, Minor in Philosophy | GPA: 3.97/4.0 | Dean's List 2021-2024 *Lewiston, ME*

Technical Skills

IC Design: CMOS transistor sizing, op-amp/filter design, small-signal analysis, biasing, stability; Cadence Virtuoso (schematic/layout/DRC/LVS/extraction), LTspice, Synopsys Design Compiler, PrimeTime
HDL & Digital: Verilog, VHDL, SystemVerilog; RTL/gate-level simulation, timing analysis, FSM design, synthesis
Lab & PCB: Oscilloscope, function generator, DMM, soldering; Autodesk Fusion 360 Electronics
Programming: Python, C/C++, MATLAB, Java; embedded systems, data analysis
Languages: English (native), Chinese (fluent)

Projects

Full-Custom 65nm VLSI Microprocessor Fall 2025, *New York, NY*

- Designed 8-bit microprocessor schematic-to-layout in 65nm CMOS using **Cadence Virtuoso**; included ALU, shifter, 8×8 SRAM, decoder, PLA control.
- Achieved 100 MHz with 88.8% timing margin, 4,100 μm^2 area; completed DRC/LVS verification for all blocks.
- Post-layout characterization: 2-3× delay increase from parasitic effects; optimized for 876 μW power consumption.

64-Tap FIR Filter with Clock Domain Crossing Fall 2025, *New York, NY*

- Designed 64-tap 16-bit FIR filter in **Verilog** with asynchronous FIFO (Gray code sync), MAC with saturation, FSM controller.
- Synthesized using **Synopsys Design Compiler** (IBM 130nm) achieving 100 MHz timing closure, 46,551 μm^2 area; validated via gate-level simulation with SDF.
- Power analysis via **PrimeTime PX**: 3.384 mW total, 0.034 mW/MHz efficiency, 100% VCD annotation.

Two-Stage CMOS Op-Amp with Miller Compensation Fall 2025, *New York, NY*

- Designed two-stage OTA with Miller compensation: gain = 4 V/V, 76 dB open-loop, 47° phase margin, 203 kHz.
- Optimized transistor sizing (W/L 4-184) for 700 μA budget with <0.1% DC accuracy; 5.4 μs, <6.5% overshoot.
- Performed AC/DC/transient analysis in **Cadence Spectre**; verified stability across process, voltage, and temperature corners.

Power Distribution PCB - Columbia Space Initiative Fall 2024, *New York, NY*

- Led electronics team designing power distribution PCB using **Autodesk Fusion 360**; integrated overcurrent protection for high-power rocket avionics.

Experience

Hardware Security Intern (PUF/HSM) July 2025 – September 2025
eMemory Technology Inc. *Hsinchu, Taiwan*

- Mapped Thales **LunaSH/LunaCM** and **PKCS#11** to **PUF**-backed HSM framework; co-authored API specs for partitions, protocols, HA/backup, operations.
- Aligned interface designs with **FIPS 140-3** requirements; identified compliance checkpoints and test methodologies for certification.

Research

NSF-REU Computational Physics Researcher May 2024 – October 2024
Clarkson University *Potsdam, NY*

- Developed projection-based learning methodology in **MATLAB** achieving 100× speedup for photonic crystal simulations; co-authored SPIE Photonics West paper (DOI: 10.1117/12.3028208).

Undergraduate Researcher in Neutrino Detection May 2023 – May 2024
University of Massachusetts Amherst *Amherst, MA*

- Investigated SiPM photon detection efficiency in liquid xenon for nEXO neutrinoless double beta decay experiment; analyzed waveforms using **Python**/Geant4; presented at APS April 2024.