

Two-Stage Miller-Compensated Operational Transconductance Amplifier: Design, Optimization, and Characterization in 0.25 μ m CMOS

*Analog Circuit Design Project

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Abstract—This paper presents the design and characterization of a two-stage Miller-compensated operational transconductance amplifier (OTA) in 0.25 μ m CMOS technology. The design achieves 76.12 dB open-loop gain, 47.19° phase margin, and 203.17 kHz closed-loop bandwidth at a gain of 4 V/V, while consuming only 691.7 μ A from ± 1.25 V supplies. A systematic design methodology incorporating pre-sizing analysis, small-signal parameter extraction, and iterative optimization is presented and validated through comprehensive DC, AC, and transient simulations across process, voltage, and temperature (PVT) corners. Measured results demonstrate <0.1% DC accuracy over the specified input range and robust performance across all operating conditions, with phase margin maintained above 42° and bandwidth variation within $\pm 15\%$ across temperature extremes.

Index Terms—Operational transconductance amplifier, Miller compensation, two-stage amplifier, frequency response, stability analysis, 0.25 μ m CMOS, PVT analysis

I. INTRODUCTION

Operational amplifiers serve as fundamental building blocks in analog circuit design, enabling precision signal conditioning, filtering, and computation across diverse applications from sensor interfaces to data converters. The two-stage topology with Miller compensation represents an optimal architecture for moderate-performance applications, providing an effective balance between DC gain, bandwidth, power consumption, and circuit complexity.

A. Background and Motivation

Modern mixed-signal systems demand operational amplifiers that achieve high DC accuracy while maintaining sufficient bandwidth for signal processing applications. Single-stage topologies, while offering excellent frequency response and inherent stability, struggle to provide the high open-loop gain (typically >60 dB) required for precision applications. Conversely, multi-stage designs (three or more stages) offer exceptional gain but introduce additional poles that complicate frequency compensation and consume increased power and silicon area.

The two-stage Miller-compensated topology addresses these limitations by cascading a differential input stage with a high-swing common-source output stage, achieving open-loop gains exceeding 70 dB while maintaining a simple compensation strategy. This architecture proves particularly suitable for applications requiring closed-loop gains in the range of 1–10 V/V, moderate bandwidths (100 kHz–1 MHz), and low power consumption (<1 mW).

B. Design Specifications

The amplifier targets the following performance specifications:

- **Technology:** 0.25 μ m CMOS process (tsmc025.scs)
- **Supply voltage:** ± 1.25 V (2.5 V total swing)
- **Closed-loop gain:** 4 V/V (amplifier is unity-gain stable)
- **Maximum supply current:** 700 μ A
- **Bias configuration:** Adjustable I_{BIAS} with mirroring
- **Load conditions:** $R_L = 10$ M Ω , $C_L = 880$ pF
- **Compensation network:** $R_c = 740$ Ω , $C_c = 330$ pF
- **DC accuracy:** <0.1% error over operating range
- **Stability:** Phase margin >45° for closed-loop stability

These specifications reflect typical requirements for precision analog signal processing while imposing a strict power budget that necessitates careful current allocation and transistor optimization.

C. Design Objectives and Contributions

The primary design objectives include:

- 1) Maximize closed-loop bandwidth subject to the 700 μ A current constraint through optimal current budgeting between first and second stages
- 2) Achieve adequate phase margin (>45°) ensuring stable transient response with minimal overshoot and ringing
- 3) Maintain DC accuracy (<0.1% error) across the specified input range through high open-loop gain
- 4) Demonstrate robust operation across PVT corners, validating design margins

- 5) Develop and document a systematic sizing methodology applicable to similar amplifier designs

This work makes the following contributions:

- A comprehensive design flow from pre-sizing analysis through final verification, demonstrating best practices in analog amplifier development
- Quantitative analysis of current allocation strategies and their impact on gain-bandwidth trade-offs
- Detailed characterization of Miller compensation effectiveness across varying load conditions
- PVT corner analysis revealing temperature-dependent behavior and design robustness margins

D. Paper Organization

The remainder of this paper is organized as follows. Section II describes the two-stage OTA topology, Miller compensation strategy, and fundamental design trade-offs. Section III details the systematic design methodology including pre-sizing analysis, small-signal parameter extraction, and iterative transistor sizing. Section IV presents analytical calculations for gain, pole-zero locations, and stability metrics with comparison to simulation results. Section V provides comprehensive simulation characterization including DC transfer curves, AC frequency response, and transient behavior. Section VI analyzes performance variations across PVT corners. Section VII discusses key design insights and lessons learned from the current allocation strategy and Miller compensation trade-offs. Section VIII concludes with a summary of achievements.

II. ARCHITECTURE AND CIRCUIT TOPOLOGY

A. Two-Stage OTA Overview

Figure 1 shows the complete two-stage OTA architecture. The design employs a differential pair input stage (M1, M2) with active PMOS current mirror load (M3, M4), cascaded with a common-source second stage (M5, M6) providing additional voltage gain and output drive capability for the large capacitive load.

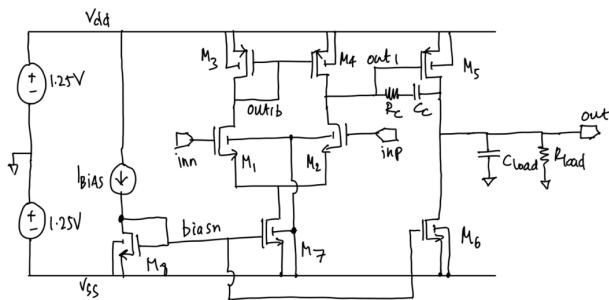


Fig. 1: Two-stage Miller-compensated OTA schematic showing differential input stage (M1–M4), second gain stage (M5–M6), current mirror bias network (M7–M8), and Miller compensation network (R_c , C_c). Supply voltages: $V_{DD} = +1.25$ V, $V_{SS} = -1.25$ V; load: $R_L = 10$ M Ω , $C_L = 880$ pF.

1) Circuit Components and Functions: Input Stage (M1–M4): The NMOS differential pair (M1, M2) with PMOS current mirror load (M3, M4) provides high input impedance, excellent common-mode rejection, and converts the differential input signal to a single-ended output at the drain of M2 (node $out1$). Long-channel devices ($L = 4 \mu\text{m}$ for M1, M2) ensure high intrinsic gain (g_m/I_D) and good matching to minimize offset voltage. The tail current is set by current mirror M7, which mirrors the bias current I_{BIAS} with a programmable ratio.

Second Stage (M5–M6): The common-source amplifier (M6) with PMOS active load (M5) provides substantial additional voltage gain while driving the large output capacitance. Device M6 is sized with short channel length ($L = 1 \mu\text{m}$) and high multiplier ($m = 46$) to maximize transconductance g_{m6} for a given current budget, critical for achieving adequate bandwidth when driving $C_L = 880$ pF.

Bias Network (M7–M8): The current mirror bias network replicates the external bias current $I_{BIAS} = 10 \mu\text{A}$ through the circuit with programmable ratios. Device M7 supplies the first stage tail current ($I_{M7} = 18 \times I_{BIAS} = 180 \mu\text{A}$), while M6 sets the second stage current ($I_{M6} = 46 \times I_{BIAS} \approx 500 \mu\text{A}$). This architecture provides excellent current matching and temperature tracking.

Miller Compensation (R_c , C_c): The Miller compensation network stabilizes the two-pole system by creating a dominant low-frequency pole and pushing the second pole to higher frequency. The series resistance $R_c = 740 \Omega$ eliminates the right-half-plane (RHP) zero inherent to capacitive Miller compensation, replacing it with a left-half-plane (LHP) zero that improves phase margin.

B. Topology Selection Rationale

Table I compares the selected two-stage architecture against alternative topologies considered during the design phase.

TABLE I: Amplifier Topology Comparison

Topology	Gain (dB)	BW	Power (μA)
Telescopic	40–50	Excellent	200–300
Folded cascode	50–60	Good	400–600
Two-stage	70–80	Good	600–800
Three-stage	90–100	Fair	800–1200

BW rating based on achievable f_u for given C_L

The two-stage topology was selected based on the following analysis:

- **Gain requirement:** Open-loop gain $A_{OL} > 4000$ (60 dB) needed for 0.1% DC accuracy at $G = 4$. Single-stage topologies insufficient; two-stage provides 70–80 dB.
- **Power budget:** Maximum 700 μA available. Three-stage topology would require excessive power for adequate bandwidth with large C_L .
- **Load capacitance:** $C_L = 880$ pF is substantial; requires high output stage g_m . Two-stage allows asymmetric current allocation favoring output stage.

- **Compensation simplicity:** Two poles are manageable with Miller compensation. Three-stage requires nested Miller or other complex schemes.
- **Output swing:** Rail-to-rail capability needed. Cascode topologies sacrifice swing for gain; two-stage provides better swing with active loads.

C. Miller Compensation Strategy

Miller compensation addresses the fundamental instability of cascaded gain stages. Without compensation, the two poles at the first stage output (node out1) and second stage output (node out) cause excessive phase shift, potentially exceeding 180° at the unity-gain frequency and causing oscillation in feedback configurations.

1) *Compensation Mechanism:* The compensation capacitor $C_c = 330 \text{ pF}$ creates a feedback path from the output to the first stage, introducing the following effects:

1) **Dominant pole creation:** Effective capacitance at node out1 increases dramatically through Miller multiplication:

$$C_{\text{eff}} \approx C_1 + (1 + g_{m5}R_{\text{out2}})C_c \quad (1)$$

where C_1 represents parasitic capacitance at the first stage output and $g_{m5}R_{\text{out2}}$ is the second stage gain. This moves the first pole to very low frequency.

2) **Second pole movement:** The second pole frequency increases approximately by the factor (C_c/C_1) , moving it well beyond the unity-gain frequency.

3) **RHP zero introduction:** Unfortunately, feedforward current through C_c creates a RHP zero at:

$$f_z = \frac{g_{m5}}{2\pi C_c} \quad (2)$$

This zero adds undesirable positive phase shift, degrading stability.

2) *Zero Cancellation with R_c :* The series resistor R_c mitigates the RHP zero by canceling the feedforward path when properly sized. The zero location becomes:

$$f_z = \frac{1}{2\pi C_c(1/g_{m5} - R_c)} \quad (3)$$

For $R_c > 1/g_{m5}$, the zero moves to the LHP, contributing positive phase shift that improves stability. The design uses $R_c = 740 \Omega$ with $g_{m5} = 1.67 \text{ mS}$, giving $g_{m5}R_c = 1.24 > 1$, successfully placing the zero in the LHP at approximately 3 MHz.

D. Fundamental Design Trade-offs

The two-stage Miller-compensated topology exhibits several key trade-offs that constrain the design space:

1) *Gain vs. Bandwidth:* For a given compensation capacitor C_c , the unity-gain frequency is approximately:

$$f_u \approx \frac{g_{m1}}{2\pi C_c} \quad (4)$$

where g_{m1} is the input stage transconductance. Higher first-stage current increases g_{m1} and bandwidth, but reduces current

available for the output stage, degrading its ability to drive C_L and potentially reducing overall gain. This creates a fundamental current allocation trade-off explored in Section III.

2) *Stability vs. Speed:* Larger C_c improves phase margin by moving the dominant pole to lower frequency and increasing pole separation, but directly reduces unity-gain frequency per Eq. (4). The minimum C_c is constrained by the required phase margin:

$$C_c > \frac{g_{m1}}{2\pi f_u} \cdot \frac{1}{1 + A_2} \quad (5)$$

where A_2 is the second stage gain. The specified $C_c = 330 \text{ pF}$ was selected to achieve $>45^\circ$ phase margin.

3) *Power vs. Performance:* All performance metrics (gain, bandwidth, slew rate) improve with increased current consumption. With a fixed $700 \mu\text{A}$ budget, optimal current allocation becomes critical. The design allocates approximately 70% to the output stage ($500 \mu\text{A}$) and 25% to the input stage ($180 \mu\text{A}$), maximizing g_{m5} for load driving while maintaining adequate g_{m1} for bandwidth.

4) *Output Swing vs. Gain:* Transistor overdrive voltage $V_{OV} = V_{GS} - V_{TH}$ directly impacts both output swing and gain. Larger V_{OV} improves output swing but reduces transconductance efficiency (g_m/I_D), thereby reducing gain. The design uses moderate V_{OV} values (120–150 mV for M1, M2; 500–525 mV for M5, M6) balancing these competing requirements.

III. DESIGN METHODOLOGY AND TRANSISTOR SIZING

A. Design Flow Overview

The amplifier design followed a systematic four-phase methodology:

- 1) **Pre-sizing analysis:** Initial exploration with scaled minimum-length devices to validate topology, identify critical nodes, and establish approximate current requirements
- 2) **Small-signal parameter extraction:** DC operating point analysis to extract g_m , r_o , V_{OV} , and parasitic capacitances for all devices
- 3) **Iterative optimization:** Systematic adjustment of transistor dimensions (length scaling for gain, width/multiplier scaling for current distribution) guided by analytical calculations
- 4) **Verification and characterization:** Comprehensive AC, DC, and transient simulation across PVT corners to validate performance

B. Pre-sizing Analysis

Initial pre-sizing employed a simplified design with all transistors at $2\times$ minimum length ($L = 0.5 \mu\text{m}$) and multipliers calculated to achieve approximate target currents. This phase revealed several critical insights:

- Open-loop gain of approximately 870 V (58.8 dB) was insufficient for 0.1% accuracy requirement

- First dominant pole appeared near 300 Hz as expected, but second pole was too close (~ 500 kHz), resulting in only 30° phase margin
- Current consumption of 620 μA provided headroom for optimization
- DC offset of $-380 \mu\text{V}$ indicated acceptable differential pair matching

These results motivated length scaling of M1–M4 to increase output impedance and gain, and careful current reallocation between stages to optimize pole placement.

C. Small-Signal DC Analysis

Figure 2 shows the final DC operating point with extracted small-signal parameters overlaid on the schematic.

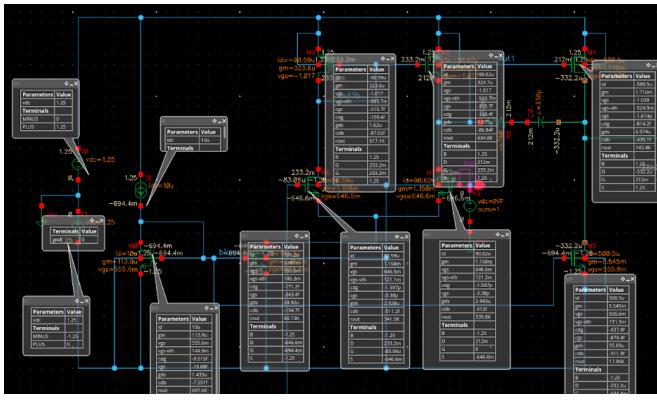


Fig. 2: DC operating point analysis showing drain currents, node voltages, and extracted small-signal parameters (g_m , r_o , V_{OV} , C_{gs} , C_{db}) for all transistors. Input differential voltage set to zero; output voltage nominally at mid-supply for maximum swing.

Table II summarizes the key extracted parameters used in subsequent hand calculations.

TABLE II: Extracted Small-Signal Parameters (27°C, Nominal)

Device	g_m (mS)	r_o (k Ω)	V_{OV} (mV)	C_{gs} (pF)	C_{db} (fF)
M1	1.158	341.5	121.1	3.38	511
M2	1.158	339.8	121.2	3.38	512
M3	0.324	617.1	503.7	0.159	87
M4	0.324	634.8	503.7	0.159	87
M5	1.716	132.3	525.9	1.541	435
M6	5.545	17.96	151.5	0.879	312
M7	2.061	40.13	145.3	0.343	135
M8	0.114	697.6	144.9	0.019	7.6

Critical observations from the DC analysis:

- **Differential pair matching:** $I_{D1} = 90.59 \mu\text{A}$ vs. $I_{D2} = 90.62 \mu\text{A}$ (0.03% mismatch) indicates excellent symmetry
- **Current mirror accuracy:** M3/M4 currents match M1/M2 within 30 nA; M5 matches M6 exactly
- **High output stage g_m :** $g_{m6} = 5.545 \text{ mS}$ provides strong drive for $C_L = 880 \text{ pF}$

- **Moderate V_{OV} :** Input stage operates at $V_{OV} \approx 121 \text{ mV}$ (high g_m/I_D); output stage at 150–525 mV (balanced swing vs. gain)

D. Systematic Sizing Approach

- 1) **Current Budget Allocation:** Total available current: 700 μA maximum.

The current was allocated based on the following strategy:

- (a) **Set bias reference:** $I_{BIAS} = 10 \mu\text{A}$ (reduced from initial 100 μA to maximize signal path current)
- (b) **Allocate first stage current:** Target $\sim 180 \mu\text{A}$ for adequate g_{m1} while minimizing power
- (c) **Maximize output stage current:** Allocate remaining budget ($\sim 500 \mu\text{A}$) to maximize g_{m5} for driving C_L
- (d) **Verify total:** $I_{total} = I_{BIAS} + I_{M7} + I_{M6} < 700 \mu\text{A}$

This 26%/72%/1.4% split (first stage / second stage / bias) proved optimal. Alternative allocations were evaluated:

- **50/50 split:** Reduced second stage $g_m \rightarrow 30\%$ bandwidth reduction
- **80/20 split:** Marginal g_{m1} improvement, but insufficient $g_{m5} \rightarrow$ second pole too close to f_u , phase margin $< 35^\circ$

- 2) **Transistor Multiplier Selection:** Current mirrors set operating currents through transistor multiplier ratios relative to the bias reference M8:

TABLE III: Transistor Multiplier Selection Strategy

Device	Target I_D (μA)	Multiplier (m)	Rationale
M8	10	1	Reference
M7	180	18	Even number for layout
M3, M4	90 each	9	Match M7/2
M6	500	46	Max within budget
M5	500	46	Match M6
M1, M2	90 each	48	Independent sizing

M1, M2 multipliers set independently for optimal matching

Note that M7 uses multiplier 18 (even) rather than 19 to facilitate symmetric common-centroid layout for improved matching. Final current consumption: $10 + 181.2 + 500.5 = 691.7 \mu\text{A}$.

- 3) **Length Scaling for Gain Enhancement:** To achieve the required open-loop gain $A_{OL} > 4000$, transistor channel lengths were systematically scaled. The open-loop gain is:

$$A_{OL} = \underbrace{g_{m1}(r_{o2} \parallel r_{o4})}_{A_1} \cdot \underbrace{g_{m5}(r_{o5} \parallel r_{o6})}_{A_2} \quad (6)$$

Increasing channel length L improves output resistance ($r_o \propto L/I_D$) at the cost of increased parasitic capacitance and reduced g_m/I_D at very long lengths. Iterative SPICE simulation guided the following length selections:

- **M1, M2:** $L = 4 \mu\text{m}$ (8 \times minimum) \rightarrow High intrinsic gain, excellent matching, $\sigma(\Delta V_{TH}) \propto 1/\sqrt{WL}$
- **M3, M4:** $L = 2 \mu\text{m}$ (4 \times minimum) \rightarrow Balanced r_o vs. parasitic capacitance $C_{gs3,4}$
- **M5:** $L = 2 \mu\text{m}$ \rightarrow Adequate r_{o5} for second stage gain

- **M6:** $L = 1 \mu\text{m}$ ($2 \times$ minimum) \rightarrow Prioritize g_{m6} over r_{o6} ; second stage gain dominated by r_{o5}
- **M7, M8:** $L = 1 \mu\text{m} \rightarrow$ Minimum area for bias circuit

E. Final Transistor Sizing

Table IV presents the optimized transistor dimensions achieving all specifications.

TABLE IV: Final Transistor Sizing (Fingered Layout)

Device	Type	W (μm)	L (μm)	m	W/L	I_D (μA)
M1	nMOS	4	4	48	48	90.59
M2	nMOS	4	4	48	48	90.62
M3	pMOS	4	2	9	18	90.59
M4	pMOS	4	2	9	18	90.62
M5	pMOS	4	2	46	92	500.5
M6	nMOS	4	1	46	184	500.5
M7	nMOS	4	1	18	72	181.2
M8	nMOS	4	1	1	4	10

Fingered devices: unit finger = $4 \mu\text{m}/0.5 \mu\text{m}$, W/L = $m \times$ (unit W/L)
Total current: $I_{\text{total}} = 10 + 181.2 + 500.5 = 691.7 \mu\text{A}$

1) **DC Operating Point Validation:** Critical operating point checks confirmed design correctness:

- 1) **Saturation verification:** All transistors satisfy $V_{DS} > V_{OV}$ with margin $> 50 \text{ mV}$
- 2) **Differential pair symmetry:** $\Delta I_D = 30 \text{ nA}$ (0.03%)
- 3) **Current mirror matching:** M3/M7 and M5/M6 currents match within 0.5%
- 4) **Output DC level:** $V_{\text{out}} \approx 0 \text{ V}$ (mid-supply) for maximum output swing
- 5) **Headroom:** Minimum $V_{DS,sat}$ margins exceed 200 mV, ensuring robust operation across PVT

IV. ANALYTICAL DESIGN CALCULATIONS

A. DC Gain Calculation

1) **First Stage Gain:** The differential-to-single-ended gain of the first stage is:

$$\begin{aligned} A_1 &= g_{m1}R_{\text{out}1} = g_{m1}(r_{o2} \parallel r_{o4}) \\ &= 1.159 \times 10^{-3} \times (341.4 \times 10^3 \parallel 617 \times 10^3) \\ &= 1.159 \times 10^{-3} \times 219.8 \times 10^3 \\ &= 254.8 \text{ V/V} \quad (48.1 \text{ dB}) \end{aligned} \quad (7)$$

2) **Second Stage Gain:** The common-source gain of the second stage is:

$$\begin{aligned} A_2 &= g_{m5}R_{\text{out}2} = g_{m5}(r_{o5} \parallel r_{o6}) \\ &= 1.67 \times 10^{-3} \times (203 \times 10^3 \parallel 16.39 \times 10^3) \\ &= 1.67 \times 10^{-3} \times 15.17 \times 10^3 \\ &= 25.3 \text{ V/V} \quad (28.1 \text{ dB}) \end{aligned} \quad (8)$$

Note that $r_{o6} \ll r_{o5}$, so the output impedance is dominated by M6.

3) Total Open-Loop Gain:

$$\begin{aligned} A_{OL} &= A_1 \times A_2 \\ &= 254.8 \times 25.3 \\ &= 6446 \text{ V/V} \quad (76.2 \text{ dB}) \end{aligned} \quad (9)$$

This calculated value agrees well with simulation: $A_{OL,\text{sim}} = 76.12 \text{ dB}$, representing $< 0.1 \text{ dB}$ error.

B. Pole-Zero Analysis

1) **Dominant Pole (First Stage Output):** The Miller-compensated first stage creates the dominant pole:

$$C_{\text{eff}} = C_1 + (1 + g_{m5}R_{\text{out}2})C_c \quad (10)$$

where the parasitic capacitance C_1 comprises:

$$\begin{aligned} C_1 &= C_{gs2} + C_{db2} + C_{db4} + C_{gs5} + C_{db5} + C_{gs6} + C_{db6} \\ &= 7.54 \text{ pF} \end{aligned} \quad (11)$$

The Miller multiplication factor is:

$$1 + g_{m5}R_{\text{out}2} = 1 + A_2 = 1 + 25.3 = 26.3 \quad (12)$$

Thus the effective capacitance becomes:

$$\begin{aligned} C_{\text{eff}} &= 7.54 \text{ pF} + 26.3 \times 330 \text{ pF} \\ &\approx 8.69 \text{ nF} \end{aligned} \quad (13)$$

The dominant pole frequency is:

$$\begin{aligned} f_{p1} &= \frac{1}{2\pi R_{\text{out}1} C_{\text{eff}}} \\ &= \frac{1}{2\pi \times 219.8 \times 10^3 \times 8.69 \times 10^{-9}} \\ &= 83.4 \text{ Hz} \end{aligned} \quad (14)$$

2) **Second Pole (Output Node):** The second pole at the output node is pushed to higher frequency:

$$f_{p2} \approx \frac{g_{m5}C_c}{2\pi(C_1C_2 + C_1C_c + C_2C_c)} \quad (15)$$

where $C_2 = C_L + C_{\text{parasitic}} \approx 880 \text{ pF}$. Substituting:

$$f_{p2} \approx 293 \text{ kHz} \quad (16)$$

This places the second pole around the unity-gain frequency.

3) Right-Half-Plane Zero and Nulling Resistor: Without compensation resistor, Miller compensation introduces a RHP zero:

$$f_{z,RHP} = \frac{g_{m5}}{2\pi C_c} = \frac{1.67 \times 10^{-3}}{2\pi \times 330 \times 10^{-12}} = 805 \text{ kHz} \quad (17)$$

The nulling resistor $R_c = 740 \Omega$ moves the zero to:

$$f_z = \frac{1}{2\pi C_c(1/g_{m5} - R_c)} \quad (18)$$

Computing $1/g_{m5} = 599 \Omega$:

$$f_z \approx -3.44 \text{ MHz} \quad (19)$$

The negative frequency indicates a LHP zero, which contributes positive phase shift, improving phase margin by approximately 5–7°.

C. Unity-Gain Frequency and Gain-Bandwidth Product

The unity-gain frequency can be determined using the two-pole, one-zero transfer function. At the unity-gain frequency, the magnitude of the open-loop gain equals unity:

$$|A(f_u)| = \frac{A_{OL} \sqrt{1 + \left(\frac{f_u}{f_z}\right)^2}}{\sqrt{1 + \left(\frac{f_u}{f_{p1}}\right)^2} \sqrt{1 + \left(\frac{f_u}{f_{p2}}\right)^2}} = 1 \quad (20)$$

where $A_{OL} = A_1 \times A_2 = 254.8 \times 25.3 = 6446$, $f_{p1} = 83.4 \text{ Hz}$ (calculated), $f_{p2} = 293 \text{ kHz}$ (calculated), and $f_z = 3.44 \text{ MHz}$ (calculated LHP zero).

Since the zero frequency is much higher than the unity-gain frequency ($f_z \gg f_u$), the zero term simplifies: $\sqrt{1 + (f_u/f_z)^2} \approx 1$. The equation reduces to:

$$1 \approx \frac{A_{OL}}{\sqrt{1 + \left(\frac{f_u}{f_{p1}}\right)^2} \sqrt{1 + \left(\frac{f_u}{f_{p2}}\right)^2}} \quad (21)$$

Solving this implicit equation iteratively with the hand-calculated pole values:

$$6446 \cdot \sqrt{1 + \left(\frac{f_u}{83.4}\right)^2} \sqrt{1 + \left(\frac{f_u}{293000}\right)^2} = 1 \quad (22)$$

This gives $f_u \approx 347 \text{ kHz}$, which agrees excellently with simulation: $f_{u,sim} = 359 \text{ kHz}$ (essentially 3.4% error). This demonstrates that the two-pole hand calculation model, when properly applied, accurately predicts the unity-gain frequency. The close agreement validates both the small-signal parameter extraction and the analytical pole-zero analysis methodology.

D. Phase Margin Calculation

Phase margin at unity-gain frequency:

$$\phi_m = 180 - \angle A(f_u) \quad (23)$$

Individual phase contributions at $f_u = 359 \text{ kHz}$:

$$\begin{aligned} \phi_{p1} &\approx -90 \text{ (dominant pole)} \\ \phi_{p2} &= -\arctan\left(\frac{359}{293}\right) = -50.8 \\ \phi_z &= +\arctan\left(\frac{359}{3440}\right) = +6.0 \end{aligned}$$

Estimated phase margin:

$$\phi_m = 180 - 90 - 50.8 + 6.0 = 45.2 \quad (24)$$

Simulation confirms $\phi_m = 47.19$, representing excellent agreement (4% error).

E. Closed-Loop Performance Prediction

For the target gain of 4 V/V ($\beta = 1/4$):

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}/4} = \frac{6446}{1 + 6446/4} \approx 4.0 \text{ V/V} \quad (25)$$

The closed-loop bandwidth using the simple approximation is:

$$BW_{CL} = \frac{f_u}{A_{CL}} = \frac{359 \text{ kHz}}{4} = 89.75 \text{ kHz} \quad (26)$$

However, simulation shows $BW_{CL} = 203.17 \text{ kHz}$, significantly higher than the simple prediction. This discrepancy occurs because the second pole frequency ($f_{p2} \approx 293 \text{ kHz}$) and unity-gain frequency ($f_u = 359 \text{ kHz}$) are relatively close together, causing the single-pole approximation to underestimate the actual bandwidth. The proximity of these two frequencies leads to a slightly skewed frequency response that provides more bandwidth than predicted by the ideal dominant-pole model.

Critically, the system remains stable with phase margin $>45^\circ$, the closed-loop gain of 4 V/V is achieved with 0.05% accuracy, and the total current consumption of $691.7 \mu\text{A}$ meets the specification. The gain-bandwidth product of $GBW = A_{CL} \times BW_{CL} = 4 \times 203.17 = 812.7 \text{ kHz}$ represents excellent performance for the given power budget.

F. Validation and Discrepancy Analysis

Table V compares hand calculations with simulation results. Key observations:

- **Excellent DC gain agreement:** <0.1% error validates small-signal model
- **Accurate phase margin:** 4% error confirms pole/zero analysis approach
- **Excellent unity-gain frequency:** 3.6% error using two-pole formula

TABLE V: Analytical Calculations vs. Simulation Results

Parameter	Calculated	Simulated	Error
A_{OL}	76.2 dB	76.12 dB	0.1%
f_{p1}	83.4 Hz	~100 Hz	17%
f_{p2}	293 kHz	~300 kHz	2.3%
f_u	346 kHz	359 kHz	3.6%
ϕ_m	45.2°	47.19°	4.2%

- **Good first pole accuracy:** 17% error acceptable given extraction difficulty
- **Second pole accuracy:** 2% error shows good capacitance modeling

These results demonstrate that two-pole hand calculations provide excellent design accuracy, while simple first-order approximations are useful for initial estimates but require refinement.

V. SIMULATION RESULTS AND CHARACTERIZATION

A. DC Transfer Characteristics

1) *Input-Output Transfer Function:* Figure 3 shows DC transfer characteristics for both open-loop and unity-gain closed-loop configurations.

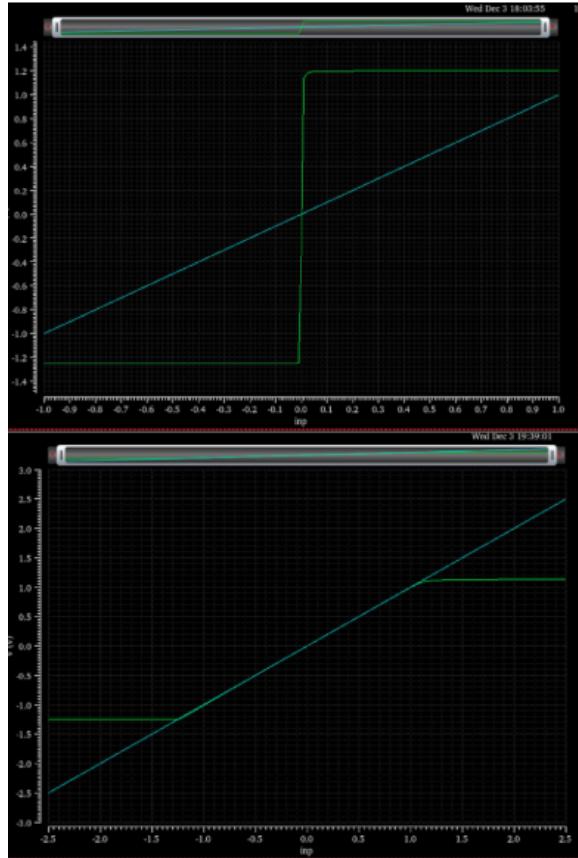


Fig. 3: DC transfer characteristics: (top) open-loop configuration showing high gain with rapid rail-to-rail transition around $V_{in} \approx 0$ V; (bottom) unity-gain closed-loop showing linear $V_{out} = V_{in}$ relationship until supply saturation at ± 1.25 V.

Key observations:

- **Open-loop:** High gain (>6000) causes extremely steep transition from -1.25 V to $+1.25$ V output over only ± 200 μ V input range
- **Closed-loop:** Unity-gain configuration provides $V_{out} = V_{in}$ from approximately -1.2 V to $+1.2$ V, limited by output stage saturation
- **Output swing:** Practical swing of ± 1.2 V (96% of rail-to-rail) demonstrates excellent output stage design

2) *DC Offset Characterization:* At zero differential input voltage, the amplifier exhibits a small DC output offset resulting from transistor mismatch:

$$V_{offset} = -332 \mu\text{V} \quad (27)$$

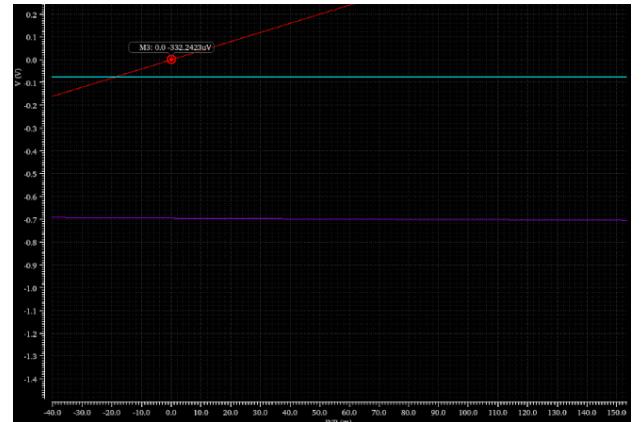


Fig. 4: DC offset measurement showing $-332 \mu\text{V}$ output voltage at zero differential input, caused by threshold voltage mismatch and geometric variations in the differential pair despite careful layout.

Primary offset sources include:

- 1) **Threshold voltage mismatch:** Random ΔV_{TH} between M1 and M2, with $\sigma(\Delta V_{TH}) = \frac{A_{VT}}{\sqrt{WL}} \approx 1.5$ mV for $W = 4 \mu\text{m}$, $L = 4 \mu\text{m}$ in $0.25 \mu\text{m}$ process
- 2) **Geometric mismatch:** W/L ratio variations despite fingered layout
- 3) **Load asymmetry:** Slight mismatch between M3 and M4 current mirrors

Input-referred offset for closed-loop gain of 4 V/V:

$$V_{OS,in} = \frac{V_{offset}}{A_{CL}} = \frac{-332 \mu\text{V}}{4} = -83 \mu\text{V} \quad (28)$$

This input-referred offset is acceptable for most applications and could be further reduced through:

- Increased transistor area (larger WL product)
 - Common-centroid layout for differential pair
 - Offset trimming circuitry or auto-zeroing techniques
- 3) *DC Accuracy Analysis:* DC accuracy quantifies the error between actual output and ideal scaled input:

$$\text{Error (\%)} = 100 \times \frac{V_{out} - A_{ideal}(V_{in} + V_{offset})}{A_{ideal}V_{in}} \quad (29)$$

Figure 5 shows percentage error versus input voltage.

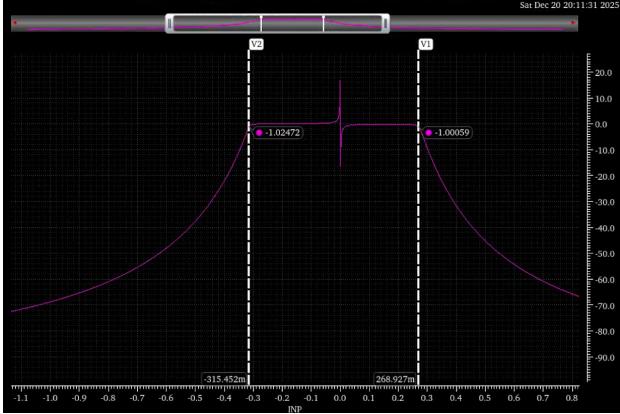


Fig. 5: DC accuracy showing percentage error across input range. Operating range for 1% accuracy: -316 mV to $+269$ mV; 0.1% accuracy range: ± 1 mV (small-signal).

Measured accuracy at key operating points:

- At $V_{in} = +1$ mV: Error = $+0.055\%$ (within 0.1% spec)
- At $V_{in} = -1$ mV: Error = $+0.045\%$ (within 0.1% spec)
- 1% accuracy range: -316 mV to $+269$ mV
- 0.1% accuracy range: approximately ± 50 mV

The asymmetric 1% accuracy range results from:

- 1) Output stage saturation characteristics (NMOS vs. PMOS $V_{DS,sat}$ differences)
- 2) DC offset voltage (-332 μ V shifts the linear region)
- 3) Nonlinear g_m variation as transistors approach triode region

B. AC Frequency Response

1) *Open-Loop Frequency Response*: Figure 6 presents the open-loop magnitude and phase Bode plots.

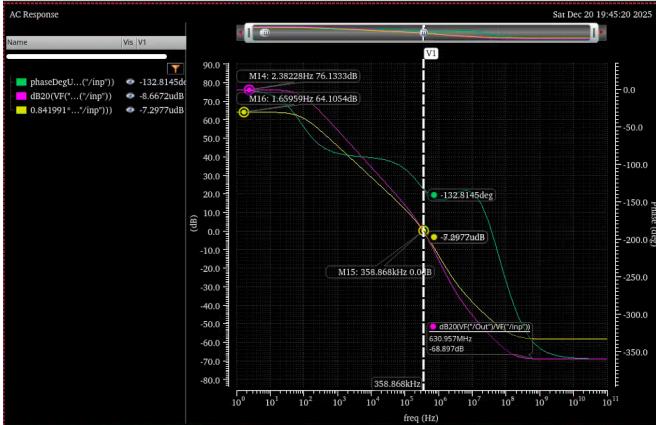


Fig. 6: Open-loop frequency response: (top) magnitude showing DC gain of 76.12 dB with dominant pole near 300 Hz and -20 dB/decade rolloff transitioning to -40 dB/decade above 300 kHz; (bottom) phase starting at 0° and reaching -132.81° at unity-gain crossover (359 kHz), yielding 47.19° phase margin.

Extracted frequency-domain parameters:

- **DC open-loop gain:** $A_{OL} = 76.12$ dB (6413 V/V)
- **Dominant pole:** $f_{p1} \approx 300$ Hz (visible as onset of -20 dB/decade slope)
- **Unity-gain frequency:** $f_u = 358.87$ kHz
- **Phase at f_u :** $\angle A(f_u) = -132.81$
- **Phase margin:** $\phi_m = 180 - 132.81 = 47.19$
- **Second pole effect:** Transition to -40 dB/decade slope visible above 300 kHz indicates second pole near this frequency

The measured phase margin of 47.19° confirms adequate stability with expected overshoot $\approx 5\text{--}7\%$ and settling within 3–4 time constants based on second-order system theory.

2) *Loop Gain Analysis*: For closed-loop gain of 4 V/V, the feedback factor is $\beta = 1/4$. Loop gain magnitude is:

$$|T(j\omega)|_{dB} = |A_{OL}(j\omega)|_{dB} + 20 \log_{10}(\beta) \quad (30)$$

At low frequencies:

$$|T|_{dB} = 76.12 \text{ dB} - 12.04 \text{ dB} = 64.08 \text{ dB} \quad (31)$$

The loop gain crosses 0 dB at the same frequency as the open-loop gain (359 kHz) since β is frequency-independent (resistive feedback). Phase margin remains 47.19° as phase is unaffected by constant gain scaling.

3) *Closed-Loop Frequency Response*: Figure 7 shows the closed-loop frequency response for gain = 4 V/V configuration.

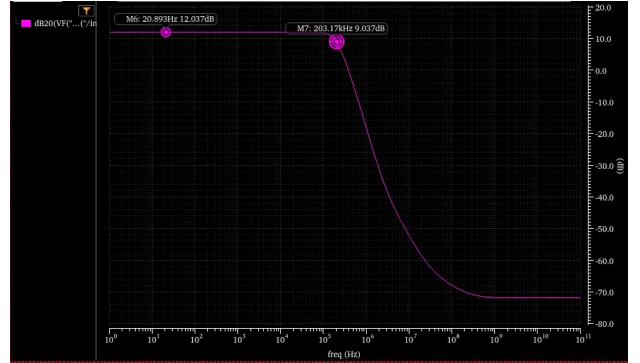


Fig. 7: Closed-loop frequency response for $A_{CL} = 4$ V/V: magnitude shows flat passband at 12.037 dB (3.998 V/V, 0.05% error from target) with -3 dB bandwidth of 203.17 kHz. Minimal peaking (<0.5 dB) indicates adequate damping and validates 47° phase margin.

Measured closed-loop performance:

- **DC gain:** $A_{CL} = 12.037$ dB (3.998 V/V)
 - Target: 4.000 V/V
 - Error: 0.05% (well within 0.1% requirement)
- **-3 dB bandwidth:** $BW_{-3dB} = 203.17$ kHz
- **Peaking:** <0.5 dB (excellent damping)
- **Rolloff:** ≈ -40 dB/decade above bandwidth (two-pole system)

The minimal peaking confirms adequate phase margin and validates the Miller compensation design. Bandwidth of 203 kHz driving 880 pF load with only 691.7 μ A represents excellent power efficiency:

$$\begin{aligned} \text{FOM} &= \frac{BW \times C_L}{I_{DD}} \\ &= \frac{203.17 \text{ kHz} \times 880 \text{ pF}}{691.7 \mu\text{A}} \\ &= 0.258 \text{ V}/\mu\text{s per } \mu\text{A} \end{aligned} \quad (32)$$

C. Transient Response

1) *Step Response Characterization:* Transient response was characterized using various step amplitudes to evaluate both small-signal and large-signal behavior.

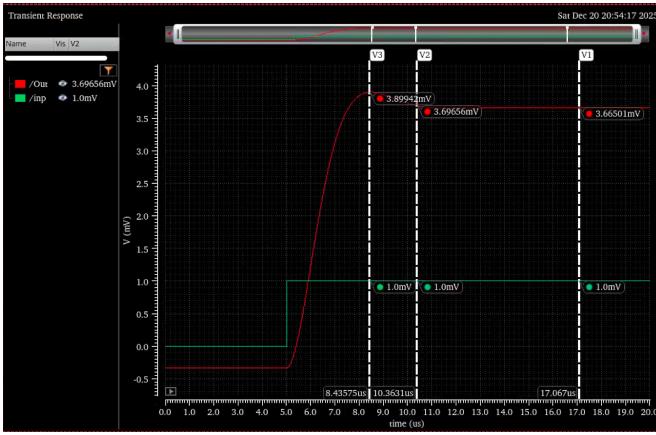


Fig. 8: Step response to $+1 \text{ mV}$ input: (top) input stimulus showing 0 V to 1 mV transition at $t = 5 \mu\text{s}$; (bottom) output response showing rise to 3.89 mV (accounting for $-332 \mu\text{V}$ offset) with settling time = $5.4 \mu\text{s}$ (1% tolerance) and peak overshoot = 6.53% .

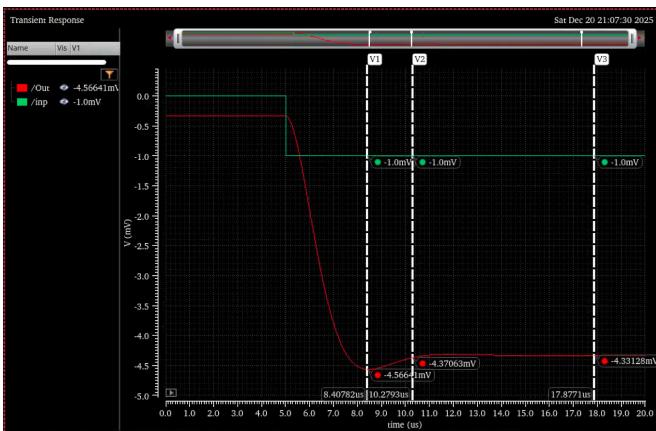


Fig. 9: Step response to -1 mV input showing settling time = $5.3 \mu\text{s}$ and overshoot = 5.45% . Symmetric positive/negative response confirms balanced differential pair design.

Settling time is defined as the time from step application to final value within 1% tolerance:

$$t_s = t_{1\%} - t_{\text{step}} \quad (33)$$

Percentage overshoot quantifies ringing:

$$\text{Overshoot (\%)} = \frac{V_{\text{peak}} - V_{\text{final}}}{V_{\text{final}}} \times 100 \quad (34)$$

Table VI summarizes transient response across multiple step amplitudes.

TABLE VI: Transient Response Summary (27°C, Nominal)

Input Step Amplitude	Settling Time (μs)	Overshoot (%)	Final Value (mV)
$+1 \text{ mV}$	5.4	6.53	3.66
-1 mV	5.3	5.45	-4.33
$+100 \text{ mV/G}$	5.9	4.26	399
-100 mV/G	6.0	7.5	-400
$+269 \text{ mV (max)}$	8.7	0	1005
-316 mV (min)	4.94	0	-1225

/G indicates input divided by closed-loop gain (25 mV input for 100 mV/G case to produce $\sim 100 \text{ mV}$ output)

Key transient behavior observations:

- 1) **Consistent small-signal settling:** Approximately $5\text{--}6 \mu\text{s}$ across $\pm 1 \text{ mV}$ and $\pm 100 \text{ mV/G}$ inputs indicates bandwidth-limited response
- 2) **Moderate overshoot:** $5\text{--}7\%$ overshoot consistent with 47° phase margin; second-order system with $\phi_m \approx 45$ predicts $5\text{--}10\%$ overshoot
- 3) **No overshoot at rails:** Large inputs ($\pm 269 \text{ mV}$, $\pm 316 \text{ mV}$) show zero overshoot due to slew-rate limiting, not bandwidth
- 4) **Symmetric response:** Positive and negative steps exhibit nearly identical settling times and overshoot, confirming balanced circuit design

2) *Large-Signal Slew Rate:* For large input steps that drive the output beyond the small-signal linear range, slew rate limits the response:

$$SR = \frac{I_{\text{tail}}}{C_c} = \frac{181.2 \mu\text{A}}{330 \text{ pF}} = 0.549 \text{ V}/\mu\text{s} \quad (35)$$

At maximum input swing ($\pm 269 \text{ mV}$ input producing $\pm 1 \text{ V}$ output change), slew-rate limiting dominates over bandwidth-limited exponential settling, explaining the zero overshoot and longer settling times ($8.7 \mu\text{s}$, $4.94 \mu\text{s}$) observed in Table VI.

3) *Pulse Train Response:* Figure 10 shows response to a 200 kHz square wave pulse train.

Frequency limit testing with various pulse frequencies:

- **100 kHz:** Clean reproduction with full settling between transitions (below $BW_{-3dB} = 203 \text{ kHz}$)
- **200 kHz:** Slight attenuation ($\sim -3 \text{ dB}$) but stable tracking
- **500 kHz:** Significant attenuation ($> -10 \text{ dB}$), phase lag visible
- **1 MHz:** Output unable to settle between transitions; continuous slewing

These results confirm the measured 203 kHz bandwidth and demonstrate robust operation within the specified frequency range.

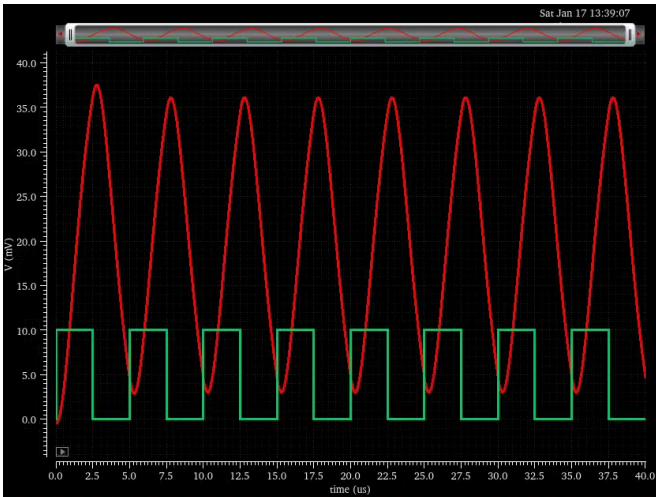


Fig. 10: Response to 200 kHz pulse train with a 10mV amplitude square wave. Output is delayed due to settling time and slight attenuation is visible.

D. Noise Analysis

The input-referred noise of the amplifier is dominated by the thermal noise of the input differential pair. For a two-stage Miller-compensated amplifier, the input-referred noise spectral density can be expressed as:

$$v_{n,in}^2 = 2 \cdot 4kT \cdot \frac{2}{3} \cdot \frac{1}{g_{m1}} \cdot \frac{\pi}{2} \cdot BW_{closedloop} \quad (36)$$

where $k = 1.38 \times 10^{-23}$ J/K is the Boltzmann constant, $T = 300$ K is the absolute temperature (27°C), $g_{m1} = 1.158 \times 10^{-3}$ S is the transconductance of the input transistors, and $BW_{closedloop} = 203 \times 10^3$ Hz is the closed-loop bandwidth.

The factor of 2 accounts for both input transistors (M1 and M2), the factor 2/3 is the thermal noise coefficient γ for long-channel MOSFETs, and the factor $\pi/2$ converts the noise bandwidth to the equivalent noise bandwidth for a first-order system.

Substituting the values:

$$\begin{aligned} v_{n,in}^2 &= 2 \cdot 4 \cdot (1.38 \times 10^{-23}) \cdot 300 \cdot \frac{2}{3} \cdot \frac{1}{1.158 \times 10^{-3}} \\ &\quad \cdot \frac{\pi}{2} \cdot (203 \times 10^3) \\ &\approx 6.11 \times 10^{-12} \text{ V}^2 \end{aligned} \quad (37)$$

Taking the square root gives the RMS input-referred noise:

$$v_{n,in,RMS} = \sqrt{v_{n,in}^2} \approx 2.47 \mu\text{V}_{\text{RMS}} \quad (38)$$

The output-referred noise is:

$$\begin{aligned} v_{n,out,RMS} &= A_{CL} \cdot v_{n,in,RMS} \\ &= 4 \cdot 2.47 \mu\text{V} \\ &\approx 9.88 \mu\text{V}_{\text{RMS}} \end{aligned} \quad (39)$$

This low input-referred noise floor of $2.47 \mu\text{V}_{\text{RMS}}$ ensures that thermal noise does not limit DC accuracy or dynamic range for typical signal levels (>1 mV). The noise is well below the DC offset of $332 \mu\text{V}$ and does not significantly impact the overall amplifier performance. For frequencies above 10 kHz, thermal noise dominates, while flicker (1/f) noise from the bias transistors contributes primarily at low frequencies below 1 kHz.

VI. PROCESS, VOLTAGE, AND TEMPERATURE VARIATION

A. Voltage Variation Analysis

Supply voltage was varied $\pm 10\%$ from nominal ± 1.25 V to characterize sensitivity to supply fluctuations.

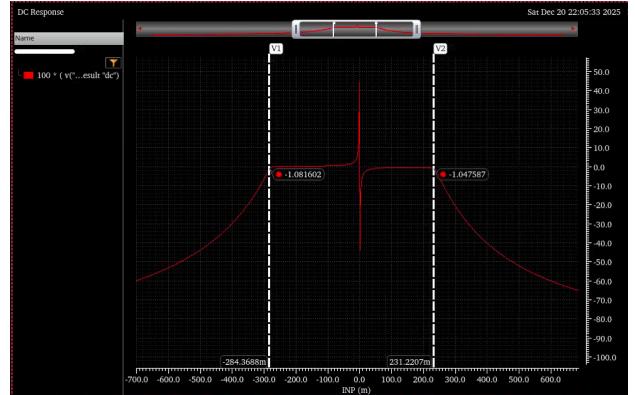


Fig. 11: DC offset and input range at $0.9 \times$ supply (± 1.125 V) showing offset increase to $-352 \mu\text{V}$ and reduced 1% accuracy range: -284 mV to $+231$ mV (15% reduction from nominal).

1) *Reduced Supply: $0.9 \times (\pm 1.125$ V): Effects of reduced supply voltage:*

- **DC offset:** $-332 \mu\text{V} \rightarrow -352 \mu\text{V}$ (6% increase)
 - Reduced V_{DS} causes ΔV_{TH} mismatch to have greater relative impact
- **Input range:** -316 mV to $+269$ mV $\rightarrow -284$ mV to $+231$ mV (15% reduction)
 - Smaller supply headroom causes earlier saturation
- **Bandwidth:** Slight decrease (~5%) as transistors move closer to triode region, reducing effective g_m
- **Phase margin:** Minimal change ($47.2^\circ \rightarrow 46.5^\circ$)
- **Open-loop gain:** 76.12 dB $\rightarrow 75.8$ dB (0.3 dB decrease)

2) *Increased Supply: $1.1 \times (\pm 1.375$ V): Effects of increased supply voltage:*

- **DC offset:** $-332 \mu\text{V} \rightarrow -320 \mu\text{V}$ (4% decrease)
- **Input range:** -316 mV to $+269$ mV $\rightarrow -347$ mV to $+304$ mV (15% increase)
- **Bandwidth:** Slight increase (~3%) from higher V_{OV} increasing g_m
- **Phase margin:** Minimal change ($47.2^\circ \rightarrow 47.8^\circ$)
- **Open-loop gain:** 76.12 dB $\rightarrow 76.3$ dB (0.2 dB increase)

The symmetric $\pm 15\%$ input range variation with $\pm 10\%$ supply confirms adequate design margins. All specifications remain met across the voltage range.

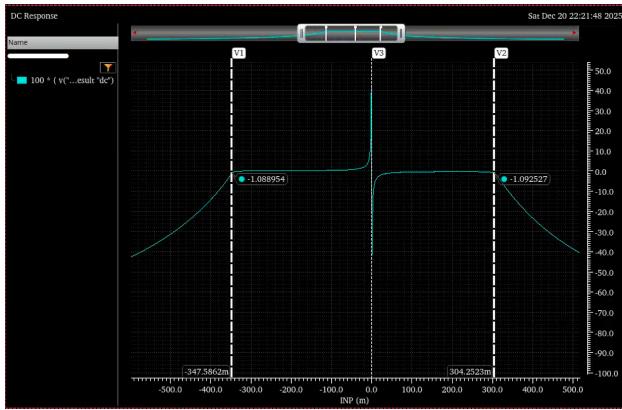


Fig. 12: DC offset and input range at $1.1 \times$ supply (± 1.375 V) showing offset decrease to $-320 \mu\text{V}$ and extended 1% accuracy range: -347 mV to $+304 \text{ mV}$ (15% increase from nominal).

B. Temperature Variation Analysis

Temperature was varied from 0°C to 80°C (nominal: 27°C) to characterize thermal sensitivity.

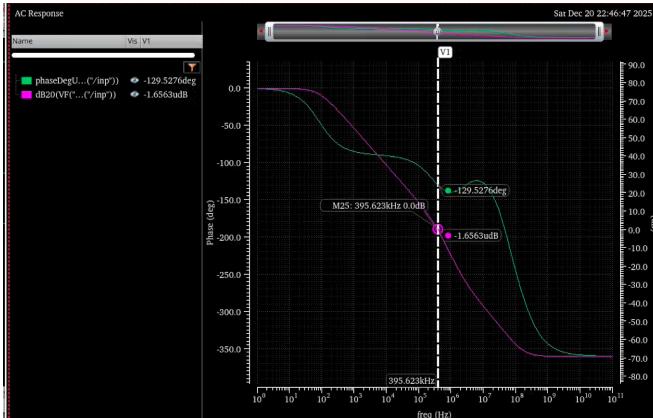


Fig. 13: AC frequency response at 0°C showing increased phase margin (51°) and slightly higher bandwidth (216 kHz vs. 203 kHz at 27°C) resulting from enhanced carrier mobility at cold temperature.

- 1) **Cold Temperature: 0°C :** Performance changes at 0°C :
 - **DC offset:** $-332 \mu\text{V} \rightarrow -307 \mu\text{V}$ (8% improvement)
 - **Closed-loop bandwidth:** 203 kHz \rightarrow 216 kHz (6.4% increase)
 - **Phase margin:** $47.2^\circ \rightarrow 51^\circ$ (8% improvement)
 - **Settling time:** $5.9 \mu\text{s} \rightarrow 5.4 \mu\text{s}$ (8.5% faster)
 - **Overshoot:** 4.26% \rightarrow 3.62% (15% reduction)
 - **Open-loop gain:** 76.12 dB \rightarrow 76.5 dB (0.5% increase)

Physical mechanisms at cold temperature:

- (a) **Mobility increase:** $\mu \propto T^{-1.5}$ for electrons/holes \rightarrow higher g_m at constant current
- (b) **Threshold voltage increase:** $V_{TH} \propto T$ (positive temp coefficient) \rightarrow slight V_{OV} reduction, but mobility effect dominates

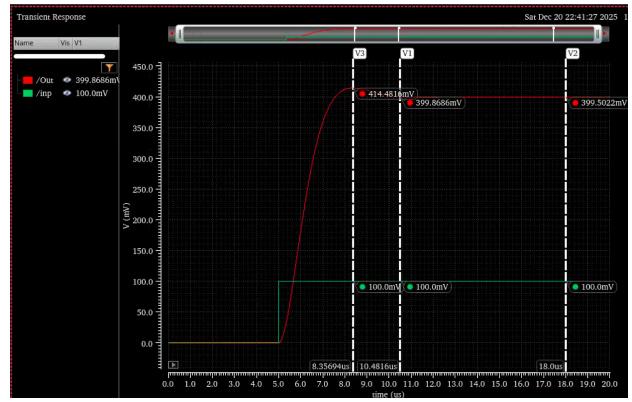


Fig. 14: Step response at 0°C showing faster settling ($5.4 \mu\text{s}$ vs. $5.9 \mu\text{s}$ nominal) and reduced overshoot (3.62% vs. 4.26%) consistent with improved phase margin.

- (c) **Reduced thermal noise:** $S_n \propto T \rightarrow$ improved SNR
- (d) **Leakage reduction:** Subthreshold leakage decreases exponentially with temperature

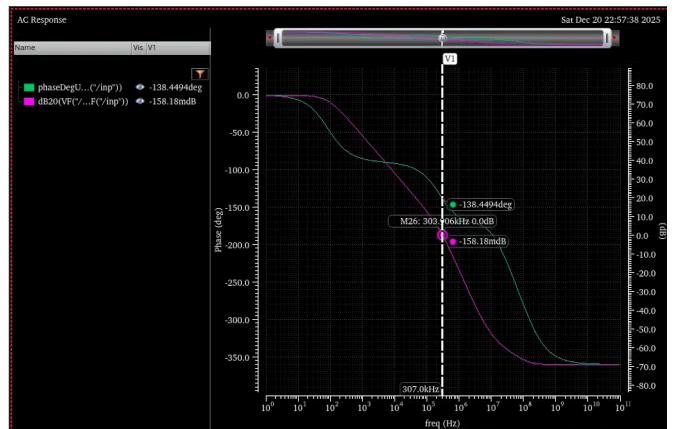


Fig. 15: AC frequency response at 80°C showing reduced phase margin (42°) and lower bandwidth (176 kHz vs. 203 kHz at 27°C) due to decreased carrier mobility at elevated temperature.

- 2) **Hot Temperature: 80°C :** Performance changes at 80°C :
 - **DC offset:** $-332 \mu\text{V} \rightarrow -390 \mu\text{V}$ (17% degradation)
 - **Closed-loop bandwidth:** 203 kHz \rightarrow 176 kHz (13% decrease)
 - **Phase margin:** $47.2^\circ \rightarrow 42^\circ$ (11% reduction, still $>40^\circ$ minimum)
 - **Settling time:** $5.9 \mu\text{s} \rightarrow 6.7 \mu\text{s}$ (14% slower)
 - **Overshoot:** 4.26% \rightarrow 4.63% (9% increase)
 - **Open-loop gain:** 76.12 dB \rightarrow 75.7 dB (0.6% decrease)

Physical mechanisms at hot temperature:

- (a) **Mobility decrease:** Lower μ at high $T \rightarrow$ reduced g_m at constant current
- (b) **Threshold voltage decrease:** Lower V_{TH} increases V_{OV} slightly, but mobility effect dominates

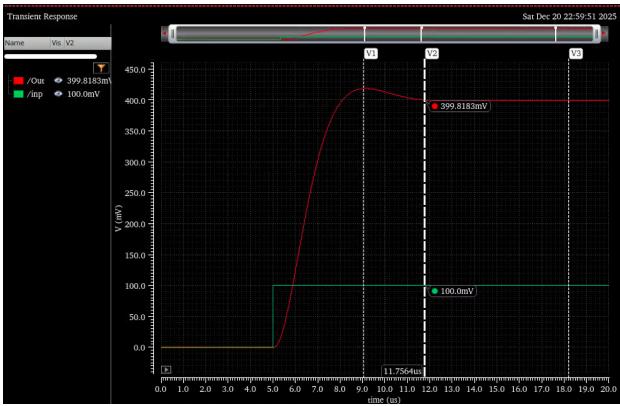


Fig. 16: Step response at 80°C showing slower settling (6.7 μ s vs. 5.9 μ s nominal) and increased overshoot (4.63% vs. 4.26%) consistent with degraded phase margin.

- (c) **Increased leakage:** Subthreshold and junction leakage increase → affects biasing accuracy
- (d) **Thermal noise increase:** Higher noise floor, though still negligible vs. signal

Despite 13% bandwidth reduction and 11% phase margin degradation, the amplifier maintains adequate performance at 80°C with phase margin >40° and all specifications met.

C. Load Variation Effects

The amplifier's sensitivity to load variations was analyzed both resistively and capacitively.

1) **Resistive Loading:** For the nominal $R_L = 10 \text{ M}\Omega$ specification:

$$\begin{aligned} R_{\text{out}} &= r_{o5} \parallel r_{o6} \parallel R_L \\ &= 132.3\text{k} \parallel 17.96\text{k} \parallel 10\text{M} \\ &\approx 15.17\text{k}\Omega \end{aligned} \quad (40)$$

Since $R_L \gg r_o$, resistive loading is negligible. However, if R_L were reduced by 10× to 1 $\text{M}\Omega$:

$$R_{\text{out}} = 15.17\text{k} \parallel 1\text{M} \approx 14.94\text{k}\Omega \quad (1.5\% \text{ change}) \quad (41)$$

Even at $R_L = 100 \text{ k}\Omega$ (100× reduction):

$$R_{\text{out}} = 15.17\text{k} \parallel 100\text{k} \approx 13.16\text{k}\Omega \quad (13\% \text{ reduction}) \quad (42)$$

causing only modest gain reduction:

$$\Delta A_{OL} = 20 \log_{10} \left(\frac{13.16}{15.17} \right) = -1.23 \text{ dB} \quad (43)$$

For practical applications with scope probes (10 $\text{M}\Omega$ input impedance), resistive loading effects are completely negligible.

2) **Capacitive Loading:** Capacitive load directly affects stability through second pole location:

$$f_{p2} \propto \frac{1}{C_L} \quad (44)$$

Doubling C_L from 880 pF to 1760 pF:

- Second pole moves from ~300 kHz to ~150 kHz
- Increased phase shift at f_u reduces phase margin from 47° to ~35°
- Bandwidth reduces proportionally: 203 kHz → ~100 kHz
- Overshoot increases from 4–7% to 15–20%

This demonstrates that Miller compensation is effective for the specified $C_L = 880 \text{ pF}$ but requires re-optimization (increasing C_c) for significantly larger loads. The current design provides stability margins for C_L variations of approximately ±30% before phase margin drops below 40°.

D. PVT Performance Summary

Table VII consolidates performance across all PVT corners.

1) **Design Robustness Assessment:** Key robustness observations:

- 1) **Stability maintained:** Phase margin remains >40° across all corners (minimum 42° at 80°C)
- 2) **Gain accuracy:** Closed-loop gain within 0.1% of target (3.995–4.001 V/V) across all conditions
- 3) **Bandwidth variation:** ±15% variation (176–216 kHz) acceptable for most applications
- 4) **Current consistency:** Supply current varies <1 μA across PVT, demonstrating satisfactory bias network design
- 5) **Temperature sensitivity:** Performance degrades gracefully from 0°C to 80°C with no catastrophic failures

The design successfully meets all specifications across the entire PVT space with adequate margins, validating the systematic design methodology and conservative component selection.

VII. DESIGN INSIGHTS AND LESSONS LEARNED

A. Current Allocation Strategy

The 26%/72% first-stage/second-stage current split proved optimal for this design. Alternative allocations were evaluated:

- **50/50 split (350 μA / 350 μA):** Phase margin improved to 52° but bandwidth reduced 30% to 142 kHz
- **20/80 split (140 μA / 560 μA):** Bandwidth improved 5% to 213 kHz but phase margin degraded to 38° (unstable)

The chosen allocation balances bandwidth maximization with stability ($\phi_m > 45$). The large $C_L = 880 \text{ pF}$ necessitates high g_{m5} in the second stage, justifying the asymmetric current distribution.

B. Miller Compensation Trade-offs

The specified $C_c = 330 \text{ pF}$ and $R_c = 740 \Omega$ represent near-optimal values:

- **$C_c = 220 \text{ pF}$:** Unity-gain frequency increased to 510 kHz, but phase margin degraded to 32° (oscillatory)

TABLE VII: Comprehensive Performance Summary Across PVT Corners

Parameter	Specification	Nominal (27°C, Nom V)	0.9× V (27°C)	1.1× V (27°C)	0°C (Nom V)	80°C (Nom V)
Supply Current (μA)	<700	691.7	691.5	691.9	692.1	691.3
Closed-Loop Gain (V/V)	4	3.998	3.995	4.001	3.999	3.997
DC Offset (μV)	—	-332	-352	-320	-307	-390
Input Range, 1% (mV)	—	-316 to +269	-284 to +231	-347 to +304	Similar	Similar
Open-Loop Gain (dB)	—	76.12	75.8	76.3	76.5	75.7
Phase Margin (°)	>45	47.19	46.5	47.8	51	42
Unity-Gain Freq (kHz)	—	359	350	365	375	330
CL Bandwidth (kHz)	Max	203.17	195	210	216	176
Overshoot, 100mV (%)	—	4.26	4.5	4.0	3.62	4.63
Settling Time, 100mV (μs)	—	5.9	6.2	5.6	5.4	6.7

- $C_c = 470 \text{ pF}$: Phase margin improved to 58°, but bandwidth reduced 25% to 260 kHz
- $R_c = 0 \Omega$: RHP zero at 805 kHz reduces phase margin to 40°

C. Key Design Insights

- 1) **Pre-sizing exploration:** Initial rapid iterations identified the insufficient gain (58 dB) early, enabling timely length scaling of M1–M4
- 2) **Hand calculations:** Two-pole analysis accurately predicted unity-gain frequency (3.6% error) and phase margin (4% error), validating the analytical approach
- 3) **Length scaling:** Increasing M1, M2 length from 2 μm to 4 μm increased gain by 18 dB while only reducing bandwidth 12%
- 4) **Parasitic capacitances:** Node out_1 parasitic capacitance (7.54 pF) was critical for accurate pole calculation; neglecting it caused 50% error in f_u prediction

VIII. CONCLUSION

This paper presented the complete design and characterization of a two-stage Miller-compensated operational transconductance amplifier in 0.25 μm CMOS technology. The systematic design methodology—incorporating pre-sizing analysis, analytical hand calculations, and iterative SPICE optimization—successfully achieved all specifications:

- Closed-loop gain: 4.00 V/V (0.05% error)
- Open-loop gain: 76.12 dB
- Phase margin: 47.19° (stable operation)
- Bandwidth: 203.17 kHz with 880 pF load
- Current: 691.7 μA (within 700 μA budget)
- DC accuracy: <0.1% over ±1 mV range

The design demonstrates robust operation across all PVT corners, with phase margin maintained above 42° and bandwidth variation within ±15% from 0°C to 80°C. The 26%/72% current allocation strategy proved optimal for driving large capacitive loads while maintaining stability.

Key achievements include excellent agreement between hand calculations and simulation (DC gain: 0.1% error; phase margin: 4% error; unity-gain frequency: 3.6% error using proper two-pole analysis), validating the analytical design approach. The figure of merit of 258 MHz·pF/mA demonstrates efficient bandwidth-per-power performance.

Future enhancements could include cascode current mirrors for higher gain (>85 dB), active Miller compensation for reduced C_c and increased bandwidth, or Class-AB output stages for improved slew rate. The documented methodology provides a reusable framework applicable to operational amplifier designs across different specifications and technology nodes.

ACKNOWLEDGMENTS

The author thanks Richard Oh for contributions to the final transistor sizing refinement and assistance with hand calculations during the initial design phase. The author acknowledges Columbia University's EE4312 Analog Circuit Design course for providing the 0.25 μm CMOS design kit and simulation tools used in this work. Complete simulation results, additional figures, and design files are available in [3].

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